Radiation Hardened Product Databook

Space Products Operation

1993

HARRIS SEMICONDUCTOR

$10.00

HARRIS SEMICONDUCTOR

HARRIS SEMICONDUCTOR RADIATION HARDENED PRODUCT DATA BOOK SPACE PRODUCTS OPERATION

Harris Semiconductor has been an industry leader for more than two decades in radiation-hardened circuits which provide high performance and high reliability in severe operating environments. Harris technologies used to achieve radiation hardness include dielectric isolation (DI), Silicon-on-Sapphire (SOS), and Silicon-on-Insulator (SOI). The Harris radiation-hardened products include the CD4000, HCS/HCTS and ACS/ACTS logic families, SRAMs, PROMs, op amps, analog multiplexers, the 80C85/80C86 microprocessor family, analog switches, gate arrays, standard cells and custom devices which provide the system designer with a full complement of products for radiation-hardened systems.

For complete, current and detailed technical specifications on any Harris devices please contact the nearest Harris sales, representative or distributor office see complete worldwide listing in Section 16, page 16-1.

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COVER PHOTO:

The EOS-Earth Observing System Satellite courtesy of the Jet Propulsion Laboratory Pasadena, California

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RAD-HARD HIGH-REL

INTEGRATED CIRCUITS

MILITARY AND AEROSPACE APPLICATIONS

RAD-HARD HIGH REL PRODUCTS
TECHNICAL ASSISTANCE

For technical assistance on the Harris products listed in this databook, please contact the Field Applications Engineering staff available at one of the following Harris Sales Offices:

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RAD HARD 1

GENERAL INFORMATION

ALPHA NUMERIC PRODUCT INDEX

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ALPHA NUMERIC PRODUCT INDEX (Continued)

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RAD HARD 2

DESIGNING FOR RADIATION ENVIRONMENT

Designing for Radiation Environments

Jupiter's trapped radiation belts present a severe total dose environment. Harris rad hard SRAMs continue to operate long after Voyager's journey through those belts.

Semiconductors performing signal processing and control functions are at the heart of today's electronically controlled systems. Many of these systems such as commercial satellites, scientific space probes, and military systems are required to operate in radiation environments of various severity. The designers of these systems must anticipate and account for the effects of the environment on the components used to build them in order to ensure system performance and reliability. Harris Semiconductor has been the leader in the design and production of radiation hardened semiconductors since the early 1960's. Harris offers the rad hard system designer the widest choice of the highest performance hardened semiconductors available anywhere: CD4000 and SOS Logic, epi and SOS memories, microprocessors and peripherals, and analog, interface, and data converter circuits. Harris also has the capability to produce gate arrays and full- or semi-custom analog or digital circuits to round out the options available to the system designer. Harris commitment to the rad hard semiconductor market is illustrated in our development of advanced SOS and SOI fabrication processes; these processes will allow the design of new generations of circuits with hardness and performance levels superior to those obtainable with junction isolated processes.

Unlike many semiconductor manufacturers who produce space capable semiconductors as a sideline, Harris considers radiation hardened space level ICs and discretes to be a core business. Our products and processes are designed, from original concept, to meet the full rigors of radiation environments. When you buy from Harris Semiconductor, you can be assured of receiving radiation hardened products of the highest quality and long term reliability.

Types of Radiation & Effects on Semiconductors

There are several types of radiation with significant effects on semiconductors. The types of radiation encountered in different environments are listed in the table on page 2-4, and their effects on semiconductors are described here.

Total dose is the measure of energy absorbed due to ionizing radiation. Ionizing radiation can be in the form of photons (such as X-rays or gamma rays) or particles (such as electrons or protons). Ionizing radiation, as the name implies, creates electron-hole pairs or ionization in the silicon and insulating materials used to fabricate integrated circuits. When the rate of ionization is low, as it is for a satellite traversing the Van Allen belts, electron-hole pairs produced in silicon are quickly swept away to the circuits's power supply notes, and have negligible effects on circuit operation. In the insulating layers of the circuit, electrons are also swept to the positive supply node. Holes, however, move much more slowly than electrons and tend to become trapped at the silicon/insulator interface. When this trapped charge builds up at the channel of a MOS transistor, the transistor's threshold voltage will shift. Charge that builds up along the silicon surfaces between transistors causes leakage, performance degradation and eventually, functional failure. The amount of total dose received is measured in RADs(Si).

Extremely short, intense bursts of ionizing radiation can also have severe impacts on a circuits's operation. These types of irradiations are commonly referred to as gamma dot or dose rate irradiations (gamma dot refers to the time derivative of gamma dose). The total amount of ionization (total dose) received by a circuit during one of these ionizing pulses can be quite low. In this case, trapped charge at silicon/insulator interfaces will be insufficient to degrade device performance. A large amount of charge produced in the silicon, however, creates a large current pulse as it is swept to the supply nodes. This current pulse can cause momentary output glitches, change the state of a RAM cell or other bistable circuit element, or trigger latchup in non-epitaxial junction isolated circuits. The dose rate level a circuit can withstand is measured in RADs (Si)/s.

Neutron irradiations damage circuits by knocking silicon atoms out of their place in the crystal lattice. While this will severely impact bipolar transistor gains, MOS transistors (and, therefore, CMOS circuits) are not impacted except at extremely high fluence. At these extremely high levels, the accompanying total dose will impact the circuits much more severely than the displacement due to neutrons. Neutron irradiations can cause severe degradation in bipolar circuits due to the reduction in minority carrier lifetimes that result from displacement damage. Neutron fluence is measured in Neutrons/cm^2.

A single, energetic, highly ionizing particle travelling through a memory circuit is known as a single event. As the particle travels through the circuit it leaves an ionized trail. The charge in this trail is collected by nearby circuit modes. Collected charge due to single events can cause momentary changes in output voltages, change the state of a RAM cell or other bistable circuit element, or trigger latchup in a non-epitaxial junction isolated circuit.

Radiation Environments

RELATIVE INTENSITY OF RADIATION TYPES IN VARIOUS ENVIRONMENTS . . .

ENVIRONMENT	TOTAL DOSE	DOSE RATE	NEUTRONS	HEAVY IONS (SINGLE EVENT)
Low Equatorial Earth Orbit	Low	Very Low	None	Low
Low Polar Earth Orbit	Moderate	Very Low	None	Moderate
Geosynchronous Earth Orbit	Moderate	Very Low	None	High
Deep Space	Moderate-High	Very Low	None	High

. . . AND IN VARIOUS APPLICATIONS

APPLICATION	TOTAL DOSE	DOSE RATE	NEUTRONS	HEAVY IONS (SINGLE EVENT)
Tactical Weapons	Low	High	Low	None
Strategic Weapons	Very High	Very High	Very High	Moderate
SDI	Very High	Very High	Very High	High
Reactor Instruments	Very High	Moderate	Very High	None

Producing Rad Hard ICs

There are three factors that are essential for the production of radiation hardened ICs process design and control, circuit design, and hardness assurance. By far the most important of these factors is process design and control. Harris has developed several different process technologies to provide the levels of hardness necessary for the harsh environments in which modern electronic systems operate.

Harris 4K and 16K SRAMs, 16K fuse link PROM, and CD4000 family and microprocessor family are fabricated on hardened field epitaxial junction isolated processes. Special low temperature gate and field oxide processing steps and other proprietary processing techniques are used to minimize the generation and trapping of charge that results in circuit degradation with accumulated total dose. The optimized epitaxial layer thickness prevents latchup due to high dose rate irradiations or high LET single events.

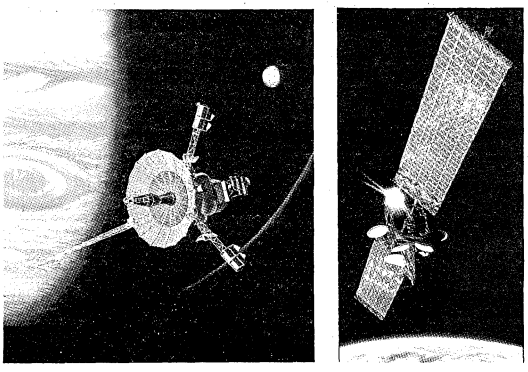
Dielectrically isolated (DI) CMOS technology is used to fabricate Harris' rad hard MUXs and switches; bipolar DI is used for the rad hard op amps and 24XRH line drivers and receivers. These DI processes eliminate the possibility of latchup, and hardened gate and field oxides provide excellent total dose hardness.

Harris 64K RAMs (HS-65643RH and HS-65647RH) and the HCS/HCTS and ACS/ACTS logic families are produced on a 1.2μm silicon on sapphire (SOS) process. This process provides high levels of total dose immunity and extreme single event upset immunity. Since this is an insulation isolated process, latchup is not possible under any condition. Another advantage of the insulation isolation processes is the elimination of the capacitances associated with the reverse biased junctions used for isolation in a JI process. The elimination of these capacitances increases circuit speed significantly.

The next generation of digital radiation hardened processes are now in development at Harris. A submicron silicon on insulator (SOI) process using implanted oxygen to form the isolation layer will be used to build Harris' 256K Rad Hard SRAMs and future digital circuits. This process will give these circuits excellent hardness and speed. Access and read/write cycle times for the 256K SRAM are 35ns guaranteed over specified temperature, supply voltage, and radiation exposure. This insulation isolation process also prevents latchup under any conditions.

The processes used to fabricate hardened ICs are designed to minimize the effects of radiation on device, and therefore circuit, operation. Conversely, circuit designs are optimized to provide the maximum tolerance to the device level effects. An example of a circuit hardening technique is the use of Miller capacitors in Harris' 64K bit SRAM cells. These capacitors significantly increase the amount of deposited charge necessary to cause upset, making the circuits much less susceptible to single events.

Finally, a hardness assurance program must be in place to ensure the processes used are in control. Hardness assurance at Harris takes place primarily by SPC (Statistical Process Control) of the wafer fabrication, assembly, and test processes. End of line testing is also performed (e.g. Method 1019 compliant testing for total dose hardness), but the emphasis at Harris is on process control. QML (Qualified Manufacturer's List) hardness assurance techniques are currently in place for the wafer fabrication processes, and are being implemented in assembly and test.



In deep space or Earth orbit, Harris rad hard circuits perform reliably for years.

RAD HARD 3

MULTIPLEXERS AND SWITCHES

HARRIS SEMICONDUCTOR

HS-508ARH/883S

Radiation Hardened 8 Channel CMOS Analog Multiplexer with Overvoltage Protection

December 1992

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Radiation Environment
  - Gamma Rate ($\dot{\gamma}$) 1 x 10^8 RAD(Si)/s
  - Gamma Dose (γ) 1 x 10^5 RAD(Si)
- Analog/Digital Overvoltage Protection
- Fail Safe with Power Loss (No Latchup)
- Break-Before-Make Switching
- DTL/TTL and CMOS Compatible
- Analog Signal Range ±15V
- Fast Access Time
- Supply Current at 1MHz Address Toggle (Typ.) 4mA
- Standby Power (Typ.) 7.5mW
- Dielectrically Isolated Device Islands

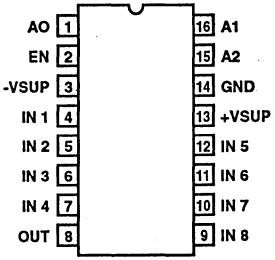
Description

The HS-508ARH/883S is a dielectrically isolated, radiation hardened, CMOS analog multiplexer incorporating an important feature; it withstands analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10V greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important, it can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage current combine to produce low errors. Reference Application Notes 520 and 521, available from the Semiconductor Products Division of Harris, for further information on the HS-508ARH/883S multiplexer in general.

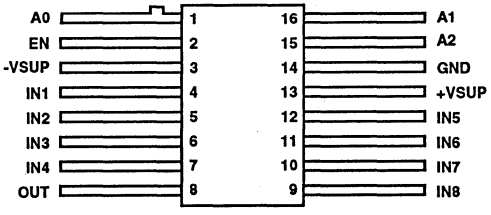
The HS-508ARH/883S has been specifically designed to meet exposure to radiation environments. Operation from -55°C to +125°C is guaranteed.

Pinouts

HS1-508ARH/883S 16 PIN SIDEBRAZE DIP
CASE OUTLINE D-2, COMPLIANT TO MIL-M-38510 PACKAGE
TOP VIEW



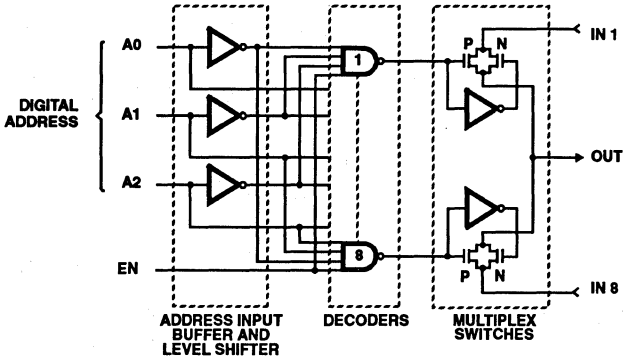
HS9-508ARH/883S 16 PIN FLATPACK
CASE OUTLINE F-5A, COMPLIANT TO MIL-M 38510 PACKAGE
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3021**

Functional Diagram



Truth Table

A2	A1	A0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

Absolute Information

Supply Voltage Between Pins 1 and 27 ..... +40V
+VSUPPLY to Ground ..... +20V
-VSUPPLY to Ground ..... -20V
Analog input Overvoltage:
+VS ..... +VSUPPLY +20V
-VS ..... -VSUPPLY -20V
Digital Input Overvoltage:
+VEN, +VA ..... +VSUPPLY +4V
-VEN, -VA ..... -VSUPPLY -4V
Peak Current, S or D Pulsed at 1ms,
10% Duty Cycle Maximum 40mA
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +275°C

Reliability Information

	θ_{ja}	θ_{jc}
Thermal Resistance		
Sidebraze Package	74.7°C/W	12.1°C/W
Flatpack Package	85.0°C/W	11.1°C/W

Total Power Dissipation 725mW
Gate Count ..... 253 Gates
ESD Classification ..... Class 1

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage (±VSUPPLY) ..... ±15V
Operating Temperature Range ..... -55°C to +125°C
Logic Low Level (VAL) ..... +0.8V
Logic High Level (VAH) ..... +4.0V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested Unless Otherwise Specified: V- = -15V, V+ = +15V, VAH = +4.0V, VAL = 0.8V

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current, Address, or Enable Pins	IAH IAL	Measure Inputs Sequentially Ground All Unused Pins	1, 2, 3	+25°C, +125°C, -55°C	-1000	1000	nA
Leakage Current into the Source Terminal of an "OFF" Switch	+IS(OFF)	VS = +10V, All Unused Inputs and Output = -10V, VEN = 0.8V	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-50	50	nA
	-IS(OFF)	VS = -10V, All Unused Inputs and Output = +10V, VEN =0.8V	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-50	50	nA
Leakage Current into the Drain Terminal of an "OFF" Switch	+ID(OFF)	VD = +10V, VEN = 0.8V. All Unused Inputs = -10V	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-250	250	nA
	-ID(OFF)	VD = -10V, VEN = 0.8V. All Unused Inputs = +10V	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-250	250	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch With Overvoltage Applied	+ID(OFF) Overvoltage	VS =+25V, Measure VD, VEN = 0.8V, All Unused Inputs to GND	1, 2, 3	+25°C, +125°C, -55°C	-2000	2000	nA
	-ID(OFF) Overvoltage	VS = -25V, Measure VD, VEN = 0.8V, All Unused Inputs to GND	1, 2, 3	+25°C, +125°C, -55°C	-2000	2000	nA
Leakage Current from an "ON" Driver into the Switch (Drain & Source)	+ID(On)	VS = VD = +10V, VEN = 4.0V. All Unused Inputs = -10V	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-250	250	nA
	-ID(On)	VS = VD = -10V, VEN = 4.0V. All Unused Inputs = +10V	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-250	250	nA
Analog Signal Range	VS		7, 8A, 8B	+25°C, +125°C, -55°C	-15	+15	V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Guaranteed and 100% Tested Unless Otherwise Specified: V- = -15V, V+ = +15V, VAH = +4.0V, VAL = 0.8V

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch On Resistance	+R(On)	VS = +10V, IOUT = -100µA, VEN = 4.0V	1	+25°C	-	1500	ohms
			1, 2	-55°C, +125°C	-	1800	ohms
	-R(On)	VS = -10V, IOUT = +100µA, VEN = 4.0V	1	+25°C	-	1500	ohms
			1, 2	-55°C, +125°C	-	1800	ohms
Positive Supply Current	I(+)	VEN = 4.0V	1, 2, 3	-55°C, +25°C, +125°C	-	2	mA
Negative Supply Current	I(-)	VEN = 4.0V	1, 2, 3	-55°C, +25°C, +125°C	-1	-	mA
Positive Standby Supply Current	+I(SBY)	VEN = 0.8V	1, 2, 3	-55°C, +25°C,+125°C	-	2	mA
Negative Standby Supply Current	-I(SBY)	VEN = 0.8V	1, 2, 3	-55°C, +25°C, +125°C	-1	-	mA

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested. Unless Otherwise Specified: V- = 15V, V+ = +15V, VAH = +4.0V, VAL = 0.8V

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Break-Before-Make Time Delay	TD	RL = 1000Ω, CL = 50pF	9	+25°C	25	-	ns
			10, 11	-55°C, +125°C	5	-	ns
Propogation Delay Times: Address Inputs to I/O Channels	TOn(A)	RL = 10KΩ, CL = 50pF	9	+25°C	-	600	ns
	TOff(A)		10, 11	-55°C, +125°C	-	1000	ns
Enable to I/O	TOn(EN)	RL = 1000Ω, CL = 50pF	9	+25°C	-	600	ns
	TOff(EN)		10, 11	-55°C, +125°C	-	1000	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: V- = 15V, V+ = +15V, VAH = +4.0V, VAL = 0.8V Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Address Input	CA	VS+ = VS- = 0V, f = 1MHz	1	+25°C	-	7	pF
Capacitance Channel Input	CS(Off)	VS+ = VS- = 0V, f = 1MHz	1	+25°C	-	7	pF
Capacitance Channel Output	CD(Off)	VS+ = VS- = 0V, f = 1MHz	1	+25°C	-	25	pF
Off Isolation	VISO	VEN = 0.8V, f = 200KHz, CL = 7pF, RL = 1KΩ, VS = 3.0VRMS	1, 2	+25°C	45	-	dB

NOTES:

1. The parameters listed in this table are controlled via design or process parameters and not directly tested. These parameters are characterized upon initial design changes which would affect these characteristics.
2. Worst case isolation occurs on channel 4 due to proximity of the output pins.

TABLE 4. POST 100K RAD (si) ELECTRICAL SPECIFICATIONS

Tested, per MIL-STD 883. Unless Otherwise Specified: V- = -15V, V+ = +15V, VAH = +4.5V, VAL= 0.5V

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current, Address,or Enable Pins	IAH	Measure Inputs Sequentially, Ground All Unused Pins	1	+25°C	-1000	1000	nA
	IAL						
Leakage Current Into the Source Terminal of an "OFF" Switch	+IS(OFF)	VS = +10V, All Unused Inputs and Output = -10V, VEN = 0.8V	1	+25°C	-50	50	nA
	-IS(OFF)	VS = -10V, All Unused Inputs and Output = +10V, VEN =0.8V	1	+25°C	-50	50	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch	+ID(OFF)	VD = +10V, VEN = 0.8V. All Unused Inputs = -10V	1	+25°C	-250	250	nA
	-ID(OFF)	VD = -10V, VEN = 0.8V. All Unused Inputs = +10V	1	+25°C	-250	250	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch With Overvoltage Applied	+ID(OFF) Overvoltage	VS =+25V, Measure VD, VEN = 0.8V, All Unused Inputs tied to GND	1	+25°C	-2000	2000	nA
	-ID(OFF) Overvoltage	VS = -25V, Measure VD, VEN = 0.8V, All Unused Inputs tied to GND	1	+25°C	-2000	2000	nA
Leakage Current from an "ON" Driver into the Switch (Drain & Source)	+ID(On)	VS = VD = +10V, VEN = 4.0V. All Unused Inputs = -10V	1	+25°C	-250	250	nA
	-ID(On)	VS = VD = -10V, VEN = 4.0V. All Unused Inputs = +10V	1	+25°C	-250	250	nA
Switch On Resistance	+R(On)	VS = +10V, IOUT = -100µA, VEN = 4.0V	1	+25°C	-	1500	Ω
	-R(On)	VS = -10V, IOUT = +100µA, VEN = 4.0V	1	+25°C	-	1500	Ω
Positive Supply Current	I(+)	VEN = 4.0V	1	+25°C	-	2	mA
Negative Supply Current	I(-)	VEN = 4.0V	1	+25°C	-1	-	mA
Positive Standby Supply Current	+ISBY	VEN = 0.8V	1	+25°C	-	2	mA
Negative Standby Supply Current	-ISBY	VEN = 0.8V	1	+25°C	-1	-	mA
Break-Before-Make Time Delay	TD	RL = 1000Ω, CL = 50pF	9	+25°C	5	-	ns
Propogation Delay Times: Address Inputs to I/O Channels	TOn(A)	RL = 10KΩ, CL = 50pF	9	+25°C	-	3000	ns
	TOff(A)		10, 11	-55°C, +125°C	-	3000	ns
Enable to I/O	TOn(EN)	RL = 1000Ω, CL = 50pF	9	+25°C	-	3000	ns
	TOff(EN)		10, 11	-55°C, +125°C	-	3000	ns

TABLE 5. DC POST BURN-IN DELTA ELECTRICAL SPECIFICATIONS

Guaranteed, per MIL-STD 883. Unless Otherwise Specified: V- = -15V, V+ = +15V, VAH = +4.0V, VAL = 0.8V

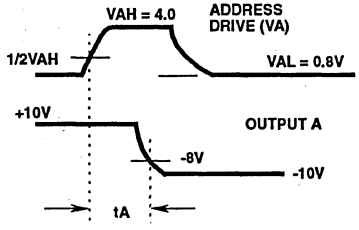
PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current, Address,or Enable Pins	IAH IAL	Measure Inputs Sequentially,Ground All Unused Pins	1	+25°C	-100	100	nA
Leakage Current into the Source Terminal of an "OFF" Switch	+IS(OFF)	VS = +10V, All Unused Inputs and Output = -10V, VEN = 0.8V	1	+25°C	-20	20	nA
	-IS(OFF)	VS = -10V, All Unused Inputs and Output = +10V, VEN =0.8V	1	+25°C	-20	20	nA
Leakage Current into the Drain Terminal of an "OFF" Switch	+ID(OFF)	VD = +10V, VEN = 0.8V, All Unused Inputs = -10V	1	+25°C	-20	20	nA
	-ID(OFF)	VD = -10V, VEN = 0.8V. All Unused Inputs = +10V	1	+25°C	-20	20	nA
Leakage Current from an "ON" Driver into the Switch (Drain & Source)	+ID(On)	VS = VD = +10V, VEN = 4.0V. All Unused Inputs = -10V	1	+25°C	-20	20	nA
	-ID(On)	VS = VD = -10V, VEN = 4.0V All Unused Inputs = +10V	1	+25°C	-20	20	nA
Switch On Resistance	+R(On)	VS = +10V, IOUT = -100µA, VEN = 4.0V	1	+25°C	-150	-150	Ω
	-R(On)	VS = -10V, IOUT = +100µA, VEN = 4.0V	1	+25°C	-150	-150	Ω
Positive Supply Current	I(+)	VEN = 4.0V	1	+25°C	-200	200	µA
Negative Supply Current	I(-)	VEN = 4.0V	1	+25°C	-100	100	µA
Positive Standby Supply Current	+I(SBY)	VEN = 0.8V	1	+25°C	-200	200	µA
NegativeStandby Supply Current	-I(SBY)	VEN = 0.8V	1	+25°C	-100	100	µA

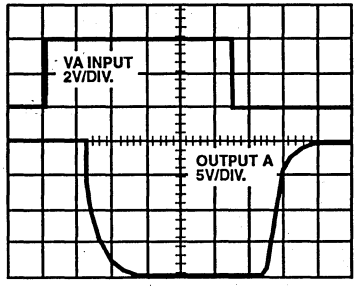
TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	Q SUBGROUPS
Initial Test		100%/5004	1, 4
Interim Test		100%/5004	1
PDA		100%/5004	1
Final Test		100%/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B	B5	Samples/5005	1, 2, 3
	Others	Samples/5005	1, 7
Group D		Samples/5005	1, 7
Group E, Subgroup 2		Samples/5005	1, 7

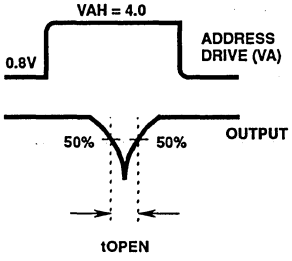
Switching Waveforms

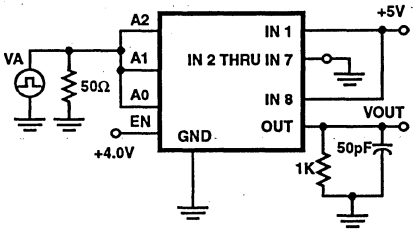
ACCESS TIME

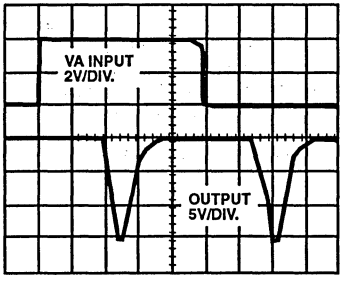




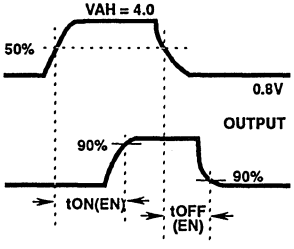
BREAK-BEFORE-MAKE DELAY (tOPEN)

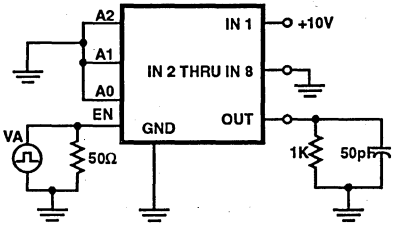


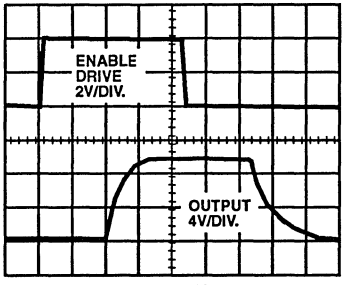




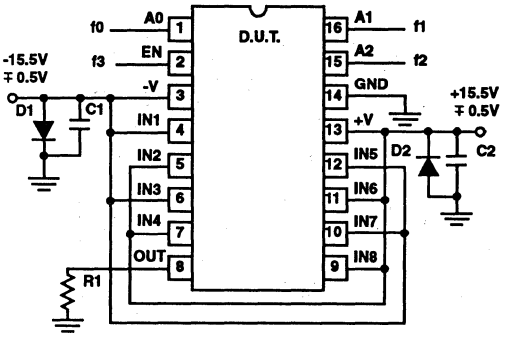
ENABLE DELAY (tON(EN), tOFF(EN))







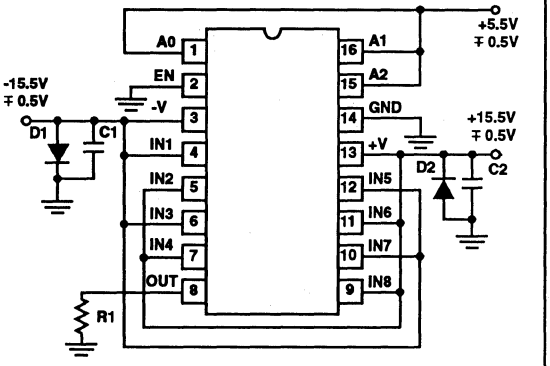
Burn-In Circuits



DYNAMIC BURN-IN AND LIFE TEST CIRCUIT

NOTES:

R1 = 10K ohms ±5%, $^1/_2$ or $^1/_4$ watt (per socket)
C1 = C2 = 0.01µF minimum (per socket) or
0.1µF minimum (per row)
D1 = D2 = 1N4002 (or equivalent)
f0 = 100KHz; f1 = f0/2; f2 = f0/4; f3 = f0/8; 50% Duty Cycle
VIL = 0.8V max; VIH = 4.0V min.



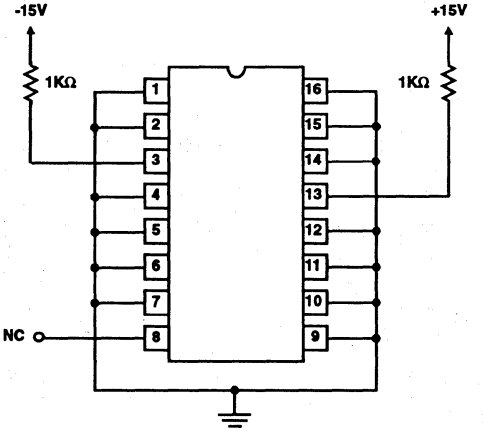
STATIC BURN-IN TEST CIRCUIT

NOTES:

R1 = 10K ohms ±5%, $^1/_2$ or $^1/_4$ watt (per socket)
C1 = C2 = 0.01µF minimum (per socket) or
0.1µF minimum (per row)
D1 = D2 = 1N4002 (or equivalent)

Irradiation Circuit

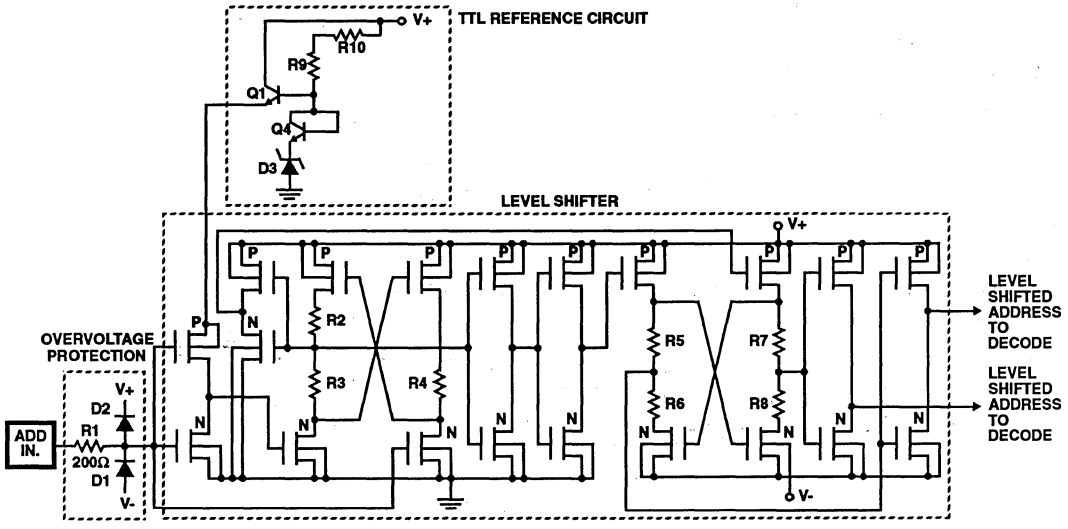
16 PIN DIP



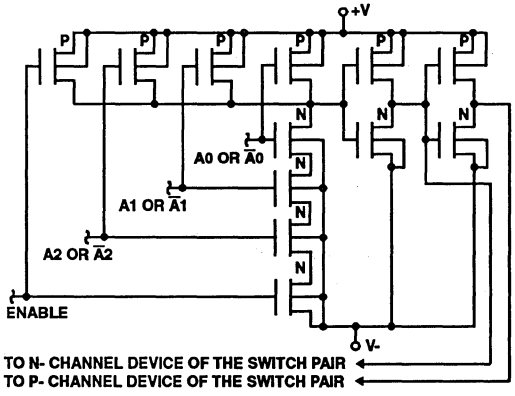
NOTE: All irradiation testing is performed in the 16 pin sidebrazed DIP package

Schematic Diagrams

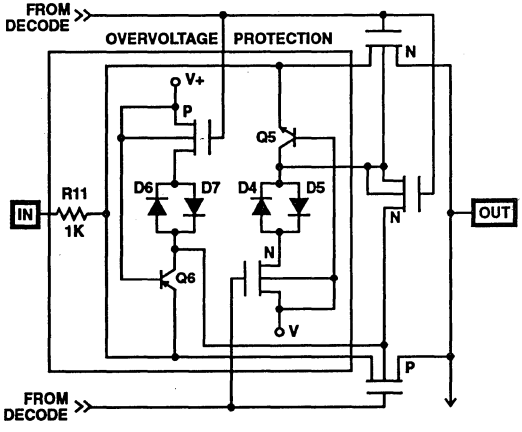
ADDRESS INPUT BUFFER AND LEVEL SHIFTER



ADDRESS DECODER



MULTIPLEX SWITCH



Harris - Space Level Product Flow

SEM - Traceable to Diffusion Method 2018

Wafer Lot Acceptance Method 5007

Internal Visual Inspection (Note 1)

Gamma Radiation Assurance Tests Method 1019

100% Nondestructive Bond Pull Method 2023

Customer Pre-Cap Visual Inspection (Notes 1, 2)

Temperature Cycling Method 1010 Condition C

Constant Acceleration method 2001 Y1 30KG

Particle Impact Noise Detection method 2020, Condition A 20G

Marking and Serialization

X-Ray Inspection Method 2012

Initial Electrical Tests (T0)

Static Burn-In 72 Hour, +125°C method 1015 Condition A

Room Temperature Electrical Tests (T1)

Burn-In Delta Calculation (T0-T1)

PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ

Dynamic Burn-In 240 Hours, +125°C Method 1015 Condition D

Electrical Tests Subgroups 1, 7, 9 (T2)

Burn-In Delta Calculation (T0 - T2)

PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ

Electrical Test +125°C, -55°C

Alternate Group A Inspection Method 5005

Fine and Gross Leak Tests Method 1014

Customer Source Inspection (Note 2)

Group B Inspection (Notes 2, 4) Method 5005

Group D Inspection (Notes 2, 4) Method 5005

External Visual Inspection Method 2009

Data Package Generation (Note 3)

NOTES:

1. Visual Inspection is performed to MIL-STD-883 Method 2010, Condition A.
2. These steps are optional, and should be listed on the purchase order if required.
3. Data package contains: Assembly Attributes (post seal)
   Test Attributes (includes Group A) -55°C, +25°C, +125°C
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (includes SEM report)
   X-Ray Report and Film
   Test Variables Data, DC Test and TELQV
   +25°C Initial Test
   +25°C Interim Test 1
   +25°C Interim Test 2
   +25°C Delta Over Burn-In
4. Group B data package contains Attributes Data pulse Variables Data, DC Test and TE2HQV. Group D data package contains Attributes only.

Metallization Topology

DIE DIMENSIONS:
83 x108 x 11 mils

METALLIZATION:
Type: Aluminum
Thickness: 12.5kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

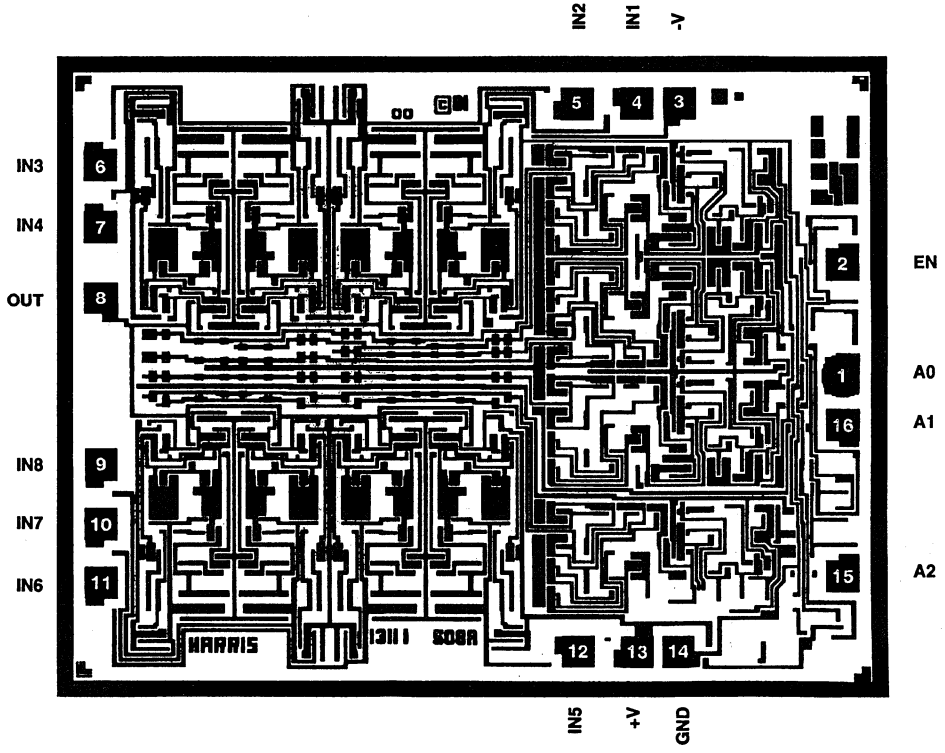
DIE ATTACH:
Material: Gold Eutectic
Temperature: Side Braze DIP - 335°C (Max)
Flatpack - 460°C (Max)

WORST CASE CURRENT DENSITY:
6.68e04 Amps/cm^2

PROCESS: CMOS-DI

Metallization Mask Layout

HS-508ARH/883S



HARRIS SEMICONDUCTOR

HS-1840RH/883S

Rad-Hard 16 Channel CMOS Analog Multiplexer with High-Z Analog Input Protection

December 1992

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Radiation Environment
  - Gamma Rate ($\dot{\gamma}$) 1 x 10^8 RAD(Si)/s
  - Gamma Dose (γ) 2 x 10^5 RAD(Si)
- Low Power Consumption
- Fast Access Time 1000ns
- High Analog Input Impedance 500MΩ During Power Loss (Open)
- Dielectrically Isolated Device Islands
- Excellent in Hi-Rel Redundant Systems
- Break-Before-Make Switching
- No Latch-Up

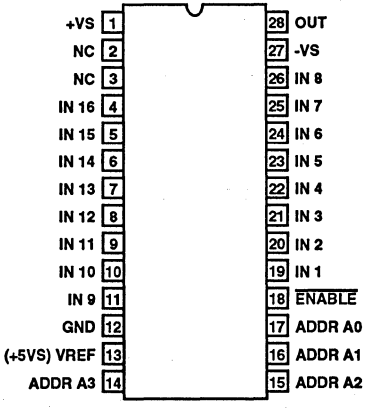
Description

The HS-1840RH/883S is a radiation hardened, monolithic 16 channel multiplexer constructed with the Harris Linear Dielectric Isolation CMOS process. It is designed to provide a high input impedance to the analog source if device power fails (open) or the analog signal voltage inadvertently exceeds the supply rails during powered operation. Excellent for use in redundant applications, since the secondary device can be operated in a standby unpowered mode affording no additional power drain. More significantly, a very high impedance exists between the active and inactive devices preventing any interaction. One of sixteen channel selection is controlled by a 4-bit binary address plus an Enable-Inhibit input which conveniently controls the ON/OFF operation of several multiplexers in a system. All digital inputs have electrostatic discharge protection.

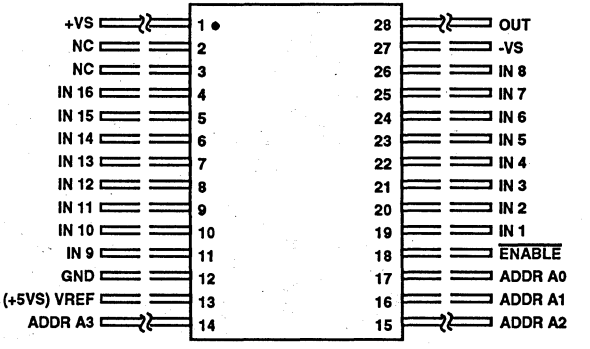
The HS-1840RH/883S has been specifically designed to meet exposure to radiation environments. It is available in a 28 pin Ceramic Sidebraze dual-in-line package and 28 pin Ceramic Flatpack. It is guaranteed operational from -55°C to +125°C.

Pinouts

HS1-1840RH/883S 28 PIN CERAMIC SIDEBRAZE DIP
CASE OUTLINE D-10,COMPLIANT TO MIL-M-38510 PACKAGE
TOP VIEW



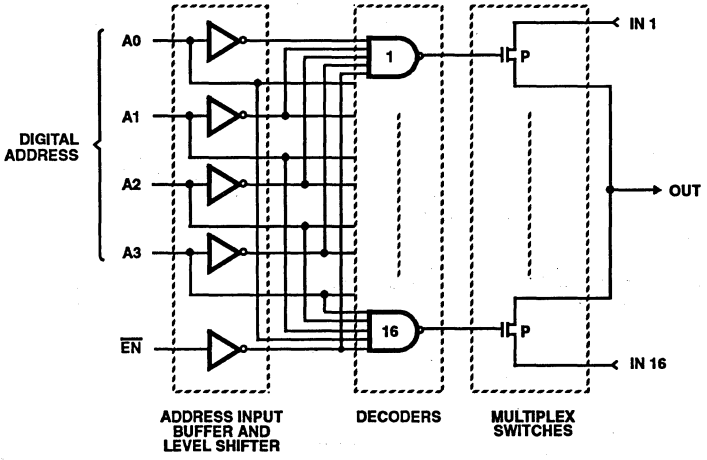
HS9-1840RH/883S 28 PIN CERAMIC SIDEBRAZE FLATPACK
CASE OUTLINE F-11A, COMPLIANT TO MIL-M-38510 PACKAGE
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3022

Functional Diagram



Truth Table

A3	A2	A1	A0	EN	"ON" CHANNEL
X	X	X	X	H	None
L	L	L	L	L	1
L	L	L	H	L	2
L	L	H	L	L	3
L	L	H	H	L	4
L	H	L	L	L	5
L	H	L	H	L	6
L	H	H	L	L	7
L	H	H	H	L	8
H	L	L	L	L	9
H	L	L	H	L	10
H	L	H	L	L	11
H	L	H	H	L	12
H	H	L	L	L	13
H	H	L	H	L	14
H	H	H	L	L	15
H	H	H	H	L	16

Absolute Maximum Ratings

Supply Voltage Between Pins 1 and 27 ..... +40V
+VSUPPLY to Ground ..... +20V
-VSUPPLY to Ground ..... -20V
VREF to Ground ..... +20V
Analog input Overvoltage:
+VS ..... +25V (Power On/Off)
-VS ..... -25V (Power On)
Digital Input Overvoltage:
+VEN, +VA ..... VREF +4V
-VEN, -VA ..... GND -4V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +275°

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Sidebraze Package	83.1°C/W	19.1°C/W
Flatpack Package	49.1°C/W	16.5°C/W

Total Power Dissipation*:
Sidebraze DIP Package 1600mW
Ceramic Flatpack Package 1400mW
ESD Classification ..... Class 1

* For DIP Derate 20.4mW/°C above T_A = +95°C
For Flatpack Derate 18.5mW/°C above T_A = +95°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage (±VSUPPLY) ..... ±15V
Operating Temperature Range ..... -55°C to +125°C
VREF (Pin 13) ..... +5V
Logic Low Level (VAL) ..... +0.8V
Logic High Level (VAH) ..... +4.0V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested. Unless Otherwise Specified: V- = -15V, V+ = +15V, VREF = +5V, VAH = +4.0V, VAL = 0.8V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Analog Signal Range	VS		7, 8A, 8B	-55°C, +25°C, +125°C	-5	+15	V
Input Leakage Current, Address, or Enable Pins	IAH IAL	Measure Inputs Sequentially Ground All Unused Pins VAL = 0.8V, VAH = 4.0V	1, 2, 3	-55°C, +25°C, +125°C	-1000	1000	nA
Leakage Current Into the Source Terminal of an "Off" Switch	+IS(OFF)	VS = +10V, All Unused Inputs and Output = -10V, VEN = 4V	1	+25°C	-10	10	nA
			2, 3	+125°C,-55°C	-100	100	nA
	-IS(OFF)	VS = -10V, All Unused Inputs, Output = +10V, VEN = 4V	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-100	100	nA
Leakage Current into the Source Terminal of an "Off" Switch With Power "Off"	+IS(OFF) Power Off	V+, V-, VREF, A0, A1, A2, A3,A4, EN = GND, Unused Inputs Tied to GND, VS = +25V	1	+25°C	-50	50	nA
			2, 3	+125°C, -55°C	-100	100	nA
Leakage Current Into the Source Terminal of an "Off" Switch With Overvoltage Applied	+IS(OFF) Overvoltage	VS = +25V, VD = 0V, VEN = 4V All Unused Inputs Tied to GND	1, 2, 3	-55°C, +25°C, +125°C	-1000	1000	nA
	-IS(OFF) Overvoltage	VS = -25V, VD = 0V, VEN = 4V All Unused Inputs Tied to GND	1, 2, 3	-55°C, +25°C, +125°C	-1000	1000	nA
Leakage Current Into the Drain Terminal of an "Off" Switch	+ID(OFF)	VD = +10V, VEN = 4V All Unused Inputs = -10V	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-100	100	nA
	-ID(OFF)	VD = -10V, VEN = 4V All Unused Inputs = +10V	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-100	100	nA
Leakage Current Into the Drain Terminal of an "Off" Switch With Overvoltage Applied	+ID(OFF) Overvoltage	VS = +25V, Measure VD, VEN = 4V, All Unused Inputs to GND	1, 2, 3	-55°C, +25°C, +125°C	-1000	1000	nA
	-ID(OFF) Overvoltage	VS = -25V, Measure VD, All Unused Inputs to GND	1, 2, 3	-55°C, +25°C, +125°C	-1000	1000	nA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Guaranteed and 100% Tested. Unless Otherwise Specified: V- = -15V, V+ = +15V, VREF = +5V, VAH = +4.0V, VAL = 0.8V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Leakage Current from an "On" Driver into the Switch (Drain & Source)	+ID(ON)	VS = +10V, VD = +10V, VEN = 0.8V All unused inputs = -10V	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-100	100	nA
	-ID(ON)	VS = -10V, VD = -10V, VEN = 0.8V, All Unused Inputs = +10V	1	+25°C	-10	10	nA
			2, 3	+125°C, -55°C	-100	100	nA
Switch On Resistance	+15V R(ON)	VS = +15V, ID = -1mA, VEN = 0.8V	1, 2, 3	-55°C, +25°C, +125°C	50	1000	Ω
	-5V R(ON)	VS = -5V, ID = +1mA, VEN = 0.8V	1, 2, 3	-55°C, +25°C, +125°C	50	4000	Ω
	+5V R(ON)	VS = +5V, ID = -1mA, VEN = 0.8V	1, 2, 3	-55°C, +25°C, +125°C	50	2500	Ω
Positive Supply Current	I(+)	VEN = 0.8V	1, 2, 3	-55°C, +25°C, +125°C	-	0.5	mA
Negative Supply Current	I(-)	VEN = 0.8V	1, 2, 3	-55°C, +25°C, +125°C	-0.5	-	mA
Positive Standby Supply Current	+ISBY	VEN = 4.0V	1, 2, 3	-55°C, +25°C, +125°C	-	0.5	mA
Negative Standby Supply Current	-ISBY	VEN = 4.0V	1, 2, 3	-55°C, +25°C, +125°C	-0.5	-	mA

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested. Unless Otherwise Specified: V- = -15V, V+ = +15V, VREF = +5V, VAH = +4.0V, VAL = 0.8V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Break-Before-Make Time Delay	TD	RL = 1000Ω, CL = 50pF	9	+25°C	25	-	ns
			10, 11	+125°C, -55°C	5	-	ns
Propagation Delay Times: Address Inputs to I/O Channels	TON(A), TOFF(A)	RL = 10KΩ,CL = 50pF	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	1000	ns
Enable to I/O	TON(EN), TOFF(EN)	RL = 1000Ω, CL = 50pF	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	1000	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized At: V- = -15V, V+ = +15V, VREF = +5V, VAH = +4.0V, VAL = 0.8V, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Address Input	CA	+VS = -VS = 0V, f = 1MHz	1	+25°C	-	7	pF
Capacitance Channel Input	CS(OFF)	+VS = -VS = 0V, f = 1MHz	1	+25°C	-	5	pF
Capacitance Channel Output	CD(OFF) TOFF(EN)	+VS = -VS = 0V, f = 1MHz	1	+25°C	-	50	pF
Off Isolation	VISO	VEN = 4.0V, f = 200kHz, CL = 7pF, RL = 1kΩ, VS = 3.0VRMS	1	+25°C	45	-	dB

NOTE: 1. The parameters listed in Table 3 are controlled via design or process parameters and not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. POST 200K RAD(Si) ELECTRICAL CHARACTERISTICS

Tested, per Mil-Std-883. Unless Otherwise Specified: V- = -15V, V+ = +15V, VREF = +5V, VAH = +4.5V, VAL = 0.5V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current, Address, or Enable Pins	IAH IAL	Measure Inputs Sequentially, Ground All Unused Pins	1	+25°C	-1000	1000	nA
Leakage Current Into the Source Terminal of an "Off" Switch	+IS(OFF)	VS = +10V, All Unused Inputs & Output = -10V, VEN = 4.5V	1	+25°C	-100	100	nA
	-IS(OFF)	VS = -10V, All Unused Inputs & Output = +10V, VEN = 4.5V	1	+25°C	-100	100	nA
Leakage Current into the Source Terminal of an "Off" Switch With Power "Off"	+IS(OFF) Power Off	V+, V-, VREF, A0, A1, A2, A3, A4, EN = GND, Unused Inputs Tied to GND, VS = +25V	1	+25°C	-100	100	nA
Leakage Current Into the Source Terminal of an "Off" Switch With Overvoltage Applied	+IS(OFF) Overvoltage	VS = +25V, VD=0V, VEN=4.5V All Unused Inputs Tied to GND	1	+25°C	-1500	1500	nA
	-IS(OFF) Overvoltage	VS = -25V, VD=0V, VEN=4.5V All Unused Inputs Tied to GND	1	+25°C	-1500	1500	nA
Leakage Current Into the Drain Terminal of an "Off" Switch	+ID(OFF)	VD = +10V, VEN = 4.5V All Unused Inputs = -10V	1	+25°C	-100	100	nA
	-ID(OFF)	VD = -10V, VEN = 4.5V All Unused Inputs = +10V	1	+25°C	-100	100	nA
Leakage Current Into the Drain Terminal of an "Off" Switch With Overvoltage Applied	+ID(OFF) Overvoltage	VS = +25V, Measure VD, VEN = 4.5V All Unused Inputs to GND	1	+25°C	-1000	1000	nA
	-ID(OFF) Overvoltage	VS = -25V, Measure VD, VEN = 4.5V All Unused Inputs to GND	1	+25°C	-1000	1000	nA
Leakage Current from an "On" Driver into the Switch (Drain & Source)	+ID(ON)	VS=+10V, VD = +10V, VEN = 0.5V All Unused Inputs = -10V	1	+25°C	-100	100	nA
	-ID(ON)	VS = -10V, VD = -10V, VEN = 0.5V All Unused Inputs = +10V	1	+25°C	-100	100	nA
Switch On Resistance	+15V R(ON)	VS = +15V, ID = -1mA, VEN = 0.5V	1	+25°C	50	1000	Ω
	-5V R(ON)	VS = -5V, ID = +1mA, VEN = 0.5V	1	+25°C	50	4000	Ω
	+5V R(ON)	VS = +5V, ID = -1mA, VEN = 0.5V	1	+25°C	50	2500	Ω
Positive Supply Current	I(+)	VEN = 0.5V	1	+25°C	-	0.50	mA
Negative Supply Current	I(-)	VEN = 0.5V	1	+25°C	-0.50	-	mA
Positive Standby Supply Current	+I(SBY)	VEN = 4.5V	1	+25°C	-	0.50	mA
Negative Standby Supply Current	-I(SBY)	VEN = 4.5V	1	+25°C	-0.50	-	mA
Make-Before-Break Time Delay	TD	RL = 1000Ω, CL = 50pf	9	+25°C	5	-	ns
Propagation Delay Times: Adress Inputs to I/O Channels	TON (A) TOFF (A)	RL = 10KΩ, CL = 50pf	9	+25°C	-	3000	ns
Enable to I/O	TON (EN) TOFF (EN)	RL = 1000Ω, CL = 50pf	9	+25°C	-	3000	ns

TABLE 5. DC POST BURN-IN DELTA ELECTRICAL CHARACTERISTICS

Guaranteed, per Mil-Std-883, Method 1019. Unless Otherwise Specified: V- = -15V, V+ = +15V, VREF = +5V, VAH = +4.0V, VAL = 0.8V

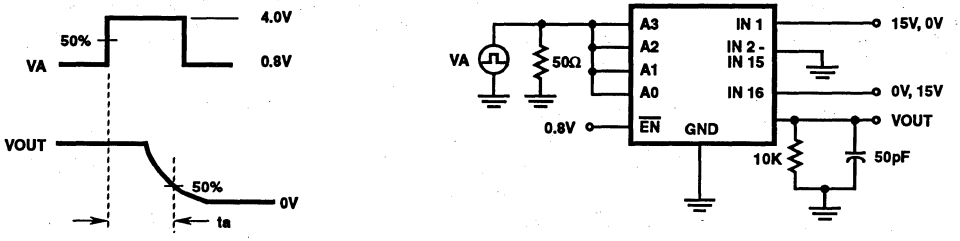
PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current, Address, or Enable Pins	IAH IAL	Measure Inputs Sequentially, Ground All Unused Pins	1	+25°C	-100	100	nA
Leakage Current Into the Source Terminal of an "Off" Switch	+IS(OFF)	VS = +10V, All Unused Inputs & Output = -10V, VEN = 4.0V	1	+25°C	-20	20	nA
	-IS(OFF)	VS = -10V, All Unused Inputs & Output = +10V, VEN = 4.0V	1	+25°C	-20	20	nA
Leakage Current Into the Drain Terminal of an "Off" Switch	+ID(OFF)	VD = +10V, VEN = 4.0V All Unused Inputs = -10V	1	+25°C	-20	20	nA
	-ID(OFF)	VD = -10V, VEN = 4.0V All Unused Inputs = +10V	1	+25°C	-20	20	nA
Leakage Current from an "On" Driver into the Switch (Drain & Source)	+ ID(ON)	VS = +10V, VD = +10V, VEN = 0.8V All Unused Inputs = -10V	1	+25°C	-20	20	nA
	-ID(ON)	VS = -10V, VD = -10V, VEN = 0.8V All Unused Inputs = +10V	1	+25°C	-20	20	nA
Switch On Resistance	+15V R(ON)	VS = +15V, ID = -1mA, VEN = 0.8V	1	+25°C	-150	150	Ω
	-5V R(ON)	VS = -5V, ID = +1mA, VEN = 0.8V	1	+25°C	-250	250	Ω
Positive Supply Current	I(+)	VEN = 0.8V	1	+25°C	-50	50	µA
Negative Supply Current	I(-)	VEN = 0.8V	1	+25°C	-50	50	µA
Positive Standby Supply Current	+ISBY	VEN = 4.0V	1	+25°C	-50	50	µA
Negative Standby Supply Current	-ISBY	VEN = 4.0V	1	+25°C	-50	50	µA

TABLE 6. APPLICABLE SUBGROUPS

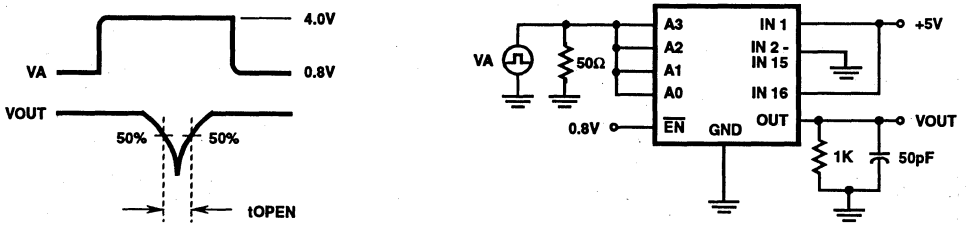
CONFORMANCE GROUPS		METHOD	Q SUBGROUPS
Initial Test		100%/5004	1
Interim Test		100%/5004	1
PDA		100%/5004	1
Final Test		100%/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B	B5	Samples/5005	1, 2, 3
	Others	Samples/5005	1, 7
Group D		Samples/5005	1, 7
Group E, Subgroup 2		Samples/5005	1, 7

Performance Characteristics and Test Circuits

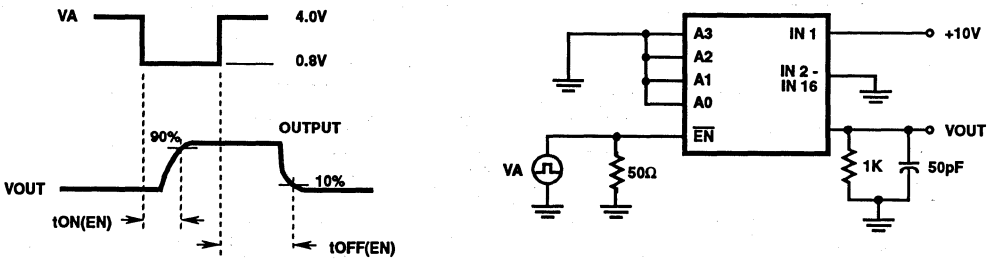
ACCESS TIME vs. LOGIC LEVEL (HIGH)



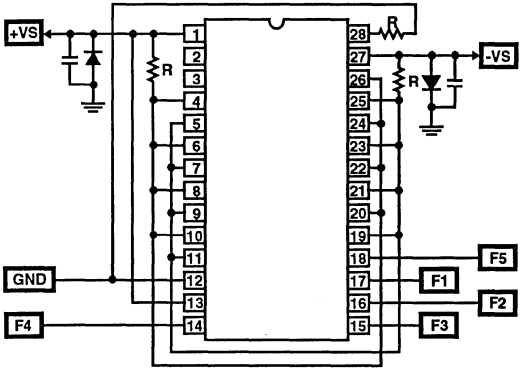
BREAK-BEFORE-MAKE DELAY (tOPEN)



ENABLE DELAY (tON(EN), tOFF(EN))



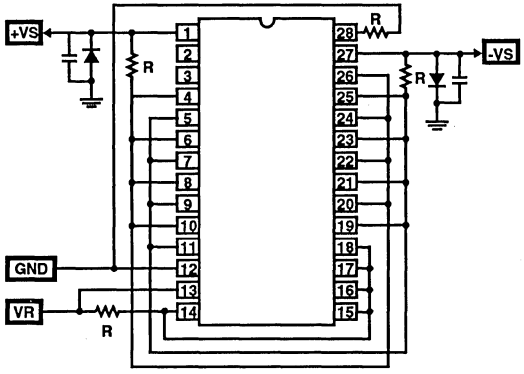
Burn-In/Life Test Circuits



DYNAMIC BURN-IN AND LIFE TEST CIRCUIT

NOTES:

VS+ = +15.5V ± 0.5V, VS- = -15.5V ± 0.5V
R = 1kΩ ± 5%
C1 = C2 = 0.01µF ± 10%, 1 each per socket, minimum
D1 = D2 = 1N4002, 1 each per board, minimum
Input Signals: square wave, 50% duty cycle, 0V to 15V peak ± 10%
F1 = 100kHz; F2 = F1/2; F3 = F1/4; F4 = F1/8; F5 = F1/16



STATIC BURN-IN TEST CIRCUIT

NOTES:

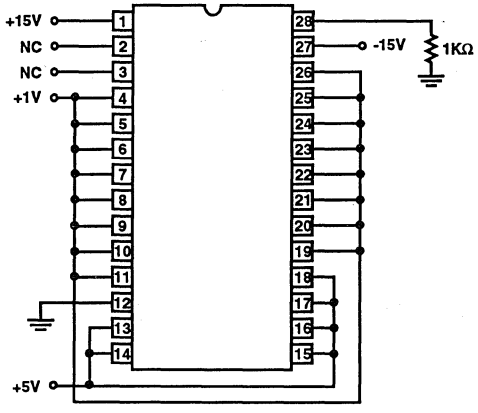
R = 1kΩ ± 5%, 1/4W
C1 = C2 = 0.01µF minimum, 1 each per socket, minimum
VS+ = 15.5V ± 0.5V, VS- = -15.5V ± 0.5V, VR = 15.5 ± 0.5V

NOTES:

1. The Above Test Circuits are Utilized for All Package Types
2. The Dynamic Test Circuit is Utilized for All Life Testing

Irradiation Circuit

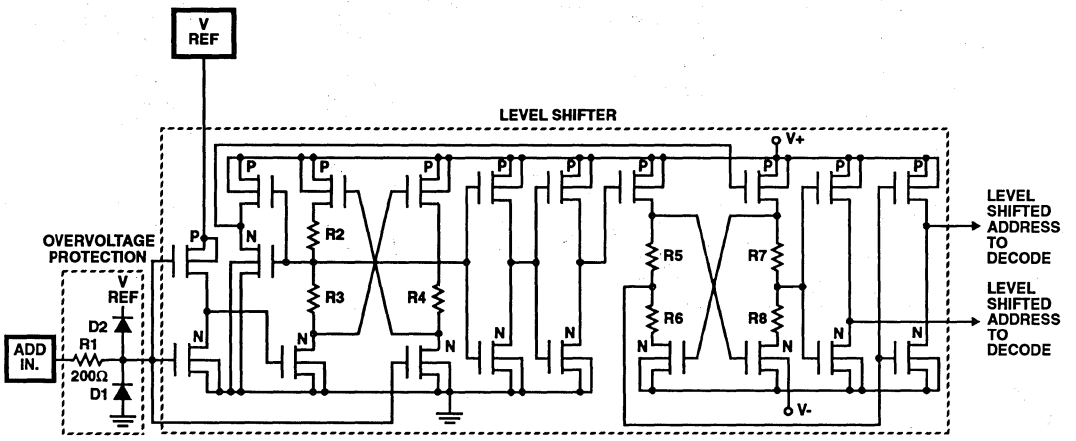
28 PIN DIP



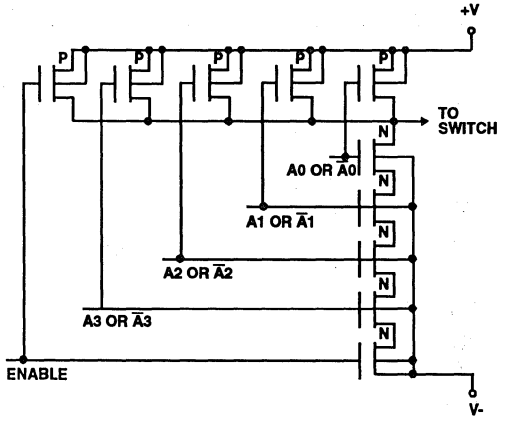
NOTE: All irradiation testing is performed in the 28 pin DIP package

Schematic Diagrams

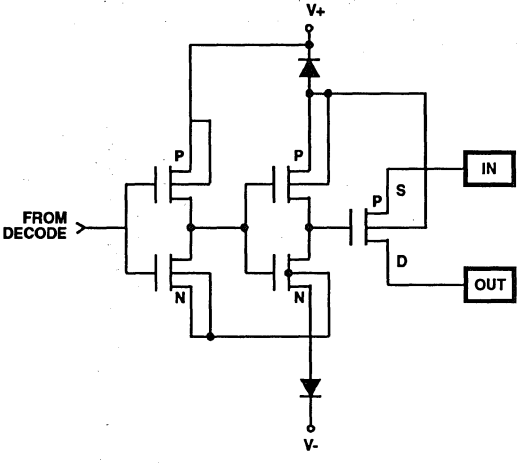
ADDRESS INPUT BUFFER AND LEVEL SHIFTER



ADDRESS DECODER



MULTIPLEX SWITCH



Harris - Space Level Product Flow

SEM - Traceable to Diffusion Method 2018

Wafer Lot Acceptance Method 5007

Internal Visual Inspection (Note 1)

Gamma Radiation Assurance Tests Method 1019

100% Nondestructive Bond Pull Method 2023

Customer Pre-Cap Visual Inspection (Notes 1, 2)

Temperature Cycling Method 1010 Condition C

Constant Acceleration method 2001 Y1 30KG

Particle Impact Noise Detection method 2020, Condition A 20G

Marking and Serialization

X-Ray Inspection Method 2012

Initial Electrical Tests (T0)

Static Burn-In 72 Hour, +125°C method 1015 Condition A

Room Temperature Electrical Tests (T1)

Burn-In Delta Calculation (T0-T1)

PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ

Dynamic Burn-In 240 Hours, +125°C Method 1015 Condition D

Electrical Tests Subgroups 1, 7, 9 (T2)

Burn-In Delta Calculation (T0 - T2)

PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ

Electrical Test +125°C, -55°C

Alternate Group A Inspection Method 5005

Fine and Gross Leak Tests Method 1014

Customer Source Inspection (Note 2)

Group B Inspection (Notes 2, 4) Method 5005

Group D Inspection (Notes 2, 4) Method 5005

External Visual Inspection Method 2009

Data Package Generation (Note 3)

NOTES:

1. Visual Inspection is performed to MIL-STD-883 Method 2010, Condition A.
2. These steps are optional, and should be listed on the purchase order if required.
3. Data package contains: Assembly Attributes (post seal)
   Test Attributes (includes Group A) -55°C, +25°C, +125°C
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (includes SEM report)
   X-Ray Report and Film
   Test Variables Data, DC Test and TELQV
   +25°C Initial Test
   +25°C Interim Test 1
   +25°C Interim Test 2
   +25°C Delta Over Burn-In
4. Group B data package contains Attributes Data pulse Variables Data, DC Test and TE2HQV. Group D data package contains Attributes only.

Metallization Topology

DIE DIMENSIONS:
110 x 159 x 11mils

METALLIZATION:
Type: Al
Thickness: 12.5kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Eutectic
Temperature: Sidebrazed Ceramic DIP - 460°C (Max)
Flatpack - 460°C (Max)

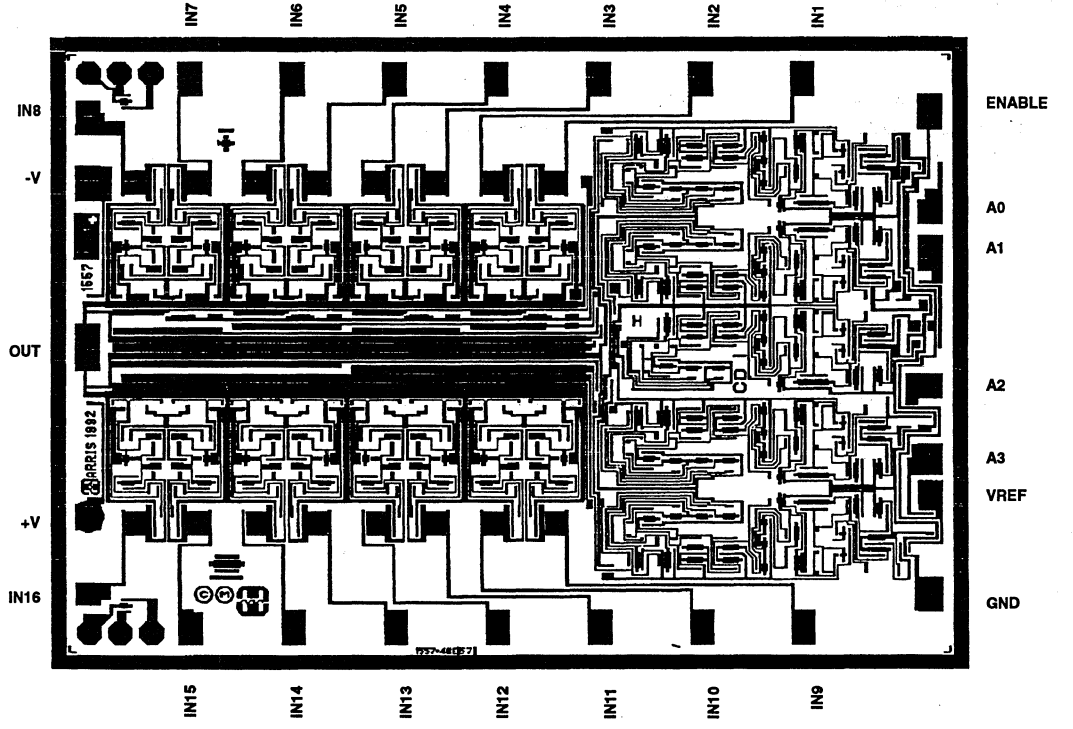
WORST CASE CURRENT DENSITY: 1.90e04A/cm^2

LEAD TEMPERATURE (10 Seconds Soldering): <275°C

PROCESS: CMOS-DI

Metallization Mask Layout

HS-1840RH/883S



HS-302RH/883S, HS-303RH/883S HS-306RH/883S, HS-307RH/883S HS-384RH/883S, HS-390RH/883S

Radiation Hardened CMOS Analog Switches

December 1992

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Radiation Hardened**
  - **Functional Total Dose Exceeds 1 x 10^5 RAD Si**
- **Pin for Pin Compatible with Harris HI-3XX Series Analog Switches**
- **Analog Signal Range 15V**
- **Low Leakage**
- **Low R_{ON}**
- **No Latch Up**
- **Versions for 5V and 15V Digital Systems**
- **Low Operating Power**
- **Military Temperature Range -55°C to +125°C**

Applications

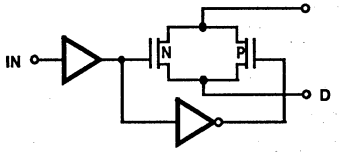
- **Sample and Hold i.e. Low Leakage Switching**
- **Op Amp Gain Switching i.e. Low ON Resistance**
- **Switched Capacitor Filters**
- **Low Level Switching Circuits**
- **Satellites**
- **Nuclear Reactor Controls**
- **Military Environments**

Description

The HS-3XXRH/883S family of analog switches are monolithic devices fabricated using Radiation Hardened CMOS technology and the Harris dielectric isolation process for latch-up free operation. Improved total dose hardness is obtained by layout (thin oxide tabs extending to a channel stop) and processing (hardened gate oxide). These switches offer low-resistance switching performance for analog voltages up to the supply rails. "ON" resistance is low and stays reasonably constant over the full range of operating voltage and current. "ON" resistance also stays reasonably constant when exposed to radiation, being typically 30Ω pre-rad and 35Ω post 100K RAD-Si. All devices provide break-before-make switching.

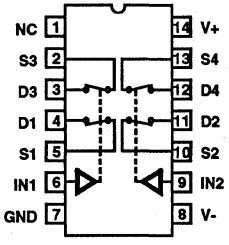
The 6 devices in this switch series are differentiated by type of switch action, pinout and digital logic levels. The HS-302/303/384/390RH/883S switches have 5V digital inputs while the HS-306/307RH/883S switches have 15V digital inputs. All devices are available in ceramic DIP packages. The HS-3XXRH/883S switches can directly replace the HI-3XX series devices.

Functional Diagram



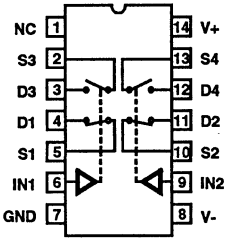
Pinouts (Switch States are for Logic "1" Inputs) TOP VIEWS

DUAL DPST
HS-302RH/883S
HS-306RH/883S



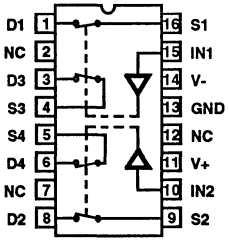
LOGIC	SWITCH 1 - 4
0	OFF
1	ON

DUAL SPDT
HS-303RH/883S
HS-307RH/883S



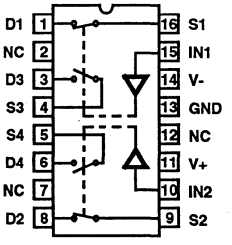
LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

DUAL DPST
HS-384RH/883S



LOGIC	SWITCH 1 - 4
0	OFF
1	ON

DUAL SPDT
HS-390RH/883S



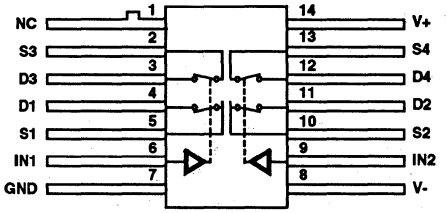
LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3067**

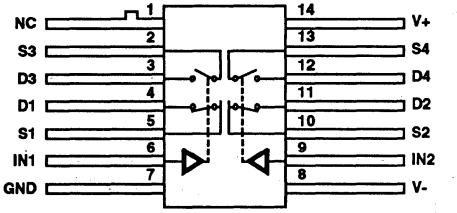
Pinouts (Switch States are for Logic "1" Inputs) TOP VIEWS (Continued)

DUAL DPST
HS-302RH/883S
HS-306RH/883S



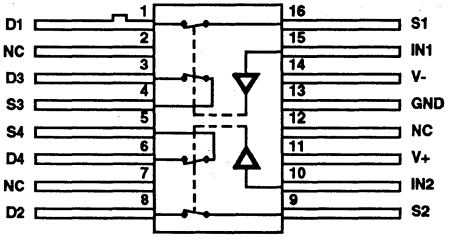
LOGIC	SWITCH 1 - 4
0	OFF
1	ON

DUAL SPDT
HS-303RH/883S
HS-307RH/883S



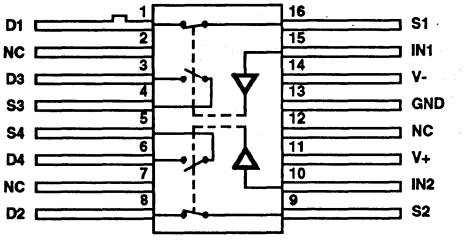
LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

DUAL DPST
HS-384RH/883S



LOGIC	SWITCH 1 - 4
0	OFF
1	ON

DUAL SPDT
HS-390RH/883S



LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

Absolute Maximum Ratings

Supply Voltage Between V+ and V- ..... +44V
+VSUPPLY to Ground ..... +22V
-VSUPPLY to Ground ..... -22V
Analog Input Overvoltages:
+VS ..... +VSUPPLY +1.5V
-VS ..... -VSUPPLY - 1.5V
Digital Input Overvoltage:
+VA ..... +VSUPPLY +4V
-VA ..... -VSUPPLY -4V
Peak Current, S or D Pulsed at 1ms, 10% Duty Cycle Max ... 40mA
Continuous Current 10mA
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (soldering 10s) ..... ≤ +300°C

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
14 Lead DIP	85.5°C/W	24.3°C/W
14 Lead Flatpack	85.0°C/W	11.5°C/W
16 Lead DIP	85.5°C/W	24.3°C/W
16 Lead Flatpack	85.0°C/W	11.5°C/W

Transistor Count 80
Total Power Dissipation:
14 Pin 588mW
16 Pin 685mW
ESD Classification ..... Class 1

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage (± VSupply) ..... ±15V
Operating Temperature Range ..... -55°C to +125°C

TABLE 1. HS-302RH/303RH/384RH/390RH/883S DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested. Unless Otherwise Specified: V- = -15V, V+ = +15V, VAH = +4.0V, VAL = 0.8V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
"Switch On" Resistance	+RDS	VD = 10V, IS = -10mA, S1/S2/S3/S4	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
	-RDS	VD = -10V, IS = 10mA, S1/S2/S3/S4	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
Leakage Current Into the Source Terminal of an "Off" Switch	+IS(OFF)	VS = +14V, VD = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
	-IS(OFF)	VS = -14V, VD = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
Leakage Current into the Drain Terminal of an "Off" Switch	+ID(OFF)	VS = -14V, VD = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
	-ID(OFF)	VS = +14V, VD = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
Leakage Current from an "On" Driver Into the Switch (Drain & Source)	+ID(ON)	VS = VD = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
	-ID(ON)	VS = VD = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
Low Level Input Address Current	IAL	All Channels VA = 0.8V	1	+25°C	-1	1	µA
			2, 3	-55°C to +125°C	-1	1	µA
High Level Input Address Current	IAH	All Channels VA = 4.0V	1	+25°C	-1	1	µA
			2, 3	-55°C to +125°C	-1	1	µA
Positive Supply Current	I(+)	All Channels VA = 0.8V	1	+25°C	-	10	µA
			2, 3	-55°C to +125°C	-	100	µA
		VA1 = 0V, VA2 = 4.0V and VA1 = 4.0V, VA2 = 0V	1	+25°C	-	0.5	mA
			2, 3	-55°C to +125°C	-	1	mA

TABLE 1. HS-302RH/303RH/384RH/390RH/883S DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested. Unless Otherwise Specified: V- = -15V, V+ = +15V, VAH = +4.0V, VAL = 0.8V **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Negative Supply Current	I(-)	All Channels VA = 0.8V	1	+25°C	-10	-	µA
			2, 3	-55°C to +125°C	-100	-	µA
		VA1 = 0V, VA2 = 4.0V and VA1 = 4.0V, VA2 = 0V	1	+25°C	-10	-	µA
			2, 3	-55°C to +125°C	-100	-	µA

TABLE 1. HS-306RH/307RH/883S DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested. Unless Otherwise Specified: V- = -15V, V+ = +15V, VAH = +11.0V, VAL = 3.5V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
"Switch On" Resistance	+RDS	VD = 10V, IS = -10mA, S1/S2/S3/S4	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
	+RDS	VD = -10V, IS = 10mA, S1/S2/S3/S4	1	+25°C	-	50	Ω
			2, 3	-55°C to +125°C	-	75	Ω
Leakage Current Into the Source Terminal of an "Off" Switch	+IS(OFF)	VS = +14V, VD = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
	-IS(OFF)	VS = -14V, VD = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
Leakage Current into the Drain Terminal of an "Off" Switch	+ID(OFF)	VS = -14V, VD = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
	-ID(OFF)	VS = +14V, VD = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
Leakage Current from an "On" Driver Into the Switch (Drain and Source)	+ID(ON)	VS = VD = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
	-ID(ON)	VS = VD = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
			2, 3	-55°C to +125°C	-100	100	nA
Low Level Input Address Current	IAL	All Channels VA = 3.5V	1	+25°C	-1	1	µA
			1, 2	-55°C to +125°C	-1	1	µA
High Level Input Address Current	IAH	All Channels VA = 11V	1	+25°C	-1	1	µA
			1, 2	-55°C to +125°C	-1	1	µA
Positive Supply Current	I(+)	All Channels VA = 0V	1	+25°C	-	10	µA
			2, 3	-55°C to +125°C	-	100	µA
		All Channels VA = 15V	1	+25°C	-	10	µA
			2, 3	-55°C to +125°C	-	100	µA
Negative Supply Current	I(-)	All Channels VA = 0V	1	+25°C	-10	-	µA
			2, 3	-55°C to +125°C	-100	-	µA
		All Channels VA = 15V	1	+25°C	-10	-	µA
			2, 3	-55°C to +125°C	-100	-	µA

TABLE 2. HS-302RH/303RH/384RH/390RH/883S AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested. Unless Otherwise Specified: V- = -15V, V+ = +15V, VAH = +4.0V, VAL = 0V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Break-Before-Make Time Delay (HS-303RH & 390RH Only)	TOPEN	RL = 300Ω, CL = 33pF, VS = +3V, VAH = 5V	9	+25°C	30	150	ns
			10, 11	-55°C to +125°C	-	300	ns
Switch Turn "On" Time	TON	RL = 300Ω, CL = 33pF, VS = +3V	9	+25°C	-	300	ns
			10, 11	-55°C to +125°C	-	500	ns
Switch Turn "Off" Time	TOFF	RL = 300Ω, CL = 33pF, VS = +3V	9	+25°C	-	250	ns
			10, 11	-55°C to +125°C	-	450	ns

TABLE 2. HS-306RH/307RH/883S A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested. Unless Otherwise Specified: V- = -15V, V+ = +15V, VAH = +15.0V, VAL = 0V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Break-Before-Make Time Delay (HS-307RH Only)	TOPEN	RL = 300Ω, CL = 33pF, VS = +3V	9	+25°C	30	150	ns
			10, 11	-55°C to +125°C	-	300	ns
Switch Turn "On" Time	TON	RL = 300Ω, CL = 33pF, VS = +3V	9	+25°C	-	300	ns
			10, 11	-55°C to +125°C	-	500	ns
Switch Turn "Off" Time	TOFF	RL = 300Ω, CL = 33pF, VS = +3V	9	+25°C	-	250	ns
			10, 11	-55°C to +125°C	-	450	ns

TABLE 3. HS-302RH/303RH/306RH/307RH/384RH/390RH/883S ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Unless Otherwise Specified: HS-302RH/303RH/384RH/390RH/883S V- = -15V, V+ = +15V, VAH = +4.0V, VAL = 0V
HS-306RH/307RH/883S V- = -15V, V+ = +15V, VAH = +15.0V, VAL = 0V

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch Input Capacitance	CIS(OFF)	Measured Source to GND	1	+25°C	-	28	pF
Driver Input Capacitance	CC1	VA = 0V	1	+25°C	-	10	pF
	CC2	VA = 15V	1	+25°C	-	10	pF
Switch Output	COS	Measured Drain to GND	1	+25°C	-	28	pF
Off Isolation	VISO	VGEN = 1Vp-p, f = 1MHz	1	+25°C	40	-	dB
Crosstalk	VCR	VGEN = 1Vp-p, f = 1MHz	1	+25°C	40	-	dB
Charge Transfer	VCTE	VS = GND, CL = 0.01µF	1	+25°C	-	15	mV

NOTE: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

TABLE 4. HS-302RH/303RH/384RH/390RH/883S DC POST 100K RAD (SI) ELECTRICAL CHARACTERISTICS

Tested Per Mil-Std-883. Unless Otherwise Specified: HS-302RH/303RH/384RH/390RH/883S V- = -15V, V+ = +15V, VAH = +4.0V, VAL = 0.8V
HS-306RH/307RH/883S V- = -15V, V+ = +15V, VAH = +11.0V, VAL = 3.5V

PARAMETER	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
"Switch On" Resistance	+RDS	VD = 10V, IS = -10mA, S1/S2/S3/S4	+25°C	-	60	Ω
	-RDS	VD = -10V, IS = 10mA, S1/S2/S3/S4	+25°C	-	60	Ω
Leakage Current Into the Source Terminal of an "Off" Switch	+IS(OFF)	VS = +14V, VD = -14V, S1/S2/S3/S4	+25°C	-100	100	nA
	-IS(OFF)	VS = -14V, VD = +14V, S1/S2/S3/S4	+25°C	-100	100	nA
Leakage Current into the Drain Terminal of an "Off" Switch	+ID(OFF)	VS = -14V, VD = +14V, S1/S2/S3/S4	+25°C	-100	100	nA
	-ID(OFF)	VS = +14V, VD = -14V, S1/S2/S3/S4	+25°C	-100	100	nA
Leakage Current from an "On" Driver Into the Switch (Drain & Source)	-ID(ON)	VS = VD = +14V, S1/S2/S3/S4	+25°C	-100	100	nA
	-ID(ON)	VS = VD = -14V, S1/S2/S3/S4	+25°C	-100	100	nA
Positive Supply Current	I(+)	All Channels VA = 0.8V	+25°C	-	100	µA
		VA1 = 0V, VA2 = 4.0V and VA1 = 4.0V, VA2 = 0V	+25°C	-	1	mA
Negative Supply Current	I(-)	All Channels VA = 0.8V	+25°C	-100	-	µA
		VA1 = 0V, VA2 = 4.0V and VA1 = 4.0V, VA2 = 0V	+25°C	-100	-	µA
High Level Address Current	IAH	All Channels High	+25°C	-1	+1	µA
Low Level Address Current	IAL	All Channels Low	+25°C	-1	+1	µA
Break-Before-Make Time Delay (HS-303RH/883S and HS390RH/883S Only)	TOPEN	RL = 300Ω, CL = 33pf, VS = +3V (Note 1)	+25°C	2	300	ns
Switch Turn-On Time	TON	RL = 300Ω, CL = 33pf, VS = +3V (Note 1)	+25°C	-	500	ns
Switch Turn-Off Time	TOFF	RL = 300Ω, CL = 33pf, VS = +3V (Note 1)	+25°C	-	450	ns

NOTE: 1. VAL = 0V; VAH = 4.0V

TABLE 4. HS-306/307RH/883S DC POST 100K RAD (Si) ELECTRICAL CHARACTERISTICS

Tested Per Mil-Std-883. Unless Otherwise Specified: HS-306RH/307RH/883S V- = -15V, V+ = +15V, VAH = +11.0V, VAL = 3.5V

PARAMETER	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
"Switch On" Resistance	+RDS	VD = 10V, IS = -10mA, S1/S2/S3/S4	+25°C	-	60	Ω
	-RDS	VD = -10V, IS = 10mA, S1/S2/S3/S4	+25°C	-	60	Ω
Leakage Current Into the Source Terminal of an "Off" Switch	+IS(OFF)	VS = +14V, VD = -14V, S1/S2/S3/S4	+25°C	-100	100	nA
	-IS(OFF)	VS = -14V, VD = +14V, S1/S2/S3/S4	+25°C	-100	100	nA
Leakage Current into the Drain Terminal of an "Off" Switch	+ID(OFF)	VS = -14V, VD = +14V, S1/S2/S3/S4	+25°C	-100	100	nA
	-ID(OFF)	VS = +14V, VD = -14V, S1/S2/S3/S4	+25°C	-100	100	nA
Leakage Current from an "On" Driver Into the Switch (Drain & Source)	-ID(ON)	VS = VD = +14V, S1/S2/S3/S4	+25°C	-100	100	nA
	-ID(ON)	VS = VD = -14V, S1/S2/S3/S4	+25°C	-100	100	nA
Positive Supply Current	I(+)	All Channels VA = 0V	+25°C	-	100	µA
		All Channels VA = 15V	+25°C	-	1	mA
Negative Supply Current	I(-)	All Channels VA = 0V	+25°C	-100	-	µA
		All Channels VA = 15V	+25°C	-100	-	µA

TABLE 4. HS-306/307RH/883S DC POST 100K RAD (SI) ELECTRICAL CHARACTERISTICS

Tested Per Mil-Std-883. Unless Otherwise Specified: HS-306RH/307RH/883S V- = -15V, V+ = +15V, VAH = +11.0V, VAL = 3.5V

PARAMETER	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
High Level Address Current	IAH	All Channels High	+25°C	-1	+1	µA
Low Level Address Current	IAL	All Channels Low	+25°C	-1	+1	µA
Break-Before-Make Time Delay (HS-307RH/883S Only)	TOPEN	RL = 300Ω, CL = 33pf, VS = +3V (Note 1)	+25°C	2	300	ns
Switch Turn-On Time	TON	RL = 300Ω, CL = 33pf, VS = +3V (Note 1)	+25°C	-	500	ns
Switch Turn-Off Time	TOFF	RL = 300Ω, CL = 33pf, VS = +3V (Note 1)	+25°C	-	450	ns

NOTE: 1. VAL = 0V; VAH = 15V

TABLE 5. HS-302RH/303RH/384RH/390RH/883S DC POST BURN-IN DELTA ELECTRICAL CHARACTERISTICS

Guaranteed, Per Mil-Std-883. Unless Otherwise Specified: V- = -15V, V+ = +15V, VAH = +4.0V, VAL = 0.8V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
"Switch On" Resistance	+RDS	VD = 10V, IS = -10mA, S1/S2/S3/S4	1	+25°C	-5	5	Ω
	-RDS	VD = -10V, IS = 10mA, S1/S2/S3/S4	1	+25°C	-5	5	Ω
Leakage Current Into the Source Terminal of an "Off" Switch	+IS(OFF)	VS = +14V, VD = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
	-IS(OFF)	VS = -14V, VD = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
Leakage Current into the Drain Terminal of an "Off" Switch	+ID(OFF)	VS = -14V, VD = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
	-ID(OFF)	VS = +14V, VD = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
Leakage Current from an "On" Driver Into the Switch (Drain & Source)	+ID(ON)	VS = VD = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
	-ID(ON)	VS = VD = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
Low Level Input Address Current	IAL	All Channels VA = 0.8V	1	+25°C	-100	100	nA
High Level Input Address Current	IAH	All Channels VA = 4.0V	1	+25°C	-100	100	nA
Positive Supply Current	I(+)	All Channels VA = 0.8V	1	+25°C	-1	1	µA
		VA1 = 0V, VA2 = 4.0V and VA1 = 4.0V, VA2 = 0V	1	+25°C	-0.1	0.1	mA
Negative Supply Current	I(-)	All Channels VA = 0.8V	1	+25°C	-1	1	µA
		VA1 = 0V, VA2 = 4.0V and VA1 = 4.0V, VA2 = 0V	1	+25°C	-1	1	µA

TABLE 5. HS-306RH/307RH/883S DC POST BURN-IN DELTA ELECTRICAL CHARACTERISTICS

Guaranteed, Per Mil-Std-883. Unless Otherwise Specified: V- = -15V, V+ = +15V, VAH = +11.0V, VAL = 3.5V

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
"Switch On" Resistance	+RDS	VD = 10V, IS = -10mA, S1/S2/S3/S4	1	+25°C	-5	5	Ω
	-RDS	VD = -10V, IS = 10mA, S1/S2/S3/S4	1	+25°C	-5	5	Ω
Leakage Current Into the Source Terminal of an "Off" Switch	+IS(OFF)	VS = +14V, VD = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
	-IS(OFF)	VS = -14V, VD = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
Leakage Current into the Drain Terminal of an "Off" Switch	+ID(OFF)	VS = -14V, VD = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
	-ID(OFF)	VS = +14V, VD = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
Leakage Current from an "On" Driver Into the Switch (Drain & Source)	+ID(ON)	VS = VD = +14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
	-ID(ON)	VS = VD = -14V, S1/S2/S3/S4	1	+25°C	-2	2	nA
Low Level Input Address Current	IAL	All Channels VA = 3.5V	1	+25°C	-100	100	nA
High Level Input Address Current	IAH	All Channels VA = 11V	1	+25°C	-100	100	nA
Positive Supply Current	I(+)	All Channels VA = 0V	1	+25°C	-1	1	µA
		All Channels VA = 15V	1	+25°C	-1	1	µA
Negative Supply Current	I(-)	All Channels VA = 0V	1	+25°C	-1	1	µA
		All Channels VA = 15V	1	+25°C	-1	1	µA

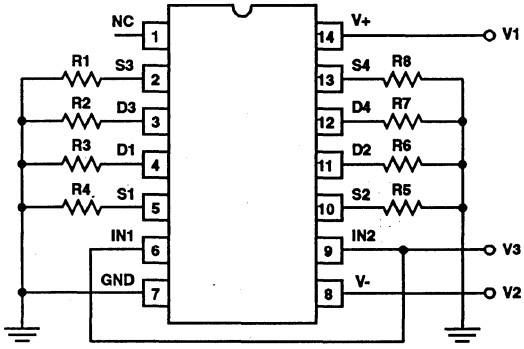
TABLE 6. HS-302RH/303RH/306RH/307RH/384RH/390RH/883S APPLICABLE SUBGROUPS

MIL-STD-883 TEST REQUIREMENTS	GROUP A SUBGROUPS PER METHOD 5005 (SEE TABLES 1 & 2)
Interim Electrical Parameters (Method 5004)	1
Final Electrical Test Parameters (Method 5004)	1, 2, 3, 9, 10,11 (Note 1) 7, 8A, 8B (Functional Tests)
Group A Test Requirements (Method 5005)	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B5 End-Point Electrical Parameters (Method 5005) (Class S Only)	1, 2, 3, 9, 10, 11 (Note 2)
Group B6 End-Point Electrical Parameters (Method 5005) (Class S Only)	1
Group C End-Point Electrical Parameters (Method 5005) (Class B Only)	1
Group D End-Point Electrical Parameters (Method 5005)	1
Group E2 End-Point Electrical Parameters (Method 5005)	1, 7 (Note 3)

NOTES:

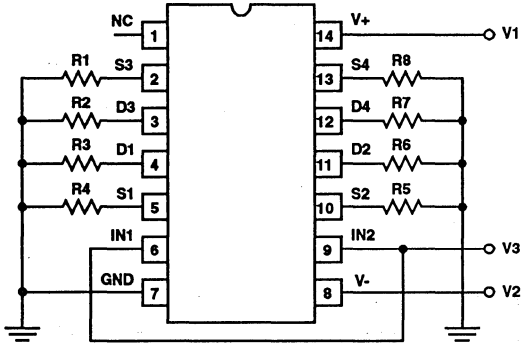
1. PDA applies to subgroup 1 and delta limits.
2. Subgroups 1, 2, 3 are datalogged; 9, 10 & 11 are go-no-go tests.
3. Endpoints are datalogged pre- and post-irradiation testing.

Irradiation Circuits



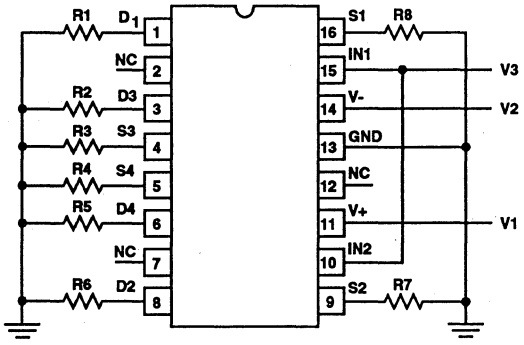
HS-302RH/303RH/883S

R1 - R8 = 10kΩ ± 5%, 1/4W
V1 = +15V ± 10%
V2 = -15V ± 10%
V3 = +5V ± 10%



HS-306RH/307RH/883S

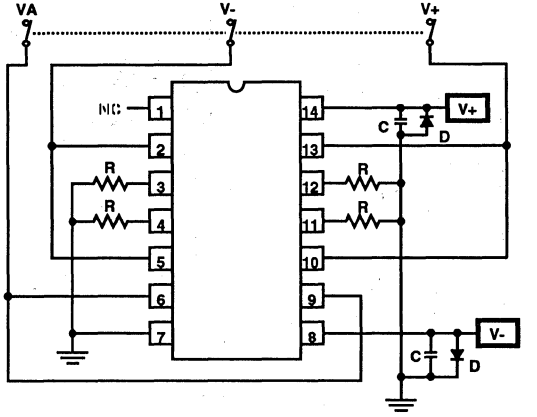
R1 - R8 = 10kΩ ± 5%, 1/4W
V1 = +15V ± 10%
V2 = -15V ± 10%
V3 = +12V ± 10%



HS-384RH/390RH/883S

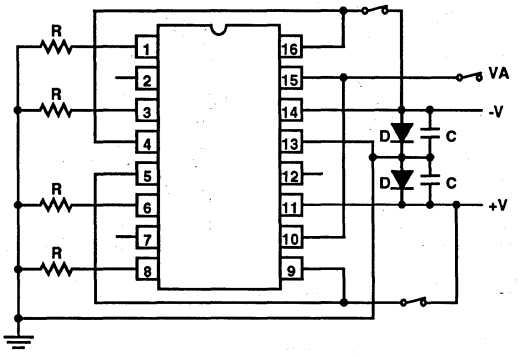
R1 - R8 = 10kΩ ± 5%, 1/4W
V1 = +15V ± 10%
V2 = -15V ± 10%
V3 = +5V ± 10%

Burn-In Circuits



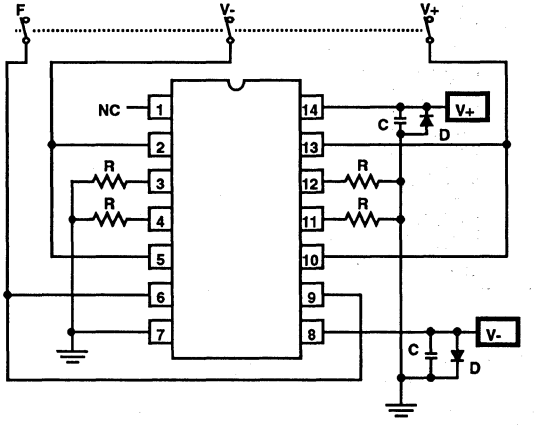
STATIC CONFIGURATION
HS-302RH/303RH/306RH/307RH/883S

R = 10KΩ ± 5%, 1/4W (4 per position)
C = 0.01µF minimum (per position) or 0.1µF minimum per row
D = IN4002 (or equivalent)
+V = +15.5V ± 0.5V, -V = -15.5V ± 0.5V
VA +15.5V ± 0.5V for 306RH/307RH
VA = +5.5V ± 0.5V for 302RH/303RH



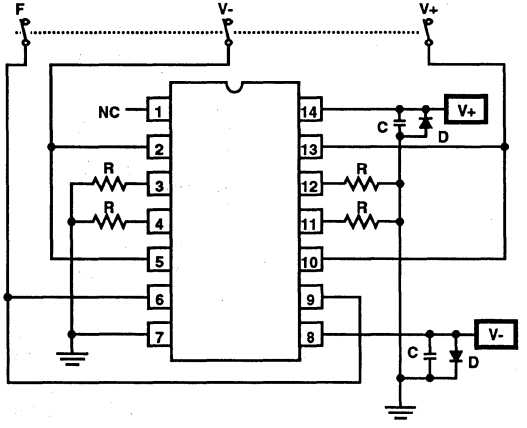
STATIC CONFIGURATION
HS-384RH/390RH/883S

R = 10KΩ ± 5%, 1/4W (4 per position)
C = 0.01µF minimum (per position) or 0.1µF minimum per row
D = IN4002 (or equivalent)
+V = +15.5V ± 0.5V, -V = -15.5V ± 0.5V
VA = +5.5V ± 0.5V



DYNAMIC CONFIGURATION
HS-302RH/303RH/883S

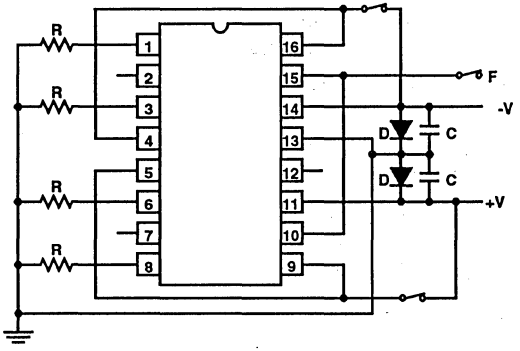
R = 10KΩ ± 5%, 1/4W (4 per position)
C = 0.01µF minimum (per position) or 0.1µF minimum per row
D = IN4002 (or equivalent)
F = 100kHz square wave, 50% duty cycle,
VL = 0.8V, VH = 5.5V
+V = +15.5V ± 0.5V, -V = -15.5V ± 0.5V



DYNAMIC CONFIGURATION
HS-306RH/307RH/883S

R = 10KΩ ± 5%, 1/4W (4 per position)
C = 0.01µF minimum (per position) or 0.1µF minimum per row
D = IN4002 (or equivalent)
F = 100kHz square wave, 50% duty cycle,
VL = 0.8V, VH = 15V
+V = +15.5V ± 0.5V, -V = -15.5V ± 0.5V

Burn-In Circuits (Continued)



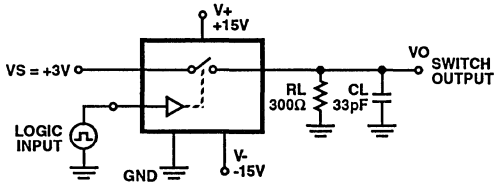
DYNAMIC CONFIGURATION
HS-384RH/390RH/883S

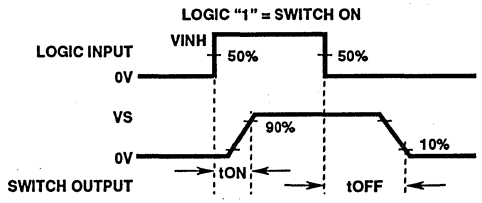
R = 10KΩ ± 5%, 1/4W (4 per position)
C = 0.01µF minimum (per position) or 0.1µF minimum per row
D = IN4002 (or equivalent)
F = 100kHz square wave, 50% duty cycle,
VL = 0.8V, VH = +5.5V
+V = +15.5V ± 0.5V, -V = -15.5V ± 0.5V

Test Circuits

SWITCHING TEST CIRCUIT (tON, tOFF)

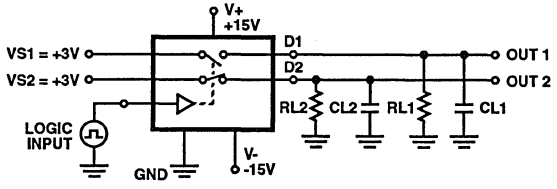
SWITCH TYPE	VINH
HS-302RH/303RH/384RH/390RH/883S	4V
HS-306RH/307RH/883S	15V

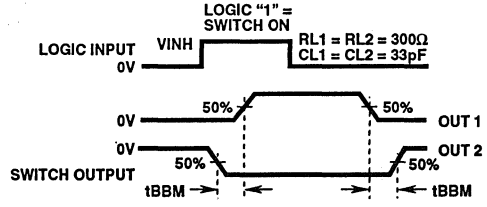




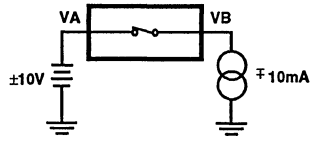
BREAK-BEFORE-MAKE TEST CIRCUIT (tBBM)

SWITCH TYPE	VINH
HS-303RH/390RH/883S	5V
HS-307RH/883S	15V



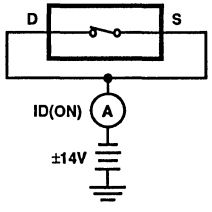


ON RESISTANCE TEST CIRCUIT (RON)

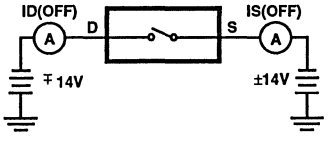


$$RON = \frac{VB - VA}{\pm 10mA}$$

ON LEAKAGE CURRENT TEST CIRCUIT (IDON)



OFF LEAKAGE CURRENT TEST CIRCUIT (ISOFF, IDOFF)



Harris - Space Level Product Flow

SEM - Traceable to Diffusion Method 2018

Wafer Lot Acceptance Method 5007

Internal Visual Inspection (Note 1)

Gamma Radiation Assurance Tests Method 1019

100% Nondestructive Bond Pull Method 2023

Customer Pre-Cap Visual Inspection (Notes 1, 2)

Temperature Cycling Method 1010 Condition C

Constant Acceleration Method 2001 Y1 30KG

Particle Impact Noise Detection method 2020, Condition A 20G

Marking and Serialization

X-Ray Inspection Method 2012

Initial Electrical Tests (T0)

Static Burn-In 72 Hour, +125°C method 1015 Condition A

Room Temperature Electrical Tests (T1)

Burn-In Delta Calculation (T0-T1)

PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ

Dynamic Burn-In 240 Hours, +125°C Method 1015 Condition D

Electrical Tests Subgroups 1, 7, 9 (T2)

Burn-In Delta Calculation (T0 - T2)

PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ

Electrical Test +125°C, -55°C

Alternate Group A Inspection Method 5005

Fine and Gross Leak Tests Method 1014

Customer Source Inspection (Note 2)

Group B Inspection (Notes 2, 4) Method 5005

Group D Inspection (Notes 2, 4) Method 5005

External Visual Inspection Method 2009

Data Package Generation (Note 3)

NOTES:

1. Visual Inspection is performed to MIL-STD-883 Method 2010, Condition A.
2. These steps are optional, and should be listed on the purchase order if required.
3. Data package contains: Assembly Attributes (post seal)
   Test Attributes (includes Group A) -55°C, +25°C, +125°C
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (includes SEM report)
   X-Ray Report and Film
   Test Variables Data, DC Test and TELQV
   +25°C Initial Test
   +25°C Interim Test 1
   +25°C Interim Test 2
   +25°C Delta Over Burn-In
4. Group B data package contains Attributes Data pulse Variables Data, DC Test. Group D data package contains Attributes only.

Metallization Topology

DIE DIMENSIONS:
Die Size: 2130 x 1930
Die Thickness: 11 ±1 mils

METALLIZATION:
Type: Al, 12.5kÅ ± 2kÅ
Back: Gold

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold
Temperature: Sidebrazed Ceramic DIP - 450°C ± 10°C (Max)
Cerpack - 450°C ± 10°C (Max)

WORST CASE CURRENT DENSITY: 1.732e05 A/cm^2

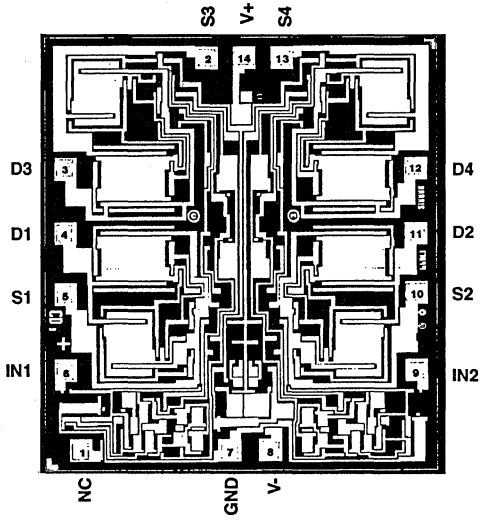
SUBSTRATE POTENTIAL: Unbiased

LEAD TEMPERATURE (10s Soldering): <275°C

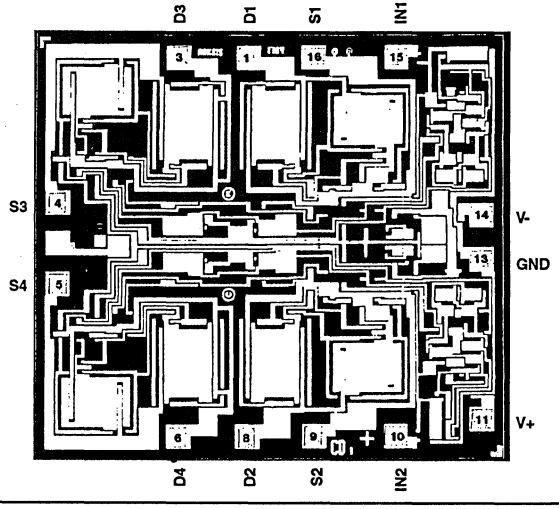
PROCESS: DI Linear Metal Gate CMOS

Metallization Mask Layout

HS-302RH/303RH/306RH/307RH/883S



HS-384RH/390RH/883S



RAD HARD 4

OPERATIONAL AMPLIFIERS

HARRIS SEMICONDUCTOR

HS-3516RH

High Slew Rate, Wideband, Radiation Hardened, Operational Amplifier

December 1992

Features

- Radiation Environment
  - Gamma Rate ($\dot{\gamma}$) 1 x 10^9 RAD(Si)/s
  - Gamma Dose (γ) 1 x 10^6 RAD(Si)
- High Slew Rate >±22V/μs
- Fast Settling Time 130ns
- Unity Gain Bandwidth (Typ) 12MHz
- Low Offset Voltage ±3mV
- Low Power Supply Current 6.5mA
- Dielectrically Isolated Device Islands

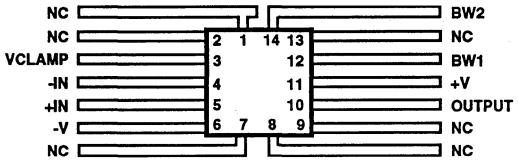
Description

The HS-3516RH is a monolithic, high slew rate, wideband, radiation resistant, operational amplifier. It provides a bandwidth (unity gain stable) of greater than 10MHz and a slew rate in excess of 22V/ms. Optional frequency compensation adjustment is provided. The HS-3516RH has an internal unity gain frequency compensation capacitor which is internally connected. A clamp node feature enables the user to clamp the output voltage via pin 3 which can source or sink up to 3mA for high frequency clamped switching purposes.

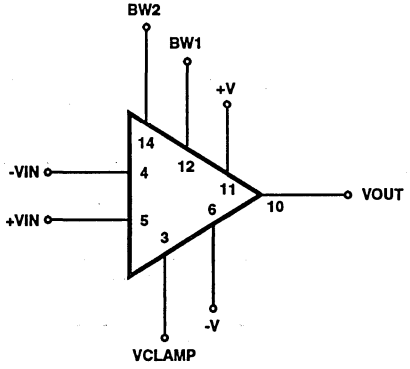
This device is designed to operate from -55°C to +125°C and in both space and strategic-level radiation environments.

Pinout

HS9-3516RH 14 PIN CERAMIC FLATPACK
CASE OUTLINE F2, CONFIGURATION 2
TOP VIEW



Functional Diagram



4 OPERATIONAL AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3023

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage. 7V
Voltage at Either Input Terminal . . . . . V+ to V-
Output Short Circuit Duration (Note 5) . . . . . Indefinite
Junction Temperature (TJ) . . . . . +175°C
Storage Temperature Range . . . . . -65°C to +150°C
ESD Rating. . . . . <2000V
Lead Temperature (Soldering 10s) . . . . . 275°C

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic CERPAK	82°C/W	16.9°C/W

Package Power Dissipation at +75°C for TJ ≤ +175°C
Ceramic Package 1.2W
Package Power Dissipation Derating Factor Above +75°C
Ceramic Package . . . . . 12.2mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . ±5V to ±15V
Operating Temperature Range. . . . . -55°C to +125°C

VINcm ≤ $^1/_2$(V+ = V-)
RL ≥ 2kΩ

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, RSOURCE = 100Ω, RLOAD = 500kΩ, VOUT = 0V. Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	VIO	VCM = 0V	1	+25°C	-3.0	3.0	mV
			2	+125°C	-5.0	5.0	mV
			3	-55°C	-10.0	10.0	mV
Input Bias Current	+IB	VCM = 0V, +RS = 10kΩ, -RS = 100Ω	1	+25°C	-100	100	nA
			2	+125°C	-100	100	nA
			3	-55°C	-500	500	nA
	-IB	VCM = 0V,+RS = 100Ω, -RS = 10kΩ	1	+25°C	-100	100	nA
			2	+125°C	-100	100	nA
			3	-55°C	-500	500	nA
Input Offset Current	IIO	VCM = 0V,+RS = 10kΩ, -RS = 10kΩ	1	+25°C	-100	100	nA
			2	+125°C	-150	150	nA
			3	-55°C	-500	500	nA
Common Mode Range	+CMR	V+ = +5V, V- = -25V	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	-CMR	V+ = 25V, V- = -5V	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
Large Signal Voltage Gain	+AVOL	VOUT = 0V and +10V, RL = 2kΩ	4	+25°C	90	-	dB
			5, 6	+125°C, -55°C	90	-	dB
	-AVOL	VOUT = 0V and -10V, RL = 2kΩ	4	+25°C	90	-	dB
			5, 6	+125°C, -55°C	90	-	dB
Common Mode Rejection Ratio	+CMRR	ΔVCM = +10V, +V = +5V, -V = -25V, VOUT = -10V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	-CMRR	ΔVCM = -10V, +V = +25V, -V = -5V, VOUT = +10V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
Output Voltage Swing	+VOUT	RL = 2kΩ	1	+25°C	12.5	-	V
			2	+125°C	12.5	-	V
			3	-55°C	12.0	-	V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, RSOURCE = 100Ω, RLOAD = 500kΩ, VOUT = 0V. Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing (Continued)	-VOUT	RL = 2kΩ	1	+25°C	-	-11.0	V
			2	+125°C	-	-11.0	V
			3	-55°C	-	-11.0	V
Output Current	+IOUT	VOUT = -10V	1	+25°C	12	-	mA
			2, 3	+125°C, -55°C	12	-	mA
	-IOUT	VOUT = +10V	1	+25°C	-	12	mA
			2, 3	+125°C, -55°C	-	12	mA
Quiescent Power Supply Current	+ICC	VOUT = 0V, IOUT = 0mA	1	+25°C	-	6.5	mA
			2	+125°C	-	6.5	mA
			3	-55°C	-	8.7	mA
	-ICC	VOUT = 0V, IOUT = 0mA	1	+25°C	-6.5	-	mA
			2	+125°C	-6.5	-	mA
			3	-55°C	-8.7	-	mA
Power Supply Rejection Ratio	+PSRR	ΔVSUP = 10V, +V = +10V, -V = -15V, +V = +20V, -V = -15V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	-PSRR	ΔVSUP = 10V, +V = +15V, -V = -10V, +V = +15V, -V = -20V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
Output Short Circuit Current	IOSC	VOUT = 0V	1	+25°C	-	45	mA
			2	+125°C	-	45	mA
			3	-55°C	-	60	mA
Output Clamp Voltage Tolerance	VOC1+	VIN = 1V, VCLAMP = -3.0V, VOC1+ = VOUT - VCLAMP	1	+25°C	-0.4	0.4	V
	VOC2+	VIN = 1V, VCLAMP = -6.0V, VOC2+ = VOUT - VCLAMP	1	+25°C	-0.4	0.4	V
	VOC1-	VIN = -1V, VCLAMP = 3.0V, VOC1- = VOUT - VCLAMP	1	+25°C	-0.4	0.4	V
	VOC2-	VIN = -1V, VCLAMP = 6.0V, VOC2- = VOUT - VCLAMP	1	+25°C	-0.4	0.4	V
Input Clamp Current	ICNL-	VIN = -1V, VCLAMP = 3.0V	1	+25°C	-3.3	-0.25	mA
			2	+125°C	-3.3	-0.18	mA
			3	-55°C	-3.5	-0.30	mA
	ICNH-	VIN = -1V, VCLAMP = 6.0V	1	+25°C	-3.3	-0.25	mA
			2	+125°C	-3.3	-0.18	mA
			3	-55°C	-3.5	-0.30	mA
	ICNL+	VIN = 1V, VCLAMP = -3.0V	1	+25°C	+0.5	+3.0	mA
			2	+125°C	+0.3	+3.0	mA
			3	-55°C	+0.3	+3.2	mA
	ICNH+	VIN = 1V, VCLAMP = -6.0V	1	+25°C	+0.5	+3.0	mA
			2	+125°C	+0.3	+3.0	mA
			3	-55°C	+0.3	+3.2	mA

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, RSOURCE = 50Ω, RLOAD = 2kΩ, CLOAD = 100pF, AVCL = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Slew Rate	+SR	VOUT = ±3V	4	+25°C	22	-	V/µs
	-SR	VOUT = ±3V	4	+25°C	22	-	V/µs
Rise and Fall Time	TR	VOUT = 0V to 1V, 10% ≤ TR ≤ 90%	4	+25°C	-	35	ns
	TF	VOUT = 0V to -1V, 10% ≤ TF ≤ 90%	4	+25°C	-	35	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, RLOAD = 2kΩ, CLOAD = 100pF, AVCL = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Differential Input Resistance	RIN	VCM = 0V	1	+25°C	10	-	MΩ
Full Power Bandwidth	FPBW	VPEAK = 10V	1, 2	+25°C	350	-	kHz
Minimum Closed Loop Stable Gain	CLSG	RL = 2kΩ, CL = 50pF	1	-55°C to +125°C	+1	-	V/V
Output Resistance	ROUT	Open Loop	1	+25°C	-	70	Ω
Quiescent Power Consumption	PC	VOUT = 0V, IOUT = 0mA	1, 3	-55°C to +125°C	-	195	mW
Overshoot	+OS	VOUT = 0V to +1.0V	1	+25°C	-	10	%
	-OS	VOUT = 0V to -1.0V	1	+25°C	-	10	%
Settling Time	TS	To ±5% for a 1V Step	1	+25°C	-	130	ns
Overdrive Recovery Time	TOR		1, 4	+25°C	-	5	µs
Gain Bandwidth Product	GBWP	fO = 1MHz, VO = 200mV, AVCL = 10 V/V	1	+25°C	11	-	MHz

NOTES:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/(2πVPEAK).
3. Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)
4. Overdrive recovery time is the time required for the device to return to linear operation after being overdriven into saturation.
5. Caution: Continuous long duration output short-circuit operation may degrade the operating life of the device.

TABLE 4. POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	1M LIMITS		UNITS
				MIN	MAX	
Open Loop Voltage Gain	AVOL	VSUPPLY = ±15V, ISET = 15µA	25°C	80	-	dB
Input Offset Voltage	VIO	VSUPPLY = ±15V, ISET = 15µA	25°C	-5	+5	mV
Input Bias Current	+IB	VSUPPLY = ±15V, ISET = 15µA	25°C	-400	+400	nA
	-IB	VSUPPLY = ±15V, ISET = 15µA	25°C	-400	+400	nA

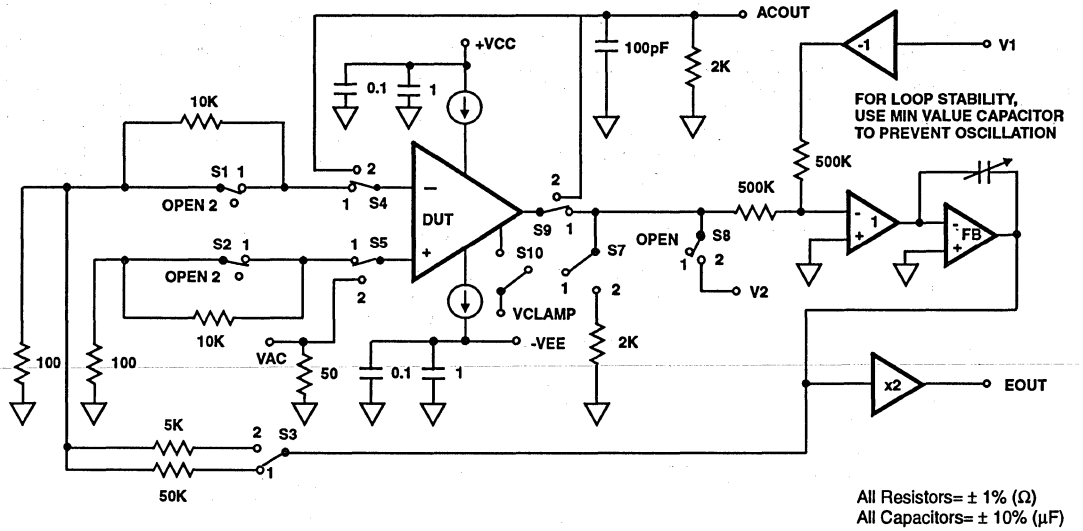
TABLE 5. BURN-IN DELTA PARAMETERS GROUP B, SUBGROUP 5 (T_A = +25°C)

PARAMETERS	DELTA LIMITS
VIO	±1mV
IBIAS	±50nA

TABLE 6. APPLICABLE SUBGROUPS

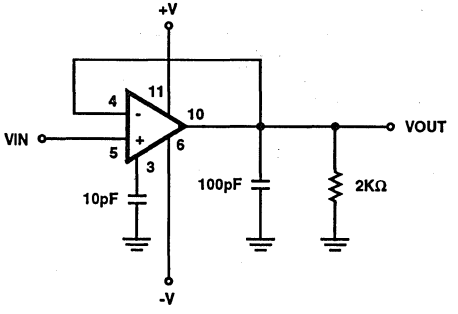
CONFORMANCE GROUPS		METHOD	Q SUBGROUPS
Initial Test		100%/5004	1, 4
Interim Test		100%/5004	1
PDA		100%/5004	1
Final Test		100%/5004	1, 2, 3, 4, 5, 6
Group A		Samples/5005	1, 2, 3, 4, 5, 6
Group B	B5	Samples/5005	1, 2, 3
	Others	Samples/5005	1
Group D		Samples/5005	1
Group E, Subgroup 2		Samples/5005	1

Test Circuit

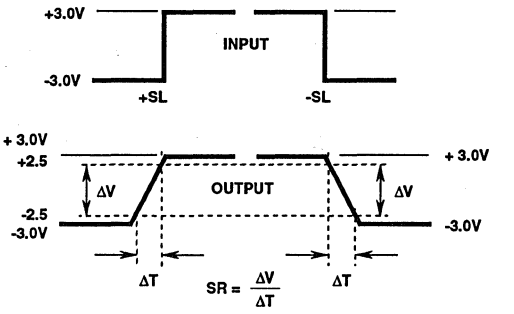


Simplified Test Circuits and Waveforms

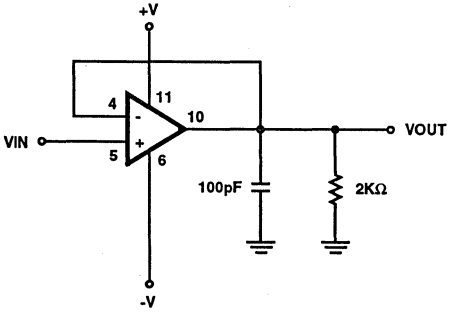
SLEW RATE CIRCUIT



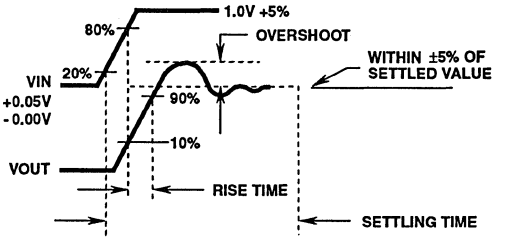
SLEW RATE WAVEFORMS



OVERSHOOT, RISE/FALL/SETTLING TIME CIRCUIT

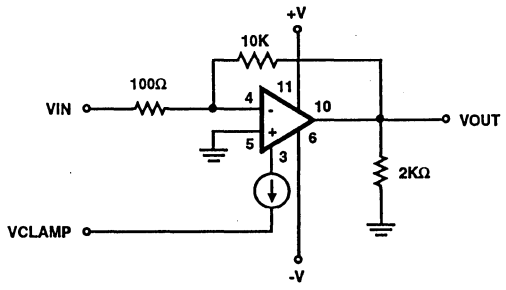


OVERSHOOT, RISE/SETTLING TIME WAVEFORMS

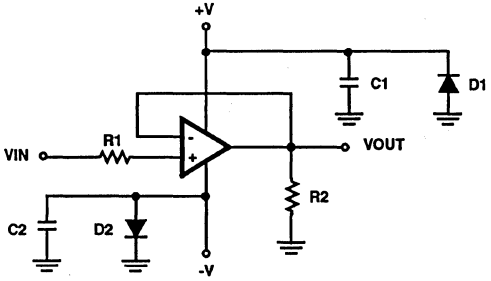


Simplified Test Circuits and Waveforms (Continued)

VOLTAGE CLAMP CIRCUIT



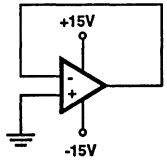
Burn-In Circuit



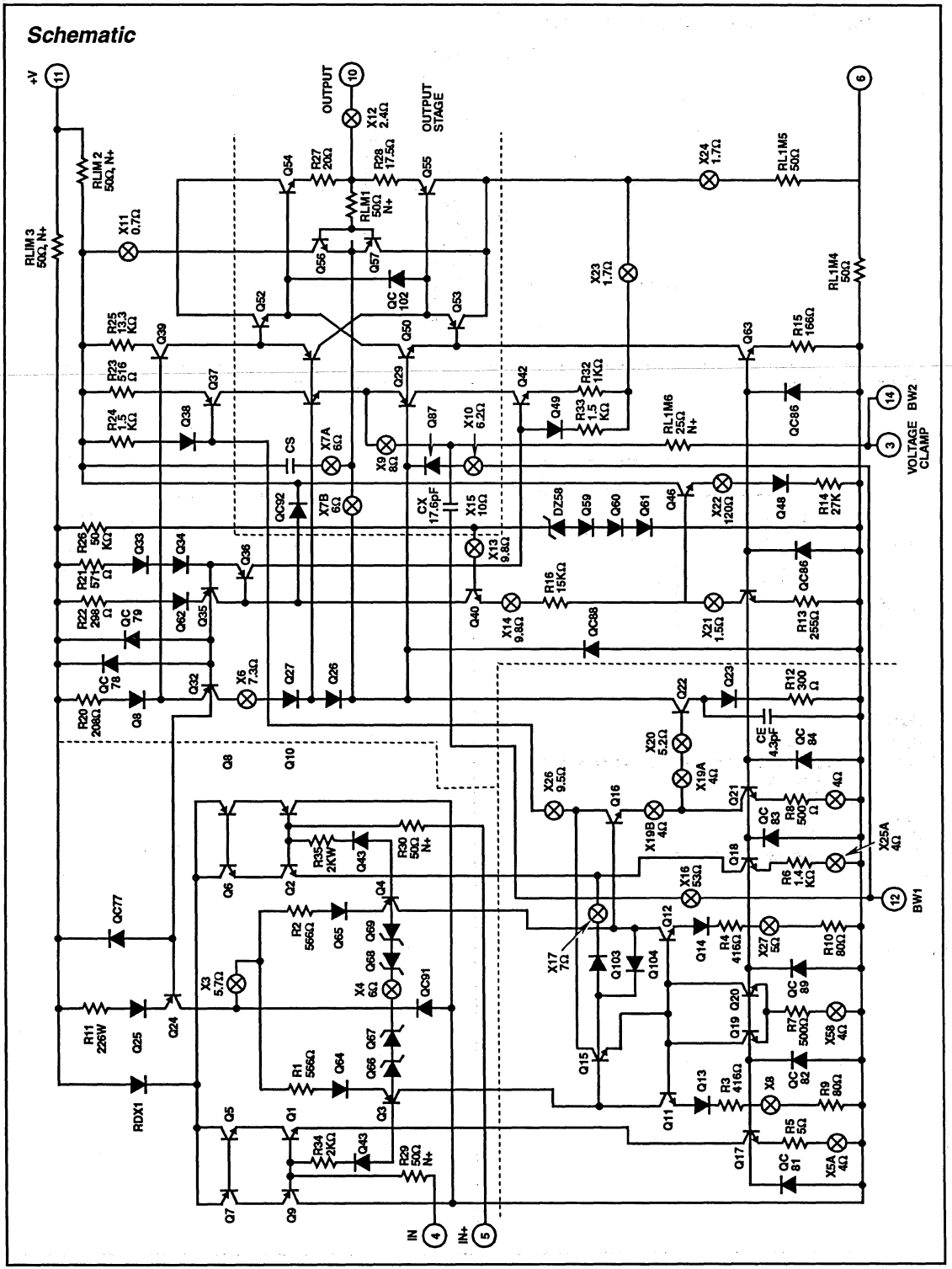
NOTES:

I(+V) - (-V)I = 31V ±1V
VIN = 50kHz Square Wave, 50% Duty Cycle, -3.0V to +3.0V
(All Tolerance ±10%)
R1 = 47kΩ, 5% $^1/_4$W (Min)
R2 = 510Ω, 5%, $^1/_4$W (Min)
C1 = C2 = 0.01µF (Min)
D1 = D2 = IN4002 or Equivalent/Board

Irradiation Circuit



Schematic


+V
OUTPUT
OUTPUT STAGE
VOLTAGE CLAMP
BW1
BW2
IN
IN+
RLIM 3 50Ω, N+
RLIM 2 50Ω, N+
RLIM1 50Ω N+
RL1M5 50Ω
RL1M4 50Ω
RL1M6 25Ω N+
X11 0.7Ω
X12 2.4Ω
X23 1.7Ω
X24 1.7Ω
R27 20Ω
R28 17.5Ω
R25 133 KΩ
R23 516 Ω
R24 1.5 KΩ
R32 1KΩ
R33 1.5 KΩ
R15 166Ω
R14 27K
R26 50 KΩ
R21 571 Ω
R22 298 Ω
R16 15KΩ
R13 255Ω
R12 300 Ω
R20 208Ω
R8 500 Ω
R6 1.4 KΩ
R35 2KW
R30 50Ω N+
R2 556Ω
R4 416Ω
R10 80Ω
R11 226W
R7 500Ω
R1 556Ω
R3 416Ω
R9 80Ω
R34 2KΩ
R29 50Ω N+
R5 5Ω
X7A 6Ω
X7B 6Ω
X9 8Ω
X10 6.2Ω
X15 10Ω
X13 9.8Ω
X14 9.8Ω
X22 120Ω
X21 1.5Ω
X5 7.3Ω
X20 5.2Ω
X19A 4Ω
X19B 4Ω
X26 9.5Ω
X16 53Ω
X17 7Ω
X3 5.7Ω
X4 6Ω
X8
X27 5Ω
X58 4Ω
X5A 4Ω
X25A 4Ω
CS
CX 17.6pF
CE 4.3pF
DZ58
QC 102
QC 79
QC 78
QC 84
QC 83
QC 89
QC 82
QC 81
QC77
QC91
RDX1

Harris - Space Level Product Flow

SEM - Traceable to Diffusion Method 2018

Wafer Lot Acceptance Method 5007

Internal Visual Inspection (Note 1)

Gamma Radiation Assurance Tests Method 1019

100% Nondestructive Bond Pull Method 2023

Customer Pre-Cap Visual Inspection (Notes 1, 2)

Temperature Cycling Method 1010 Condition C

Constant Acceleration method 2001 Y1 30KG

Particle Impact Noise Detection method 2020, Condition A 20G

Marking and Serialization

X-Ray Inspection Method 2012

Initial Electrical Tests (T0)

Static Burn-In 240 Hours, +125°C Method 1015 Condition A

Electrical Tests Subgroups 1, 7, 9 (T1)

Burn-In Delta Calculation (T0 - T1)

PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ

Electrical Test +125°C, -55°C

Alternate Group A Inspection Method 5005

Fine and Gross Leak Tests Method 1014

Customer Source Inspection (Note 2)

Group B Inspection (Notes 2, 4) Method 5005

Group D Inspection (Notes 2, 4) Method 5005

External Visual Inspection Method 2009

Data Package Generation (Note 3)

NOTES:

1. Visual Inspection is performed to MIL-STD-883 Method 2010, Condition A.
2. These steps are optional, and should be listed on the purchase order if required.
3. Data package contains: Assembly Attributes (post seal)
   Test Attributes (includes Group A) -55°C, +25°C, +125°C
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (includes SEM report)
   X-Ray Report and Film
   Test Variables Data, DC Test and TELQV
   +25°C Initial Test
   +25°C Interim Test 1
   +25°C Delta Over Burn-In
4. Group B data package contains Attributes Data pulse Variables Data, DC Test and TE2HQV. Group D data package contains Attributes only.

Metallization Topology

DIE DIMENSIONS:
93 x 93 x 11mils
(2360 x 2360 x 280µm)

METALLIZATION:
Type: Al
Thickness: 12.5kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP - 400°C (Max)

WORST CASE CURRENT DENSITY:
1.385 x 10^5 A/cm^2 at 12mA

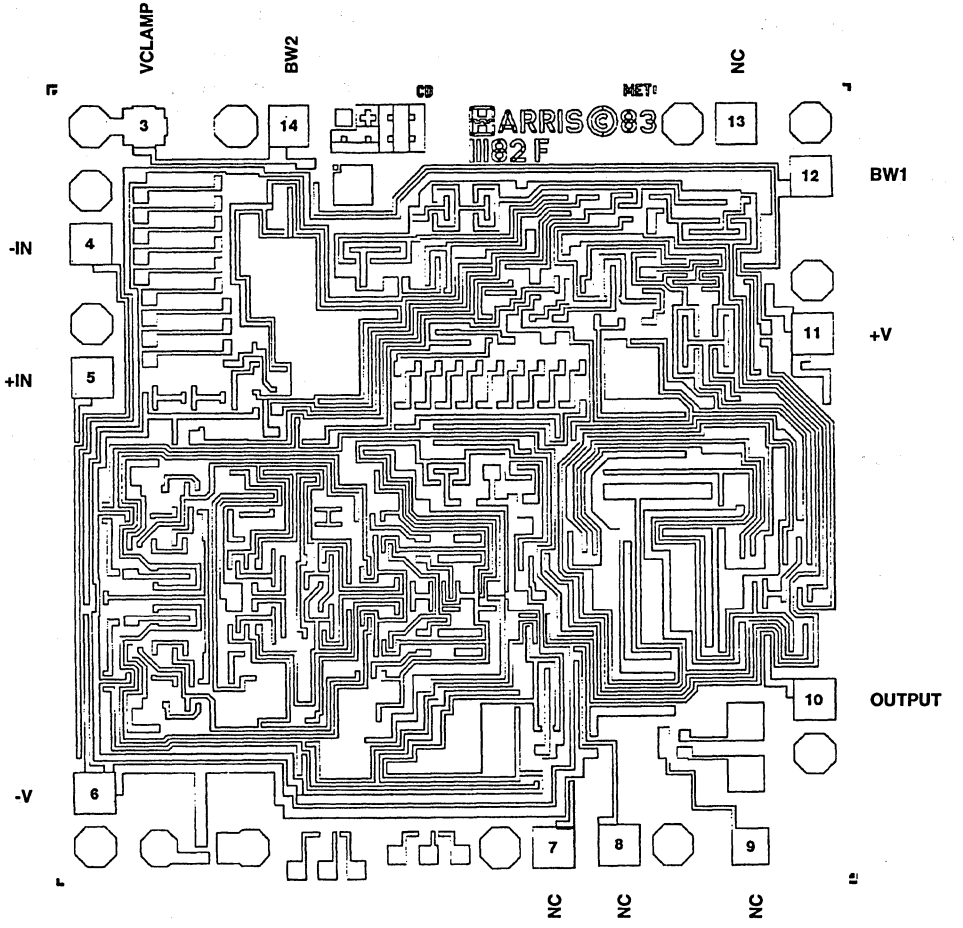
SUBSTRATE POTENTIAL (POWERED UP): -V

TRANSISTOR COUNT: 84

PROCESS: High Frequency Linear

Metallization Mask Layout

HS-3516RH



HARRIS SEMICONDUCTOR

HS-3530RH

Low Power, Radiation Hardened Programmable Operational Amplifier

December 1992

Features

- Radiation Environment
  - Gamma Rate ($\dot{\gamma}$) 1 x 10^9 RAD (Si)/s
  - Gamma Dose (γ) 1 x 10^6 RAD (Si)
- Wide Range AC Programming
  - Slew Rate 0.06 to 3V/μs
  - Gain X Bandwidth 100KHz to 5.0MHz
- Wide Range DC Programming
  - Power Supply Range ±3.0V to ±15V
- Supply Current 10μA to 1.2mA
- Dielectrically Isolated Device Islands
- Short Circuit Protection

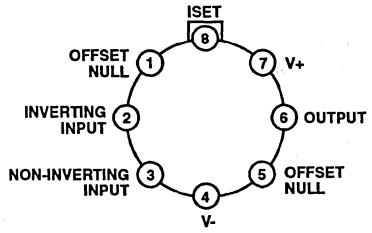
Description

The HS-3530RH is a Low Power Operational Amplifier which is an internally compensated monolithic device offering a wide range of performance specifications. Parameters such as power dissipation, slew rate, bandwidth, noise and input DC parameters are programmed by selecting an external resistor or current source. Supply voltages as low as ±3 volts may be used with little degradation of AC performance. The HS-3530RH has been specifically designed to meet exposure to space radiation environments. Operation from -55°C to +125°C is guaranteed.

A major advantage of the HS-3530RH is that operating characteristics remain virtually constant over a wide supply range (±3V to ±15V), allowing the amplifier to offer maximum performance in almost any system, including battery operated equipment. A primary application for this device is in active filtering and conditioning for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the set current, it can be used for designs such as current controlled oscillators/modulators, sample and hold circuits and variable active filters.

Pinout

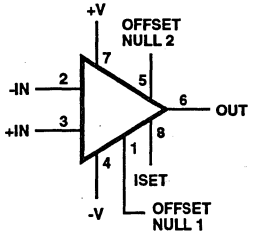
HS2-3530RH 8 PIN METAL CAN
TOP VIEW



NOTES:

1. Case tied to V-.
2. Compliant to MIL-M-38510, package outline A-1.

Functional Diagram



4 OPERATIONAL AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3024

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 20V
Voltage at Either Input Terminal . . . . . V+ to V-
ISET (Current at ISET) 500µA
VSET (Voltage to GND at ISET) . . . . . (V+ -2.0V) < VSET < V+
Output Short Circuit Duration (Note 1) . . . . . Indefinite
Junction Temperature (TJ) . . . . . +175°C
Storage Temperature Range . . . . . -65°C to +150°C
ESD Rating . . . . . <2000V
Lead Temperature (Soldering 10 sec) . . . . . 275°C

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Metal Can Package	75°C/W	12°C/W

Package Power Dissipation at +75°C for TJ < +175°C
Metal Can Package 0.9W
Package Power Dissipation Derating Factor Above +75°C
Metal Can Package . . . . . 9mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range . . . . . -55°C to +125°C
Operating Supply Voltage . . . . . ±3V to ±15V

VINcm ≤ $^1/_2$ (V+ - V-)
RL ≥ 2kV

TABLE 1A. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, RSOURCE = 100Ω, RLOAD = 500kΩ, VOUT = 0V, Unless Otherwise Specified.

DC PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS ISET = 1.5µA MIN	LIMITS ISET = 1.5µA MAX	LIMITS ISET = 15µA MIN	LIMITS ISET = 15µA MAX	UNITS
Input Offset Voltage	VIO	VCM = 0V	1	+25°C	-3	3	-3	3	mV
			2, 3	+125°C, -55°C	-5	5	-5	5	mV
Input Bias Current	+IB	VCM = 0V, +RS = 10kΩ -RS = 100Ω	1	+25°C	-	-	-20	20	nA
			2, 3	+125°C, -55°C	-	-	-40	40	nA
	-IB	VCM = 0V, +RS = 100Ω -RS = 10kΩ	1	+25°C	-	-	-20	20	nA
			2, 3	+125°C, -55°C	-	-	-40	40	nA
Input Offset Current	IIO	VCM = 0V, +RS = 10kΩ -RS = 10kΩ	1	+25°C	-	-	-5	5	nA
			2, 3	+125°C, -55°C	-	-	-10	10	nA
Large Signal Voltage Gain	+AVOL	VOUT = 0V and +10V Note 1	4	+25°C	65	-	80	-	kV/V
			5, 6	+125°C, -55°C	25	-	50	-	kV/V
	-AVOL	VOUT = 0V and -10V Note 1	4	+25°C	65	-	80	-	kV/V
			5, 6	+125°C, -55°C	25	-	50	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔVCM = +5V, +V = +10V -V = -20V, VOUT = -5V	1	+25°C	80	-	80	-	dB
			2, 3	+125°C, -55°C	80	-	80	-	dB
	-CMRR	ΔVCM = -5V, +V = +20V -V = -10V, VOUT = +5V	1	+25°C	80	-	80	-	dB
			2, 3	+125°C, -55°C	80	-	80	-	dB
Output Voltage Swing	+VOUT	Note 1	1	+25°C	12.5	-	12.5	-	V
			2, 3	+125°C, -55°C	10.5	-	10.5	-	V
	-VOUT	Note 1	1	+25°C	-	-12.5	-	-12.5	V
			2, 3	+125°C, -55°C	-	-10.5	-	-10.5	V
Output Current	+IOUT	RL = 2kΩ	1	+25°C	2.5	-	2.5	-	mA
	-IOUT	RL = 2kΩ	1	+25°C	-	-2.5	-	-2.5	mA
Quiescent Power Supply Current	+ICC	VOUT = 0V IOUT =0mA	1	+25°C	-	15	-	150	µA
			2, 3	+125°C, -55°C	-	15	-	160	µA
	-ICC	VOUT = 0V IOUT =0mA	1	+25°C	-15	-	-150	-	µA
			2, 3	+125°C, -55°C	-15	-	-160	-	µA

TABLE 1A. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, RSOURCE = 100Ω, RLOAD = 500kΩ, VOUT = 0V, Unless Otherwise Specified.

DC PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS ISET = 1.5µA MIN	LIMITS ISET = 1.5µA MAX	LIMITS ISET = 15µA MIN	LIMITS ISET = 15µA MAX	UNITS
Power Supply Rejection Ratio	+PSRR	ΔVSUP = 10V +V = +10V, -V = -15V +V = +20V, -V = -15V	1	+25°C	80	-	80	-	dB
			2, 3	+125°C, -55°C	80	-	80	-	dB
	-PSRR	ΔVSUP = 10V +V = +15V, -V = -10V +V = +15V, -V = -20V	1	+25°C	80	-	80	-	dB
			2, 3	+125°C, -55°C	80	-	80	-	dB

NOTE:

1. RL = 75Ω at ISET = 1.5µA, RL = 5kΩ at ISET = 15µA.

TABLE 1B. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±3V, RSOURCE = 100Ω, RLOAD = 500kΩ, VOUT = 0V, Unless Otherwise Specified.

DC PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS ISET = 1.5µA MIN	LIMITS ISET = 1.5µA MAX	LIMITS ISET = 15µA MIN	LIMITS ISET = 15µA MAX	UNITS
Input Offset Voltage	VIO	VCM = 0V	1	+25°C	-3	3	-3	3	mV
			2, 3	+125°C, -55°C	-5	5	-5	5	mV
Large Signal Voltage Gain	+AVOL	VOUT = 0V and +1V Note 1	4	+25°C	25	-	25	-	kV/V
			5, 6	+125°C, -55°C	15	-	25	-	kV/V
	-AVOL	VOUT = 0V and -1V Note 1	4	+25°C	25	-	25	-	kV/V
			5, 6	+125°C, -55°C	15	-	25	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔVCM = +1.5V +V = +1.5V, -V = -4.5V VOUT = -1.5V	1	+25°C	80	-	80	-	dB
			2, 3	+125°C, -55°C	80	-	80	-	dB
	-CMRR	ΔVCM = -1.5V +V = +4.5V, -V = -1.5V VOUT = +1.5V	1	+25°C	80	-	80	-	dB
			2, 3	+125°C, -55°C	80	-	80	-	dB
Output Voltage Swing	+VOUT	Note 1	1	+25°C	2.0	-	2.0	-	V
			2, 3	+125°C, -55°C	2.0	-	2.0	-	V
	-VOUT	Note 1	1	+25°C	-	-2.0	-	-2.0	V
			2, 3	+125°C, -55°C	-	-2.0	-	-2.0	V
Quiescent Power Supply Current	+ICC	VOUT = 0V IOUT = 0mA	1	+25°C	-	15	-	150	µA
			2, 3	+125°C, -55°C	-	15	-	160	µA
	-ICC	VOUT = 0V IOUT = 0mA	1	+25°C	-15	-	-150	-	µA
			2, 3	+125°C, -55°C	-15	-	-160	-	µA
Power Supply Rejection Ratio	+PSRR	ΔVSUP = 1.5V +V = +3V, -V = -3V +V = +4.5V, -V = -3V	1	+25°C	80	-	80	-	dB
			2, 3	+125°C, -55°C	80	-	80	-	dB
	-PSRR	DVSUP = 1.5V +V = +3V, -V = -3V +V = +3V, -V = -4.5V	1	+25°C	80	-	80	-	dB
			2, 3	+125°C, -55°C	80	-	80	-	dB

NOTE:

1. RL = 75Ω at ISET = 1.5µA, RL = 5kΩ at ISET = 15µA.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: RSOURCE = 50Ω, CL = 100pF, AVCL = +1, RL = 5kΩ, Unless Otherwise Specified.

AC PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS				UNITS
					ISET = 1.5µA		ISET = 15µA		
					MIN	MAX	MIN	MAX	
VSUPPLY = ±15V									
Slew Rate Note 1	+SR	VOUT = -10V to +10V	4	+25°C	0.025	-	0.25	-	V/µs
	-SR	VOUT = +10V to -10V	4	+25°C	0.025	-	0.25	-	V/µs
Rise & Fall Time	TR	VOUT = 0 to +400mV 10% < TR < 90%	4	+25°C	-	8.0	-	0.8	µs
	TF	VOUT = 0 to -400mV 10% < TF < 90%	4	+25°C	-	6.0	-	0.6	µs
Overshoot	+OS	VOUT = 0 to +400mV	4	+25°C	-	35	-	35	%
	-OS	VOUT = 0 to -400mV	4	+25°C	-	35	-	35	%
VSUPPLY = ±3V									
Slew Rate Note 1	+SR	VOUT = -2V to +2V	4	+25°C	0.01	-	0.1	-	V/µs
	-SR	VOUT = 2V to -2V	4	+25°C	0.01	-	0.1	-	V/µs

NOTE:

1. RL = 20Ω at ISET = 1.5µA.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: RSOURCE = 50Ω, CL = 100pF, AVCL = +1, Unless Otherwise Specified.

AC PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS				UNITS
					ISET = 1.5µA		ISET = 15µA		
					MIN	MAX	MIN	MAX	
VSUPPLY = ±15V									
Differential Input Resistance	RIN	VCM = 0V	1	+25°C	50	-	50	-	MΩ
Full Power Bandwidth	FPBW	VPEAK = 10V	1, 2	+25°C	0.4	-	4	-	kHz
Minimum Closed Loop Stable Gain	CLSG	RL = 2kΩ, CL = 50pF	1	-55°C to +125°C	+1	-	+1	-	V/V
Output Resistance	ROUT	Open Loop	1	+25°C	-	10	-	10	Ω
Quiescent Power Consumption	PC	VOUT = 0V, IOUT = 0mA	1, 3	-55°C to +125°C	-	4.8	-	4.8	mW
Output Short-Circuit Current	IOSC	VOUT = 0V	1, 4	+25°C	-14	38	-27	42	mA
Gain Bandwidth Product	GBWP	AVCL = 10V/V VO = 200mV, fO = 10kHz	1	+25°C	45	-	750	-	kHz
VSUPPLY = ±3V									
Gain Bandwidth Product	GBWP	AVCL = 10V/V VO = 200mV, fO = 10kHz	1	+25°C	30	-	600	-	kHz

NOTES:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/(2πVPEAK).
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs).
4. Caution: Continuous long-duration short-circuit operation may degrade the operating life of the device.

TABLE 4. POST RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

DC PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Open Loop Voltage Gain	AVOL	VSUPPLY = ±15V ISET = 15µA, RL = 25kΩ	+25°C	20	-	kV/V
Input Offset Voltage	VIO	VSUPPLY = ±15V ISET = 15µA, RL = 25kΩ	+25°C	-	3.5	mV

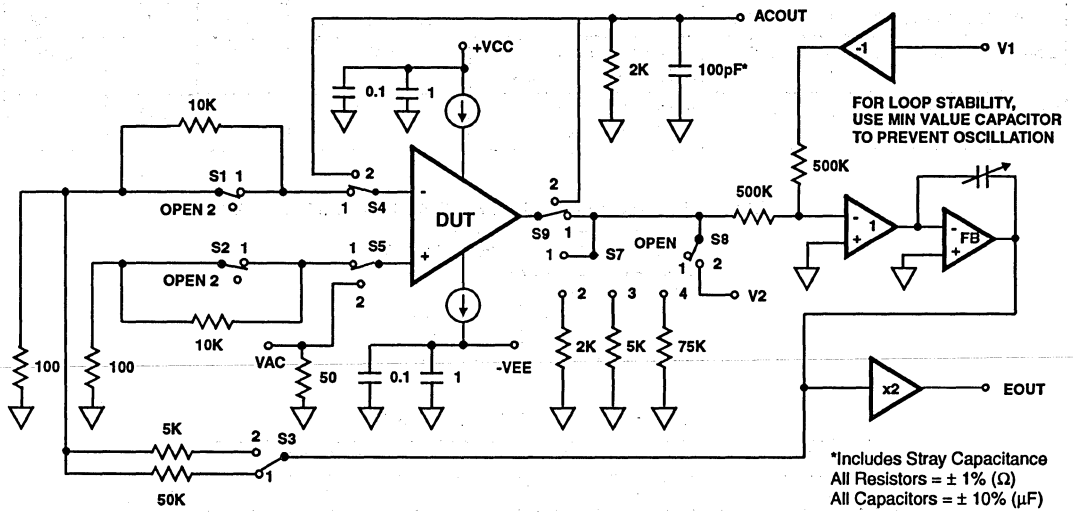
TABLE 5. BURN-IN DELTA PARAMETERS GROUP B, SUBGROUPS 5 (T_A = +25°C)

PARAMETERS	DELTA LIMITS
VIO	±1mV
IBIAS	±10nA

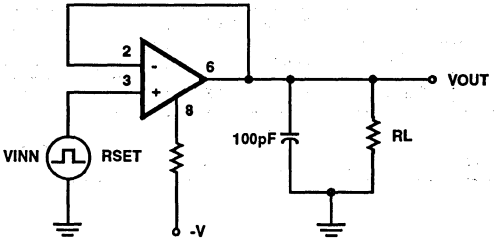
TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	Q SUBGROUPS
Initial Test		100%/5004	1, 4
Interim Test		100%/5004	1
PDA		100%/5004	1
Final Test		100%/5004	1, 2, 3, 4, 5, 6
Group A		Samples/5005	1, 2, 3, 4, 5, 6
Group B	B5	Samples/5005	1, 2, 3
	Others	Samples/5005	1
Group D		Samples/5005	1
Group E, Subgroup 2		Samples/5005	1

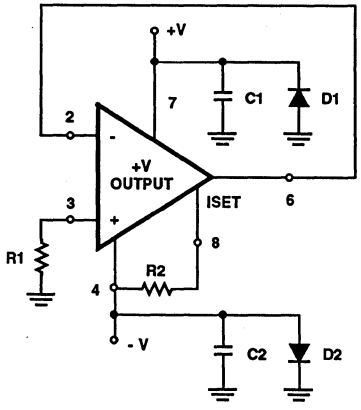
Test Circuit



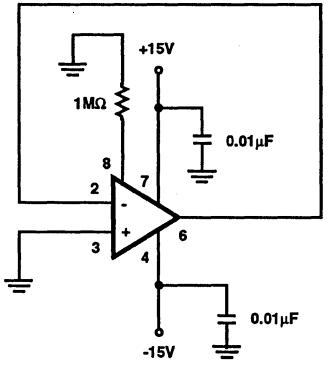
Simplified Transient Response/Slew Rate Circuit



Burn-In Circuit

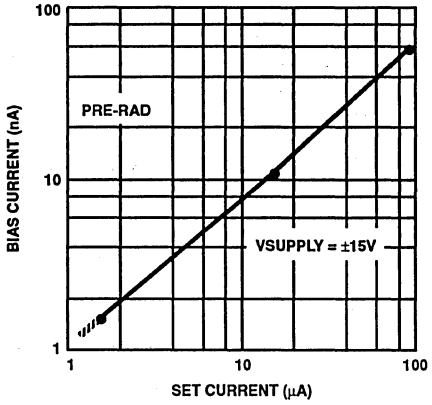


Irradiation Circuit

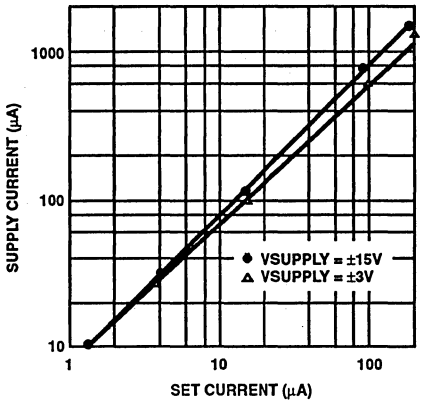


Typical Performance Curves

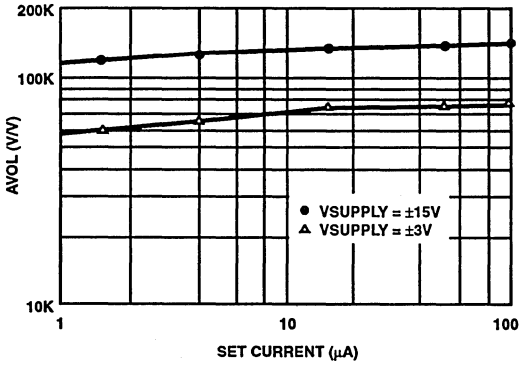
INPUT BIAS CURRENT vs SET CURRENT



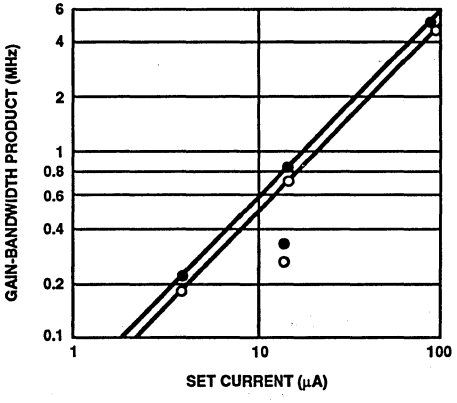
PRERAD POSITIVE SUPPLY CURRENT



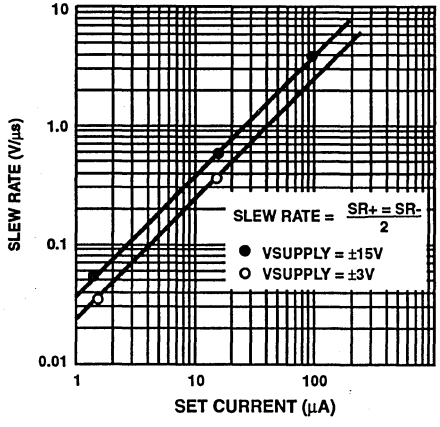
PRERAD LARGE SIGNAL VOLTAGE GAIN vs ISET



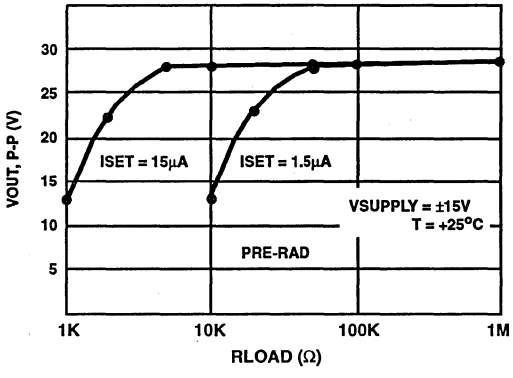
GAIN BANDWIDTH PRODUCT vs SET CURRENT



SLEW RATE vs SET CURRENT



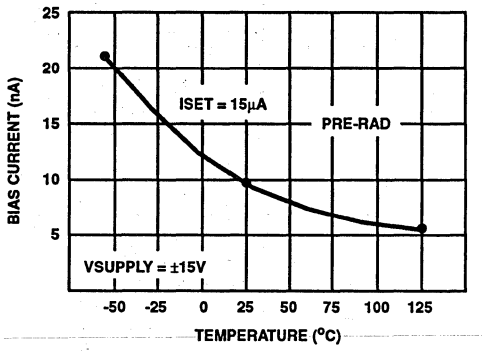
OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



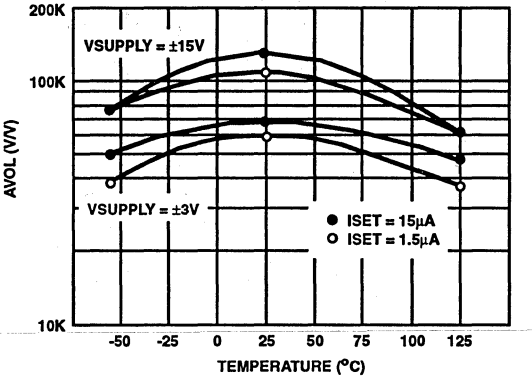
4 OPERATIONAL AMPLIFIERS

Typical Performance Curves (Continued)

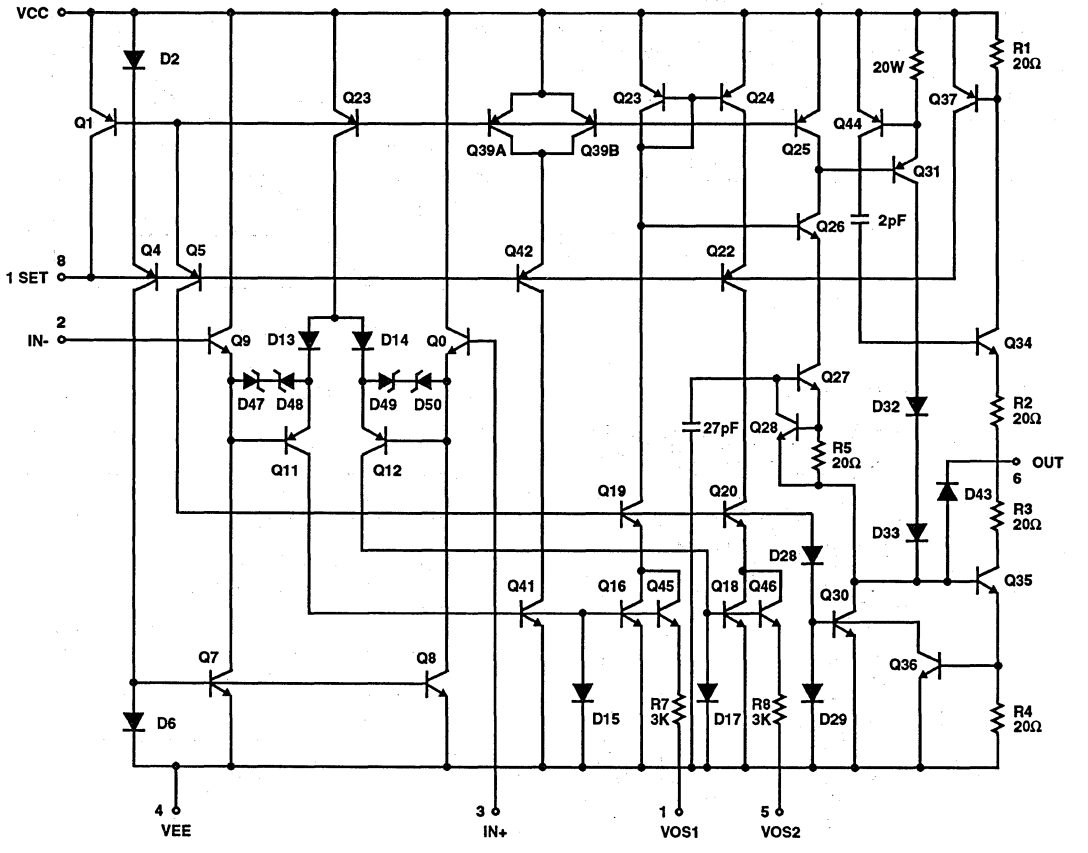
INPUT BIAS CURRENT vs TEMPERATURE



OPEN LOOP VOLTAGE GAIN vs TEMPERATURE



Schematic



Harris - Space Level Product Flow

SEM - Traceable to Diffusion Method 2018

Wafer Lot Acceptance Method 5007

Internal Visual Inspection (Note 1)

Gamma Radiation Assurance Tests Method 1019

100% Nondestructive Bond Pull Method 2023

Customer Pre-Cap Visual Inspection (Notes 1, 2)

Temperature Cycling Method 1010 Condition C

Constant Acceleration method 2001 Y1 30KG

Particle Impact Noise Detection method 2020, Condition A 20G

Marking and Serialization

X-Ray Inspection Method 2012

Initial Electrical Tests (T0)

Static Burn-In 240 Hours, +125°C Method 1015 Condition A

Electrical Tests Subgroups 1, 7, 9 (T1)

Burn-In Delta Calculation (T0 - T1)

PDA Calculation 3% Functional
5% Subgroups 1, 7, D

Electrical Test +125°C, -55°C

Alternate Group A Inspection Method 5005

Fine and Gross Leak Tests Method 1014

Customer Source Inspection (Note 2)

Group B Inspection (Notes 2, 4) Method 5005

Group D Inspection (Notes 2, 4) Method 5005

External Visual Inspection Method 2009

Data Package Generation (Note 3)

NOTES:

1. Visual Inspection is performed to MIL-STD-883 Method 2010, Condition A.
2. These steps are optional, and should be listed on the purchase order if required.
3. Data package contains: Assembly Attributes (post seal)
   Test Attributes (includes Group A) -55°C, +25°C, +125°C
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (includes SEM report)
   X-Ray Report and Film
   Test Variables Data, DC Test and TELQV
   +25°C Initial Test
   +25°C Interim Test 1
   +25°C Delta Over Burn-In
4. Group B data package contains Attributes Data pulse Variables Data, DC Test and TE2HQV. Group D data package contains Attributes only.

Metallization Topology

DIE DIMENSIONS:
54 x 67 x 11.5mils
(1370 x 1700 x 290µm)

METALLIZATION:
Type: Al
Thickness: 12.5kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Metal Can - 420°C (Max)

WORST CASE CURRENT DENSITY:
0.544 x 10^5 A/cm^2 at 2.5mA

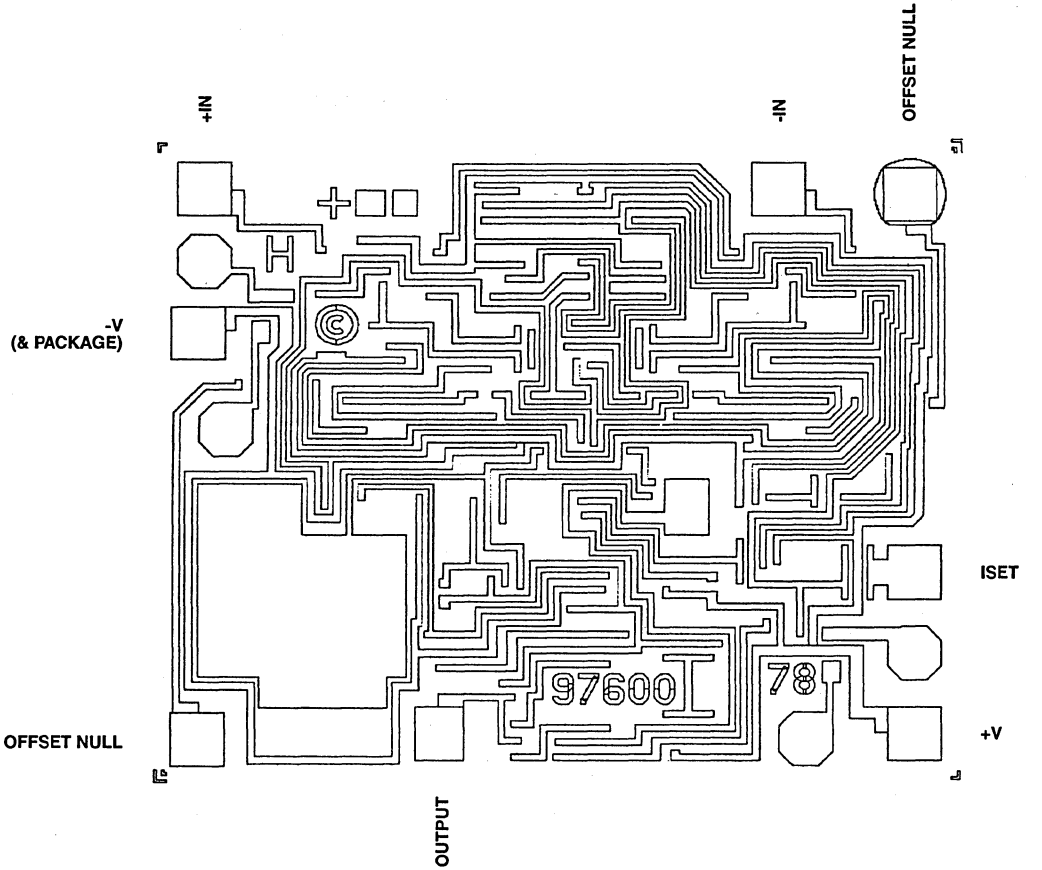
SUBSTRATE POTENTIAL (POWERED UP): -V

TRANSISTOR COUNT: 49

PROCESS: Complimentary Bipolar

Metallization Mask Layout

HS-3530RH



HARRIS SEMICONDUCTOR

HS-5104RH

Radiation Hardened Low Noise Quad Operational Amplifier

December 1992

Features

- Radiation Environment
  - Gamma Rate ($\dot{\gamma}$) 1 x 10^9 RAD (Si)/s
  - Gamma Dose (γ) 1 x 10^5 RAD (Si)
- Low Noise
- At 1kHz 3.5nV/$\sqrt{Hz}$ (Typ)
- At 1kHz 0.5pA/$\sqrt{Hz}$ (Typ)
- Low Offset Voltage 3.0mV
- High Slew Rate 2.5V/μs (Typ)
- Gain Bandwidth Product 6.5MHz (Typ)
- Dielectrically Isolated Bipolar Technology
- Single 5V Supply Capability

Applications

- High Q, Active Filters
- Audio Amplifiers
- Voltage Regulators
- Integrators
- Signal Generators
- Voltage References
- Space and Reactor Environments

Description

The HS-5104RH is a radiation hardened, dielectrically isolated bipolar monolithic quad operational amplifier that provides low noise operation in a radiation hardened design. The predominant feature of the HS-5104RH is its excellent noise characteristics, typically only 3.5nV/$\sqrt{Hz}$ and 0.5pA/$\sqrt{Hz}$ at 1kHz. This general purpose amplifier also offers an array of dynamic specifications ranging from a typical 2.5V/μs slew rate and a 6.5MHz unity gain bandwidth to a minimum output drive current of 10mA.

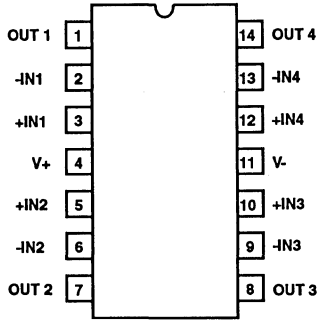
The HS-5104RH shows almost no change in offset voltage after exposure to 100K rad(Si) gamma radiation, with only a minor increase in current. Complementing these specifications is a post radiation open loop gain in excess of 40K.

This impressive combination of features makes this amplifier ideally suited for a variety of applications such as active filter design, signal conditioning, and instrumentation circuits. Designed to meet exposure in radiation environments, this amplifier is a necessity for satellite, spacecraft, and nuclear power systems where its unique properties will prolong the useful life of a system.

This quad operational amplifier is available in an industry standard pinout allowing for immediate interchangeability with most other quad operational amplifiers.

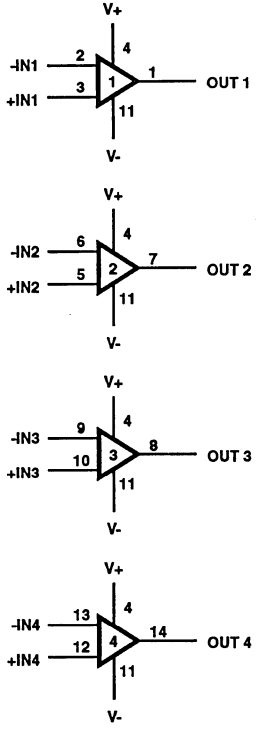
Pinout

HS1-5104RH
(14 PIN CERAMIC SIDEBRAZED DIP)
TOP VIEW



COMPLIANT TO MIL-M-38510 PACKAGE OUTLINE D-1

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3025

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 7V
Voltage at Either Input Terminal . . . . . V+ to V-
Peak Output Current (Note 5) . . . . . Indefinite
(One Amplifier Shorted to GND)
Junction Temperature (TJ) . . . . . +175°C
Storage Temperature Range . . . . . -65°C to +150°C
ESD Rating . . . . . <2000V
Lead Temperature (Soldering 10s) . . . . . +275°C

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic Sidebraze Package	75°C/W	12°C/W

Package Power Dissipation at +75°C for TJ ≤ +175°C
Ceramic Sidebraze Package 1.3W
Package Power Dissipation Derating Factor Above +75oC
Ceramic Sidebraze Package . . . . . 13mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range . . . . . -55°C to +125°C
Operating Supply Voltage . . . . . ±5V to ±15V

VINcm ≤ 1/2 (V+ - V-)
RL ≥ 2kΩ

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ± 15V, RSOURCE = 100Ω, RLOAD = 100kΩ, VOUT = 0V, Unless Otherwise Specified

DC PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	VIO	VCM = 0V	1	+25°C	-3.0	3.0	mV
			2, 3	+125°C, -55°C	-15.0	15.0	mV
Input Bias Current	+IB	VCM = 0V, +RS = 10kΩ, -RS = 100Ω	1	+25°C	-300	300	nA
			2, 3	+125°C, -55°C	-550	550	nA
	-IB	VCM = 0V, +RS = 100Ω, -RS = 10kΩ	1	+25°C	-300	300	nA
			2, 3	+125°C, -55°C	-550	550	nA
Input Offset Current	IIO	VCM = 0V, +RS = 10kΩ, -RS = 10kΩ	1	+25°C	-300	300	nA
			2, 3	+125°C, -55°C	-400	400	nA
Common Mode Range	+CMR	V+ = 3V, V- = -27V	1	+25°C	12	-	V
			2, 3	+125°C, -55°C	12	-	V
	-CMR	V+ = 27V, V- = -3V	1	+25°C	-	-12	V
			2, 3	+125°C, -55°C	-	-12	V
Large Signal Voltage Gain	+AVOL	VOUT = 0V and +10V, RL = 2kΩ	1	+25°C	75	-	kV/V
			2	+125°C	100	-	kV/V
			3	-55°C	50	-	kV/V
	-AVOL	VOUT = 0V and -10V, RL = 2kΩ	1	+25°C	75	-	kV/V
			2	+125°C	100	-	kV/V
			3	-55°C	50	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔVCM = +12V, +V = +3V, -V = -27V, VOUT = -12V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	-CMRR	ΔVCM = -12V, +V = +27V, -V = -3V, VOUT = +12V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ± 15V, RSOURCE = 100Ω, RLOAD = 100kΩ, VOUT = 0V, Unless Otherwise Specified

DC PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	+VOUT1	RL = 2kΩ	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	+VOUT2	RL = 10kΩ	1	+25°C	12	-	V
			2, 3	+125°C, -55°C	12	-	V
	-VOUT1	RL = 2kΩ	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
	-VOUT2	RL = 10kΩ	1	+25°C	-	-12	V
			2, 3	+125°C, -55°C	-	-12	V
Output Current	+IOUT	VOUT = -5V	1	+25°C	10	-	mA
			2, 3	+125°C, -55°C	10	-	mA
	-IOUT	VOUT = +5V	1	+25°C	-	-10	mA
			2, 3	+125°C, -55°C	-	-10	mA
Quiescent Power Supply Current	+ICC	VOUT = 0V, IOUT = 0mA	1	+25°C	-	6.0	mA
			2, 3	+125°C, -55°C	-	6.0	mA
	-ICC	VOUT = 0V, IOUT = 0mA	1	+25°C	-6.0	-	mA
			2, 3	+125°C, -55°C	-6.0	-	mA
Power Supply Rejection Ratio	+PSRR	ΔVSUP = 10V, +V = +10V, -V = -15V, +V = +20V, -V = -15V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	-PSRR	ΔVSUP = 10V, +V = +15V, -V = -10V, +V = +15V, -V = -20V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ± 15V, RSOURCE = 50Ω, RLOAD = 2kΩ, CLOAD = 50pF, AVCL = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	+SR	VOUT = -3V to +3V	4	+25°C	2	-	V/µs
	-SR	VOUT = +3V to -3V	4	+25°C	2	-	V/µs
Rise & Fall Time	TR	VOUT = 0 to +200mV 10% ≤ TR ≤ 90%	4	+25°C	-	150	ns
	TF	VOUT = 0 to -200mV 10% ≤ TR ≤ 90%	4	+25°C	-	150	ns
Overshoot	+OS	VOUT = 0 to +200mV	4	+25°C	-	45	%
	-OS	VOUT = 0 to -200mV	4	+25°C	-	45	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ± 15V, RLOAD = 2kΩ, CLOAD = 50pF, AVCL = +1V/V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Differential Input Resistance	RIN	VCM = 0V	1	+25°C	250	-	kΩ
Input Noise Voltage Density	En	RS = 20Ω, fo = 1000Hz	1	+25°C	-	4	nV/√Hz
Input Noise Current Density	In	RS = 20MΩ, fo = 1000Hz	1	+25°C	-	1	pA/√Hz
Full Power Bandwidth	FPBW	VPEAK = 10V	1, 2	+25°C	15	-	kHz
Minimum Closed Loop Stable Gain	CLSG	RL = 2kΩ, CL = 50pF	1	-55°C to +125°C	+1	-	V/V
Output Resistance	ROUT	Open Loop	1	+25°C	-	200	Ω
Quiescent Power Consumption	PC	VOUT = 0V, IOUT = 0mA	1, 3	-55°C to +125°C	-	180	mW
Channel Separation	CS	RS = 1kΩ, AVCL = 100V/V, VIN = 100mVRMS at 10kHz, Referred to Input	1	+25°C	90	-	dB
Settling Time	TS	AVCL = -1	1, 4	+25°C	-	5	µs

NOTES:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/(2πVPEAK)
3. Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)
4. Settling time measured from the 90% point of a 10V input pulse to within 10mV of the settled value.
5. Caution: Continuous long-duration short-circuit operation may degrade the operating life of the device.

TABLE 4. POST RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V

DC PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Open Loop Voltage Gain	AVOL	RL = 2kΩ	+25°C	40	-	kV/V
Input Offset Voltage	VIO	VCM = 0V	+25°C	-	5.0	mV
Input Offset Current	IIO	RS = 10kΩ, VCM = 0V	+25°C	-	1.0	µA
Input Bias Current	IBIAS	VCM = 0V	+25°C	-	1.0	µA

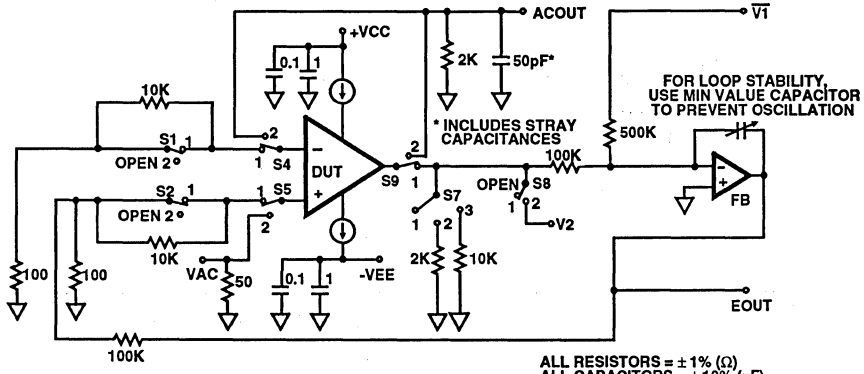
TABLE 5. HS-5104RH BURN-IN DELTA PARAMETERS (+25°C)
GROUP B, SUBGROUP 5

PARAMETERS	DELTA LIMITS
VIO	± 2.0mV
IBIAS	± 75nA
IIO	±75nA

TABLE 6. APPLICABLE SUBGROUPS

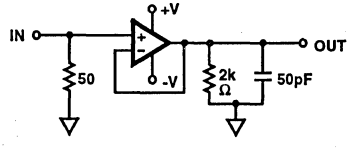
CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS
Initial Test		100%/5004	1, 4
Interim Test		100%/5004	1
PDA		100%/5004	1
Final Test		100%/5004	1, 2, 3, 4, 5, 6
Group A		Samples/5005	1, 2, 3, 4, 5, 6
Group B	B5	Samples/5005	1, 2, 3
	Others	Samples/5005	1
Group D		Samples/5005	1
Group E, Subgroup 2		Samples/5005	1

Test Circuits (Applies to Table 1 and Table 2)

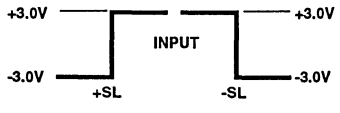


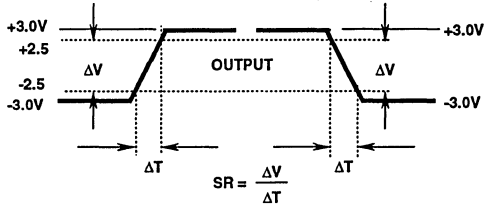
Test Circuits and Waveforms

SIMPLIFIED TEST CIRCUIT (Applies to Table 2 and Table 3)



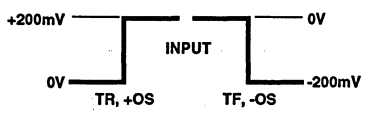
SLEW RATE WAVEFORMS

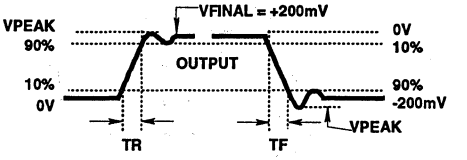




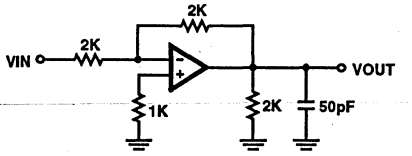
Test Circuits and Waveforms (Continued)

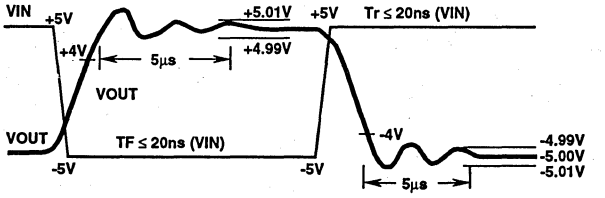
OVERSHOOT, RISE/FALL TIME WAVEFORMS



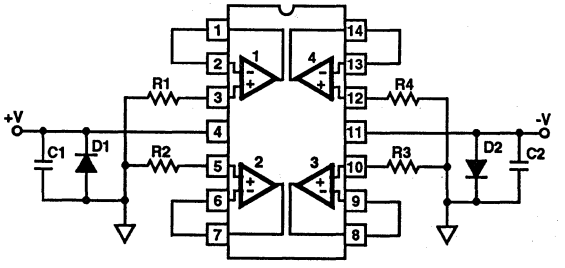


SETTLING TIME TEST CIRCUIT AND WAVEFORM



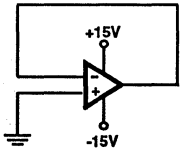


Burn-In Circuit



NOTES:
R1 = R2 = R3 = R4 = 1MΩ, 5%, 1/4W (Min.)
C1 = C2 = 0.01µF/Socket (Min) or 0.1µF/Row (Min)
D1 = D2 = IN4002 or Equivalent/Board
I(V+) - (V-)I = 31V ± 1V

Irradiation Circuit

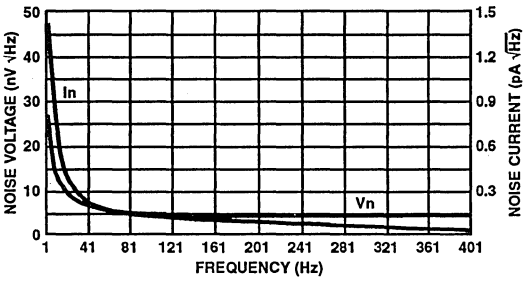


(ONE OF FOUR)

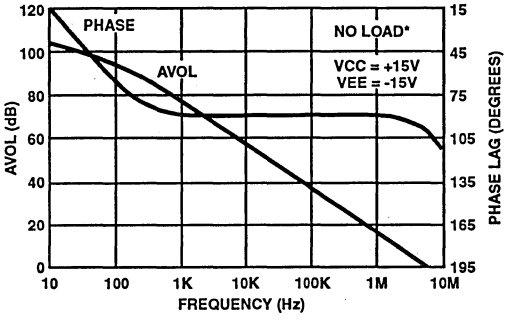
NOTES:
+V = 15V
-V = -15V
Group E Sample Size = 4 Die Per Wafer

Typical Performance Curves

TYPICAL NOISE VOLTAGE AND CURRENT vs FREQUENCY

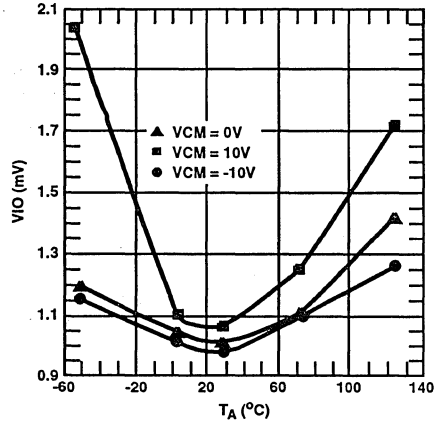


OPEN LOOP GAIN AND PHASE vs FREQUENCY

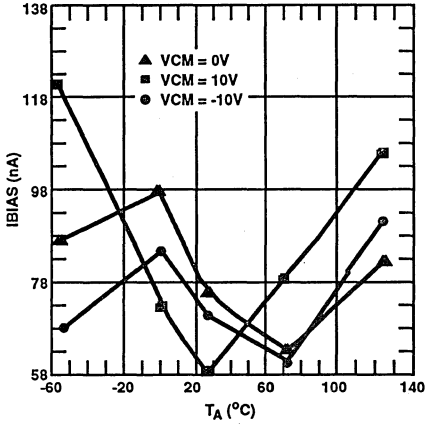


*DERATE 4dB FOR RL = 2K

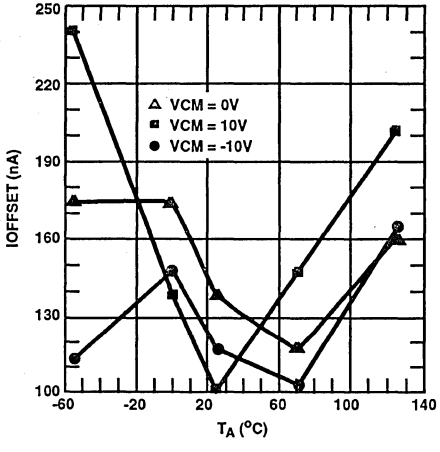
INPUT OFFSET VOLTAGE vs COMMON VOLTAGE AND TEMPERATURE



BIAS CURRENT vs COMMON MODE VOLTAGE AND TEMPERATURE

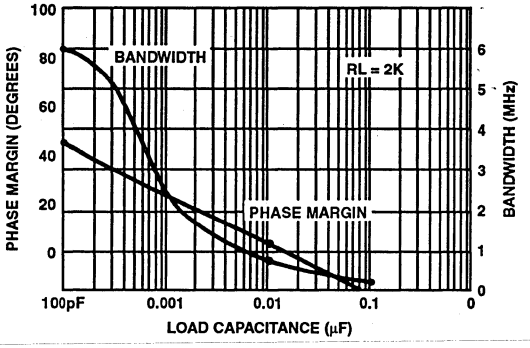


OFFSET CURRENT vs COMMON MODE VOLTAGE AND TEMPERATURE

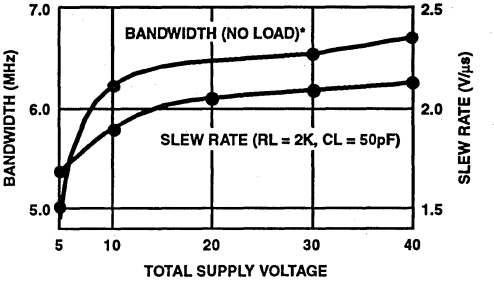


Typical Performance Curves (Continued)

BANDWIDTH AND PHASE MARGIN vs LOAD CAPACITANCE

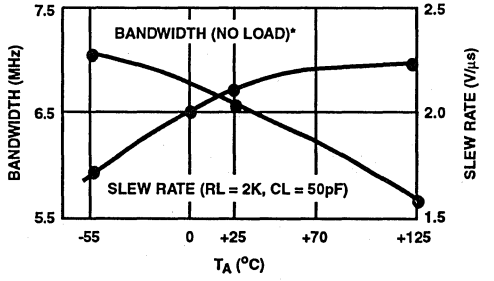


SLEW RATE AND BANDWIDTH vs SUPPLY VOLTAGE



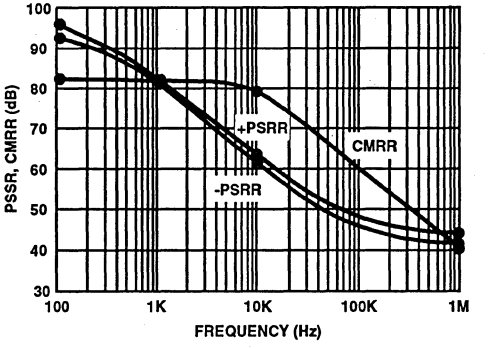
*DERATE 0.5MHz for RL = 2K

SLEW RATE AND BANDWIDTH vs TEMPERATURE

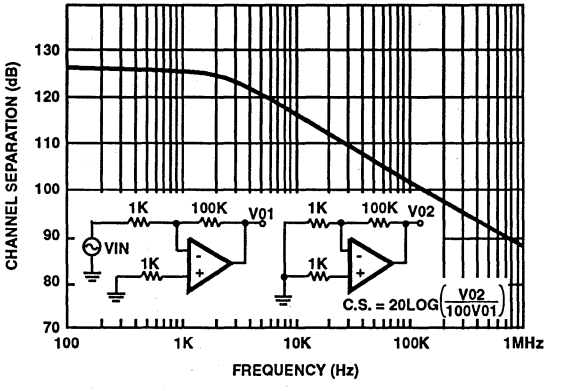


*DERATE 0.5MHz for RL = 2K

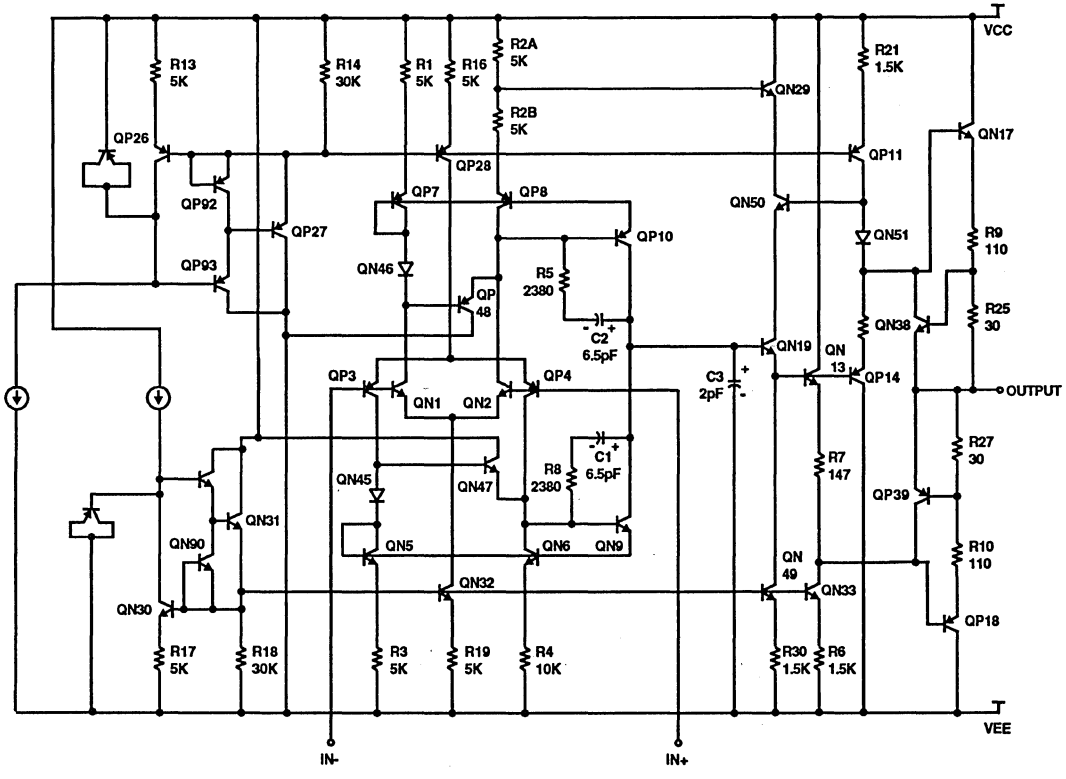
COMMON MODE REJECTION RATIO AND POWER SUPPLY REJECTION RATIO vs FREQUENCY



CHANNEL SEPARATION vs FREQUENCY



Schematic



(ONE OF FOUR)

Harris - Space Level Product Flow

SEM - Traceable to Diffusion Method 2018

Wafer Lot Acceptance Method 5007

Internal Visual Inspection (Note 1)

Gamma Radiation Assurance Tests Method 1019

100% Nondestructive Bond Pull Method 2023

Customer Pre-Cap Visual Inspection (Notes 1, 2)

Temperature Cycling Method 1010 Condition C

Constant Acceleration method 2001 Y1 30KG

Particle Impact Noise Detection method 2020, Condition A 20G

Marking and Serialization

X-Ray Inspection Method 2012

Initial Electrical Tests (T0)

Static Burn-In 240 Hours, +125°C Method 1015 Condition A

Electrical Tests Subgroups 1, 7, 9 (T1)

Burn-In Delta Calculation (T0 - T1)

PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ

Electrical Test +125°C, -55°C

Alternate Group A Inspection Method 5005

Fine and Gross Leak Tests Method 1014

Customer Source Inspection (Note 2)

Group B Inspection (Notes 2, 4) Method 5005

Group D Inspection (Notes 2, 4) Method 5005

External Visual Inspection Method 2009

Data Package Generation (Note 3)

NOTES:

1. Visual Inspection is performed to MIL-STD-883 Method 2010, Condition A.
2. These steps are optional, and should be listed on the purchase order if required.
3. Data package contains: Assembly Attributes (post seal)
   Test Attributes (includes Group A) -55°C, +25°C, +125°C
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (includes SEM report)
   X-Ray Report and Film
   Test Variables Data, DC Test and TELQV
   +25°C Initial Test
   +25°C Interim Test 1
   +25°C Delta Over Burn-In
4. Group B data package contains Attributes Data pulse Variables Data, DC Test and TE2HQV. Group D data package contains Attributes only.

Metallization Topology

DIE DIMENSIONS:
124 x 108 x 11 mils
(3160 x 2740 x 280µm)

METALLIZATION:
Type: Aluminum
Thickness: 12.5kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
1.45×10^5 A/cm^2 at 10mA

SUBSTRATE POTENTIAL (Powered Up):
V-

GLASSIVATION:
Type: Silox
Thickness: 8kÅ ± 1kÅ

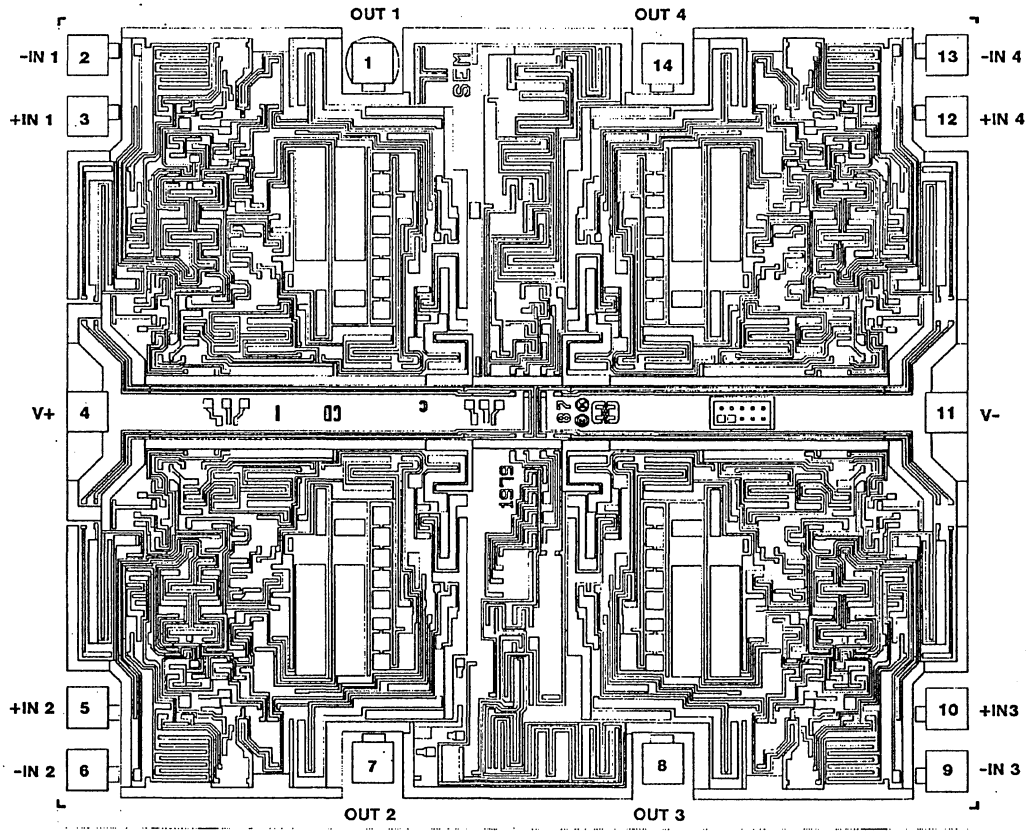
TRANSISTOR COUNT:
175

PROCESS:
High Frequency Linear

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature:Ceramic DIP - 460°C (Max)

Metallization Mask Layout

HS-5104RH



RAD HARD 5

DATA CONVERTERS

HARRIS SEMICONDUCTOR

HS-565ARH

PRELIMINARY

December 1992

High Speed, Monolithic Digital-to-Analog Converter

Features

- DAC and Reference on a Single Chip
- Pin Compatible with AD-565A and HI-565A
- Very High Speed: Settles to 1/2LSB in 500ns Max
- Monotonicity Guaranteed Over Temperature
- 1/2LSB Max Nonlinearity Guaranteed Over Temperature
- Low Gain Drift (Max., DAC Plus Reference) 25ppm/°C
- Total Dose Hardness to 50KRAD

Applications

- High Speed A/D Converters
- Precision Instrumentation
- Signal Reconstruction

Description

The HS-565ARH is a fast, 12 bit current output, digital-to-analog converter. The monolithic chip includes a precision voltage reference, thin-film R-2R ladder, reference control amplifier and twelve high-speed bipolar current switches.

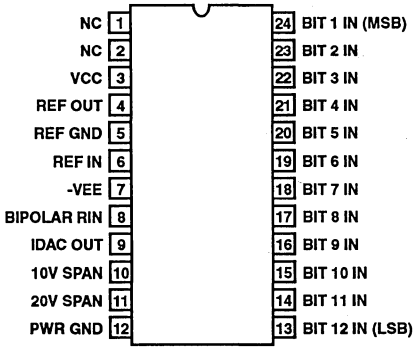
The Harris Semiconductor Dielectric Isolation process provides latch-up free operation while minimizing stray capacitance and leakage currents, to produce an excellent combination of speed and accuracy. Also, ground currents are minimized to produce a low and constant current through the ground terminal, which reduces error due to code-dependent ground currents.

HS-565ARH dice are laser trimmed for a maximum integral nonlinearity error of ±1/4LSB at +25°C. In addition, the low noise buried zener reference is trimmed both for absolute value and minimum temperature coefficient.

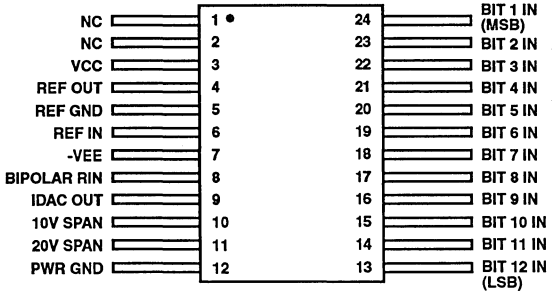
The HS-565ARH is packaged in ceramic 24 pin DIP and Flatpack packages.

Pinouts

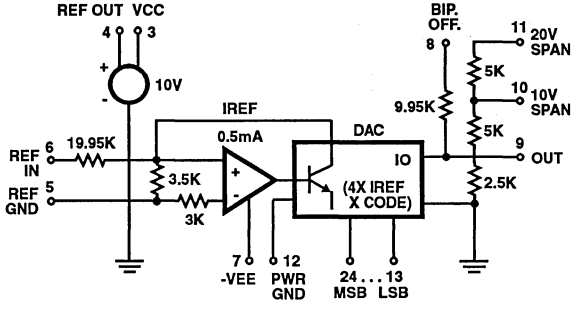
HS1-565ARH (24 PIN DIP)
TOP VIEW



HA1-565A/883 (FLATPACK)
TOP VIEW



Functional Diagram



5 DATA CONVERTERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3278

Absolute Maximum Ratings

VCC to Power Ground ..... 0V to +18V
VEE to Power Ground ..... 0V to -18V
Voltage on DAC Output (Pin 9) ..... -3V to +12V
Digital Input (Pins 13 - 24) to Power Ground ..... -1V to +7V
Ref In to Reference Ground ..... ±12V
Bipolar Offset to Reference Ground ..... ±12V
10V Span R to Reference Ground ..... ±12V
20V Span R to Reference Ground ..... ±24V
Junction Temperature (TJ) ..... +175°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +265°C

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	TBD	TBD
Flatpack Package	TBD	TBD

Package Power Dissipation for T_A = -55°C to +125°C
Ceramic DIP Package ..... TBD
Flatpack Package ..... TBD

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range (VCC) ..... +11.4V to +16.5V
Operating Voltage Range (VEE) ..... -11.4V to +16.5V
Operating Temperature Range ..... -55°C to +125°C
Digital Input Low Voltage ..... 0V to +0.8V
Digital Input High Voltage ..... +2.2V to +5.5V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

All Typical Values Represent +25°C, Nominal Conditions and have been characterized but are not tested.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Resolution		VSSD = VSSA = 0V, VCC = +15V, VEE = -15V	1, 2, 3	-55°C to +125°C	-	-	12	Bits
Accuracy		VSSD = VSSA = 0V, VCC = +15V, VEE = -15V, Error Relative to Full Scale	1, 2, 3	-55°C to +125°C	-	±1/8	±1/2	LSB
Digital Input High Current	IIH	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V	1, 2, 3	-55°C to +125°C	-	0.01	+1.0	µA
Digital Input Low Current	IIL	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V	1, 2, 3	-55°C to +125°C	-	-2.0	-20	µA
Differential Nonlinearity	DNLE	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V, +25°C (Monotonicity Guaranteed)	1, 2, 3	-55°C to +125°C	-	±1/4	±1/2	LSB
Power Supply Currents								
VCC	ICC	VSSD = VSSA = 0V, VCC = +16.5V, VEE = -15V	1, 2, 3	-55°C to +125°C	-	9.0	11.8	mA
VEE	IEE	VSSD = VSSA = 0V, VCC = +15V, VEE = -16.5V	1, 2, 3	-55°C to +125°C	-	9.5	14.5	mA
Reference Input Impedance	RREF	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V	1, 2, 3	-55°C to +125°C	15K	20K	25K	Ω
Reference Output Voltage	Ref Out	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V	1, 2, 3	-55°C to +125°C	9.9	10	10.1	V
Reference Output Current	IREF	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V, Available for external loads	1, 2, 3	-55°C to +125°C	1.5	2.5	-	mA
Output Current								
Unipolar		VSSD = VSSA = 0V, VCC = +15V, VEE = -15V, All Bits On	1, 2, 3	-55°C to +125°C	-1.6	-2.0	-2.4	mA
Bipolar		VSSD = VSSA = 0V, VCC = +15V, VEE = -15V, All Bits On or Off	1, 2, 3	-55°C to +125°C	±0.8	±1.0	±1.2	mA
Output Resistance	ROUT	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V, Exclusive of Span Resistors	1, 2, 3	-55°C to +125°C	1.8K	2.5K	3.2K	Ω

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

All Typical Values Represent +25°C, Nominal Conditions and have been characterized but are not tested. **(Continued)**

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Output Offset								
Unipolar		VSSD = VSSA = 0V, VCC = +15V, VEE = -15V	1, 2, 3	-55°C to +125°C	-	0.01	0.05	% of F.S.
Bipolar		VSSD = VSSA = 0V, VCC = +15V, VEE = -15V, Figure 2, R3 = 50Ω Fixed	1, 2, 3	-55°C to +125°C	-	0.05	0.1	% of F.S.
Power Supply Gain Sensitivity								
VCC		Note 1	1, 2, 3	-55°C to +125°C	-	3	10	ppm of F.S.
VEE		Note 1	1, 2, 3	-55°C to +125°C	-	15	25	ppm of F.S.

NOTE:

1. The Power Supply Gain Sensitivity is tested in reference to a VCC = +15V and VEE = -15V

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

All Typical Values Represent +25°C, Nominal Conditions and have been characterized but are not tested.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Settling Time (Note 1)		VSSD = VSSA = 0V, VCC = +15V, VEE = -15V, High Z External Load	9, 10, 11	-55°C to +125°C	-	350	500	ns
		VSSD = VSSA = 0V, VCC = +15V, VEE = -15V, 75Ω External Load	9, 10, 11	-55°C to +125°C	-	150	250	ns
Full Scale Transition								
Rise Time	TRISE	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V	9, 10, 11	-55°C to +125°C	-	15	30	ns
Fall Time	TFALL	VSSD = VSSA = 0V, VCC = +15V, VEE = -15V	9, 10, 11	-55°C to +125°C	-	30	60	ns

NOTE:

1. Reference the Settling Time discussion and Figure 3.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

All Typical Values Represent +25°C, Nominal Conditions and have been characterized but are not tested.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Output Capacitance	COUT	f = 1MHz	1, 2	+25°C	-	20	-	pF
			1, 3	+25°C	-	TBD	-	pF
Output Compliance Voltage			1	-55°C to +125°C	-1.5	-	10	V
Temperature Coefficients								
Unipolar Zero		With Internal Reference	1	-55°C to +125°C	-	1	2	ppm/°C
Bipolar Zero		With Internal Reference	1	-55°C to +125°C	-	5	10	ppm/°C
Gain (Full Scale)		With Internal Reference	1	-55°C to +125°C	-	10	25	ppm/°C
Differential Nonlinearity			1	-55°C to +125°C	-	2	-	ppm/°C

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

All Typical Values Represent +25°C, Nominal Conditions and have been characterized but are not tested. **(Continued)**

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Programmable Output Ranges			1	-55°C to +125°C	0	-	5	V
				-55°C to +125°C	-2.5	-	2.5	V
				-55°C to +125°C	0	-	10	V
				-55°C to +125°C	-5	-	5	V
				-55°C to +125°C	-10	-	10	V
External Adjustments			1					
Gain Error		Fixed 50Ω Resistor for R2 Figures 1, 2	1	-55°C to +125°C	-	±0.10	±0.25	% of F.S.
Bipolar Zero Error		Fixed 50Ω Resistor for R3 Figures 1, 2	1	-55°C to +125°C	-	±0.05	±0.10	% of F.S.
Gain Adjustment Range		Figures 1, 2	1	-55°C to +125°C	±0.25	-	-	% of F.S.
Bipolar Zero Adjustment Range		Figures 1, 2	1	-55°C to +125°C	±0.15	-	-	% of F.S.

NOTES:

1. The parameters listed in Table 3 are controlled via design or process and are not tested. These parameters are characterized upon initial design release.
2. 24 Pin DIP package only.
3. 24 Pin Flatpack package only.

TABLE 4. POST 50KRAD ELECTRICAL PERFORMANCE CHARACTERISTICS

Post 50KRAD Electrical Performance is per Tables 1, 2, and 3

TABLE 5. BURN-IN DELTA PARAMETERS (T_A = +25°C)

TBD

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	Q SUBGROUPS
Initial Test		100%/5004	1, 7, 9
PDA		100%/5004	1, 7, Δ
Final Test		100%/5004	1, 7, 9
Group A		Samples/5005	1, 2, 3, 7, 8, 9, 10, 11
Group B	B5	Samples/5005	1, 2, 3, 7, 8, 9, 10, 11
	Others	Samples/5005	1, 7
Group D		Samples/5005	1, 7
Group E, Subgroup 2		Samples/5005	1, 7, 9

Definitions of Specifications

Digital Inputs

The HS-565ARH accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight binary, Two's Complement*, or Offset Binary. (See Operating Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
MSB . LSB	STRAIGHT BINARY	OFFSET BINARY	TWO'S COMPLEMENT*
000 . . .000	Zero	-FS (Full Scale)	Zero
100 . . .000	$^1/_2$FS	Zero	-FS
111 . . .111	+FS - 1LSB	+FS - 1LSB	Zero - 1LSB
011 . . .111	$^1/_2$FS - 1LSB	Zero - 1LSB	+FS - 1LSB

* Invert MSB with external inverter to obtain Two's Complement Coding

Accuracy

Nonlinearity - Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full scale (all bits ON).

Differential Nonlinearity - For a D/A converter, it is the difference between the actual output voltage change and the ideal (1LSB) voltage change for a one bit change in code. A Differential Nonlinearity of ±1LSB or less guarantees monotonicity; i.e., the output always increases and never decreases for an increasing input.

Settling Time

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition, settling to within $^1/_2$LSB of final value.

Drift

Gain Drift - The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (TH) and low (TL) temperatures. Gain drift is calculated for both high (TH - 25°C) and low ranges (+25°C - TL) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

Offset Drift - The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (TH) and low (TL) temperatures. Offset drift is calculated for both high (TH - 25°C) and low +25°C - TL) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst case drift.

Power Supply Sensitivity

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

Compliance

Compliance Voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance Limit implies functional operation only and makes no claims to accuracy.

Glitch

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half scale or the major carry code transition from 011 . . . 1 to 100 . . . 0 or vice versa. For example, if turn ON is greater than turn OFF for 011 . . . 1 to 100 . . . 0, an intermediate state of 000 . . . 0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

Applying the HS-565ARH

OP AMP Selection

The HS-565ARH's current output may be converted to voltage using the standard connections shown in Figures 1 and 2. The choice of operational amplifier should be reviewed for each application, since a significant trade-off may be made between speed and accuracy. Remember settling time for the DAC-amplifier combination is

$$\sqrt{(t_D)^2 + (t_A)^2}$$

where t_D, t_A are settling times for the DAC and amplifier.

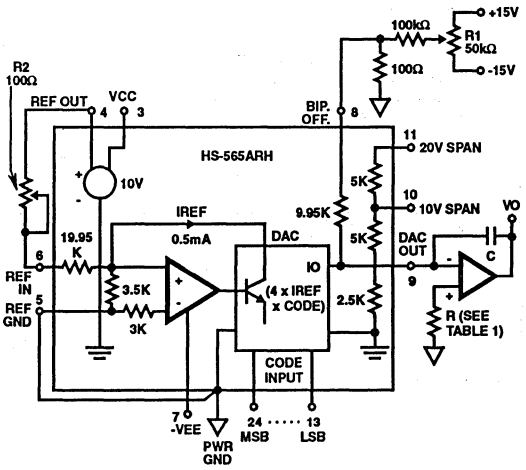


FIGURE 1. UNIPOLAR VOLTAGE OUTPUT

No Trim Operation

The HS-565ARH will perform as specified without calibration adjustments. To operate without calibration, substitute 50Ω resistors for the 100Ω trimming potentiometers: In Figure 1 replace R2 with 50Ω; also remove the network on pin 8 and connect 50Ω to ground. For bipolar operation in Figure 2, replace R3 and R4 with 50Ω resistors.

With these changes, performance is guaranteed as shown under Specifications, "External Adjustments". Typical unipolar zero will be $\pm^1/_2$LSB plus the op amp offset.

The feedback capacitor C must be selected to minimize settling time.

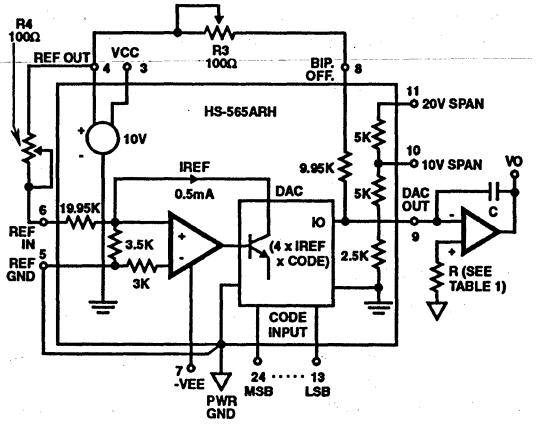


FIGURE 2. BIPOLAR VOLTAGE OUTPUT

Calibration

Calibration provides the maximum accuracy from a converter by adjusting its gain and offset errors to zero, For the HS-565ARH, these adjustments are similar whether the current output is used, or whether an external op amp is added to convert this current to a voltage. Refer to Table 1 for the voltage output case, along with Figure 1 or 2.

Calibration is a two step process for each of the five output ranges shown in Table 1. First adjust the negative full scale (zero for unipolar ranges). This is an offset adjust which translates the output characteristic, i.e. affects each code by the same amount.

Next adjust positive FS. This is a gain error adjustment, which rotates the output characteristic about the negative FS value.

For the bipolar ranges, this approach leaves an error at the zero code, whose maximum values is the same as for integral nonlinearity error. In general, only two values of output may be calibrated exactly; all others must tolerate some error. Choosing the extreme end points (plus and minus full scale) minimizes this distributed error for all other codes.

Settling Time

This is a challenging measurement, in which the result depends on the method chosen, the precision and quality of test equipment and the operating configuration of the DAC (test conditions). As a result, the different techniques in use by converter manufacturers can lead to consistently different results. An engineer should understand the advantage and limitations of a given test methods before using the specified settling time as a basis for design.

TABLE 1. OPERATING MODES AND CALIBRATION

MODE	CIRCUIT CONNECTIONS				CALIBRATION		
	OUTPUT RANGE	PIN 10 TO	PIN 11 TO	RESISTOR (R)	APPLY INPUT CODE	ADJUST	TO SET VO
Unipolar (See Figure 1)	0 to +10V	VO	Pin 10	1.43K	All 0's All 1's	R1 R2	0V +9.99756V
	0 to +5V	VO	Pin 9	1.1K	All 0's All 1's	R1 R2	0V +4.99878V
Bipolar (See Figure 2)	±10V	NC	VO	1.69K	All 0's All 1's	R3 R4	-10V +9.99512V
	±5V	VO	Pin 10	1.43K	All 0's All 1's	R3 R4	-5V +4.99756V
	±2.5V	VO	Pin 9	1.1K	All 0's All 1's	R3 R4	-2.5V +2.49878V

The approach used for several years at Harris calls for a strobed comparator to sense final perturbations of the DAC output waveform. This gives the LSB a reasonable magnitude (814mV for the HS-565ARH, which provides the comparator with enough overdrive to establish an accurate $\pm^1/_2$LSB window about the final settled value. Also, the required test conditions simulate the DAC's environment for a common application - use in a successive approximation A/D converter. Considerable experience has shown this to be a reliable and repeatable way to measure settling time.

The usual specification is based on a 10V step, produced by simultaneously switching all bits from off-to-on (tON) or on-to-off (tOFF). The slower of the two cases is specified, as measured from 50% of the digital input transition to the final entry within a window of $\pm^1/_2$LSB about the settled value. Four measurements characterize a given type of DAC:

(a) tON, to final value $+^1/_2$LSB

(b) tON, to final value $-^1/_2$LSB

(c) tOFF, to final value $+^1/_2$LSB

(d) OFF, to final value $-^1/_2$LSB

(Cases (b) and (c) may be eliminated unless the overshoot exceeds $^1/_2$LSB). For example, refer to Figure 3 for the measurement of case (d).

Procedure

As shown in Figure 3B, settling time equals tX plus the comparator delay (tD = 15ns). To measure tX,

- Adjust the delay on generator number 2 for a tX of several microseconds. This assures that the DAC output has settled to its final wave
- Switch on the LSB (+5V)
- Adjust the VLSB supply for 50% triggering at COMPARATOR OUT. This is indicated by traces of equal brightness on the oscilloscope display as shown in Figure 3B. Note DVM reading.
- Switch to LSB to Pulse (P)
- Readjust the VLSB supply for 50% triggering as before, and note DVM reading. One LSB equals one tenth the difference in the DVM readings noted above
- Adjust the VLSB supply to reduce the DVM reading by 5LSB's (DVM reads 10X, so this sets the comparator to sense the final settled value minus $^1/_2$LSB). Comparator output disappears
- Reduce generator number 2 delay until comparator output reappears, and adjust for "equal brightness"
- Measure tX from scope as shown in Figure 3B. Settling time equals tX + tD, i.e. tX + 15ns

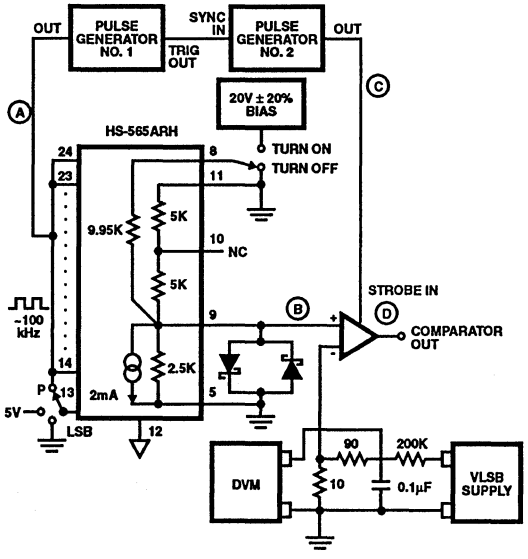


FIGURE 3A.

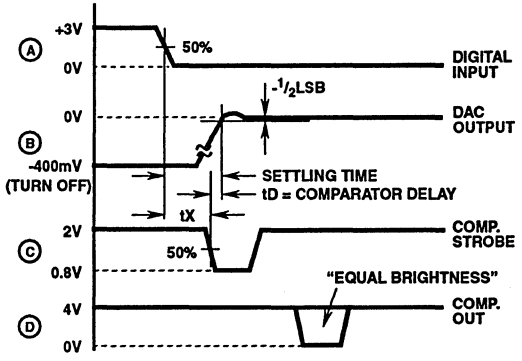


FIGURE 3B.

FIGURE 3.

Other Considerations

Grounds

The HS-565ARH has two ground terminals, pin 5 (REF GND) and pin 12 (PWR GND). These should not be tied together near the package unless that point is also the system signal ground to which all returns are connected. (If such a point exists, then separate paths are required to pins 5 and 12).

The current through pin 5 is near zero DC*; but pin 12 carries up to 1.75mA of code - dependent current from bits 1, 2, and 3. The general rule is to connect pin 5 directly to the system "quiet" point, usually called signal or analog ground. Connect pin 12 to the local digital or power ground. Then, of course, a single path must connect the analog/signal and digital/power grounds.

Layout

Connections to pin 9 (IOUT) on the HS-565ARH are most critical for high speed performance. Output capacitance of the DAC is only 20pF, so a small change of additional capacitance may alter the op amp's stability and affect settling time. Connections to pin 9 should be short and few. Component leads should be short on the side connecting to pin 9 (as for feedback capacitor C). See the Settling Time section.

Bypass Capacitors

Power supply bypass capacitors on the op amp will serve the HS-565ARH also. If no op amp is used, a 0.01µF ceramic capacitor from each supply terminal to pin 12 is sufficient, since supply current variations are small.

* Current cancellation is a two step process within the HS-565ARH in which code dependent variations are eliminated, the resulting DC current is supplied internally. First an auxiliary 9 bit R-2R ladder is driven by the complement of the DAC's input code. Together, the main and auxiliary ladders draw a continuous 2.25mA from the internal ground node, regardless of input code. Part of the DC current is supplied by the zener voltage reference, and the remainder is sourced from the positive supply via a current mirror which is laser trimmed for zero current through the external terminal (pin 5).

Die Characteristics

Transistor Count 200

Die Size ..... 179 x 107 mils

Tie Substrate to ..... Reference Ground

Process ..... Bipolar - DI

Thermal Constants

θ_{ja} ..... +51°C

θ_{jc} ..... +16°C

HARRIS SEMICONDUCTOR

HS-9008RH

PRELIMINARY

December 1992

CMOS 8 Bit Flash Analog-to-Digital Converter

Features

- Excellent Noise Rejection - Fully Differential Design
- Superior Linearity (0.5LSB Typical)
- Single Reference Supply
- Low Power (400mW Typical)
- 20MHz Sampling Rate (50ns Conversion Time)
- Total Dose Hardness to 300KRAD

Description

The Harris HS-9008RH is a CMOS 8 Bit Flash Converter designed for space applications were relatively low power, exceptional accuracy and very fast conversion speeds are a necessity.

The HS-9008RH design differs substantially from most other available Flash Converters as it employs fully differential analog input sampling networks and amplifiers, as well as regenerative, offset nulled (error correcting) comparators. These circuit techniques improve noise performance and render the circuit much less sensitive to process and radiation induced device parametric shifts. Outstanding integral and differential linearity error is achieved through the use of a metal film resistor network which exhibits >10 bit linearity without trim. As a result of these innovations, the device operates with a single fixed reference supply as opposed to the multiple, adjustable references used in similar devices.

The HS-9008RH is fabricated in Harris' new AVLSI1RA process, which is dual level metal, twin well, thin EPI, 1.25µM junction isolated CMOS process. The capacitors are metal to metal with a nitride dielectric and have a negligible attenuation factor.

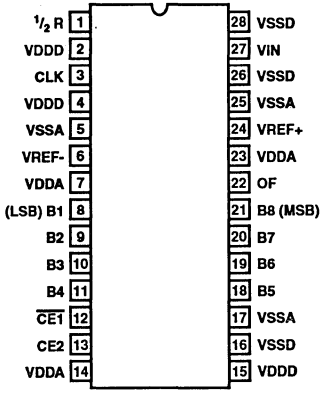
This combination of factors makes the HS-9008RH one of the best 8 Bit Flash Converters available in the Commercial, Military or Rad Hard markets.

Truth Table

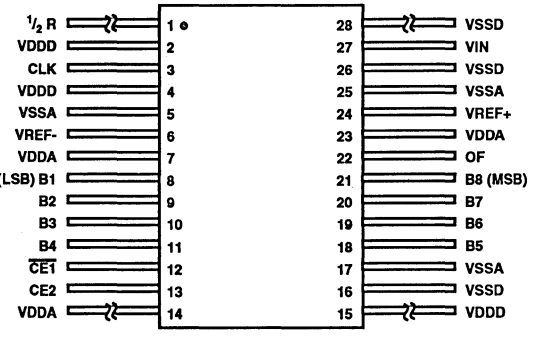
$\overline{CE1}$	CE2	B1 - B8	OF
0	1	Valid	Valid
1	1	Tri-State	Valid
X	0	Tri-State	Tri-State

Pinouts

28 PIN CERAMIC DIP CASE OUTLINE D1, CONFIGURATION 3
TOP VIEW



28 PIN FLATPACK CASE OUTLINE F11A, CONFIGURATION 2
TOP VIEW



5 DATA CONVERTERS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

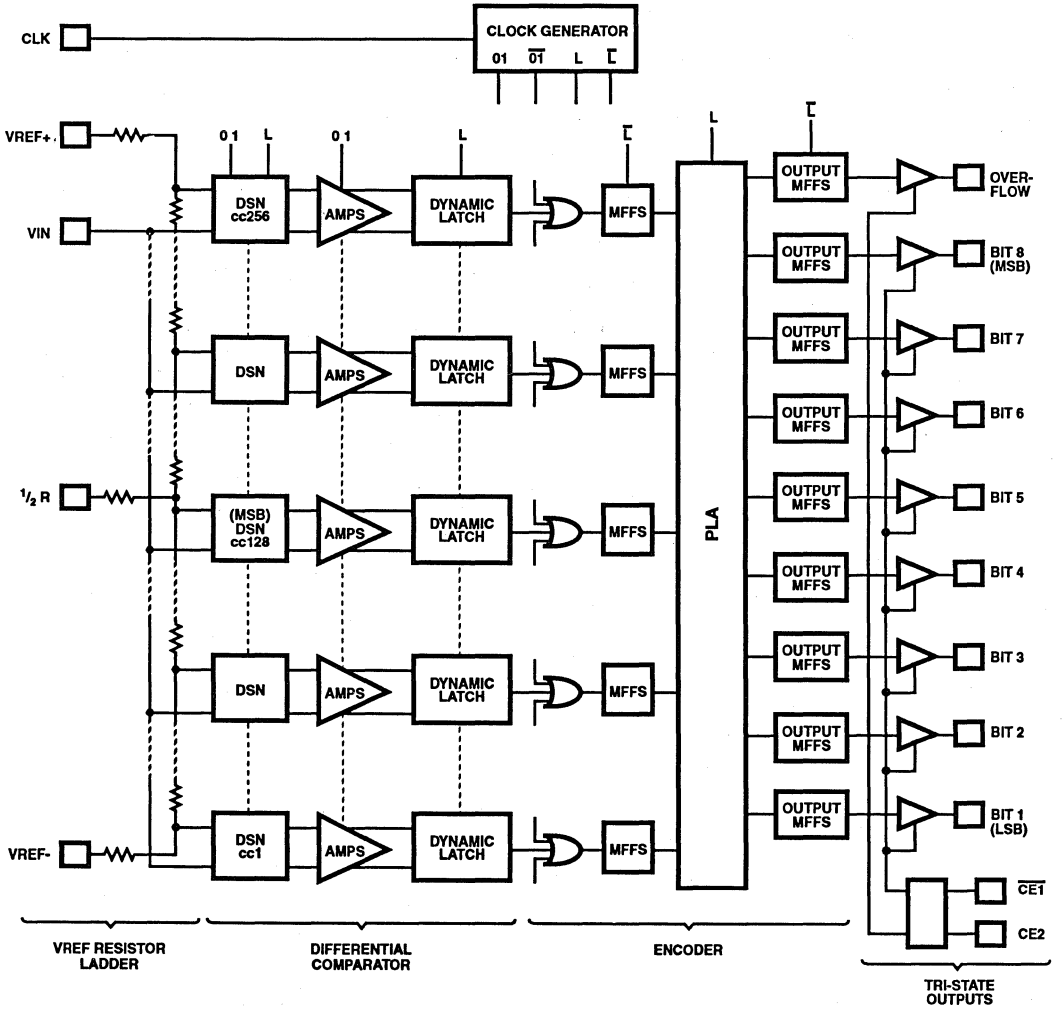
File Number 3279

Pin Description

PACKAGE PIN 28 DIP/FP	NAME	DESCRIPTION
8	B1	(LSB) Output Data Bits
9	B2	Output Data Bits
10	B3	Output Data Bits
11	B4	Output Data Bits
18	B5	Output Data Bits
19	B6	Output Data Bits
20	B7	Output Data Bits
21	B8	(MSB) Output Data Bits
22	OF	Overflow
16, 26, 28	VSSD	Digital Ground

PACKAGE PIN 28 DIP/FP	NAME	DESCRIPTION
2, 4, 15	VDDD	Digital Supply
13	CE2	Tri-State Output Enable
12	$\overline{CE1}$	Tri-State Output Enable
6	VREF-	Negative Reference Input
27	VIN	Analog Signal In
5, 17, 25	VSSA	Analog Ground
3	CLK	Clock Input
1	1/2 R	Reference Midpoint
24	VREF+	Positive Reference Input
7, 14, 23	VDDA	Analog Supply

Functional Diagram



Absolute Maximum Ratings

DC Supply Voltage Range, VDDD = VDDA
(Referenced to VSSD = VSSA = GND) .....-0.3V to +7.0V
Input Voltage Range: $\overline{CE1}$, CE2, CLK, VREF-,
VREF+, VIN, $^1/_2$ R .....VSS -0.3V to VDD +0.3V
Output Voltage Range: B1 - B8, OF
(Outputs Off).....VSS -0.3V to VDD +0.3V
DC Input Current $\overline{CE1}$, CE2, CLK, VIN, B1 - B8, OF.....10mA
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s)..... +265°C

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
28 Flatpack Package.....	TBD	TBD
28 Ceramic DIP Package	TBD	TBD
24 Flatpack Package.....	TBD	TBD

Package Power Dissipation
For T_A = -55°C to +125°C .....TBD

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range (VDDD = VDDA) ..... +4.5V to +5.5V
Operating Temperature Range..... -55°C to +125°C
Digital Input Low Voltage.....0V to +0.2VDDD
Input High Voltage..... 0.8VDDD to VDDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

All Typical Values Represent +25°C, Nominal Conditions and have been characterized but are not tested.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Resolution		VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	1, 2, 3	-55°C to +125°C	8	-	-	Bits
Integral Linearity Error	ILE	VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	1, 2, 3	-55°C to +125°C	-	±0.5	±1.0	LSB
Differential Linearity Error	DLE	VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	1, 2, 3	-55°C to +125°C	-	±0.25	±0.5	LSB
Offset Error	VOS	VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.), VIN = VREF- + 0.5LSB	1, 2, 3	-55°C to +125°C	-	-	±1.25	LSB
Gain Error	GE	VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.), VIN = VREF+ - 1.5LSB	1, 2, 3	-55°C to +125°C	-	-	±2.25	LSB
Ladder Impedance	Ref	VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	1, 2, 3	-55°C to +125°C	300	500	600	Ω
Full Scale Range (VIN and (VREF+) - (VREF-))		VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	1, 2, 3	-55°C to +125°C	-	4	5	V
Supply Current (IDDD + IDDA + IREF)								
Dynamic	IDDD	VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.), CLK = 25MHz (Note 1)	1, 2, 3	-55°C to +125°C	-	60	135	mA
Static	IDDS	VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.), CLK = High	1, 2, 3	-55°C to +125°C	-	40	80	mA

NOTE:

1. For typical value, CLK = 1MHz.

TABLE 2A. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

All Typical Values Represent +25°C, Nominal Conditions and have been characterized but are not tested.

PARAMETERS	SYMBOL	CONDITIONS		GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Conversion Speed		VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.), CLK = 50% Duty Cycle, Square Wave		9, 10, 11	-55°C to +125°C	20	-	-	MSPS
Full Power Bandwidth		VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.), VIN = Full Scale Sine Wave (Note 1)		9, 10, 11	-55°C to +125°C	-	10	-	MHz
Differential Gain Error		VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.), (Note 2)		9, 10, 11	-55°C to +125°C	-	-	2.5	%
Differential Phase Error		VDDD = VDDA = 5V, CLK = 10MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.), (Note 2)		9, 10, 11	-55°C to +125°C	-	-	2.5	Deg.
Total Harmonic Distortion	THD	VDDD = VDDA = 5V, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	CLK = 1MHz	9, 10, 11	-55°C to +125°C	-	-	-48	dB
			CLK = 10MHz	9, 10, 11	-55°C to +125°C	-	-	-48	dB
			CLK = 20MHz	9, 10, 11	-55°C to +125°C	-	-	-48	dB
Signal-to-Noise Ratio (Plus Distortion)	SNRD	VDDD = VDDA = 5V, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	CLK = 1MHz	9, 10, 11	-55°C to +125°C	47	-	-	dB
			CLK = 10MHz	9, 10, 11	-55°C to +125°C	47	-	-	dB
			CLK = 20MHz	9, 10, 11	-55°C to +125°C	42	-	-	dB

NOTE:

1. The -3dB bandwidth for frequency response purposes is greater than 30MHz.
2. VIN = 3.58MHz burst, CLK = 14MHz, 6 DC levels (2.0, 2.2, 2.4, 2.6, 2.8, 3.0V).

TABLE 2B. AC ELECTRICAL SWITCHING CHARACTERISTICS

All Typical Values Represent +25°C, Nominal Conditions and have been characterized but are not tested.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Track Time (Auto Balance Time)	TTRACK	VDDD = VDDA = 5V, CLK = 25MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.), CLK = High	9, 10, 11	-55°C to +125°C	20	-	-	ns
Hold Time	THOLD	VDDD = VDDA = 5V, CLK = 25MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.), CLK = Low	9, 10, 11	-55°C to +125°C	20	-	-	ns
Data Output Delay	TOD	VDDD = VDDA = 5V, CLK = 25MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	9, 10, 11	-55°C to +125°C	-	-	35	ns
Output Enable Time	TEN	VDDD = VDDA = 5V, CLK = 25MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	9, 10, 11	-55°C to +125°C	-	-	25	ns
Output Disable Time	TDIS	VDDD = VDDA = 5V, CLK = 25MHz, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	9, 10, 11	-55°C to +125°C	-	-	25	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

All Typical Values Represent +25°C, Nominal Conditions and have been characterized but are not tested.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Digital Input Capacitance	CI	f = 1MHz, VDDD = VDDA = OPEN, VSSD = VSSA = 0V, T_A = +25°C	1, 2	+25°C	-	-	15	pF
			1, 3	+25°C	-	-	15	pF
Output Capacitance	CO	f = 1MHz, VDDD = VDDA = OPEN, VSSD = VSSA = 0V, T_A = +25°C	1, 2	+25°C	-	-	10	pF
			1, 3	+25°C	-	-	10	pF
Analog Input Capacitance (Static)	CIN	CLK = High, VDDD = VDDA = 5V, VSSD = VSSA = 0V, VREF = 4.000V (Adj.),	1	-55°C to +125°C	-	70	-	pF
Analog Input Capacitance (Dynamic)	DYNCIN	CLK = 3MHz, VDDD = VDDA = 5V, VSSD = VSSA = 0V, VREF = 4.000V (Adj.),	1	-55°C to +125°C	-	30	-	pF
Aperture Delay		VDDD = VDDA = 5V, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	1	-55°C to +125°C	-	TBD	-	ns
Aperture Jitter		VDDD = VDDA = 5V, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	1	-55°C to +125°C	-	TBD	-	ps
Analog DC Input Current	IREF	VIN = 4.0V, VDDD = VDDA = 5V, VSSD = VSSA = 0V, VREF = 4.000V (Adj.),	1	-55°C to +125°C	-	2	-	mA
Power Supply Rejection	PSR	VDDD = VDDA = 5.5V, VSSD = VSSA = 0V, VREF = 4.000V (Adj.)	1	-55°C to +125°C	-	<1.0	-	$\frac{LSB}{V}$

NOTES:

1. The parameters listed in Table 3 are controlled via design or process and are not tested. These parameters are characterized upon initial design release.
2. 28 Pin DIP package only.
3. 28 Pin Flatpack package only.

TABLE 4. POST 300KRAD ELECTRICAL PERFORMANCE CHARACTERISTICS

Post 300KRAD Electrical Performance is per Tables 1, 2, and 3

TABLE 5. BURN-IN DELTA PARAMETERS (T_A = +25°C)

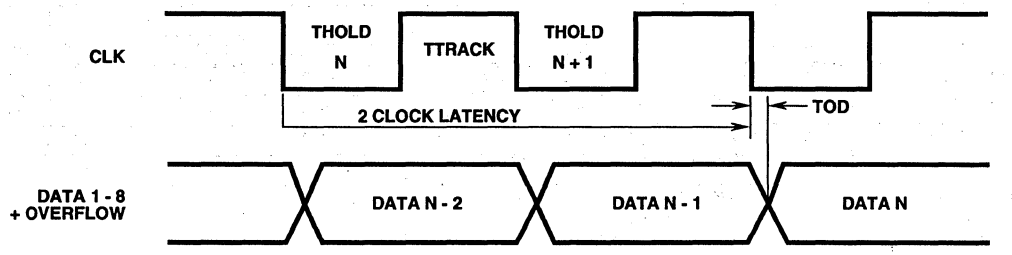
TBD

TABLE 6. APPLICABLE SUBGROUPS

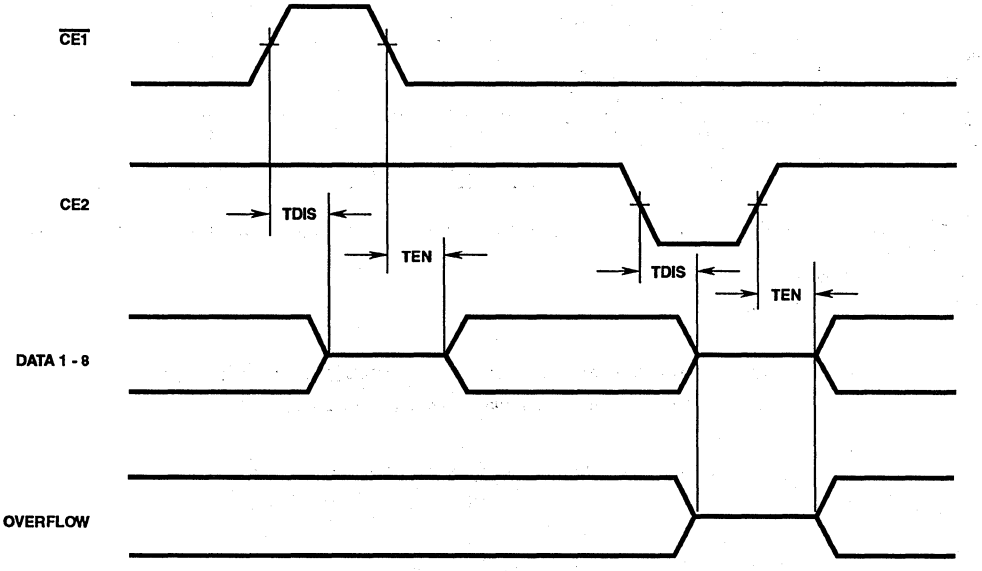
CONFORMANCE GROUPS		METHOD	Q SUBGROUPS
Initial Test		100%/5004	1, 7, 9
PDA		100%/5004	1, 7, Δ
Final Test		100%/5004	1, 7, 9
Group A		Samples/5005	1, 2, 3, 7, 8, 9, 10, 11
Group B	B5	Samples/5005	1, 2, 3, 7, 8, 9, 10, 11
	Others	Samples/5005	1, 7
Group D		Samples/5005	1, 7
Group E, Subgroup 2		Samples/5005	1, 7, 9

Timing Diagrams

INPUT TIMING

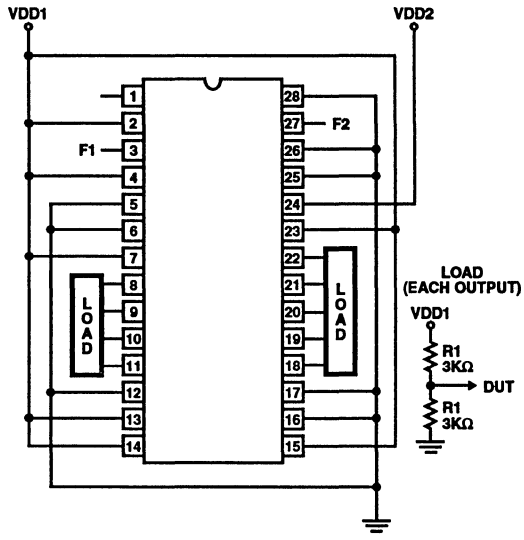


OUTPUT ENABLE TIMING



Burn-In Diagram

HS-9008RH 28 PIN DIP/FLATPACK

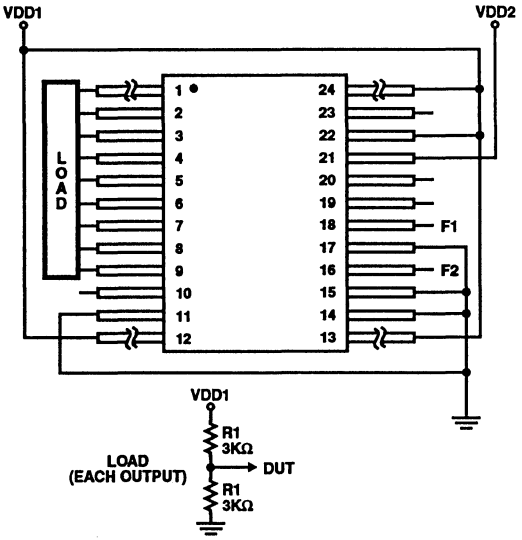


DYNAMIC

NOTES:

VDD1 = 5.5V Min
VDD2 = 4V Min
Input Signals: F1 = 1MHz (50% Duty Cycle); F2 = F1/4
VIH = 5V, +0.5V, -0; VIL = 0V, +0.5V, -0

HS-9008RH 24 PIN FLATPACK

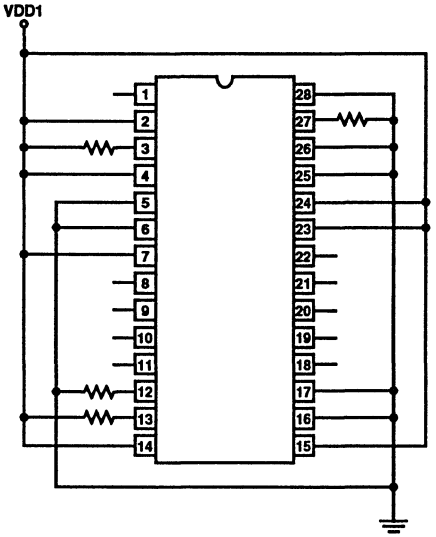


DYNAMIC

NOTES:

VDD1 = 5.5V Min
VDD2 = 4V Min
Input Signals: F1 = 1MHz (50% Duty Cycle); F2 = F1/4
VIH = 5V, +0.5V, -0; VIL = 0V, +0.5V, -0

Irradiation Circuit



NOTES:

All Total Dose Testing is performed using the HS1-9008RH package (28 DIP)
VDD1 = 5.5V Min
Resistors = 10KΩ ± 10%
Total Dose = 300KRADS

RAD HARD 6

FIELD PROGRAMMABLE GATE ARRAY

HARRIS SEMICONDUCTOR

HS-XC3020MS

ADVANCE INFORMATION

December 1992

Radiation Hardened Field Programmable Gate Array

Features

- 1.25 Micron Radiation Hardened SOS CMOS
  - Total Dose 300KRAD
  - Transient Upset 1 x 10^9 RAD (Si/s)
  - SEU Error Rate 1 x 10^{-12} E/B-Day
- XILINX XC3020 Compatible
- Pin-For-Pin Functionally Equivalent
- Uses XILINX Supported PC or Work-Station Based Development System
- Latch-up Free Under any Conditions
- Low Power CMOS Static Memory Technology
- Available in 100 Lead Ceramic Quad Flatpack
- Flexible Array Architecture

Description

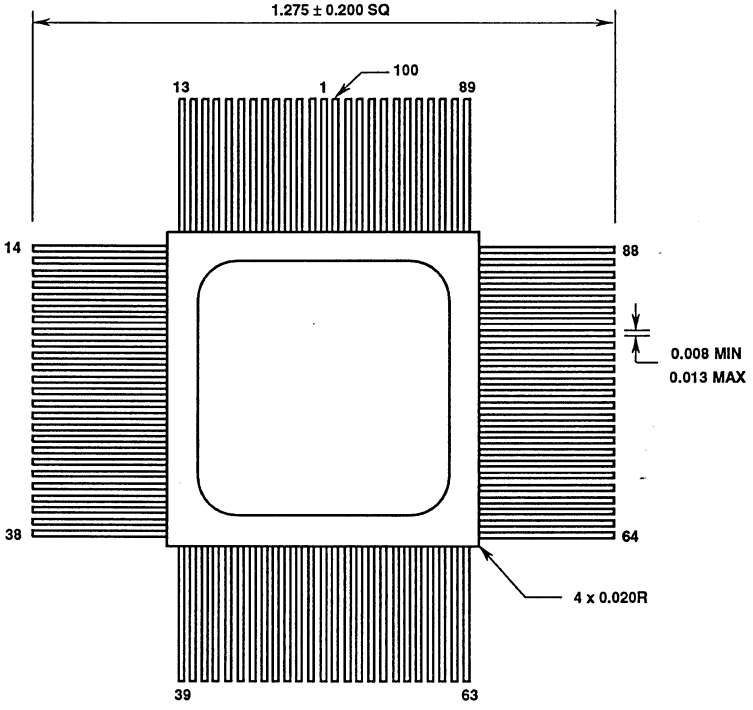
The HS-XC3020MS is a high density CMOS programmable gate array which is functionally compatible with the XILINX XC3020 Logic Cell™ Array. All XILINX development tools (XACT™) can be used to capture/edit, simulate, and place & route designs on the HS-XC3020MS. The HS-XC3020MS is fabricated on the Harris 1.25 micron Silicon-on-Sapphire CMOS process. This technology gives exceptional hardness to all types of radiation, including neutron fluence, total ionizing dose, and cosmic rays.

Architecture

The perimeter of configurable I/O blocks provides a programmable interface between the internal logic array and the device package pins. The array of configurable logic blocks performs user-specified logic functions. The interconnect resources are programmed to form networks that carry logic signals among blocks.

Pinout

100 PIN CERAMIC QUAD FLATPACK
BOTTOM VIEW



6 PROGRAMMABLE GATE ARRAYS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3200

Pin Description

PIN NO.	PIN NAME
1	GND
2	A13 (I/O)
3	A6 (I/O)
4	A12 (I/O)
5	A7 (I/O)
6	NC
7	NC
8	All (I/O)
9	A8 (I/O)
10	A10 (I/O)
11	A9 (I/O)
12	NC
13	NC
14	$\overline{\text{PWRDWN}}$
15	I/O (TCLKIN)
16	NC
17	NC
18	NC
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O

PIN NO.	PIN NAME
26	VCC
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	NC
36	NC
37	M1 ($\overline{\text{RDATA}}$)
38	NC
39	M0 (RT)
40	NC
41	M2 (I/O)
42	HDC (I/O)
43	I/O
44	$\overline{\text{LDC}}$ (I/O)
45	NC
46	NC
47	I/O
48	I/O
49	I/O
50	$\overline{\text{INIT}}$ (I/O)

PIN NO.	PIN NAME
51	GND
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	NC
60	NC
61	XTAL2 (I/O)
62	NC
63	$\overline{\text{RESET}}$
64	NC
65	DONE ($\overline{\text{PROG}}$)
66	D7 (I/O)
67	XTAL1 (I/O) (BCLKIN)
68	D6 (I/O)
69	NC
70	NC
71	I/O
72	D5 (I/O)
73	$\overline{\text{CS0}}$ (I/O)
74	D4 (I/O0
75	I/O

PIN NO.	PIN NAME
76	VCC
77	D3 (I/O)
78	$\overline{\text{CS1}}$ (I/O)
79	D2 (I/O)
80	I/O
81	NC
82	NC
83	D1 (I/O)
84	$\overline{\text{RCLK}}$-BUSY/RDY (I/O)
85	D0-DIN (I/O)
85	DOUT (I/O)
87	CCLK
88	NC
89	NC
90	A0 - $\overline{\text{WS}}$ (I/O)
91	A1 - CS2 (I/O)
92	NC
93	A2 (I/O)
94	A3 (I/O)
95	NC
96	NC
97	A15 (I/O)
98	A4 (I/O)
99	A14 (I/O)
100	A5 (I/O)

NOTE: 0.025 Pitch and 0.025 Spacing

Logic Capacity (Gates) 2000	User I/O's 64
Configurable Logic Blocks 64	Configuration Program Bits 14779

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input Voltage Range ..... -0.5V to VCC+0.5V
DC Input Current, any one input ..... ±10mA
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (Soldering 10s) ..... +260°C
Typical Derating Factor ..... TBD
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Flatpack Package	TBD	TBD

Maximum Package Power Dissipation
For T_A = -55°C to +100°C ..... TBD
For T_A = +100°C to +125°C ..... Derate Linearly at TBD
Gate Count ..... TBD

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Rise and Fall Time ..... TBD
Input Low Voltage (TTL) ..... 0V to +0.8V
Input Low Voltage (CMOS) ..... 0V to 0.3V
Input High Voltage (TTL) ..... VCC to VCC/2V
Input High Voltage (CMOS) ..... VCC to 0.7VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	NOTE 1 CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Operational Supply Current (CMOS Mode)	ICCO	VCC = 5.5V, VIN = VCC or GND (Note 2)	1	+25°C	-	-	mA
			2, 3	-55°C, +125°C	-	10	mA
Quiescent Operational Supply Current (TTL Mode)	ICCO	VCC = VIN = 5.5V, $\overline{\text{PWRDWN}}$ = 0V (Note 2)	1	+25°C	-	-	mA
			2, 3	-55°C, +125°C	-	24	mA
Power Down Supply Current	ICCPD	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	-	mA
			2, 3	-55°C, +125°C	-	5	mA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC - 0.8V, VIL = 0V (Note 3)	1	+25°C	-	-	mA
			2, 3	-55°C, +125°C	-4.0	-	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0V (Note 3)	1	+25°C	-	-	mA
			2, 3	-55°C, +125°C	4.0	-	mA
I/O Pin Leakage (Tri-Stated)	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	1	+25°C	-	-	µA
			2, 3	-55°C, +125°C	-	±10	µA
Horizontal Long Line Pull-Up Current	IRLL	VCC = 5.5V, VIN = VCC or GND, as an average	1	+25°C	-	-	mA
			2, 3	-55°C, +125°C	-	2.4	mA
$\overline{\text{PWRDWN}}$ Power Down Supply	VCCPD	Note 4	1	+25°C	-	-	V
			2, 3	-55°C, +125°C	-	3.5	V
Functional Noise Immunity (TTL Mode)	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V	7, 8A, 8B	-55°C, +25°C, +125°C	4.0	0.5	V
Functional Noise Immunity (CMOS Mode)	FN	VCC = 4.5V, VIH = 0.7 x VCC, VIL = 0.3 x VCC	7, 8A, 8B	-55°C, +25°C, +125°C	4.0	0.5	V

NOTES:

1. All voltages referenced to device ground.
2. No output current loads, no active input or long line pull-up resistors, and with the device configured with the MAKEBITS 'tie' option.
3. Force/Measure functions may be interchanged.
4. $\overline{\text{PWRDWN}}$ transitions must occur during operational VCC levels.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
SWITCHING CHARACTERISTICS, GENERAL LCA (SEE FIGURE 1)							
DONE/$\overline{\text{PROG}}$ Program Width (Low)	(5) TPGW	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	-	-	µs
			10, 11	-55°C, +125°C	6	-	µs
DONE/$\overline{\text{PROG}}$ Initialization	(6) TPGI	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	-	-	µs
			10, 11	-55°C, +125°C	-	7	µs
RESET M2, M1, M0 Setup (Note 3)	(2) TMR	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	-	-	µs
			10, 11	-55°C, +125°C	1	-	µs
RESET M2, M1, M0 Hold (Note 3)	(3) TRM	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	-	-	µs
			10, 11	-55°C, +125°C	1	-	µs
RESET Width (Low) Abort (Note 3)	(4) TMRW	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	-	-	µs
			10, 11	-55°C, +125°C	6	-	µs
SWITCHING CHARACTERISTICS, PERIPHERAL MODE PROGRAMMING (SEE FIGURE 4, NOTE 4)							
$\overline{\text{WS}}$ Low	(1) TCA	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	-	-	µs
			10, 11	-55°C, +125°C	0.5	-	µs
DIN Setup	(2) TDC	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	-	-	ns
			10, 11	-55°C, +125°C	60	-	ns
DIN Hold	(3) TCD	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	-	-	ns
			10, 11	-55°C, +125°C	0	-	ns
READY/$\overline{\text{BUSY}}$	(4) TWTRB	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	-	-	ns
			10, 11	-55°C, +125°C	-	60	ns
SWITCHING CHARACTERISTICS, SLAVE MODE PROGRAMMING (SEE FIGURE 5, NOTE 4)							
CCLK to DOUT	(3) TCCO	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	-	-	ns
			10, 11	-55°C, +125°C	-	100	ns
CCLK to DIN Setup	(1) TDCC	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	-	-	ns
			10, 11	-55°C, +125°C	60	-	ns
CCLK to DIN Hold	(2) TCCD	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	-	-	ns
			10, 11	-55°C, +125°C	60	-	ns
CCLK, High Time	(4) TCCH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	-	-	µs
			10, 11	-55°C, +125°C	0.5	-	µs
CCLK, Low Time	(5) TCCL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	-	-	µs
			10, 11	-55°C, +125°C	0.5	1.0	µs
CCLK, Frequency	FCC	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	-	-	MHz
			10, 11	-55°C, +125°C	-	1.0	MHz
SWITCHING CHARACTERISTICS, PROGRAM READBACK (SEE FIGURE 7, NOTES 5, 6)							
RTRIG Setup	(1) TRTH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	-	-	ns
			10, 11	-55°C, +125°C	250	-	ns
CCLK, RTRIG Setup	(2) TRTCC	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	-	-	ns
			10, 11	-55°C, +125°C	200	-	ns
CCLK, RDATA Delay	(3) TCCRD	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	-	-	ns
			10, 11	-55°C, +125°C	-	100	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	(NOTE 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
SWITCHING CHARACTERISTICS, PROGRAM READBACK (SEE FIGURE 7, NOTES 5, 6) CONTINUED							
CCLK, Clock Low	(4) TTCLR	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	-	-	µs
			10, 11	-55°C, +125°C	0.5	1.0	µs
CCLK, Clock High	(5) TCCHR	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	-	-	µs
			10, 11	-55°C, +125°C	0.5	-	µs
BENCHMARK PATTERNS							
TPID + Interconnect + 8(TILO) + TOP. Measure 8 Columns	TB1	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	-	-	ns
			10, 11	-55°C, +125°C	-	135	ns
TCKO + TICK + TCKI + Interconnect	TB2	VCC = 4.5V, VIH = 3.0V, VIL = 0V (On all CLBs)	9	+25°C	-	-	ns
			10, 11	-55°C, +125°C	-	32	ns
TCKO + TQLO + TILO + TDICK + Interconnect	TB3	VCC = 4.5V, VIH = 3.0V, VIL = 0V (On all CLBs)	9	+25°C	-	-	ns
			10, 11	-55°C, +125°C	-	53	ns
TILO + TECCK + Interconnect	TB4	VCC = 4.5V, VIH = 3.0V, VIL = 0V (On all CLBs)	9	+25°C	-	-	ns
			10, 11	-55°C, +125°C	-	35	ns
TOKPO + TOPS - TOPF + TPICK	TB5	VCC = 4.5V, VIH = 3.0V, VIL = 0V (On all CLBs)	9	+25°C	-	-	ns
			10, 11	-55°C, +125°C	-	73	ns
TCKO + TQLO + TPUS + TICK + Interconnect	TB6	VCC = 4.5V, VIH = 3.0V, VIL = 0V (1 LL Pull-Up)	9	+25°C	-	-	ns
			10, 11	-55°C, +125°C	-	73	ns
TCKO + TQLO + TPUS + TICK + Interconnect	TB7	VCC = 4.5V, VIH = 3.0V, VIL = 0V (Alt. LL Pull-Up)	9	+25°C	-	-	ns
			10, 11	-55°C, +125°C	-	83	ns
TCKO + TQLO + TIO + TICK + Interconnect	TB8	VCC = 4.5V, VIH = 3.0V, VIL = 0V (No Pull-Up, Lower LLs)	9	+25°C	-	-	ns
			10, 11	-55°C, +125°C	-	47	ns
TCKO + TQLO + TIO + TICK + Interconnect	TB9	VCC = 4.5V, VIH = 3.0V, VIL = 0V (No Pull-Up, Upper LLs)	9	+25°C	-	-	ns
			10, 11	-55°C, +125°C	-	57	ns
APPLICATION GUIDELINES, SWITCHING, CLB (SEE FIGURE 2)							
Combinatorial	(1) TILO	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	-	14	ns
RESET to CLB Output	(9) TRIO	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	-	12	ns
RESET Direct Width	(13) TRPW	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	12	-	ns
Master Reset Pin to CLB Out	TMRQ	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	-	30	ns
K Clock to CLB Output (Note 7)	(8) TCKO	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	-	12	ns
K Clock + Q through F or G to CLB Out	TQLO	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	-	11	ns
K Clock to Logic Input Setup	(2) TICK	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	12	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	(NOTE 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
APPLICATION GUIDELINES, SWITCHING, CLB (SEE FIGURE 2) CONTINUED							
K Clock to Logic Input Hold	(3) TCKI	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	1	-	ns
K Clock to Data Input Setup	(4) TDICK	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	8	-	ns
K Clock to Data Input Hold	(5) TCKDI	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	6	-	ns
K Clock to Enable Clock Setup	(6) TECCK	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	10	-	ns
K Clock to Enable Clock Hold	(7) TCKEC	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	0	-	ns
K Clock High (Notes 7, 8)	(11) TCH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	9	-	ns
K Clock Low (Note 8)	(12) TCL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	9	-	ns
APPLICATION GUIDELINES, SWITCHING, INTERNAL BUFFERS							
Clock Buffer	TGCK	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	-	9	ns
TBUF Data to Output, Tri-State to Output	TIO	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	-	8	ns
TBUF Single Pull-Up	TPUS	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	-	34	ns
TBUF Pair of Pull-Ups	TPUF	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	-	17	ns
TBUF Bidirectional	TBIDI	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	-	6	ns
APPLICATION GUIDELINES, SWITCHING, IOB (SEE FIGURE 3, NOTE 9)							
PAD (Pkg Pin) to Inputs TCLKIN, BCLKIN	TPIDC	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	-	5	ns
PAD (Pkg Pin) to Inputs DIRECT IN	(3) TPID	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	-	9	ns
I/O CLOCK to I/O RI Input (FF)	(4) TIKRI	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	-	11	ns
I/O CLOCK to I/O Pad-Input Setup	(1) TPICK	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	30	-	ns
I/O CLOCK to I/O Pad-Input Hold	(2) TIKPI	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	0	-	ns
I/O CLOCK to I/O Pad (Fast)	(7) TOKPO	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	-	18	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	(NOTE 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
APPLICATION GUIDELINES, SWITCHING, IOB (SEE FIGURE 3, NOTE 9) CONTINUED							
I/O CLOCK to I/O Pad-Output Setup	(5) TOOK	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	15	-	ns
I/O CLOCK to I/O Pad Output Hold	(6) TOKO	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	0	-	ns
CLOCK (High) Note 8	(11) TIOH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	9	-	ns
CLOCK (Low) Note 8	(12) TIOL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	9	-	ns
Output to PAD (Enabled Fast)	(10) TOPF	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	-	15	ns
Output Pad (Enabled Slow)	(10) TOPS	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	-	40	ns
Three-State to PAD Begin HI-Z (Fast)	(9) TTSHZ	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	-	18	ns
Three-State to PAD Valid (Fast)	(8) TTSON	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	-	20	ns
Master RESET to Input RI	(13) TRRI	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	-	35	ns
Master RESET to Output (FF)	(14) TRPO	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	-	50	ns
APPLICATION GUIDELINES, SWITCHING, MASTER PARALLEL MODE PROG. (SEE FIGURE 6, NOTE 10)							
$\overline{\text{RCLK}}$ to Address Valid	(1) TRAC	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	0	200	ns
$\overline{\text{RCLK}}$ to Data Setup	(2) TDRC	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	60	-	ns
$\overline{\text{RCLK}}$ to Data Hold	(3) TRCD	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	0	-	ns
$\overline{\text{RCLK}}$ (High)	TRCH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	600	-	ns
$\overline{\text{RCLK}}$ (Low)	TRCL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	N/A	+25°C	-	-	ns
				-55°C, +125°C	4.0	-	ns

NOTES:

1. All voltages referenced to device ground.
2. Force/Measure functions may be interchanged.
3. $\overline{\text{RESET}}$ timing relative to valid mode lines (M0, M1, M2) is relevant only when $\overline{\text{RESET}}$ is used to delay configuration.
4. Configuration must be delayed until the $\overline{\text{INIT}}$ of all LCA's is high. $\overline{\text{WS}}$ cannot go active until RDY/$\overline{\text{BUSY}}$ goes HIGH.
5. Readback should not be initiated until configuration is complete.
6. DOUT timing is the same as for slave mode.
7. The CLB K to Q output delay (TCKO) plus the shortest possible interconnect delay is always longer than the Data In hold time requirement (TCKDI) on the same die.
8. These parameters are for clock pulses within an LCA device. Increase values by 20% for externally applied clock.
9. Voltage levels of unused pads must be valid logic levels. Each can be configured with the internal pull-up resistor, configured as a driven output, or driven form an external source.
10. At power-up, VCC must rise from 2.0V to VCC minimum is less than 10ms. Otherwise, delay configuration using $\overline{\text{RESET}}$.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, VIH 5.0V, VIL = 0.0V, f = 1MHz	1	+25°C	TBD		pF
				-55°C, +125°C	TBD		pF
Input Capacitance	CIN	VCC = 5.0V, VIH 5.0V, VIL = 0.0V, f = 1MHz	1	+25°C	-	-	pF
				-55°C, +125°C	-	TBD	pF
Output Capacitance	COUT	VCC = 5.0V, VIH 5.0V, VIL = 0.0V, f = 1MHz	1	+25°C	-	-	pF
				-55°C, +125°C	-	TBD	pF

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max limits are guaranteed but not directly tested. These parameters are characterized at initial design release and upon design changes which would affect these characteristics.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	NOTES 1, 2 CONDITIONS	TEMPERATURE	300K LIMITS MIN	300K LIMITS MAX	UNITS
Quiescent Operational Supply Current (CMOS Mode)	ICCO	VCC = 5.5V, VIN = VCC or GND (Note 3)	+25°C	-	10	mA
Quiescent Operational Supply Current (TTL Mode)	ICCO	VCC = VIN = 5.5V, $\overline{PWRDWN}$ = 0V (Note 3)	+25°C	-	24	mA
Power Down Supply Current	ICCPD	VCC = 5.5V, VIN = VCC or GND	+25°C	-	5	mA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VIL = 0V, VOUT = VCC - 0.8V (Note 4)	+25°C	-4.0	-	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0V (Note 4)	+25°C	4.0	-	mA
I/O Pin Leakage (Tri-Stated)	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC, VIN = VCC or GND	+25°C	-	±10	µA
Horizontal Long Line Pull-Up Current	IRLL	VCC = 5.5V, VIN = VCC or GND, as an average	+25°C	-	2.4	mA
$\overline{PWRDWN}$ Power Down Supply	VCCPD	Note 5	+25°C	-	3.5	V
Functional Noise Immunity (TTL Mode)	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V	+25°C	4.0	0.5	V
Functional Noise Immunity (CMOS Mode)	FN	VCC = 4.5V, VIH = 0.7 x VCC, VIL = 0.3 x VCC	+25°C	4.0	0.5	V
SWITCHING CHARACTERISTICS, GENERAL LCA (SEE FIGURE 1)						
DONE/$\overline{PROG}$ Program Width (Low)	(5) TPGW	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	6	-	µs
DONE/$\overline{PROG}$ Initialization	(6) TPGI	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	7	µs
RESET M2, M1, M0 Setup (Note 6)	(2) TMR	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	1	-	µs
RESET M2, M1, M0 Hold (Note 6)	(3) TRM	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	1	-	µs
RESET Width (Low) Abort (Note 6)	(4) TMRW	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	6	-	µs
SWITCHING CHARACTERISTICS, PERIPHERAL MODE PROGRAMMING (SEE FIGURE 4, NOTE 7)						
$\overline{WS}$ Low	(1) TCA	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	0.5	-	µs
DIN Setup	(2) TDC	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	60	-	µs
DIN Hold	(3) TCD	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	0	-	µs
READY/$\overline{BUSY}$	(4) TWTRB	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	60	µs

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	NOTES 1, 2 CONDITIONS	TEMPERATURE	300K LIMITS MIN	300K LIMITS MAX	UNITS
SWITCHING CHARACTERISTICS, SLAVE MODE PROGRAMMING (SEE FIGURE 5, NOTE 7)						
CCLK to DOUT	(3) TCCO	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	100	ns
CCLK to DIN Setup	(1) TDCC	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	60	-	ns
CCLK to DIN Hold	(2) TCCD	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	60	-	ns
CCLK, High Time	(4) TCCH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	0.5	-	µs
CCLK, Low Time	(5) TCCL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	0.5	1.0	µs
CCLK, Frequency	FCC	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	1.0	MHz
SWITCHING CHARACTERISTICS, PROGRAM READBACK (SEE FIGURE 7, NOTES 8, 9)						
RTRIG Setup	(1) TRTH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	250	-	ns
CCLK, RTRIG Setup	(2) TRTCC	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	200	-	ns
CCLK, RDATA Delay	(3) TCCRD	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	100	ns
CCLK, Clock Low	(4) TTCLR	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	0.5	1.0	ns
CCLK, Clock High	(5) TCCHR	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	0.5	-	ns
BENCHMARK PATTERNS						
TPID + Interconnect + 8(TILO) + TOP. Measure 8 Columns	TB1	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	135	ns
TCKO + TICK + TCKI + Interconnect	TB2	VCC = 4.5V, VIH = 3.0V, VIL = 0V (On all CLBs)	+25°C	-	32	ns
TCKO + TQLO + TILO + TDICK + Interconnect	TB3	VCC = 4.5V, VIH = 3.0V, VIL = 0V (On all CLBs)	+25°C	-	53	ns
TILO + TECCK + Interconnect	TB4	VCC = 4.5V, VIH = 3.0V, VIL = 0V (On all CLBs)	+25°C	-	35	ns
TOKPO + TOPS - TOPF + TPICK	TB5	VCC = 4.5V, VIH = 3.0V, VIL = 0V (On all CLBs)	+25°C	-	73	ns
TCKO + TQLO + TPUS + TICK + Interconnect	TB6	VCC = 4.5V, VIH = 3.0V, VIL = 0V (1 LL Pull-Up)	+25°C	-	73	ns
TCKO + TQLO + TPUS + TICK + Interconnect	TB7	VCC = 4.5V, VIH = 3.0V, VIL = 0V (Alt. LL Pull-Up)	+25°C	-	83	ns
TCKO + TQLO + TIO + TICK + Interconnect	TB8	VCC = 4.5V, VIH = 3.0V, VIL = 0V (No Pull-Up, Lower LLs)	+25°C	-	47	ns
TCKO + TQLO + TIO + TICK + Interconnect	TB9	VCC = 4.5V, VIH = 3.0V, VIL = 0V (No Pull-Up, Upper LLs)	+25°C	-	57	ns
APPLICATION GUIDELINES, SWITCHING, CLB (SEE FIGURE 2)						
Combinatorial	(1) TILO	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	14	ns
RESET to CLB Output	(9) TRIO	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	12	ns
RESET Direct Width	(13) TRPW	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	12	-	ns
Master Reset Pin to CLB Out	TMRQ	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	30	ns
K Clock to CLB Output (Note 10)	(8) TCKO	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	12	ns
K Clock + Q through F or G to CLB Out	TQLO	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	11	ns
K Clock to Logic Input Setup	(2) TICK	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	12	-	ns

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	NOTES 1, 2 CONDITIONS	TEMPERATURE	300K LIMITS MIN	300K LIMITS MAX	UNITS
APPLICATION GUIDELINES, SWITCHING, CLB (SEE FIGURE 2) CONTINUED						
K Clock to Logic Input Hold	(3) TCKI	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	1	-	ns
K Clock to Data Input Setup	(4) TDICK	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	8	-	ns
K Clock to Data Input Hold	(5) TCKDI	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	6	-	ns
K Clock to Enable Clock Setup	(6) TECCK	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	10	-	ns
K Clock to Enable Clock Hold	(7) TCKEC	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	0	-	ns
K Clock High (Notes 10, 11)	(11) TCH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	9	-	ns
K Clock Low (Note 11)	(12) TCL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	9	-	ns
APPLICATION GUIDELINES, SWITCHING, INTERNAL BUFFERS						
Clock Buffer	TGCK	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	9	ns
TBUF Data to Output, Tri-State to Output	TIO	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	8	ns
TBUF Single Pull-Up	TPUS	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	34	ns
TBUF Pair of Pull-Ups	TPUF	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	17	ns
TBUF Bidirectional	TBIDI	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	6	ns
APPLICATION GUIDELINES, SWITCHING, IOB (SEE FIGURE 3, NOTE 12)						
PAD (Pkg Pin) to Inputs TCLKIN, BCLKIN	TPIDC	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	5	ns
PAD (Pkg Pin) to Inputs DIRECT IN	(3) TPID	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	9	ns
I/O CLOCK to I/O RI Input (FF)	(4) TIKRI	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	11	ns
I/O CLOCK to I/O Pad-Input Setup	(1) TPICK	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	30	-	ns
I/O CLOCK to I/O Pad-Input Hold	(2) TIKPI	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	0	-	ns
I/O CLOCK to I/O Pad (Fast)	(7) TOKPO	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	18	ns
I/O CLOCK to I/O Pad-Output Setup	(5) TOOK	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	15	-	ns
I/O CLOCK to I/O Pad Output Hold	(6) TOKO	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	0	-	ns
CLOCK (High) Note 11	(11) TIOH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	9	-	ns
CLOCK (Low) Note 11	(12) TIOL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	9	-	ns
Output to PAD (Enabled Fast)	(10) TOPF	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	15	ns
Output Pad (Enabled Slow)	(10) TOPS	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	40	ns
Three-State to PAD Begin HI-Z (Fast)	(9) TTSHZ	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	18	ns
Three-State to PAD Valid (Fast)	(8) TTSON	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	20	ns
Master RESET to Input RI	(13) TRRI	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	35	ns
Master RESET to Output (FF)	(14) TRPO	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	-	50	ns
APPLICATION GUIDELINES, SWITCHING, MASTER PARALLEL MODE PROG. (SEE FIGURE 6, NOTE 13)						
$\overline{\text{RCLK}}$ to Address Valid	(1) TRAC	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	0	200	ns
$\overline{\text{RCLK}}$ to Data Setup	(2) TDRC	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	60	-	ns
$\overline{\text{RCLK}}$ to Data Hold	(3) TRCD	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	0	-	ns

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	NOTES 1, 2 CONDITIONS	TEMPERATURE	300K LIMITS MIN	300K LIMITS MAX	UNITS
APPLICATION GUIDELINES, SWITCHING, MASTER PARALLEL MODE PROG. (SEE FIGURE 6, NOTE 13) CONTINUED						
$\overline{RCLK}$ (High)	TRCH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	600	-	ns
$\overline{RCLK}$ (Low)	TRCL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	4.0	-	ns

NOTES:

1. All voltage referenced to device ground.
2. Measurements made with CL > 50pF, Input tr = tf = 6ns
3. No output current loads, no active input or long line pull-up resistors, and with the device configured with the MAKEBITS 'tie' option.
4. Force/Measure functions may be interchanged.
5. $\overline{PWRDWN}$ transitions must occur during operational VCC levels.
6. $\overline{RESET}$ timing relative to valid mode lines (M0, M1, M2) is relevant only when $\overline{RESET}$ is used to delay configuration.
7. Configuration must be delayed until the $\overline{INIT}$ of all LCA's is high. $\overline{WS}$ cannot go active until RDY/$\overline{BUSY}$ goes HIGH.
8. Readback should not be initiated until configuration is complete
9. DOUT timing is the same as for slave mode.
10. The CLB K to Q output delay (TCKO) plus the shortest possible interconnect delay is always longer than the Data In hold time requirement (TCKDI) on the same die.
11. These parameters are for clock pulses within an LCA device. Increase values by 20% for externally applied clock.
12. Voltage levels of unused pads must be valid logic levels. Each can be configured with the internal pull-up resistor, configured as a driven output, or driven from an external source.
13. At power-up, VCC must rise from 2.0V to VCC minimum in less than 10ms. Otherwise, delay configuration using $\overline{RESET}$.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C) GROUP B, SUBGROUP 5

PARAMETER	SYMBOL	DELTA LIMITS
Supply Current	ICC	TBD (µA)
Tri-State Leakage Current	IOZ	TBD (nA)
Output Current (Note 1)	IOL/IOH	TBD (%)

NOTE: 1. Force/Measure functions may be interchanged.

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test I (Post Burn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test II (Post Burn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Δ	-
Interim Test III (Post-Burn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Δ	-
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	-
Group A (Note 1)		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	-
Group B	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Δ	Subgroups 1, 2, 3, 9, 10, 11
	B6	Samples/5005	1, 7, 9	-
Group D		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	-

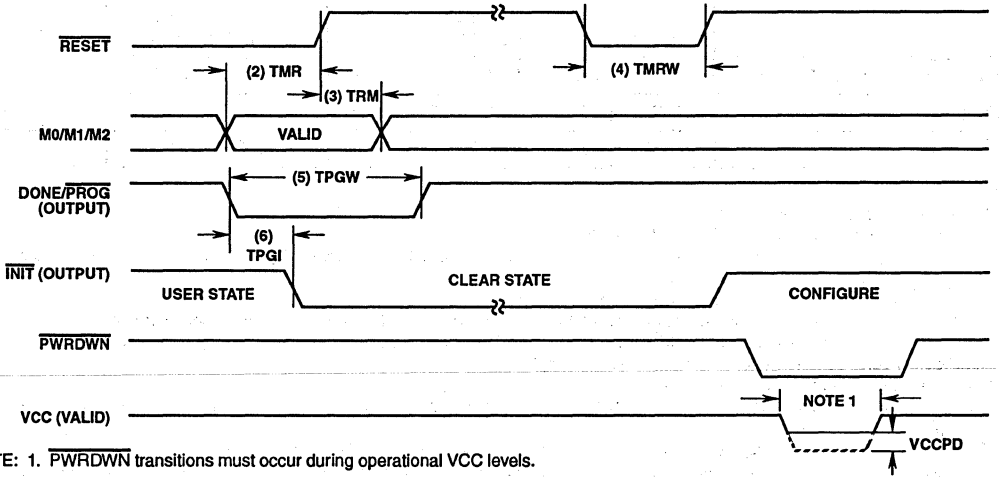
NOTE: 1. Alternate Group A testing in accordance with MIL-STD 883 method 5005 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST PRE-RAD	TEST POST-RAD	READ AND RECORD PRE-RAD	READ AND RECORD POST-RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE: 1. Except FN test which will be performed 100% GO/NOGO

Waveforms



NOTE: 1. PWRDWN transitions must occur during operational VCC levels.

FIGURE 1. GENERAL LCA WAVEFORMS

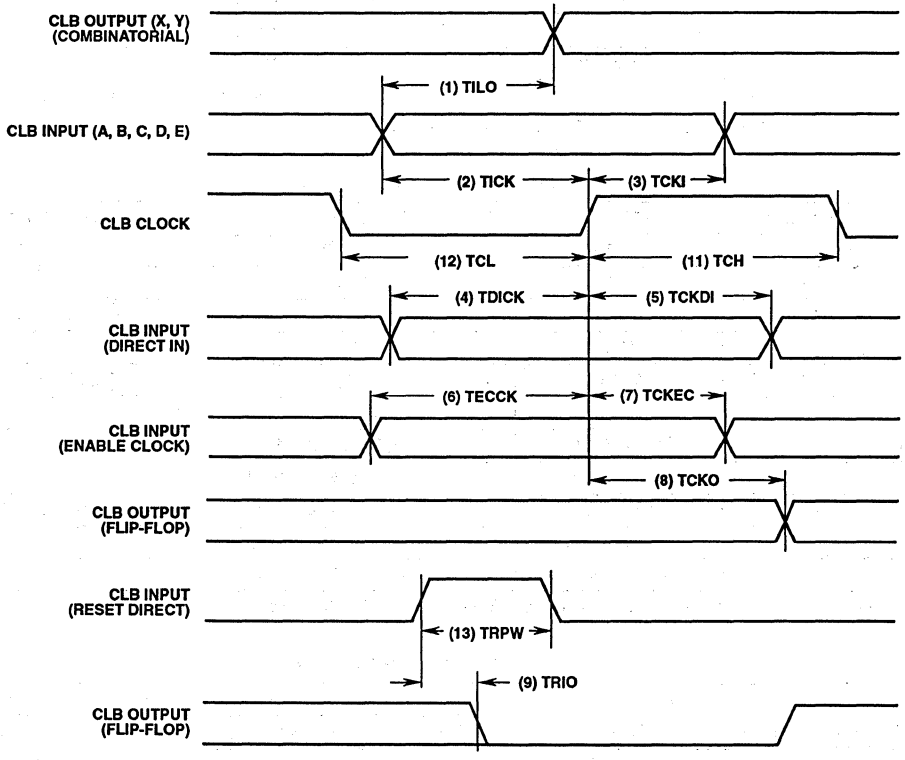


FIGURE 2. CLB WAVEFORMS

Waveforms (Continued)

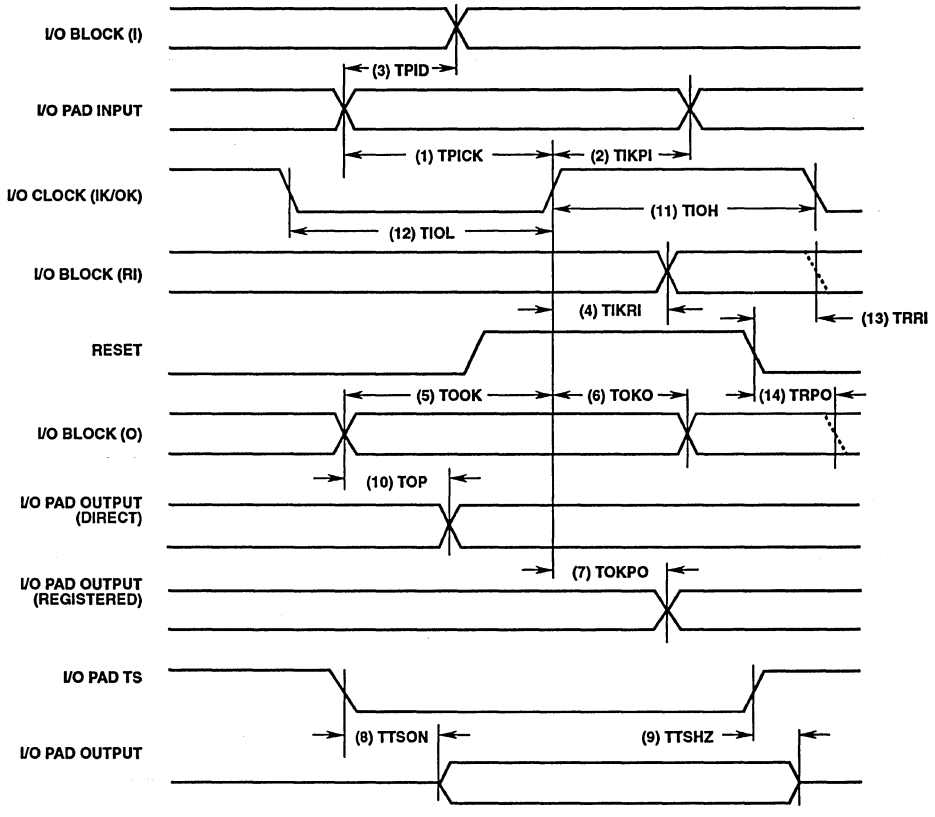
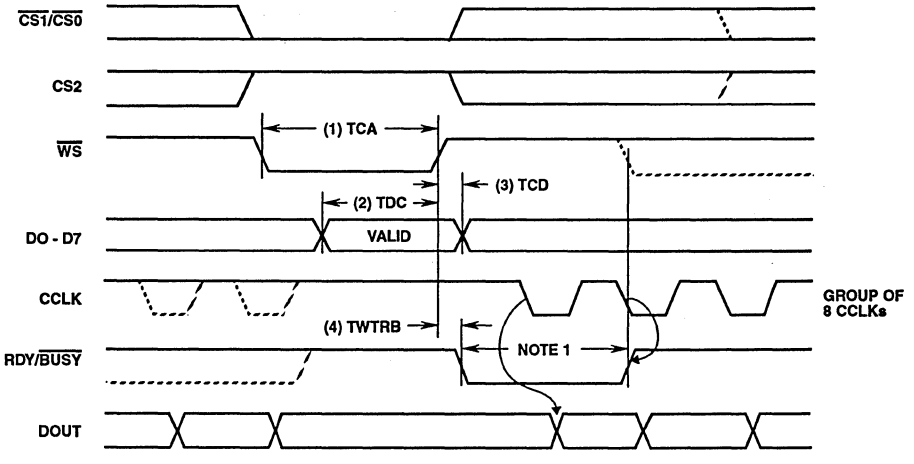


FIGURE 3. IOB WAVEFORMS



NOTE: 1. No output current loads, no active input or long line pull-up resistors, and with the device configured with the MAKEBITS 'tie' option.

FIGURE 4. PERIPHERAL MODE WAVEFORMS

Waveforms (Continued)

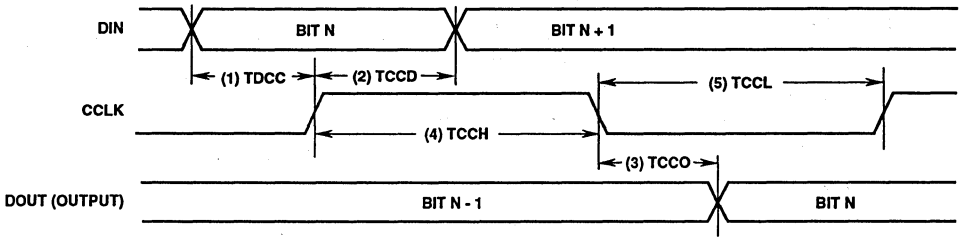


FIGURE 5. SLAVE MODE WAVEFORMS

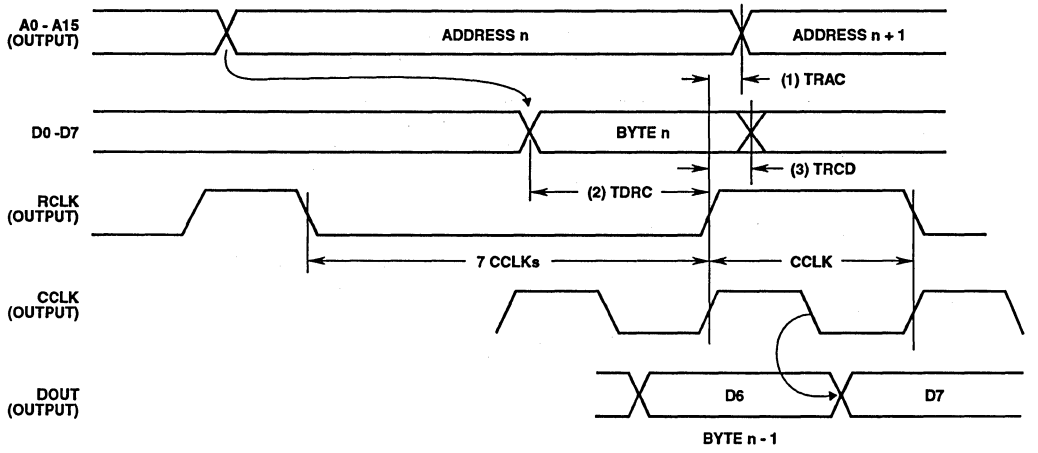


FIGURE 6. MASTER PARALLEL MODE WAVEFORMS

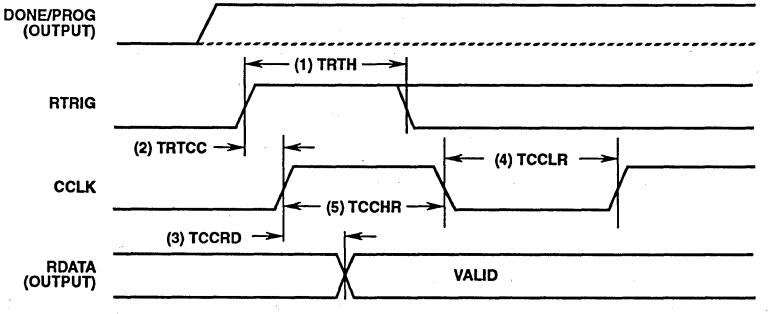


FIGURE 7. PROGRAM READBACK WAVEFORMS

Harris Space Products MS Screening

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

Radiation Verification (Each Wafer) Method 1019, 300K RAD (SI), 2 Samples/Wafer, 0 Rejects

100% Nondestructive Bond Pull Method 2023

100% Internal Visual Inspection

100% Temperature Cycling Method 1010, Condition C (-65°C to +150°C)

100% External Visual Inspection

100% Serialization

100% Initial Electrical Test (T0)

100% Static Burn-In Method 1015, 72 Hr., +125°C Min

100% Interim Electrical Tests (T1)

Burn-In Delta Calculation (T0-T1)

PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ

100% Dynamic Burn-In Method 1015, 240 Hr. at +125°C or 180 Hr. at +135°C

100% Electrical Tests Subgroups 1, 7, 9 (T2)

Delta Calculation (T0-T2)

PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ

100% Final Electrical Test +125°C, -55°C

100% Fine and Gross Seal Method 1014

100% Radiographics Method 2012

100% External Visual Method 2009

Group A (All Tests) Method 5005 (Class S)

Group B (Optional) Method 5005 (Class S) (Note 1)

Group D (Optional) Method 5005 (Class S) (Note 1)

CSI and/or GSI (Optional) (Note 2)

Data Package Generation (Note 3)

SCREENING NOTES:

1. Force/Measurements functions may be interchanged.
2. These steps are optional, and should be listed on the purchase order if required.
3. Data package Contents:
   Cover Sheet (P.O. Number, Customer Number, Lot Data Code, Harris Number, Lot Number, Quantity
   Certificated of Conformance (as found on shipper)
   Lot Serial Number Sheet (Good Unit(s) Serial Number and Lot Number)
   Variables Data (All Read, Record and Delta Operations)
   Group A Attributes Data Summary
   Wafer Lot Acceptance Report (Method 5007) to include SEM Photos.
   NOTE: SEM Photos to include % of step coverage
   X-Ray Report and File(s), including Penetrameter Measurements
   Gamma Radiation Report with Initial Shipment of Devices from the same wafer lot; containing a cover page, Disposition, Rad Dose, Lot Number, Test Package, Specification Number(s), Test Equipment, etc.; Irradiation Read and Record data will be on file at Harris.

Metallization Topology

DIE DIMENSIONS:
TBD mils
TBD mm

METALLIZATION:
Type: Al/Si/Cu
Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Silver Glass

WORST CASE CURRENT DENSITY:
2.0×10^5 A/cm^2

BOND PAD SIZE:
110µm x 110µm
4.4 x 4.4 mils

Metallization Mask Layout

TBD

RAD HARD 7

LOGIC

LOGIC (Continued)

LOGIC (Continued)

LOGIC (Continued)

LOGIC (Continued)

LOGIC (Continued)

ACS/ACTS MS Screening

Wafer Lot Acceptance	(All Lots)	Method 5007 (Includes SEM)
Radiation Verification	(EachWafer)	Method 1019, 1M RAD (SI), 4 Samples/Wafer, 0 Rejects
Nondestructive Bond Pull	100%	Method 2023
Internal Visual Inspection	100%	Method 2010
Temperature Cycling	100%	Method 1010 Condition C (-65°C to +150°C)
Constant Acceleration	100%	
PIND Testing	100%	
External Visual Inspection	100%	
Serialization	100%	
Initial Electrical Test	100%	
Static Burn-In I	100%	Method 1015, 24 Hours, +125°C Minimum
Interim Electrical Test I	100%	(Note 1)
Static Burn-In II	100%	Method 1015, 24 Hours, +125°C Minimum
Interim Electrical Test II	100%	(Note 1)
Dynamic Burn-In	100%	Method 1015, 240 Hours, +125°C or 180 Hours, at +135°C
Interim Electrical Test III	100%	(Note 1)
Final Electrical Test	100%	
Fine and Gross Seal	100%	Method 1014
Radiographics	100%	Method 2012 (2 Views)
External Visual	100%	Method 2009
Group A (All Tests)		Method 5005 (Class S)
Group B (Optional)		Method 5005 (Class S) (Note 2)
Group D (Optional)		Method 5005 (Class S) (Note 2)
CSI and/or GSI (Optional)		(Note 2)
Data Package Generation		(Note 3)

NOTES:

1. Failure from interim electrical tests I and II are combined for determining PDA (PDA = 5% for subgroups 1, 7, 9 and delta failures combined, PDA = 3% for subgroup 7 failures). Interim electrical tests III PDA (PDA = 5% for subgroups 1, 7, 9 and delta failures combined, PDA = 3% for subgroup 7 failures.
2. These steps are optional, and should be listed on the purchase order if required.
3. Data Package Contents:
   Cover Sheet (P.O. #, Customer #, Lot Data Code, Harris #, Lot #, Quantity.
   Certificate of Conformance (as found on shipper).
   Lot Serial Number Sheet (Good Unit(s), Serial # and Lot #).
   Variables Data (All Read, Record and Delata Operations).
   Group A Attributes Data Summary.
   Wafer Lot Acceptance Report (Method 5007) to include SEM photos. NOTE: SEM photos to include % of step coverage.
   X-Ray Report and file(s), including parameter measurements.
   GAMMA Radiation Report with initial shipment of devices from the same wafer lot; Containing a cover page, Disposition, Rad Dose, Lot #, Test Package, Spec #(s), Test Equipment, etc.
   Irradiation Read and Record data will be on file at Harris.

HARRIS SEMICONDUCTOR

ACS03MS

Radiation Hardened Quad 2-Input NAND Gate with Open Drain

December 1992

Features

- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose Up to 1 Mega-RAD (Si)
- Dose Rate Upset >10^{11} RAD(Si)/s, 20ns Pulse
- Cosmic Ray Upset Immunity <1 x 10^{-11} Error/Bit Day (Typ)
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.3 VCC Max
  - VIH = 0.7 VCC Min
- Input Current Levels Ii ≤ 1μA at VOL, VOH

Description

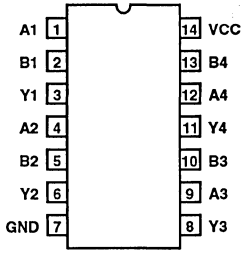
The Harris ACS03MS is a Radiation Hardened quad 2-input NAND gate with open drain outputs. The open drain output can drive resistance loads from a separate supply voltage.

The ACS03MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

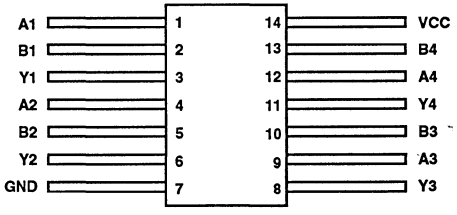
The ACS03MS is supplied in a 14 lead Ceramic flatpack (K suffix) or a Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR, CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR, CDFP3-F14, LEAD FINISH C
TOP VIEW

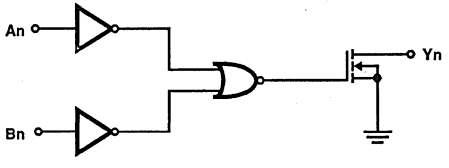


Truth Table

INPUTS		OUTPUT
An	Bn	Yn
L	L	Z*, H**
L	H	Z*, H**
H	L	Z*, H**
H	H	L

L = Low
H = High
Z = High Impedance
* Without Pull-up Resistor
** With Pull-up Resistor

Functional Diagram



7 LOGIC

File Number 3064

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +6.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±50mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
DIC	75°C/W	16°C/W
Flatpack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Input Rise and Fall Times at VCC = 4.5V (TR, TF) . . . . 10ns/V Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 30% of VCC
Input High Voltage (VIH) . . . . . VCC to 70% of VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	5	µA
			2, 3	+125°C, -55°C	-	100	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V (Note 2)	1	+25°C	16	-	mA
			2, 3	+125°C, -55°C	12	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±1.0	µA
Tri-State Output Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	1	+25°C	-1	±1	µA
			2, 3	+125°C, -55°C	-	±35	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V	7, 8A, 8B	+25°C, +125°C, -55°C	4.0	0.5	V

NOTES:

1. All voltages reference to device GND.
2. Force/Measure functions may be interchanged.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPLZ	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	15	ns
			10, 11	+125°C, -55°C	2	15	ns
Propagation Delay	TPZL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	10	ns
			10, 11	+125°C, -55°C	2	11	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Transition Time	TTHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	9	ns
			10, 11	+125°C, -55°C	1	10	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25°C	Typical 10		pF
				+125°C	Typical 10		pF
Input Capacitance	CIN	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25°C	-	10	pF
				+125°C	-	10	pF
Output Capacitance	COUT	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25°C	-	10	pF
				+125°C	-	10	pF

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	1M LIMITS MIN	1M LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.10	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0	+25°C	12	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOL = 50μA	+25°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, VIL = 1.65V, IOL = 50μA	+25°C	-	0.1	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±1	μA
Tri-State Output Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	+25°C	-	±35	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V	+25°C	4.0	0.5	V
Propagation Delay	TPLZ	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	15	ns
Propagation Delay	TPZL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	11	ns
Transition Time	TTHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	1	10	ns

NOTE:

1. All voltages referenced to device GND.

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	±1µA
IOL/IOH	5	±15%
IOZ	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	VCC = 6V ± 0.5V	$^1/_2$VCC = 3V ± 0.5V	OSCILLATOR	
				50KHz	25KHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
3, 6, 8, 11	1, 2, 4, 5, 7, 9, 10, 12, 13	14	-	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 6, 8, 11	7	1, 2, 4, 5, 9, 10, 12, 13, 14	3, 6, 8, 11	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	7	14	3, 6, 8, 11	1, 2, 4, 5, 9, 10, 12, 13	-

NOTES:

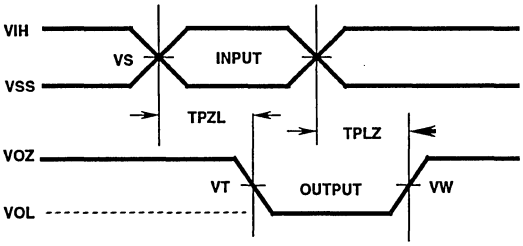
1. Each pin except VCC and GND will have a series resistor of 10K ± 5%
2. Each pin except VCC and GND will have a series resistor of 1K ± 5%

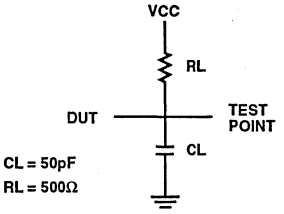
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 6, 8, 11	7	1, 2, 4, 5, 9, 10, 12, 13, 14

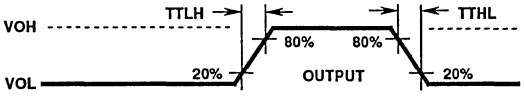
NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

Tri-State Low Timing Diagram and Load Circuit





TRANSITION TIMING DIAGRAM



TRI-STATE LOW VOLTAGE LEVELS

PARAMETER	ACS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	0.90	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
68 x 79 mils
1730mm x 2010mm

METALLIZATION:
Type: AlSiCu
Metal 1 Thickness: 6.75kÅ Min., 8.25kÅ Max.
Metal 2 Thickness: 9kÅ Min., 11kÅ Max.

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

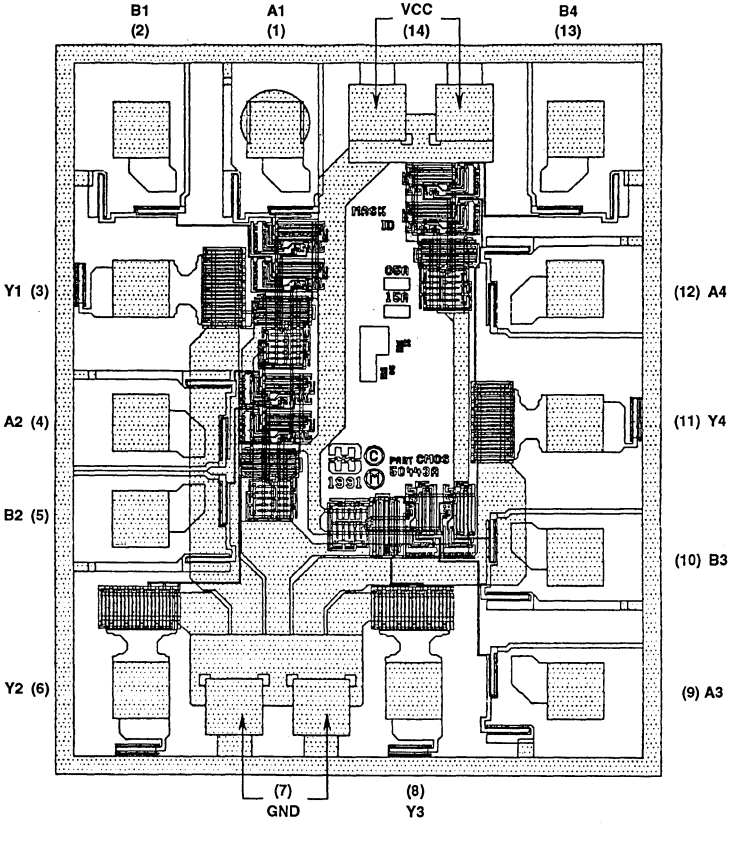
DIE ATTACH:
Material: Silver Glass

WORST CASE CURRENT DENSITY:
$< 2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
110µm x 110µm
4.3 x 4.3 mils

Metallization Mask Layout

ACS03MS



HARRIS SEMICONDUCTOR

ACTS04MS

Radiation Hardened Hex Inverter

December 1992

Features

- 1.25 Micron Radiation Hardened SOS CMOS
  - Total Dose Up To 1 Mega-RAD (Si)
  - Dose Rate Upset >10^{11} RAD(Si)/s 20ns Pulse
  - Cosmic Ray Upset Immunity (Typ. < 1 x 10^{-11} Errors/ Bit Day
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to ALSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic levels
  - VIL = 0.8V Max
  - VIH = VCC/2 V Min
- Input Current Levels Ii ≤ 1μA at VOL, VOH

Description

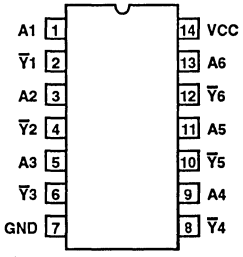
The Harris ACTS04MS is a Radiation Hardened Hex Inverter.

The ACTS04MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

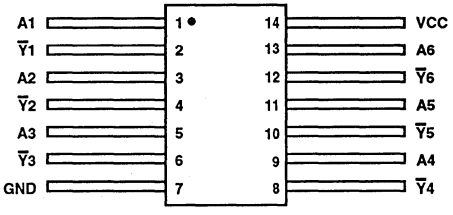
The ACTS04MS is supplied in a 14 lead Ceramic flatpack (K suffix) or a Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

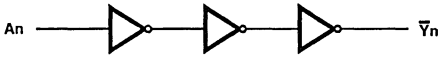


Truth Table

INPUTS	OUTPUTS
An	$\overline{Y}$n
L	H
H	L

NOTE: L = Logic Level Low,
H = Logic level High

Functional Diagram



7 LOGIC

File Number 3383

Absolute Maximum Ratings

Supply Voltage . . . . . -0.5V to +6.0V
Input Voltage Range . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±50mA
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification (All voltage reference to VSS) . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 10ns/V Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC to VCC/2 V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	.1	µA
			2, 3	+125°C, -55°C	-	100	µA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC -0.4V , VIL = 0V (Note 2)	1	+25°C	-12	-	mA
			2, 3	+125°C, -55°C	-8	-	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0V, (Note 2)	1	+25°C	12	-	mA
			2, 3	+125°C, -55°C	8	-	mA
Output Voltage High	VOH	VCC = 5.5V, VIH =2.75V, IOH = -50µA, VIL = 0.80V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Output Voltage Low	VOL	VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.80V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.80V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±1.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltages reference to device GND.
2. Force / Measure functions may be interchanged.
3. Per functional tests, VO ≥ 3.0V is recognized as a logic "1", and VO = 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay A to $\overline{Y}$	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	1	12	ns
			10, 11	+125°C, -55°C	1	14	ns
	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	1	9	ns
			10, 11	+125°C, -55°C	1	11	ns
Output Transition Time	TTHL TTLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	1	8	ns
			10, 11	+125°C, -55°C	1	9	ns

NOTES:

1. All voltages referenced to device GND.
2. Measurements made with RL = 500Ω, CL = 50pF, Input TR = TF = 3ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, VIH = 5.0V, VIL = 0.0V, f = 1MHz	1	+25°C	Typical 30		pF
			1	+125°C	Typical 40		pF
Input Capacitance	CIN	VCC = 5V, VIH = 5.0V, VIL = 0.0V, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Capacitance	COUT	VCC = 5V, VIH = 5.0V, VIL = 0.0V, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	1M LIMITS RAD MIN	1M LIMITS RAD MAX	UNITS
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.1	mA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VIL = 0, VOUT = VCC -0.4V	+25°C	-8	-	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VIL = 0, VOUT = 0.4V	+25°C	8	-	mA
Output Voltage High	VOH	VCC = 5.5V, VIH = 2.75V, VIL = 0.80V, IOH = -50µA	+25°C	VCC -0.1	-	V
		VCC = 4.5V, VIH = 2.25V, VIL = 0.80V, IOH = -50µA	+25°C	VCC -0.1	-	V
Output Voltage Low	VOL	VCC = 5.5V, VIH = 2.75V, VIL = 0.80V, IOH = 50µA	+25°C	-	0.1	V
		VCC = 4.5V, VIH = 2.25V, VIL = 0.80V, IOH = 50µA	+25°C	-	0.1	V

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	1M LIMITS RAD		UNITS
				MIN	MAX	
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±1	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.80V	+25°C	-	-	V
Propagation Delay A to $\overline{Y}$	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	1	14	ns
	TPLH		+25°C	1	11	ns
Output Transition Time	TTHL TTLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	1	9	ns

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMIT	UNITS
Supply Current	ICC	±1	µA
Output Current	IOL / IOH	±15	%

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A testing in accordance with MIL-STD-883 Method 5005 of may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I (Note 1)					
-	1, 3, 5, 7, 9, 11, 13	2, 4, 6, 8, 10, 12	14	-	-
STATIC BURN-IN II (Note 1)					
-	7	2, 4, 6, 8, 10, 12	1, 3, 5, 9, 11, 13, 14	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 1)					
-	7	2, 4, 6, 8, 10, 12	14	1, 3, 5, 9, 11, 13	-

NOTES:

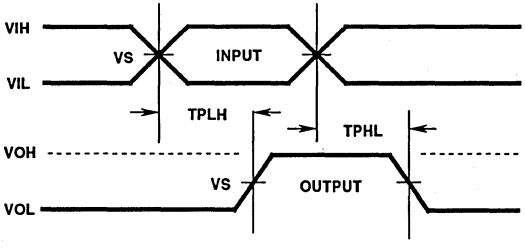
1. Each pin except VCC and GND will have a resistor of 500Ω ± 5%.

TABLE 9. IRRADIATION TEST CONNECTIONS

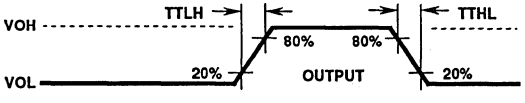
OPEN	GROUND	VCC = 5V ± 0.5V
2, 4, 6, 8, 10, 12	7	1, 3, 5, 9, 11, 13, 14

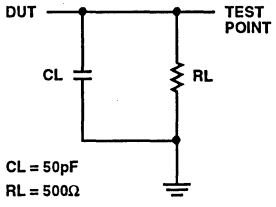
NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5%. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

AC Timing Diagrams and Load Circuit



TRANSITION TIMING DIAGRAM





AC VOLTAGE LEVELS

PARAMETER	ACTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
88 x 88 mils
2240 x 2240mm

METALLIZATION:
Type: AlSiCu
Metal 1 Thickness: 6.75kÅ Min, 8.25kÅ Max
Metal 2 Thickness: 9kÅ Min, 11kÅ Max

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

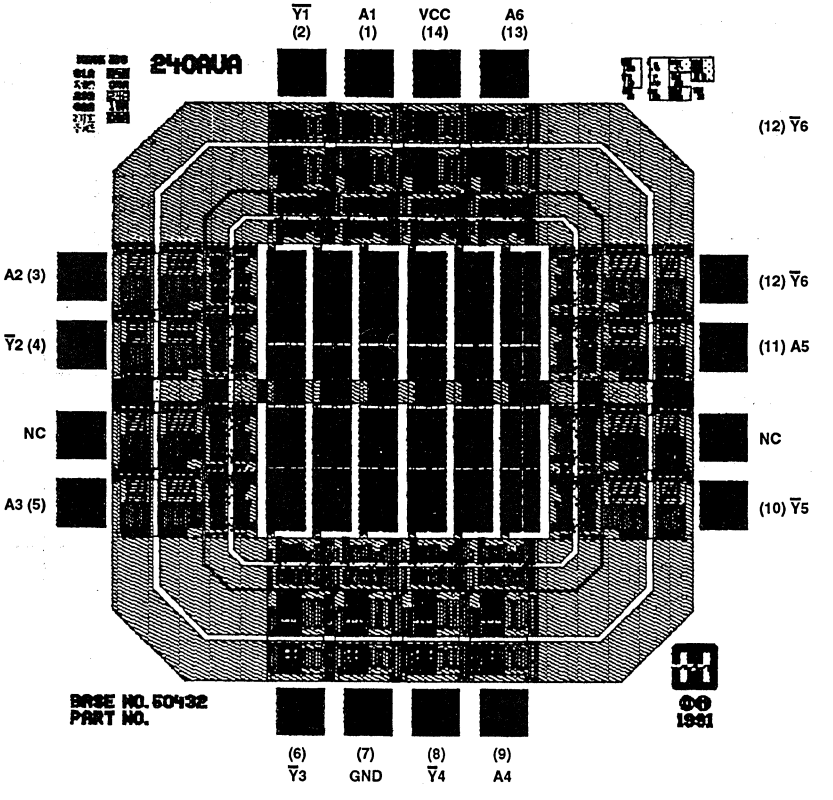
DIE ATTACH:
Material: Silver Glass

WORST CASE CURRENT DENSITY:
$< 2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
4.3 mils x 4.3 mils
> 110µm x 110µm

Metallization Mask Layout

ACTS04MS



HARRIS SEMICONDUCTOR

ACTS74MS

Radiation Hardened Dual D Flip Flop with Set and Reset

December 1992

Features

- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose Up to 1 Mega-RAD (Si)
- Dose Rate Upset >10^{11} RAD(Si)/s, 20ns Pulse
- Cosmic Ray Upset Immunity < 10^{-11} Errors/Bit-Day
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to ALSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.8V Max
  - VIH = VCC/2V Min
- Input Current Levels Ii ≤ 1μA at VOL, VOH

Description

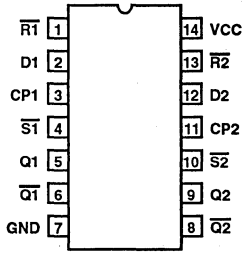
The Harris ACTS74MS is a Radiation Hardened dual D flip flop with set(s) and reset (R). The logic level at data input is transferred to the output during the positive transition of the clock. The Set and Reset are independent from the clock and accomplished by a low level on the appropriate input.

The ACTS74MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

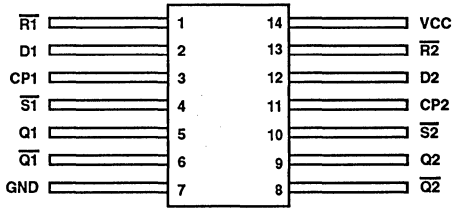
The ACTS74MS is supplied in a 14 lead Ceramic flatpack (K suffix) or a 14 Lead Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW



Truth Table

INPUTS				OUTPUTS	
SET	RESET	CP	D	Q	Q
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↗	H	H	L
H	H	↗	L	L	H
H	H	L	X	Q0	Q0

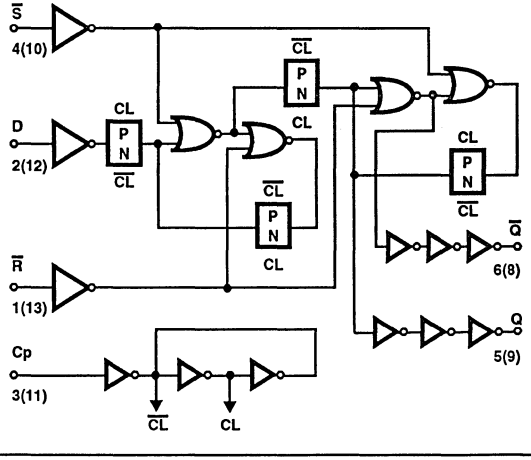
H = High Level (Steady State)
L = Low Level (Steady State)
X = Don't Care
↗ = Transition from Low to High Level

NOTES:

1. Q0 = the level of Q before the indicated input conditions were established.

*This configuration is nonstable, that is, it will not persist when set and reset inputs return to their inactive (high) level.

Functional Diagram



7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3382

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +6.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input. . . . . ±10mA
DC Drain Current, Any One Output. . . . . ±50mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
DIC	75°C/W	16°C/W
Flatpack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 10ns/V Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Source)	IOH	VCC = VIH = 4.5V VOUT = VCC - 0.4V, VIL = 0V (Note 2)	1	+25°C	-12	-	mA
			2, 3	+125°C, -55°C	-8	-	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V VOUT = 0.4V VIL = 0V (Note 2)	1	+25°C	12	-	mA
			2, 3	+125°C, -55°C	8	-	mA
Output Voltage High	VOH	VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC - 0.1	-	V
		VCC = 4.5V, VIH =2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC - 0.1	-	V
Output Voltage Low	VOL	VCC = 5.5V, VIH = 2.75V, IOH = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 4.5V, VIH = 2.25V, IOH = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	1.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 3)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:
1. All voltages reference to device GND.
2. Force/Measure functions may be interchanged.
3. Per functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO = 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay CP to Q, $\overline{Q}$	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	1	20	ns
			10, 11	+125°C, -55°C	1	20	ns
	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	1	15	ns
			10, 11	+125°C, -55°C	1	18	ns
Propagation Delay $\overline{S}$ to Q, $\overline{Q}$	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	1	16	ns
			10, 11	+125°C, -55°C	1	17	ns
	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	1	12	ns
			10, 11	+125°C, -55°C	1	13	ns
Propagation Delay $\overline{R}$ to Q, $\overline{Q}$	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	1	16	ns
			10, 11	+125°C, -55°C	1	17	ns
	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	1	12	ns
			10, 11	+125°C, -55°C	1	13	ns
Output Transition Time	TTHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	1	11	ns
	TTLH		10, 11	+125°C, -55°C	1	12	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, VIH = 5.0V F = 1MHz	1	+25°C	Typical 43		pF
			1	+125°C	Typical 50		pF
Input Capacitance	CIN	VCC = 5.0V, VIH = 5.0V F = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Pulse Width CP, $\overline{S}$, $\overline{R}$	TW	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	5.5	-	ns
			1	+125°C	6.3	-	ns
Data to CP Set-up Time	TSU	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	4.3	-	ns
			1	+125°C	4.9	-	ns
Hold Time	TH	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	2	-	ns
			1	+125°C	2	-	ns
Removal Time $\overline{S}$, $\overline{R}$ to CP	TREM	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	3.7	-	ns
			1	+125°C	3.7	-	ns
Max Operating Frequency	FMAX	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	79	-	MHz
			1	+125°C	76	-	MHz

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	1M LIMITS MIN	1M LIMITS MAX	UNITS
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	mA
Output Current (Source)	IOH	VCC = VIH = 4.5V VOUT = VCC -0.4V, VIL = 0,	+25°C	-8	-	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V VOUT = 0.4V, VIL = 0,	+25°C	8	-	mA
Output Voltage High	VOH	VCC = 5.5V, VIH = 2.75V, VIL = 0.8V, IOH = -50µA	+25°C	VCC -0.1	-	V
		VCC = 4.5V, VIH = 2.25V, VIL = 0.8V, IOH = -50µA	+25°C	VCC -0.1	-	V
Output Voltage Low	VOL	VCC = 5.5V, VIH = 2.75V, VIL = 0.8V, IOH = 50µA	+25°C	-	0.1	V
		VCC = 4.5V, VIH = 2.25V, VIL = 0.8V, IOH = 50µA	+25°C	-	0.1	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±1	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	+25°C	-	-	V
Propagation Delay CP to Q, $\overline{Q}$	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	1	20	ns
	TPLH		+25°C	1	18	ns
Propagation Delay $\overline{S}$ to Q, $\overline{Q}$	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	1	17	ns
	TPLH		+25°C	1	13	ns
Propagation Delay $\overline{R}$ to Q, $\overline{Q}$	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	1	17	ns
	TPLH		+25°C	1	13	ns
Output Transition Time	TTHL TTLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	1	12	ns

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMIT	UNITS
Supply Current	ICC	±2	µA
Output Current	IOL / IOH	±15	%

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with MIL-STD-883 Method 5005 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
-	1, 2, 3, 4, 7, 10, 11, 12, 13	5, 6, 8, 9	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
-	7	5, 6, 8, 9	1, 2, 3, 4, 10, 11, 12, 13, 14	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	7	5, 6, 8, 9	1, 4, 10, 13, 14	3, 11	2, 12

NOTES:

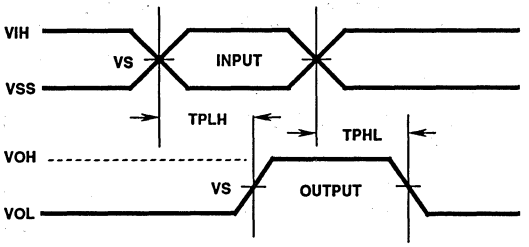
1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1kΩ ± 5% for dynamic burn-in.

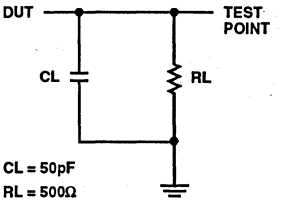
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V	1/2 VCC = 3V ± 0.5V
5, 6, 8, 9	7	1, 2, 3, 4, 10, 11, 12, 13, 14	-

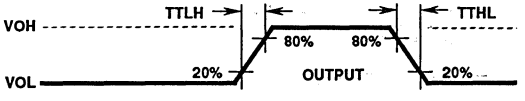
NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

Propagation Delay Timing Diagram and Load Circuit





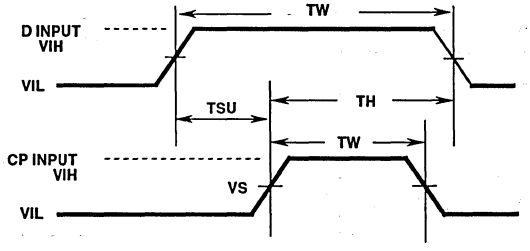
Transition Timing Diagram



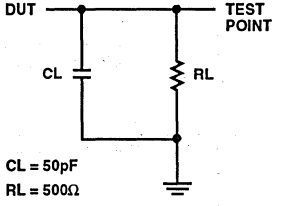
PROPAGATION DELAY VOLTAGE LEVELS

PARAMETER	ACTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Pulse Width, Setup, Hold Timing Diagram Positive Edge Trigger



TH = Hold Time
TSU = Setup Time
TW = Pulse Width



PULSE WIDTH, SETUP, HOLD VOLTAGE LEVELS

PARAMETER	ACTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
88 x 88 mils
2240 x 2240 mm

METALLIZATION:
Type: AlSiCu
Metal 1 Thickness: 6.75kÅ ± 8.25kÅ
Metal 2 Thickness: 9kÅ ± 11kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

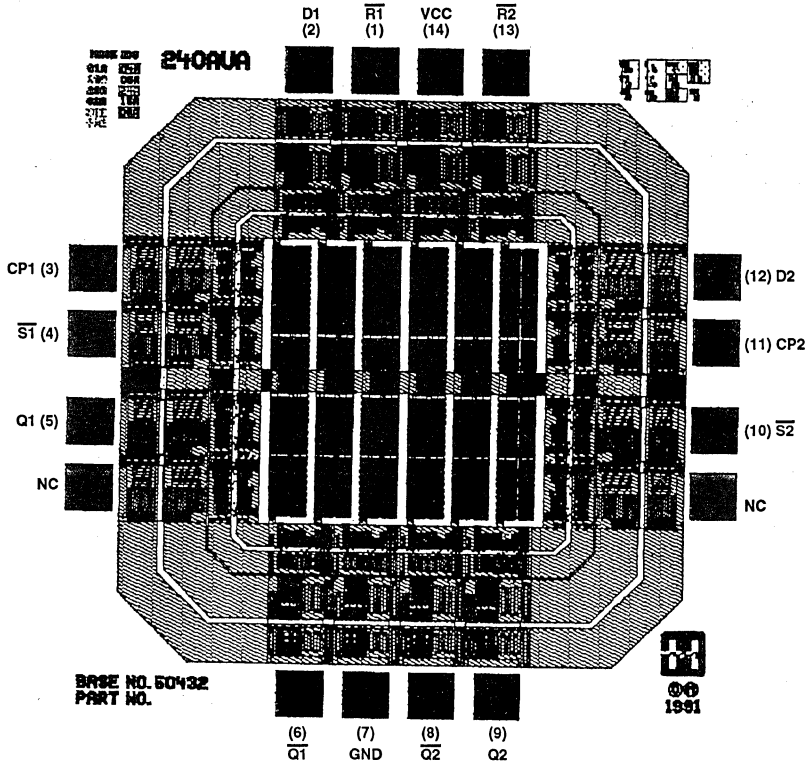
DIE ATTACH:
Material: Silver Glass

WORST CASE CURRENT DENSITY:
$< 2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
110µm x 110µm
4.3 x 4.3 mils

Metallization Mask Layout

ACTS74MS



HARRIS SEMICONDUCTOR

ACTS240MS

High Reliability, Radiation Hardened High-Speed CMOS/SOS

December 1992

Features

- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose Up to 1 Mega-RAD (Si)
- Dose Rate Upset >10^{11} RADs/Sec. 20ns Pulse
- Cosmic Ray Upset Immunity < 1 x 10^{-11} Errors/Gate Day (Typ)
- Latch Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to ALSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
  - CMOS Input Compatibility Ii ≤ 5μA at VOL, VOH

Description

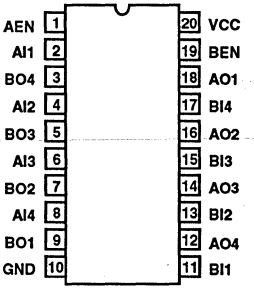
The Harris ACTS240MS is a Radiation Hardened octal inverting tri-state buffer having two active low enable inputs.

The ACTS240MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

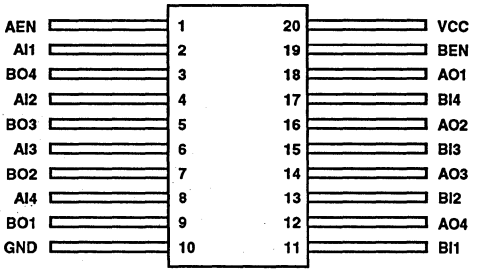
The ACTS240MS is supplied in a 20 lead Ceramic flatpack (K suffix) or a Dual-In-Line Ceramic Package (D suffix).

Pinouts

20 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T20, LEAD FINISH C
TOP VIEW



20 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F20, LEAD FINISH C
TOP VIEW

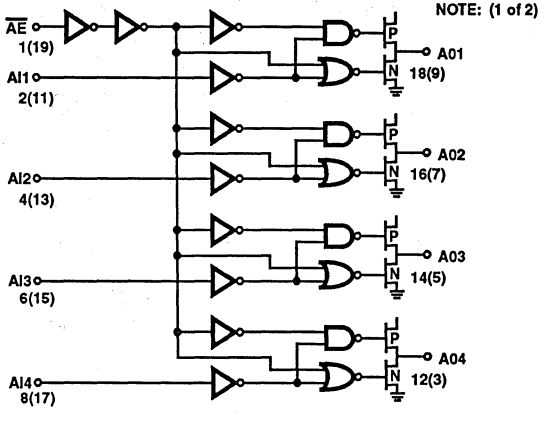


Truth Table

INPUTS		OUTPUT
$\overline{AE}$, $\overline{BE}$	AIn, BIn	AOn, BOn
L	L	H
L	H	L
H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3186

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +6.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±50mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
DIC	75°C/W	16°C/W
Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 12mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 10ns/V Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... VCC to VCC/2

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	20	µA
			2, 3	+125°C, -55°C	-	400	
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0 (Note 2)	1	+25°C	16	-	mA
			2, 3	+125°C, -55°C	12	-	
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC - 0.4V VIL = 0 (Note 2)	1	+25°C	-16	-	mA
			2, 3	+125°C, -55°C	-12	-	
Output Voltage Low	VOL	VCC = 4.5V, VIH = 4.5V, IOL = 50µA, VIL = 0V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 5.5V, IOL = 50µA, VIL = 0V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 4.5V, IOH = -50µA, VIL = 0V	1, 2, 3	+25°C, +125°C, -55°C	VCC-0.1	-	V
		VCC = 5.5V, VIH = 5.5V, IOH = -50µA, VIL = 0V	1, 2, 3	+25°C, +125°C, -55°C	VCC-0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±1.0	
Tri-State Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	1	+25°C	-	±1.0	µA
			2, 3	+125°C, -55°C	-	±35	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = VCC/2, VIL = 0.8V (Note 3)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltage referenced to device GND.
2. Force/Measure function may be interchanged.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPLH	VCC = 4.5V, VIH = 3V, VIL = 0V	9	+25°C	1	8.5	ns
			10, 11	+125°C, -55°C	1	9.5	
	TPHL		9	+25°C	1	11.5	ns
			10, 11	+125°C, -55°C	1	13.0	
Tri-State Test	TPZL	VCC = 4.5V, VIH = 3V, VIL = 0	9	+25°C	2	14.0	ns
			10, 11	+125°C, -55°C	2	16.0	
	TPZH		9	+25°C	2	10.5	ns
			10, 11	+125°C, -55°C	2	11.5	
	TPLZ	VCC = 4.5V, VIH = 3V, VIL = 0	9	+25°C	2	14.0	ns
			10, 11	+125°C, -55°C	2	14.5	
	TPHZ		9	+25°C	2	14.5	ns
			10, 11	+125°C, -55°C	2	15.5	
Output Transition Time	TTLH	VCC = 4.5V, VIH = 3V, VIL = 0	9	+25°C	1	5.0	ns
			10, 11	+125°C, -55°C	1	5.0	
	TTHL		9	+25°C	1	5.0	ns
			10, 11	+125°C, -55°C	1	5.0	

NOTES:

1. All voltage referenced to device GND.
2. Measurements made with CL = 50pF, RL = 500Ω, Input TR = TF = 3ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5V, VIH = 5V, VIL = 0V, f = 1MHz	1	+25°C	Typical 40		pF
			1	+125°C	Typical 40		pF
Input Capacitance	CIN	VCC = 5V, VIH = 5V, VIL = 0V, f = 1MHz	1	+25°C	-	18	pF
			1	+125°C	-	18	pF
Output Capacitance	COUT	VCC = 5V, VIH = 5V, VIL = 0V, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	1 MEG LIMITS MIN	1 MEG LIMITS MAX	UNITS
Quiescent Current	ICC	VIN = 5.5V, VIN = VCC or GND	+25°C	-	0.4	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0, (Note 2)	+25°C	12	-	mA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0, (Note 2)	+25°C	-12	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 4.5V, VIL = 0V, IOL = 50µA	+25°C	-	0.1	V
		VCC = 5.5V, VIH = 5.5V, VIL = 0V, IOL = 50µA		-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 4.5V, VIL = 0V, IOH = -50µA	+25°C	VCC-0.1	-	V
		VCC = 5.5V, VIH = 5.5V, VIL = 0V, IOH = -50µA		VCC-0.1	-	V
Tri-State Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	+25°C	-	±35	µA
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±1	µA
Noise Immunity Functional	FN	VCC = 4.5V, VIL = 0.8V, VIH = VCC/2 (Note 3)	+25°C	-	-	-
Propagation Delay	TPLH	VCC = 4.5V, VIH = 3V, VIL = 0V	+25°C	1	9.5	ns
	TPHL			1	13	ns
Tri-State Test	TPZL	VCC = 4.5V, VIH = 3V, VIL = 0V	+25°C	2	16	ns
	TPZH			2	11.5	ns
	TPLZ			2	14.5	ns
	TPHZ			2	15.5	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	±4µA
IOL/IOH	5	±15% of 0 Hour
IOZL/IOZH	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/6005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11; Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/6005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
3, 5, 7, 9, 12, 14, 16, 18	1, 2, 4, 6, 8, 10, 11, 13, 15, 17, 19	-	20	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 5, 7, 9, 12, 14, 16, 18	10	-	1, 2, 4, 6, 8, 11, 13, 15, 17, 19, 20	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 1)					
-	1, 10, 19	3, 5, 7, 9, 12, 14, 16, 18	20	-	2, 4, 6, 8, 11, 13, 15, 17

NOTES:

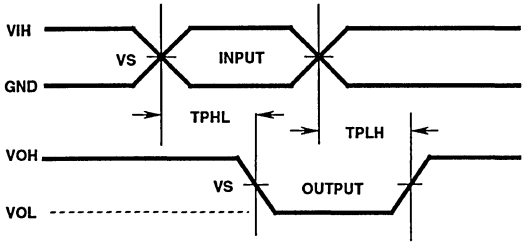
1. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for burn-in.

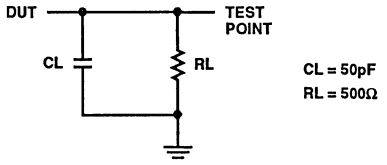
TABLE 9. RADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 5, 7, 9, 12, 14, 16, 18	6, 8, 10, 15, 17, 19	1, 2, 4, 11, 13, 20

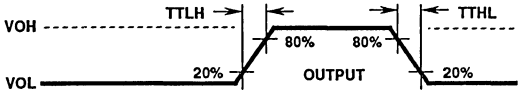
NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures.

Propagation Delay Timing Diagram and Load Circuit





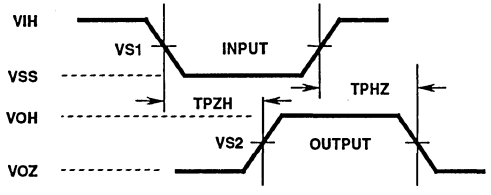
Transition Timing Diagram

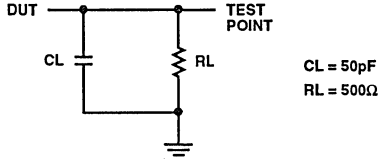


AC VOLTAGE LEVELS

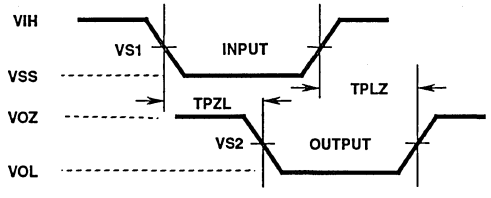
PARAMETER	ACTS	UNITS
VCC	4.50	V
VIH	3.00	V
VIL	0.0	V
VS	1.30	V
GND	0.0	V

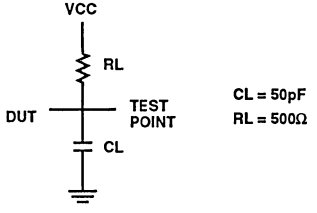
Tri-State High Timing Diagram and Load Circuit





Tri-State Low Timing Diagram and Load Circuit





TRI-STATE VOLTAGE LEVELS

	TPLH	TPHL	TPZL	TPZH	TPHZ	TPLZ
VIH	3V	3V	3V	3V	3V	3V
VS1	1.3V	1.3V	1.3V	1.3V	1.3V	1.3V
VS2	1.3V	1.3V	1.3V	1.3V	80% VCC	20% VCC
VIL	GND	GND	GND	GND	GND	GND

Die Characteristics

DIE DIMENSIONS:
100 x 100 mils
2.54 x 2.54 mm

METALLIZATION:
Type: AlSiCu
Metal 1 Thickness: 7.5kÅ ± 2kÅ
Metal 2 Thickness: 10kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

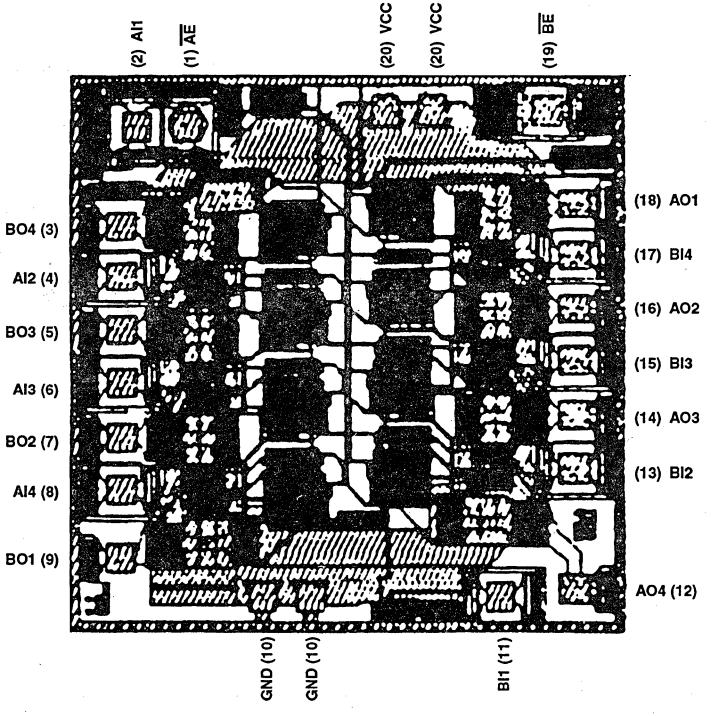
DIE ATTACH:
Material: Silver Glass

WORST CASE CURRENT DENSITY:
$< 2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
110µm x 110µm
4.4 mils x 4.4 mils

Metallization Mask Layout

ACTS240MS



HARRIS SEMICONDUCTOR

ACTS244MS

Radiation Hardened Octal Non-Inverting Tri-State Buffer

December 1992

Features

- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose Up to 1 Mega-RAD (Si)
- Dose Rate Upset >10^{11} RADs(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity < 1 x 10^{-11} Errors/Gate day (Typ)
- Latch Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to ALSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
  - CMOS Input Compatibility Ii ≤ 5μA at VOL, VOH

Description

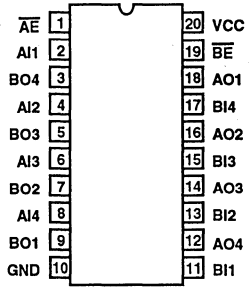
The Harris ACTS244MS is a Radiation Hardened octal non-inverting tri-state buffer having two active low enable inputs.

The ACTS244MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

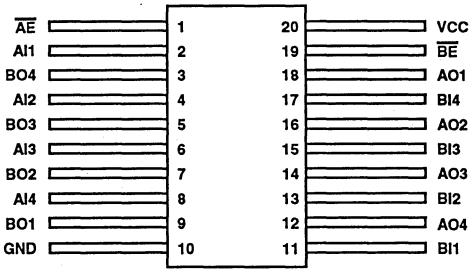
The ACTS244MS is supplied in a 20 lead Ceramic flatpack (K suffix) or a Dual-In-Line Ceramic Package (D suffix).

Pinouts

20 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T20, LEAD FINISH C
TOP VIEW



20 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F20, LEAD FINISH C
TOP VIEW

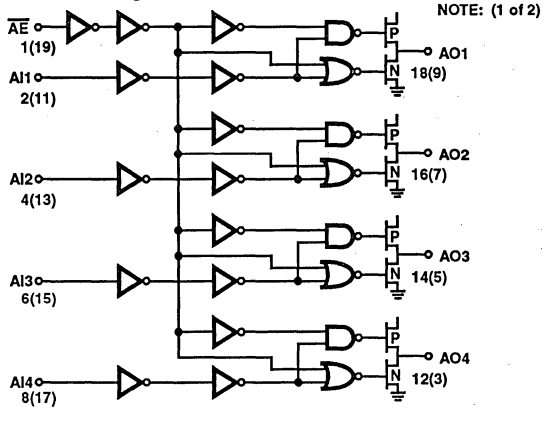


Truth Table

INPUTS		OUTPUT
$\overline{AE}$, $\overline{BE}$	AIn, BIn	AOn, BOn
L	L	L
L	H	H
H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Functional Diagram



7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3187

Absolute Maximum Ratings

Supply Voltage . . . . . -0.5V to +6.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input. . . . . ±10mA
DC Drain Current, Any One Output. . . . . ±50mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10 sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
DIC	75°C/W	16°C/W
Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 10ns/V Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC to VCC/2

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	20	µA
			2, 3	+125°C, -55°C	-	400	
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0 (Note 2)	1	+25°C	16	-	mA
			2, 3	+125°C, -55°C	12	-	
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC - 0.4V VIL = 0 (Note 2)	1	+25°C	-16	-	mA
			2, 3	+125°C, -55°C	-12	-	
Output Voltage Low	VOL	VCC = 4.5V, VIH = 4.5V, IOL = 50µA, VIL = 0V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 5.5V, IOL = 50µA, VIL = 0V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 4.5V, IOH = -50µA, VIL = 0V	1, 2, 3	+25°C, +125°C, -55°C	VCC-0.1	-	V
		VCC = 5.5V, VIH = 5.5V, IOH = -50µA, VIL = 0V	1, 2, 3	+25°C, +125°C, -55°C	VCC-0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±1.0	
Tri-State Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	1	+25°C	-	±1.0	µA
			2, 3	+125°C, -55°C	-	±35	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = VCC/2, VIL = 0.8V (Note 3)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltage referenced to device GND.
2. Force/Measure function may be interchanged.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPLH	VCC = 4.5V, VIH = 3V, VIL = 0V	9	+25°C	1	9.0	ns
			10, 11	+125°C, -55°C	1	10.0	
	TPHL		9	+25°C	1	9.0	ns
			10, 11	+125°C, -55°C	1	10.0	
Tri-State Test	TPZL	VCC = 4.5V, VIH = 3V, VIL = 0	9	+25°C	2	11.0	ns
			10, 11	+125°C, -55°C	2	14.0	
	TPZH		9	+25°C	2	10.0	ns
			10, 11	+125°C, -55°C	2	11.0	
	TPLZ	VCC = 4.5V, VIH = 3V, VIL = 0	9	+25°C	2	13.5	ns
			10, 11	+125°C, -55°C	2	14.0	
	TPHZ		9	+25°C	2	14.5	ns
			10, 11	+125°C, -55°C	2	14.5	
Output Transition Time	TTLH	VCC = 4.5V, VIH = 3V, VIL = 0	9	+25°C	1	5.0	ns
			10, 11	+125°C, -55°C	1	5.0	
	TTHL		9	+25°C	1	5.0	ns
			10, 11	+125°C, -55°C	1	5.0	

NOTES:

1. All voltage referenced to device GND.
2. Measurements made with CL = 50pF, RL = 500Ω, Input TR = TF = 3ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5V, VIH = 5V, VIL = 0V, f = 1MHz	1	+25°C	Typical 40		pF
			1	+125°C	Typical 40		pF
Input Capacitance	CIN	VCC = 5V, VIH = 5V, VIL = 0V, f = 1MHz	1	+25°C	-	15	pF
			1	+125°C	-	15	pF
Output Capacitance	COUT	VCC = 5V, VIH = 5V, VIL = 0V, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	1 MEG LIMITS		UNITS
				MIN	MAX	
Quiescent Current	ICC	VIN = 5.5V, VIN = VCC or GND	+25°C	-	0.4	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0, (Note 2)	+25°C	12	-	mA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0, (Note 2)	+25°C	-12	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 4.5V, VIL = 0V, IOL = 50µA	+25°C	-	0.1	V
		VCC = 5.5V, VIH = 5.5V, VIL = 0V, IOL = 50µA		-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 4.5V, VIL = 0V, IOH = -50µA	+25°C	VCC-0.1	-	V
		VCC = 5.5V, VIH = 5.5V, VIL = 0V, IOH = -50µA		VCC-0.1	-	V
Tri-State Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	+25°C	-	±35	µA
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±1	µA
Noise Immunity Functional	FN	VCC = 4.5V, VIL = 0.8V, VIH = VCC/2 (Note 3)	+25°C	-	-	-
Propagation Delay	TPLH	VCC = 4.5V, VIH = 3V, VIL = 0V	+25°C	1	10.0	ns
	TPHL			1	10.0	ns
Tri-State Test	TPZL	VCC = 4.5V, VIH = 3V, VIL = 0V	+25°C	2	14.0	ns
	TPZH			2	11.0	ns
	TPLZ			2	14.0	ns
	TPHZ			2	14.5	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	±4µA
IOL/IOH	5	±15% of 0 Hour
IOZL/IOZH	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/6005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/6005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
3, 5, 7, 9, 12, 14, 16, 18	1, 2, 4, 6, 8, 10, 11, 13, 15, 17, 19	-	20	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 5, 7, 9, 12, 14, 16, 18	10	-	1, 2, 4, 6, 8, 11, 13, 15, 17, 19, 20	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 1)					
-	1, 10, 19	3, 5, 7, 9, 12, 14, 16, 18	20	-	2, 4, 6, 8, 11, 13, 15, 17

NOTE:

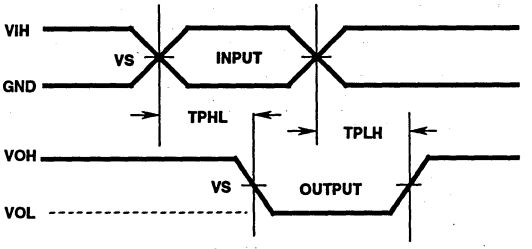
1. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for burn-in.

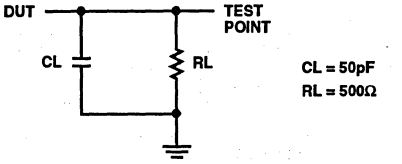
TABLE 9. RADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 5, 7, 9, 12, 14, 16, 18	6, 8, 10, 15, 17, 19	1, 2, 4, 11, 13, 20

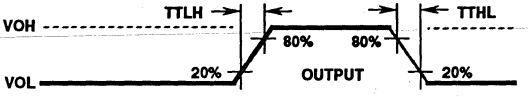
NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures.

Propagation Delay Timing Diagram and Load Circuit





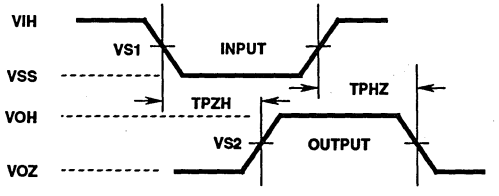
Transition Timing Diagram

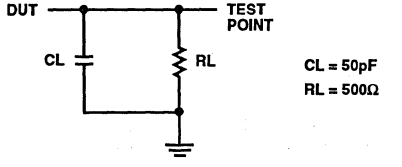


AC VOLTAGE LEVELS

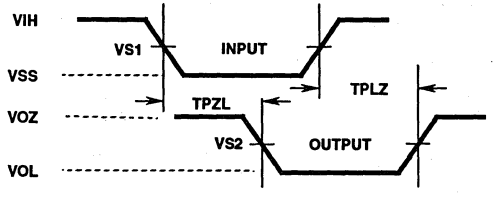
PARAMETER	ACTS	UNITS
VCC	4.50	V
VIH	3.00	V
VIL	0.0	V
VS	1.30	V
GND	0.0	V

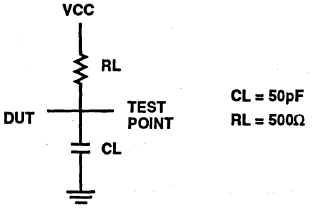
Tri-State High Timing Diagram and Load Circuit





Tri-State Low Timing Diagram and Load Circuit





TRI-STATE VOLTAGE LEVELS

	TPLH	TPHL	TPZL	TPZH	TPHZ	TPLZ
VIH	3V	3V	3V	3V	3V	3V
VS1	1.3V	1.3V	1.3V	1.3V	1.3V	1.3V
VS2	1.3V	1.3V	1.3V	1.3V	80% VCC	20% VCC
VIL	GND	GND	GND	GND	GND	GND

Die Characteristics

DIE DIMENSIONS:
100 x 100 mils
2.54 x 2.54 mm

METALLIZATION:
Type: AlSiCu
Metal 1 Thickness: 7.5kÅ ± 2kÅ
Metal 2 Thickness: 10kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

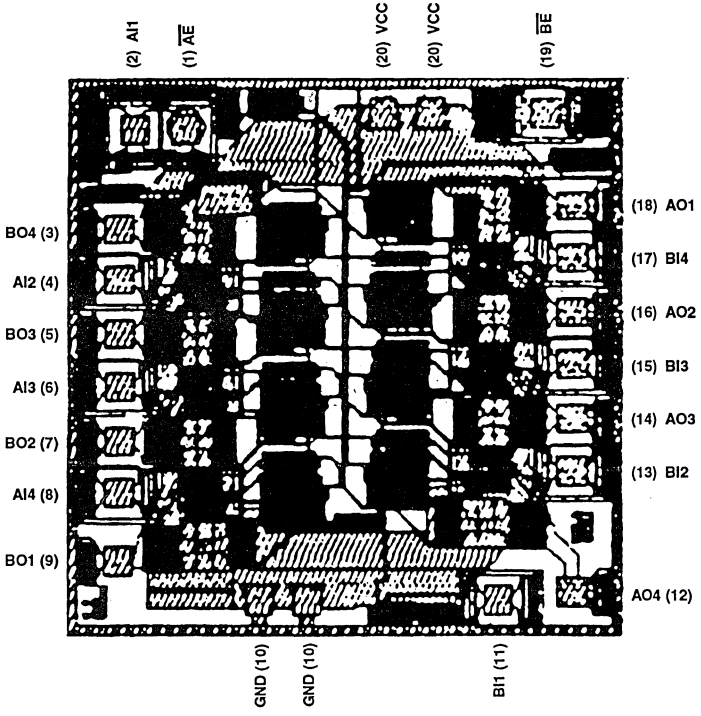
DIE ATTACH:
Material: Silver Glass

WORST CASE CURRENT DENSITY:
< $2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
110µm x 110µm
4.4 mils x 4.4 mils

Metallization Mask Layout

ACTS244MS



HARRIS SEMICONDUCTOR

ACS245MS

Radiation Hardened Octal Non-Inverting Bidirectional Bus Transceiver

December 1992

Features

- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose Up to 1 Mega-RAD (Si)
- Dose Rate Upset >10^{11} RADs(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity <1 x 10^{-11} Errors/Gate Day (Typ)
- Latch Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to ALSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.3 VCC Max
  - VIH = 0.7 VCC Min
  - CMOS Input Compatibility $I_I \leq 5\mu A$ at VOL, VOH

Description

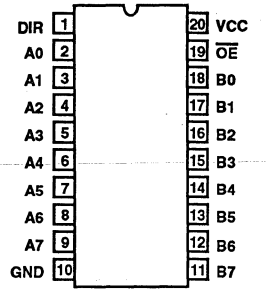
The Harris ACS245MS is a Radiation Hardened octal non-inverting bidirectional bus transceiver intended for two-way asynchronous communication between data busses.

The ACS245MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

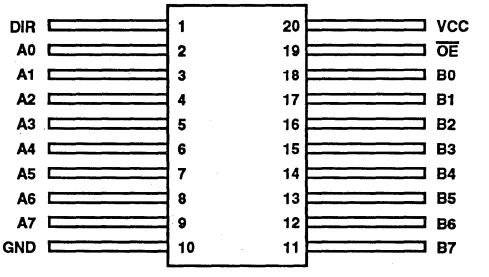
The ACS245MS is supplied in a 20 lead Ceramic flatpack (K suffix) or a Dual-In-Line Ceramic Package (D suffix).

Pinouts

20 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T20, LEAD FINISH C
TOP VIEW



20 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F20, LEAD FINISH C
TOP VIEW



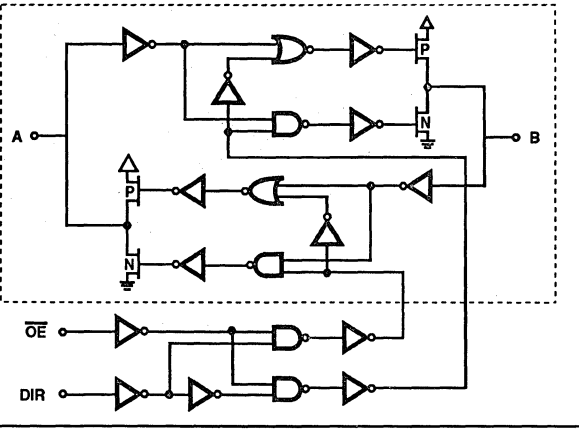
Truth Table

INPUTS		
$\overline{OE}$	DIR	OPERATION
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

H = High Voltage Level
L = Low Voltage Level
X = Immaterial

Functional Diagram

NOTE: (1 of 8)



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3198

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +6.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±50mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
DIC	75°C/W	16°C/W
Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 10ns/V Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 0.3VCC Max.
Input High Voltage (VIH) ..... 0.7VCC to VCC Min.

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	20	µA
			2, 3	+125°C, -55°C	-	400	
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0 (Note 2)	1	+25°C	16	-	mA
			2, 3	+125°C, -55°C	12	-	
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC - 0.4V VIL = 0 (Note 2)	1	+25°C	-16	-	mA
			2, 3	+125°C, -55°C	-12	-	
Output Voltage Low	VOL	VCC = 4.5V, VIH = 4.5V, IOL = 50µA, VIL = 0V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 5.5V, IOL = 50µA, VIL = 0V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 4.5V, IOH = -50µA, VIL = 0V	1, 2, 3	+25°C, +125°C, -55°C	VCC-0.1	-	V
		VCC = 5.5V, VIH = 5.5V, IOH = -50µA, VIL = 0V	1, 2, 3	+25°C, +125°C, -55°C	VCC-0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±1.0	
Tri-State Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	1	+25°C	-	±1.0	µA
			2, 3	+125°C, -55°C	-	±35	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.7VCC, VIL = 0.3VCC (Note 3)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltage referenced to device GND.
2. Force/Measure function may be interchanged.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	8.5	ns
			10, 11	+125°C, -55°C	1	10.0	
	TPHL		9	+25°C	1	8.0	ns
			10, 11	+125°C, -55°C	1	9.0	
Tri-State Test	TPZL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	11.5	ns
			10, 11	+125°C, -55°C	2	15.0	
	TPZH		9	+25°C	2	12.5	ns
			10, 11	+125°C, -55°C	2	15.0	
	TPLZ	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	13.5	ns
			10, 11	+125°C, -55°C	2	14.5	
	TPHZ		9	+25°C	2	14.5	ns
			10, 11	+125°C, -55°C	2	15.0	
Output Transition Time	TTLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	5.0	ns
			10, 11	+125°C, -55°C	1	5.0	
	TTHL		9	+25°C	1	5.0	ns
			10, 11	+125°C, -55°C	1	5.0	

NOTES:

1. All voltage referenced to device GND.
2. Measurements made with CL = 50pF, RL = 500Ω, Input TR = TF = 3ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5V, VIH = 5V, VIL = 0V, f = 1MHz	1	+25°C	Typical 50		pF
			1	+125°C	Typical 50		pF
Input Capacitance	CIN	VCC = 5V, VIH = 5V, VIL = 0V, f = 1MHz	1	+25°C	-	15	pF
			1	+125°C	-	15	pF
Output Capacitance	COUT	VCC = 5V, VIH = 5V, VIL = 0V, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	1 MRAD LIMITS MIN	1 MRAD LIMITS MAX	UNITS
Quiescent Current	ICC	VIN = 5.5V, VIN = VCC or GND	+25°C	-	0.4	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0, (Note 2)	+25°C	12	-	mA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	1 MRAD LIMITS MIN	1 MRAD LIMITS MAX	UNITS
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0, (Note 2)	+25°C	-12	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 4.5V, VIL = 0V, IOL = 50µA	+25°C	-	0.1	V
		VCC = 5.5V, VIH = 5.5V, VIL = 0V, IOL = 50µA		-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 4.5V, VIL = 0V, IOH = -50µA	+25°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 5.5V, VIL = 0V, IOH = -50µA		VCC -0.1	-	V
Tri-State Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	+25°C	-	±35	µA
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±1	µA
Noise Immunity Functional	FN	VCC = 4.5V, VIL = .3 VCC, VIH = .> VCC (Note 3)	+25°C	-	-	-
Propagation Delay	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	1	10.0	ns
	TPHL			1	8.0	ns
Tri-State Test	TPZL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	15.0	ns
	TPZH			2	15.0	ns
	TPLZ			2	14.5	ns
	TPHZ			2	15.0	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	±4µA
IOL/IOH	5	±15% of 0 Hour
IOZL/IOZH	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)	100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test I (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test II (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA	100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)	100%/5004	1, 7, 9	
PDA	100%/5004	1, 7, 9, Deltas	

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/6005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/6005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
2 - 9	1, 10 - 19	-	20	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
-	10	-	1 - 9, 11 - 20	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 1)					
-	10	11 - 18	1, 20	19	2 - 9
DYNAMIC BURN-IN II TEST CONNECTIONS (Note 2)					
-	1, 10	2 - 9	20	19	11 - 18

NOTES:

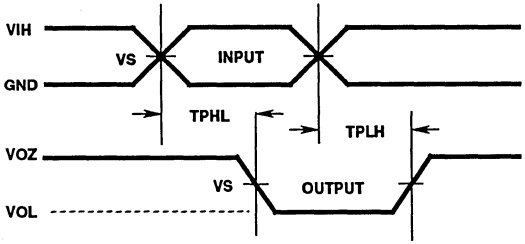
1. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for burn-in.
2. Second dynamic burn-in assures proper stress in both directions. 400 additional hours at life test with a down point; 96 additional hours at production burn-in without a down point.

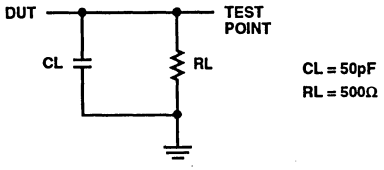
TABLE 9. RADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
-	10	1 - 9, 11 - 20

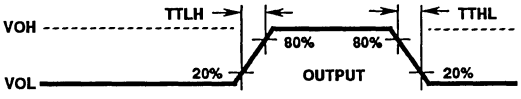
NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5%. Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures.

Propagation Delay Timing Diagram and Load Circuit





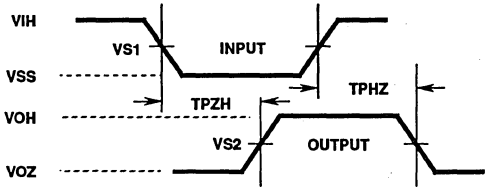
Transition Timing Diagram

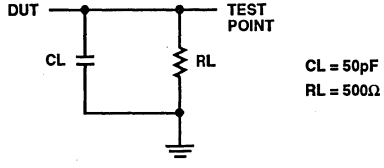


AC VOLTAGE LEVELS

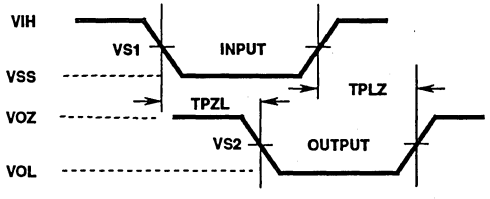
PARAMETER	ACS	UNITS
VCC	4.50	V
VIH	4.50	V
VIL	0.0	V
VS	2.25	V
GND	0	V

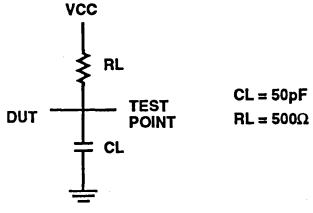
Tri-State High Timing Diagram and Load Circuit





Tri-State Low Timing Diagram and Load Circuit





TRI-STATE VOLTAGE LEVELS

	TPLH	TPHL	TPZL	TPZH	TPHZ	TPLZ
VIH	4.5V	4.5V	4.5V	4.5V	4.5V	4.5V
VS1	2.25V	2.25V	2.25V	2.25V	2.25V	2.25V
VS2	2.25V	2.25V	2.25V	2.25V	80% VCC	20% VCC
VIL	GND	GND	GND	GND	GND	GND

Die Characteristics

DIE DIMENSIONS:
96 x 117 mils
2.44 x 2.97 mm

METALLIZATION:
Type: AlSiCu
Metal 1 Thickness: 7.5kÅ ± 2kÅ
Metal 2 Thickness: 10kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

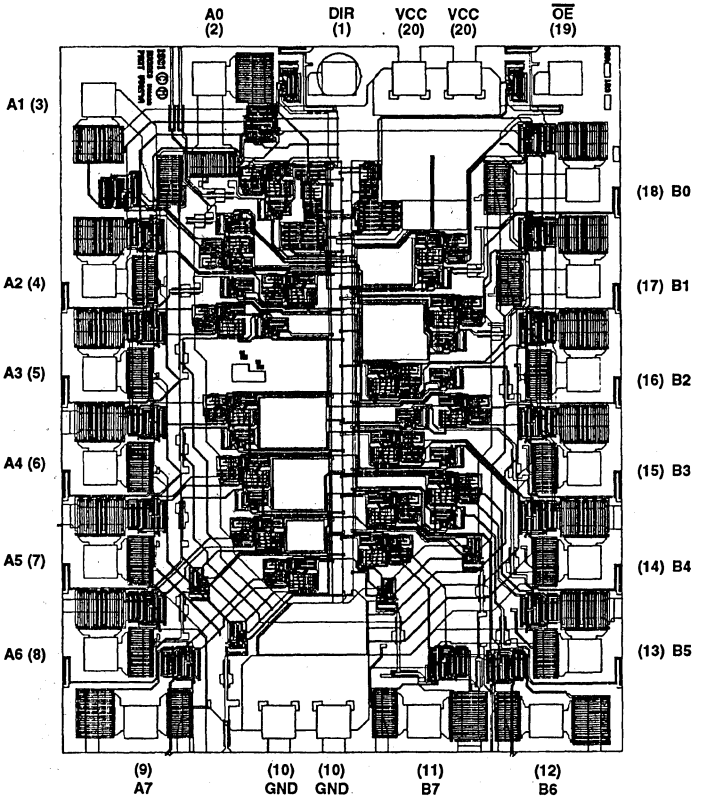
DIE ATTACH:
Material: Silver Glass

WORST CASE CURRENT DENSITY:
< 2.0 x 10^5A/cm^2

BOND PAD SIZE:
110µm x 110µm
4.4 mils x 4.4 mils

Metallization Mask Layout

ACS245MS



HARRIS SEMICONDUCTOR

ACTS245MS

Radiation Hardened Octal Non-Inverting Bidirectional Bus Transceiver

December 1992

Features

- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose Up to 1 Mega-RAD (Si)
- Dose Rate Upset >10^{11} RADs(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity < 1 X 10^{-11} Errors/Gate -day (Typ)
- Latch Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to ALSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
  - CMOS Input Compatibility Ii ≤ 5μA at VOL, VOH

Description

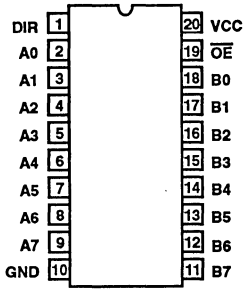
The Harris ACTS245MS is a Radiation Hardened octal non-inverting bidirectional bus transceiver intended for two-way asynchronous communication between data busses .

The ACTS245MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

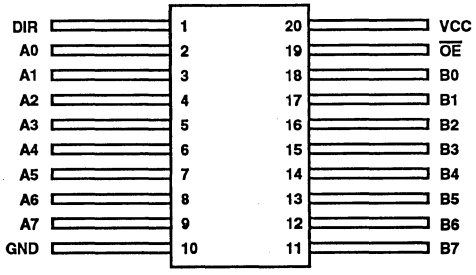
The ACTS245MS is supplied in a 20 lead Ceramic flatpack (K suffix) or a Dual-In-Line Ceramic Package (D suffix).

Pinouts

20 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T20, LEAD FINISH C
TOP VIEW



20 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F20, LEAD FINISH C
TOP VIEW



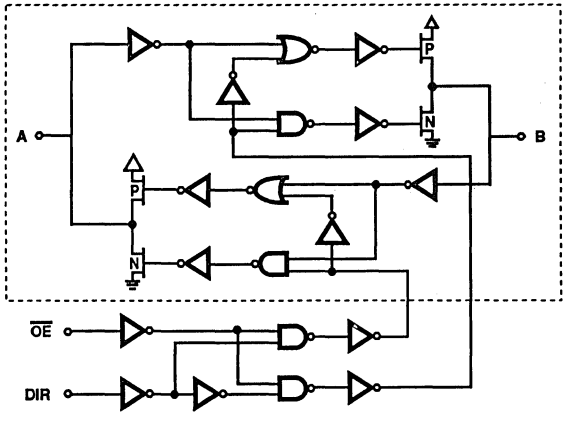
Truth Table

INPUTS		
$\overline{OE}$	DIR	OPERATION
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

H = High Voltage Level
L = Low Voltage Level
X = Immaterial

Functional Diagram

NOTE: (1 of 8)



7 LOGIC

File Number 3188

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +6.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±50mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
DIC	75°C/W	16°C/W
Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 10ns/V Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... VCC to VCC/2

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	20	µA
			2, 3	+125°C, -55°C	-	400	
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0 (Note 2)	1	+25°C	16	-	mA
			2, 3	+125°C, -55°C	12	-	
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC - 0.4V VIL = 0 (Note 2)	1	+25°C	-16	-	mA
			2, 3	+125°C, -55°C	-12	-	
Output Voltage Low	VOL	VCC = 4.5V, VIH = 4.5V, IOL = 50µA, VIL = 0V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 5.5V, IOL = 50µA, VIL = 0V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 4.5V, IOH = -50µA, VIL = 0V	1, 2, 3	+25°C, +125°C, -55°C	VCC-0.1	-	V
		VCC = 5.5V, VIH = 5.5V, IOH = -50µA, VIL = 0V	1, 2, 3	+25°C, +125°C, -55°C	VCC-0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±1.0	
Tri-State Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	1	+25°C	-	±1.0	µA
			2, 3	+125°C, -55°C	-	±35	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = VCC/2, VIL = 0.8V (Note 3)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltage referenced to device GND.
2. Force/Measure function may be interchanged.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPLH	VCC = 4.5V, VIH = 3V, VIL = 0V	9	+25°C	1	9.0	ns
			10, 11	+125°C, -55°C	1	10.0	
	TPHL		9	+25°C	1	9.5	ns
			10, 11	+125°C, -55°C	1	10.0	
Tri-State Test	TPZL	VCC = 4.5V, VIH = 3V, VIL = 0	9	+25°C	2	15.5	ns
			10, 11	+125°C, -55°C	2	18.0	
	TPZH		9	+25°C	2	13.5	ns
			10, 11	+125°C, -55°C	2	13.5	
	TPLZ	VCC = 4.5V, VIH = 3V, VIL = 0	9	+25°C	2	16.0	ns
			10, 11	+125°C, -55°C	2	16.0	
	TPHZ		9	+25°C	2	17.0	ns
			10, 11	+125°C, -55°C	2	17.0	
Output Transition Time	TTLH	VCC = 4.5V, VIH = 3V, VIL = 0	9	+25°C	1	5.0	ns
			10, 11	+125°C, -55°C	1	5.0	
	TTHL		9	+25°C	1	5.0	ns
			10, 11	+125°C, -55°C	1	5.0	

NOTES:

1. All voltage referenced to device GND.
2. Measurements made with CL = 50pF, RL = 500Ω, Input TR= TF = 3ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5V, VIH = 5V, VIL = 0V, f = 1MHz	1	+25°C	Typical 40		pF
			1	+125°C	Typical 40		pF
Input Capacitance	CIN	VCC = 5V, VIH = 5V, VIL = 0V, f = 1MHz	1	+25°C	-	15	pF
			1	+125°C	-	15	pF
Output Capacitance	COUT	VCC = 5V, VIH = 5V, VIL = 0V, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	1 MRAD LIMITS MIN	1 MRAD LIMITS MAX	UNITS
Quiescent Current	ICC	VIN = 5.5V, VIN = VCC or GND	+25°C	-	0.4	mA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	1 MRAD LIMITS		UNITS
				MIN	MAX	
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0, (Note 2)	+25°C	12	-	mA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0, (Note 2)	+25°C	-12	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 4.5V, VIL = 0V, IOL = 50µA	+25°C	-	0.1	V
		VCC = 5.5V, VIH = 5.5V, VIL = 0V, IOL = 50µA		-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 4.5V, VIL = 0V, IOH = -50µA	+25°C	VCC-0.1	-	V
		VCC = 5.5V, VIH = 5.5V, VIL = 0V, IOH = -50µA		VCC-0.1	-	V
Tri-State Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	+25°C	-	±35	µA
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±1	µA
Noise Immunity Functional	FN	VCC = 4.5V, VIL = 0.8V, VIH = VCC/2 (Note 3)	+25°C	-	-	-
Propagation Delay	TPLH	VCC = 4.5V, VIH = 3V, VIL = 0V	+25°C	1	10.0	ns
	TPHL			1	10.0	ns
Tri-State Test	TPZL	VCC = 4.5V, VIH = 3V, VIL = 0V	+25°C	2	18.0	ns
	TPZH			2	13.5	ns
	TPLZ			2	16.0	ns
	TPHZ			2	17.0	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	±4µA
IOL/IOH	5	±15% of 0 Hour
IOZL/IOZH	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
PDA	100%/5004	1, 7, 9, Deltas	

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/6005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/6005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
2 - 9	1, 10 - 19	-	20	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
-	10	-	1 - 9, 11 - 20	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 1)					
-	10	11 - 18	1, 20	19	2 - 9
DYNAMIC BURN-IN II TEST CONNECTIONS (Note 2)					
-	1, 10	2 - 9	20	19	11 - 18

NOTES:

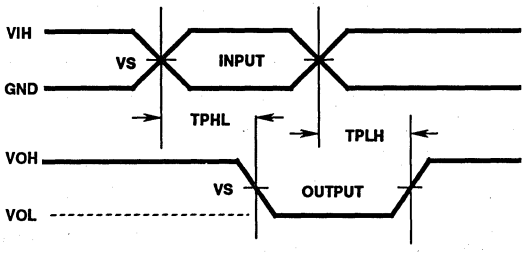
1. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for burn-in.
2. Second dynamic burn-in assures proper stress in both directions. 400 additional hours at life test with a down point; 96 additional hours at production burn-in without a down point.

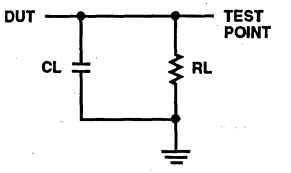
TABLE 9. RADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
-	10	1 - 9, 11 - 20

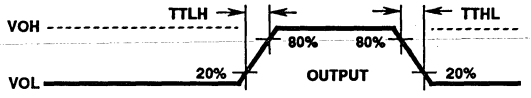
NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures.

Propagation Delay Timing Diagram and Load Circuit





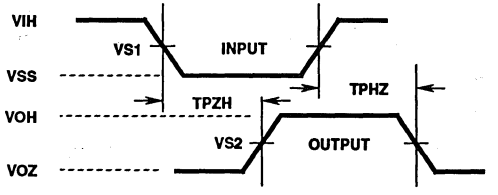
Transition Timing Diagram

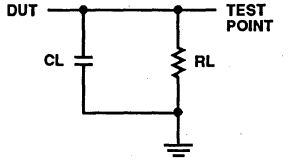


AC VOLTAGE LEVELS

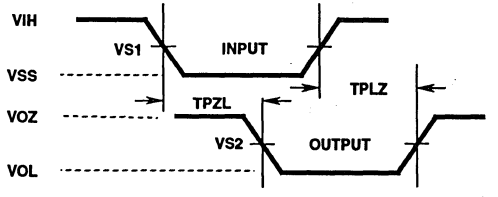
PARAMETER	ACTS	UNITS
VCC	4.50	V
VIH	3.00	V
VIL	0.0	V
VS	1.30	V
GND	0.0	V

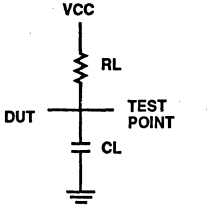
Tri-State High Timing Diagram and Load Circuit





Tri-State Low Timing Diagram and Load Circuit





TRI-STATE VOLTAGE LEVELS

	TPLH	TPHL	TPZL	TPZH	TPHZ	TPLZ
VIH	3V	3V	3V	3V	3V	3V
VS1	1.3V	1.3V	1.3V	1.3V	1.3V	1.3V
VS2	1.3V	1.3V	1.3V	1.3V	80% VCC	20% VCC
VIL	GND	GND	GND	GND	GND	GND

Die Characteristics

DIE DIMENSIONS:
96 x 117 mils
2.44 x 2.97 mm

METALLIZATION:
Type: AlSiCu
Metal 1 Thickness: 7.5kÅ ± 2kÅ
Metal 2 Thickness: 10kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

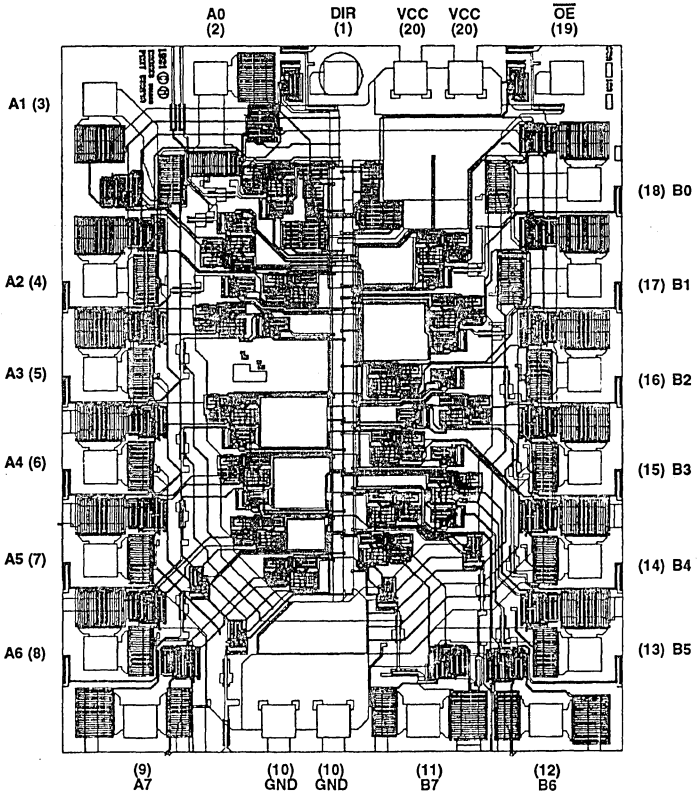
DIE ATTACH:
Material: Silver Glass

WORST CASE CURRENT DENSITY:
$< 2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
110µm x 110µm
4.4 mils x 4.4 mils

Metallization Mask Layout

ACTS245MS



HARRIS SEMICONDUCTOR

ACS630MS

Radiation Hardened EDAC (Error Detection and Correction Circuit)

December 1992

Features

- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose Up to 1 Mega-RAD (Si)
- Dose Rate Upset >10^{11} Rads(Si)/s, 20ns Pulse
- Cosmic Ray Upset Immunity (1 x 10^{-11}) Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.3 VCC Max
  - VIH = 0.7 VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH
- Fast Processing Time
  - Write Cycle: Generates Check Word in 20ns (Typ)
  - Read Cycle: Flags Errors in 10ns (Typ)

Description

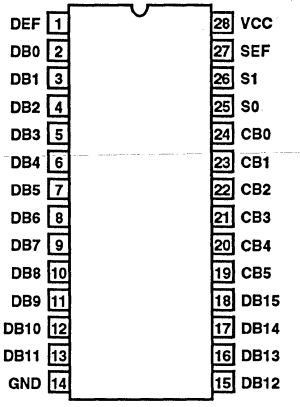
The Harris ACS630MS is a Radiation Hardened 16-bit parallel error detection and correction circuit. It uses a modified Hamming code to generate a 6-bit check word from each 16-bit data word. The check word is stored with the data word during a memory write cycle, during a memory read cycle a 22-bit word is taken form memory and checked for errors. Single bit errors in the data words are flagged and corrected. Single bit errors in check words are flagged but not corrected. The position of the incorrect bit is pinpointed, in both cases, by the 6-bit error syndrome code which is output during the error correction cycle.

The ACS630MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family .

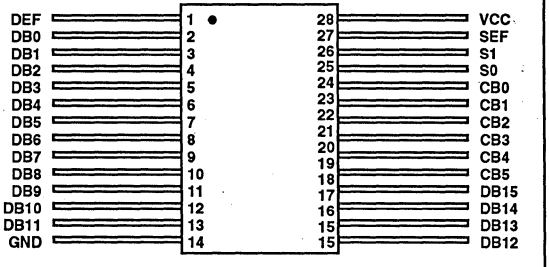
The ACS630MS is supplied in a 28 lead Ceramic flatpack (K suffix) or a Ceramic Dual-In-Line Package (D suffix).

Pinouts

28 PIN CERAMIC DUAL-IN-LINE
MIL-STD-183S DESIGNATOR CDIP2 - T28, LEAD FINISH C
TOP VIEW



28 PIN CERAMIC FLAT PACK
MIL-STD-183S DESIGNATOR CDFP3-F28, LEAD FINISH C
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3199

Function Tables

Control Functions

MEMORY CYCLE	CONTROL		EDAC FUNCTION	DATA I/O	CHECKWORD	ERROR FLAGS	
	S1	S0				SEF	DEF
WRITE	Low	Low	Generates Checkword	Input Data	Output Checkword	Low	Low
READ	Low	High	Read Data and Check-word	Input Data	Input Checkword	Low	Low
READ	High	High	Latch and Flag Error	Latch Data	Latch Checkword	Enabled	Enabled
READ	High	Low	Correct Data Word and Generate Syndrome Bits	Output Corrected Data	Output Syndrome Bits	Enabled	Enabled

Check Word Generation

CHECKWORD BIT	16-BIT DATA WORD															
	0	1	2	3	4	5	6	7	8	9	10	11	2	13	14	15
CB0	X	X		X	X				X	X	X			X		
CB1	X		X	X		X	X		X			X			X	
CB2		X	X		X	X		X		X			X			X
CB3	X	X	X				X	X			X	X	X			
CB4				X	X	X	X	X						X	X	X
CB5									X	X	X	X	X	X	X	X

NOTE: The six check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit

Error Syndrome Codes

SYNDROME ERROR CODE	ERROR LOCATIONS																						NO ERROR
	DB																CB						
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	
CB0	L	L	H	L	L	H	H	H	L	L	L	H	H	L	H	H	L	H	H	H	H	H	H
CB1	L	H	L	L	H	L	L	H	L	H	H	L	H	H	L	H	H	L	H	H	H	H	H
CB2	H	L	L	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	L	H	H	H	H
CB3	L	L	L	H	H	H	L	L	H	H	L	L	L	H	H	H	H	H	H	L	H	H	H
CB4	H	H	H	L	L	L	L	L	H	H	H	H	H	L	L	L	H	H	H	H	L	H	H
CB5	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	H	H	H	H	H	L	H

Error Functions

TOTAL NUMBER OF ERRORS		ERROR FLAGS		DATA CORRECTION
16-BIT DATA	6-BIT CHECKWORD	SEF	DEF	
0	0	Low	Low	Not Applicable
1	0	High	Low	Correction
0	1	High	Low	Correction
1	1	High	High	Interrupt
2	0	High	High	Interrupt
0	2	High	High	Interrupt

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +6.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output 50mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
DIC	75°C/W	16°C/W
Flatpack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at VCC = 4.5V (TR, TF) ..... 10ns/V Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 30% of VCC
Input High Voltage (VIH) ..... 70% of VCC to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	150	µA
			2, 3	+125°C, -55°C	-	3	mA
Output Current (Sink)	IOL1	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V (Note 2)	1	+25°C	16	-	mA
			2, 3	+125°C, -55°C	12	-	mA
Output Current (Source)	IOH1	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V (Note 2)	1	+25°C	-16	-	mA
			2, 3	+125°C, -55°C	-12	-	mA
DEF, SEF Output Current (Source)	IOL2	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V (Note 2)	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
DEF, SEF Output Current (Sink)	IOH2	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V (Note 2)	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC - 0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC - 0.1	-	V
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Tri-State Output Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	1	+25°C	-	±1	µA
			2, 3	+125°C, -55°C	-	±35	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V (Note 3)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. Force/Measure functions may be interchanged.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay DB to CB	TPHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	21	ns
			10, 11	+125°C, -55°C	1	23.5	ns
	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	20	ns
			10, 11	+125°C, -55°C	1	24.5	ns
Propagation Delay S1 to DEF	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	13	ns
			10, 11	+125°C, -55°C	1	15.5	ns
Propagation Delay S1 to SEF	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	13	ns
			10, 11	+125°C, -55°C	1	15.5	ns
Propagation Delay S0 to DB/CB	TPHZ	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	21	ns
			10, 11	+125°C, -55°C	1	21.5	ns
	TPLZ	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	18	ns
			10, 11	+125°C, -55°C	1	20.5	ns
Propagation Delay S0 to DB/CB	TPZH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	18	ns
			10, 11	+125°C, -55°C	1	20.5	ns
	TPZL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	15	ns
			10, 11	+125°C, -55°C	1	16.5	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Operation Current DB to CB	IOPER	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25°C	Typical 4.25		mA
				+125°C, -55°C	Typical 4.75		mA
Input Capacitance	CIN	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25°C	-	10	pF
				+125°C, -55°C	-	10	pF
Output Capacitance	COUT	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25°C	-	10	pF
				+125°C, -55°C	-	10	pF

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	1MRAD LIMITS MIN	1MRAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	3	mA
Output Current (Sink)	IOL1	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0	+25°C	12	-	mA
Output Current (Source)	IOH1	VCC = VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0	+25°C	-12	-	mA
DEF, SEF Output Current (Sink)	IOL2	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0	+25°C	4	-	mA
DEF, SEF Output Current (Source)	IOH2	VCC = VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0	+25°C	-4	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOL = 50µA	+25°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, VIL = 1.65V, IOL = 50µA	+25°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOH = -50µA	+25°C	VCC-0.1	-	V
		VCC = 5.5V, VIH = 3.85V, VIL = 1.65V, IOH = -50µA	+25°C	VCC-0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	µA
Tri-State Output Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	+25°C	-	±35	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V (Note 3)	+25°C	-	-	-
Propagation Delay DB to CB	TPHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	1	23.5	ns
	TPLH		+25°C	1	24.5	ns
Propagation Delay S1 to DEF	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	1	15.5	ns
Propagation Delay S1 to SEF	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	1	15.5	ns
Propagation Delay S0 to DB/CB	TPHZ	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	1	21.5	ns
	TPLZ		+25°C	1	19.5	ns
Propagation Delay S0 to DB/CB	TPZH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	1	20.5	ns
	TPZL		+25°C	1	16.5	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	±30µA
IOL/IOH	5	±15%
IOZ	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE: 1. Except FN Test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
-	2 - 18, 25, 26	1, 27, 19 - 24	28	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
-	14	1, 27	2 - 13, 15 - 26, 28	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 2)					
-	14, 25, 26	1, 19 - 24, 27	4 - 13, 15 - 26, 28	3, 17	2, 18

NOTES:

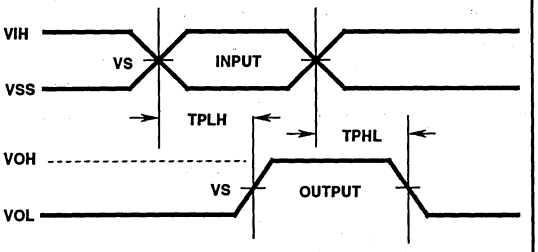
1. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for burn-in.
2. Second dynamic burn-in assures proper stress in both directions. 400 additional hours at life test with a down point; 96 additional hours at production burn-in without a down point.

TABLE 9. RADIATION TEST CONNECTIONS

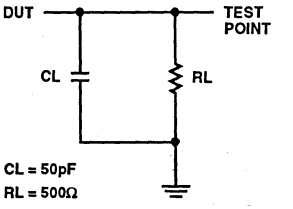
OPEN	GROUND	VCC = 5V ± 0.5V
-	14	2 - 13, 15 - 26, 28

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5%. Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures.

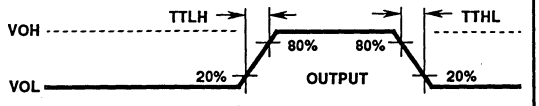
Propagation Delay Timing Diagram



Propagation Delay Load Circuit



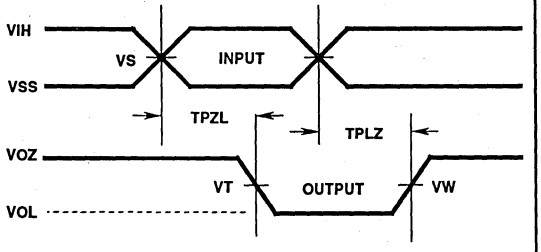
Transition Timing Diagrams



VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

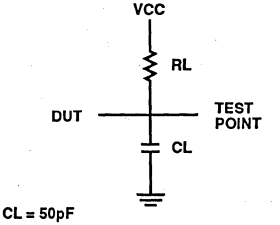
Tri-State Low Timing Diagrams



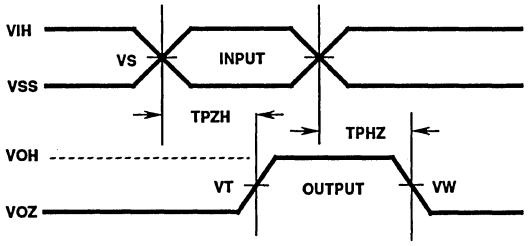
TRI-STATE LOW VOLTAGE LEVELS

PARAMETER	ACS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	0.2	VCC
GND	0	V

Tri-State Low Load Circuit



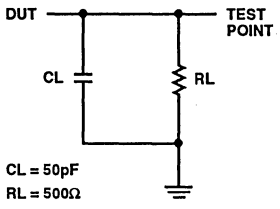
Tri-State High Timing Diagrams



TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	ACS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	0.8	VCC
GND	0	V

Tri-State High Load Circuit



7 LOGIC

Die Characteristics

DIE DIMENSIONS:
171 x 159 (Mils)
4340 x 4040 (mm)

METALLIZATION:
Type: AlSiCu
Metal 1 Thickness: 7.5kÅ ± 2kÅ
Metal 2 Thickness: 10kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

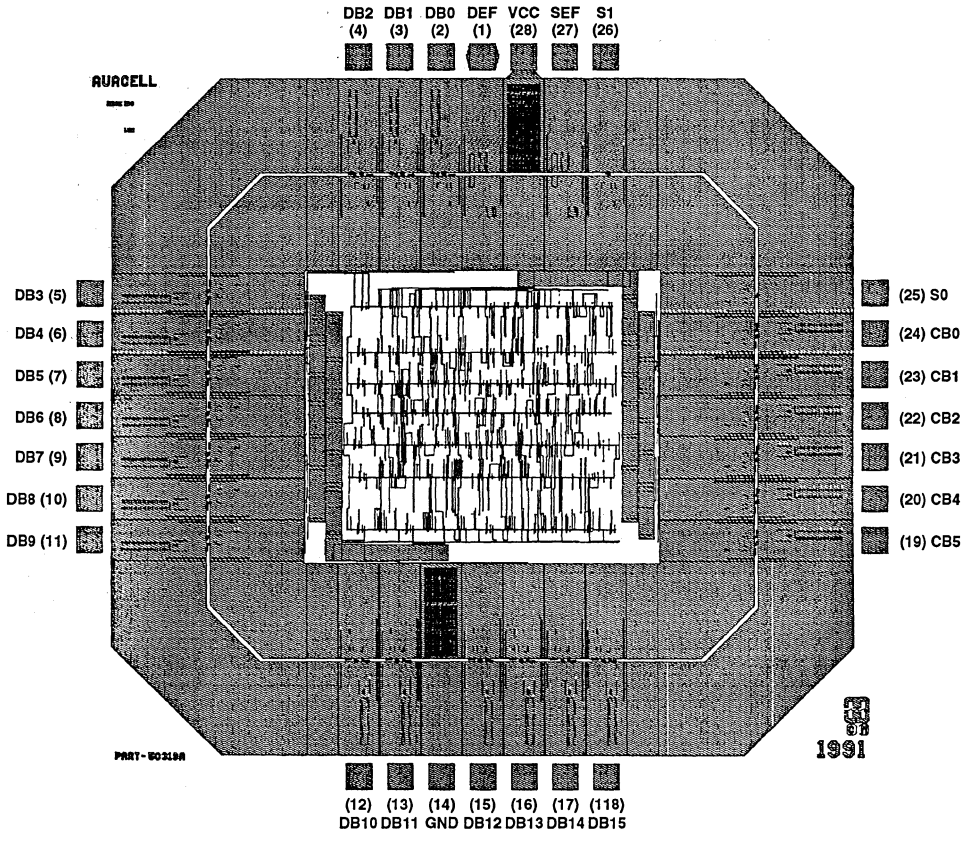
DIE ATTACH:
Material: Silver Glass

WORST CASE CURRENT DENSITY:
< 2.0 x 10^5A/cm^2

BOND PAD SIZE:
110µm x 110µm
4.4 x 4.4 (Mils)

Metallization Mask Layout

ACS630MS



HARRIS SEMICONDUCTOR

ACTS630MS

Radiation Hardened EDAC (Error Detection and Correction)

December 1992

Features

- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose Up to 1 Mega-RAD (Si)
- Dose Rate Upset >10^{11} RAD(Si)/s, 20ns Pulse
- SEU Rate < 10^{-11} Errors/Bit-Day
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5µA at VOL, VOH
- Fast Processing Time
  - Write Cycle: Generates Check Word in 20ns (Typ)
  - Read Cycle: Flags Errors in 10ns (Typ)

Description

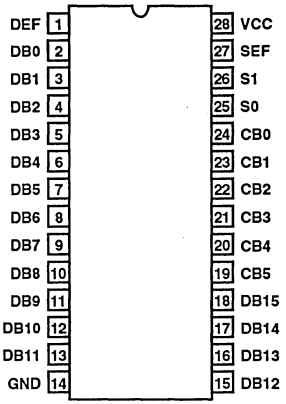
The Harris ACTS630MS is a Radiation Hardened 16-bit parallel error detection and correction circuit. It uses a modified Hamming code to generate a 6-bit check word from each 16-bit data word. The check word is stored with the data word during a memory write cycle; during a memory read cycle a 22-bit word is taken form memory and checked for errors. Single bit errors in the data words are flagged and corrected. Single bit errors in check words are flagged but not corrected. The position of the incorrect bit is pinpointed, in both cases, by the 6-bit error syndrome code which is output during the error correction cycle.

The ACTS630MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

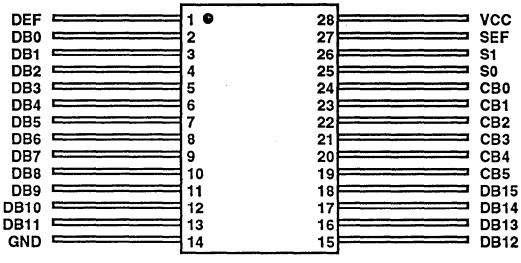
The ACTS630MS is supplied in a 28 lead Ceramic flatpack (K suffix) or a 28 Lead Ceramic Dual-In-Line Package (D suffix).

Pinouts

28 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP-T28, LEAD FINISH C
TOP VIEW



28 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F28, LEAD FINISH C
TOP VIEW



7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3204

Function Tables

Control Functions

MEMORY CYCLE	CONTROL		EDAC FUNCTION	DATA I/O	CHECKWORD	ERROR FLAGS	
	S1	S0				SEF	DEF
WRITE	Low	Low	Generates Checkword	Input Data	Output Checkword	Low	Low
READ	Low	High	Read Data and Check-word	Input Data	Input Checkword	Low	Low
READ	High	High	Latch and Flag Error	Latch Data	Latch Checkword	Enabled	Enabled
READ	High	Low	Correct Data Word and Generate Syndrome Bits	Output Corrected Data	Output Syndrome Bits	Enabled	Enabled

Check Word Generation

	16-BIT DATA WORD															
CHECKWORD BIT	0	1	2	3	4	5	6	7	8	9	10	11	2	13	14	15
CB0	X	X		X	X				X	X	X			X		
CB1	X		X	X		X	X		X			X			X	
CB2		X	X		X	X		X		X			X			X
CB3	X	X	X				X	X			X	X	X			
CB4				X	X	X	X	X						X	X	X
CB5									X	X	X	X	X	X	X	X

NOTE: The six check bits are parity bits derived from the matrix of data bits as indicated by "x" for each bit

Error Syndrome Codes

SYNDROME ERROR CODE	ERROR LOCATIONS																					
	DB																CB						NO ERROR
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	
CB0	L	L	H	L	L	H	H	H	L	L	L	H	H	L	H	H	L	H	H	H	H	H	H
CB1	L	H	L	L	H	L	L	H	L	H	H	L	H	H	L	H	H	L	H	H	H	H	H
CB2	H	L	L	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	L	H	H	H	H
CB3	L	L	L	H	H	H	L	L	H	H	L	L	L	H	H	H	H	H	H	L	H	H	H
CB4	H	H	H	L	L	L	L	L	H	H	H	H	H	L	L	L	H	H	H	H	L	H	H
CB5	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	H	H	H	H	H	L	H

Error Functions

TOTAL NUMBER OF ERRORS		ERROR FLAGS		
16-BIT DATA	6-BIT CHECKWORD	SEF	DEF	DATA CORRECTION
0	0	Low	Low	Not Applicable
1	0	High	Low	Correction
0	1	High	Low	Correction
1	1	High	High	Interrupt
2	0	High	High	Interrupt
0	2	High	High	Interrupt

Absolute Maximum Ratings

Supply Voltage (VCC) ..... -0.5V to +6.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
DIC	75°C/W	16°C/W
Flatpack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC) ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 500ns Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	150	µA
			2, 3	+125°C, -55°C	-	3	µA
Output Current (Sink)	IOL1	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V (Note 2)	1	+25°C	16	-	mA
			2, 3	+125°C, -55°C	12	-	mA
Output Current (Source)	IOH1	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V (Note 2)	1	+25°C	-16	-	mA
			2, 3	+125°C, -55°C	-12	-	mA
DEF, SEF Output Current (Sink)	IOL2	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V (Note 2)	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
DEF, SEF Output Current (Source)	IOH2	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V (Note 2)	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC - 0.1	-	V
		VCC = 5.5V, VIH =2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC - 0.1	-	V
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Tri-State Output Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	1	+25°C	-1	+1	µA
			2, 3	+125°C, -55°C	-35	+35	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 3)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:
1. All voltages reference to device GND.
2. Force/Measure functions may be interchanged.
3. Per functional tests, VO ≥ 3.0V is recognized as a logic "1", and VO = 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay DB to CB	TPHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	21	ns
			10, 11	+125°C, -55°C	1	23.5	ns
	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	20	ns
			10, 11	+125°C, -55°C	1	24.5	ns
Propagation Delay S1 to DEF	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	13	ns
			10, 11	+125°C, -55°C	1	15.5	ns
Propagation Delay S1 to SEF	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	13	ns
			10, 11	+125°C, -55°C	1	15.5	ns
Propagation Delay S0 to DB/CB	TPHZ	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	21	ns
			10, 11	+125°C, -55°C	1	21.5	ns
	TPLZ	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	18	ns
			10, 11	+125°C, -55°C	1	20.5	ns
Propagation Delay S0 to DB/CB	TPZH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	18	ns
			10, 11	+125°C, -55°C	1	20.5	ns
	TPZL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	1	15	ns
			10, 11	+125°C, -55°C	1	16.5	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Operation Current DB to CB	IOPER	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25°C	Typical 4.25		mA
				+125°C	Typical 4.75		mA
Input Capacitance	CIN	VCC = 5.0V, f = 1MHz	1	+25°C	-	10	pF
				+125°C	-	10	pF
Output Capacitance	COUT	VCC = 5.0V, f = 1MHz	1	+25°C	-	20	pF
				+125°C	-	20	pF
Setup S1	TSU	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	20	-	ns
			1	+125°C	20	-	ns
Hold S1	TH	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	10	-	ns
			1	+125°C	10	-	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	1M LIMITS MIN	1M LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	3	mA
Output Current (Sink)	IOL1	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0	+25°C	12	-	mA
Output Current (Source)	IOH1	VCC = VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0	+25°C	-12	-	mA
DEF, SEF Output Current (Sink)	IOL2	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0	+25°C	4	-	mA
DEF, SEF Output Current (Source)	IOH2	VCC = VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0	+25°C	-4	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V, IOL = 50µA	+25°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, VIL = 0.8V, IOL = 50µA	+25°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V, IOH = -50µA	+25°C	VCC - 0.1	-	V
		VCC = 5.5V, VIH = 2.75V, VIL = 0.8V, IOH = -50µA	+25°C	VCC - 0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	µA
Tri-State Output Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	+25°C	-35	+35	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V, Note 2	+25°C	-	-	-
Propagation Delay DB to CB	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	1	23.5	ns
	TPLH		+25°C	1	24.5	ns
Propagation Delay S1 to DEF	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	1	15.5	ns
Propagation Delay S1 to SEF	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	1	15.5	ns
Propagation Delay S0 to DB/CB	TPHZ	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	1	21.5	ns
	TPLZ		+25°C	1	19.5	ns
Propagation Delay S0 to DB/CB	TPZH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	1	20.5	ns
	TPZL		+25°C	1	16.5	ns

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUB-GROUP	DELTA LIMIT
ICC	5	30µA
IOL/IOH	5	-15%
IOZ	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A Testing in accordance with MIL-STD 883 Method 5005 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. .Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

				OSCILLATOR	
OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
-	2 - 18, 25, 26	1, 27, 19 - 24	28	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
-	14	1, 27	2 - 13, 15 - 26, 28	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	14, 25, 26	1, 19 - 24, 27	4 - 13, 15 - 26, 28	3, 17	2, 18

NOTES:

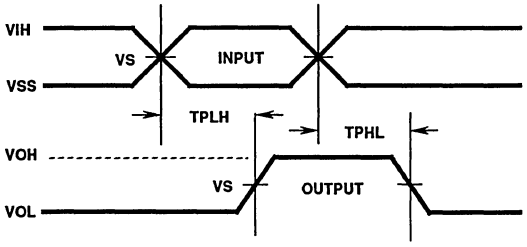
1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680Ω ± 5% for dynamic burn-in

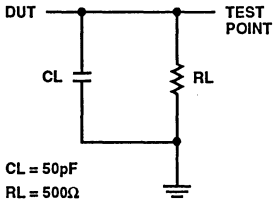
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V	1/2 VCC = 3V ± 0.5V
-	14	2 - 13, 15 - 26, 28	1, 27

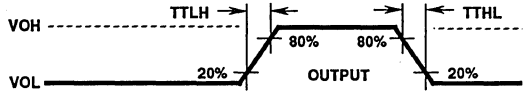
NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

Propagation Delay Timing Diagram and Load Circuit





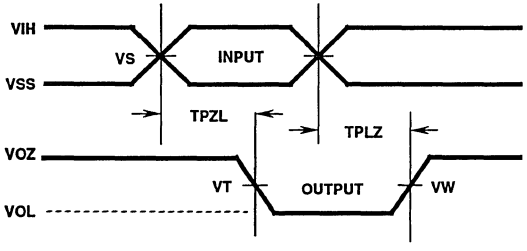
Transition Timing Diagram

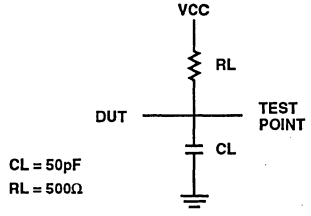


PROPAGATION DELAY VOLTAGE LEVELS

PARAMETER	ACTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Tri-State Low Timing Diagram and Load Circuit

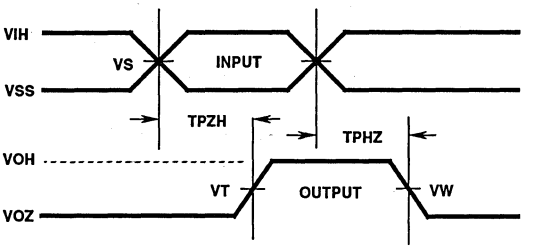


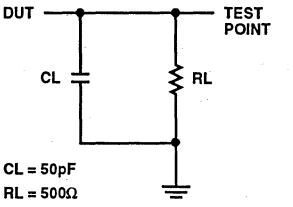


TRI-STATE LOW VOLTAGE LEVELS

PARAMETER	ACTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	0.90	V
VOZ	Approx. 4.5	V
GND	0	V

Tri-State High Timing Diagram and Load Circuit

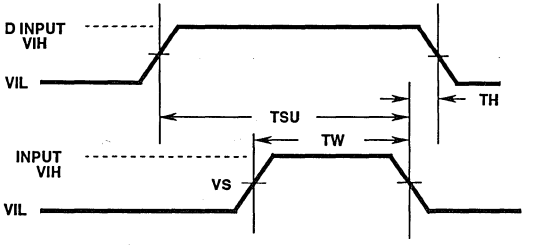




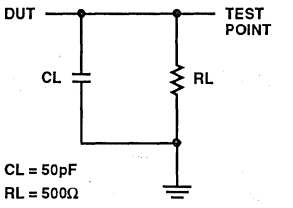
TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	ACTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	3.60	V
GND	0	V

Pulse Width, Setup, Hold Timing Diagram and Load Circuit



TH = Hold Time
TSU = Setup Time
TW = Pulse Width



PULSE WIDTH, SETUP, HOLD VOLTAGE LEVELS

PARAMETER	ACTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
171 x 159 mils
6.7 x 6.3µm

METALLIZATION:
Type: Al/Si/Cu
Metal 1 Thickness: 7.5kÅ ± 2kÅ
Metal 2 Thickness: 10kÅ ± 2kÅ

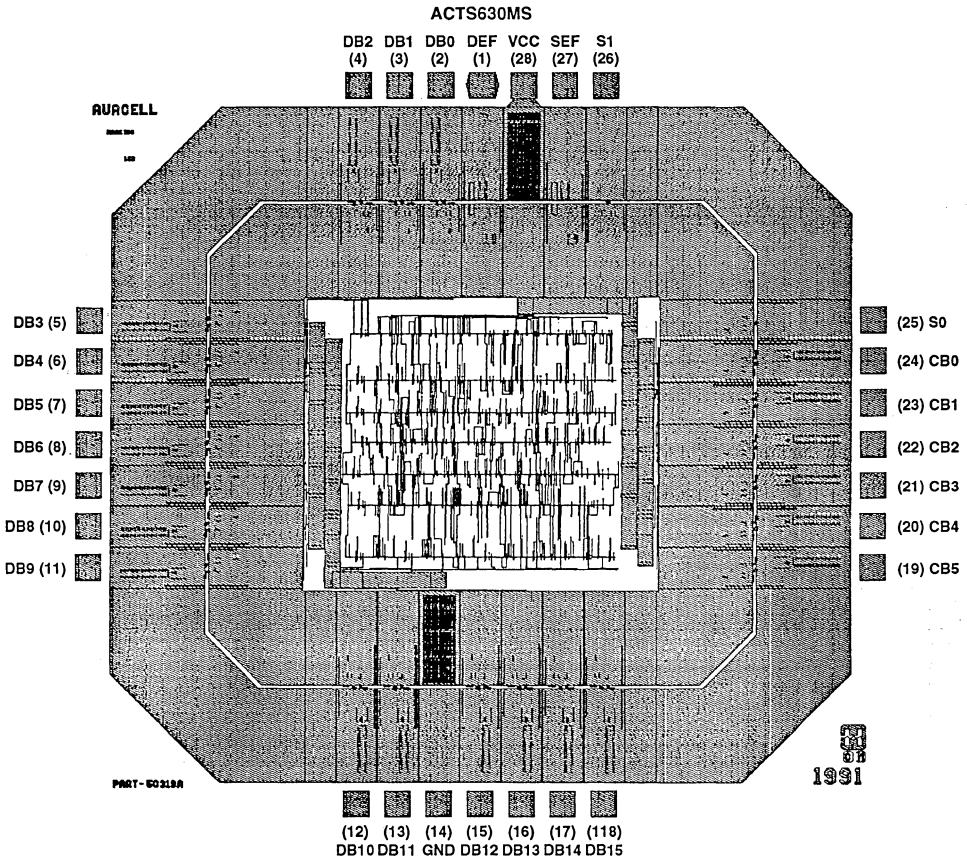
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Silver Glass

WORST CASE CURRENT DENSITY:
$< 2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
110µm x 110µm
4.3 x 4.3 mils

Metallization Mask Layout



HCS/HCTS MS Screening

Wafer Lot Acceptance	(All Lots)	Method 5007 (Includes SEM)
Radiation Verification	(EachWafer)	Method 1019, 200K or 1MRAD (SI), 4 Samples/Wafer, 0 Rejects
Nondestructive Bond Pull	100%	Method 2023
Internal Visual Inspection	100%	Modified Method 2010 (Note 4)
Temperature Cycling	100%	Method 1010 Condition C (-65°C to +150°C)
Constant Acceleration	100%	
PIND Testing	100%	
External Visual Inspection	100%	
Serialization	100%	
Initial Electrical Test	100%	
Static Burn-In I	100%	Method 1015, 24 Hours, at +125°C Minimum
Interim Electrical Test I	100%	(Note 1)
Static Burn-In II	100%	Method 1015, 24 Hours, at +125°C Minimum
Interim Electrical Test II	100%	(Note 1)
Dynamic Burn-In	100%	Method 1015, 240 Hours, at +125°C or Equivalent or 180 Hours, at +135°C
Interim Electrical Test III	100%	(Note 1)
Final Electrical Test	100%	
Fine and Gross Seal	100%	Method 1014
Radiographics	100%	Method 2012 (2 Views)
External Visual	100%	Method 2009
Group A (All Tests)		Method 5005 (Class S)
Group B (Optional)		Method 5005 (Class S) (Note 2)
Group D (Optional)		Method 5005 (Class S) (Note 2)
CSI and/or GSI (Optional)		(Note 2)
Data Package Generation		(Note 3)

NOTES:

1. Failure from interim electrical tests I and II are combined for determining PDA (PDA = 5% for subgroups 1, 7, 9 and delta failures combined, PDA = 3% for subgroup 7 failures). Interim electrical tests III PDA (PDA = 5% for subgroups 1, 7, 9 and delta failures combined, PDA = 3% for subgroup 7 failures.
2. These steps are optional, and should be listed on the purchase order if required.
3. Data Package Contents:
   Cover Sheet (P.O. #, Customer #, Lot Data Code, Harris #, Lot #, Quantity.
   Certificate of Conformance (as found on shipper).
   Lot Serial Number Sheet (Good Unit(s), Serial # and Lot #).
   Variables Data (All Read, Record and Delata Operations).
   Group A Attributes Data Summary.
   Wafer Lot Acceptance Report (Method 5007) to include SEM photos. NOTE: SEM photos to include % of step coverage.
   X-Ray Report and file(s), including parameter measurements.
   GAMMA Radiation Report with initial shipment of devices from the same wafer lot; Containing a cover page, Disposition, Rad Dose, Lot #, Test Package, Spec #(s), Test Equipment, etc.
   Irradiation Read and Record data will be on file at Harris.
4. Visual Inspection for class S is performed to Mil-Std-883S, Method 2010, Condition a with the following modifications: SOS Technology, Semicircular cracks not in an active area which start and end at the pellet edge are acceptable.
5. Table 5 Delta limit values without a "+" or "-" sign indicate the value is positive; negative deltas of any magnitude will not be counted as failures.

HARRIS SEMICONDUCTOR

HCS00MS

Radiation Hardened Quad 2-Input NAND Gate

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD (Si)
- Dose Rate Upset >10^{10} Rad(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity < 2 x 10^{-9} Errors/Gate Day (Typ)
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

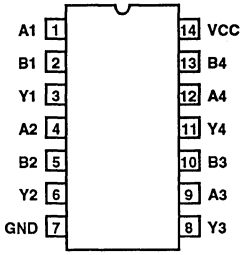
The Harris HCS00MS is a Radiation Hardened Quad 2-Input NAND Gate. A high on both inputs forces the output to a Low state.

The HCS00MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

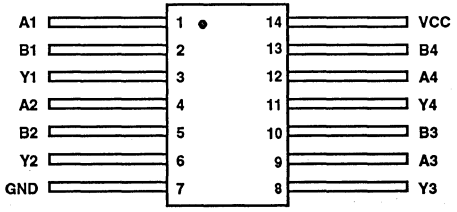
The HCS00MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835, DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835, DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

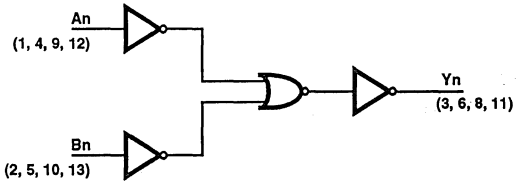


Truth Table

INPUTS		OUTPUTS
An	Bn	Yn
L	L	H
L	H	H
H	L	H
H	H	L

NOTE: L = Logic Level Low, H = Logic level High

Functional Diagram



7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2138.1**

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 100ns/V Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 30% of VCC
Input High Voltage (VIH) ..... 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Yn	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	20	ns
Input to Yn	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 38		pF
			1	+125°C	Typical 51		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics..

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70 (VCC), VIL = 0.30 (VCC) at 200K RAD, VIL = 0.12 (VCC) at 1M, RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70 (VCC), VIL = 0.30 (VCC) at 200K RAD, VIL = 0.12 (VCC) at 1M, IOL = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70 (VCC), VIL = 0.30 (VCC) at 200K RAD, VIL = 0.12 (VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Input to Yn	TPHL	VCC = 4.5V	+25°C	2	20	2	25	ns
	TPLH	VCC = 4.5V	+25°C	2	22	2	26	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
3, 6, 8, 11	1, 2, 4, 5, 7, 9, 10, 12, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 6, 8, 11	7	-	1, 2, 4, 5, 9, 10, 12, 13, 14	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 2)					
-	7	3, 6, 8, 11	14	1, 2, 4, 5, 9, 10, 12, 13	-

NOTES:

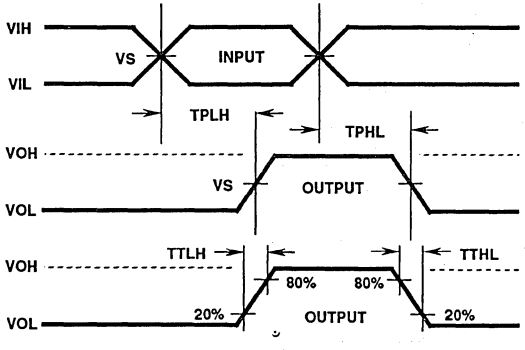
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% static burn-in.
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% static burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 6, 8, 11	7	1, 2, 4, 5, 9, 10, 12, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5%. Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures.

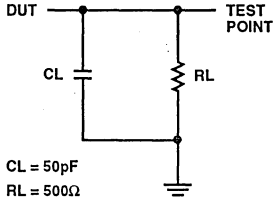
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2.20mm x 2.24mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

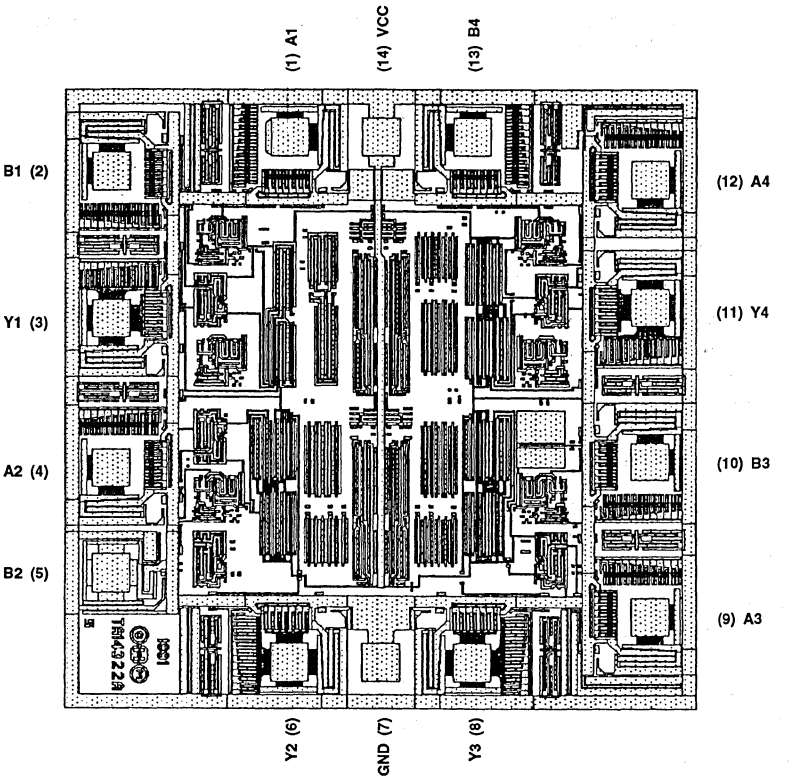
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCS00MS



HARRIS SEMICONDUCTOR

HCTS00MS

Radiation Hardened Quad 2-Input NAND Gate

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD (Si)
- Dose Rate Upset >10^{10} Rad(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity < 2 x 10^{-9} Errors/Gate Day (Typ)
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- CMOS Input Compatibility Ii ≤ 5μA at VOL, VOH

Description

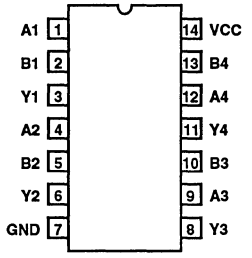
The Harris HCTS00MS is a Radiation Hardened Quad 2-Input NAND Gate. A high on both inputs forces the output to a Low state.

The HCTS00MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

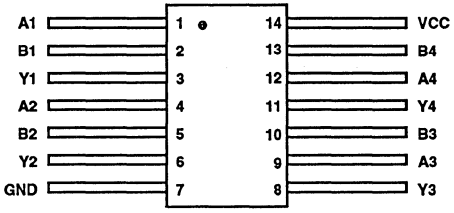
The HCTS00MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835, DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835, DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

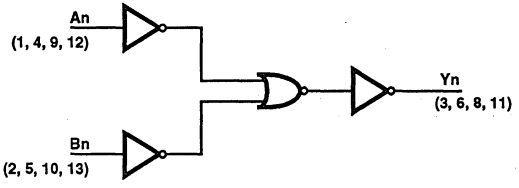


Truth Table

INPUTS		OUTPUTS
An	Bn	Yn
L	L	H
L	H	H
H	L	H
H	H	L

NOTE: L = Logic Level Low, H = Logic level High.

Functional Diagram



7 LOGIC

File Number **2139.1**

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 100ns/V Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.80V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Yn	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
Input to Yn	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 25		pF
			1	+125°C	Typical 48		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 2.25V, VIL = 0.80V at 200K RAD, VIL = 0.30V at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 2.25V, VIL = 0.80V at 200K RAD, VIL = 0.30V at 1M RAD, IOL = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.80V at 200K RAD, VIL = 0.30V at 1M RAD (Note 3)	+25°C	-	-	-	-	-

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Input to Yn	TPHL	VCC = 4.5V	+25°C	2	20	2	25	ns
	TPLH	VCC = 4.5V	+25°C	2	22	2	26	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
3, 6, 8, 11	1, 2, 4, 5, 7, 9, 10, 12, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 2)					
3, 6, 8, 11	7	-	1, 2, 4, 5, 9, 10, 12, 13, 14	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 3)					
-	7	3, 6, 8, 11	14	1, 2, 4, 5, 9, 10, 12, 13	-

NOTES:

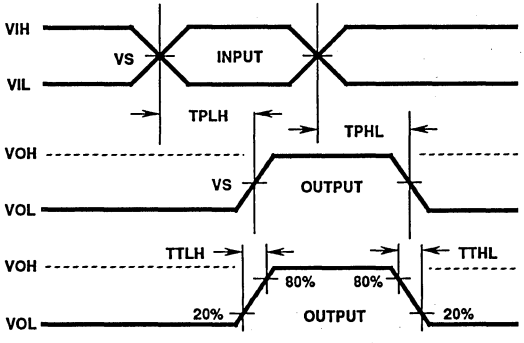
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
3. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 6, 8, 11	7	1, 2, 4, 5, 9, 10, 12, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

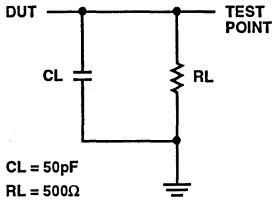
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2.20mm x 2.24mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

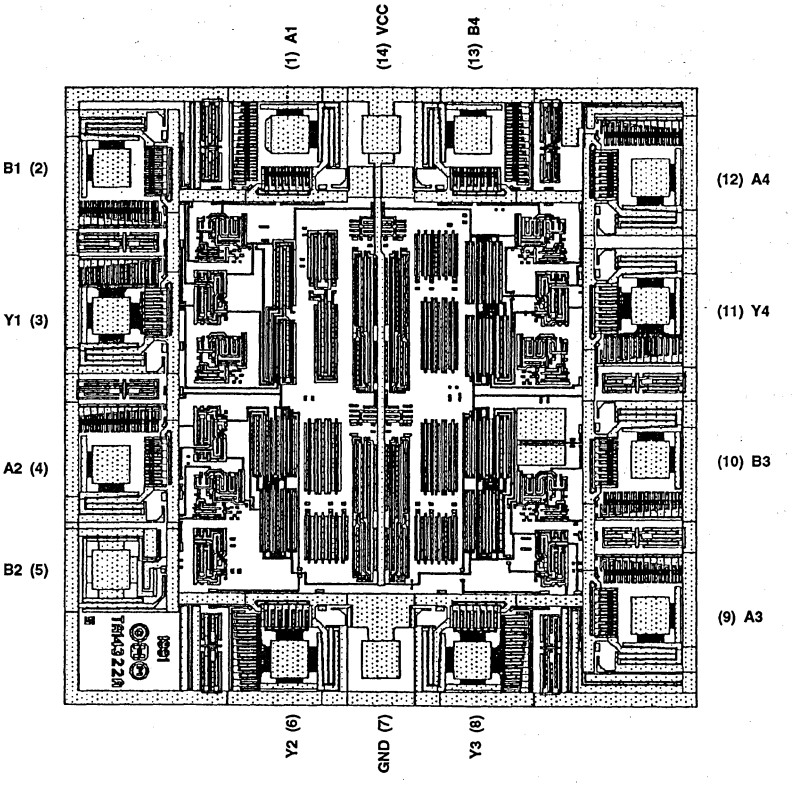
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCTS00MS



HARRIS SEMICONDUCTOR

HCS02MS

Radiation Hardened Quad 2-Input NOR Gate

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

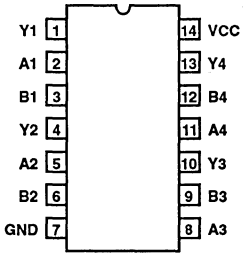
The Harris HCS02MS is a Radiation Hardened Quad 2-Input NOR Gate. A low on both inputs forces the output to a High state.

The HCS02MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

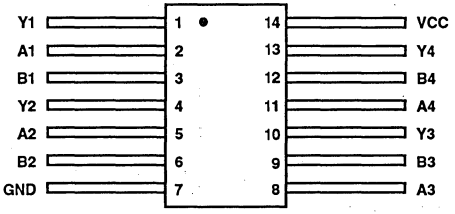
The HCS02MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

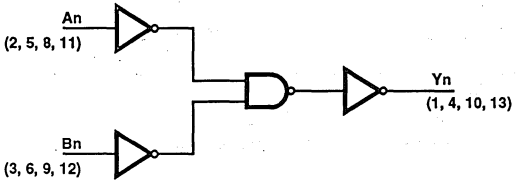


Truth Table

INPUTS		OUTPUTS
An	Bn	Yn
L	L	H
L	H	L
H	L	L
H	H	L

NOTE: L = Logic Level Low, H = Logic level High

Functional Diagram



7 LOGIC

File Number 2433.1

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Junction Temperature (TJ) ..... +175°C
Lead Temperature (Soldering 10sec) ..... +265°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 100ns/V Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 30% of VCC Max.
Input High Voltage (VIH) ..... 70% of VCC to VCC Min.

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Yn	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
Input to Yn	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 12		pF
			1	+125°C	Typical 17		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V or 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V or 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Input to Yn	TPHL	VCC = 4.5V	+25°C	2	20	2	25	ns
	TPLH	VCC = 4.5V	+25°C	2	22	2	26	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
1, 4, 10, 13	2, 3, 5, 6, 7, 8, 9, 11, 12	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
1, 4, 10, 13	7	-	2, 3, 5, 6, 8, 9, 11, 12, 14	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 2)					
-	7	1, 4, 10, 13	14	2, 3, 5, 6, 8, 9, 11, 12	-

NOTES:

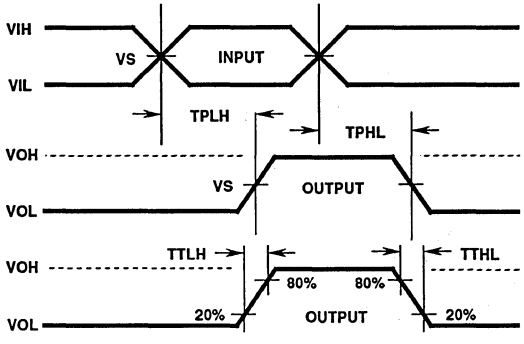
1. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% static burn-in.
2. Second dynamic burn-in assures proper stress in both directions. 400 additional hours at life test with a down point; 96 additional hours at production burn-in without a down point.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
1, 4, 10, 13	7	2, 3, 5, 6, 8, 9, 11, 12, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

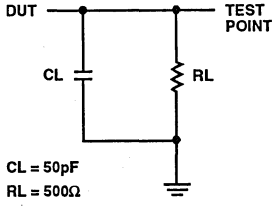
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2.20mm x 2.24mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

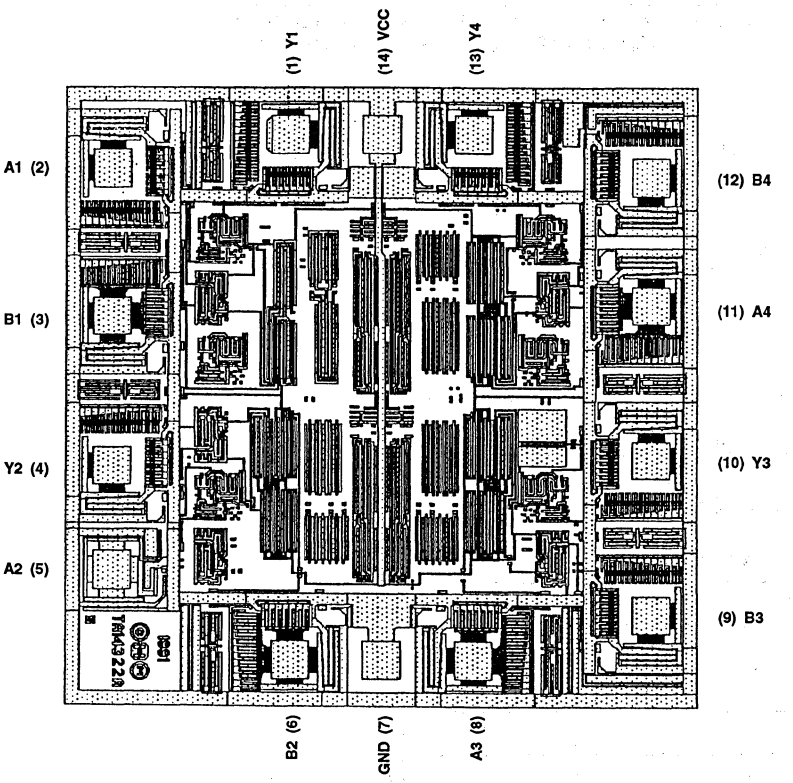
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCS02MS



HARRIS SEMICONDUCTOR

HCTS02MS

Radiation Hardened Quad 2-Input NOR Gate

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD (Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels II ≤ 5μA at VOL, VOH

Description

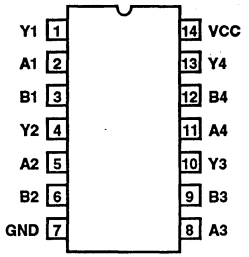
The Harris HCTS02MS is a Radiation Hardened Quad 2-Input NOR Gate. A Low on both inputs forces the output to a High state.

The HCTS02MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

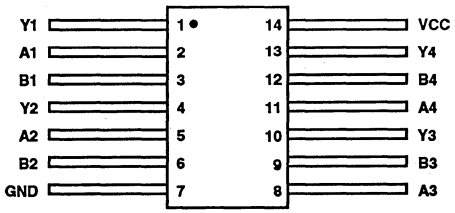
The HCTS02MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

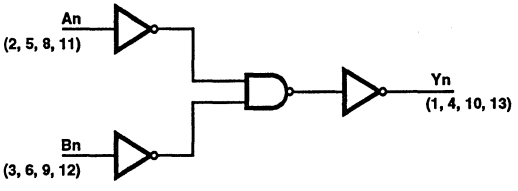


Truth Table

INPUTS		OUTPUTS
An	Bn	Yn
L	L	H
L	H	L
H	L	L
H	H	L

NOTE: L = Logic Level Low, H = Logic level High

Functional Diagram



7 LOGIC

File Number 2137.1

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC) ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 100ns/V Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... VCC/2 to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V , VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH =2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	4.0	0.5	V

NOTE:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Output	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:
1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 30		pF
			1	+125°C	Typical 45		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:
1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	200K LIMITS RAD MIN	200K LIMITS RAD MAX	1M LIMITS RAD MIN	1M LIMITS RAD MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Input to Output	TPHL	VCC = 4.5V	+25°C	2	20	2	25	ns
	TPLH		+25°C	2	22	2	26	ns

NOTES:
1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A inspection in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
1, 4, 10, 13	2, 3, 5, 6, 7, 8, 9, 11, 12	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
1, 4, 10, 13	7	-	2, 3, 5, 6, 8, 9, 11, 12, 14	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	7	1, 4, 10, 13	14	2, 3, 5, 6, 8, 9, 11, 12	-

NOTES:

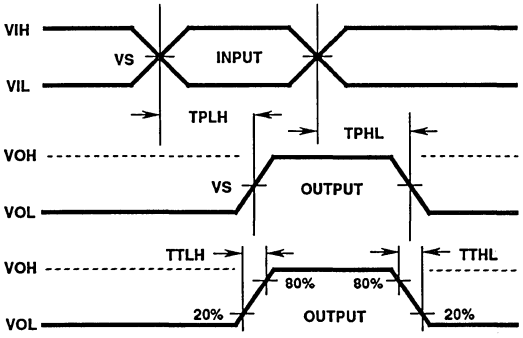
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
1, 4 10, 13	7	2, 3, 5, 6, 8, 9, 11, 12, 14

NOTE: Each pin.except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

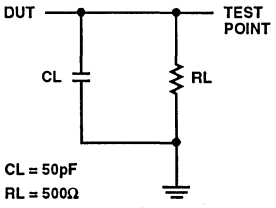
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



7 LOGIC

Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2.20 x 2.24mm

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

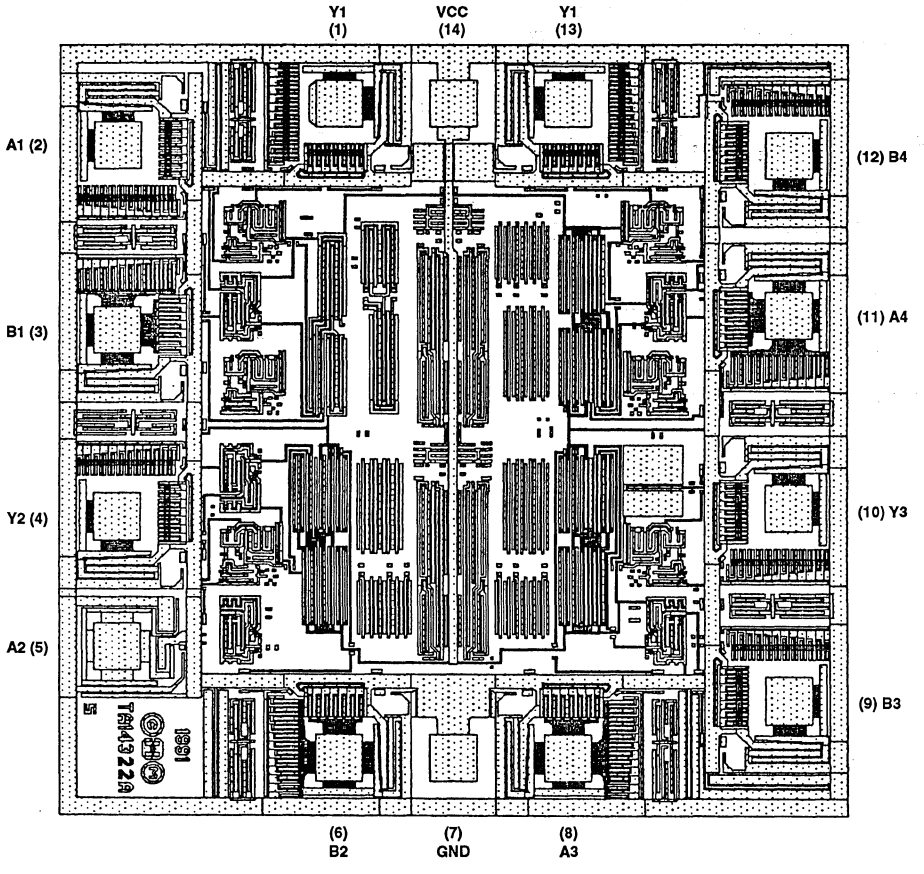
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS02MS



HARRIS SEMICONDUCTOR

HCS04MS

Radiation Hardened Hex Inverter

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity < 2 x 10^{-9} Errors/Gate Day (Typ)
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

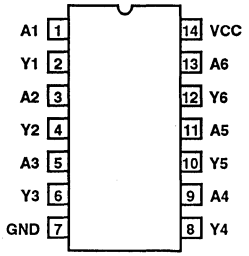
The Harris HCS04MS is a Radiation Hardened Hex Inverter. A logic level on any input forces the output to the opposite logic state.

The HCS04MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

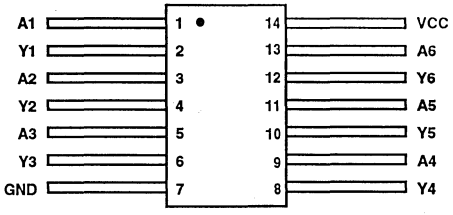
The HCS04MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-183S, DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-183S, DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

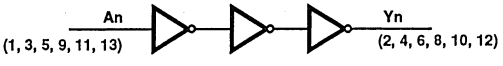


Truth Table

INPUTS	OUTPUTS
An	Yn
L	H
H	L

NOTE: L = Logic Level Low,
H = Logic level High

Functional Diagram



7 LOGIC

File Number 3046

Absolute Maximum Ratings

Supply Voltage . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input. . . . . ±10mA
DC Drain Current, Any One Output. . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 100ns/V Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 30% of VCC
Input High Voltage (VIH) . . . . . 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Yn	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	20	ns
Input to Yn	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = RF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 14		pF
			1	+125°C	Typical 18		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0..12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K Rad, VIL = 0.12(VCC) at 1M Rad, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	-	-	-	-	-	-
Input to Yn	TPHL	VCC = 4.5V	+25°C	2	20	2	25	ns
	TPLH	VCC = 4.5V	+25°C	2	22	2	26	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
2, 4, 6, 8, 10, 12	1, 3, 5, 7, 9, 11, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
2, 4, 6, 8, 10, 12	7	-	1, 3, 5, 9, 11, 13, 14	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 2)					
-	7	2, 4, 6, 8, 10, 12	14	1, 3, 5, 9, 11, 13	-

NOTES:

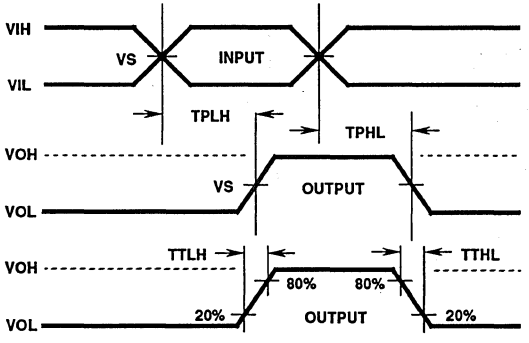
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
2, 4, 6, 8, 10, 12	7	1, 3, 5, 9, 11, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

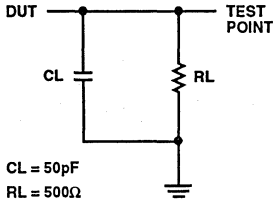
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2.20mm x 2.24mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

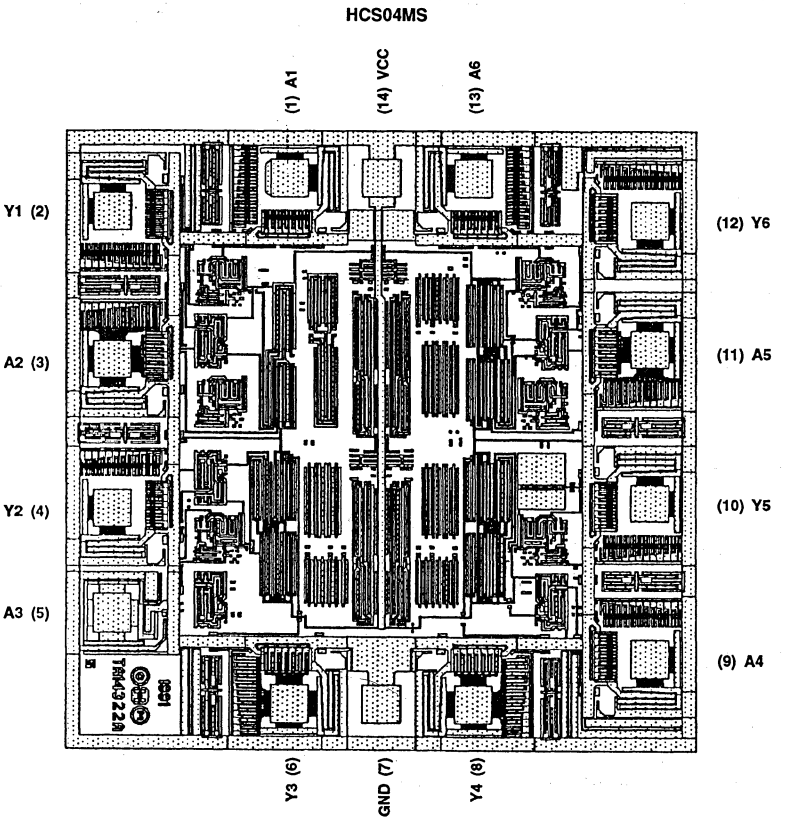
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HCTS04MS

Radiation Hardened Hex Inverter

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD (Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2
- Input Current Levels Ii ≤ 5μA @ VOL, VOH

Description

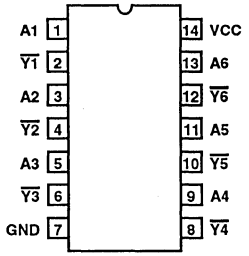
The Harris HCTS04MS is a Radiation Hardened Hex Inverter. A logic level on any input forces the output to the opposite logic state.

The HCTS04MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

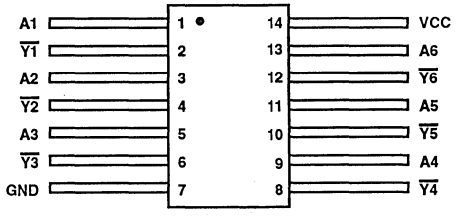
The HCTS04MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

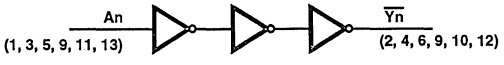


Truth Table

INPUTS	OUTPUTS
An	$\overline{Yn}$
L	H
H	L

NOTE: L = Logic Level Low,
H = Logic level High

Functional Diagram



7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2140.1**

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature TJ ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (tr, tf) ..... 100ns/V Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	0.5	0.5	µA
			2, 3	+125°C, -55°C	5.0	5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic"0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input to Output	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
Input to $\overline{Yn}$	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 33		pF
			1	+125°C	Typical 63		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V @ 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Input to Output	TPHL	VCC = 4.5V	+25°C	2	20	2	25	ns
	TPLH		+25°C	2	22	2	26	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A inspection in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% GO/NO-GO.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
2, 4, 6, 8, 10, 12	1, 3, 5, 7, 9, 11, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
2, 4, 6, 8, 10, 12	7	-	1, 3, 5, 9, 11, 13, 14	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	7	2, 4, 6, 8, 10, 12	14	1, 3, 5, 9, 11, 13	-

NOTES:

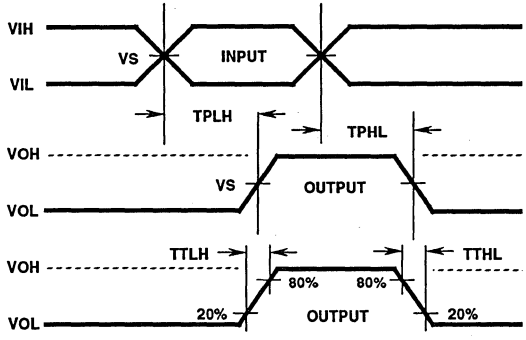
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
2, 4, 6, 8, 10, 12	7	1, 3, 5, 9, 11, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

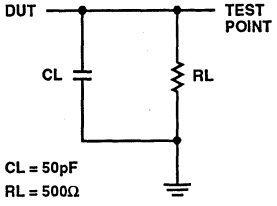
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



7 LOGIC

Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2.20 x 2.24mm

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

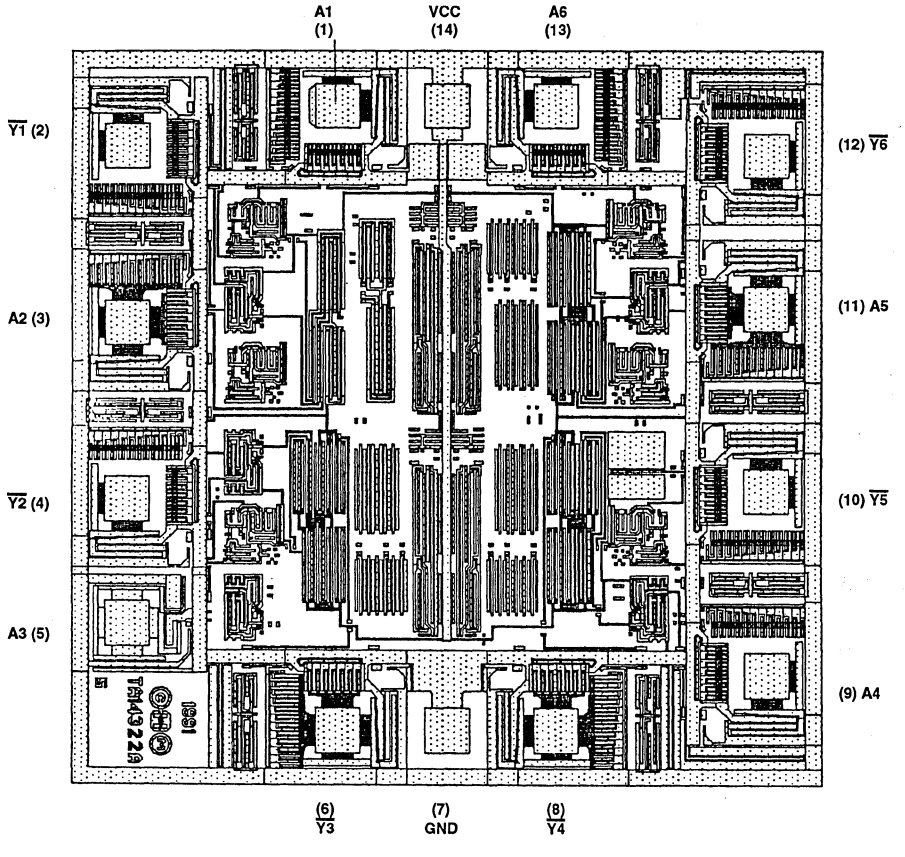
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS04MS



HARRIS SEMICONDUCTOR

HCS08MS

Radiation Hardened Quad 2-Input AND Gate

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity < 2 x 10^{7} Errors/Gate Day (Typ)
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current Levels II ≤ 5μA at VOL, VOH

Description

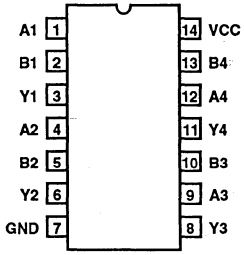
The Harris HCS08MS is a Radiation Hardened Quad 2-Input AND Gate. A high on both inputs force the output to a High state.

The HCS08MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

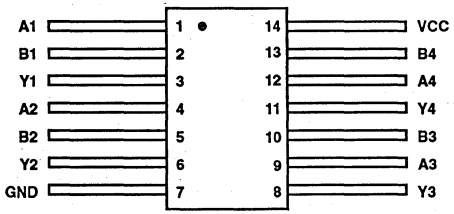
The HCS08MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-183S, DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-183S, DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

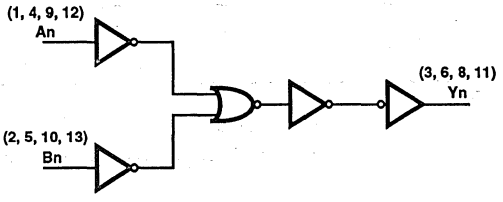


Truth Table

INPUTS		OUTPUTS
An	Bn	Yn
L	L	L
L	H	L
H	L	L
H	H	H

NOTE: L = Logic Level Low, H = Logic level High

Functional Diagram



7 LOGIC

File Number 3047

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 100ns/V Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 30% of VCC
Input High Voltage (VIH) ..... 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Yn	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
Input to Yn	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 12		pF
			1	+125°C	Typical 12		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Input to Yn	TPHL	VCC = 4.5V	+25°C	2	20	2	25	ns
	TPLH	VCC = 4.5V	+25°C	2	22	2	26	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
3, 6, 8, 11	1, 2, 4, 5, 7, 9, 10, 12, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 6, 8, 11	7	-	1, 2, 4, 5, 9, 10, 12, 13, 14	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 2)					
-	7	3, 6, 8, 11	14	1, 2, 4, 5, 9, 10, 12, 13	-

NOTES:

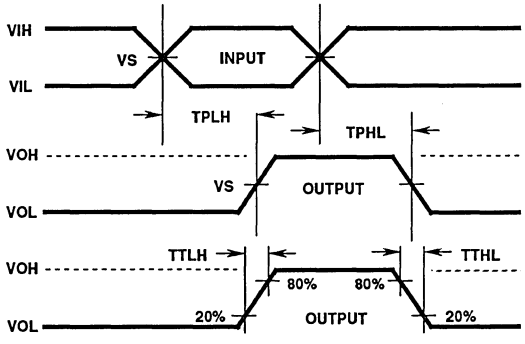
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 6, 8, 11	7	1, 2, 4, 5, 9, 10, 12, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

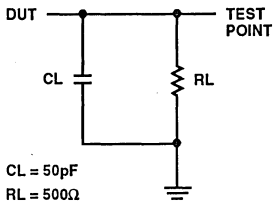
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
VSS	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2.20 x 2.24mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

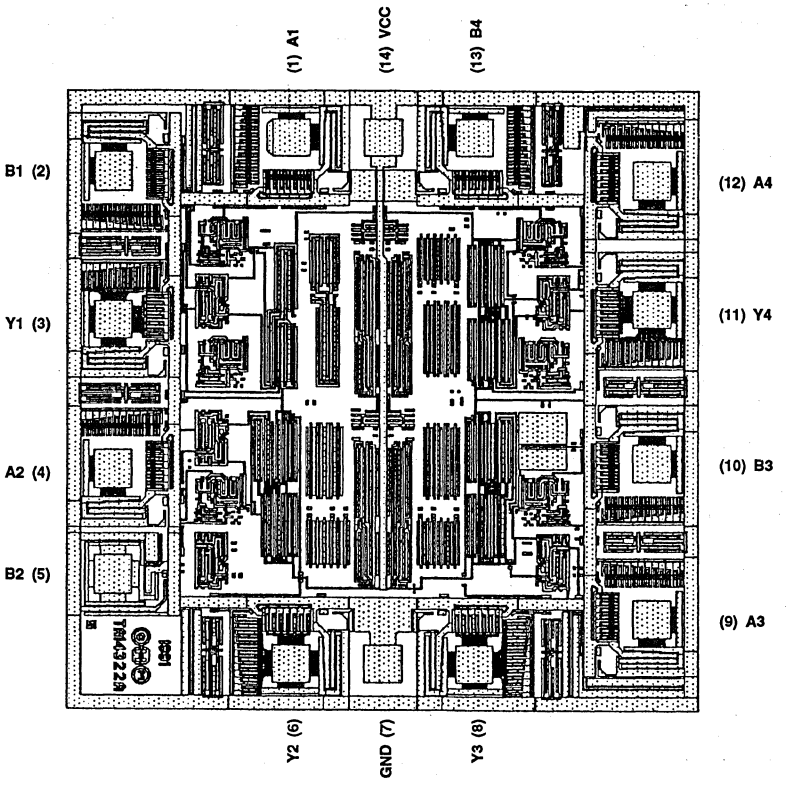
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCS08MS



HARRIS SEMICONDUCTOR

HCTS08MS

Radiation Hardened Quad 2-Input AND Gate

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD (Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V
  - VIH = VCC/2
- Input Current Levels Ii ≤ 5μA @ VOL, VOH

Description

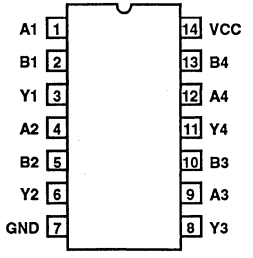
The Harris HCTS08MS is a Radiation Hardened Quad 2-Input AND Gate. A high on both input forces the output to a High state.

The HCTS08MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

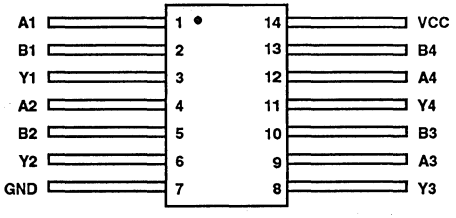
The HCTS08MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

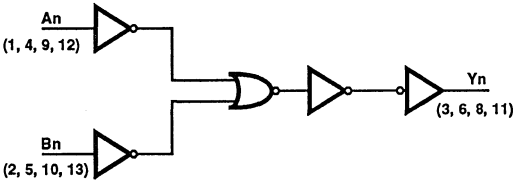


Truth Table

INPUTS		OUTPUTS
An	Bn	Yn
L	L	L
L	H	L
H	L	L
H	H	H

NOTE: L = Logic Level Low, H = Logic level High

Functional Diagram



7 LOGIC

File Number 2136.1

Absolute Maximum Ratings

Supply Voltage . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input. . . . . ±10mA
DC Drain Current, Any One Output. . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC). . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . 100ns/V Max.
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL). . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	4.0	0.5	V

NOTE:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input to Output	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 30		pF
			1	+125°C	Typical 53		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V @ 200K RAD, VIL = 0.3V @ 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V @ 200K RAD, VIL = 0.3V @ 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V @ 200K RAD, VIL = 0.3V @ 1M RAD (Note 3)	+25°C	-	-	-	-	-

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TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Input to Output	TPHL	VCC = 4.5V	+25°C	2	20	2	25	ns
	TPLH		+25°C	2	22	2	26	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUB-GROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
3, 6, 8, 11	1, 2, 4, 5, 7, 9, 10, 12, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 6, 8, 11	7	-	1, 2, 4, 5, 9, 10, 12, 13, 14	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	7	3, 6, 8, 11	14	1, 2, 4, 5, 9, 10, 12, 13	-

NOTES:

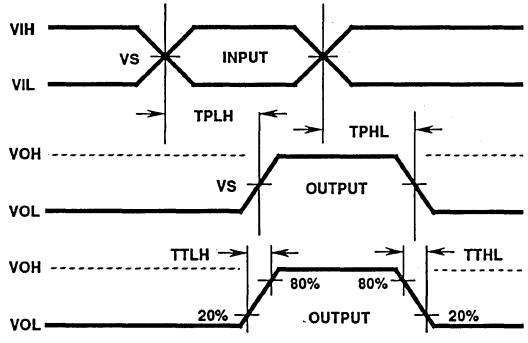
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 6V ± 0.5V
3, 6, 8, 11	7	1, 2, 4, 5, 9, 10, 12, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

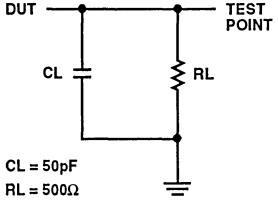
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



7 LOGIC

Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2.20 x 2.24mm

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

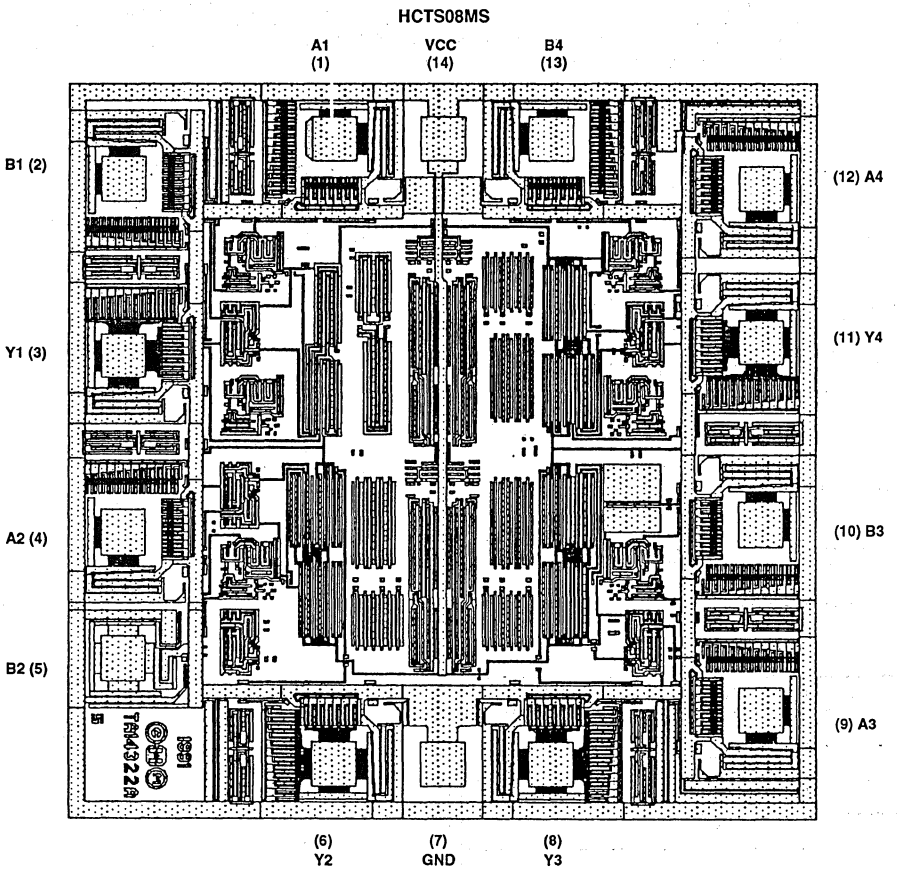
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HCS10MS

Radiation Hardened Triple 3-Input NAND Gate

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity < 2 x 10^{-9} Errors/Gate Day (Typ)
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

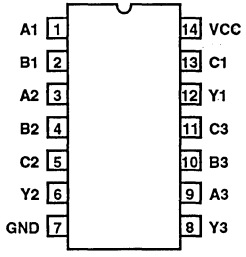
The Harris HCS10MS is a Radiation Hardened Triple 3-Input NAND Gate. A high on all inputs forces the output to a Low state.

The HCS10MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

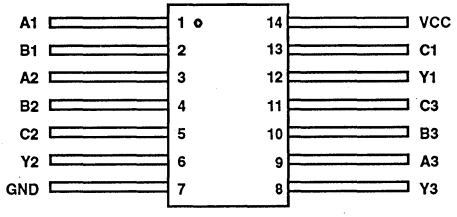
The HCS10MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-183S, DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-183S, DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

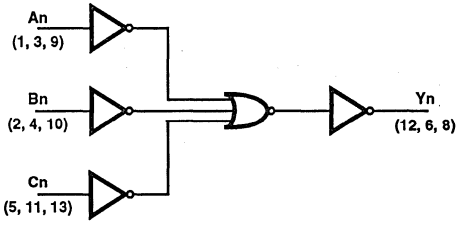


Truth Table

INPUTS			OUTPUTS
An	Bn	Cn	Yn
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

NOTE: L = Logic Level Low, H = Logic level High

Functional Diagram



7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2435.1**

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 100ns/V Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 30% of VCC
Input High Voltage (VIH) ..... 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input to Yn	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
Input to Yn	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 26		pF
			1	+125°C	Typical 31		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Input to Yn	TPHL	VCC = 4.5V	+25°C	2	20	2	25	ns
	TPLH	VCC = 4.5V	+25°C	2	22	2	26	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
6, 8, 12	1, 2, 3, 4, 5, 7, 9, 10, 11, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
6, 8, 12	7	-	1, 2, 3, 4, 5, 9, 10, 11, 13, 14	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 2)					
-	7	6, 8, 12	14	1, 2, 3, 4, 5, 9, 10, 11, 13	-

NOTES:

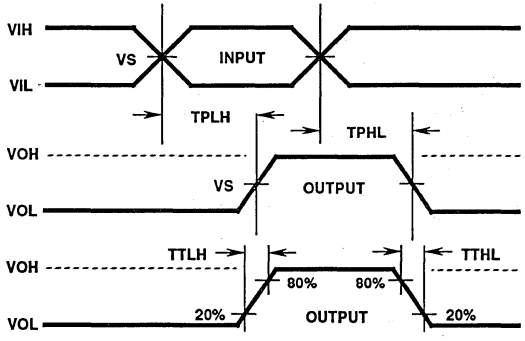
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
6, 8, 12	7	1, 2, 3, 4, 5, 9, 10, 11, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

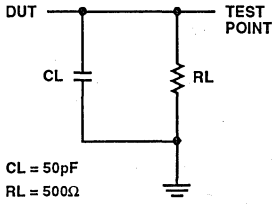
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2.20mm x 2.24mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

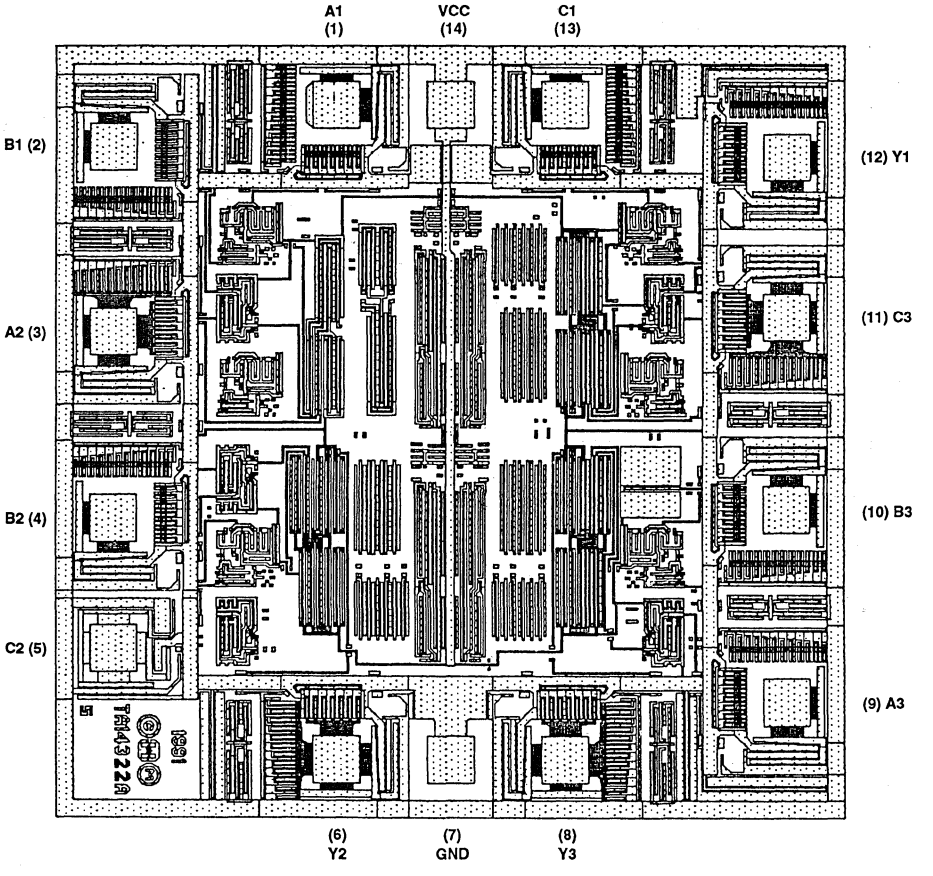
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCS10MS



HARRIS SEMICONDUCTOR

HCTS10MS

Radiation Hardened Triple 3-Input NAND Gate

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity < 2 x 10^{-9} Errors/Gate Day (Typ)
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
  - LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

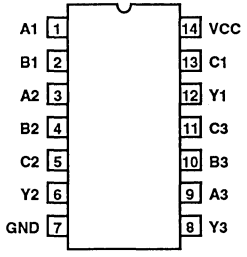
The Harris HCTS10MS is a Radiation Hardened Triple 3-Input NAND Gate. A high on all inputs forces the output to a Low state.

The HCTS10MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

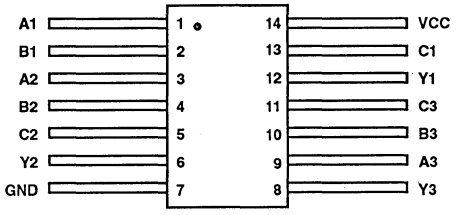
The HCTS10MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

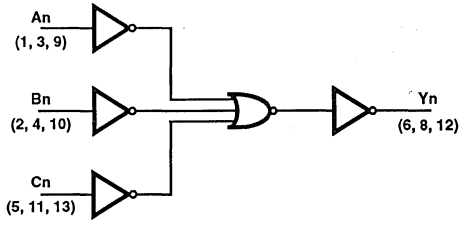


Truth Table

INPUTS			OUTPUTS
An	Bn	Cn	Yn
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

NOTE: L = Logic Level Low, H = Logic level High

Functional Diagram



7 LOGIC

File Number 2434.1

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 100ns/V Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Output	TPHL	VCC = 4.5V	9	+25°C	2	22	ns
			10, 11	+125°C, -55°C	2	24	ns
	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 35		pF
			1	+125°C	Typical 47		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5Vand 5.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Input to Output	TPHL	VCC = 4.5V	+25°C	2	24	2	28	ns
	TPLH		+25°C	2	22	2	26	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUB-GROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A inspection in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
6, 8, 12	1, 2, 3, 4, 5, 7, 9, 10, 11, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
6, 8, 12	7	-	1, 2, 3, 4, 5, 9, 10, 11, 13, 14	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 2)					
-	7	6, 8, 12	14	1, 2, 3, 4, 5, 9, 10, 11, 13	-

NOTES:

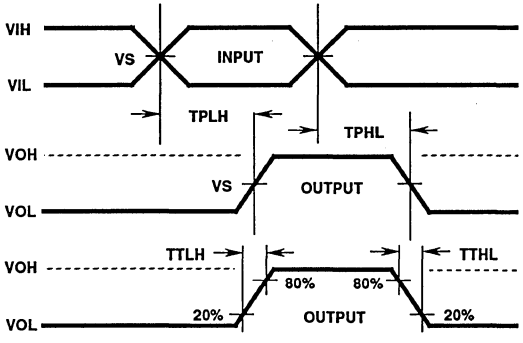
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
6, 8, 12	7	1, 2, 3, 4, 5, 9, 10, 11, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

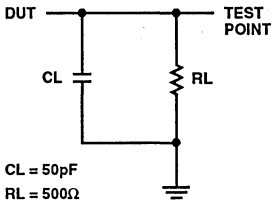
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2.20 x 2.24mm

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

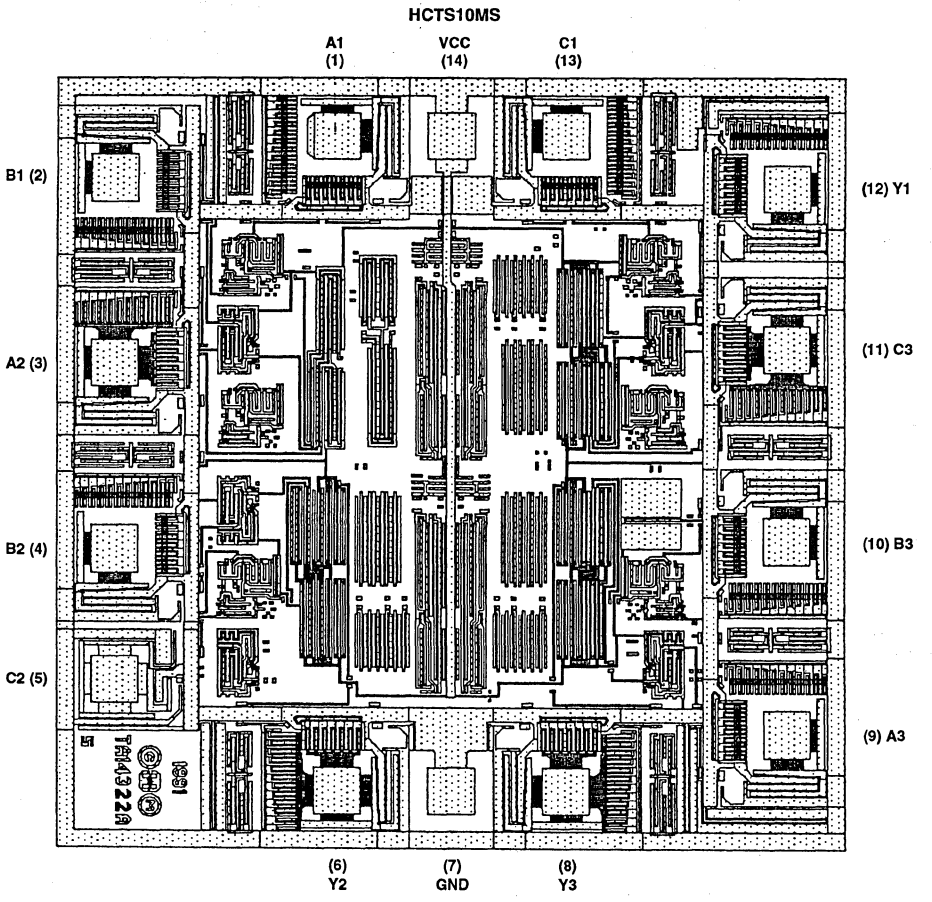
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100nm
4 x 4 mils

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HCS11MS

Radiation Hardened Triple 3-Input AND Gate

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity < 2 x 10^{-9} Errors/Gate Day (Typ)
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

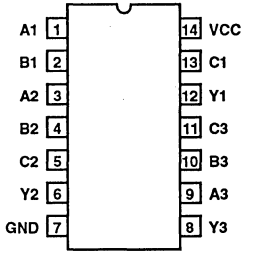
The Harris HCS11MS is a Radiation Hardened Triple 3-Input AND Gate. A high on all inputs forces the output to a High state.

The HCS11MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

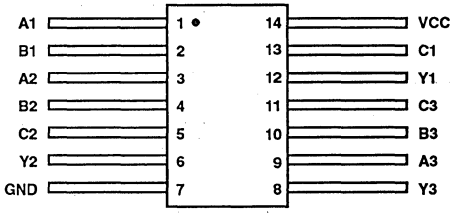
The HCS11MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

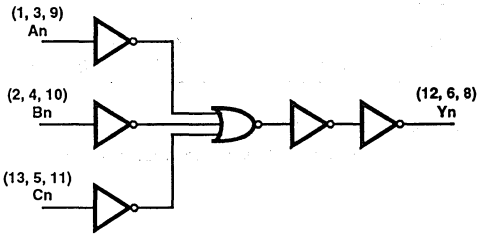


Truth Table

INPUTS			OUTPUTS
An	Bn	Cn	Yn
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

NOTE: L = Logic Level Low, H = Logic level High

Functional Diagram



7 LOGIC

File Number 3048

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 100ns/V Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 30% of VCC
Input High Voltage (VIH) ..... 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Yn	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
Input to Yn	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 20		pF
			1	+125°C	Typical 30		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Data to Output	TPHL	VCC = 4.5V	+25°C	2	20	2	25	ns
	TPLH	VCC = 4.5V	+25°C	2	22	2	28	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A inspection in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
6, 8, 12	1, 2, 3, 4, 5, 7, 9, 10, 11, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
6, 8, 12	7	-	1, 2, 3, 4, 5, 9, 10, 11, 13, 14	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 2)					
-	7	6, 8, 12	14	1, 2, 3, 4, 5, 9, 10, 11, 13	-

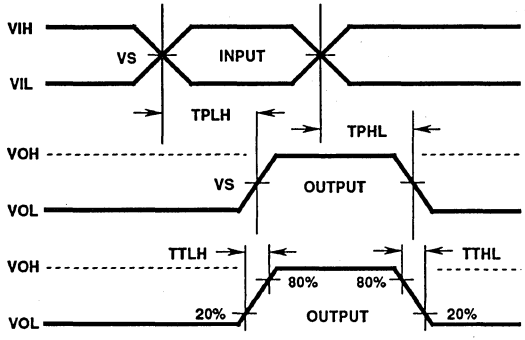
NOTES:

1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
6, 8, 12	7	1, 2, 3, 4, 5, 9, 10, 11, 13, 14

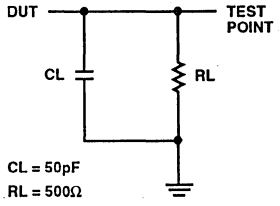
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2.20 x 2.24mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

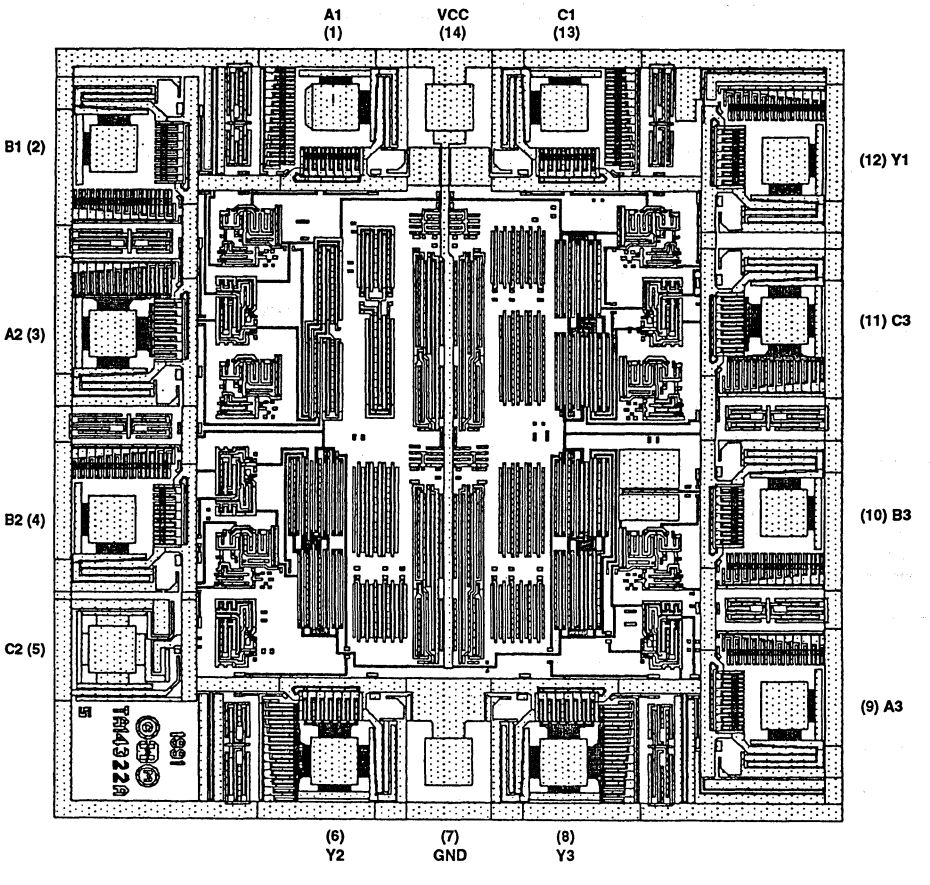
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCS11MS



HARRIS SEMICONDUCTOR

HCTS11MS

Radiation Hardened Triple 3-Input AND Gate

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD (Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max.
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

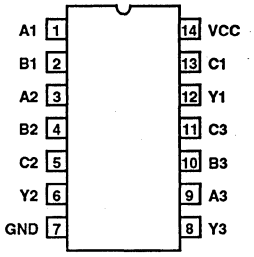
The Harris HCTS11MS is a Radiation Hardened Triple 3-Input AND Gate. A high on all inputs forces the output to a High state.

The HCTS11MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

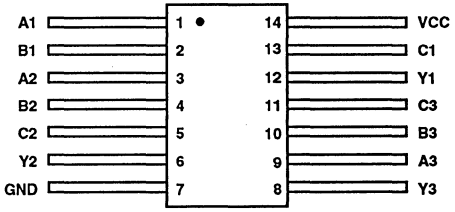
The HCTS11MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

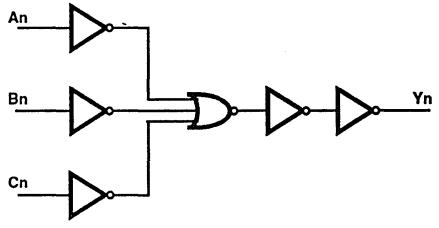


Truth Table

INPUTS			OUTPUTS
An	Bn	Cn	Yn
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

NOTE: L = Logic Level Low, H = Logic level High

Functional Diagram



7 LOGIC

File Number 2409.1

Absolute Maximum Ratings

Supply Voltage . . . . . -0.5V to 7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input. . . . . ±10mA
DC Drain Current, Any One Output. . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC). . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . 100ns/V Max.
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL). . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	4.0	0.5	-

NOTE:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Output	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input tr = tf = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 26		pF
			1	+125°C	Typical 56		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Input to Output	TPHL	VCC = 4.5V	+25°C	2	20	2	25	ns
	TPLH		+25°C	2	22	2	26	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input tr = tf = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
6, 8, 12	1, 2, 3, 4, 5, 7, 9, 10, 11, 13	-	14	-	-
STATIC BURN-IN II TEST CONDITIONS (Note 1)					
6, 8, 12	7	-	1, 2, 3, 4, 5, 9, 10, 11, 13, 14	-	-
DYNAMIC BURN-IN TEST CONDITIONS (Note 2)					
-	7	6, 8, 12	14	1, 2, 3, 4, 5, 9, 10, 11, 13	-

NOTE:

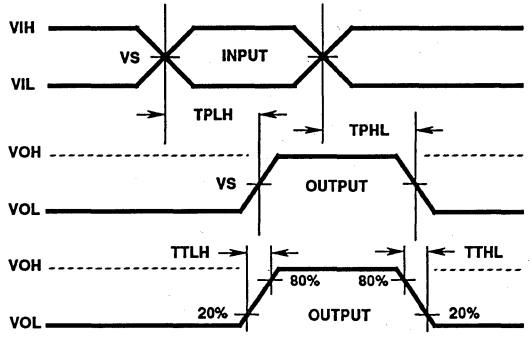
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
6, 8, 12	7	1, 2, 3, 4, 5, 9, 10, 11, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

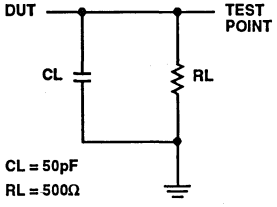
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2.20 x 2.24mm

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

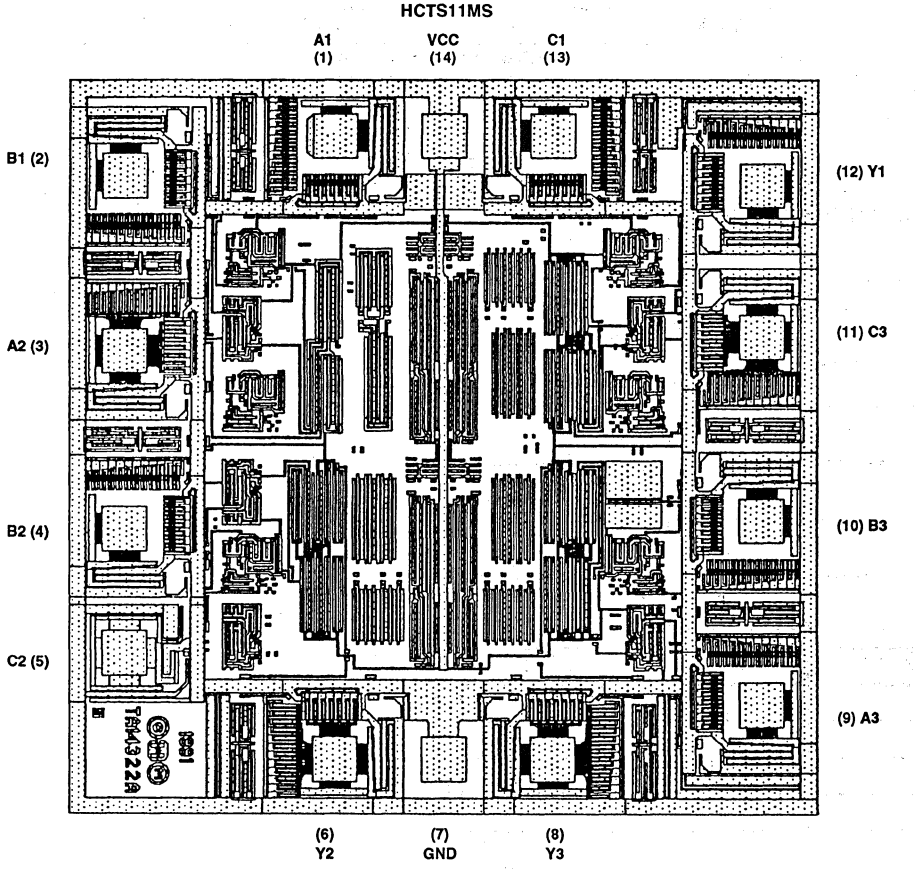
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HCS14MS

Radiation Hardened HEX Inverting Schmitt Trigger

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity < 2 x 10^{-9} Errors/Gate Day (Typ)
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

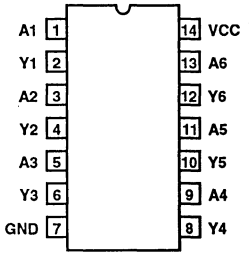
The Harris HCS14MS is a Radiation Hardened HEX Inverting Schmitt trigger. A high on any input forces the output to a Low state.

The HCS14MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

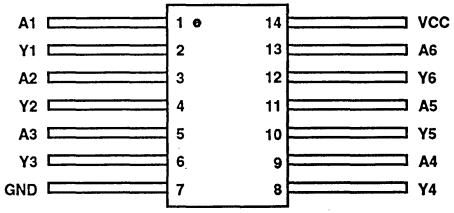
The HCS14MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-183S, DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-183S, DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

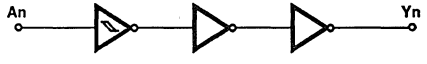


Truth Table

INPUTS An	OUTPUTS Yn
L	H
H	L

NOTE: L = Logic Level Low,
H = Logic level High

Functional Diagram



7 LOGIC

File Number 3049

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) .... Unlimited Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 30% of VCC Max.
Input High Voltage (VIH) ..... 70% of VCC to VCC Min.

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Input Switch Point	Vt+	VCC = 4.5V	1	+25°C	2.00	3.15	V
			2, 3	+125°C, -55°C	2.00	3.15	V
	Vt-	VCC = 4.5V	1	+25°C	1.35	2.60	V
			2, 3	+125°C, -55°C	1.35	2.60	V
	VH	VCC = 4.5V	1	+25°C	0.40	1.40	V
			2, 3	+125°C, -55°C	0.40	1.40	V
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), (Note 2) VIL = 0.30(VCC)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Output	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
Input to Output	TPLH	VCC = 4.5V	9	+25°C	2	22	ns
			10, 11	+125°C, -55°C	2	25	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 22		pF
			1	+125°C	Typical 26		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Input to Output	TPHL	VCC = 4.5V	+25°C	2	21	2	27	ns
	TPLH	VCC = 4.5V	+25°C	2	26	2	33	ns
Input Switch Points	Vt+	VCC = 4.5	+25°C	1.7	3.15	0.3	3.15	V
	Vt-	VCC = 4.5	+25°C	0.9	2.10	0.3	2.10	V
	VH	VCC = 4.5	+25°C	0.4	1.40	0.4	1.40	V

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
2, 4, 6, 8, 10, 12	1, 3, 5, 7, 9, 11, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
2, 4, 6, 8, 10, 12	7	-	1, 3, 5, 9, 11, 13, 14	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 2)					
-	7	2, 4, 6, 8, 10, 12	14	1, 3, 5, 9, 11, 13	-

NOTES:

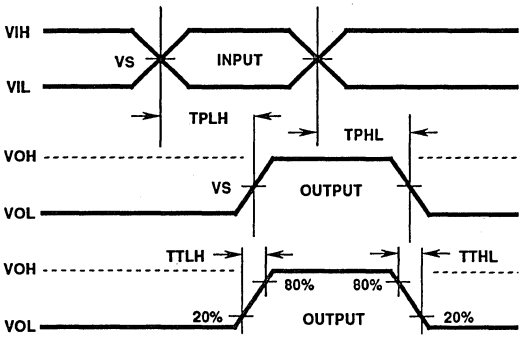
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
2, 4, 6, 8, 10, 12	7	1, 3, 5, 9, 11, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

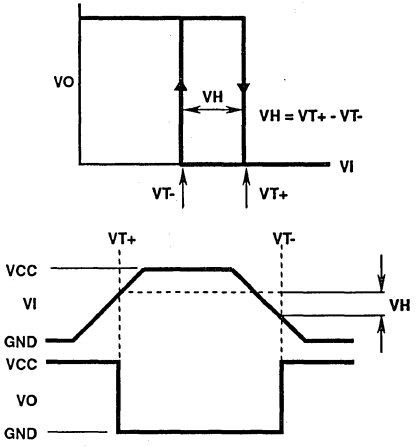
AC Timing Diagrams



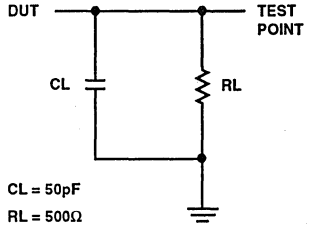
AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

Hysteresis Definition, Characteristic and Test Setup



AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2,20 x 2.24mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

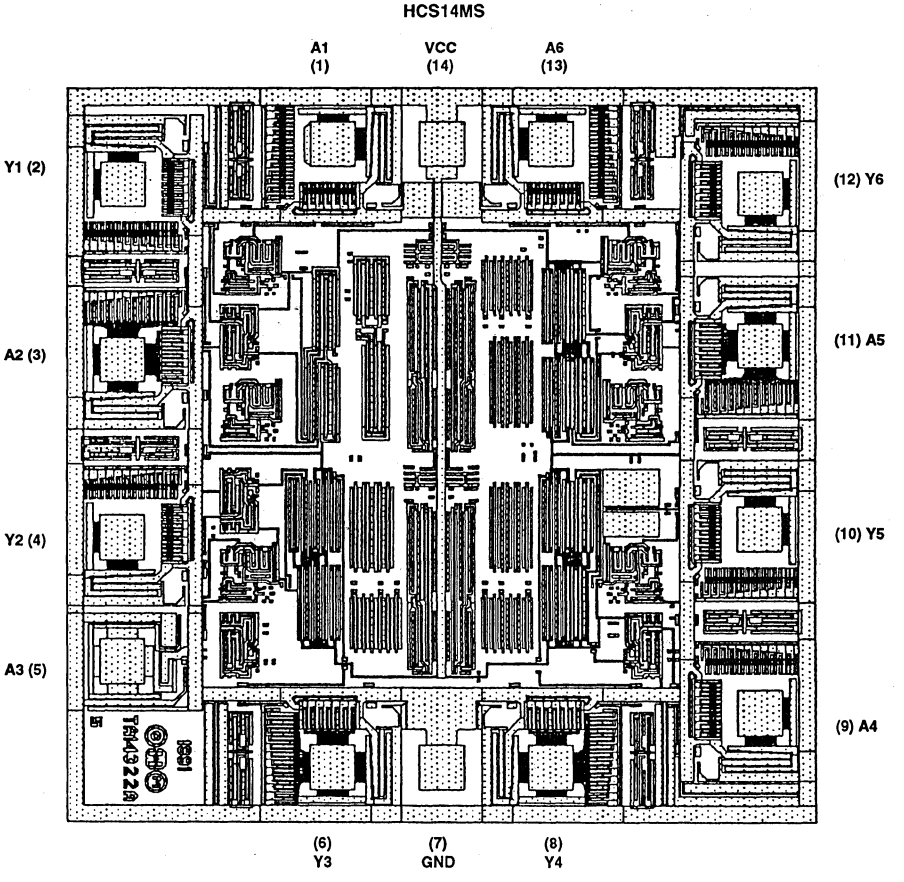
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HCTS14MS

Radiation Hardened Hex Inverting Schmitt Trigger

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD (Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Rate 2 x 10^{-9} Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA @ VOL, VOH

Description

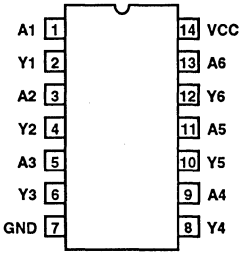
The Harris HCTS14MS is a Radiation Hardened HEX Inverting with Schmitt trigger inputs.

The HCTS14MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

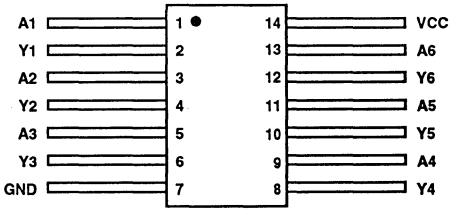
The HCTS14MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
CASE OUTLINE D-1, CONFIGURATION 3, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
CASE OUTLINE F-2A, CONFIGURATION 2, LEAD FINISH C
TOP VIEW



Truth Table

INPUTS An	OUTPUTS Yn
L	H
H	L

NOTE: L = Logic Level Low, H = Logic level High

Functional Diagram

7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3205

Absolute Maximum Ratings

Supply Voltage . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input. . . . . ±10mA
DC Drain Current, Any One Output. . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack.	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC). . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . Unlimited
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL). . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	0.5	µA
			2, 3	+125°C, -55°C	-5.0	5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V	7, 8A, 8B	+25°C, +125°C, -55°C	4.0	0.5	V

NOTE:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	19	ns
			10, 11	+125°C, -55°C	2	21	ns
	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	25	ns
			10, 11	+125°C, -55°C	2	26	ns
Input Switch Point	VT+	VCC = 4.5V	9	+25°C	0.5	2.25	V
			10, 11	+125°C, -55°C	0.5	2.25	V
	VT-	VCC = 4.5V	9	+25°C	0.5	2.25	V
			10, 11	+125°C, -55°C	0.5	2.25	V
	VH	VCC = 4.5V	9	+25°C	0.1	1.40	V
			10, 11	+125°C, -55°C	0.1	1.40	V

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, VIH = 5.0V, VIL = 0.0V, f = 1MHz	1	+25°C	Typical 17		pF
			1	+125°C	Typical 19		pF
Input Capacitance	CIN	VCC = 5.0V, VIH = 5.0V, VIL = 0.0V, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V, VIH =4.5V, VIL = 0.0V	1	+25°C	1	15	ns
			1	+125°C	1	22	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Propagation Delay	TPHL	VCC = 4.5V	+25°C	2	21	2	37	ns
	TPLH	VCC = 4.5V	+25°C	2	31	2	49	ns
Input Switch Point	VT+	VCC = 4.5	+25°C	0.40	2.25	0.30	2.25	V
	VT-	VCC = 4.5	+25°C	0.40	2.25	0.30	2.25	V
	VH	VCC = 4.5	+25°C	0.10	1.40	0.10	1.40	V

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A inspection in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS					
2, 4, 6, 8, 10, 12	1, 3, 5, 7, 9, 11, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS					
2, 4, 6, 8, 10, 12	7	-	1, 3, 5, 9, 11, 13, 14	-	-
DYNAMIC BURN-IN TEST CONNECTIONS					
-	7	2, 4, 6, 8, 10, 12	14	1, 3, 5, 9, 11, 13	-

NOTES:

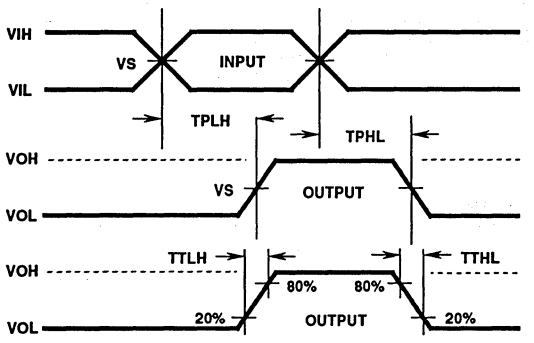
1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1kΩ ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
2, 4, 6, 8, 10, 12	7	1, 3, 5, 9, 11, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

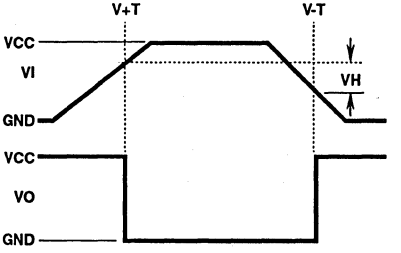
AC Timiing Diagrams

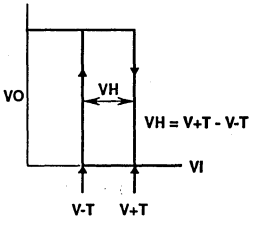


AC VOLTAGE LEVELS

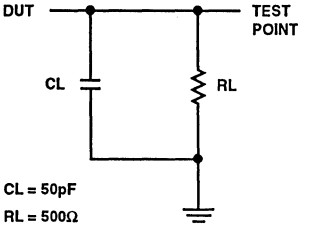
PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.0	V
VS	1.3	V
VIL	0	V
GND	0	V

Hysteresis Definition, Characteristic, and Test Setup





AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2.20 x 2.24mm

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± -2.6kÅ

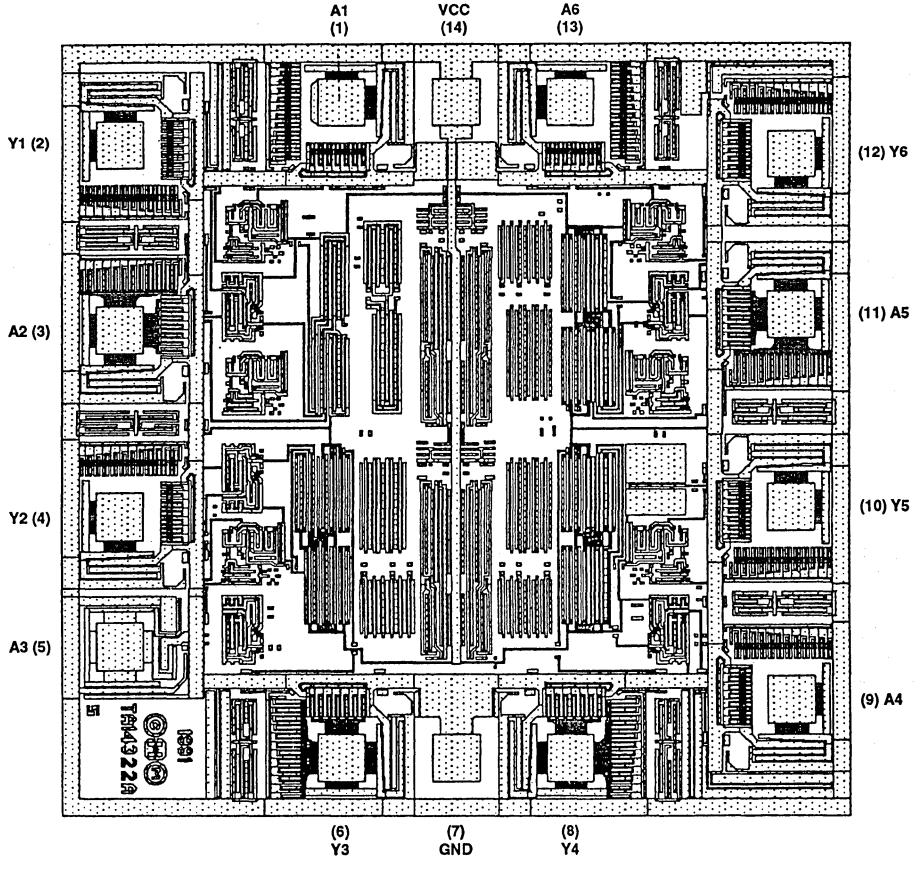
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCTS14MS



HARRIS SEMICONDUCTOR

HCS20MS

Radiation Hardened Dual 4-Input NAND Gate

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity < 2 x 10^{-9} Errors/Gate Day (Typ
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current Levels II ≤ 5μA at VOL, VOH

Description

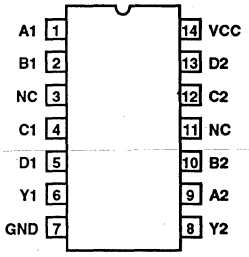
The Harris HCS20MS is a Radiation Hardened Dual 4-Input NAND Gate. A low on any input forces the output to a High state.

The HCS20MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

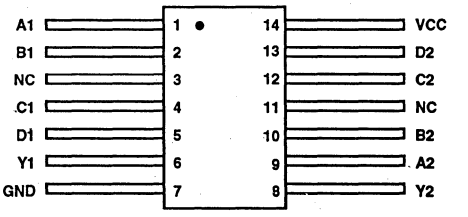
The HCS20MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-183S, DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-183S, DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

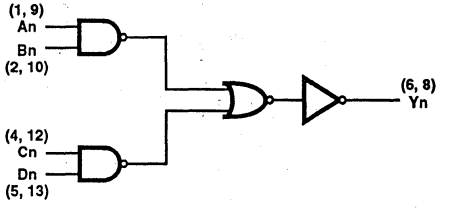


Truth Table

INPUTS				OUTPUTS
An	Bn	Cn	Dn	Yn
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

NOTE: L = Logic Level Low, H = Logic level High, X = Don't Care

Functional Diagram



File Number 3050

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 100ns Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 30% of VCC
Input High Voltage (VIH) ..... 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), (Note 2) VIL = 0.30(VCC)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Data to Output	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
Data to Output	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 25		pF
			1	+125°C	Typical 30		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	4.0	0.5	4.0	0.5	V
Input to Yn	TPHL	VCC = 4.5V	+25°C	2	20	2	25	ns
	TPLH	VCC = 4.5V	+25°C	2	22	2	26	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
3, 6, 8, 11	1, 2, 4, 5, 7, 9, 10, 12, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 6, 8, 11	7	-	1, 2, 4, 5, 9, 10, 12, 13, 14	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 2)					
-	7	3, 6, 8, 12	14	1, 2, 4, 5, 9, 10, 12, 13	-

NOTES:

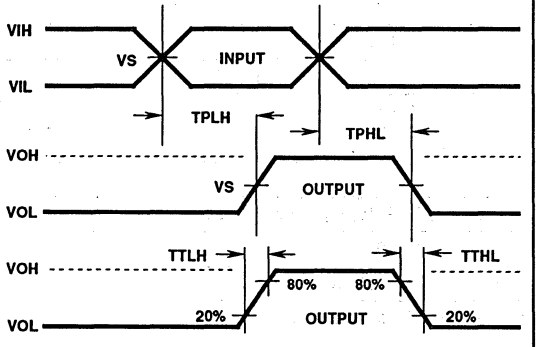
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 6, 8, 11	7	1, 2, 4, 5, 9, 10, 12, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

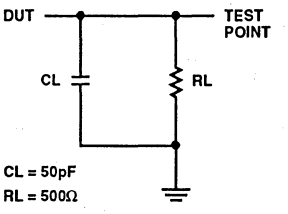
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2.20mm x 2.24mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

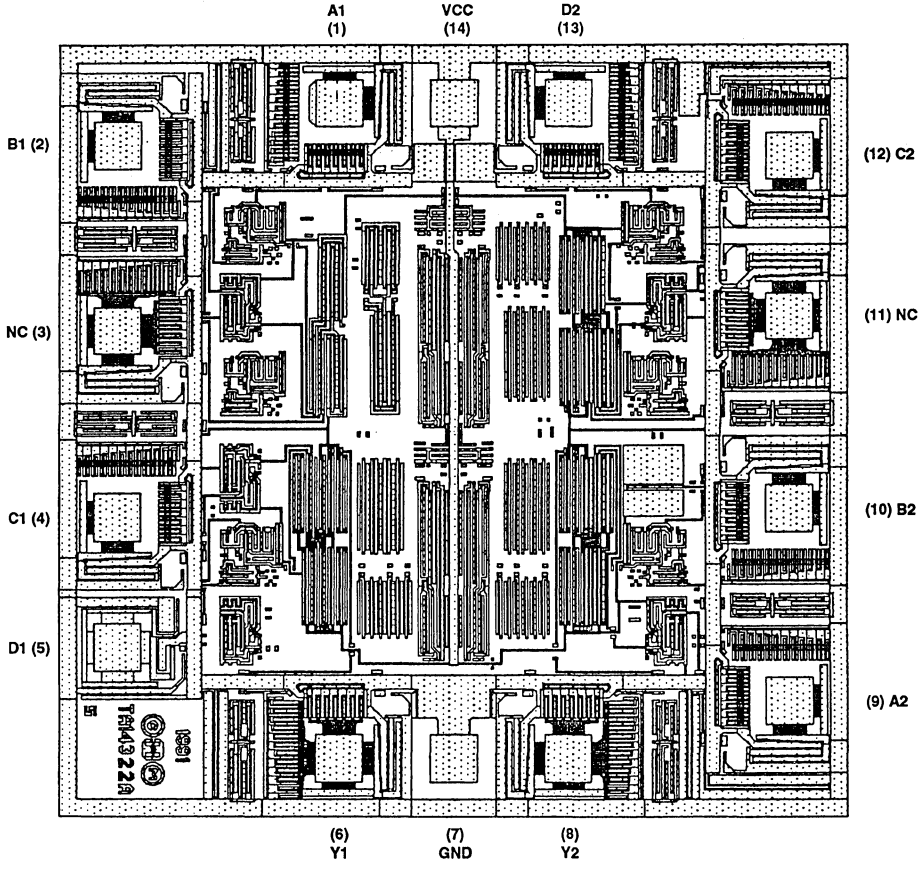
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCS20MS



HARRIS SEMICONDUCTOR

HCTS20MS

Radiation Hardened Dual 4-Input NAND Gate

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

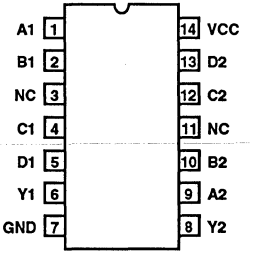
The Harris HCTS20MS is a Radiation Hardened Dual 4-Input NAND Gate. A low on both input forces the output to a High state.

The HCTS20MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

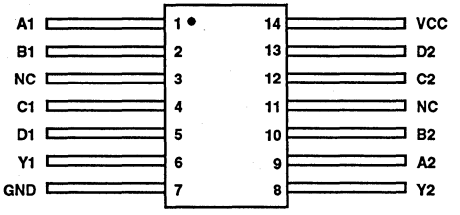
The HCTS20MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

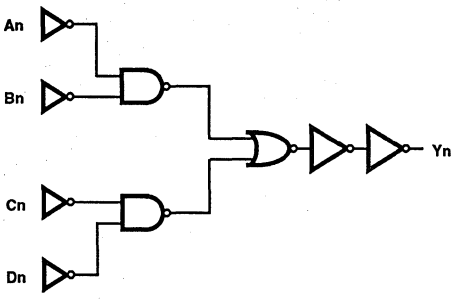


Truth Table

INPUTS				OUTPUTS
An	Bn	Cn	Dn	Yn
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

NOTE: L = Logic Level Low, H = Logic level High, X = Don't Care

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3051

Absolute Maximum Ratings

Supply Voltage (VCC) ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC) ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 100ns/V Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.80V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Output	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 40		pF
			1	+125°C	Typical 80		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 2.25V, VIL = 0.80V at 200K RAD, VIL = 0.30V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	4.0	0.5	4.0	0.5	V

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Input to Output	TPHL	VCC = 4.5V	+25°C	2	20	2	25	ns
	TPLH	VCC = 4.5V	+25°C	2	22	2	26	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input tr = tf = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A inspection in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
3, 6, 8, 11	1, 2, 4, 5, 7, 9, 10, 12, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 6, 8, 11	7	-	1, 2, 4, 5, 9, 10, 12, 13, 14	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	7	3, 6, 8, 11	14	1, 2, 4, 5, 9, 10, 12, 13	-

NOTES:

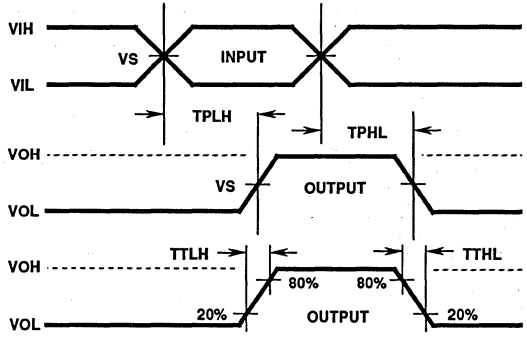
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 6, 8, 11	7	1, 2, 4, 5, 9, 10, 12, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

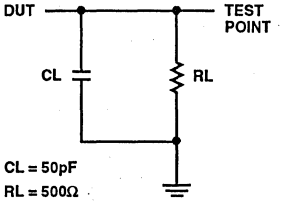
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
2.20 x 2.24(mm)

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

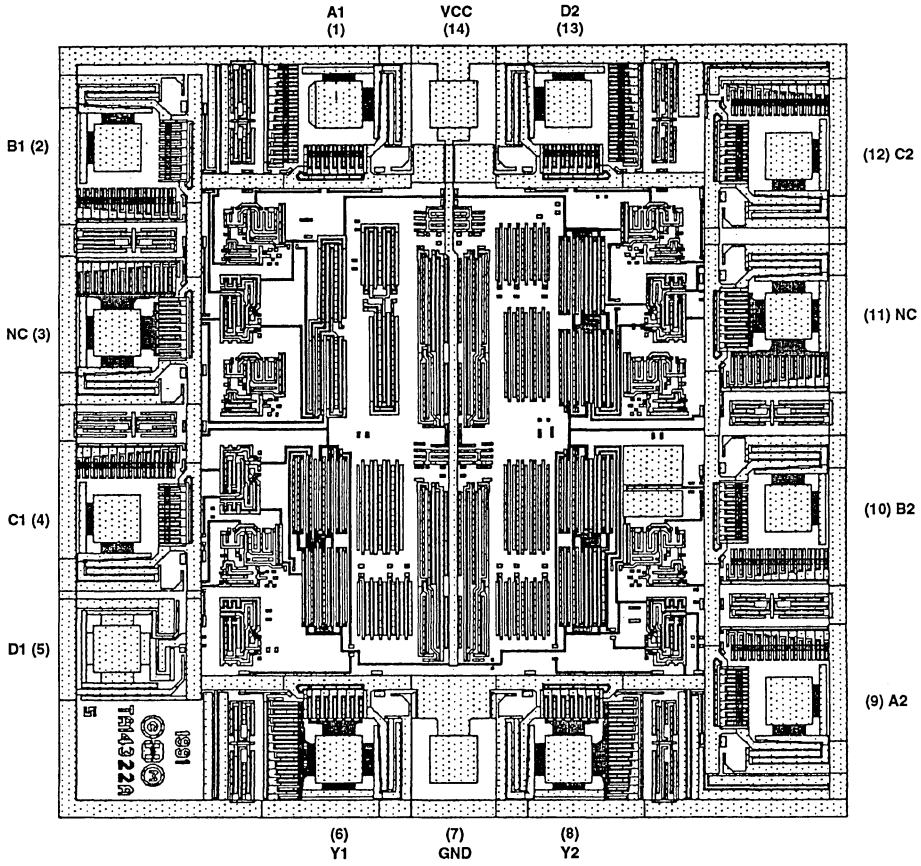
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS20MS



HARRIS SEMICONDUCTOR

HCS21MS

Radiation Hardened Dual 4-Input AND Gate

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity < 2 x 10^{-9} Errors/Gate Day (Typ
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

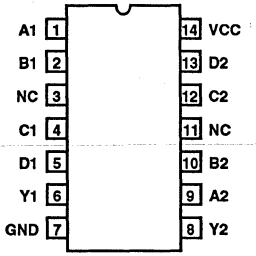
The Harris HCS21MS is a Radiation Hardened Dual Input AND Gate. A high on all inputs forces the output to a High state.

The HCS21MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

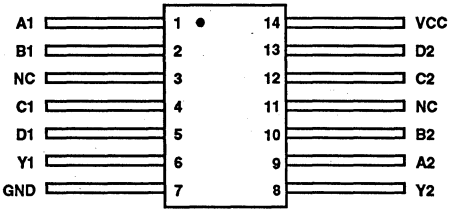
The HCS21MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
CDFP3-F14, LEAD FINISH C
TOP VIEW

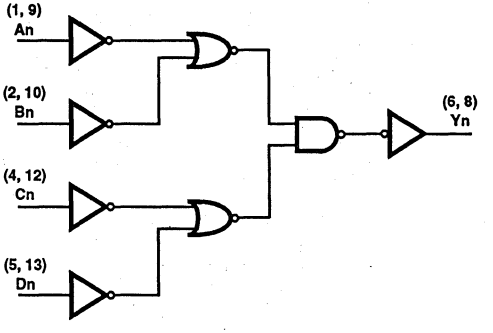


Truth Table

INPUTS				OUTPUTS
An	Bn	Cn	Dn	Yn
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	HX	H	H

NOTE: L = Logic Level Low, H = Logic level High, X = Don't Care

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3052

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 100ns Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 30% of VCC
Input High Voltage (VIH) ..... 70% of VCC of VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), (Note 2) VIL = 0.30(VCC)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input to Y	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
	TPLH	VCC = 4.5V	10, 11	+125°C, -55°C	2	20	ns
Input to YN	TPHL	VCC = 4.5V	9	+25°C	2	20	ns
	TPLH	VCC = 4.5V	10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 26		pF
			1	+125°C	Typical 29		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics..

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Input to Y	TPHL	VCC = 4.5V	+25°C	2	20	2	25	ns
	TPLH	VCC = 4.5V	+25°C	2	22	2	28	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
3, 6, 8, 11	1, 2, 4, 5, 7, 9, 10, 12, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 6, 8, 11	7	-	1, 2, 4, 5, 9, 10, 12, 13, 14	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 2)					
-	7	3, 6, 8, 12	14	1, 2, 4, 5, 9, 10, 12, 13	-

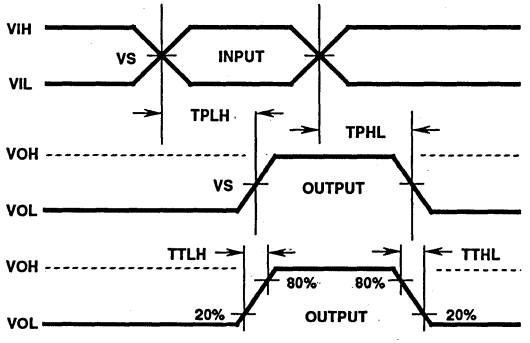
NOTES:

1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 6, 8, 11	7	1, 2, 4, 5, 9, 10, 12, 13, 14

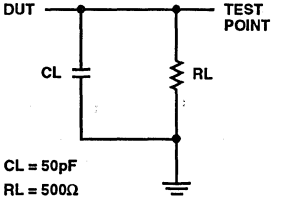
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2.20mm x 2.24mm

METALLIZATION:
Type: AlSil
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

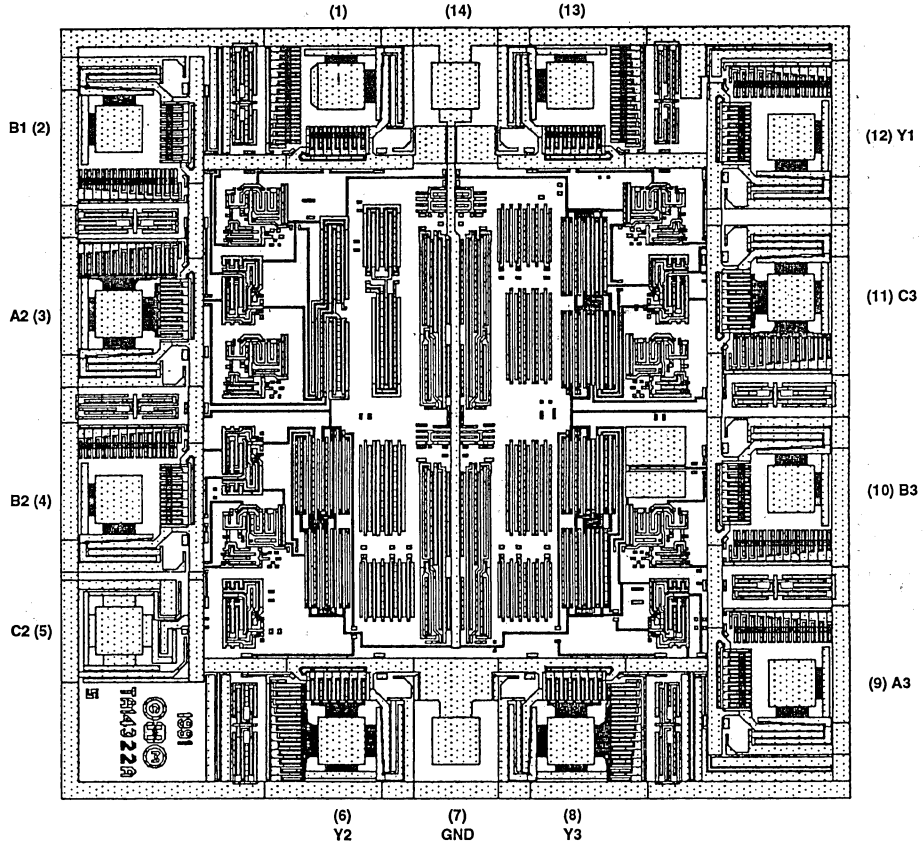
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCS21MS



HARRIS SEMICONDUCTOR

HCTS21MS

Radiation Hardened Dual 4-Input AND Gate

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

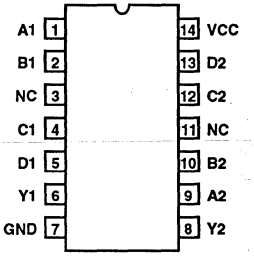
The Harris HCTS21MS is a Radiation Hardened Dual Input AND Gate. A high on all inputs forces the output to a High state.

The HCTS21MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

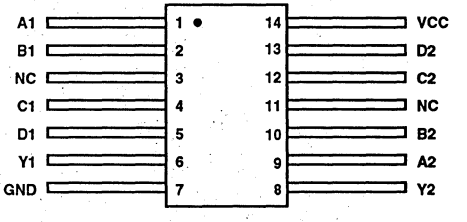
The HCTS21MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

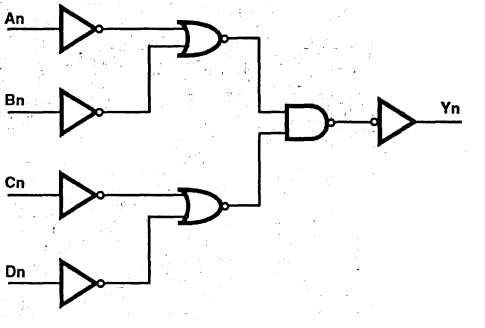


Truth Table

INPUTS				OUTPUTS
An	Bn	Cn	Dn	Yn
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

NOTE: L = Logic Level Low, H = Logic level High, X = Don't Care

Functional Diagram



File Number 3053

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) .... 100ns/V Max.
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-0.5	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Output	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 42		pF
			1	+125°C	Typical 82		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Input to Output	TPHL	VCC = 4.5V	+25°C	2	20	2	25	ns
	TPLH	VCC = 4.5V	+25°C	2	22	2	26	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A inspection in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONDITIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS					
3, 6, 8, 11	1, 2, 4, 5, 7, 9, 10, 12, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS					
3, 6, 8, 11	7	-	1, 2, 4, 5, 9, 10, 12, 13, 14	-	-
DYNAMIC BURN-IN TEST CONNECTIONS					
-	7	3, 6, 8, 11	14	1, 2, 4, 5, 9, 10, 12, 13	-

NOTE:

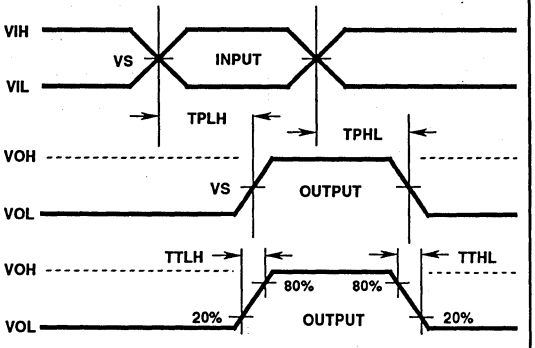
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 6, 8, 11	7	1, 2, 4, 5, 9, 10, 12, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

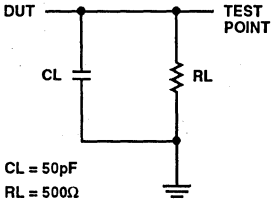
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2.20 x 2.24mm

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

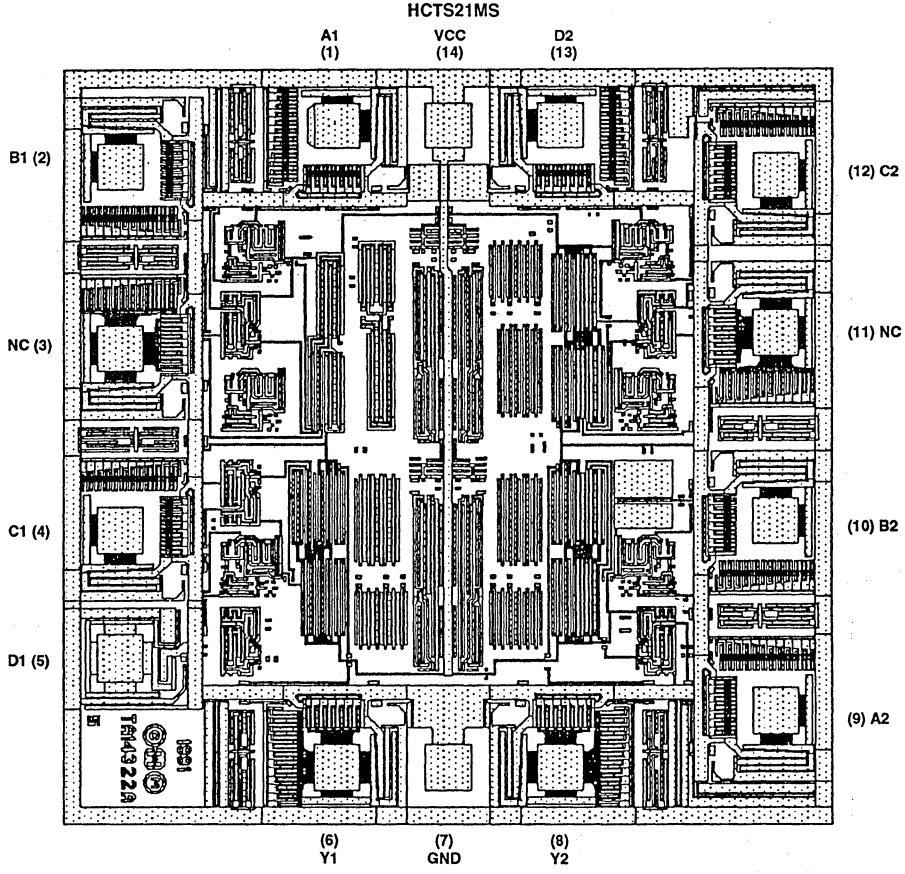
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HCS27MS

Radiation Hardened Triple 3-Input NOR Gate

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity < 2 x 10^{-9} Errors/Gate Day (Typ
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

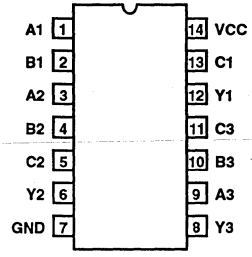
The Harris HCS27MS is a Radiation Hardened Triple 3-Input NOR Gate. A low on all inputs forces the output to a High state.

The HCS27MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

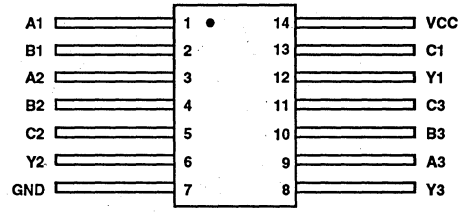
The HCS27MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

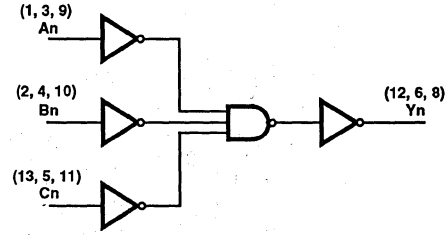


Truth Table

INPUTS			OUTPUTS
An	Bn	Cn	Yn
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	L

NOTE: L = Logic Level Low, H = Logic level High

Functional Diagram



File Number 3054

Absolute Maximum Ratings

Supply Voltage . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input. . . . . ±10mA
DC Drain Current, Any One Output. . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack.	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 100ns Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL). . . . . 0.0V to 30% to VCC
Input High Voltage (VIH) . . . . . 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), (Note 2) VIL = 0.30(VCC)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Yn	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
Input to Yn	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 16		pF
			1	+125°C	Typical 18		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Input to Yn	TPHL	VCC = 4.5V	+25°C	2	20	2	25	ns
	TPLH	VCC = 4.5V	+25°C	2	22	2	26	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
6, 8, 12	1, 2, 3, 4, 5, 7, 9, 10, 11, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
6, 8, 12	7	-	1, 2, 3, 4, 5, 9, 10, 11, 13, 14	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 2)					
-	7	6, 8, 12	14	1, 2, 3, 4, 5, 9, 10, 11, 13	-

NOTES:

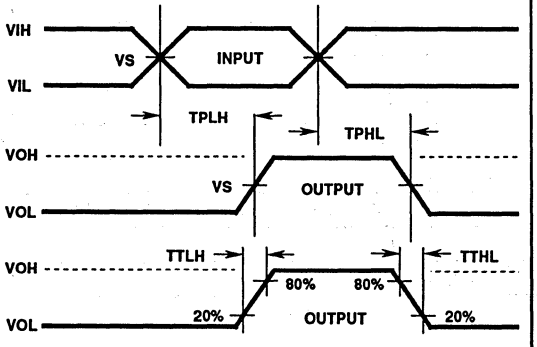
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
6, 8, 12	7	1, 2, 3, 4, 5, 9, 10, 11, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

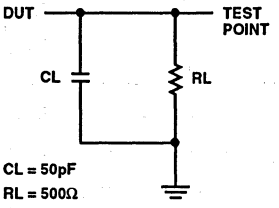
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2.20 x 2.24mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

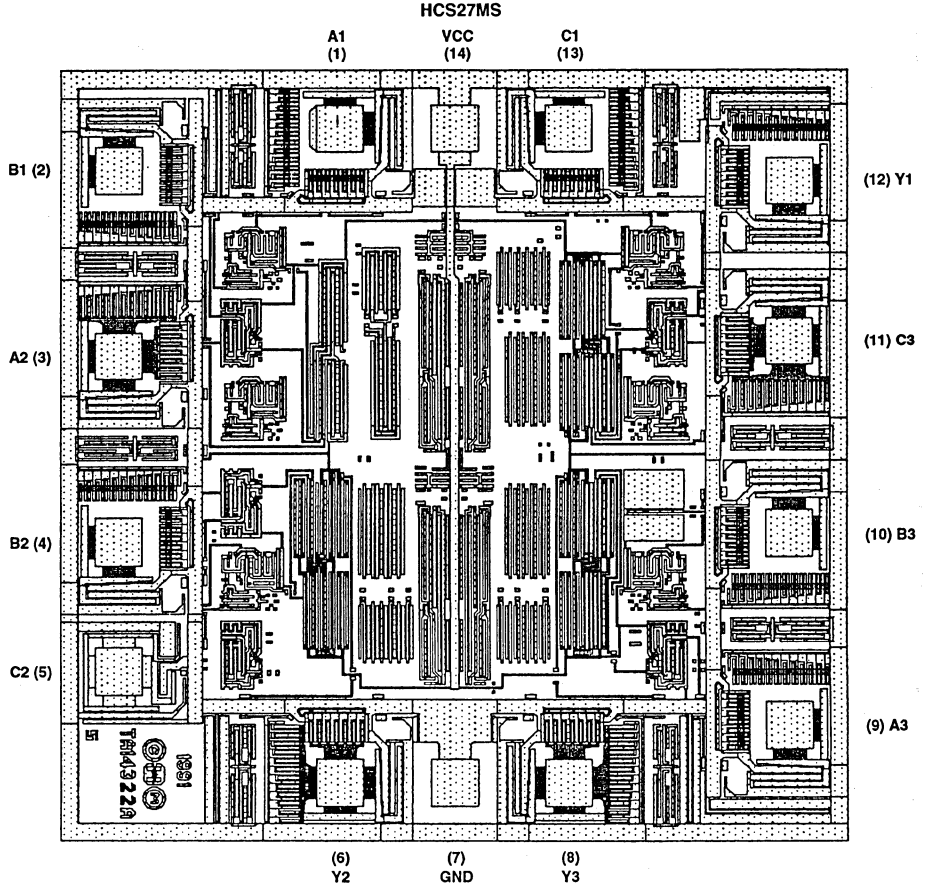
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HCTS27MS

Radiation Hardened Triple 3-Input NOR Gate

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

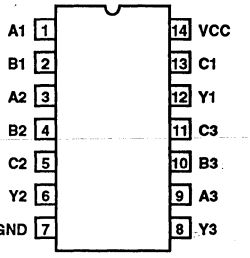
The Harris HCTS27MS is a Radiation Hardened Triple 3-Input NOR Gate. A˚Low on all inputs forces the output to a High state.

The HCTS27MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

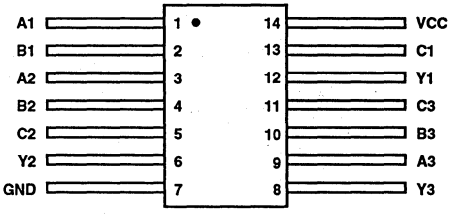
The HCTS27MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

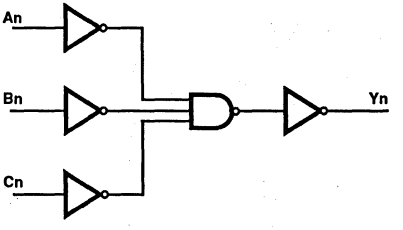


Truth Table

INPUTS			OUTPUTS
An	Bn	Cn	Yn
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	L

NOTE: L = Logic Level Low, H = Logic level High

Functional Diagram



File Number 3055

Absolute Maximum Ratings

Supply Voltage . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input. . . . . ±10mA
DC Drain Current, Any One Output. . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC). . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (tr, tf). . . . . 100ns/V Max.
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL). . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-0.5	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Output	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
Input to Output	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 23		pF
			1	+125°C	Typical 25		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C, -55°C	-	22	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Input to Output	TPHL	VCC = 4.5V	+25°C	2	20	2	25	ns
	TPLH	VCC = 4.5V	+25°C	2	22	2	26	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A inspection in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
6, 8, 12	1 - 5, 7, 9, 10, 11, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
6, 8, 12	7	-	1 - 5, 9, 10, 11, 13, 14	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	7	6, 8, 12	14	1 - 5, 9, 10, 11, 13	-

NOTE:

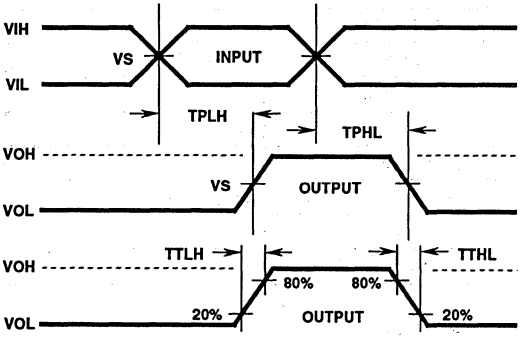
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
6, 8, 12	7	1 - 5, 9, 10, 11, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

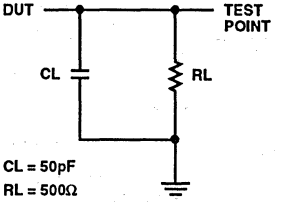
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2.20 x 2.24mm

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

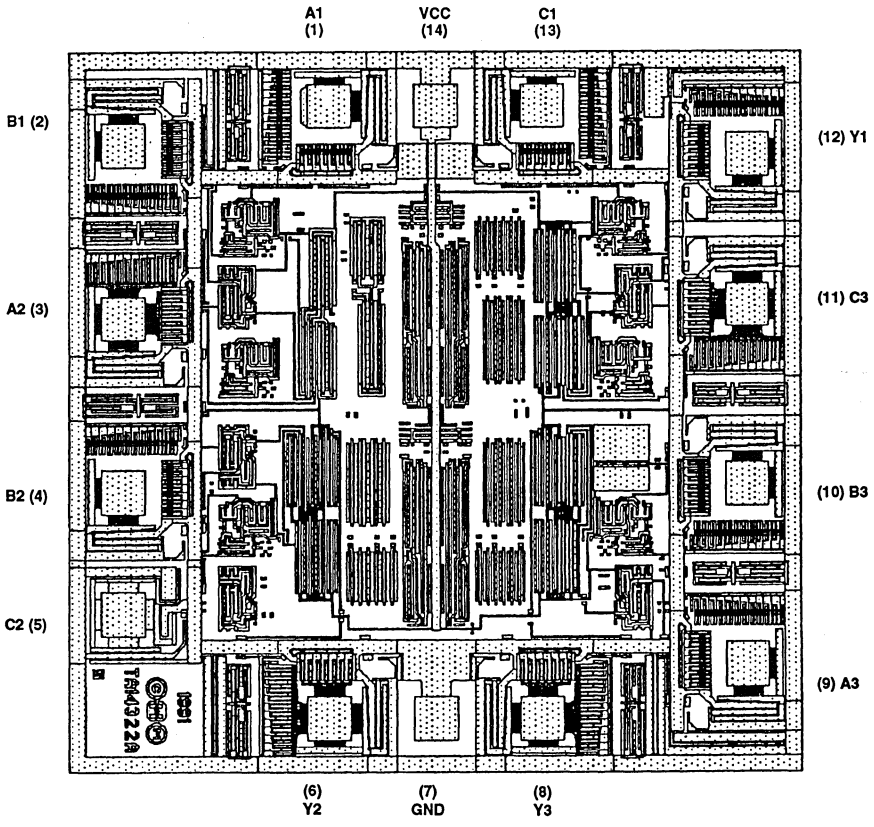
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS27MS



HARRIS SEMICONDUCTOR

HCTS30MS

Radiation Hardened 8-Input NAND Gate

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

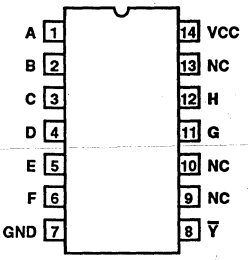
The Harris HCTS30MS is a Radiation Hardened 8-Input NAND Gate. A high on all input forces the output to a low state.

The HCTS30MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

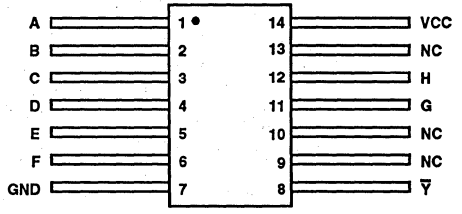
The HCTS30MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

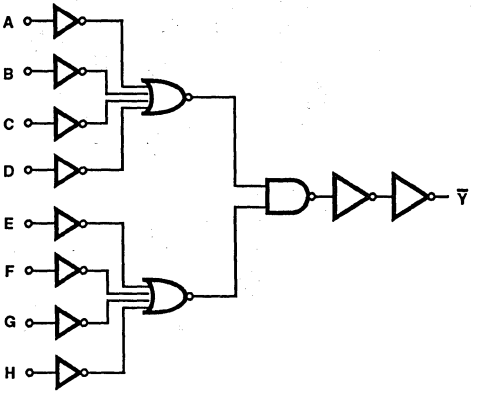


Truth Table

INPUTS								OUTPUTS
A	B	C	D	E	F	G	H	$\overline{Y}$
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

NOTE: L = Logic Level Low, H = Logic level High, X = Don't Care

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3056

Absolute Maximum Ratings

Supply Voltage (VCC) ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (tr, tf) ..... 100ns/V Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Output	TPHL	VCC = 4.5V	9	+25°C	2	22	ns
			10, 11	+125°C, -55°C	2	23	ns
	TPLH	VCC = 4.5V	9	+25°C	2	22	ns
			10, 11	+125°C, -55°C	2	25	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 70		pF
			1	+125°C	Typical 150		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 2.75V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 2.75V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Input to Output	TPHL	VCC = 4.5V	+25°C	2	23	2	37.5	ns
	TPLH	VCC = 4.5V	+25°C	2	25	2	37.5	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A inspection in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
8, 9, 10, 13	1 - 5, 6, 7, 11, 12	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
8, 9, 10, 13	7	-	1 - 5, 6, 11, 12, 14	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
9, 10, 13	7	8	14	1 - 5, 6, 11, 12	-

NOTE:

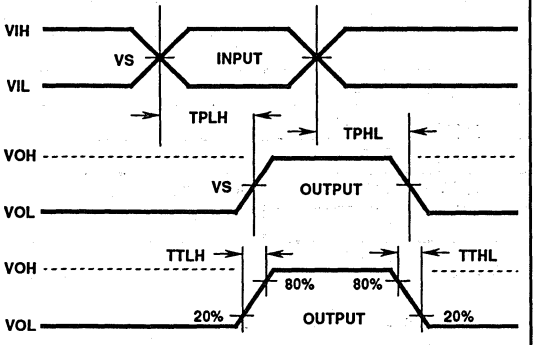
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
8, 9, 10, 13	7	1, 2, 3, 4, 5, 6, 11, 12, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

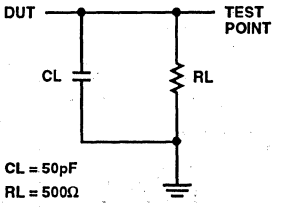
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
87 x 88 mils

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

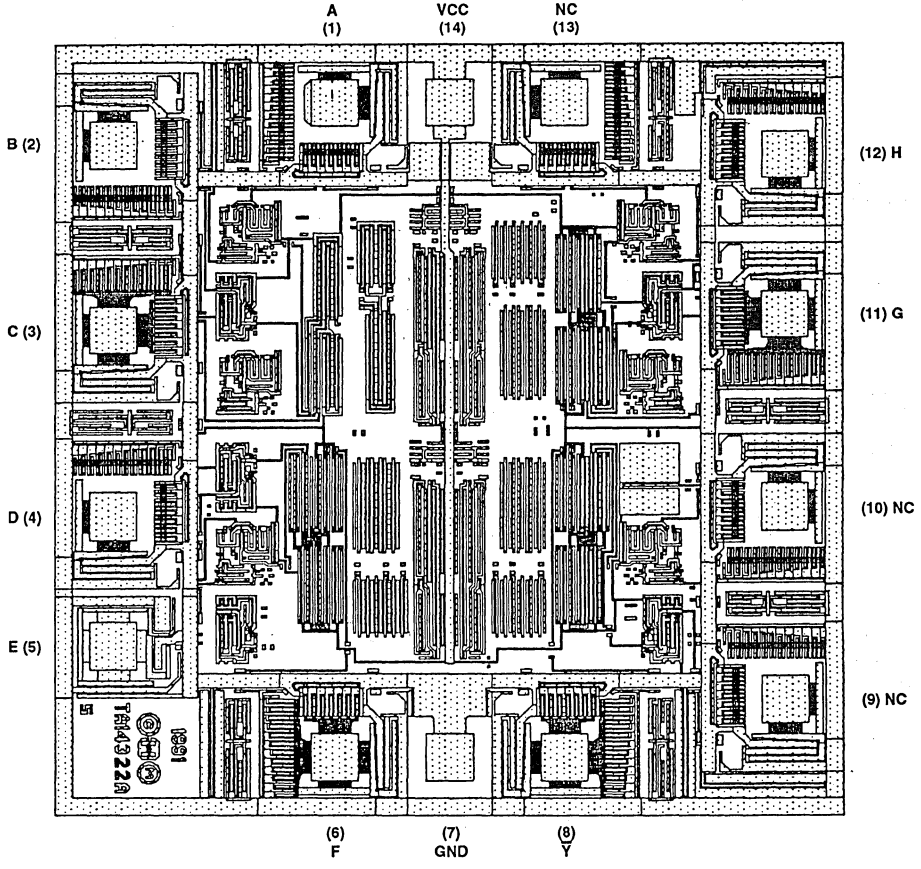
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS30MS



HARRIS SEMICONDUCTOR

HCS32MS

Radiation Hardened Quad 2-Input OR Gate

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity < 2 x 10^{-9} Errors/Gate Day (Typ)
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

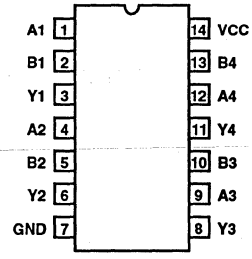
The Harris HCS32MS is a Radiation Hardened Quad 2-Input OR Gate. A low on both inputs forces the output to a High state.

The HCS32MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

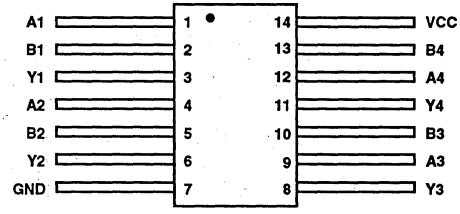
The HCS32MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

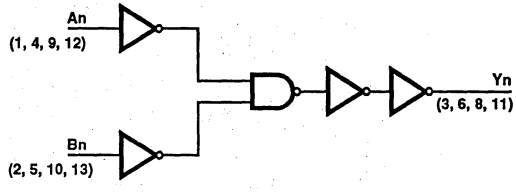


Truth Table

INPUTS		OUTPUTS
An	Bn	Yn
L	L	L
L	H	H
H	L	H
H	H	H

NOTE: L = Logic Level Low, H = Logic level High

Functional Diagram



File Number 3057

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 100ns/V Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 30% of VCC
Input High Voltage (VIH) ..... 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), (Note 2) VIL = 0.30(VCC)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Data to Output	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
Data to Output	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 4		pF
			1	+125°C	Typical 7		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Data to Output	TPHL	VCC = 4.5V	+25°C	2	20	2	25	ns
	TPLH	VCC = 4.5V	+25°C	2	22	2	26	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
3, 6, 8, 11	1, 2, 4, 5, 7, 9, 10, 12, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 6, 8, 11	7	-	1, 2, 4, 5, 9, 10, 12, 13, 14	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 2)					
-	7	3, 6, 8, 11	14	1, 2, 4, 5, 9, 10, 12, 13	-

NOTES:

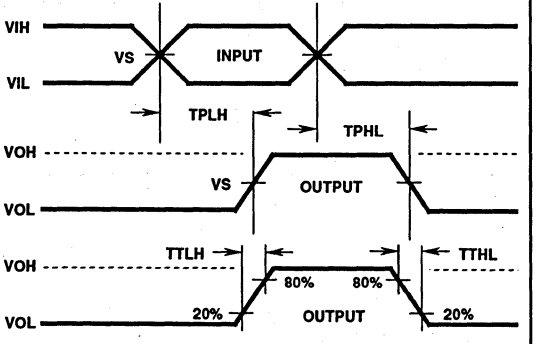
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 6, 8, 11	7	1, 2, 4, 5, 9, 10, 12, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

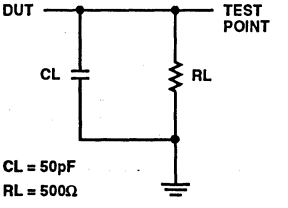
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2.20 x 2.24mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

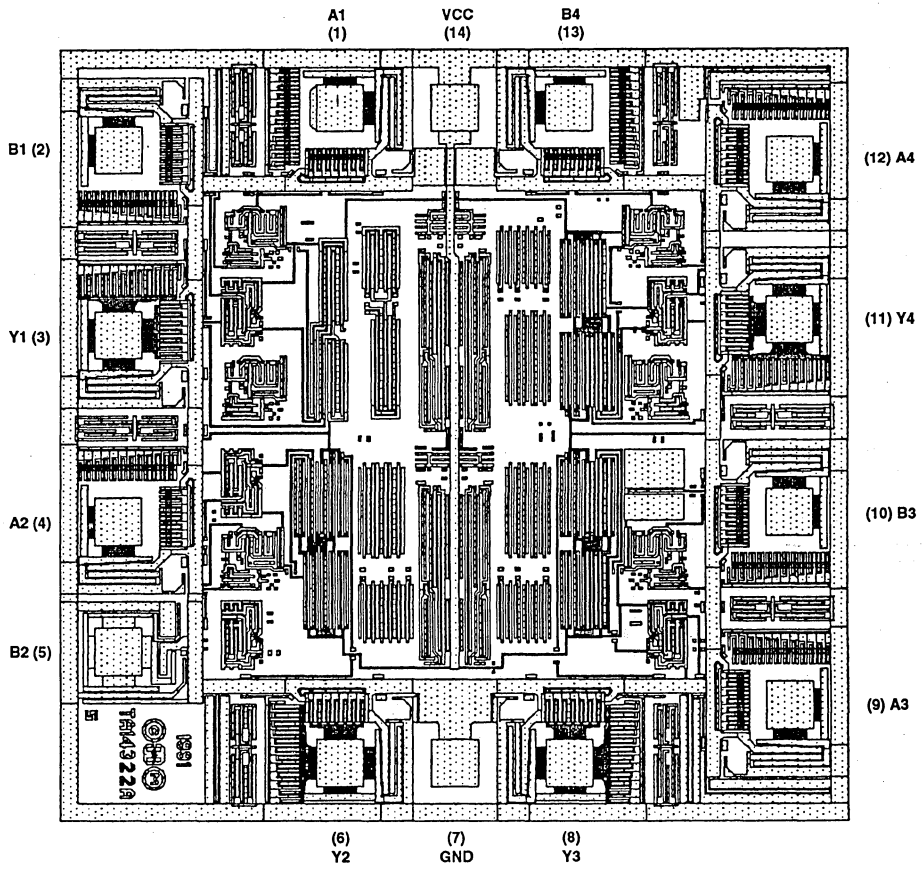
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCS32MS



HARRIS SEMICONDUCTOR

HCTS32MS

Radiation Hardened Quad 2-Input OR Gate

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA @ VOL, VOH

Description

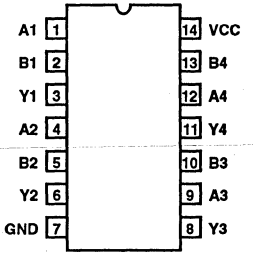
The Harris HCTS32MS is a Radiation Hardened Quad 2-Input OR Gate. A Low on all inputs forces the output to a Low state.

The HCTS32MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

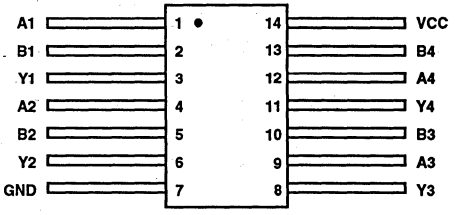
The HCTS32MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

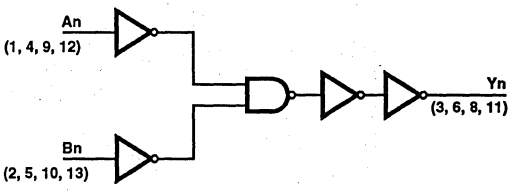


Truth Table

INPUTS		OUTPUTS
An	Bn	Yn
L	L	L
L	H	H
H	L	H
H	H	H

NOTE: L = Logic Level Low, H = Logic level High

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2248.1**

Absolute Maximum Ratings

Supply Voltage (VCC) ..... -0.5 to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC) ..... +4.5V to +5.5V
Input Rise and Fall Times at VCC = 4.5V (TR, TF) ... 100ns/V Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V (Note 3)	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V (Note 3)	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	0.5	µA
			2, 3	+125°C, -55°C	-5.0	5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".
3. Force/Measure functions may be interchanged.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Output	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
Input to Output	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input tr = tf = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 20		pF
			1	+125°C	Typical 30		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Input to Output	TPHL	VCC = 4.5V	+25°C	2	20	2	25	ns
	TPLH	VCC = 4.5V	+25°C	2	22	2	26	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A inspection in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
3, 6, 8, 11	1, 2, 4, 5, 7, 9, 10, 12, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 6, 8, 11	7	-	1, 2, 4, 5, 9, 10, 12, 13, 14	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	7	3, 6, 8, 11	14	1, 2, 4, 5, 9, 10, 12, 13	-

NOTES:

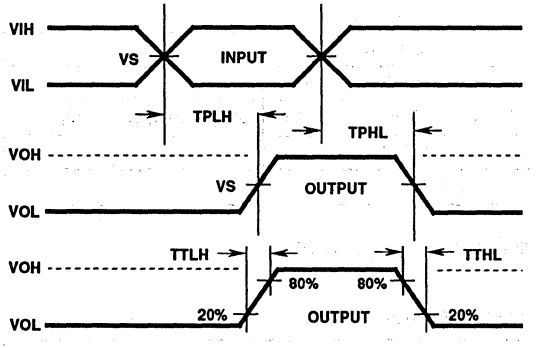
1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1kΩ ± 5% for dynamic burn-in

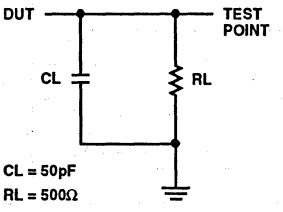
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 6, 8, 11	7	1, 2, 4, 5, 9, 10, 12, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

AC Timing Diagram and Load Circuit





AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2.20 x 2.2mm

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

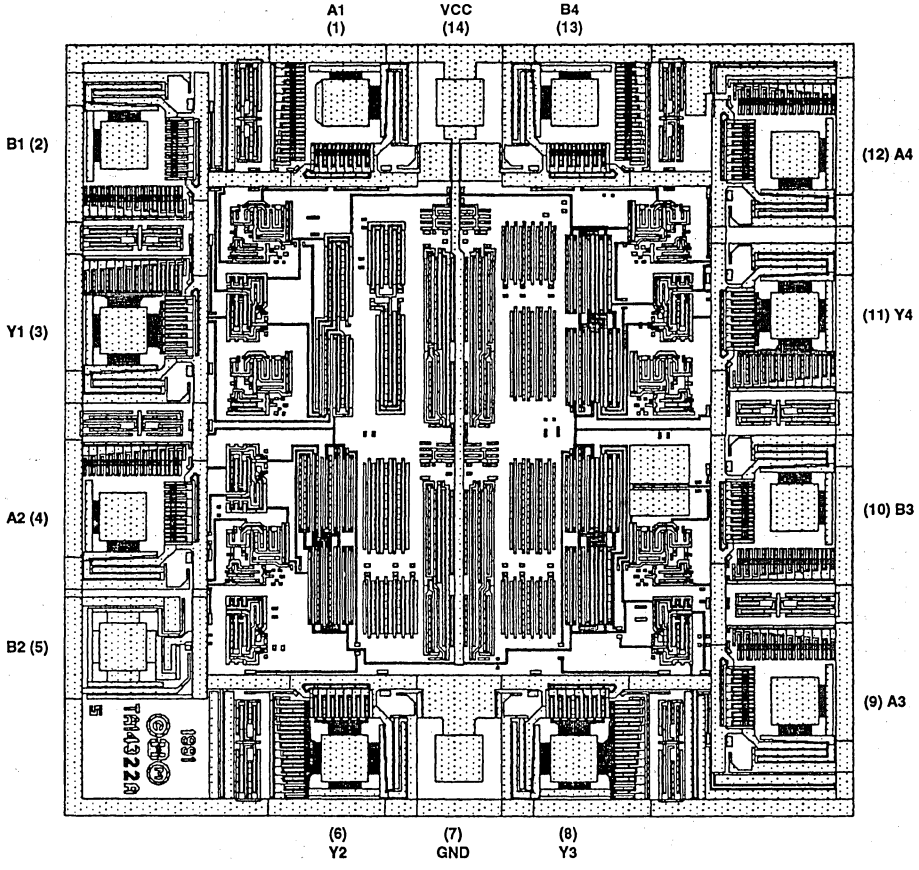
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCTS32MS



HARRIS SEMICONDUCTOR

HCS74MS

Radiation Hardened Dual-D Flip-Flop with Set and Reset

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity 2 x 10^{-9} Error/Bit Day (Typ)
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

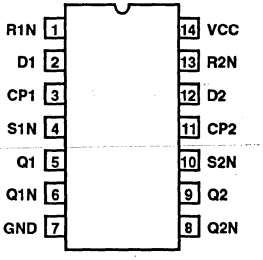
The Harris HCS74MS is a Radiation Hardened positive edge triggered flip-flop with set and reset.

The HCS74MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

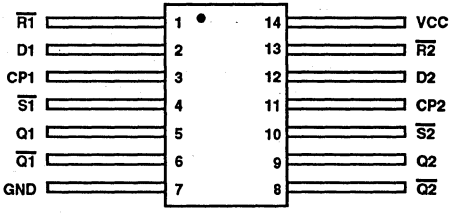
The HCS74MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW



Truth Table

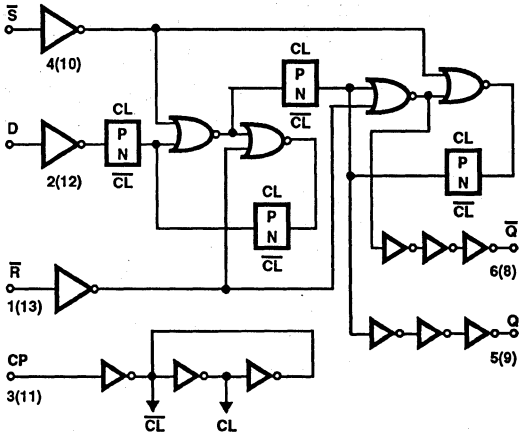
INPUTS				OUTPUTS	
SET	RESET	CP	D	Q	Q
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↗	H	H	L
H	H	↗	L	L	H
H	H	L	X	Q0	Q0

NOTE: L = Logic Level Low, H = Logic Level High, X = Don't Care
↗ = Transition from Low to High Level

Q0 = The level of Q before the indicated input conditions were established.

* This configuration is non-stable, that is, it will not persist when set and reset inputs return to their inactive (High) level.

Functional Diagram



File Number **2142.1**

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 100ns/V Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 30% of VCC
Input High Voltage (VIH) ..... 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	20	µA
			2, 3	+125°C, -55°C	-	400	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), (Note 2) VIL = 0.30(VCC)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CP to Q, $\overline{Q}$	TPHL	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	32	ns
	TPLH	VCC = 4.5V	9	+25°C	2	26	ns
			10, 11	+125°C, -55°C	2	31	ns
$\overline{S}$ to Q	TPLH	VCC = 4.5V	9	+25°C	2	26	ns
			10, 11	+125°C, -55°C	2	31	ns
$\overline{S}$ to $\overline{Q}$	TPHL	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	32	ns
$\overline{R}$ to Q	TPHL	VCC = 4.5V	9	+25°C	2	24	ns
			10, 11	+125°C, -55°C	2	29	ns
$\overline{R}$ to $\overline{Q}$	TPLH	VCC = 4.5V	9	+25°C	2	25	ns
			10, 11	+125°C, -55°C	2	30	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 35		pF
			1	+125°C	Typical 35		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns
Max Operating Frequency	FMAX	VCC = 4.5V	1	+25°C	-	30	MHz
			1	+125°C	-	20	MHz
Data to CP Set-up Time	TSU	VCC = 4.5V	1	+25°C	11	-	ns
			1	+125°C	12	-	ns
Hold Time	TH	VCC = 4.5V	1	+25°C	3	-	ns
			1	+125°C	3	-	ns
Removal Time $\overline{R}$, $\overline{S}$ to CP	TREM	VCC = 4.5V	1	+25°C	5	-	ns
			1	+125°C	6	-	ns
Pulse Width $\overline{R}$, $\overline{S}$	TW	VCC = 4.5V	1	+25°C	14	-	ns
			1	+125°C	16	-	ns
Pulse Width CP	TW	VCC = 4.5V	1	+25°C	14	-	ns
			1	+125°C	16	-	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.4	-	1.5	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
CP to Q, $\overline{Q}$	TPHL	VCC = 4.5V	+25°C	2	32	2	40	ns
	TPLH	VCC = 4.5V	+25°C	2	31	2	39	ns
$\overline{S}$ to Q	TPLH	VCC = 4.5V	+25°C	2	31	2	39	ns
$\overline{S}$ to $\overline{Q}$	TPHL	VCC = 4.5V	+25°C	2	32	2	40	ns
$\overline{R}$ to Q	TPHL	VCC = 4.5V	+25°C	2	29	2	37	ns
$\overline{R}$ to $\overline{Q}$	TPLH	VCC = 4.5V	+25°C	2	30	2	38	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	6µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
PDA	100%/5004	1, 7, 9, Deltas	

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	Subgroups 1, 2, 3, 9, 10, 11

NOTE: 1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
5, 6, 8, 91	1 - 4, 7, 10 - 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
5, 6, 8, 9	7	-	1, 2, 3, 4, 10, 11, 12, 13, 14	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 2)					
-	7	5, 6, 8, 9	1, 4, 10, 13, 14	3, 11	2, 12

NOTES:

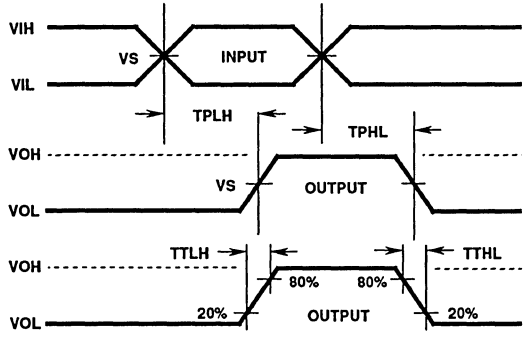
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in.

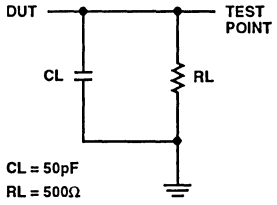
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
5, 6, 8, 9	7	1 - 4, 10 - 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

AC Timing Diagrams and AC Load Circuit

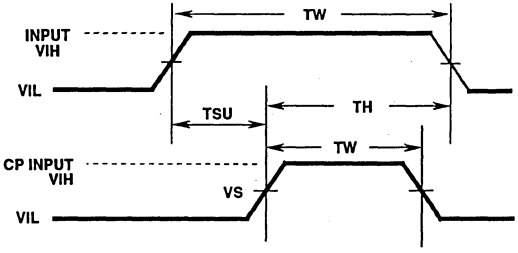




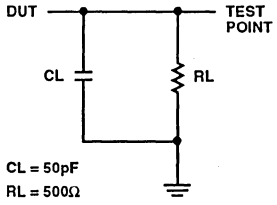
AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

Pulse Width, Setup, Hold Timing Diagram Positive Edge Trigger



TH = Hold Time
TSU = Setup Time
TW = Pulse Width



PULSE WIDTH, SETUP, HOLD VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
89 x 88 mils
2.25 x 2.24mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

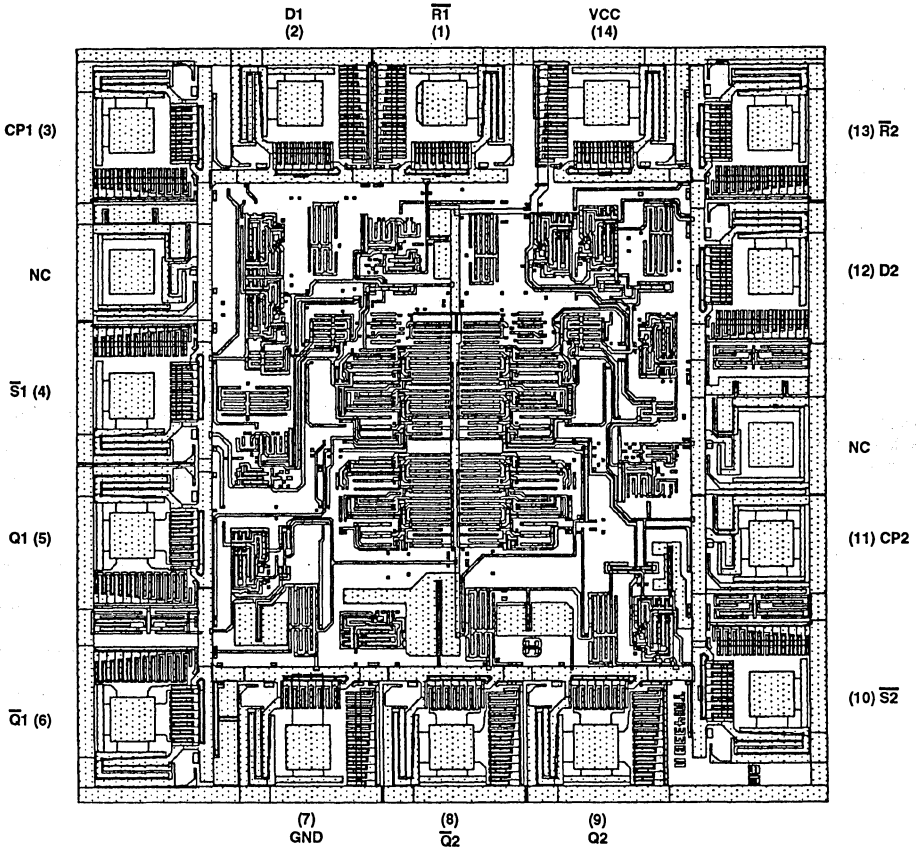
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCS74MS



HARRIS SEMICONDUCTOR

HCTS74MS

Radiation Hardened Dual-D Flip-Flop with Set and Reset

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Rate 2 x 10^{-9} Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

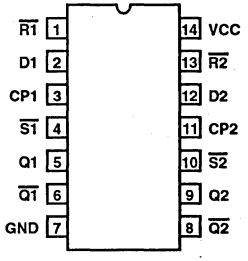
The Harris HCTS74MS is a Radiation Hardened positive edge triggered flip-flop with set and reset.

The HCTS74MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

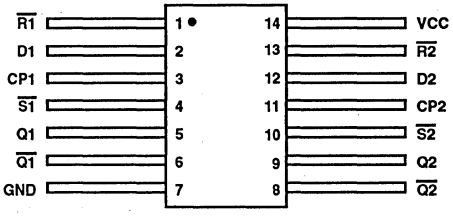
The HCTS74MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW



Truth Table

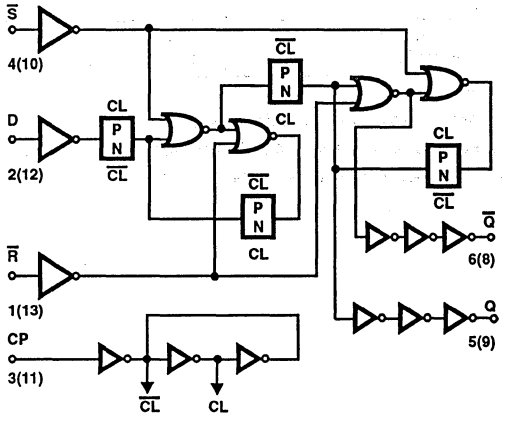
INPUTS				OUTPUTS	
$\overline{SET}$	$\overline{RESET}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q0}$

NOTE: L = Logic Level Low, H = Logic Level High, X = Don't Care
↑ = Transition from Low to High Level

Q0 = The level of Q before the indicated input conditions were established.

* This configuration is non-stable, that is, it will not persist when set and reset inputs return to their inactive (High) level.

Functional Diagram



7 LOGIC

File Number 2143.1

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input. . . . . ±10mA
DC Drain Current, Any One Output. . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Rise and Fall Times at VCC = 4.5V (TR, TF) . . 100ns/V Max.
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	20	µA
			2, 3	+125°C, -55°C	-	400	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".
3. Force/Measure functions may be interchanged.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CP to Q, $\overline{Q}$	TPHL	VCC = 4.5V	9	+25°C	2	31	ns
			10, 11	+125°C, -55°C	2	37	ns
	TPLH	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	31	ns
$\overline{S}$ to Q	TPLH	VCC = 4.5V	9	+25°C	2	21	ns
			10, 11	+125°C, -55°C	2	24	ns
$\overline{S}$ to $\overline{Q}$	TPHL	VCC = 4.5V	9	+25°C	2	33	ns
			10, 11	+125°C, -55°C	2	38	ns
$\overline{R}$ to Q	TPHL	VCC = 4.5V	9	+25°C	2	35	ns
			10, 11	+125°C, -55°C	2	40	ns
$\overline{R}$ to $\overline{Q}$	TPLH	VCC = 4.5V	9	+25°C	2	29	ns
			10, 11	+125°C, -55°C	2	34	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 35		pF
			1	+125°C	Typical 35		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns
Max Operating Frequency	FMAX	VCC = 4.5V	1	+25°C	-	25	MHz
			1	+125°C	-	16	MHz
Data to CP Set-up Time	TSU	VCC = 4.5V	1	+25°C	11	-	ns
			1	+125°C	12	-	ns
Hold Time	TH	VCC = 4.5V	1	+25°C	3	-	ns
			1	+125°C	3	-	ns
Removal Time $\overline{R}$, $\overline{S}$ to CP	TREM	VCC = 4.5V	1	+25°C	5	-	ns
			1	+125°C	6	-	ns
Pulse Width $\overline{R}$, $\overline{S}$	TW	VCC = 4.5V	1	+25°C	14	-	ns
			1	+125°C	16	-	ns
Pulse Width CP	TW	VCC = 4.5V	1	+25°C	14	-	ns
			1	+125°C	16	-	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.4	-	0.4	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
CP to Q, $\overline{Q}$	TPHL	VCC = 4.5V	+25°C	2	37	2	46	ns
	TPLH	VCC = 4.5V	+25°C	2	31	2	39	ns
$\overline{S}$ to Q	TPLH	VCC = 4.5V	+25°C	2	24	2	30	ns
$\overline{S}$ to $\overline{Q}$	TPHL	VCC = 4.5V	+25°C	2	38	2	48	ns
$\overline{R}$ to Q	TPHL	VCC = 4.5V	+25°C	2	40	2	50	ns
$\overline{R}$ to $\overline{Q}$	TPLH	VCC = 4.5V	+25°C	2	34	2	43	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	6µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
PDA	100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS					
5, 6, 8, 9	1, 2, 3, 4, 7, 10, 11, 12, 13		14		
STATIC BURN-IN II TEST CONNECTIONS					
5, 6, 8, 9	7		1, 2, 3, 4, 10, 11, 12, 13, 14		
DYNAMIC BURN-IN TEST CONNECTIONS					
-	7	5, 6, 8, 9	1, 4, 10, 13, 14	3, 11	2, 12

NOTES:

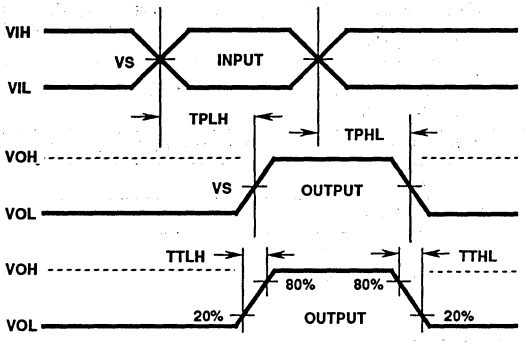
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in.

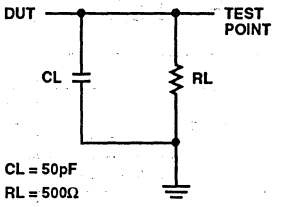
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
5, 6, 8, 9	7	1, 2, 3, 4, 10, 11, 12, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

AC Timing Diagrams and Load Circuit

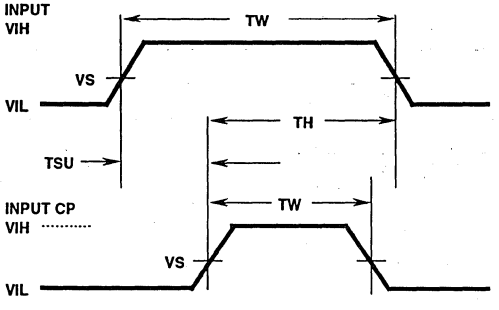




AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Pulse Width, Setup, Hold Timing Diagram Positive Edge Trigger



TH = HOLD TIME
TSU = SETUP TIME
TW = PULSE WIDTH

*VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
89 x 88 mils
2.25 x 2.24mm

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

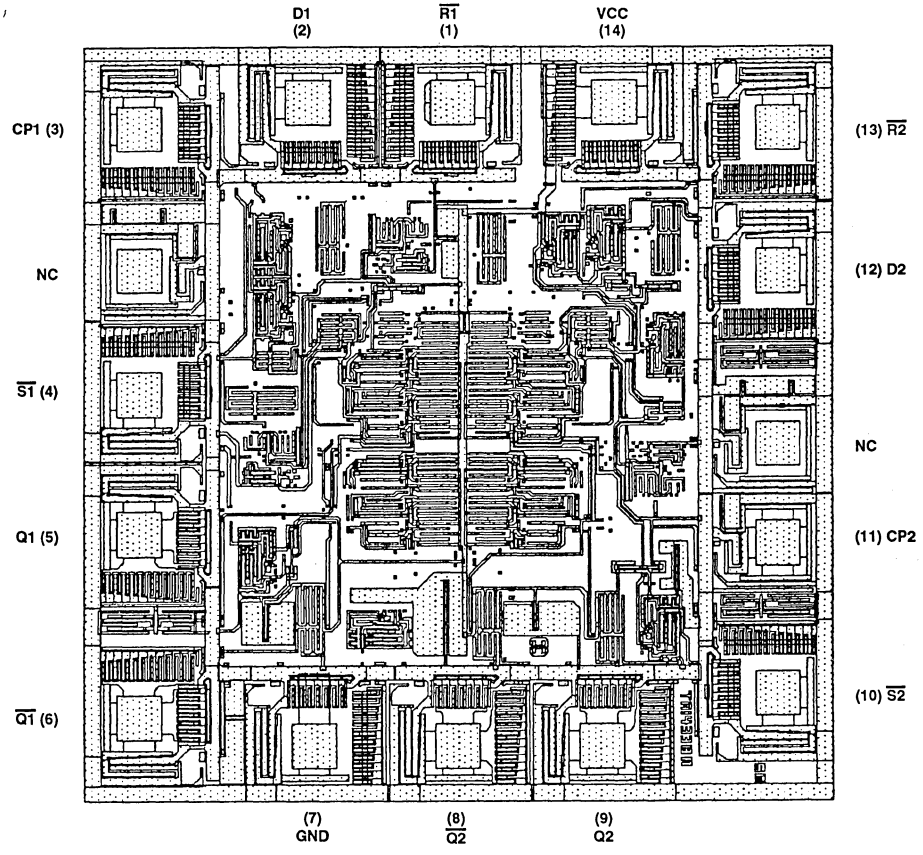
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS74MS



HARRIS SEMICONDUCTOR

HCTS75MS

Radiation Hardened Dual 2-Bit Bistable Transparent Latch

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD (Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range ..... -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range ..... 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

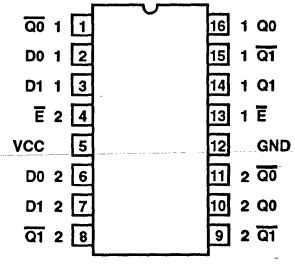
The Harris HCTS75MS is a Radiation Hardened dual 2-bit bistable transparent latch. Each of the two latches are controlled by a separate enable input ($\overline{E}$) which are active low. $\overline{E}$ low latches the output state.

The HCTS75MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

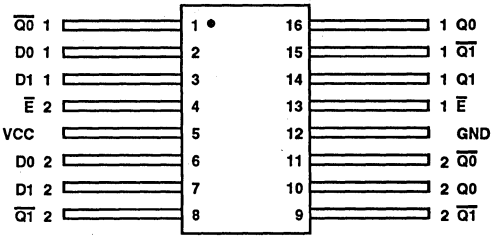
The HCTS75MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T16, LEAD FINISH C
TOP VIEW



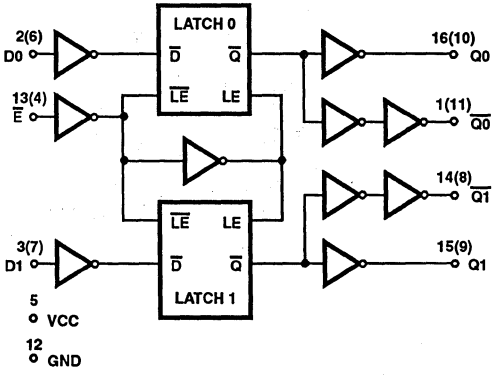
16 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F16, LEAD FINISH C
TOP VIEW



Truth Table

INPUTS		OUTPUTS	
D	E	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q0	$\overline{Q0}$

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3189

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Input Rise and Fall Times at VCC = 4.5V (TR, TF) . . . 100ns/V Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	20	µA
			2, 3	+125°C, -55°C	-	400	µA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 5.5V, VIH = 2.75V, VIL = 0.8V, IOL = 50µA	1, 2, 3	+25°C, +125°C, 55°C	-	0.1	V
		VCC = 4.5V, VIH = 2.25V, VIL = 0.8V, IOL = 50µA	1, 2, 3	+25°C, +125°C, 55°C	-	0.1	V
Output Voltage High	VOH	VCC = 5.5V, VIH = 2.75V, VIL = 0.8V, IOH = -50µA	1, 2, 3	+25°C, +125°C, 55°C	VCC -0.1	-	V
		VCC = 4.5V, VIH = 2.25V, VIL = 0.8V, IOH = -50µA	1, 2, 3	+25°C, +125°C, 55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	4.0	0.5	V

NOTES:
1. All voltages referenced to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay D to Q	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	19	ns
			10, 11	+125°C, -55°C	2	24	ns
	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	35	ns
Propagation Delay D to $\overline{Q}$	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	23	ns
			10, 11	+125°C, -55°C	2	29	ns
	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	19	ns
			10, 11	+125°C, -55°C	2	22	ns
Propagation Delay $\overline{E}$ to Q	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	21	ns
			10, 11	+125°C, -55°C	2	25	ns
	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	34	ns
Propagation Delay $\overline{E}$ to $\overline{Q}$	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	24	ns
			10, 11	+125°C, -55°C	2	29	ns
	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	23	ns

NOTES:

1. All voltages referenced to device GND.
2. Measurements made with RL = 500Ω, CL = 50pF, Input TR = TF = 3ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 24		pF
			1	+125°C	Typical 34		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Pulse Width Time	TW	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	-	16	ns
			1	+125°C	-	24	ns
Setup Time	TSU	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	-	12	ns
			1	+125°C	-	18	ns
Hold Time	TH	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	-	12	ns
			1	+125°C	-	18	ns
Output Transition Time	TTHL, TTLH	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C		15	ns
			1	+125°C		22	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	200K RAD LIMITS		1MEG RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.4	-	1.5	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 5.5V, VIH = 2.75V, VIL = 0.8V at 200k RAD, 0.3V at 1M RAD IOL = 50µA	+25°C	-	0.1	-	0.1	V
		VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200k RAD, 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 5.5V, VIH = 2.75V, VIL = 0.8Vat 200k RAD, 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
		VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200k RAD, 0.3V at 1M RAD IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200k RAD, 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	
Propagation Delay D to Q	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	35	2	TBD	ns
	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	24	2	TBD	ns
Propagation Delay D to $\overline{Q}$	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	22	2	TBD	ns
	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	29	2	TBD	ns
Propagation Delay $\overline{E}$ to Q	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	34	2	TBD	ns
	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	25	2	TBD	ns
Propagation Delay E to $\overline{Q}$	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	23	2	TBD	ns
	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	29	2	TBD	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	±6μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A inspection in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
1, 8, 9, 10, 11, 14, 15, 16	2, 3, 4, 6, 7, 12, 13	-	5	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
1, 8, 9, 10, 11, 14, 15, 16	12	-	2, 3, 4, 5, 6, 7, 13	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	12	1, 8, 9, 10, 11, 14, 15, 16	5	4, 13	2, 3, 6, 7

NOTES:

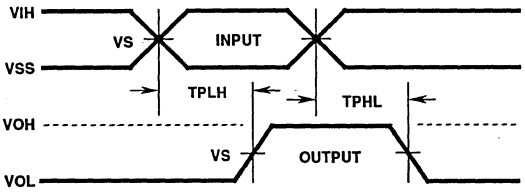
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in

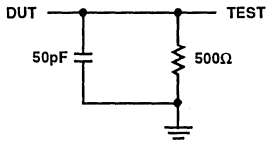
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
1, 8, 9, 10, 11, 14, 15, 16	12	2, 3, 4, 5, 6, 7, 13

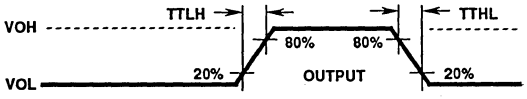
NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

Propagation Delay Timing Diagram and Load Circuit





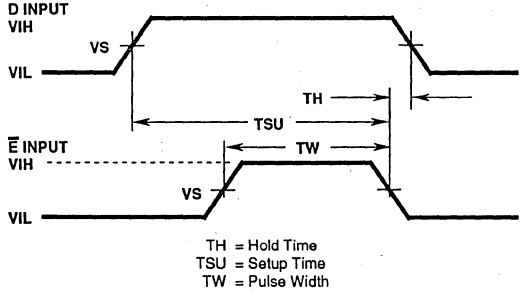
Transition Timing Diagram

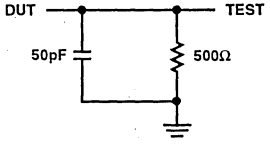


VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Pulse Width, Setup, Hold Timing Diagram and Load Circuit

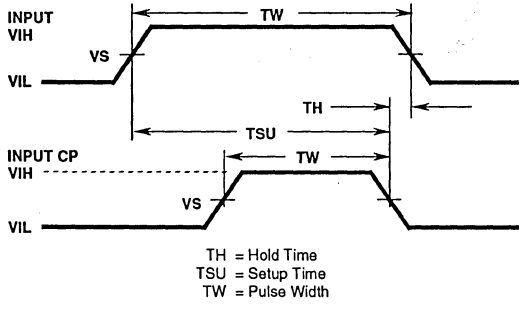


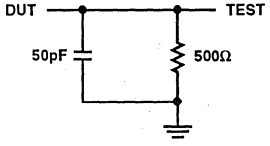


VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

Pulse Width, Setup, Hold Timing Diagram Negative Edge Trigger and Load Circuit





VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
89 x 88 mils
2.25 x 2.24mm

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

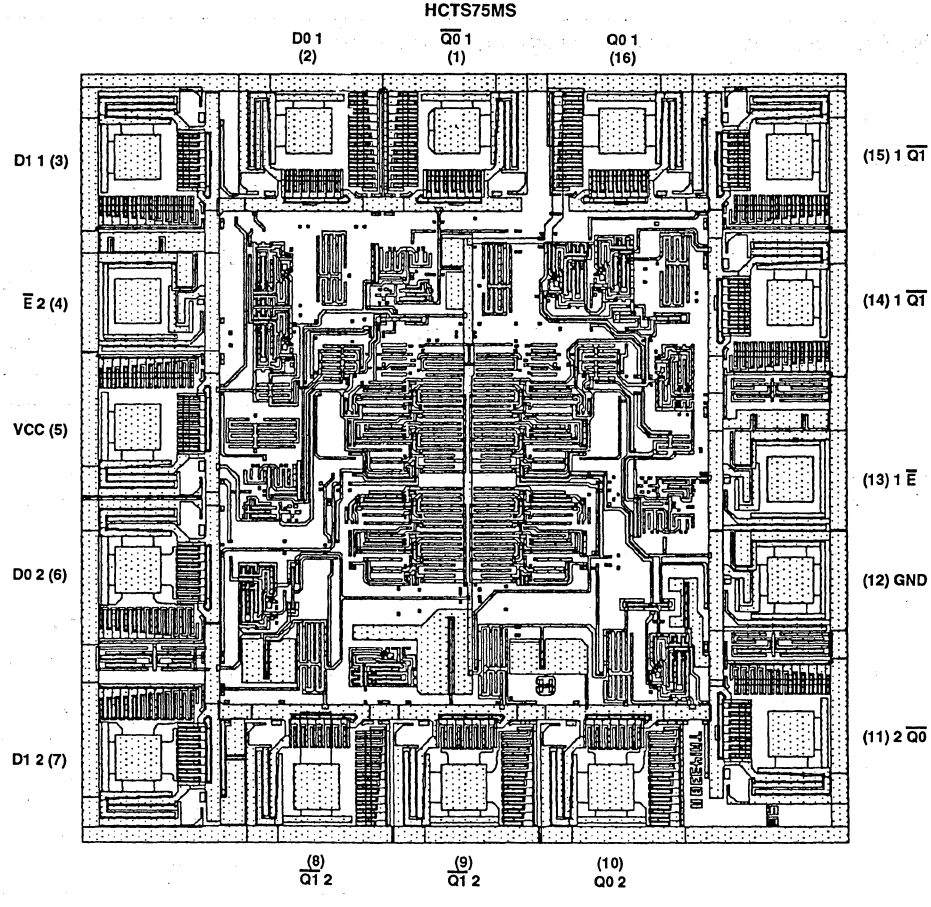
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HCTS85MS

Radiation Hardened 4-Bit Magnitude Comparator

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD (Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Rate < 2 x 10^{-9} Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
- Military Temperature Range . . . . . -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range . . . . . 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

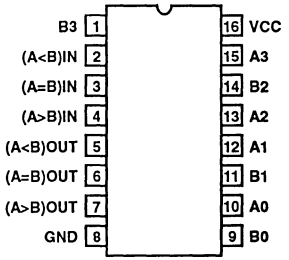
The Harris HCTS85MS is a Radiation Hardened 4-bit high speed magnitude comparator. This device compares two binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs (A>B, A<B, and A=B). The 4-bit input words are weighted (A0 to A3 and B0 to B3), where A3 and B3 are the most significant bits. The HCTS85MS is expandable without external gating, both serial and parallel operation.

The HCTS85MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family with TTL input compatibility.

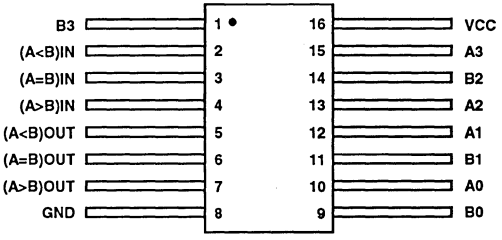
The HCTS85MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F16, LEAD FINISH C
TOP VIEW



7 LOGIC

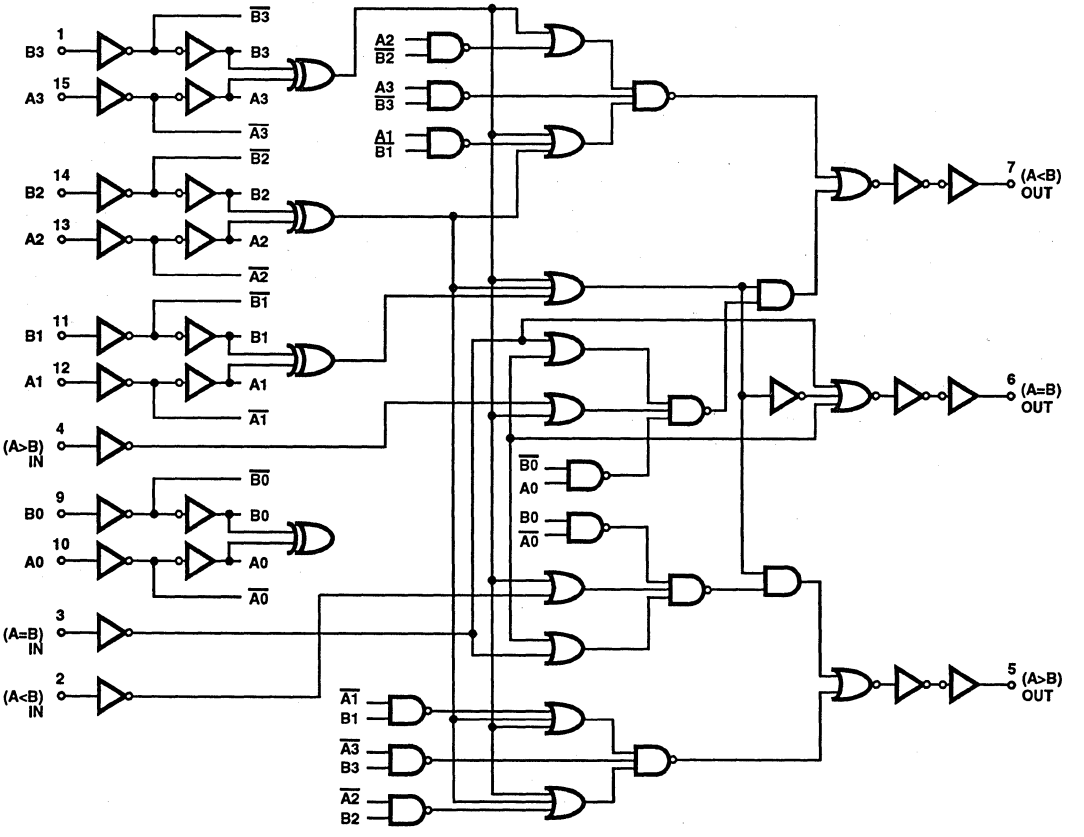
File Number 3059

Truth Table

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS			
A3, B3	A2, B2	A1, B1	A0, B0	A>B	A<B	A=B	A>B	A<B	A=B	
A3>B3	X	X	X	X	X	X	H	L	L	Single Device OR Series Cascading
A3<B3	X	X	X	X	X	X	L	H	L	
A3=B3	A2>B2	X	X	X	X	X	H	L	L	
A3=B3	A2<B2	X	X	X	X	X	L	H	L	
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L	
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L	
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L	
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L	
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L	
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L	
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H	
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H	
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L	Parallel Cascading
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L	

NOTE: L = Logic Level Low, H = Logic Level High, x = Immaterial

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Rise and Fall Times at VCC = 4.5V (TR, TF) . . . . 500ns Max.
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . 2.0V to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
An to (A>B)OUT	TPHL, TPLH	VCC = 4.5V	9	+25°C	2	36	ns
			10, 11	+125°C, -55°C	2	43	ns
Bn to (A>B)OUT	TPHL, TPLH	VCC = 4.5V	9	+25°C	2	57	ns
			10, 11	+125°C, -55°C	2	66	ns
An, Bn to (A<B)OUT	TPHL, TPLH	VCC = 4.5V	9	+25°C	2	45	ns
			10, 11	+125°C, -55°C	2	51	ns
An, Bn to (A=B)OUT	TPHL, TPLH	VCC = 4.5V	9	+25°C	2	42	ns
			10, 11	+125°C, -55°C	2	50	ns
An, Bn to (A>B)OUT	TPHL, TPLH	VCC = 4.5V	9	+25°C	2	29	ns
			10, 11	+125°C, -55°C	2	35	ns
(A>B)IN to (A>B)OUT	TPHL, TPLH	VCC = 4.5V	9	+25°C	2	34	ns
			10, 11	+125°C, -55°C	2	39	ns
(A=B)IN to (A=B)OUT	TPHL, TPLH	VCC = 4.5V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	37	ns
(A<B)IN to (A<B)OUT	TPHL, TPLH	VCC = 4.5V	9	+25°C	2	29	ns
			10, 11	+125°C, -55°C	2	35	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 26		pF
			1	+125°C, -55°C	Typical 61		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C, -55°C	-	10	pF
Output Transition Time	TTHL, TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C, -55°C	-	22	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.750	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
An to (A>B)OUT	TPHL, TPLH	VCC = 4.5V	+25°C	2	43	2	82	ns
Bn to (A>B)OUT	TPHL, TPLH	VCC = 4.5V	+25°C	2	66	2	48	ns
An, Bn to (A<B)OUT	TPHL, TPLH	VCC = 4.5V	+25°C	2	51	2	63	ns
An, Bn to (A=B)OUT	TPHL, TPLH	VCC = 4.5V	+25°C	2	50	2	62	ns
(A<B)IN to (A<B)OUT	TPHL, TPLH	VCC = 4.5V	+25°C	2	35	2	43	ns
(A>B)IN to (A>B)OUT	TPHL, TPLH	VCC = 4.5V	+25°C	2	39	2	48	ns
(A=B)IN to (A=B)OUT	TPHL, TPLH	VCC = 4.5V	+25°C	2	37	2	41	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

				OSCILLATOR	
OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
5, 6, 7	1 - 4, 8 - 15	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
5, 6, 7	8	-	1 - 4, 9 - 16	-	-
DYNAMIC BURN-IN TEST CONDITIONS (Note 2)					
-	1, 8, 10, 11, 13	5, 6, 7	2, 3, 4, 16	12, 15	9, 14

NOTES:

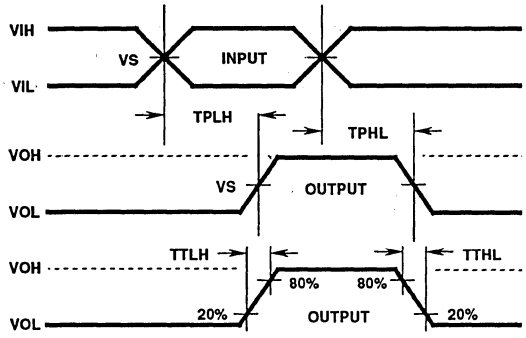
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in.

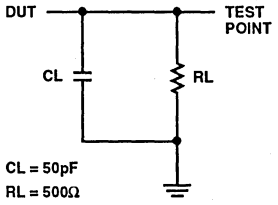
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
5, 6, 7,	8	1 - 4, 9 - 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

AC Timing Diagrams and Load Circuit





AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
100 x 100 mils

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

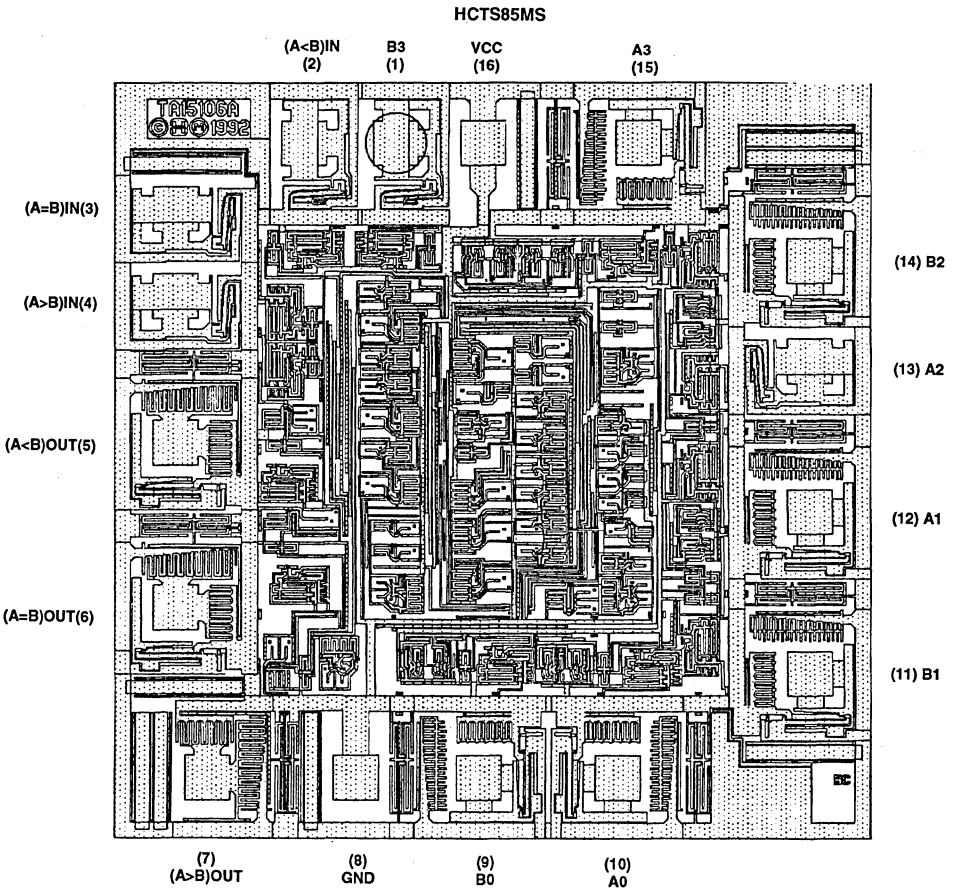
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HCS86MS

Radiation Hardened Quad 2-Input Exclusive OR Gate

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity < 2 x 10^{-9} Errors/Gate Day (Typ)
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

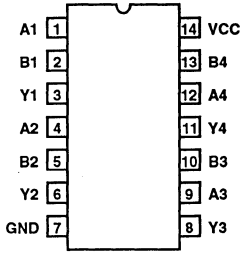
The Harris HCS86MS is a Radiation Hardened Quad 2-Input Exclusive OR Gate. A high on any one input exclusively will change the output to a High state.

The HCS86MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family with either TTL or CMOS input compatibility.

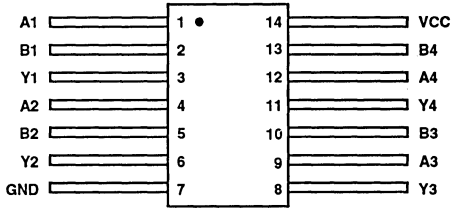
The HCS86MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-183S, DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-183S, DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

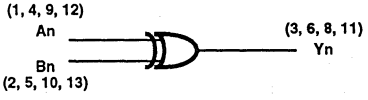


Truth Table

INPUTS		OUTPUTS
An	Bn	Yn
L	L	L
L	H	H
H	L	H
H	H	L

NOTE: L = Logic Level Low, H = Logic level High

Functional Diagram



7 LOGIC

File Number 3058

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 100ns/V Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 30% of VCC
Input High Voltage (VIH) ..... 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), (Note 2) VIL = 0.30(VCC)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Data to Input	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
Data to Input	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 22		pF
			1	+125°C	Typical 36		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	μA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Data to Output	TPHL	VCC = 4.5V	+25°C	2	20	2	25	ns
	TPLH	VCC = 4.5V	+25°C	2	22	2	26	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
3, 6, 8, 11	1, 2, 4, 5, 7, 9, 10, 12, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 6, 8, 11	7	-	1, 2, 4, 5, 9, 10, 12, 13, 14	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 2)					
-	7	3, 6, 8, 11	14	1, 2, 4, 5, 9, 10, 12, 13	-

NOTES:

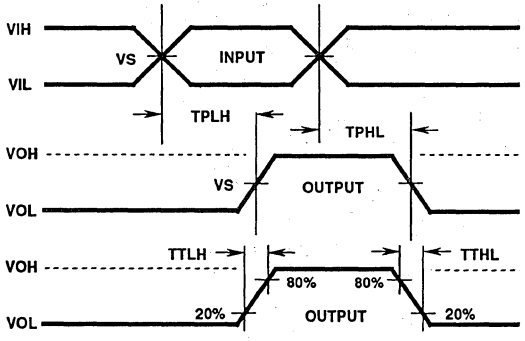
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 6, 8, 11	7	1, 2, 4, 5, 9, 10, 12, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

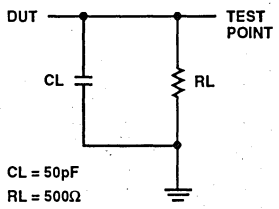
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

AC Load Circuit



7 LOGIC

Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2.20 x 2.24mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

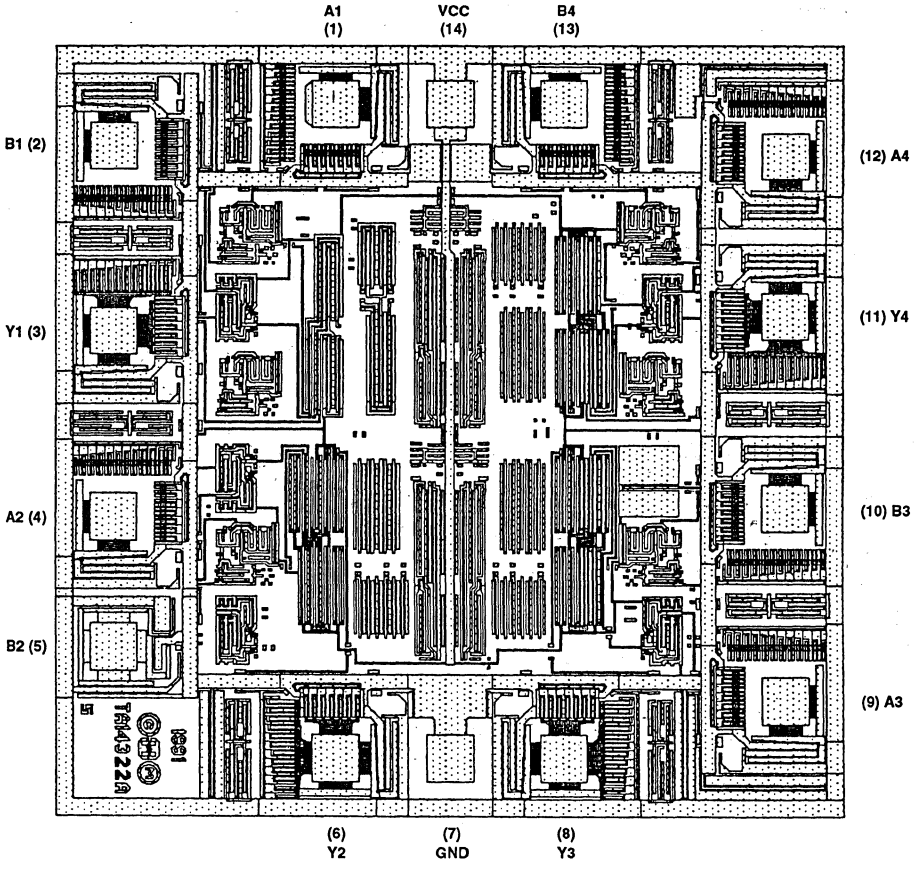
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCS86MS



HARRIS SEMICONDUCTOR

HCTS86MS

Radiation Hardened Quad 2-Input Exclusive OR Gate

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

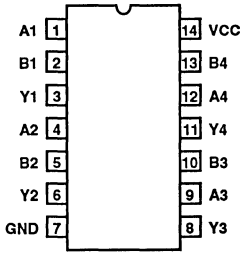
The Harris HCTS86MS is a Radiation Hardened Quad 2-Input Exclusive OR Gate. A high on any one input exclusively will change the output to a High state.

The HCTS86MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

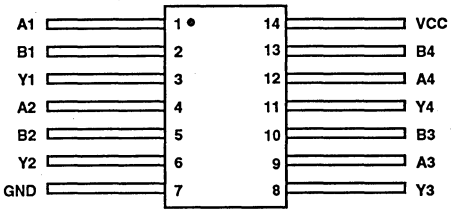
The HCTS86MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835, DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835, DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

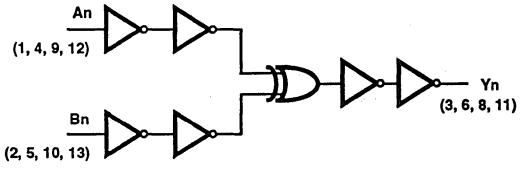


Truth Table

INPUTS		OUTPUTS
An	Bn	Yn
L	L	L
L	H	H
H	L	H
H	H	L

NOTE: L = Logic Level Low, H = Logic level High

Functional Diagram



7 LOGIC

File Number 2249.1

Absolute Maximum Ratings

Supply Voltage (VCC) ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC) ..... +4.5V to +5.5V
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Rise and Fall Times at VCC = 4.5 (TR, TF) ..... 100ns/V Max
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Output	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 24		pF
			1	+125°C	Typical 34		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Input to Output	TPHL	VCC = 4.5V	+25°C	2	20	2	25	ns
	TPLH	VCC = 4.5V	+25°C	2	22	2	26	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A testing in accordance with method 5005 of MIL-STD-883 may be excercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
3, 6, 8, 11	1, 2, 4, 5, 7, 9, 10, 12, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 6, 8, 11	7	-	1, 2, 4, 5, 9, 10, 12, 13, 14	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	7	3, 6, 8, 11	14	1, 2, 4, 5, 9, 10, 12, 13	-

NOTES:

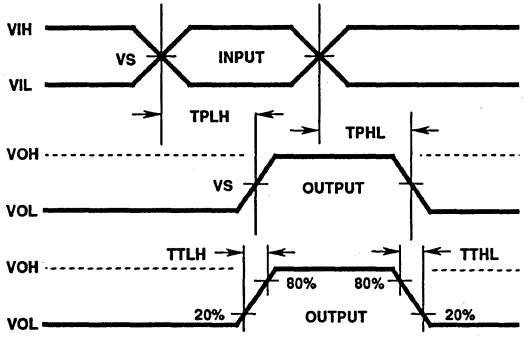
1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 6, 8, 11	7	1, 2, 4, 5, 9, 10, 12, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

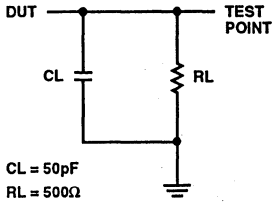
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



7 LOGIC

Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2.20 x 2.24 (mm)

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

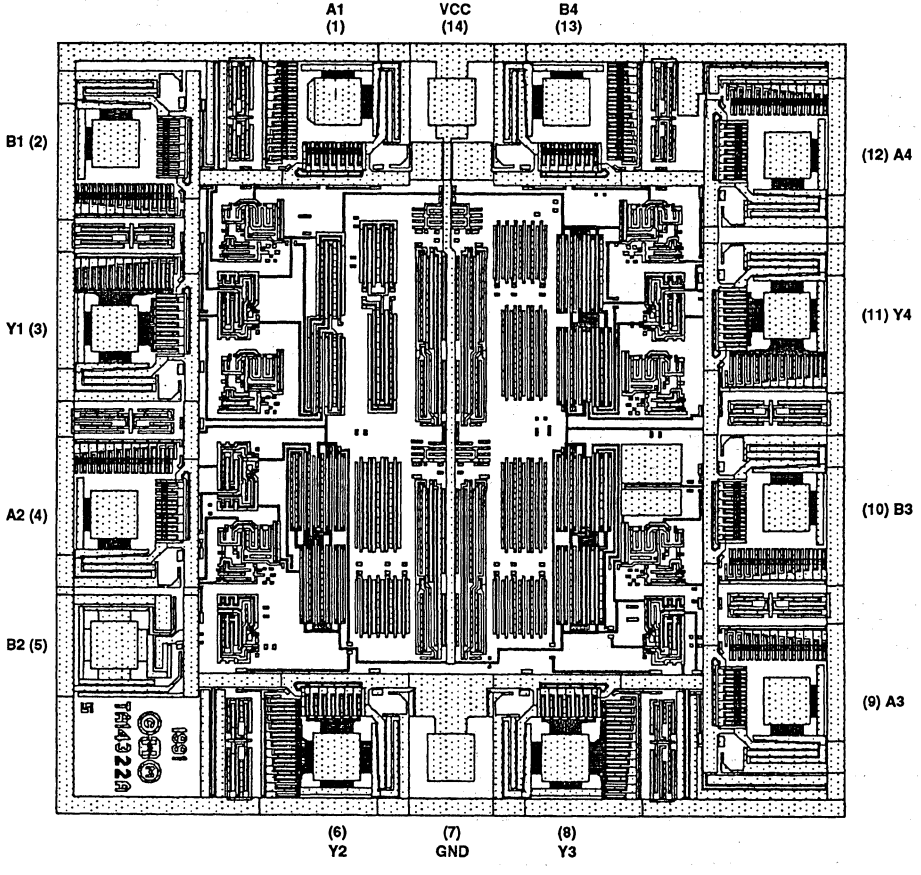
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS86MS



HARRIS SEMICONDUCTOR

HCTS93MS

Radiation Hardened 4-Bit Binary Ripple Counter

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD (Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Rate 2 x 10^{-9} Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Military Temperature Range ..... -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range ..... 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

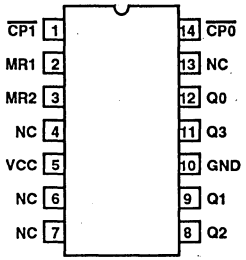
The Harris HCTS93MS is a Radiation Hardened 4-bit binary ripple counter consisting of four master-slave flip-flops internally connected to provide a divide-by-two and a divide-by-eight section. Each section has a separate clock input.

The HCTS93MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

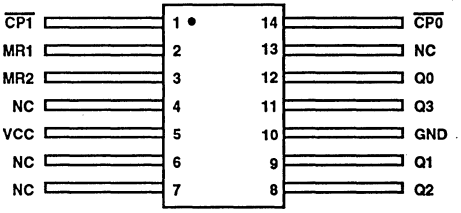
The HCTS93MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835, DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835, DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW



7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3060

Truth Table

COUNT	OUTPUTS			
	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

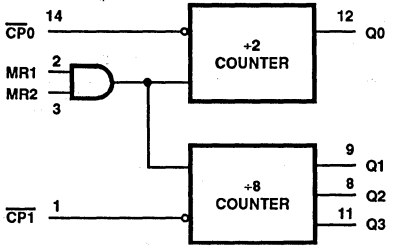
Mode Selection Table

RESET INPUTS		OUTPUTS			
MR1	MR2	Q0	Q1	Q2	Q3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

NOTE:

H = HIGH Voltage Level
L = LOW Voltage Level
Q0 Connected to $\overline{CP0}$

Functional Diagram



VCC = 5
GND = 10

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Rise and Fall Times at VCC = 4.5V (TR, TF) . . . 100ns/V Max
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	20	µA
			2, 3	+125°C, -55°C	-	400	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
$\overline{CP0}$ to Q0	TPHL	VCC = 4.5V	9	+25°C	2	32	ns
			10, 11	+125°C, -55°C	2	39	ns
	TPLH	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	33	ns
$\overline{CP1}$ to Q1	TPHL	VCC = 4.5V	9	+25°C	2	32	ns
			10, 11	+125°C, -55°C	2	39	ns
	TPLH	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	33	ns
$\overline{CP1}$ to Q2	TPHL	VCC = 4.5V	9	+25°C	2	39	ns
			10, 11	+125°C, -55°C	2	47	ns
	TPLH	VCC = 4.5V	9	+25°C	2	32	ns
			10, 11	+125°C, -55°C	2	39	ns
$\overline{CP1}$ to Q3	TPHL	VCC = 4.5V	9	+25°C	2	42	ns
			10, 11	+125°C, -55°C	2	51	ns
	TPLH	VCC = 4.5V	9	+25°C	2	36	ns
			10, 11	+125°C, -55°C	2	44	ns
MRn to Qn	TPHL	VCC = 4.5V	9	+25°C	2	33	ns
			10, 11	+125°C, -55°C	2	40	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 26		pF
			1	+125°C	Typical 66		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL, TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C, -55°C	-	22	ns
Max Clock Frequency	FMAX	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	30	-	MHz
			1	+125°C	20	-	MHz
Pulse Width $\overline{CP0}$, $\overline{CP1}$	TW	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	16	-	ns
			1	+125°C	24	-	ns
Reset Pulse Width	TW	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	16	-	ns
			1	+125°C	24	-	ns
Reset Removal Time	TREM	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	10	-	ns
			1	+125°C	15	-	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.4	-	1.5	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	4.0	0.5	4.0	0.5	V
$\overline{CP0}$ to Q0	TPHL	VCC = 4.5V	+25°C	2	39	2	49	ns
	TPLH	VCC = 4.5V	+25°C	2	33	2	42	ns
$\overline{CP1}$ to Q1	TPHL	VCC = 4.5V	+25°C	2	39	2	49	ns
	TPLH	VCC = 4.5V	+25°C	2	33	2	42	ns
$\overline{CP1}$ to Q2	TPHL	VCC = 4.5V	+25°C	2	47	2	59	ns
	TPLH	VCC = 4.5V	+25°C	2	39	2	49	ns
$\overline{CP1}$ to Q3	TPHL	VCC = 4.5V	+25°C	2	51	2	64	ns
	TPLH	VCC = 4.5V	+25°C	2	44	2	55	ns
MRn to Qn	TPHL	VCC = 4.5V	+25°C	2	40	2	50	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	6μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/IOH
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of Mil-Std-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN Test Which will be performed 100% go/no-go

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC I BURN-IN (Note 1)					
4, 6, 7, 8, 9, 11, 12, 13	1, 2, 3, 10, 14	-	5	-	-
STATIC II BURN-IN (Note 1)					
4, 6, 7, 8, 9, 11, 12, 13	10	-	1, 2, 3, 5, 14	-	-
DYNAMIC BURN-IN (Note 2)					
4, 6, 7, 13	2, 3, 10	8, 9, 11, 12	5	14	1

NOTES:

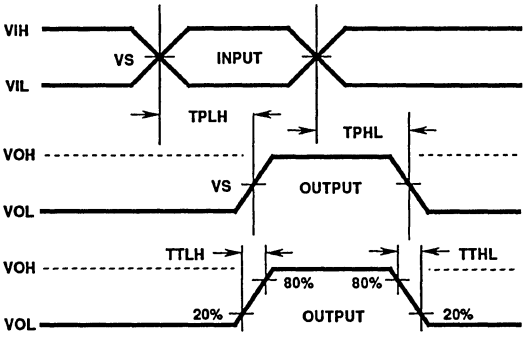
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in

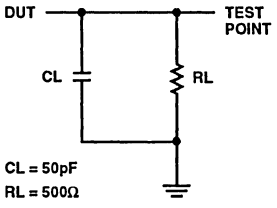
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
4, 6, 7, 8, 9, 11, 12, 13	10	1, 2, 3, 5, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

AC Timing Diagrams and Load Circuit

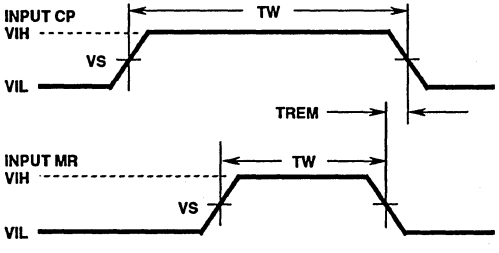




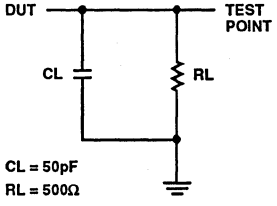
AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Pulse Width, Removal Timing Diagram Negative Edge Trigger and Load Circuit



TREM = Removal Time
TW = Pulse Width



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.5	V
VIH	3.0	V
VS	1.3	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
89 x 88 mils
2.25mm x 2.24mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

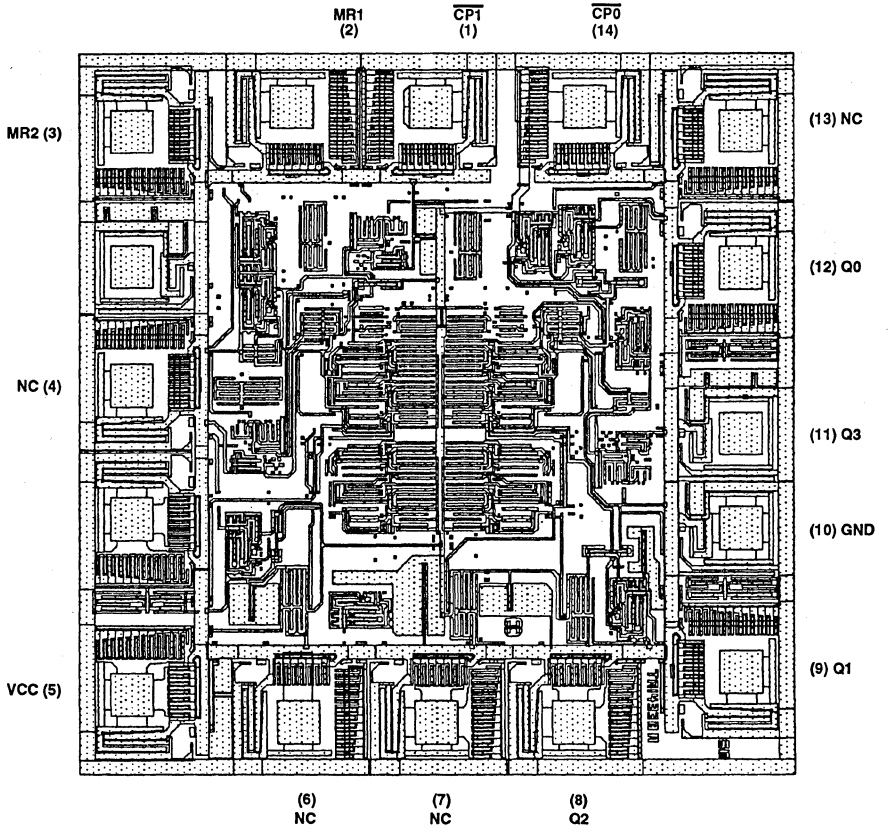
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS93MS



HARRIS SEMICONDUCTOR

HCS109MS

Radiation Hardened Dual JK Flip Flop

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity < 2 x 10^{-9} Errors/Bit Day (Typ)
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

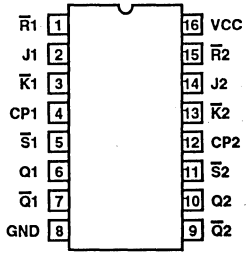
The Harris HCS109MS is a Radiation Hardened Dual JK Flip Flop with set and reset. The flip flop changes state with the positive transition of the clock (CP1 or CP2).

The HCS109MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

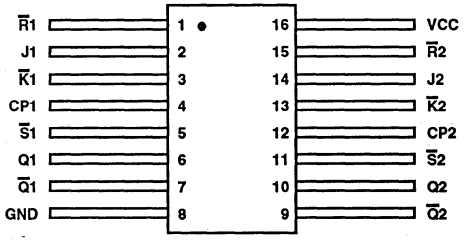
The HCS109MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-183S, DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-183S, DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

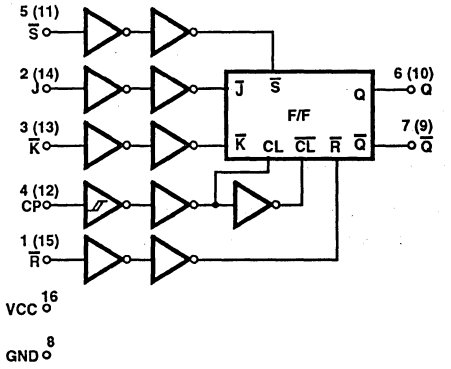


Truth Table

INPUTS					OUTPUTS	
$\overline{S}$	$\overline{R}$	CP	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↗	L	L	L	H
H	H	↗	H	L	Toggle	
H	H	↗	L	H	No Change	
H	H	↗	H	H	H	L
H	H	L	X	X	No Change	

*Unpredictable and unstable condition if both S and R go high simultaneously
L = Logic Level Low
H = Logic Level High
↗ = Transition from Low to High Level

Functional Diagram



7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2466.1**

Absolute Maximum Ratings

Supply Voltage . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input. . . . . ±10mA
DC Drain Current, Any One Output. . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5 VCC (TR, TF) . . . . . 500ns Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL). . . . . 0.0V to 30% of VCC
Input High Voltage (VIH) . . . . . 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	20	µA
			2, 3	+125°C, -55°C	-	400	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CP to Q, $\overline{Q}$	TPLH	VCC = 4.5V	9	+25°C	2	26	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	30	ns
	TPHL	VCC = 4.5V	9	+25°C	2	30	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	35	ns
$\overline{S}$ to Q	TPLH	VCC = 4.5V	9	+25°C	2	19	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	23	ns
$\overline{S}$ to $\overline{Q}$	TPHL	VCC = 4.5V	9	+25°C	2	31	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	33	ns
$\overline{R}$ to Q	TPHL	VCC = 4.5V	9	+25°C	2	31	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	33	ns
$\overline{R}$ to $\overline{Q}$	TPLH	VCC = 4.5V	9	+25°C	2	31	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	33	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 27		pF
			1	+125°C	Typical 37		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns
Max Operating Frequency	FMAX	VCC = 4.5V	1	+25°C	-	30	MHz
			1	+125°C	-	20	MHz
Setup Time JK to CP	TSU	VCC = 4.5V	1	+25°C	18	-	ns
			1	+125°C	27	-	ns
Hold Time JK to CP	TH	VCC = 4.5V	1	+25°C	3	-	ns
			1	+125°C	3	-	ns
Removal Time $\overline{R}$, $\overline{S}$ to CP	TREM	VCC = 4.5V	1	+25°C	18	-	ns
			1	+125°C	27	-	ns
Pulse Width CP	TW	VCC = 4.5V	1	+25°C	18	-	ns
			1	+125°C	27	-	ns
Pulse Width $\overline{R}$, $\overline{S}$	TW	VCC = 4.5V	1	+25°C	18	-	ns
			1	+125°C	27	-	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.4	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
CP to Q, $\overline{Q}$	TPLH	VCC = 4.5V	+25°C	2	30	2	38	ns
	TPHL	VCC = 4.5V	+25°C	2	35	2	44	ns
$\overline{S}$ to Q	TPLH	VCC = 4.5V	+25°C	2	23	2	29	ns
$\overline{S}$ to $\overline{Q}$	TPHL	VCC = 4.5V	+25°C	2	33	2	41	ns
$\overline{R}$ to Q	TPHL	VCC = 4.5V	+25°C	2	33	2	41	ns
$\overline{R}$ to $\overline{Q}$	TPLH	VCC = 4.5V	+25°C	2	33	2	41	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	6μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
6, 7, 9, 10	1 - 5, 8, 11 - 15	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
6, 7, 9, 10	8	-	1 - 5, 11 - 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	8	6, 7, 9, 10	1, 5, 11, 15, 16	4, 12	2, 3, 13, 14

NOTES:

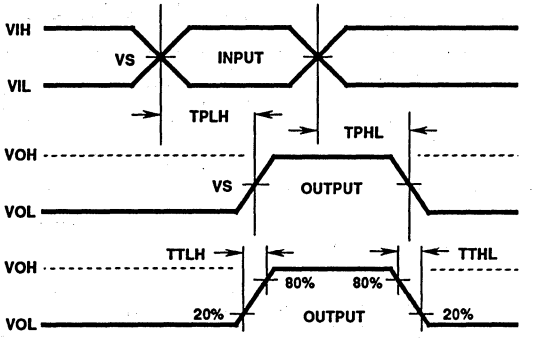
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for dynamic burn-in

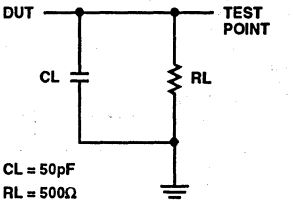
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
6, 7, 9, 10	8	1 - 5, 11 - 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

AC Timing Diagrams and AC Load Circuit

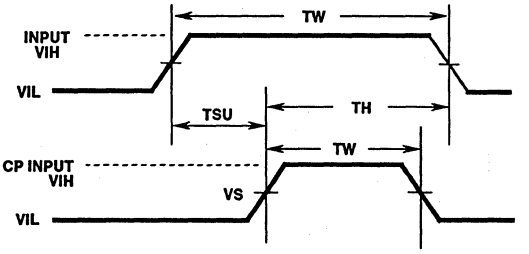




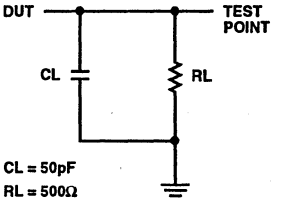
AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

Pulse Width, Setup, Hold Timing Diagram Positive Edge Trigger



TH = Hold Time
TSU = Setup Time
TW = Pulse Width



PULSE WIDTH, SETUP, HOLD VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
89 x 88 mils
2.25 x 2.24mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

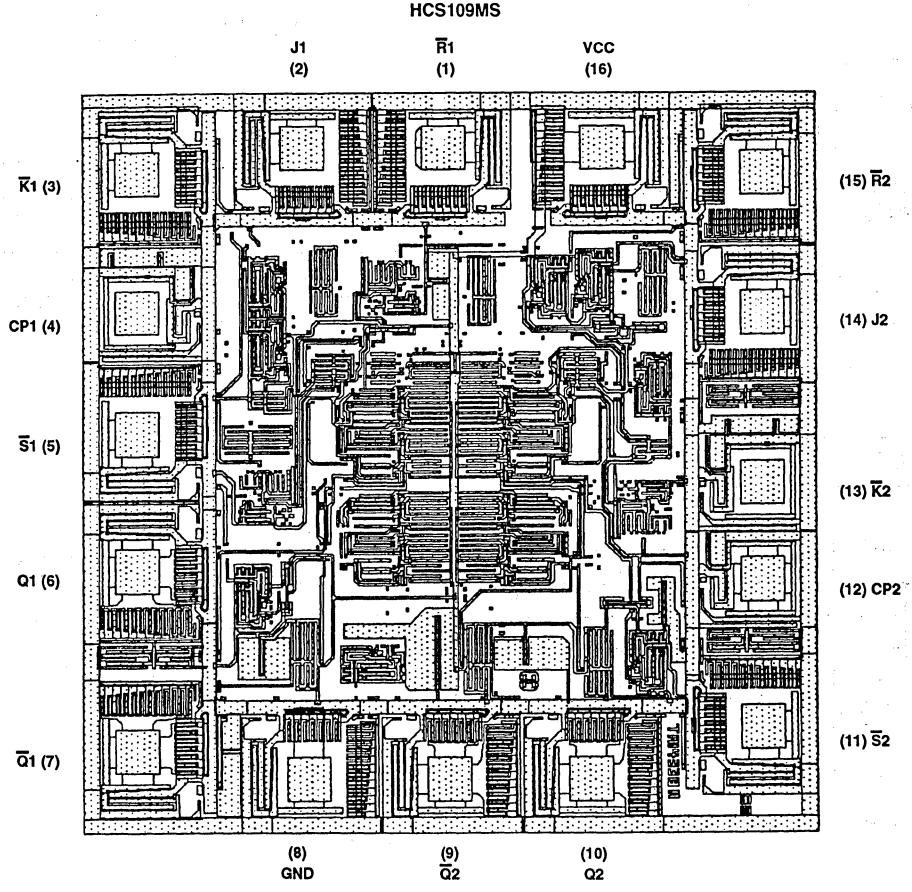
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HCTS109MS

Radiation Hardened Dual $J\overline{K}$ Flip Flop

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Rate 2 x 10^{-9} Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Logic Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

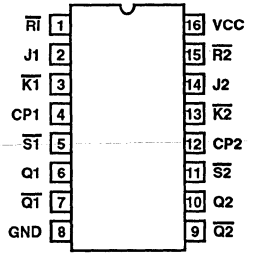
The Harris HCTS109MS is a Radiation Hardened Dual JK Flip Flop with set and reset. The flip flop changes state with the positive transition of the clock (CP1 or CP2).

The HCTS109MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

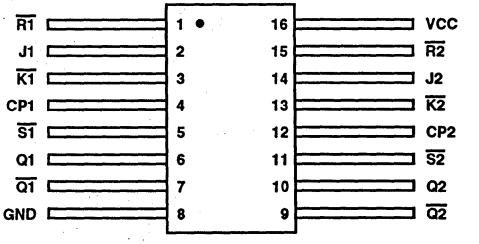
The HCTS109MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F16, LEAD FINISH C
TOP VIEW

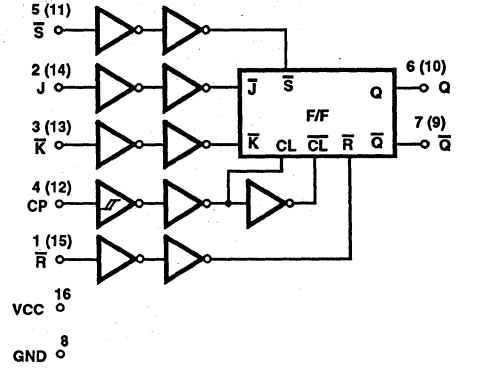


Truth Table

INPUTS					OUTPUTS	
$\overline{S}$	$\overline{R}$	CP	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	L	H
H	H	↓	H	L	Toggle	
H	H	↓	L	H	No Change	
H	H	↓	H	H	H	L
H	H	L	X	X	No Change	

*Unpredictable and unstable condition if both $\overline{S}$ and $\overline{R}$ go high simultaneously

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2141.1**

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Rise and Fall Times at VCC = 4.5V (TR, TF) . . 100ns/V Max.
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	20	µA
			2, 3	+125°C, -55°C	-	400	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CP to Q, $\overline{Q}$	TPLH	VCC = 4.5V	9	+25°C	2	26	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	30	ns
	TPHL	VCC = 4.5V	9	+25°C	2	30	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	35	ns
$\overline{S}$ to Q	TPLH	VCC = 4.5V	9	+25°C	2	19	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	23	ns
$\overline{S}$ to $\overline{Q}$	TPHL	VCC = 4.5V	9	+25°C	2	31	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	33	ns
$\overline{R}$ to Q	TPHL	VCC = 4.5V	9	+25°C	2	31	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	33	ns
$\overline{R}$ to $\overline{Q}$	TPLH	VCC = 4.5V	9	+25°C	2	31	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	33	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 53		pF
			1	+125°C	Typical 53		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns
Max Operating Frequency	FMAX	VCC = 4.5V	1	+25°C	-	27	MHz
			1	+125°C	-	18	MHz
Setup Time J, K to CP	TSU	VCC = 4.5V	1	+25°C	16	-	ns
			1	+125°C	18	-	ns
Hold Time J, K to CP	TH	VCC = 4.5V	1	+25°C	3	-	ns
			1	+125°C	3	-	ns
Removal Time $\overline{R}$, $\overline{S}$ to CP	TREM	VCC = 4.5V	1	+25°C	16	-	ns
			1	+125°C	18	-	ns
Pulse Width $\overline{R}$, $\overline{S}$	TW ($\overline{S}$, $\overline{R}$)	VCC = 4.5V	1	+25°C	16	-	ns
			1	+125°C	18	-	ns
Pulse Width $\overline{CP}$	TW (CP)	VCC = 4.5V	1	+25°C	24	-	ns
			1	+125°C	27	-	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.4	-	1.5	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
CP to Q, $\overline{Q}$	TPLH	VCC = 4.5V	+25°C	2	30	2	38	ns
	TPHL	VCC = 4.5V	+25°C	2	35	2	44	ns
$\overline{S}$ to Q	TPLH	VCC = 4.5V	+25°C	2	23	2	29	ns
$\overline{S}$ to $\overline{Q}$	TPHL	VCC = 4.5V	+25°C	2	33	2	41	ns
$\overline{R}$ to Q	TPHL	VCC = 4.5V	+25°C	2	33	2	41	ns
$\overline{R}$ to $\overline{Q}$	TPLH	VCC = 4.5V	+25°C	2	33	2	41	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUB-GROUP	DELTA LIMIT
ICC	5	6μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC BURN-IN AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
6, 7, 9, 10	1 - 5, 8, 11 - 15	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
6, 7, 9, 10	8	-	1 - 5, 11 - 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	8	6, 7, 9, 10	1, 5, 11, 15, 16	4, 12	2, 3, 13, 14

NOTES:

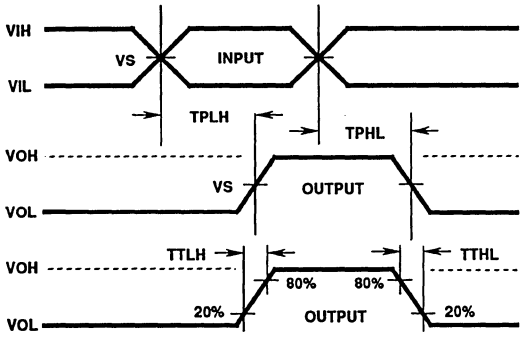
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in.

TABLE 9. RRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
6, 7, 9, 10	8	1, 2, 3, 4, 5, 11, 12, 13, 14, 15, 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

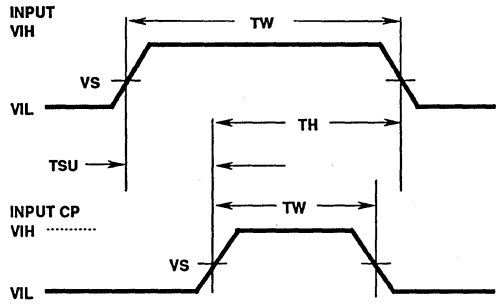
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Pulse Width, Setup, Hold Timing Diagram Positive Edge Trigger

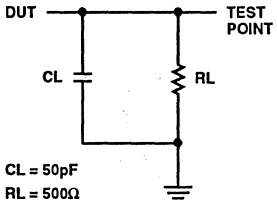


TH = HOLD TIME
TSU = SETUP TIME
TW = PULSE WIDTH

VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
89 x 88 mils
2.25 X 2.24mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

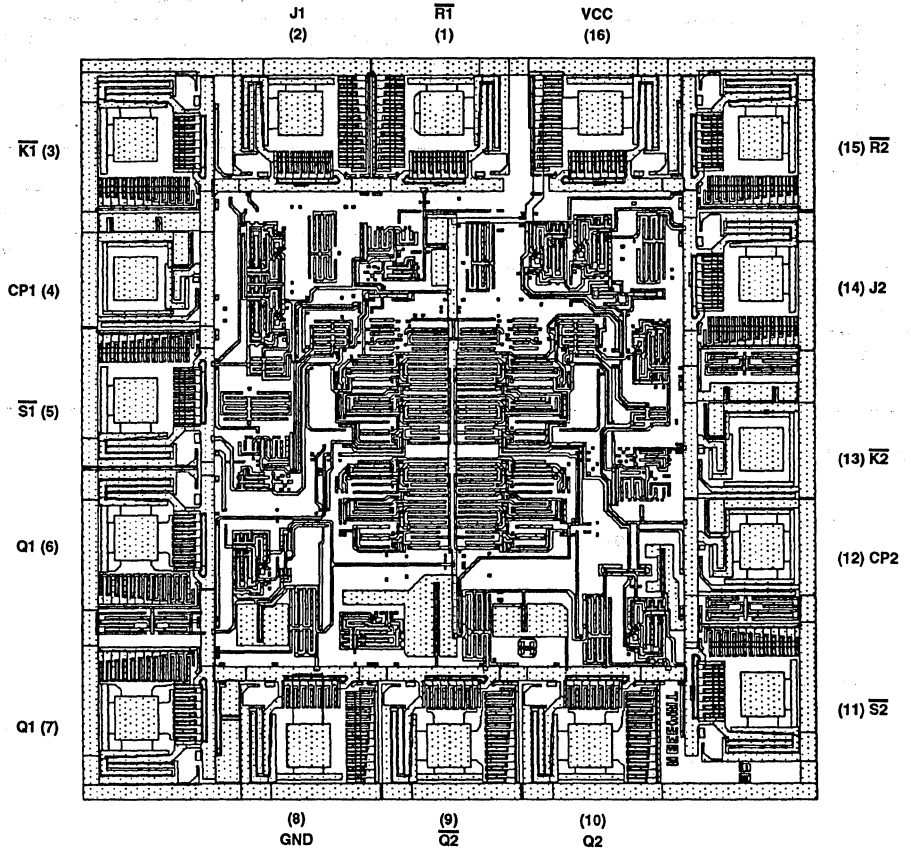
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS109MS



HARRIS SEMICONDUCTOR

HCTS112MS

Radiation Hardened Dual $\overline{JK}$ Flip-Flop

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD (Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Rate 2 x 10^{-9} Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Military Temperature Range ..... -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range ..... 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

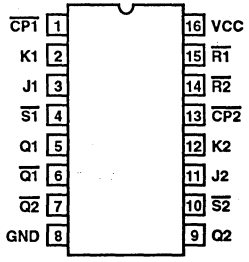
The Harris HCTS112MS is a Radiation Hardened dual JK flip-flop with set and reset. The flip-flop changes states with the negative transition of the clock (CP1N or CP2N).

The HCTS112MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

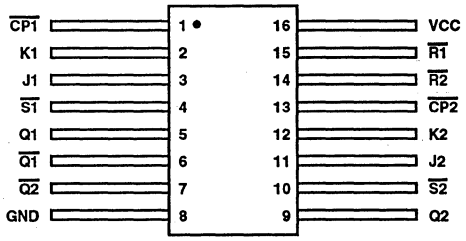
The HCTS112MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835, DESIGNATOR CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-1835, DESIGNATOR CDFP4-F16, LEAD FINISH C
TOP VIEW



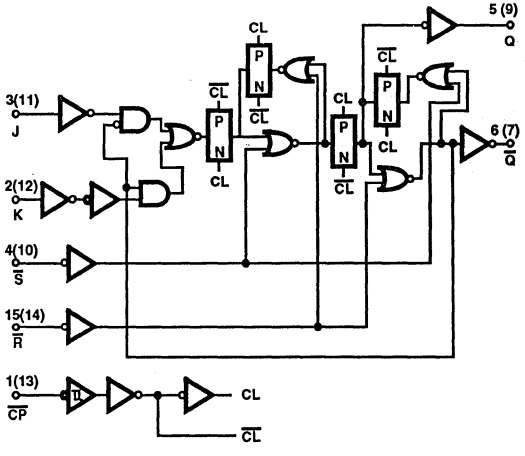
Truth Table

INPUTS					OUTPUTS	
$\overline{S}$	$\overline{R}$	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	No Change	
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	No Change	

H = High Steady State, L = Low Steady State, X = Immaterial,
↓ = High-to-Low Transition

* Output States Unpredictable if $\overline{S}$ and $\overline{R}$ Go High Simultaneously after Both being Low at the Same Time

Functional Diagram



7 LOGIC

File Number **2467.1**

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Rise and Fall Times at VCC = 4.5V (TR, TF) . . . 100ns/V Max
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . .VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	20	µA
			2, 3	+125°C, -55°C	-	400	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
$\overline{CP}$ to Q, $\overline{Q}$	TPHL	VCC = 4.5V	9	+25°C	2	37	ns
			10, 11	+125°C, -55°C	2	42	ns
	TPLH	VCC = 4.5V	9	+25°C	2	34	ns
			10, 11	+125°C, -55°C	2	38	ns
$\overline{S}$ to Q	TPLH	VCC = 4.5V	9	+25°C	2	21	ns
			10, 11	+125°C, -55°C	2	24	ns
$\overline{S}$ to $\overline{Q}$	TPHL	VCC = 4.5V	9	+25°C	2	35	ns
			10, 11	+125°C, -55°C	2	41	ns
$\overline{R}$ to Q	TPHL	VCC = 4.5V	9	+25°C	2	33	ns
			10, 11	+125°C, -55°C	2	38	ns
$\overline{R}$ to $\overline{Q}$	TPLH	VCC = 4.5V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	34	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 40		pF
			1	+125°C	Typical 100		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL, TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns
Setup Time J, K to CP	TSU	VCC = 4.5V	1	+25°C	14	-	ns
			1	+125°C	16	-	ns
Hold Time J, K to CP	TH	VCC = 4.5V	1	+25°C	3	-	ns
			1	+125°C	3	-	ns
Removal Time $\overline{R}$, $\overline{S}$ to CP	TREM	VCC = 4.5V	1	+25°C	18	-	ns
			1	+125°C	20	-	ns
Pulse Width $\overline{R}$, $\overline{S}$	TW ($\overline{R}$, $\overline{S}$)	VCC = 4.5V	1	+25°C	16	-	ns
			1	+125°C	18	-	ns
Pulse Width CP	TW (CP)	VCC = 4.5V	1	+25°C	14	-	ns
			1	+125°C	16	-	ns
Max Operating Frequency	FMAX	VCC = 4.5V	1	+25°C	-	30	MHz
			1	+125°C	-	20	MHz

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	200K LIMITS RAD		1M LIMITS RAD		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.4	-	1.5	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
CP to Q, $\overline{Q}$	TPHL	VCC = 4.5V	+25°C	2	42	2	53	ns
	TPLH	VCC = 4.5V	+25°C	2	38	2	48	ns
$\overline{S}$ to Q	TPLH	VCC = 4.5V	+25°C	2	24	2	30	ns
$\overline{S}$ to $\overline{Q}$	TPHL	VCC = 4.5V	+25°C	2	41	2	51	ns
$\overline{R}$ to Q	TPHL	VCC = 4.5V	+25°C	2	38	2	48	ns
$\overline{R}$ to $\overline{Q}$	TPLH	VCC = 4.5V	+25°C	2	34	2	43	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	6µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC BURN-IN AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
5, 6, 7, 9	1 - 4, 8, 10 - 15	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
5, 6, 7, 9	8	-	1 - 4, 10 - 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	8	5, 6, 7, 9	2, 3, 4, 10, 11, 12, 14, 15, 16	1, 13	-

NOTES:

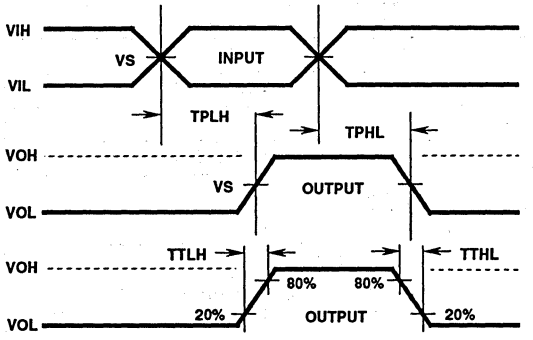
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
5, 6, 7, 9	8	1 - 4, 10 - 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

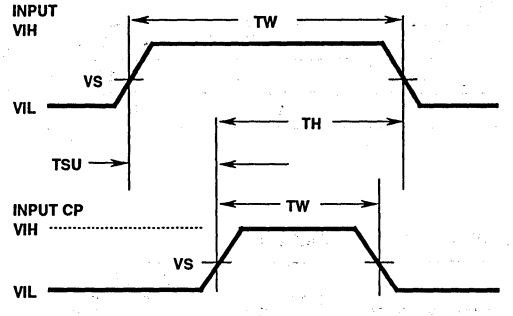
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Pulse Width, Setup, Hold Timing Diagram Positive Edge Trigger

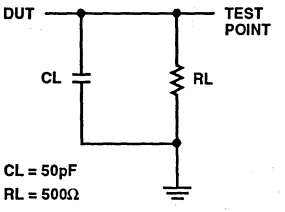


TH = HOLD TIME
TSU = SETUP TIME
TW = PULSE WIDTH

VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
89 x 88 mils
2.25 x 2.24mm

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

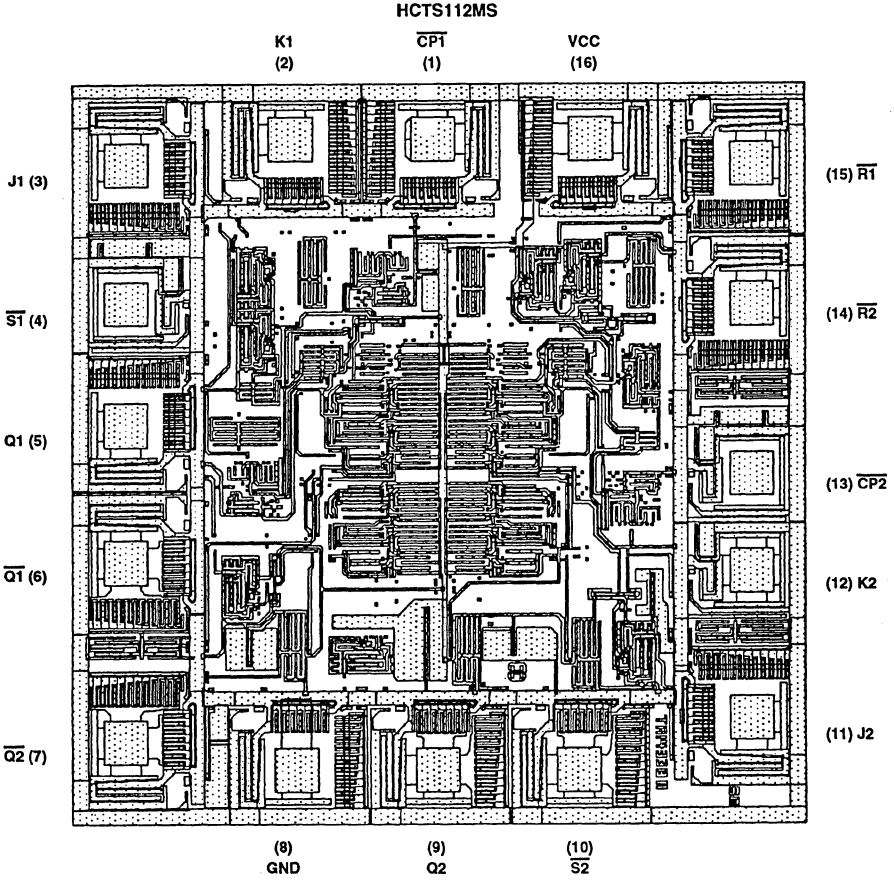
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HCS132MS

Radiation Hardened Quad 2-Input NAND Schmitt Trigger

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity < 2 x 10^{-9} Errors/Gate Day (Typ
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

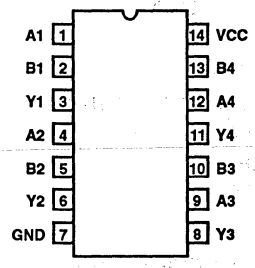
The Harris HCS132MS is a Radiation Hardened Quad 2-Input NAND Schmitt Trigger inputs. A high on both inputs forces the output to a Low state.

The HCS132MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

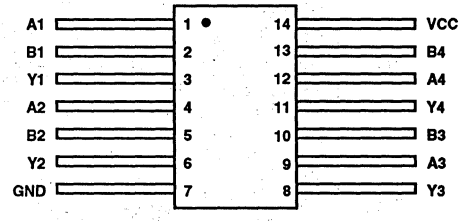
The HCS132MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

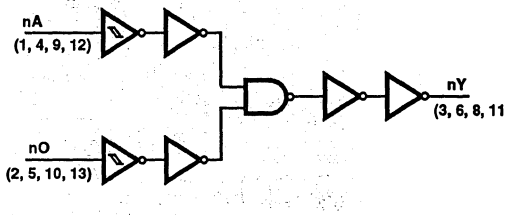


Truth Table

INPUTS		OUTPUTS
An	Bn	Yn
L	L	H
L	H	H
H	L	H
H	H	L

NOTE: L = Logic Level Low, H = Logic level High

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3061

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) .... Unlimited Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 30% of VCC
Input High Voltage (VIH) ..... 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:
1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Output	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns
	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
Input Switch Points	Vt+	VCC = 4.5V	9	+25°C	2.00	3.15	V
			10, 11	+125°C, -55°C	2.00	3.15	V
	Vt-	VCC = 4.5V	9	+25°C	1.35	2.60	V
			10, 11	+125°C, -55°C	1.35	2.60	V
	VH	VCC = 4.5V	9	+25°C	0.10	1.40	V
			10, 11	+125°C, -55°C	0.10	1.40	V

NOTES:
1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 26		pF
			1	+125°C	Typical 32		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:
1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Input to Output	TPLH	VCC = 4.5V	+25°C	2	22	2	26	ns
	TPHL	VCC = 4.5V	+25°C	2	20	2	25	ns
Input Switch Points	Vt+	VCC = 4.5	+25°C	1.70	3.15	0.80	3.15	V
	Vt-	VCC = 4.5	+25°C	0.90	2.10	0.30	2.10	V
	VH	VCC = 4.5	+25°C	0.10	1.40	0.10	1.40	V

NOTES:
1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE: Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
3, 6, 8, 11	1, 2, 4, 5, 7, 9, 10, 12, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 6, 8, 11	7	-	1, 2, 4, 5, 9, 10, 12, 13, 14	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 2)					
-	7	3, 6, 8, 11	14	1, 2, 4, 5, 9, 10, 12, 13	-

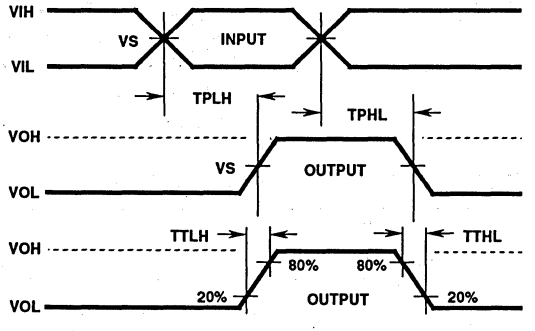
NOTES:
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for dynamic burn-in.

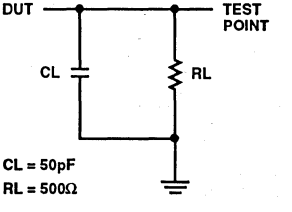
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 6, 8, 11	7	1, 2, 4, 5, 9, 10, 12, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

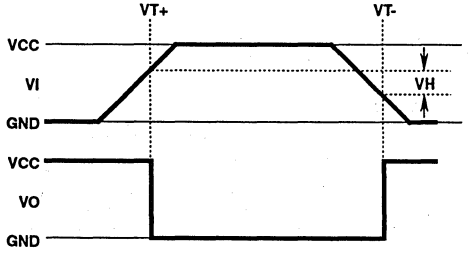
AC Timing Diagrams and Load Circuit





AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V



HYSTERESIS DEFINITION

Die Characteristics

DIE DIMENSIONS:
90 x 90 mils
2.29 x 2.29mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

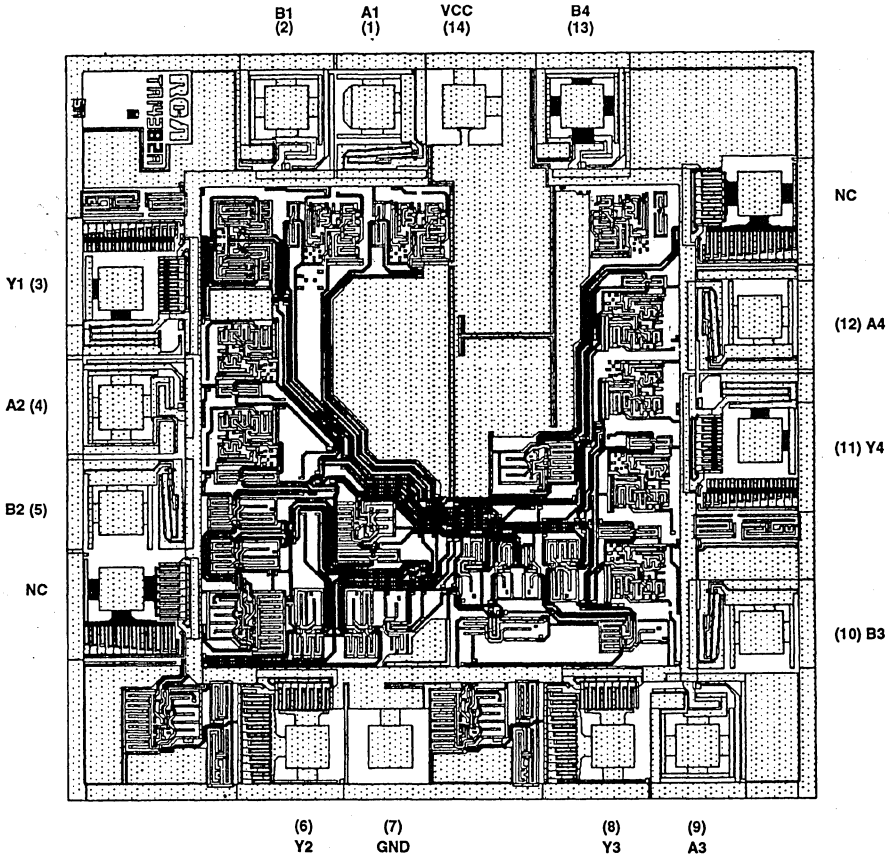
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCS132MS



HARRIS SEMICONDUCTOR

HCTS132MS

Radiation Hardened Quad 2-Input NAND Schmitt Trigger

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

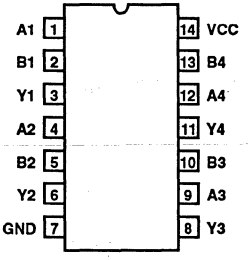
The Harris HCTS132MS is a Radiation Hardened Quad 2-Input NAND Schmitt Trigger inputs. A high on both inputs forces the output to a Low state.

The HCTS132MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

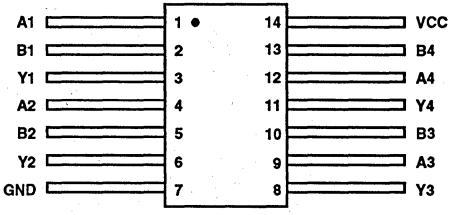
The HCTS132MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835, DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835, DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

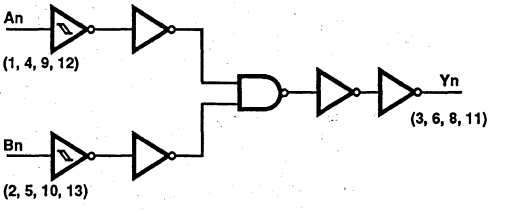


Truth Table

INPUTS		OUTPUTS
An	Bn	Yn
L	L	H
L	H	H
H	L	H
H	H	L

NOTE: L = Logic Level Low, H = Logic level High

Functional Diagram



File Number 3062

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Rise and Fall Times at VCC = 4.5V (TR, TF) . . Unlimited Max
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:
1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Output	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns
	TPHL	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
Input Switch Points	VT+	VCC = 4.5V	9	+25°C	0.50	2.25	V
			10, 11	+125°C, -55°C	0.50	2.25	V
	VT-	VCC = 4.5V	9	+25°C	0.50	2.25	V
			10, 11	+125°C, -55°C	0.50	2.25	V
	VH	VCC = 4.5V	9	+25°C	0.10	1.40	V
			10, 11	+125°C, -55°C	0.10	1.40	V

NOTES:
1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 25		pF
			1	+125°C	Typical 32		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTES:
1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Input to Output	TPLH	VCC = 4.5V	+25°C	2	22	2	26	ns
	TPHL	VCC = 4.5V	+25°C	2	20	2	25	ns
Input Switch Points	VT+	VCC = 4.5	+25°C	0.40	2.25	0.30	2.25	ns
	VT-	VCC = 4.5	+25°C	0.40	2.25	0.30	2.25	ns
	VH	VCC = 4.5	+25°C	0.10	1.40	0.10	1.40	ns

NOTES:
1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:
1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:
1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC BURN-IN AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
3, 6, 8, 11	1, 2, 4, 5, 7, 9, 10, 12, 13		14		
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 6, 8, 11	7		1, 2, 4, 5, 9, 10, 12, 13, 14		
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	7	3, 6, 8, 11	14	1, 2, 4, 5, 9, 10, 12, 13	-

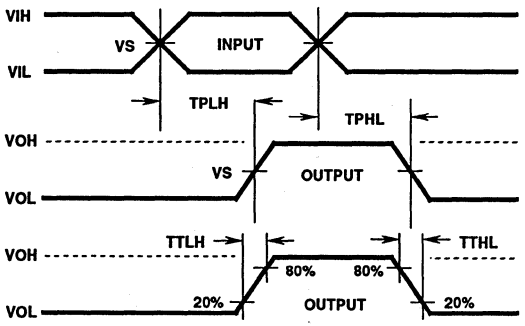
NOTES:
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 6, 8, 11	7	1, 2, 4, 5, 9, 10, 12, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

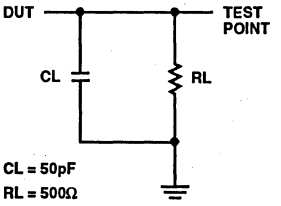
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
90 x 90 mils
2.29 x 2.29mm

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

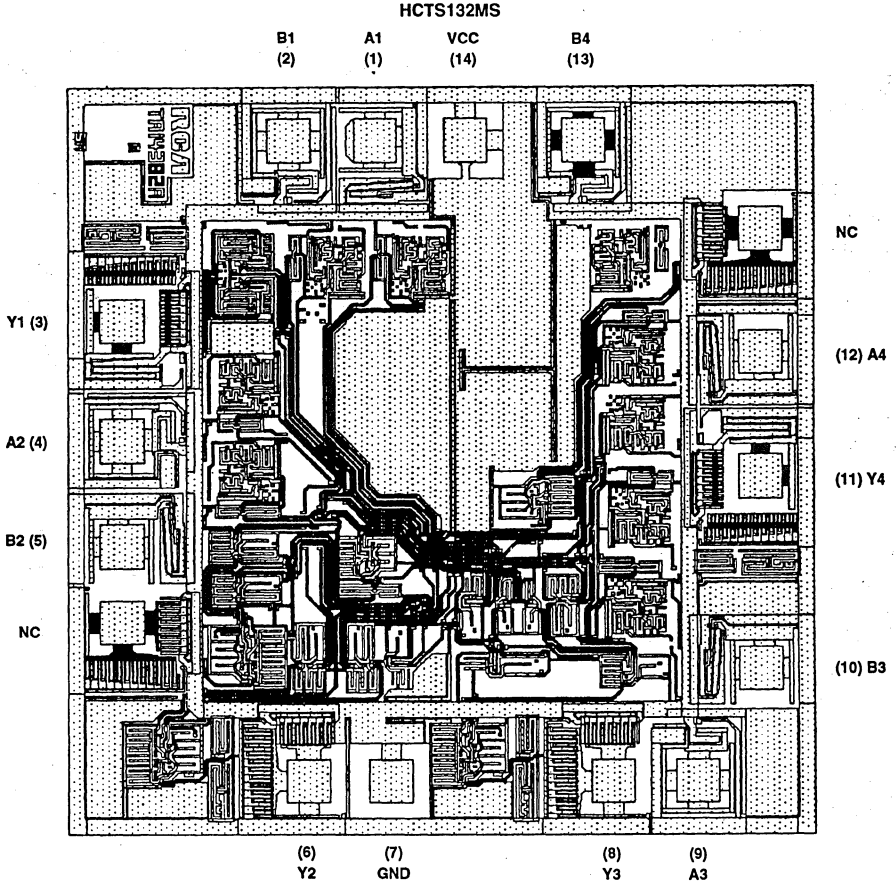
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HCS138MS

Radiation Hardened Inverting 3-to-8 Line Decoder/Demultiplexer

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Standard Outputs - 10 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.3 VCC Max
  - VIH = 0.7 VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

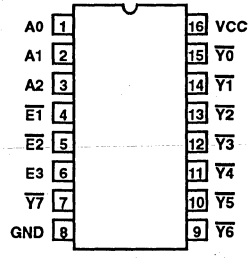
The Harris HCS138MS is a Radiation Hardened 3-to-8 line Decoder/Demultiplexer. The outputs are active in the low state. Two active low and one active high enables ($\overline{E1}$, $\overline{E2}$, E3) are provided. If the device is enabled, the binary inputs (A0, A1, A2) determine which one of the eight normally high outputs will go to a low logic level.

The HCS138MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

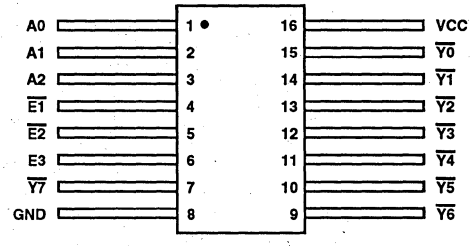
The HCS138MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR, CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
CASE OUTLINE F-5A, CONFIGURATION 2, LEAD FINISH C
MIL-STD-1835 DESIGNATOR, CDFP4-F16, LEAD FINISH C
TOP VIEW

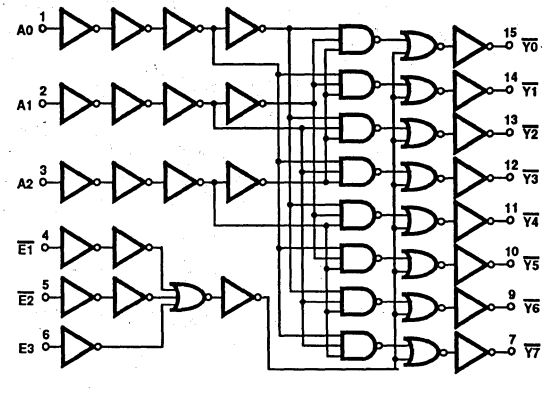


Truth Table

INPUTS						OUTPUTS							
ENABLE													
E3	$\overline{E2}$	$\overline{E1}$	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = High Level, L = Low Level, X = Don't Care

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2473.1**

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Input Rise and Fall Times at VCC = 4.5V (TR, TF) . . . . . 500ns Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 30% of VCC
Input High Voltage (VIH) . . . . . 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address to Output	TPLH	VCC = 4.5V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	34	ns
	TPHL	VCC = 4.5V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	34	ns
Enable to Output	TPLH	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	33	ns
	TPHL	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	33	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 52		pF
			1	+125°C	Typical 75		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	3.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	5.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-5.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200KRAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Address to Output	TPLH	VCC = 4.5V	+25°C	2	34	2	41	ns
	TPHL	VCC = 4.5V	+25°C	2	34	2	41	ns
Enable to Output	TPLH	VCC = 4.5V	+25°C	2	33	2	40	ns
	TPHL	VCC = 4.5V	+25°C	2	33	2	40	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A inspection in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
7, 9 - 15	1 - 6, 8		16		
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
7, 9 - 15	8	-	1 - 6, 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	4, 5, 8	7, 9 - 15	3, 6, 16	2	1

NOTES:

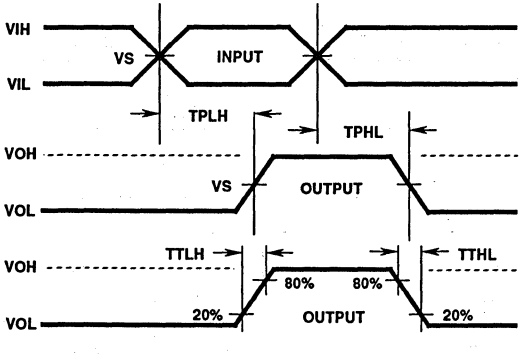
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680Ω ± 5% for dynamic burn-in

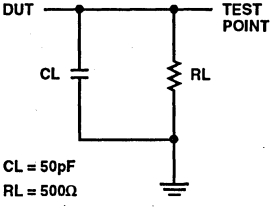
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
7, 9 - 15	8	1 - 6, 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

AC Timing Diagram and Load Circuit





AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
85 x 101 mils

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

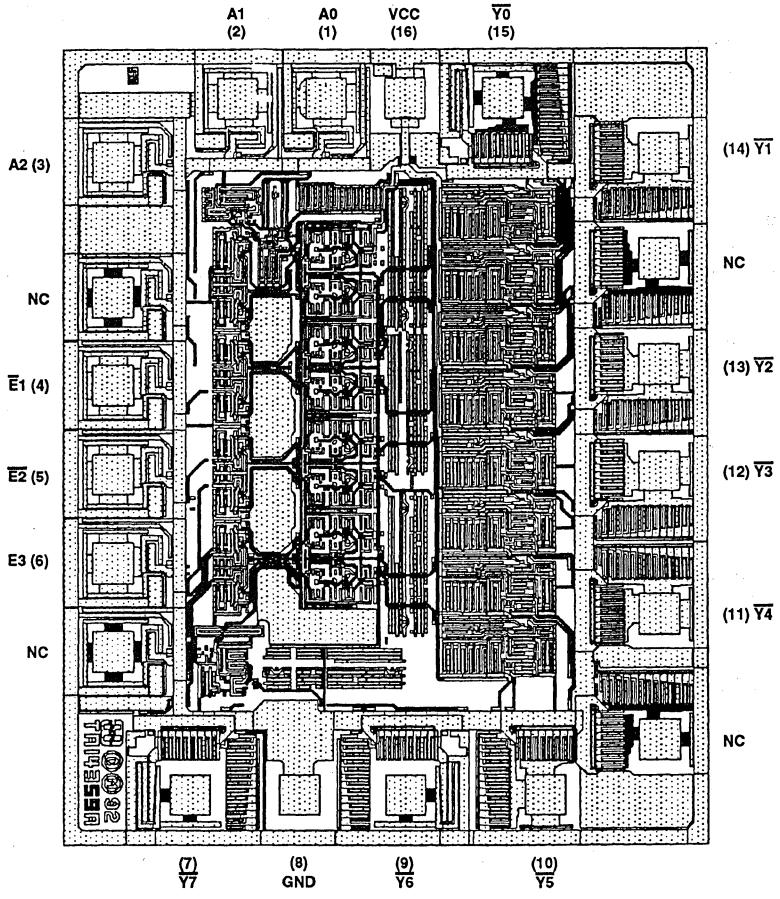
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCS138MS



HARRIS SEMICONDUCTOR

HCTS138MS

Radiation Hardened Inverting 3-to-8 Line Decoder/Demultiplexer

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Bus Driver Outputs - 15 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

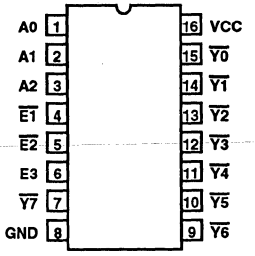
The Harris HCTS138MS is a Radiation Hardened 3-to-8 line Decoder/Demultiplexer. The outputs are active in the low state. Two active low and one active high enables ($\overline{E1}$, $\overline{E2}$, E3) are provided. If the device is enabled, the binary inputs (A0, A1, A2) determine which one of the eight normally high outputs will go to a low logic level.

The HCTS138MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family with TTL input compatibility.

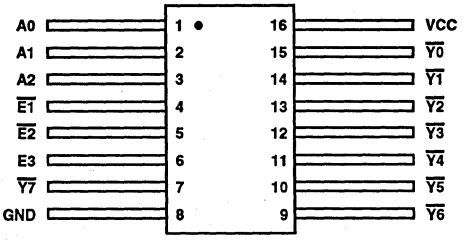
The HCTS138MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835, DESIGNATOR CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-1835, DESIGNATOR CDFP4-F16, LEAD FINISH C
TOP VIEW

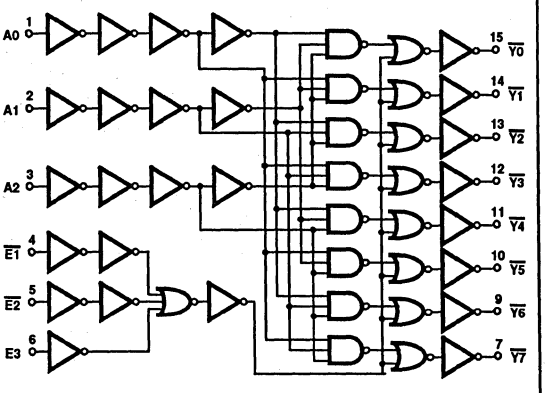


Truth Table

INPUTS						OUTPUTS							
ENABLE													
E3	$\overline{E2}$	$\overline{E1}$	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = High Level, L = Low Level, X = Don't Care

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 2462.1

Absolute Maximum Ratings

Supply Voltage (VCC) ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) ..... +4.5V to +5.5V
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Rise and Fall times at VCC = 4.5V (TR, TF) ..... 500ns Max.
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-7.2	-	mA
			2, 3	+125°C, -55°C	-6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH =2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address to Output	TPLH	VCC = 4.5V	9	+25°C	2	25	ns
			10, 11	+125°C, -55°C	2	30	ns
	TPHL	VCC = 4.5V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	39	ns
Enable to Output	TPLH	VCC = 4.5V	9	+25°C	2	26	ns
			10, 11	+125°C, -55°C	2	31	ns
	TPHL	VCC = 4.5V	9	+25°C	2	26	ns
			10, 11	+125°C, -55°C	2	34	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 59		pF
			1	+125°C, -55°C	Typical 68		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C, -55°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C, -55°C	-	22	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	3.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	5.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-5.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	μA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Address to Output	TPLH	VCC = 4.5V	+25°C	2	30	2	38	ns
	TPHL	VCC = 4.5V	+25°C	2	39	2	49	ns
Enable to Output	TPLH	VCC = 4.5V	+25°C	2	31	2	39	ns
	TPHL	VCC = 4.5V	+25°C	2	34	2	43	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC BURN-IN AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
7, 9 - 15	1 - 6, 8		16		
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
7, 9 - 15	8		1 - 6, 16		
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	4, 5, 8	7, 9 - 15	3, 6, 16	2	1

NOTES:

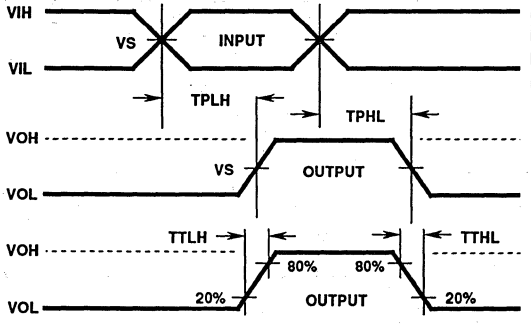
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 680Ω ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
7, 9 - 15	8	1 - 6, 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

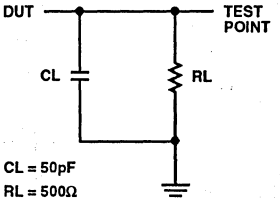
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
85 x 101 mils

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

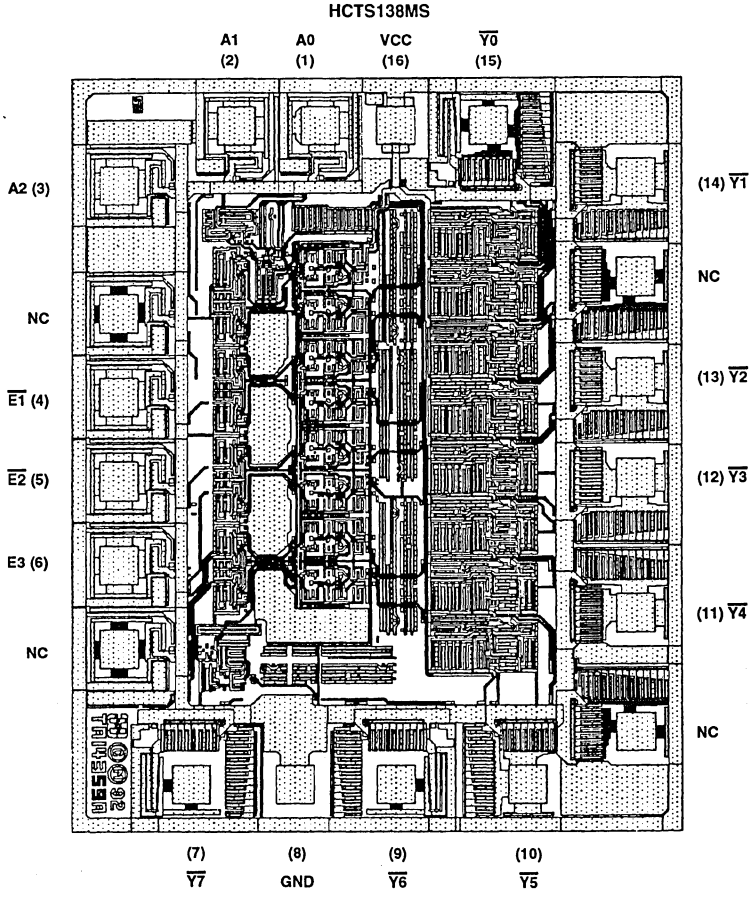
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HCTS139MS

Radiation Hardened Dual 2-to-4 Line Decoder/Demultiplexer

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Bus Driver Outputs - 15 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

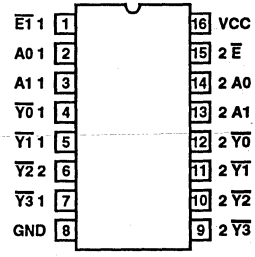
The Harris HCTS139MS is a Radiation Hardened 2-to-4 line Decoder/Demultiplexer with an active low enable ($\overline{E}$). Data on the select inputs (A0, A1) cause one of the four normally high outputs to go to a low logic level. The Demultiplexing function is performed by using the enable input as the data input.

The HCTS139MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family with TTL input compatibility.

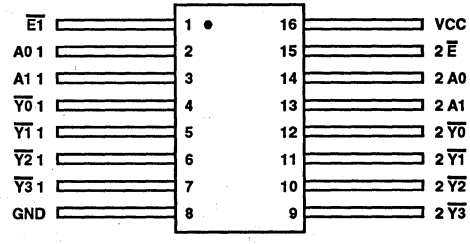
The HCTS139MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835, DESIGNATOR CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-1835, DESIGNATOR CDFP4-F16, LEAD FINISH C
TOP VIEW

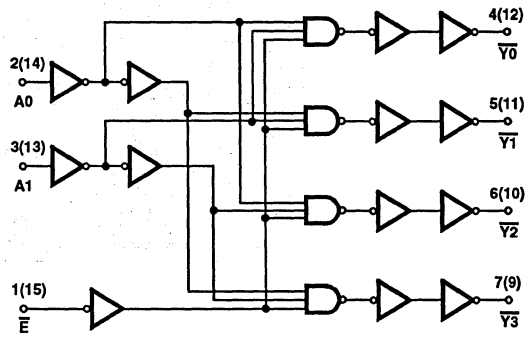


Truth Table

INPUTS ENABLE SELECT			OUTPUTS			
$\overline{E}$	A1	A0	$\overline{Y3}$	$\overline{Y2}$	$\overline{Y1}$	$\overline{Y0}$
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1
1	X	X	1	1	1	1

Logic 1 = High
Logic 0 = Low
X = Immaterial

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2231.1**

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Rise and Fall Times at VCC = 4.5V (TR, TF) . . . . . 500ns Max
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-7.2	-	mA
			2, 3	+125°C, -55°C	-6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
A0, A1 to Output	TPHL, TPLH	VCC = 4.5V	9	+25°C	2	24	ns
			10, 11	+125°C, -55°C	2	27	ns
Enable to Output	TPHL, TPLH	VCC = 4.5V	9	+25°C	2	24	ns
			10, 11	+125°C, -55°C	2	27	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 50		pF
			1	+125°C, -55°C	Typical 60		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C, -55°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C, -55°C	-	22	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	3.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	5.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-5.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
A0, A1 to Output	TPHL, TPLH	VCC = 4.5V	+25°C	2	27	2	34	ns
Enable to Output	TPHL, TPLH	VCC = 4.5V	+25°C	2	27	2	34	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of Mil-Std-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% go/no-go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC I BURN-IN TEST CONNECTIONS (Note1)					
4 -7, 9 - 12	1 - 3, 13 - 15	-	16	-	-
STATIC II BURN-IN CONNECTIONS (Note1)					
4 - 7, 9 - 12	8	-	1 - 3, 13 - 16	-	-
DYNAMIC BURN-IN CONNECTIONS (Note2)					
-	1, 8, 15	4 - 7, 9 - 12	16	2, 14	3, 13

NOTES:

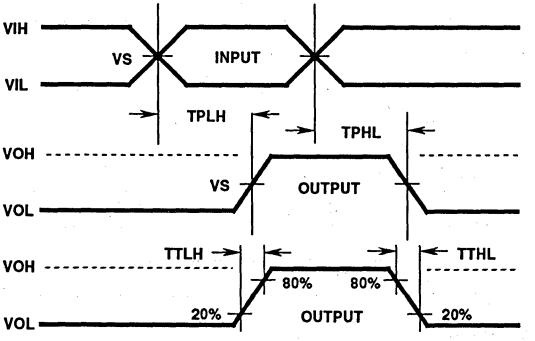
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for dynamic burn-in

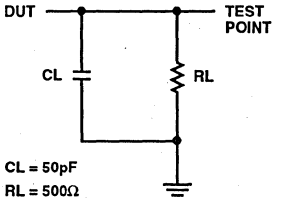
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
4 - 7, 9 - 12	8	1 - 3, 13 - 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

AC Timing Diagrams and Load Circuit





AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
2.74 mils x 2.68 mils
108mm x 106mm

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

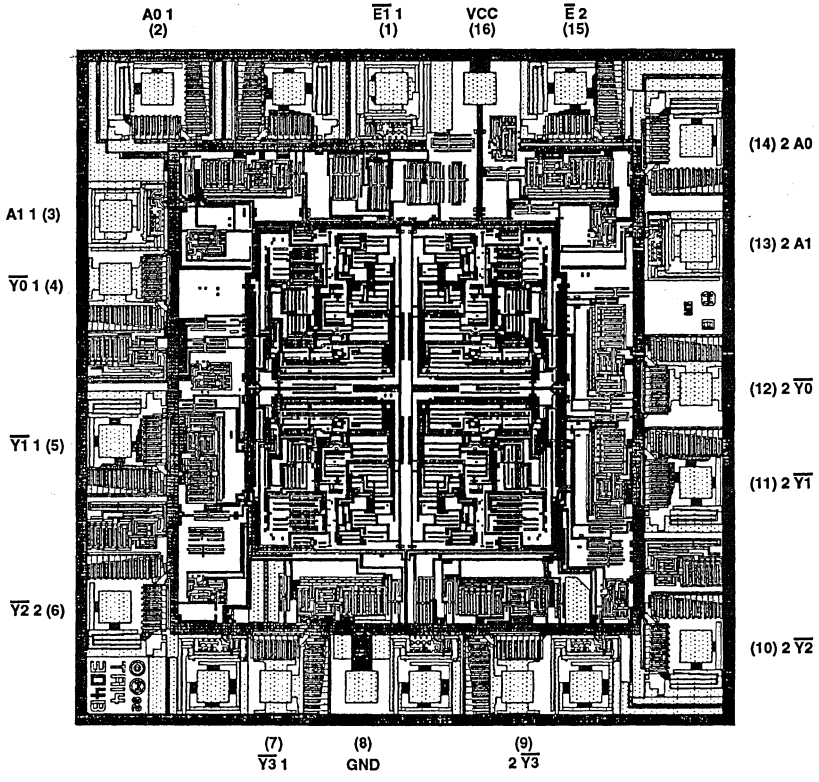
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS139MS



HARRIS SEMICONDUCTOR

HCTS147MS

Radiation Hardened 10-to-4 Line Priority Encoder

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Bus Driver Outputs - 15 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

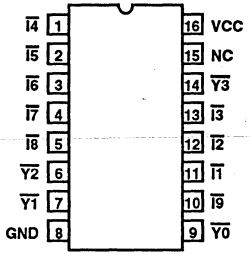
The Harris HCTS147MS is a Radiation Hardened 10-to-4 line Priority Encoder, pin compatible with low power Schottky TTL(LSTTL).

The HCTS147MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family with TTL input compatibility.

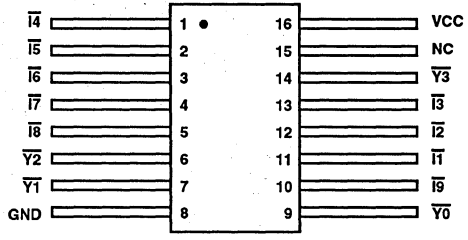
The HCTS147MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T16, LEAD FINISH C
TOP VIEW



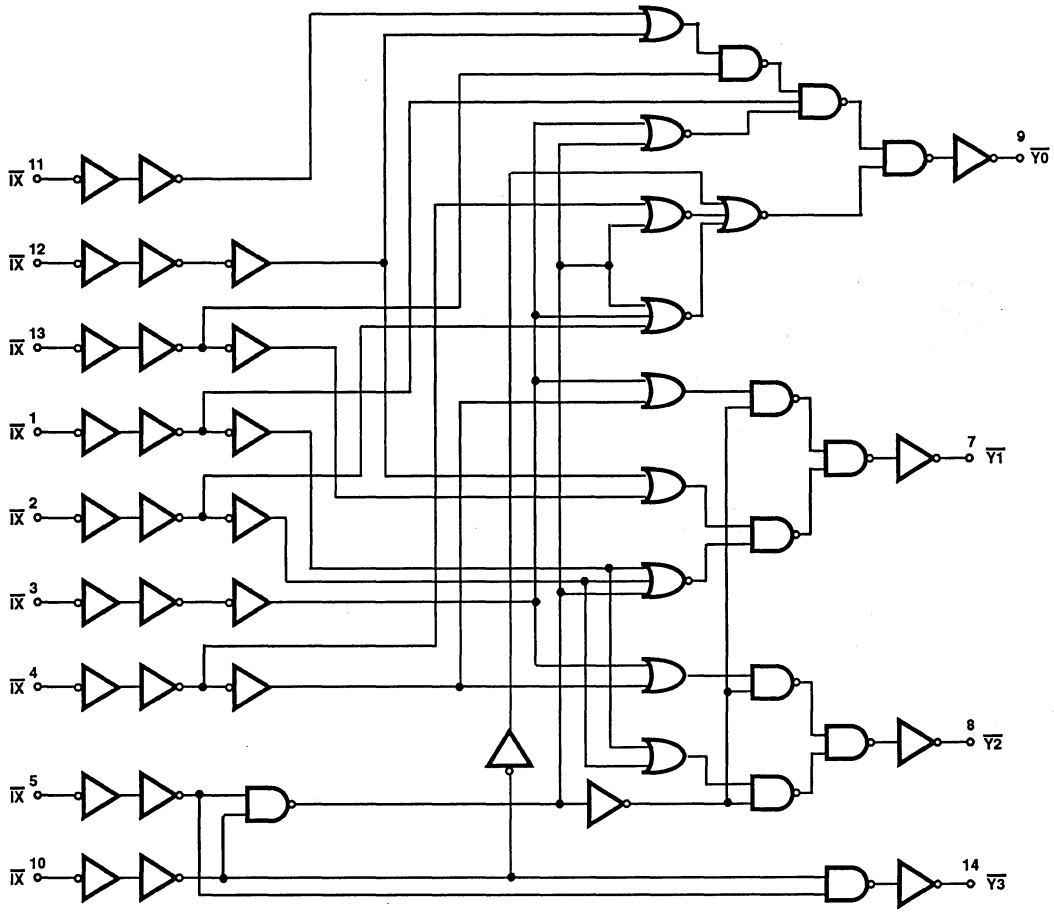
16 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F16, LEAD FINISH C
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3063

Functional Diagram



Truth Table

INPUTS									OUTPUTS			
$\overline{I1}$	$\overline{I2}$	$\overline{I3}$	$\overline{I4}$	$\overline{I5}$	$\overline{I6}$	$\overline{I7}$	$\overline{I8}$	$\overline{I9}$	$\overline{Y3}$	$\overline{Y2}$	$\overline{Y1}$	$\overline{Y0}$
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings

Supply Voltage(VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input. . . . . ±10mA
DC Drain Current, Any One Output. . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC). . . . . +4.5V to +5.5V
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 500ns Max.
Input Low Voltage (VIL). . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH =2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	0.5	µA
			2, 3	+125°C, -55°C	-5.0	5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	4.0	0.5	V

NOTE:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Output	TPLH	VCC = 4.5V	9	+25°C	2	28	ns
	TPHL		10, 11	+125°C, -55°C	2	32	ns
	TPLH	VCC = 4.5V	9	+25°C	2	28	ns
	TPHL		10, 11	+125°C, -55°C	2	32	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 44		pF
			1	+125°C, -55°C	Typical 47		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C, -55°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	µA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Input to Output	TPLH	VCC = 4.5V	+25°C	2	32	2	40	ns
	TPHL	VCC = 4.5V	+25°C	2	32	2	40	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC BURN-IN AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
6, 7, 9, 14, 15	1 - 5, 8, 10 - 13	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
6, 7, 9, 14, 15	8	-	1 - 5, 10 - 13, 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
15	8	6, 7, 9, 14	1 - 5, 10, 12, 13, 16	11	-

NOTES:

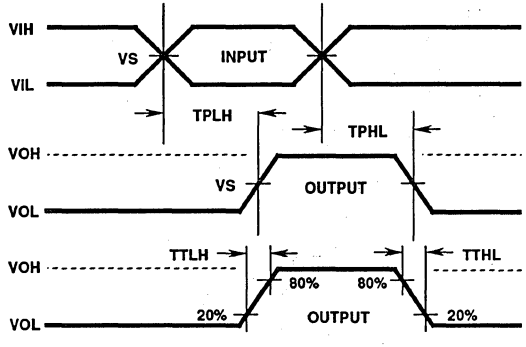
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 680Ω ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
6, 7, 9, 14, 15	8	1 - 5, 10 - 13, 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

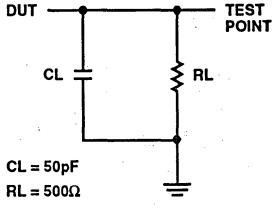
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



7 LOGIC

Die Characteristics

DIE DIMENSIONS:
85 x 101 mils

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

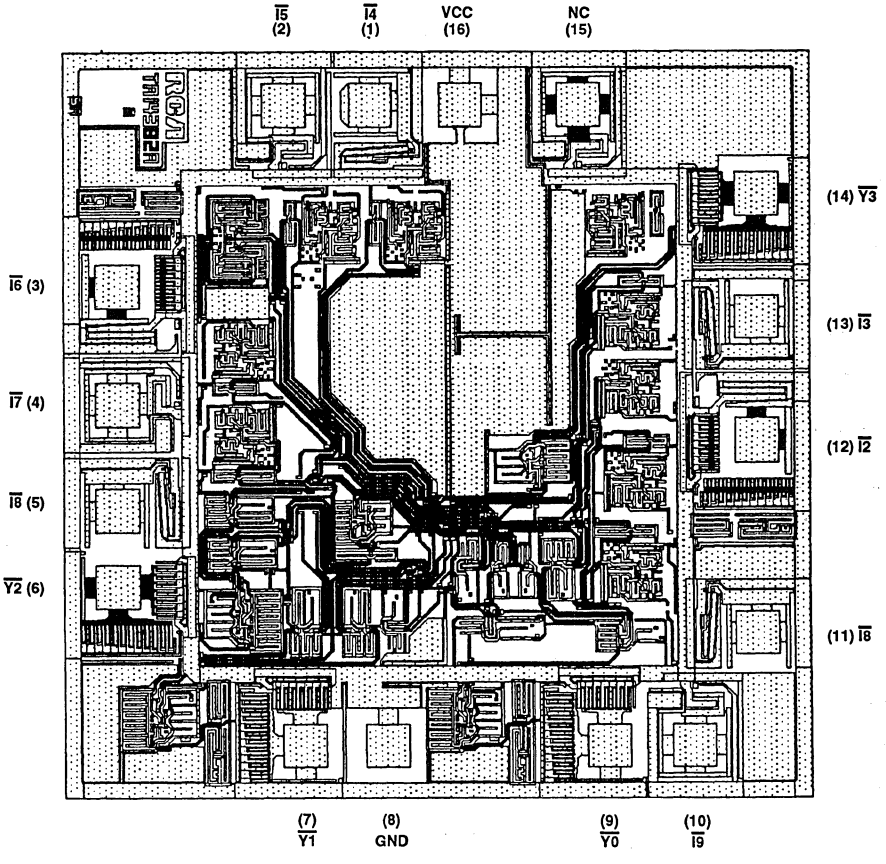
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS147MS



HARRIS SEMICONDUCTOR

HCS151MS

Radiation Hardened 8-Input Multiplexer

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity 2 x 10^{-9} Error/Gate Day (Typ)
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

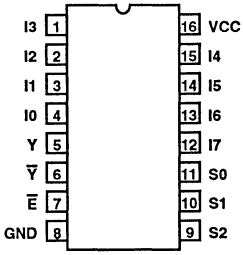
The Harris HCS151MS is a Radiation Hardened 8-Input Multiplexer having three binary control inputs (S0, S1, S2) and an active low enable ($\overline{E}$) input. The three binary signals select one of eight channels. Outputs are both inverting and non-inverting.

The HCS151MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

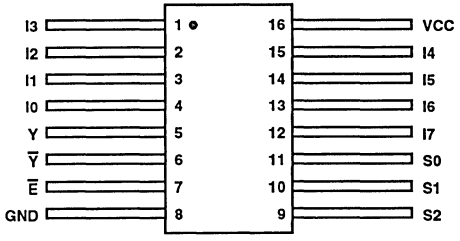
The HCS151MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F16, LEAD FINISH C
TOP VIEW



Truth Table

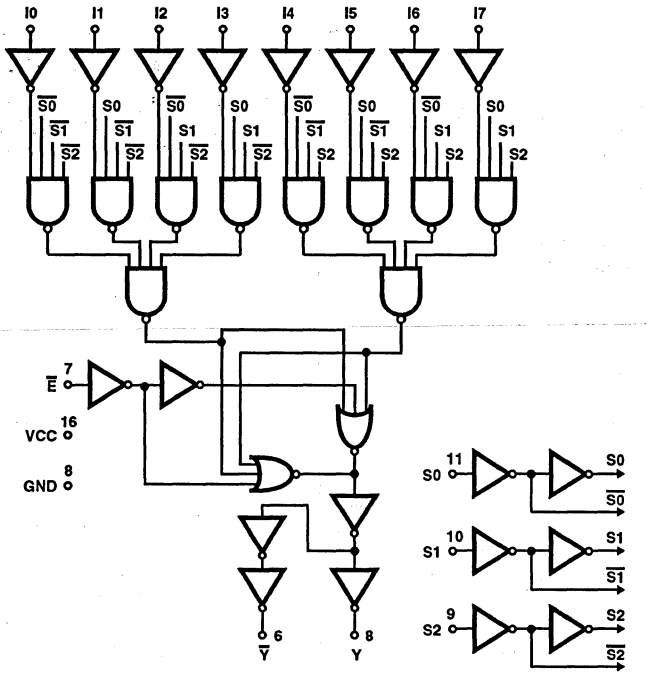
INPUTS												OUTPUTS	
$\overline{E}$	S0	S1	S2	I0	I1	I2	I3	I4	I5	I6	I7	$\overline{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = High Level, L = Low Level, X = Don't Care

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3077

Functional Diagram



Absolute Maximum Ratings

Supply Voltage . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input. . . . . ±10mA
DC Drain Current, Any One Output. . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 500ns Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 30% of VCC
Input High Voltage (VIH) . . . . . 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Y	TPHL TPLH	VCC = 4.5V	9	+25°C	2	21	ns
			10, 11	+125°C, -55°C	2	23	ns
Input to $\overline{Y}$	TPHL TPLH	VCC = 4.5V	9	+25°C	2	24	ns
			10, 11	+125°C, -55°C	2	27	ns
Select to Y	TPHL TPLH	VCC = 4.5V	9	+25°C	2	25	ns
			10, 11	+125°C, -55°C	2	29	ns
Select to $\overline{Y}$	TPHL TPLH	VCC = 4.5V	9	+25°C	2	29	ns
			10, 11	+125°C, -55°C	2	33	ns
$\overline{E}$ to Y	TPHL TPLH	VCC = 4.5V	9	+25°C	2	17	ns
			10, 11	+125°C, -55°C	2	19	ns
$\overline{E}$ to $\overline{Y}$	TPHL TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	21	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 45		pF
			1	+125°C	Typical 55		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	750	-	2000	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Input to Y	TPHL TPLH	VCC = 4.5V	+25°C	2	29	2	29	ns
Input to $\overline{Y}$	TPHL TPLH	VCC = 4.5V	+25°C	2	34	2	34	ns
Select to Y	TPHL TPLH	VCC = 4.5V	+25°C	2	37	2	37	ns
Select to $\overline{Y}$	TPHL TPLH	VCC = 4.5V	+25°C	2	42	2	42	ns
$\overline{E}$ to Y	TPHL TPLH	VCC = 4.5V	+25°C	2	24	2	24	ns
$\overline{E}$ to $\overline{Y}$	TPHL TPLH	VCC = 4.5V	+25°C	2	27	2	27	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE: Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
5, 6	1 - 4, 7 - 15	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
5, 6	8	-	1 - 4, 7, 9 - 16	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 2)					
-	2, 4, 8, 10, 13, 15	5, 6	1, 3, 9, 12, 14, 16	11	7

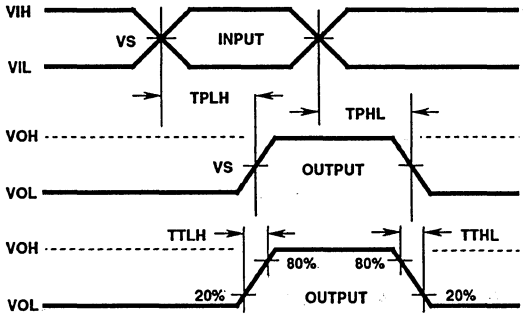
NOTES:
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
5, 6	8	1 - 4, 7, 9 - 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

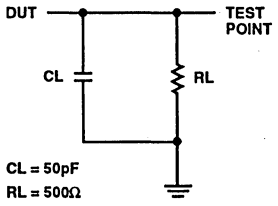
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
84 x 84 mils
2.13 x 2.13mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

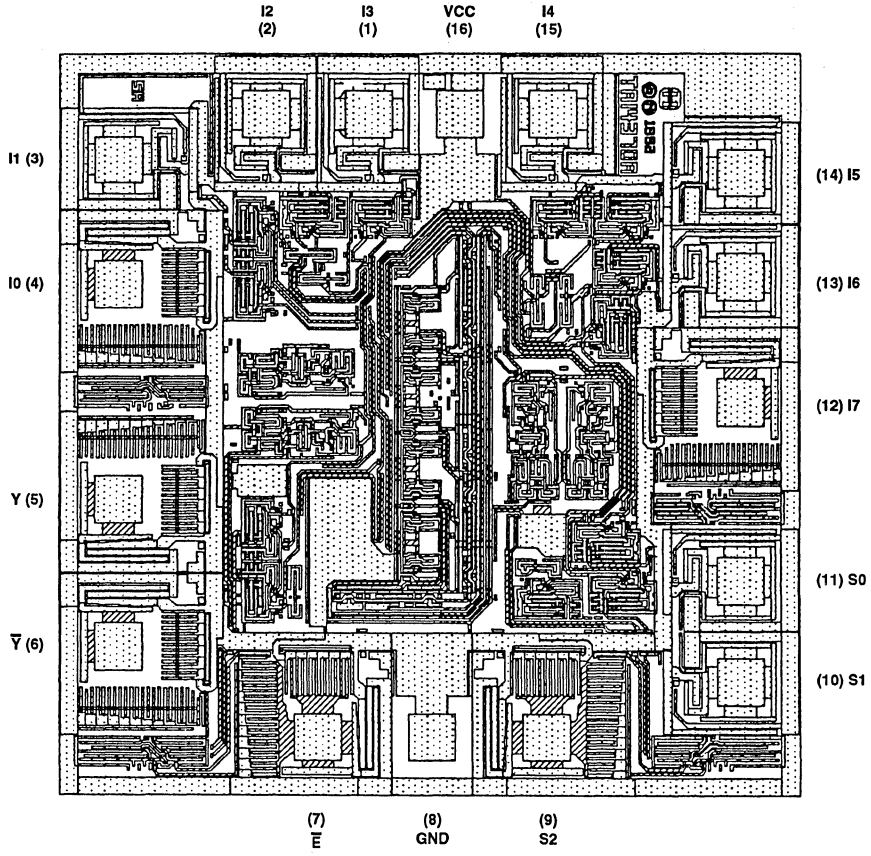
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCS151MS



HARRIS SEMICONDUCTOR

HCTS153MS

Radiation Hardened Dual 4-Input Multiplexer

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
- Military Temperature Range . . . . . -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range . . . . . 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

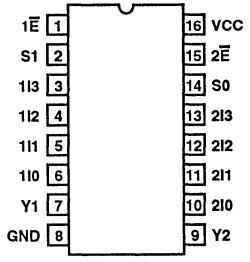
The Harris HCTS153MS is a Radiation Hardened dual 4-to-1 line selector/multiplexer which selects one of four sources for each section by the common select inputs, S0 and S1. When the enable inputs ($1\overline{E}$, $2\overline{E}$) are high, the outputs are in the low logic state.

The HCTS153MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

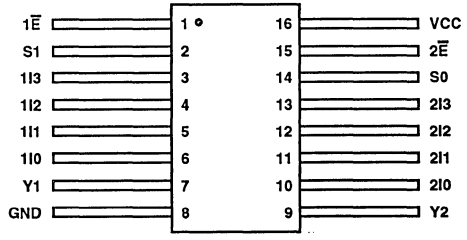
The HCTS153MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR, CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR, CDFP4-F16, LEAD FINISH C
TOP VIEW



Truth Table

SELECT INPUTS		DATA INPUTS				ENABLE	OUTPUT
S1	S0	I0	I1	I2	I3	$\overline{E}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

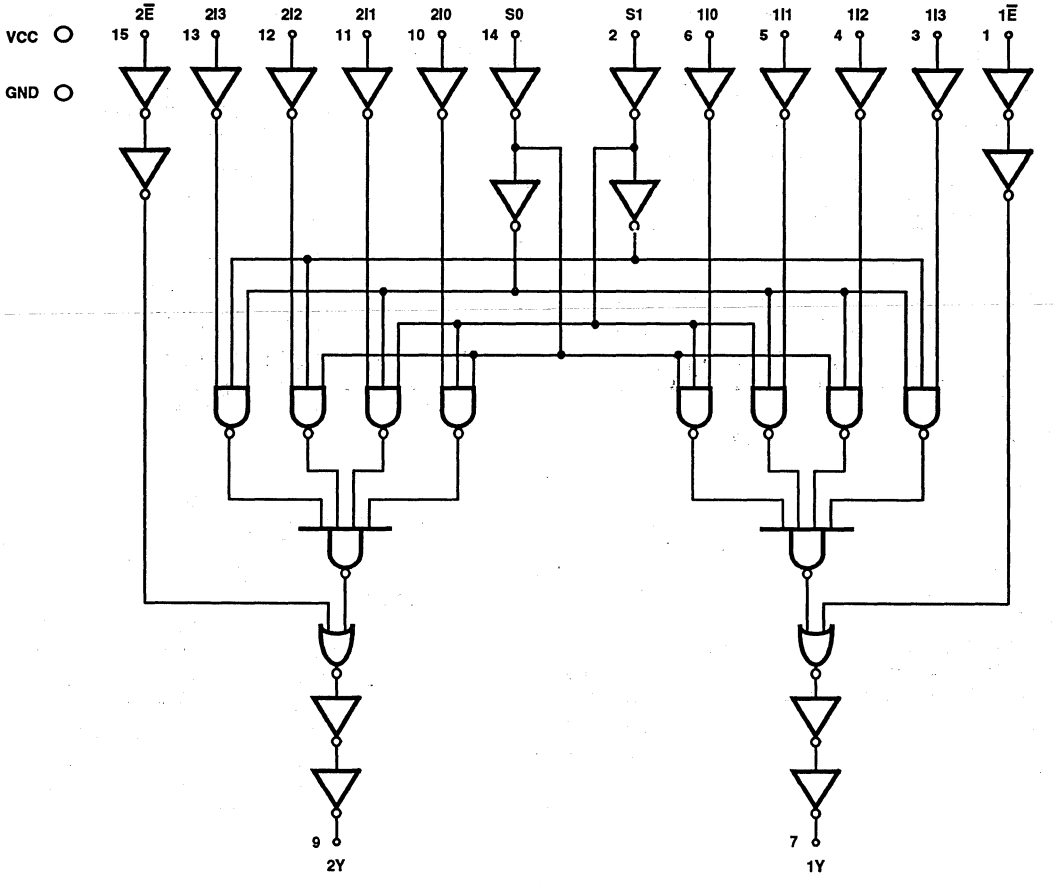
Select inputs A and B are common to both sections
H = High Level, L = Low Level, X = Immaterial

7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 2463.1

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Input Rise and Fall Times at VCC = 4.5V (TR, TF) . . . . . 500ns Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	0.5	µA
			2, 3	+125°C, -55°C	-5.0	5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Output	TPHL	VCC = 4.5V	9	+25°C	2	30	ns
			10, 11	+125°C, -55°C	2	34	ns
	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	23	ns
Select to Output	TPHL	VCC = 4.5V	9	+25°C	2	39	ns
			10, 11	+125°C, -55°C	2	46	ns
	TPLH	VCC = 4.5V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	32	ns
Enable to Data	TPHL	VCC = 4.5V	9	+25°C	2	17	ns
			10, 11	+125°C, -55°C	2	19	ns
	TPLH	VCC = 4.5V	9	+25°C	2	19	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 50		pF
			1	+125°C	Typical 60		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Output Voltage Low	VOL	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Input to Output	TPHL	VCC = 4.5V	+25°C	2	34	2	43	ns
	TPLH	VCC = 4.5V	+25°C	2	23	2	29	ns
Select to Data	TPHL	VCC = 4.5V	+25°C	2	46	2	58	ns
	TPLH	VCC = 4.5V	+25°C	2	32	2	40	ns
Enable to Data	TPHL	VCC = 4.5V	+25°C	2	19	2	24	ns
	TPLH	VCC = 4.5V	+25°C	2	22	2	28	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A inspection in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
7, 9	1 - 6, 8, 10 - 15	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
7, 9	8	-	1 - 6, 10 - 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	1, 3, 5, 8, 11, 13, 15	7, 9	4, 6, 10, 12, 16	14	2

NOTES:

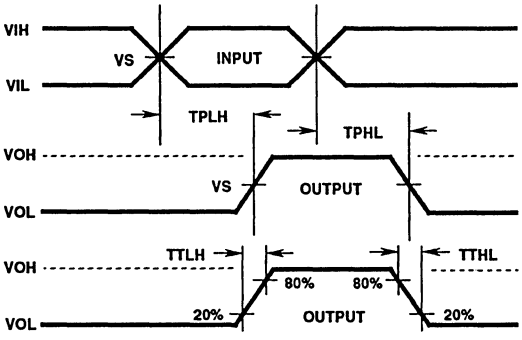
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in

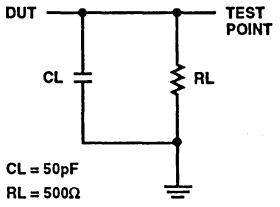
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
7, 9	8	1 - 6, 10 - 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

AC Timing Diagram and Load Circuit





AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
2.13 x 2.13 mils
84mm x 84mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

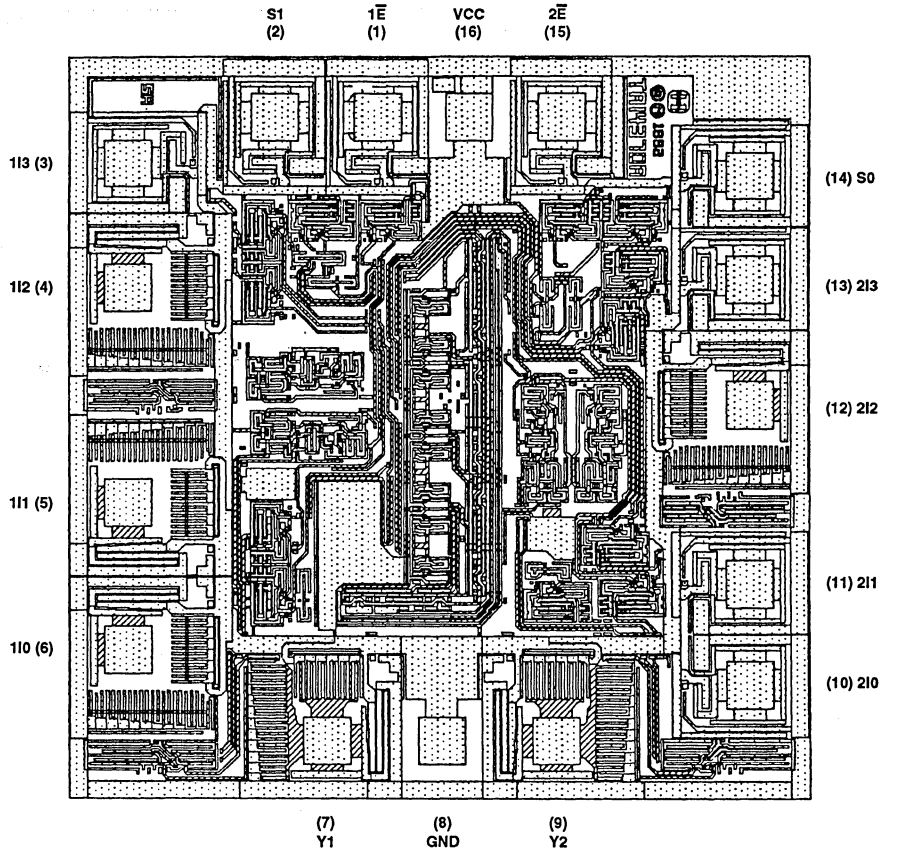
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCTS153MS



HARRIS SEMICONDUCTOR

HCS154MS

Radiation Hardened 4-to-16 Line Decoder/Demultiplexer

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity < 2 x 10^{-9} Errors/Gate Day (Typ)
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

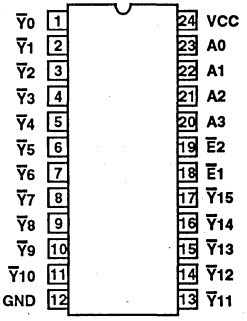
The Harris HCS154MS is a Radiation Hardened 4 to 16 line Decoder/Demultiplexer with two enable inputs. A high on either enable input forces the output to a high state. The Demultiplexing function is performed by using the four input lines A0 to A3 to select the desired output states.

The HCS154MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

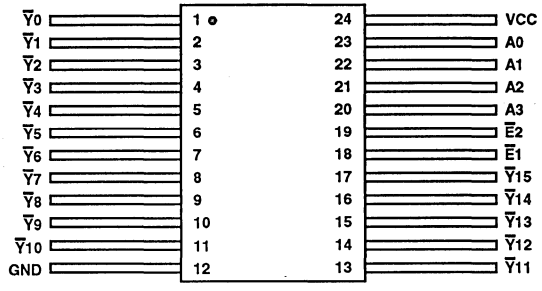
The HCS154MS is supplied in a 24 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

24 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835, DESIGNATOR CDIP2-T24, LEAD FINISH C
TOP VIEW



24 PIN CERAMIC FLAT PACK
MIL-STD-1835, DESIGNATOR CDFP4-F24, LEAD FINISH C
TOP VIEW



7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

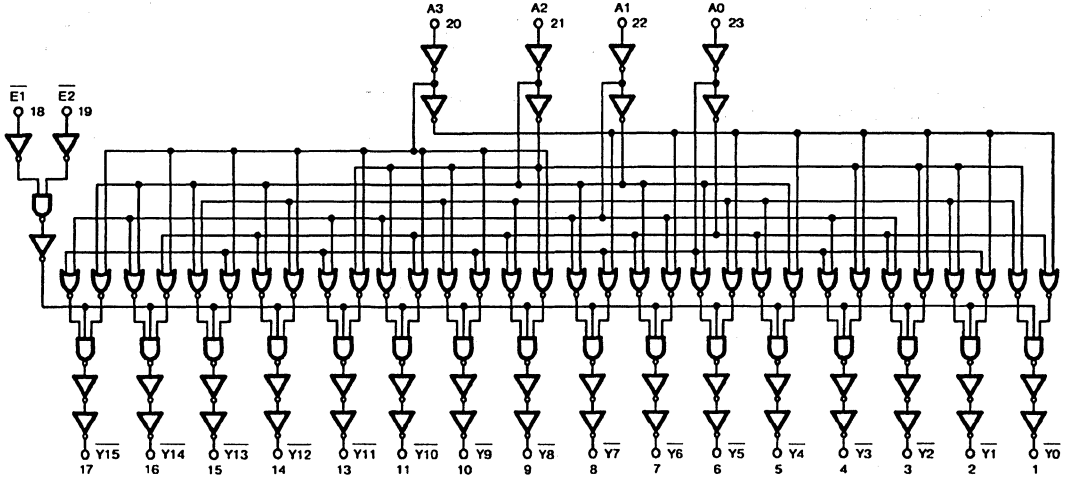
File Number **2479.1**

Truth Table

INPUTS						OUTPUTS														
$\overline{E1}$	$\overline{E2}$	A0	A1	A2	A3	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	$\overline{Y8}$	$\overline{Y9}$	$\overline{Y10}$	$\overline{Y11}$	$\overline{Y12}$	$\overline{Y13}$	$\overline{Y14}$	$\overline{Y15}$
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level, X = Immaterial

Functional Diagram



Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 100ns Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 30% of VCC
Input High Voltage (VIH) ..... 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), (Note 2) VIL = 0.30(VCC)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address to Output	TPLH	VCC = 4.5V	9	+25°C	2	29	ns
			10, 11	+125°C, -55°C	2	34	ns
	TPHL	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	31	ns
Enable to Output	TPLH TPHL	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	27	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 44		pF
			1	+125°C	Typical 49		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V or 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Address to Output	TPLH	VCC = 4.5V	+25°C	2	34	2	43	ns
	TPHL	VCC = 4.5V	+25°C	2	31	2	39	ns
Enable to Output	TPLH TPHL	VCC = 4.5V	+25°C	2	27	2	34	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
1 - 11, 13 - 17	12, 18 - 23	-	24	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
1 - 11, 13 - 17	12	-	18 - 24	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 2)					
-	12, 18 - 21	1 - 11, 13 - 17	24	23	22

NOTES:

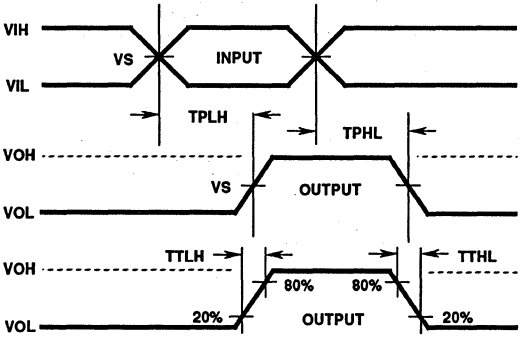
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
1 - 11, 13 - 17	12	18 - 24

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

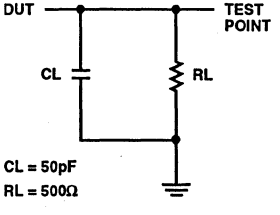
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
85 x 101 mils
2.16 x 2.57mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

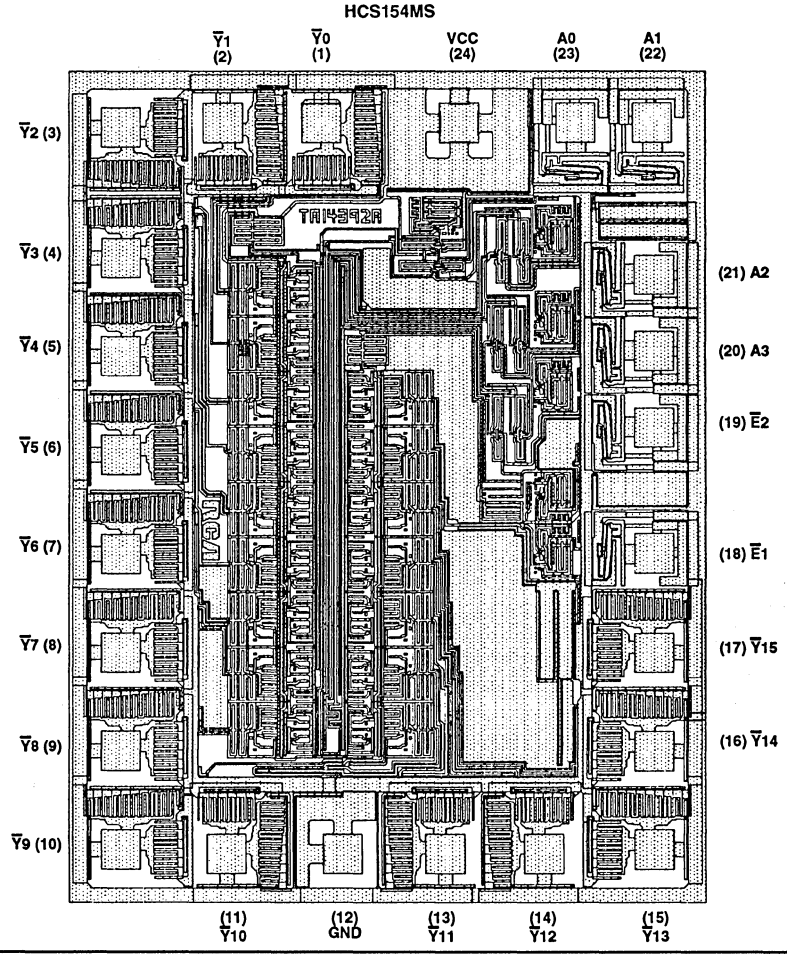
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HCTS157MS

Radiation Hardened Quad 2-Input Multiplexers

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
- Military Temperature Range . . . . . -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range . . . . . 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

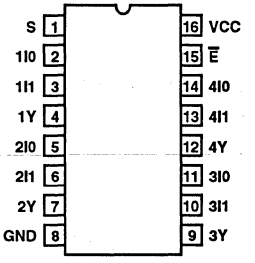
The Harris HCTS157MS is a Radiation Hardened quad 2-input multiplexers with select and enable inputs.

The HCTS157MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

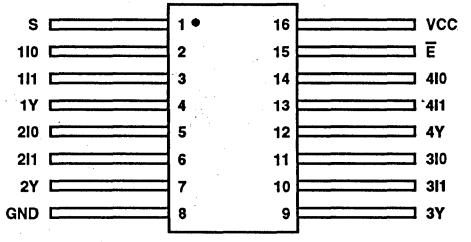
The HCTS157MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F16, LEAD FINISH C
TOP VIEW

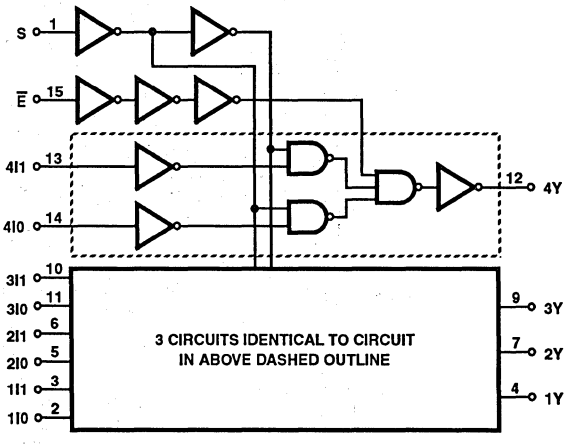


Truth Table

ENABLE	SELECT INPUTS	DATA INPUTS		OUTPUT
$\overline{E}$	S	I0	I1	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High Level
L = Low Level
X = Immaterial

Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2464.1**

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 500ns Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V	1	+25°C	-7.2	-	mA
			2, 3	+125°C, -55°C	-6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	0.5	µA
			2, 3	+125°C, -55°C	-5.0	5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Data to Output	TPHL	VCC = 4.5V	9	+25°C	2	26	ns
			10, 11	+125°C, -55°C	2	30	ns
	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	24	ns
Enable to Output	TPHL	VCC = 4.5V	9	+25°C	2	22	ns
			10, 11	+125°C, -55°C	2	25	ns
	TPLH	VCC = 4.5V	9	+25°C	2	22	ns
			10, 11	+125°C, -55°C	2	25	ns
Select to Output	TPHL	VCC = 4.5V	9	+25°C	2	31	ns
			10, 11	+125°C, -55°C	2	37	ns
	TPLH	VCC = 4.5V	9	+25°C	2	25	ns
			10, 11	+125°C, -55°C	2	29	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 36		pF
			1	+125°C	Typical 41		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHLTTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	5.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-5.0	-	mA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Data to Output	TPHL	VCC = 4.5V	+25°C	2	30	2	38	ns
	TPLH	VCC = 4.5V	+25°C	2	24	2	30	ns
Enable to Output	TPHL	VCC = 4.5V	+25°C	2	25	2	31	ns
	TPLH	VCC = 4.5V	+25°C	2	25	2	31	ns
Select to Output	TPHL	VCC = 4.5V	+25°C	2	37	2	24	ns
	TPLH	VCC = 4.5V	+25°C	2	29	2	28	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC BURN-IN AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
4, 7, 9, 12	1 - 3, 5, 6, 8, 10, 11, 13 - 15	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
4, 7, 9, 12	8	-	1 - 3, 5, 6, 10, 11, 13 - 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	8, 15	4, 7, 9, 12	16	2, 3, 5, 6, 10, 11, 13, 14	1

NOTES:

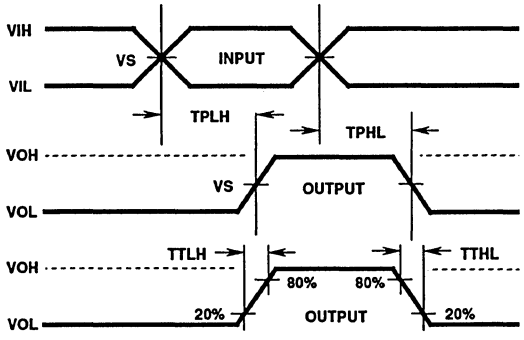
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 680Ω ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

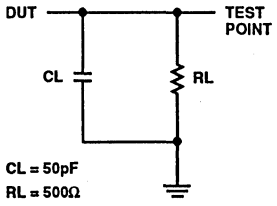
OPEN	GROUND	VCC = 5V ± 0.5V
4, 7, 9, 12	8	1, 2, 3, 5, 6, 10, 11, 13 - 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

AC Timing Diagrams



AC Load Circuit



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
84 x 84 mils

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

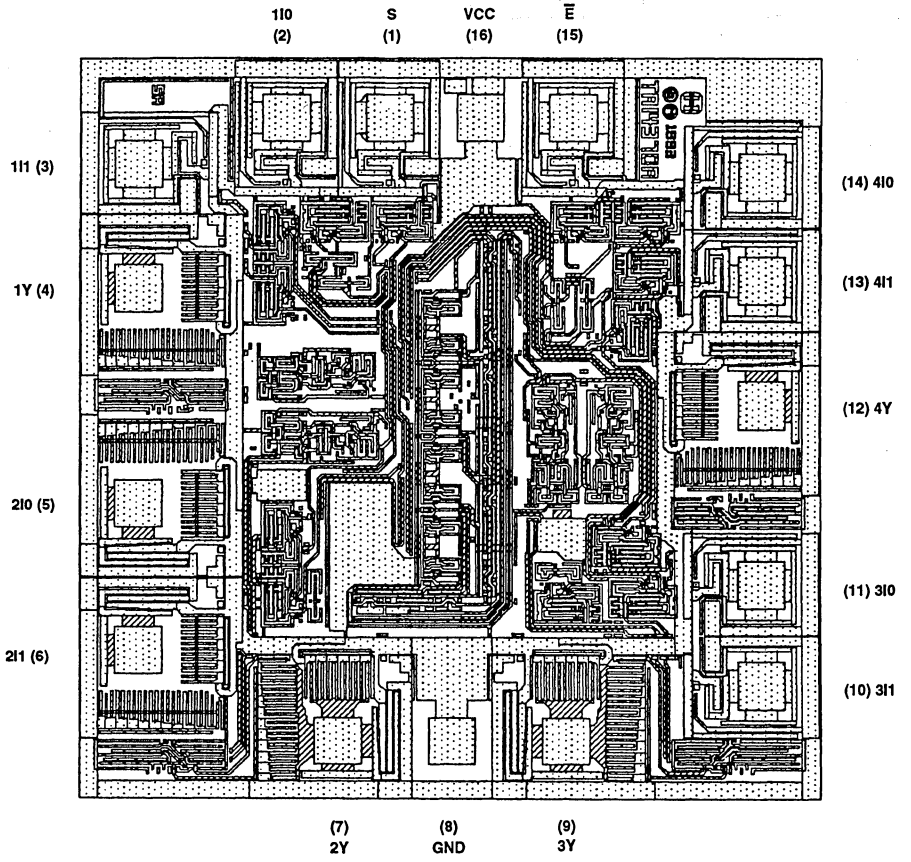
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS157MS



HARRIS SEMICONDUCTOR

HCTS160MS

Radiation Hardened Synchronous Counter

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Rate 2 x 10^{-9} Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Standard Outputs..... 10 LSTTL Loads
- Military Temperature Range ..... -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range .....4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA @ VOL, VOH

Description

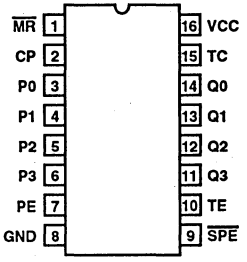
The Harris HCTS160MS is a Radiation Hardened high speed presettable BCD decade synchronous counter that features an asynchronous reset and look-ahead carry logic. Counting and parallel presetting are accomplished synchronously with the low-to-high transition of the clock. A low level on the synchronous parallel enable input, $\overline{SPE}$, disables counting and allows data at the preset inputs, P0 - P3, to be loaded into the counter. The counter is reset by a low on the master reset input, $\overline{MR}$. Two count enables, PE and TE are provided for n-bit cascading. TE also controls the terminal count output, TC. The terminal count output indicates a maximum count for one clock pulse and is used to enable the next cascaded stage to count.

The HCTS160MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

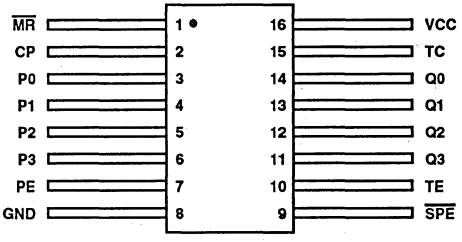
The HCTS160MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F16, LEAD FINSIH C
TOP VIEW



7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2484.1**

Truth Table

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	PE	TE	$\overline{SPE}$	Pn	Qn	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(Note 1)
Count	H	↑	h	h	h (Note 3)	X	Count	(Note 1)
Inhibit	H	X	l (Note 2)	X	h (Note 3)	X	qn	(Note 1)
	H	X	X	l (Note 2)	h (Note 3)	X	qn	L

H = HIGH Voltage Level

L = LOW Voltage Level

h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition

X = Immaterial

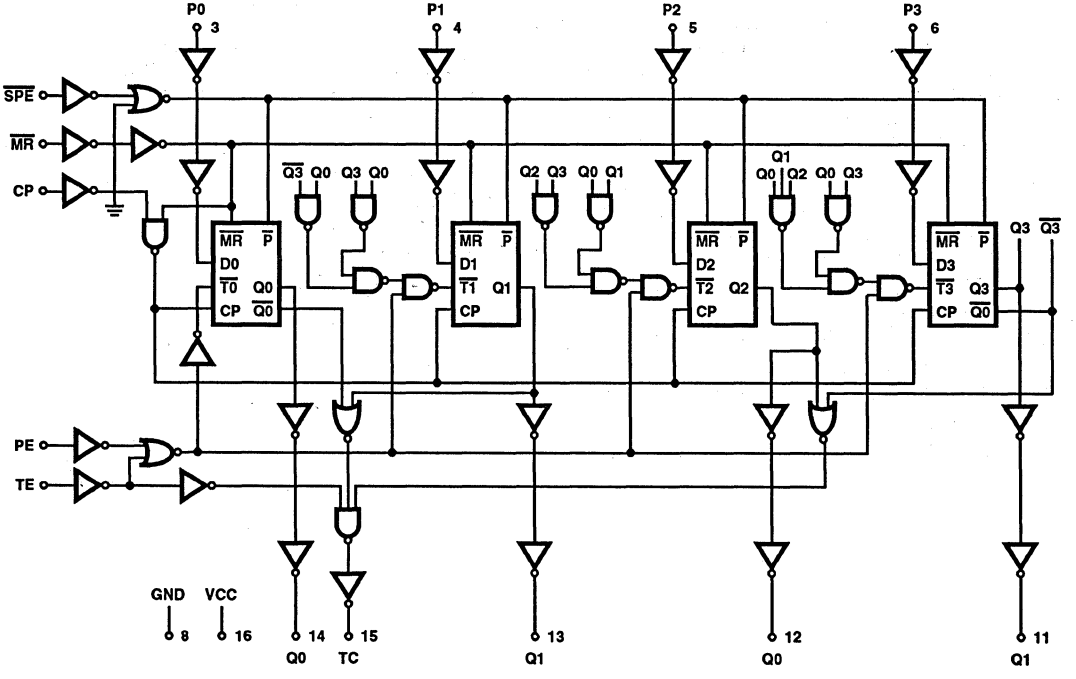
q = Lower case letterindicate the state of the referenced output prior to the LOW-to-HIGH clock transition

↑ = LOW-to-HIGH clock transition

NOTES:

1. The TC output is HIGH when TE is HIGH and the counter is at terminal count (HHHH for 161 and HLLH for 160)
2. The HIGH-to-LOW transition of PE or TE on the 54/74161 and 54/74160 should only occur while CP is high for conventional operation
3. The LOW-to-HIGH transition of $\overline{SPE}$ on the 54/74161 and 54/74160 should only occur while CP is high for conventional operation

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

	θ_{ja}	θ_{jc}
Thermal Impedance		
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 500ns Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	0.5	µA
			2, 3	+125°C, -55°C	-5.0	5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
CP to QN	TPHL	VCC = 4.5V	9	+25°C	2	26	ns
			10, 11	+125°C, -55°C	2	30	ns
	TPLH	VCC = 4.5V	9	+25°C	2	23	ns
			10, 11	+125°C, -55°C	2	26	ns
CP to TC	TPHL	VCC = 4.5V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	32	ns
	TPLH	VCC = 4.5V	9	+25°C	2	24	ns
			10, 11	+125°C, -55°C	2	28	ns
TE to TC	TPHL	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	29	ns
	TPLH	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns
$\overline{MR}$ to QN, TC	TPHL	VCC = 4.5V	9	+25°C	2	46	ns
			10, 11	+125°C, -55°C	2	51	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 69		pF
			1	+125°C	Typical 173		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K LIMITS		1M LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50μA	+25°C	-	-0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
CP to QN	TPHL	VCC = 4.5V	+25°C	2	30	2	38	ns
	TPLH	VCC = 4.5V	+25°C	2	26	2	33	ns
CP to TC	TPHL	VCC = 4.5V	+25°C	2	32	2	40	ns
	TPLH	VCC = 4.5V	+25°C	2	28	2	35	ns
TE to TC	TPHL	VCC = 4.5V	+25°C	2	29	2	37	ns
	TPLH	VCC = 4.5V	+25°C	2	20	2	25	ns
$\overline{MR}$ to QN, TC	TPHL	VCC = 4.5V	+25°C	2	51	2	64	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/6005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of Mil-Std-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% go/no-go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC I BURN-IN					
11 - 15	1 - 10	-	16	-	-
STATIC II BURN-IN					
11 - 15	8	-	1 - 7, 9, 10, 16	-	-
DYNAMIC BURN-IN					
-	4, 6, 8	11 - 15	1, 3, 5, 7, 9, 10, 16	2	-

NOTES:

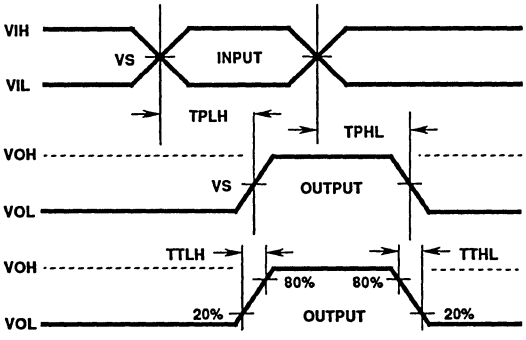
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in

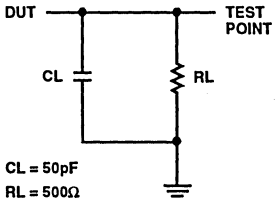
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
11 - 15	8	1 - 7, 9, 10, 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

AC Timing Diagrams and Load Circuit





AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
104 x 86 mils

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

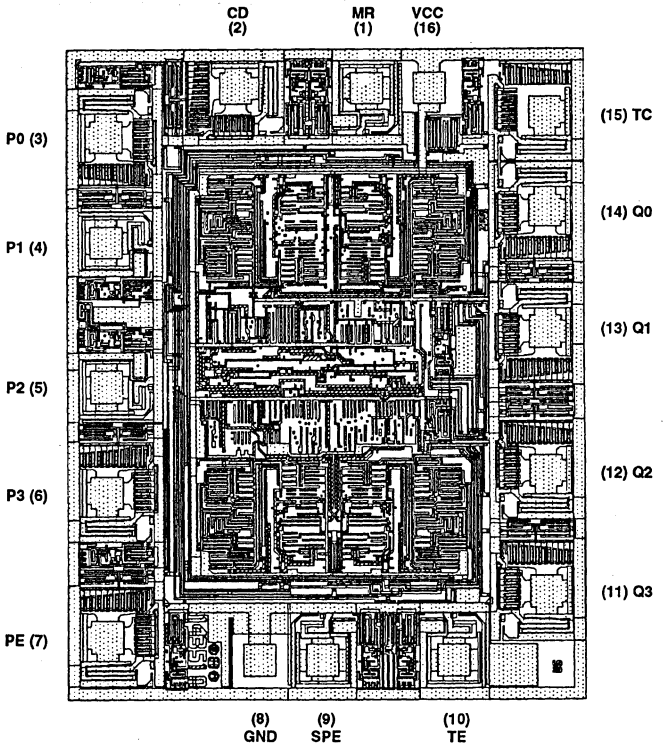
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS160MS



HARRIS SEMICONDUCTOR

HCS161MS

Radiation Hardened Synchronous Counter

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity 2 x 10^{-9} Error/Bit Day (Typ)
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.3 VCC Max
  - VIH = 0.7 VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

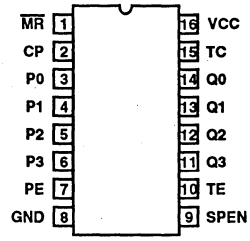
The Harris HCS161MS is a Radiation Hardened 4-Input Binary; synchronous counter featuring asynchronous reset and look-ahead carry logic. The HCS161 has an active-low master reset to zero, $\overline{MR}$. A low level at the synchronous parallel enable, $\overline{SPE}$, disables counting and allows data at the preset inputs (p0 - p3) to load the counter. The data is latched to the outputs on the positive edge of the clock input, CP. The HCS161MS has two count output, IC. The terminal count output indicates a maximum count for one clock pulse and is used to enable the next cascaded stage to count.

The HCS161MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

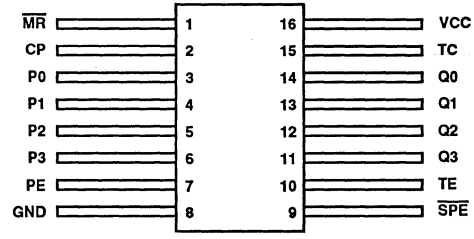
The HCS161MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835, DESIGNATOR CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-1835, DESIGNATOR CDFP4-F16, LEAD FINISH C
TOP VIEW



Truth Table

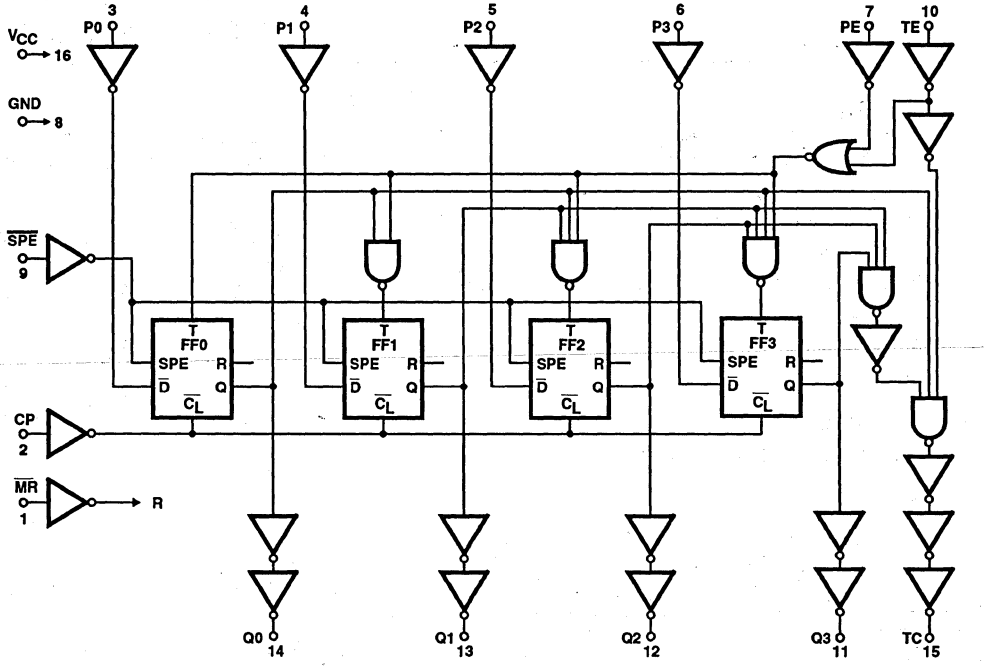
OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	PE	TE	$\overline{SPE}$	Pn	Qn	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	↗	X	X	l	l	L	L
	H	↗	X	X	l	h	H	(a)
Count	H	↗	h	h	h (c)	X	Count	(a)
Inhibit	H	X	l (b)	X	h (c)	X	qn	(a)
	H	X	X	l (b)	h (c)	X	qn	L

H = High Level, L = Low Level, X = Immaterial, ↗ = Transition from low to high

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2469.1**

Functional Diagram



Absolute Maximum Ratings

Supply Voltage . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input. . . . . ±10mA
DC Drain Current, Any One Output. . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 100ns Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 30% of VCC
Input High Voltage (VIH) . . . . . 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CP to Qn	TPHL TPLH	VCC = 4.5V	9	+25°C	2	34	ns
			10, 11	+125°C, -55°C	2	39	ns
CP to TC	TPHL TPLH	VCC = 4.5V	9	+25°C	2	37	ns
			10, 11	+125°C, -55°C	2	42	ns
TE to TC	TPHL TPLH	VCC = 4.5V	9	+25°C	2	23	
			10, 11	+125°C, -55°C	2	26	
$\overline{MR}$ to Qn	TPHL	VCC = 4.5V	9	+25°C	2	41	ns
			10, 11	+125°C, -55°C	2	45	ns
$\overline{MR}$ to TC	TPHL	VCC = 4.5V	9	+25°C	2	46	ns
			10, 11	+125°C, -55°C	2	51	ns

NOTES:
1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 36		pF
			1	+125°C	Typical 56		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:
1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
CP to Qn	TPHL	VCC = 4.5V	+25°C	2	39	2	50	ns
	TPLH	VCC = 4.5V	+25°C	2	39	2	50	ns
CP to TC	TPHL	VCC = 4.5V	+25°C	2	43	2	53	ns
	TPLH	VCC = 4.5V	+25°C	2	43	2	53	ns
TE to TC	TPHL	VCC = 4.5V	+25°C	2	27	2	33	ns
	TPLH	VCC = 4.5V	+25°C	2	27	2	33	ns
$\overline{MR}$ to Qn	TPHL	VCC = 4.5V	+25°C	2	45	2	56	ns
$\overline{MR}$ to TC	TPHL	VCC = 4.5V	+25°C	2	51	2	63	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
11 - 15	1 - 10	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
11 - 15	8	-	1 - 7, 9, 10, 16	-	-
DYNAMIC BURN-IN I TEST CONNECTIONS (Note 2)					
-	4, 6, 8	11 - 15	1, 3, 5, 7, 9, 10, 16	2	-

NOTES:

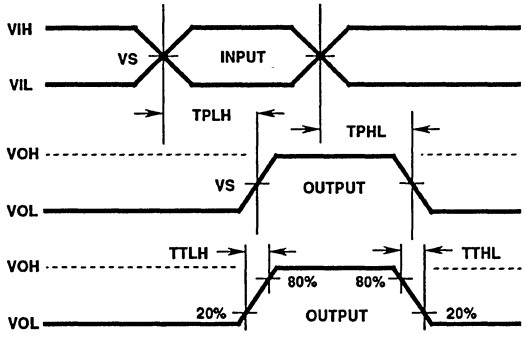
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
11 - 15	8	1 - 7, 9, 10, 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

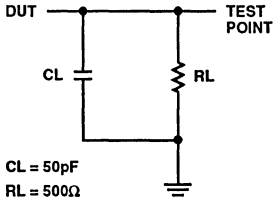
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
104 x 86 mils
2650 x 2190mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

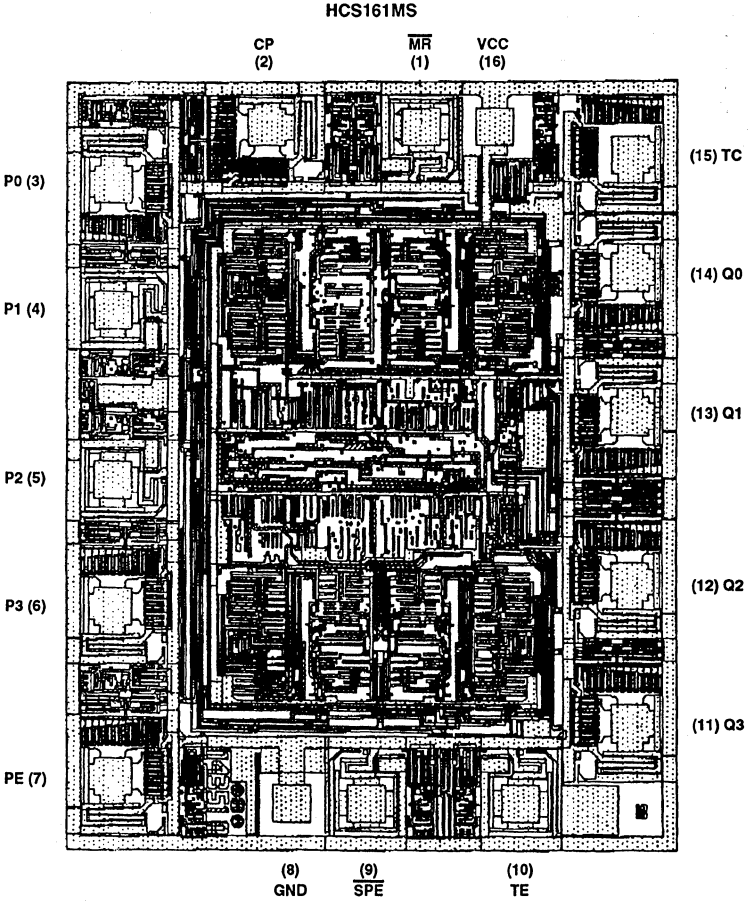
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HCTS161MS

Radiation Hardened Synchronous Counter

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity 2 x 10^{-9} Error/Bit Day (Typ)
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Standard Outputs - 10 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

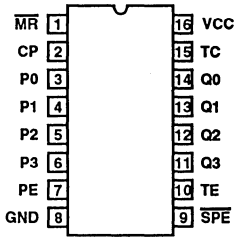
The Harris HCTS161MS high-reliability high-speed presettable four-bit binary synchronous counter features asynchronous reset and look-ahead carry logic. The HCS161 has an active-low master reset to zero, $\overline{MR}$. A low level at the synchronous parallel enable, $\overline{SPE}$, disables counting and allows data at the preset inputs (P0 - P3) to load the counter. The data is latched to the outputs on the positive edge of the clock input, CP. The HCTS161MS has two count enable pins, PE and TE. TE also controls the terminal count output, TC. The terminal count output indicates a maximum count for one clock pulse and is used to enable the next cascaded stage to count.

The HCTS161MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

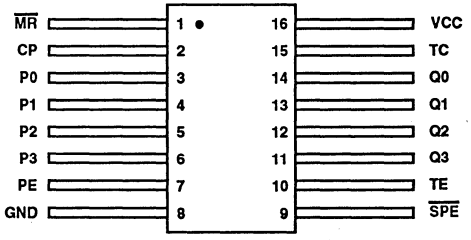
The HCTS161MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR, CDIP2-T16, LEAD FINISH C
TOP VIEW



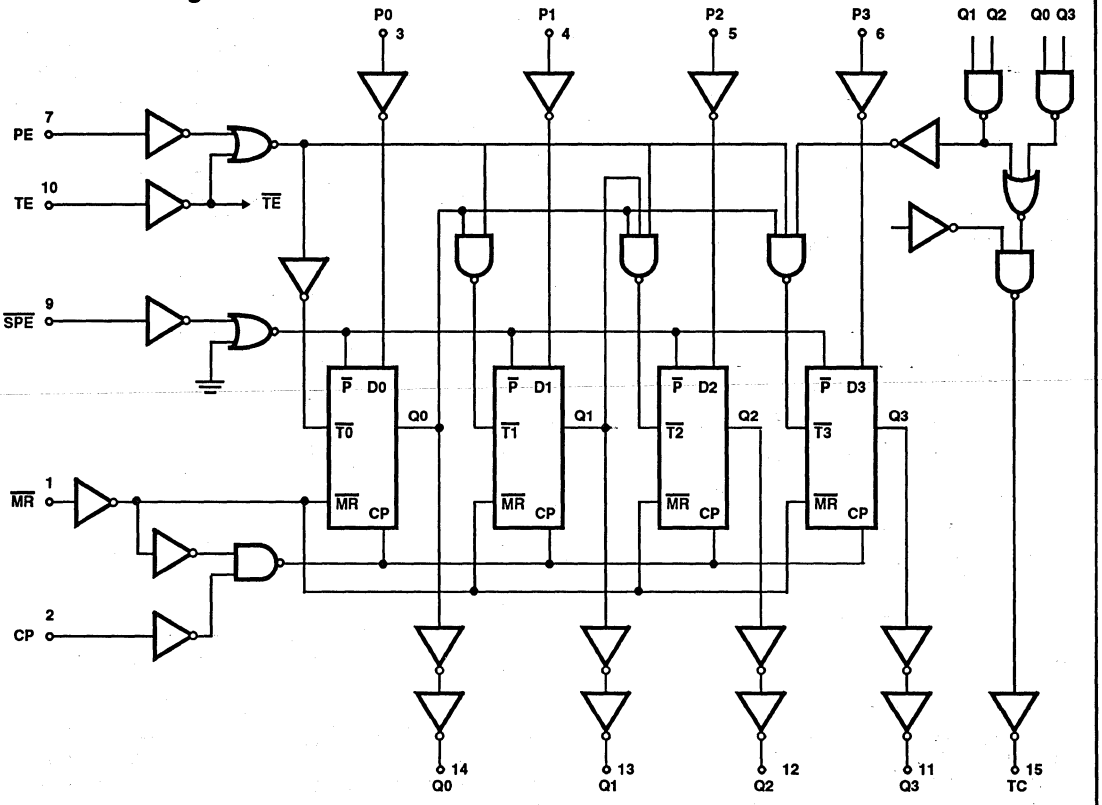
16 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR, CDFP4-F16, LEAD FINISH C
TOP VIEW



7 LOGIC

File Number **2144.1**

Functional Diagram



Truth Table

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	PE	TE	$\overline{SPE}$	Pn	Qn	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	⎍	X	X	l	l	L	L
	H	⎍	X	X	l	h	H	(a)
Count	H	⎍	h	h	h (c)	X	Count	(a)
Inhibit	H	X	l (b)	X	h (c)	X	qn	(a)
	H	X	X	l (b)	h (c)	X	qn	L

H = High Level, L = Low Level, X = Immaterial,
h = HIGH-voltage level one setup time prior to the LOW-to-HIGH clock transition,
l = LOW-voltage level one setup time prior to the LOW-to-HIGH clock transition,
q = Lower-case letters indicate the state of the referencedoutput prior to the LOW-to-HIGH clock transition.
⎍ = Transition from low to high

NOTES:

1. The TC output is HIGH when TE is HIGH and the counter is at Terminal count (HHHH).
2. The HIGH-to-LOW transition of $\overline{SPE}$ should only occur while CP is HIGH for conventional operation.

Absolute Maximum Ratings

Supply Voltage (VCC) ..... -0.5 to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC) ..... +4.5V to +5.5V
Input Rise and Fall Times at VCC = 4.5V (TR, TF) ..... 500ns Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	0.5	µA
			2, 3	+125°C, -55°C	-5.0	5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CP to Qn	TPLH	VCC = 4.5V	9	+25°C	2	23	ns
			10, 11	+125°C, -55°C	2	28	ns
	TPHL	VCC = 4.5V	9	+25°C	2	31	ns
			10, 11	+125°C, -55°C	2	36	ns
CP to TC	TPLH	VCC = 4.5V	9	+25°C	2	25	ns
			10, 11	+125°C, -55°C	2	30	ns
	TPHL	VCC = 4.5V	9	+25°C	2	32	ns
			10, 11	+125°C, -55°C	2	37	ns
TE to TC	TPLH	VCC = 4.5V	9	+25°C	2	15	ns
			10, 11	+125°C, -55°C	2	18	ns
	TPHL	VCC = 4.5V	9	+25°C	2	22	
			10, 11	+125°C, -55°C	2	25	
$\overline{MR}$ to Qn	TPHL	VCC = 4.5V	9	+25°C	2	34	ns
			10, 11	+125°C, -55°C	2	39	ns
$\overline{MR}$ to TC	TPHL	VCC = 4.5V	9	+25°C	2	36	ns
			10, 11	+125°C, -55°C	2	41	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 40		pF
			1	+125°C	Typical 64		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/ 2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
CP to Qn	TPHL	VCC = 4.5V	+25°C	2	28	2	31	ns
	TPLH	VCC = 4.5V	+25°C	2	36	2	39	ns
CP to TC	TPHL	VCC = 4.5V	+25°C	2	30	2	33	ns
	TPLH	VCC = 4.5V	+25°C	2	37	2	40	ns
TE to TC	TPHL	VCC = 4.5V	+25°C	2	18	2	21	ns
	TPLH	VCC = 4.5V	+25°C	2	25	2	28	ns
$\overline{MR}$ to Qn	TPHL	VCC = 4.5V	+25°C	2	39	2	42	ns
$\overline{MR}$ to TC	TPHL	VCC = 4.5V	+25°C	2	41	2	44	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

				OSCILLATOR	
OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
11 - 15	1 - 10	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
11 - 15	8	-	1 - 7, 9, 10, 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	4, 6, 8	11 - 15	1, 3, 5, 7, 9, 10, 16	2	-

NOTES:

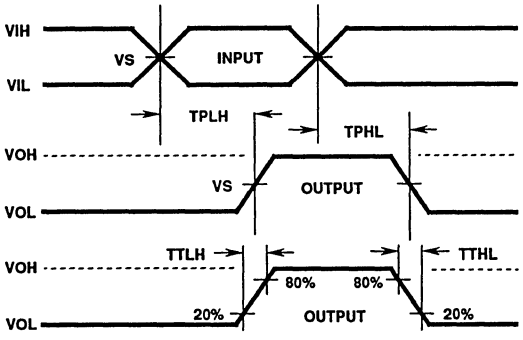
1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1kΩ ± 5% for dynamic burn-in

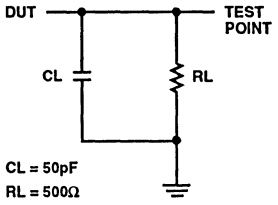
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
11 - 15	8	1 - 7, 9, 10, 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

AC Timing Diagram and Load Circuit





AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
86 x 71 mils

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

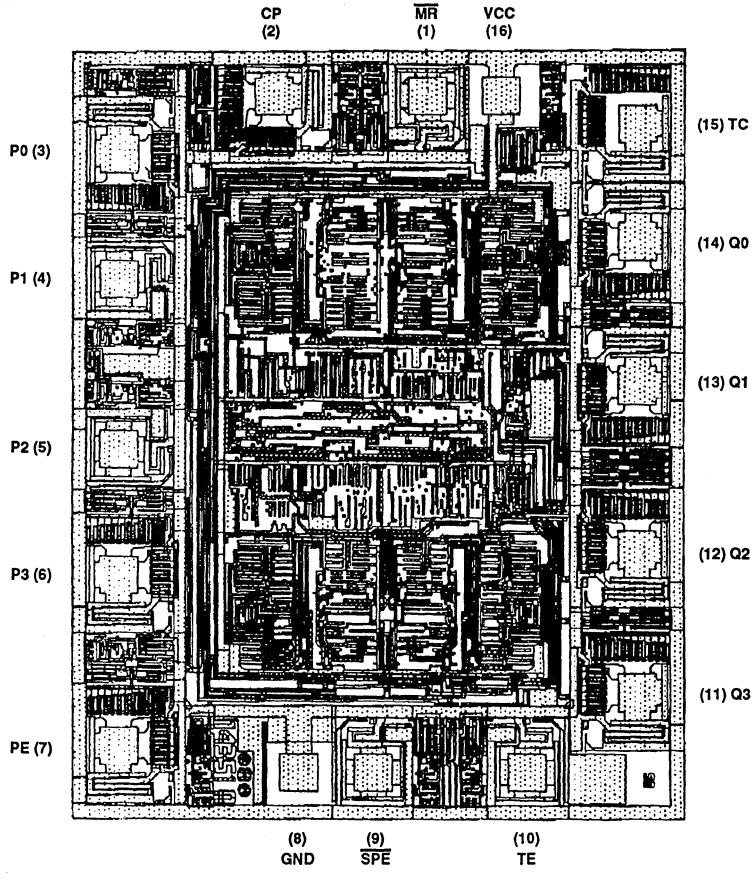
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCTS161MS



HARRIS SEMICONDUCTOR

HCTS163MS

Radiation Hardened Synchronous Counter

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Rate 2 x 10^{-9} Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
- Military Temperature Range . . . . . -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range . . . . . 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

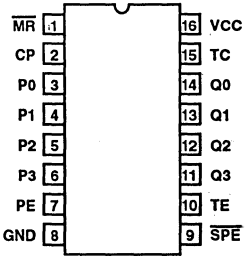
The Harris HCTS163MS is a Radiation Hardened synchronous presettable counter that feature look-ahead carry logic for use in high speed counting application. HCTS163MS is a binary counter, and is reset synchronously with the clock. Counting and parallel presetting are both accomplished synchronously with the negative to positive transition of the clock.

The HCTS163MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

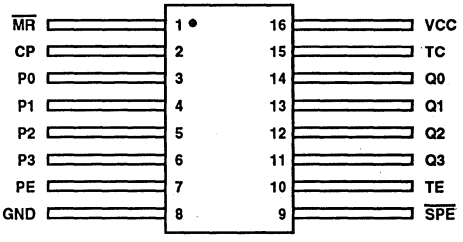
The HCTS163MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F16, LEAD FINISH C
TOP VIEW



7 LOGIC

File Number **2480.1**

Truth Table

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	PE	TE	$\overline{SPE}$	PN	QN	TC
Reset (clear)	l	⎍	X	X	X	X	L	L
Parallel Load	h (Note 3)	⎍	X	X	l	l	L	L
	h (Note 3)	⎍	X	X	l	h	H	(Note 1)
Count	h (Note 3)	⎍	h	h	h (Note 3)	X	Count	(Note 1)
Inhibit	h (Note 3)	X	l (Note 2)	X	h (Note 3)	X	Qn	(Note 1)
	h (Note 3)	X	X	l (Note 2)	h (Note 3)	X	Qn	L

H = HIGH Voltage Level

L = LOW Voltage Level

h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition

X = Immaterial

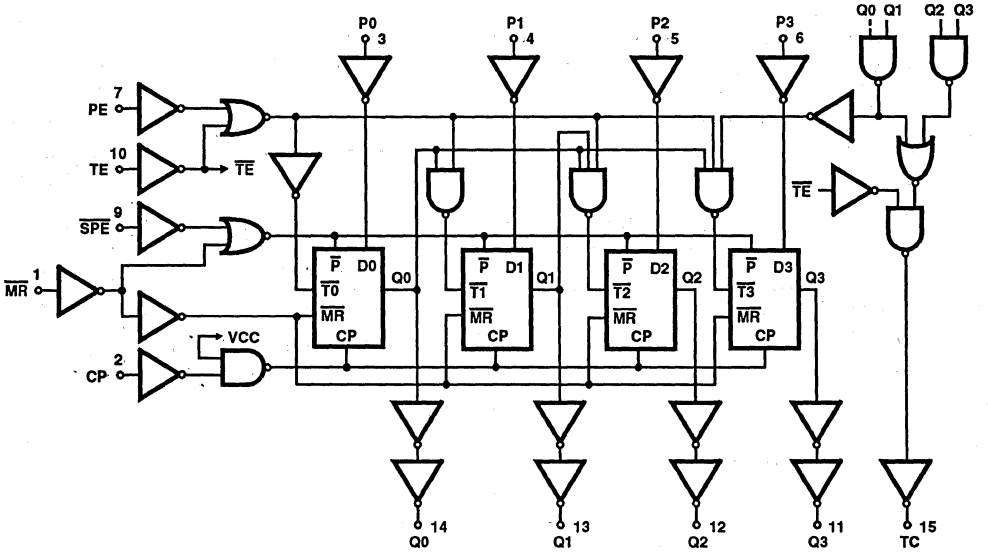
q = Lower case letter indicate the state of the referenced output prior to the LOW-to-HIGH clock transition

⎍ = LOW-to-HIGH clock transition

NOTES:

1. The TC output is HIGH when TE is HIGH and the counter is at terminal count.(HLLH for 162 and HHHH for 163)
2. The HIGH-to-LOW transition of PE or TE on the 54/74163 and 54/74160 should only occur while CP is high for conventional operation
3. The LOW-to-HIGH transition of $\overline{SPE}$ or $\overline{MR}$ on the 54/74163 should only occur while CP is high for conventional operation

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

	θ_{ja}	θ_{jc}
Thermal Impedance		
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5 VCC (TR, TF) . . . . . 500ns Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	0.5	µA
			2, 3	+125°C, -55°C	-5.0	5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CP to Qn	TPHL TPLH	VCC = 4.5V	9	+25°C	2	25	ns
			10, 11	+125°C, -55°C	2	29	ns
CP to TC	TPHL TPLH	VCC = 4.5V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	33	ns
$\overline{MR}$ to Qn, TC	TPHL	VCC = 4.5V	9	+25°C	2	50	ns
			10, 11	+125°C, -55°C	2	75	ns
TE to TC	TPHL	VCC = 4.5V	9	+25°C	2	23	ns
			10, 11	+125°C, -55°C	2	29	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	+25°C	Typical 52		pF
			+125°C	Typical 117		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	+25°C	-	10	pF
			+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	+25°C	-	15	ns
			+125°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
CP to Qn	TPHL TPLH	VCC = 4.5V	+25°C	2	29	2	36	ns
CP to TC	TPLH TPLH	VCC = 4.5V	+25°C	2	33	2	40	ns
$\overline{MR}$ to Qn, TC	TPHL	VCC = 4.5V	+25°C	2	75	2	90	ns
TE to TC	TPHL	VCC = 4.5V	+25°C	2	29	2	29	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

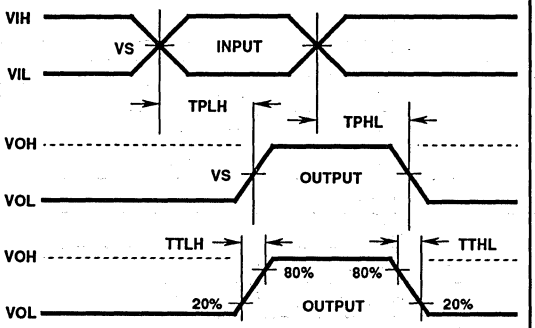
TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
11 - 15	1 - 10	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
11 - 15	8	-	1 - 7, 9, 10, 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	4, 6, 8	11 - 15	1, 3, 5, 7, 9, 10, 16	2	-

NOTES:

1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in

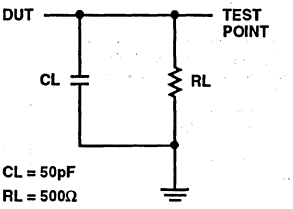
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
104 x 86 mils

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

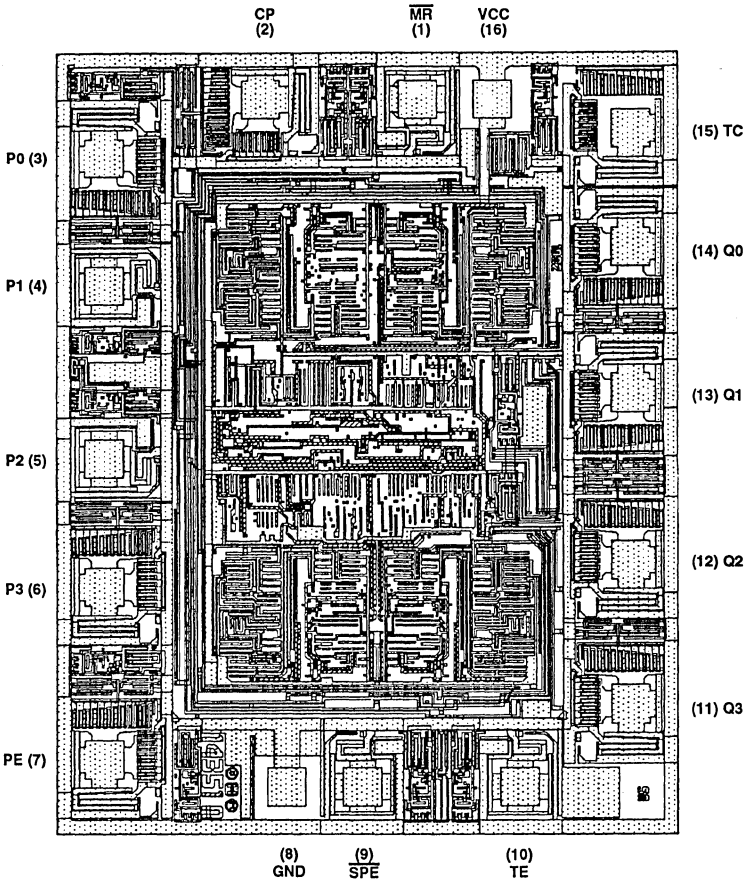
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$< 2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS163MS



HARRIS SEMICONDUCTOR

HCS164MS

Radiation Hardened 8-Bit Serial-In/Parallel-Out Register

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Rate 2 x 10^{-9} Errors/Bit Day
- Latch-Up-Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Standard Outputs - 10 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.3 VCC Max
  - VIH = 0.7 VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

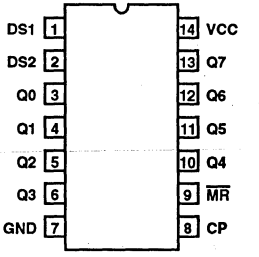
The Harris HCS164MS is a Radiation Hardened 8-bit Serial-In/Parallel-Out Shift Register that has fully synchronous serial data entry and an asynchronous master reset.

The HCS164MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

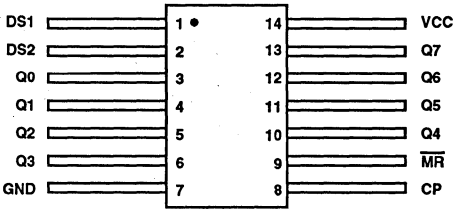
The HCS164MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW



Truth Table

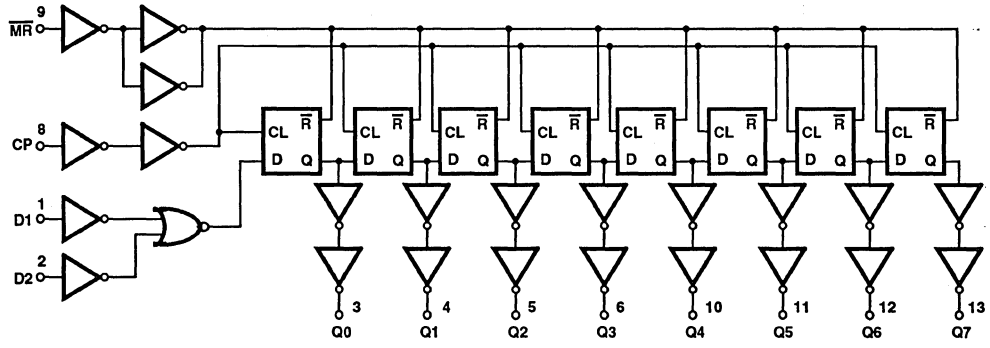
OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{MR}$	CP	DS1	DS2	Q0	Q1-Q7
Reset (Clear)	L	X	X	X	L	L-L
Shift	H	⎍	l	l	L	q0 -q6
	H	⎍	l	h	L	q0 - q6
	H	⎍	h	l	L	q0 - q6
	H	⎍	h	h	H	q0 - q6

H = High Voltage Level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transistion
L = Low VoltageLevel
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
⎍ = LOW-to-HIGH clock transition
q = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2465.1**

Functional Diagram



Absolute Maximum Ratings

Supply Voltage (VCC) ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{JA}	θ_{JC}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5 VCC (TR, TF) ..... 500ns Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 30% of VCC
Input High Voltage (VIH) ..... 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CP to Qn	TPLH TPHL	VCC = 4.5V	9	+25°C	2	32	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	37	ns
$\overline{MR}$ to Qn	TPHL	VCC = 4.5V	9	+25°C	2	32	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	37	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 90		pF
			1	+125°C	Typical 110		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
CP to Qn	TPHL TPLH	VCC = 4.5V	+25°C	2	37	2	46.25	ns
$\overline{MR}$ to Qn	TPHL	VCC = 4.5V	+25°C	2	37	2	46.25	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
3 - 6, 10 - 13	1, 2, 7 - 9	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3 - 6, 10 - 13	7	-	1, 2, 8, 9, 14	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	7	3 - 6, 10 - 13	9, 14	8	1, 2

NOTES:

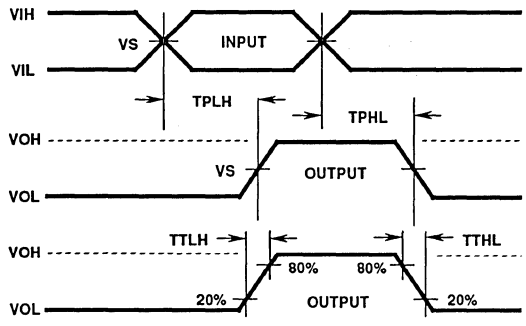
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3 - 6, 10 - 13	7	1, 2, 8, 9, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

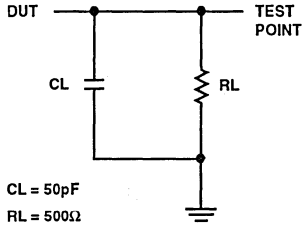
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
95 x 94mils

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

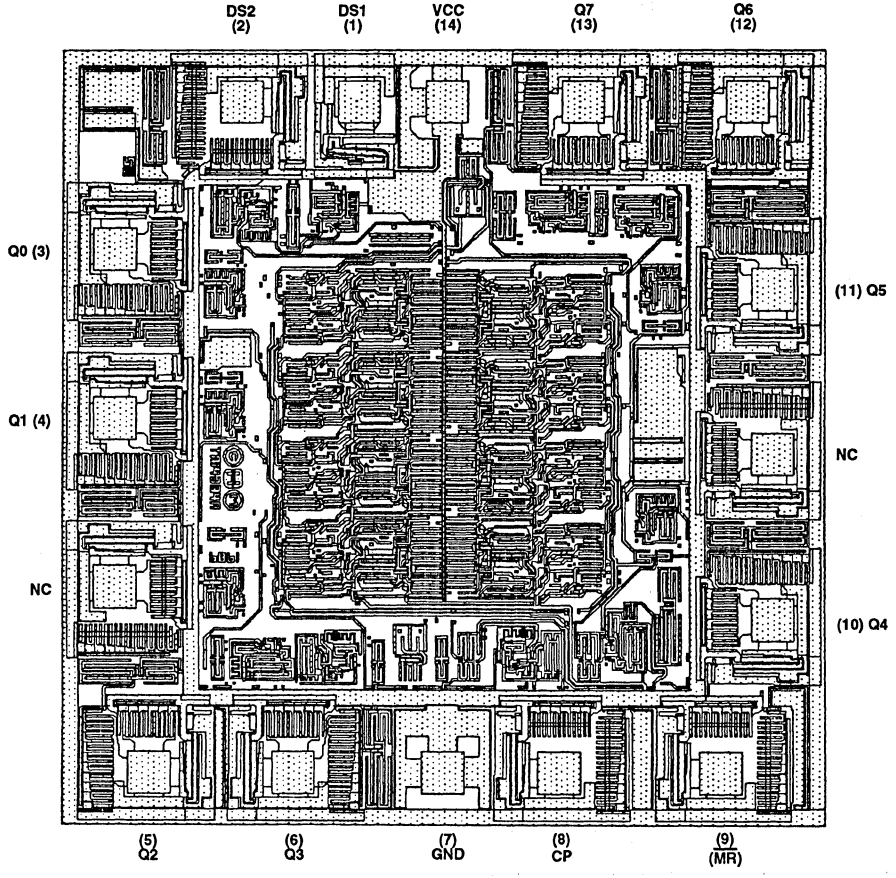
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$< 2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCS164MS



HARRIS SEMICONDUCTOR

HCTS164MS

Radiation Hardened 8-Bit Serial-In/Parallel-Out Register

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Rate 2 x 10^{-9} Errors/Bit Day
- Latch-Up-Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.8 VCC Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

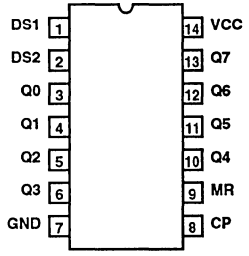
The Harris HCTS164MS is a Radiation Hardened 8-bit Serial-In/Parallel-Out Shift Register with asynchronous reset.

The HCTS164MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

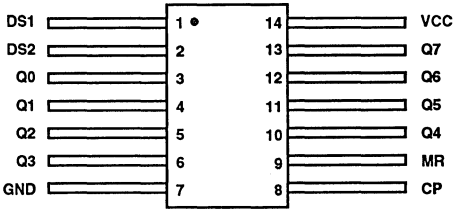
The HCTS164MS is supplied in a 14 lead Ceramic flatpack (K suffix) or a Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW



Truth Table

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{MR}$	CP	DS1	DS2	Q0	Q1-Q7
Reset (Clear)	L	X	X	X	L	L-L
Shift	H	↗	L	L	L	q0 -q6
	H	↗	L	H	L	q0 - q6
	H	↗	H	L	L	q0 - q6
	H	↗	H	H	H	q0 - q6

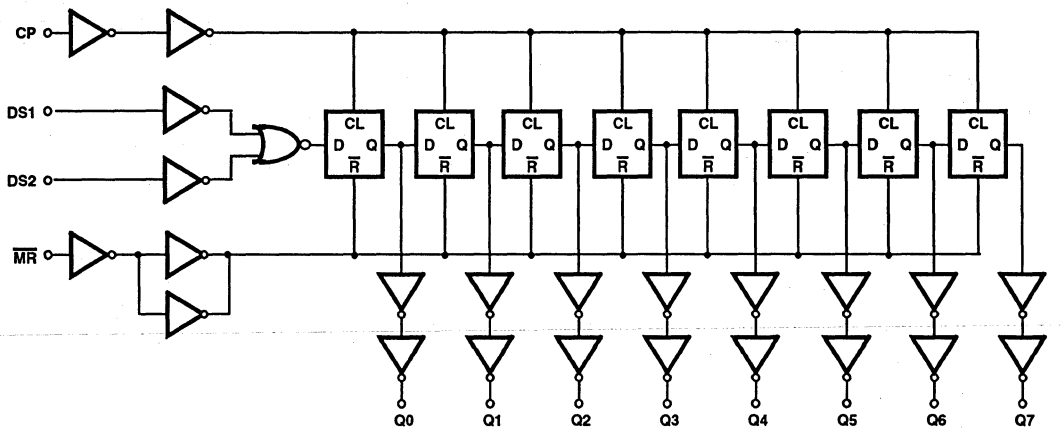
H = High Voltage Level
L = Low VoltageLevel
↗ = LOW-to-HIGH clock transition
q = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition
* DS1 and DS2 inputs must be at state one setup prior to CP (rising edge)
** Lower case letters indicate the state of the reference input (or output) one setup time prior to clock

7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3386

Functional Diagram



Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5 VCC (TR, TF) . . . . . 100ns/V Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0V to 0.8V
Input High Voltage (VIH) . . . . . VCC to VCC/2V

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0V (Note 2)	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V (Note 2)	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CP to Qn	TPLH TPHL	VCC = 4.5V	9	+25°C	2	26	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	33	ns
$\overline{MR}$ to Qn	TPHL	VCC = 4.5V	9	+25°C	2	34	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	42	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 90		pF
			1	+125°C, -55°C	Typical 140		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C, -55°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C, -55°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
CP to Qn	TPHL TPLH	VCC = 4.5V	+25°C	2	37	2	41.5	ns
$\overline{MR}$ to Qn	TPHL	VCC = 4.5V	+25°C	2	37	2	52.5	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
3 - 6, 10 - 13	1, 2, 7 - 9	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3 - 6, 10 - 13	7	-	1, 2, 8, 9, 14	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	7	3 - 6, 10 - 13	14	8	1, 2

NOTES:

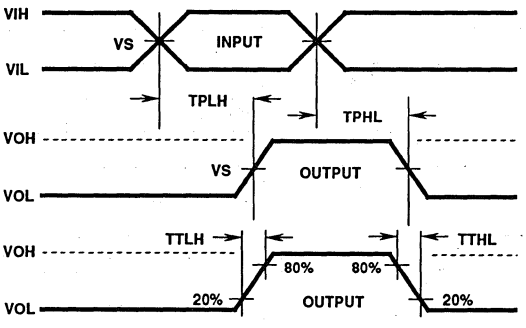
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3 - 6, 10 - 13	7	1, 2, 8, 9, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

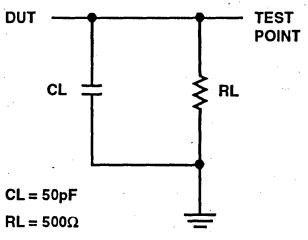
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
95 x 95 mils
2.380 x 2.410mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

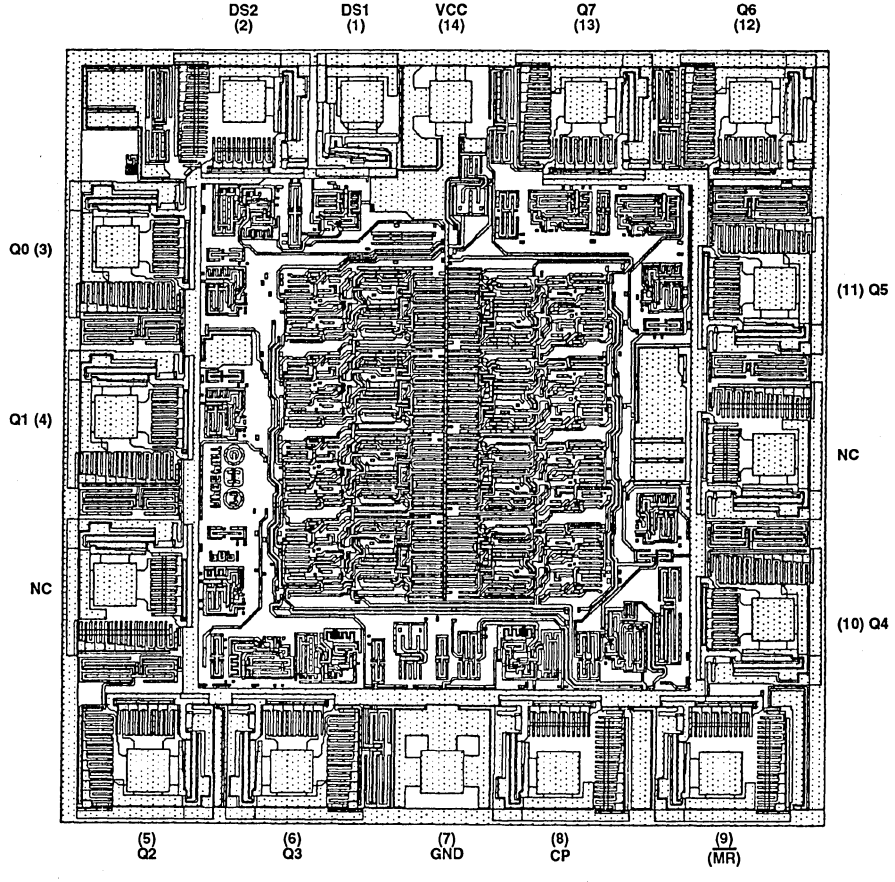
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
< 2.0 x 10^5A/cm^2

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS164MS



HARRIS SEMICONDUCTOR

HCS165MS

Radiation Hardened Inverting 8-Bit Parallel-Input/Serial Output Shift Register

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity 2 x 10^{-9} Error/Bit Day (Typ)
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Standard Outputs - 10 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.3 VCC Max
  - VIH = 0.7 VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

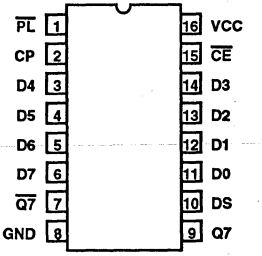
The Harris HCS165MS is a Radiation Hardened 8-Bit Parallel-In/Serial-Out Shift Register with complementary serial outputs and an asynchronous parallel load input.

The HCS165MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

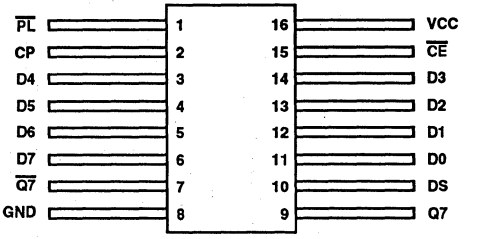
The HCS165MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR, CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR, CDFP4-F16, LEAD FINISH C
TOP VIEW



Truth Table

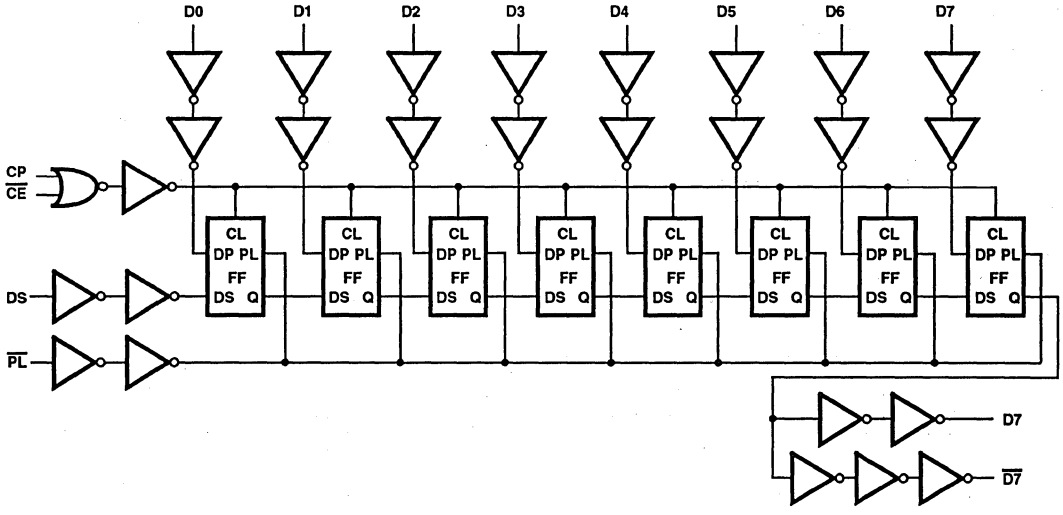
OPERATING MODES	INPUTS					Qn REGISTER		OUTPUTS	
	$\overline{PL}$	$\overline{CE}$	CP	DS	D0 - D7	Q0	Q1 - Q6	Q7	$\overline{Q7}$
Parallel Load	L	X	X	X	L	L	L - L	L	H
	L	X	X	X	H	H	H - H	H	L
Serial Shift	H	L	↘	l	X	L	Q0 - Q5	Q6	$\overline{Q6}$
	H	L	↘	h	X	H	Q0 - Q5	Q6	$\overline{Q6}$
Hold "Do Nothing"	H	H	X	X	X	Q0	Q1 - Q6	Q7	$\overline{Q7}$

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-High clock transition
Qn = Lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't Care
↘ = LOW-to-HIGH clock transition.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2481.1**

Functional Diagram



Absolute Maximum Ratings

Supply Voltage (VCC) ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC) ..... +4.5V to +5.5V
Input Rise and Fall Times at VCC = 4.5V (TR, TF) .....500ns Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 30% of VCC
Input High Voltage (VIH) ..... 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
$\overline{CP}$ or $\overline{CE}$ to Q7 or $\overline{Q7}$	TPLH TPHL	VCC = 4.5V	9	+25°C	2	35	ns
			10, 11	+125°C, -55°C	2	41	ns
PEN to Q7 or $\overline{Q7}$	TPLH TPHL	VCC = 4.5V	9	+25°C	2	40	ns
			10, 11	+125°C, -55°C	2	46	ns
D7 to Q7	TPLH TPHL	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	31	ns
D7 to $\overline{Q7}$	TPLH TPHL	VCC = 4.5V	9	+25°C	2	29	ns
			10, 11	+125°C, -55°C	2	35	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, VIH = 5.0V, VIL = 0.0V, f = 1MHz	1	+25°C	Typical 27		pF
			1	+125°C	Typical 37		pF
Input Capacitance	CIN	VCC = 5.0V, VIH = 5.0V, VIL = 0.0V, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Capacitance	COUT	VCC = 5.0V, VIH = 5.0V, VIL = 0.0V, f = 1MHz	1	+25°C	-	20	pF
			1	+125°C	-	20	pF
Pulse Width Time $\overline{CP}$, $\overline{PL}$	TW	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	16	-	ns
			1	+125°C	24	-	ns
Setup Time DS to $\overline{CP}$, $\overline{CE}$ to CP, Dn to $\overline{PL}$	TSU	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	16	-	ns
			1	+125°C	24	-	ns
Hold Time DS to CP, $\overline{CE}$	TH	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	7	-	ns
			1	+125°C	11	-	ns
Hold Time $\overline{CE}$ to CP	TH	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	0	-	ns
			1	+125°C	0	-	ns
Recovery Time $\overline{PL}$ to CP	TREC	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	20	-	ns
			1	+125°C	30	-	ns
Maximum Frequency	FMAX	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	30	-	MHz
			1	+125°C	20	-	MHz
Output Transition Time	TTHL TTLH	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	1	15	ns
			1	+125°C	1	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V or 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V or 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
CP or CEN to Q7 or Q7N	TPLH TPHL	VCC = 4.5V	+25°C	2	41	2	51.25	ns
PEN to Q7 or Q7N	TPLH TPHL	VCC = 4.5V	+25°C	2	46	2	57.50	ns
D7 to Q7	TPLH TPHL	VCC = 4.5V	+25°C	2	31	2	38.75	ns
$\overline{D7}$ to $\overline{Q7N}$	TPLH TPHL	VCC = 4.5V	+25°C	2	35	2	43.75	ns

NOTES:
1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:
1. Alternate Group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1,9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
7, 9	1 - 6, 8, 10 - 15	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
7, 9	8	-	1 - 6, 10 - 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	3 - 6, 8, 11 - 15	7, 9	1, 16	2	10

NOTES:

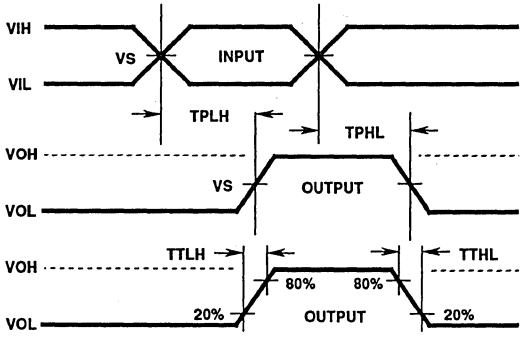
1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680kΩ ± 5% for dynamic burn-in

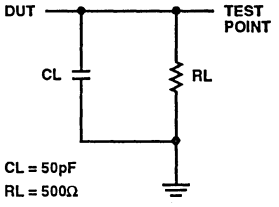
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
7, 9	8	1 - 6, 10 - 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

AC Timing Diagram and Load Circuit





AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
95 x 94 mils

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

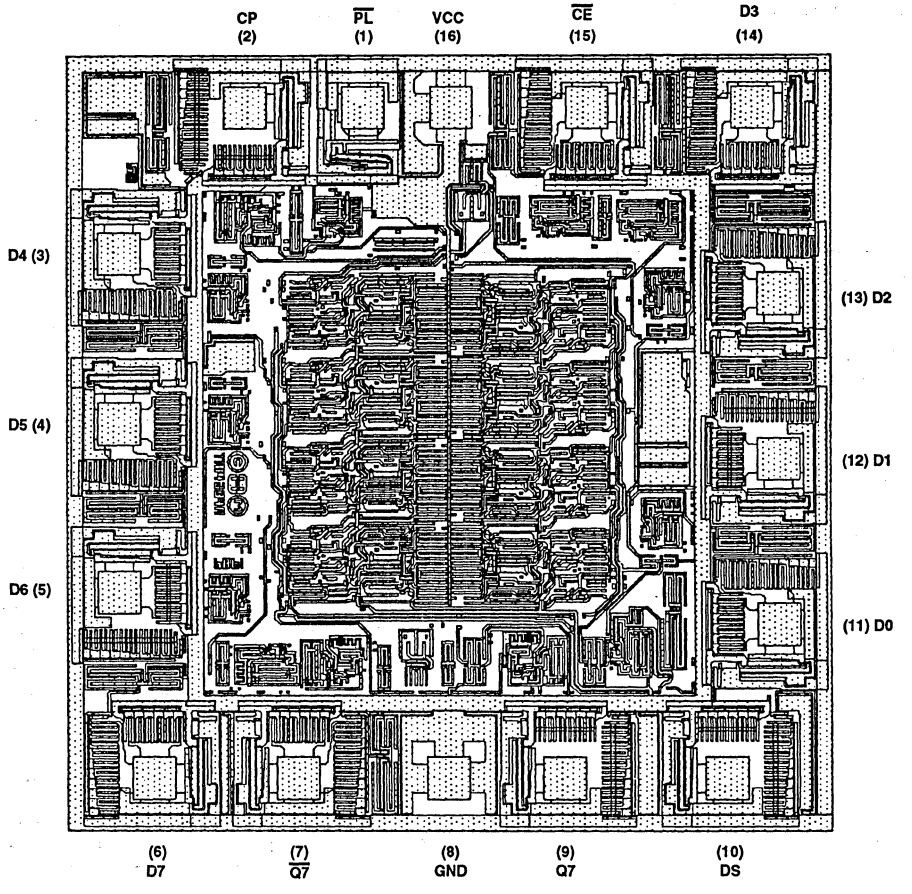
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$< 2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCS165MS



HARRIS SEMICONDUCTOR

HCS166MS

Radiation Hardened 8-Bit Parallel-Input/Serial Output Shift Register

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RADs(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity 2 x 10^{-9} Error/Bit Day (Typ)
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Standard Outputs - 10 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.3 VCC Max
  - VIH = 0.7 VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

The Harris HCS166MS is an 8-bit shift register that has fully synchronous serial or parallel data entry selected by an active LOW Parallel Enable (PE) input. When the PE is LOW one setup time before the LOW-to-HIGH clock transition, parallel data is entered into the register. When PE is HIGH, data is entered into internal bit position Q0 from Serial Data Input (DS), and the remaining bits are shifted one place to the right (Q0 → Q1 → Q2m etc.) with each positive-going clock transition. For expansion of the register in parallel to serial converters, the Q7 output is connected to the DS input of the succeeding stage.

The clock input is a gated OR structure which allows one input to be used as an active LOW Clock Enable (CE) input. The pin assignment for the CP and CE inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of CE input should only take place while the CP is HIGH for predictable operation.

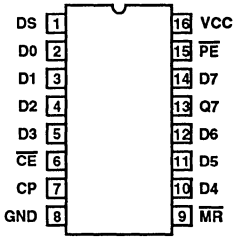
A LOW on the Master Reset (MR) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

The HCS166MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

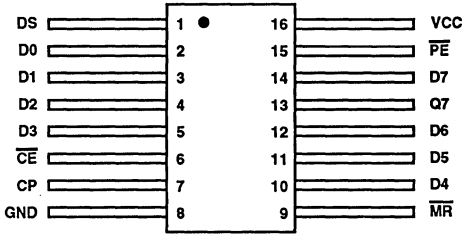
The HCS166MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR, CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F16, LEAD FINISH C
TOP VIEW



7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2482.1**

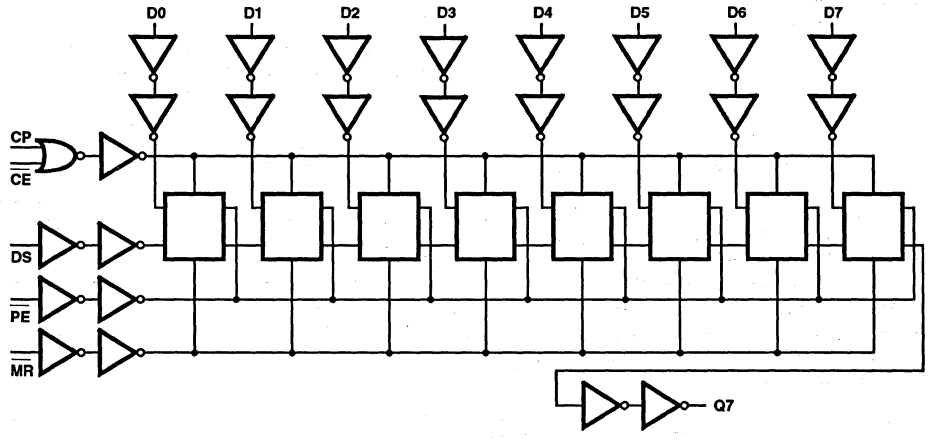
Truth Table

INPUTS						INTERNAL Q STATES		OUTPUT Q7
$\overline{\text{MASTER RESET}}$	$\overline{\text{PARALLEL ENABLE}}$	$\overline{\text{CLOCK ENABLE}}$	CLOCK	SERIAL	PARALLEL D0 - D7	Q0	Q1	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q00	Q10	Q0
H	L	L	⎍	X	a . . . h	a	b	h
H	H	L	⎍	H	X	H	Q0n	Q6n
H	H	L	⎍	L	X	L	Q0n	Q6n
H	X	H	⎍	X	X	Q00	Q10	Q70

H = High Level
L = Low Level
X = Immaterial
⎍ = Transition from low to high level

a . . . h = The level of steady state input at inputs D0 thru D7, respectively.
Q00, Q10, Q70 = The level of Q0, Q1, or Q7, respectively, before the indicated steady state input conditions were established.
Q0n, Q6n = the level of Q0 or Q6, respectively, before the most recent transition of the clock.

Functional Diagram



Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 500ns Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 30% of VCC
Input High Voltage (VIH) ..... 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC), (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CP or $\overline{CE}$ to Q7	TPHL TPLH	VCC = 4.5V	9	+25°C	2	32	ns
			10, 11	+125°C, -55°C	2	37	ns
$\overline{MR}$ to Q7	TPHL TPLH	VCC = 4.5V	9	+25°C	2	31	ns
			10, 11	+125°C, -55°C	2	36	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 43		pF
			1	+125°C	Typical 54		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C, -55°C	-	22	ns
Clock Frequency (Figure 3)	fmax	VCC = 4.5V	1	+25°C	30	-	MHz
			1	-55°C to +125°C	20	-	MHz
$\overline{MR}$ Pulse Width (Figure 4)	tw	VCC = 4.5V	1	+25°C	20	-	ns
			1	-55°C to +125°C	30	-	ns
Clock PUlse Width (Figure 3)	tw	VCC = 4.5V	1	+25°C	16	-	ns
			1	-55°C to +125°C	24	-	ns
Set-up Time Data and $\overline{CE}$ to Clock, (Figures 5, 6)	tSU	VCC = 4.5V	1	+25°C	16	-	ns
			1	-55°C to +125°C	24	-	ns
Hold Time Data to Clock (Figure 5)	tH	VCC = 4.5V	1	+25°C	1	-	ns
			1	-55°C to +125°C	1	-	ns
Removal Time $\overline{MR}$ to Clock (Figure 4(	tREM	VCC = 4.5V	1	+25°C	0	-	ns
			1	-55°C to +125°C	0	-	ns
Set-up Time $\overline{PE}$ to CP (Figure 6)	tSU	VCC = 4.5V	1	+25°C	29	-	ns
			1	-55°C to +125°C	44	-	ns
Hold Time $\overline{PE}$ to $\overline{CP}$ or CE (Figure 6)	tH	VCC = 4.5V	1	+25°C	0	-	ns
			1	-55°C to +125°C	0	-	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
CP or $\overline{CE}$ to Q7	TPHL	VCC = 4.5V	+25°C	2	37	2	46.25	ns
	TPLH	VCC = 4.5V	+25°C	2	37	2	46.25	ns
$\overline{MR}$ to Q7	TPHL	VCC = 4.5V	+25°C	2	36	2	45.0	ns
	TPLH	VCC = 4.5V	+25°C	2	36	2	45.0	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of Mil-Std-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC I BURN-IN (Note 1)					
13	1 - 12, 14	-	16	-	-
STATIC II BURN-IN (Note 1)					
13	8	-	1 - 7, 9 - 12, 14 - 16	-	-
DYNAMIC BURN-IN (Note 2)					
-	2, 4, 6, 8, 10, 12	13	3, 5, 9, 11, 14 - 16	7	1

NOTES:

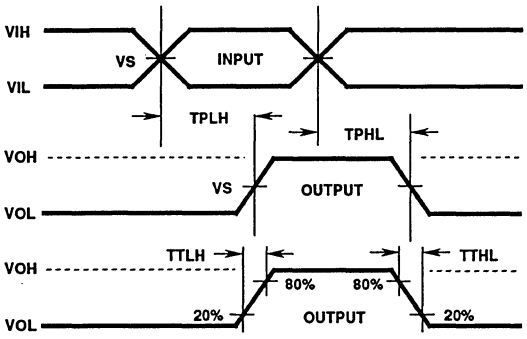
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for dynamic burn-in

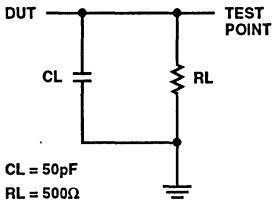
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
13	8	1 - 7, 9 - 12, 14 - 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

AC Timing Diagrams and Load Circuit





AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
94 x 94 mils

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

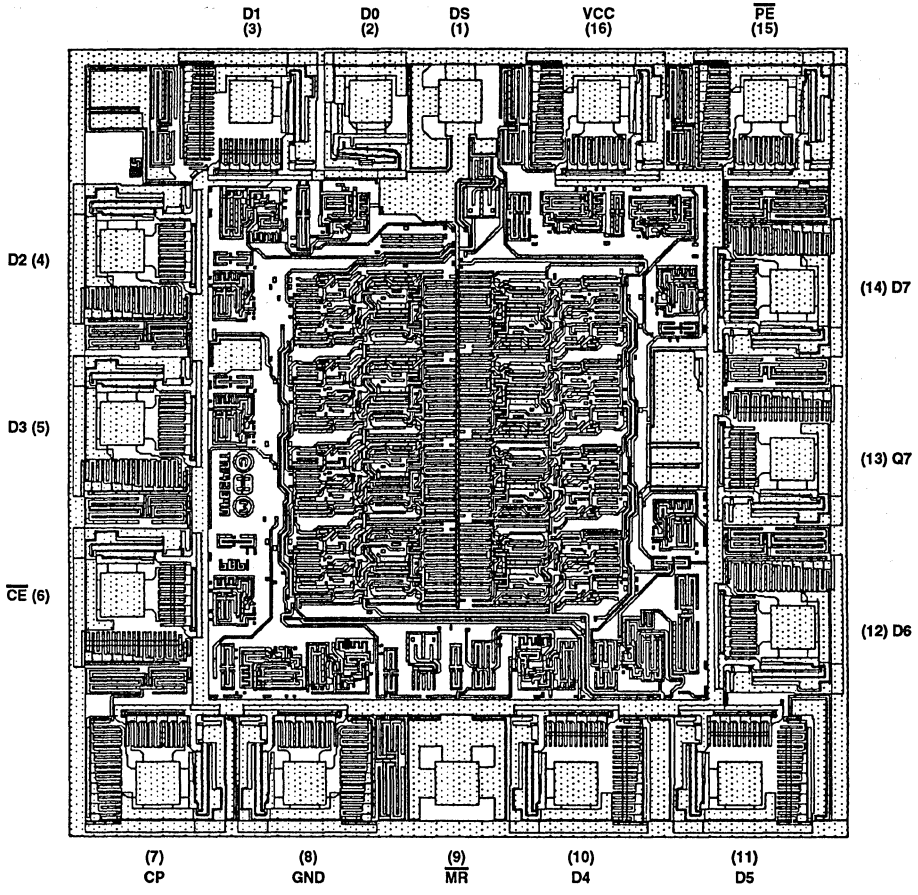
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$< 2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCS166MS



HARRIS SEMICONDUCTOR

HCTS190MS

Radiation Hardened Synchronous 4-Bit Up/Down Counter

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity 2 x 10^{-9} Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Standard Outputs - 10 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA @ VOL, VOH

Description

The Harris HCTS190MS is an asynchronously presettable BCD Decade synchronous counter. Presetting the counter to the number on the preset data inputs (P0 - P3) is accomplished by a low on the parallel load input ($\overline{PL}$). Counting occurs when ($\overline{PL}$) is high, Count Enable ($\overline{CE}$) is low and the Up/Down ($\overline{U}$/D) input is either low for up-counting or high for down-counting. The counter is incremented or decremented synchronously with the low-to-high transition of the clock.

When an overflow or underflow of the counter occurs, the Terminal Count output (TC), which is low during counting, goes high and remains high for one clock cycle. This output can be used for look-ahead carry in high speed cascading. The TC output also initiates the Ripple Clock output ($\overline{RC}$) which, normally high, goes low and remains low for the low-level portion of the clock pulse. These counter can be cascaded using the Ripple Carry output.

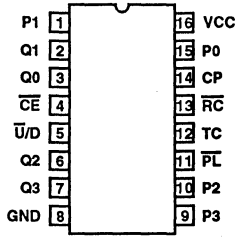
If the decade counter is preset to an illegal state or assumes an illegal state when power is applied, it will return to the normal sequence in one or two counts

The HCTS190MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

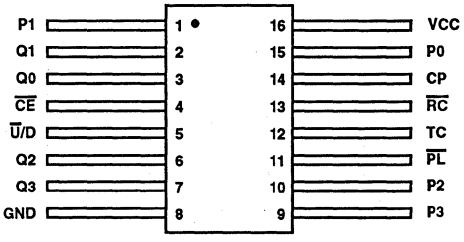
The HCTS190MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F16, LEAD FINISH C
TOP VIEW



7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

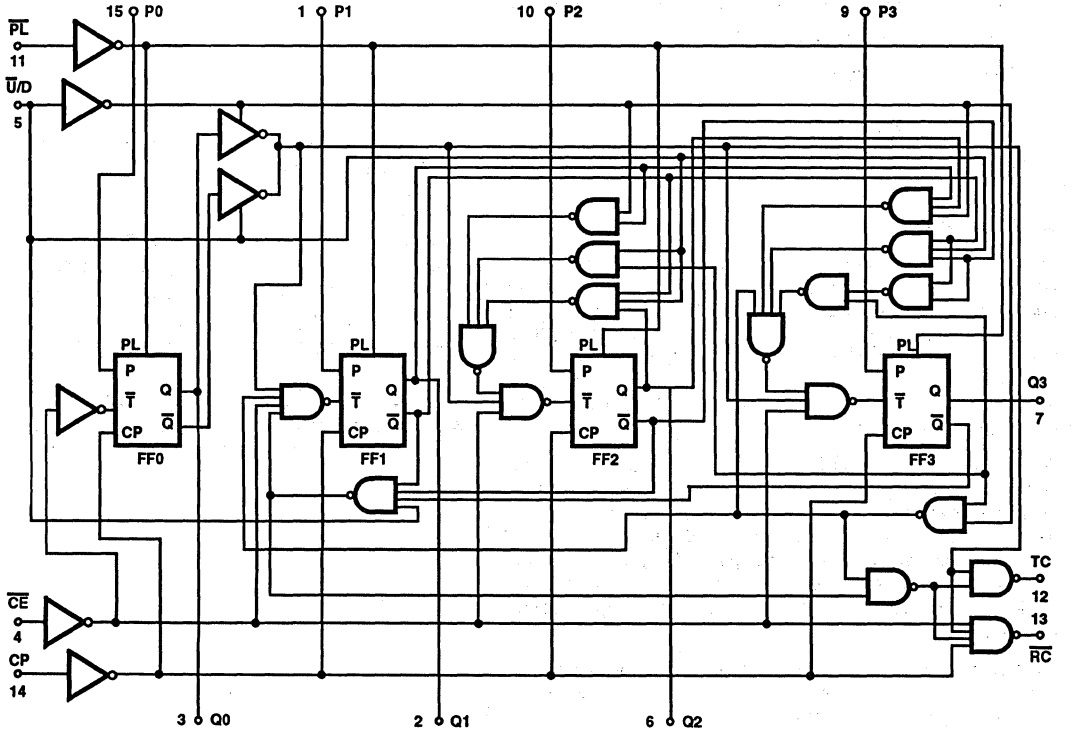
File Number **2474.1**

Truth Table

FUNCTION	$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP
Count Up	H	L	L	⎍
Count Down	H	L	H	⎍
Asynchronous Preset	L	X	X	X
No Change	H	H	X	X

H = High Level
L = Low Level
X = Immaterial
⎍ = Transition from low to high
NOTE: $\overline{U}$/D or $\overline{CE}$ should be changed only when clock is high.

Functional Diagram



Absolute Maximum Ratings

Supply Voltage (VCC) ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage(VCC) ..... +4.5V to +5.5V
Input Rise and Fall Times @ 4.5 VCC (TR, TF) ..... 500ns Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH =2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOL = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOL = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	0.5	µA
			2, 3	+125°C, -55°C	-5.0	5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
$\overline{PL}$ to Qn	TPLH	VCC = 4.5V	9	+25°C	2	32	ns
			10, 11	+125°C, -55°C	2	37	ns
	TPHL	VCC = 4.5V	9	+25°C	2	38	ns
			10, 11	+125°C, -55°C	2	44	ns
Pn to Qn	TPLH	VCC = 4.5V	9	+25°C	2	24	ns
			10, 11	+125°C, -55°C	2	28	ns
	TPHL	VCC = 4.5V	9	+25°C	2	36	ns
			10, 11	+125°C, -55°C	2	41	ns
CP to Qn	TPLH	VCC = 4.5V	9	+25°C	2	24	ns
			10, 11	+125°C, -55°C	2	29	ns
	TPHL	VCC = 4.5V	9	+25°C	2	23	ns
			10, 11	+125°C, -55°C	2	27	ns
CP to $\overline{RC}$	TPLH	VCC = 4.5V	9	+25°C	2	17	ns
			10, 11	+125°C, -55°C	2	19	ns
	TPHL	VCC = 4.5V	9	+25°C	2	26	ns
			10, 11	+125°C, -55°C	2	29	ns
CP to TC	TPLH	VCC = 4.5V	9	+25°C	2	33	ns
			10, 11	+125°C, -55°C	2	39	ns
	TPHL	VCC = 4.5V	9	+25°C	2	33	ns
			10, 11	+125°C, -55°C	2	39	ns
$\overline{U}$/D to $\overline{RC}$	TPLH	VCC = 4.5V	9	+25°C	2	32	ns
			10, 11	+125°C, -55°C	2	36	ns
	TPHL	VCC = 4.5V	9	+25°C	2	34	ns
			10, 11	+125°C, -55°C	2	38	ns
$\overline{U}$/D to TC	TPLH	VCC = 4.5V	9	+25°C	2	29	ns
			10, 11	+125°C, -55°C	2	33	ns
	TPHL	VCC = 4.5V	9	+25°C	2	35	ns
			10, 11	+125°C, -55°C	2	38	ns
$\overline{CE}$ to $\overline{RC}$	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	21	ns
	TPHL	VCC = 4.5V	9	+25°C	2	29	ns
			10, 11	+125°C, -55°C	2	31	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	+25°C	Typical 40		pF
			+125°C	Typical 85		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	+25°C	-	10	pF
			+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	+25°C	-	15	ns
			+125°C, -55°C	-	22	ns
Maximum Operating Frequency (CPU, CPD)	FMAX	VCC = 4.5V	+25°C		30	MHz
			+125°C, -55°C		20	MHz
Setup Time Pn to $\overline{PL}$	TSU	VCC = 4.5V	+25°C	12	-	ns
			+125°C, -55°C	18	-	ns
Setup Time $\overline{CE}$ to CP	TSU	VCC = 4.5V	+25°C	12	-	ns
			+125°C, -55°C	18	-	ns
Setup Time $\overline{U}$/D to CP	TSU	VCC = 4.5V	+25°C	18	-	ns
			+125°C, -55°C	27	-	ns
Hold Time Pn to $\overline{PL}$	TH	VCC = 4.5V	+25°C	2	-	ns
			+125°C, -55°C	2	-	ns
Hold Time $\overline{CE}$ to CP	TH	VCC = 4.5V	+25°C	2	-	ns
			+125°C, -55°C	2	-	ns
Hold Time $\overline{U}$/D to CP	TH	VCC = 4.5V	+25°C	0	-	ns
			+125°C, -55°C	0	-	ns
Recovery Time	TREC	VCC = 4.5V	+25°C	12	-	ns
			+125°C, -55°C	18	-	ns
CP Pulse Width	TW	VCC = 4.5V	+25°C	16	-	ns
			+125°C, -55°C	24	-	ns
PLN Pulse Width	TW	VCC = 4.5V	+25°C	20		ns
			+125°C, -55°C	30		ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
$\overline{PL}$ to Qn	TPLH	VCC = 4.5V	+25°C	2	27	2	34	ns
	TPHL	VCC = 4.5V	+25°C	2	37	2	47	ns
Pn to Qn	TPLH	VCC = 4.5V	+25°C	2	24	2	30	ns
	TPHL	VCC = 4.5V	+25°C	2	35	2	44	ns
CP to Qn	TPLH	VCC = 4.5V	+25°C	2	23	2	29	ns
	TPHL	VCC = 4.5V	+25°C	2	26	2	33	ns
Cp to $\overline{RC}$	TPLH	VCC = 4.5V	+25°C	2	16	2	20	ns
	TPHL	VCC = 4.5V	+25°C	2	24	2	30	ns
CP to TC	TPLH	VCC = 4.5V	+25°C	2	33	2	42	ns
	TPHL	VCC = 4.5V	+25°C	2	35	2	44	ns
$\overline{U}$/D to $\overline{RC}$	TPLH	VCC = 4.5V	+25°C	2	30	2	38	ns
	TPHL	VCC = 4.5V	+25°C	2	32	2	40	ns
$\overline{U}$/D to TC	TPLH	VCC = 4.5V	+25°C	2	27	2	34	ns
	TPHL	VCC = 4.5V	+25°C	2	31	2	39	ns
$\overline{CE}$ to $\overline{RC}$	TPLH	VCC = 4.5V	+25°C	2	17	2	22	ns
	TPHL	VCC = 4.5V	+25°C	2	26	2	33	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1					
2, 3, 6, 7, 12, 13	1, 4, 5, 8 - 11, 14, 15	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
2, 3, 6, 7, 12, 13	8	-	1, 4, 5, 9 - 11, 14 - 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	1, 4, 5, 8 - 10, 15	2, 3, 6, 7, 12, 13	11, 16	14	-

NOTES:

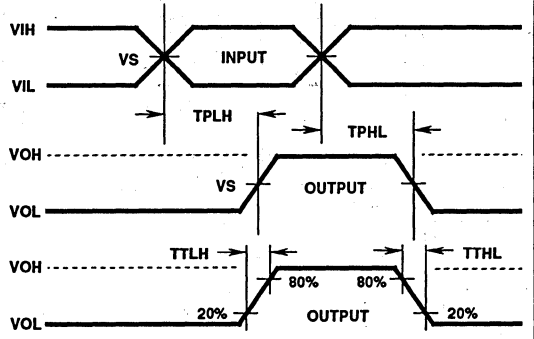
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
2, 3, 6, 7, 12, 13	8	1, 4, 5, 9 - 11, 14 - 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

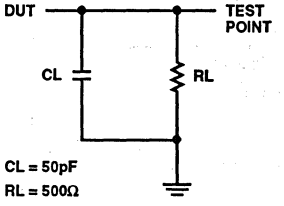
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
104 x 86 mils

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

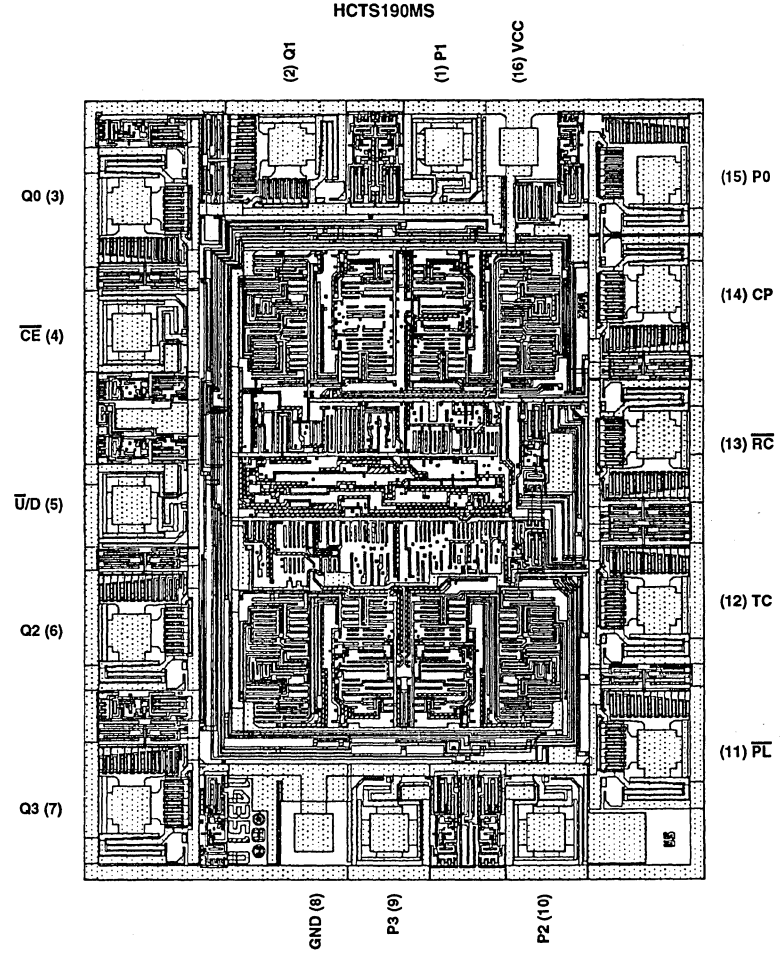
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$< 2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS190MS



HARRIS SEMICONDUCTOR

HCTS191MS

Radiation Hardened Synchronous 4-Bit Up/Down Counter

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity 2 x 10^{-9} Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Standard Outputs - 10 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA @ VOL, VOH

Description

The Harris HCTS191MS is a Radiation Hardened asynchronously presettable 4 bit binary up/down synchronous counter. Presetting the counter to the number on the preset data inputs (P0 - P3) is accomplished by a low asynchronous parallel load input ($\overline{PL}$). Counting occurs when $\overline{PL}$ is high, Count Enable ($\overline{CE}$) is low, and the Up/Down ($\overline{U}$/D) input is either low for up-counting or high for down-counting. The counter is incremented or decremented synchronously with the low-to-high transition of the clock.

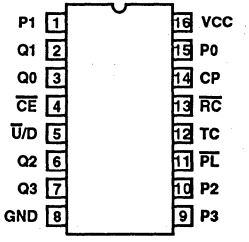
When an overflow or underflow of the counter occurs, the Terminal Count output (TC), which is low during counting, goes high and remains high for one clock cycle. This output can be used for look-ahead carry in high speed cascading. The TC output also initiates the Ripple Clock output ($\overline{RC}$) which, normally high, goes low and remains low for the low-level portion of the clock pulse. These counter can be cascaded using the Ripple Carry output.

The HCTS191MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

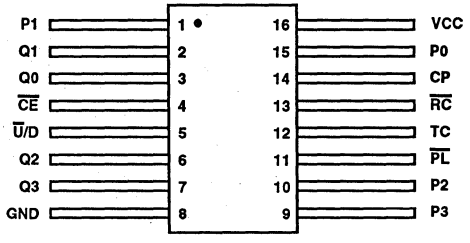
The HCTS191MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR, CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR, CDFP4-F16, LEAD FINISH C
TOP VIEW



Truth Table

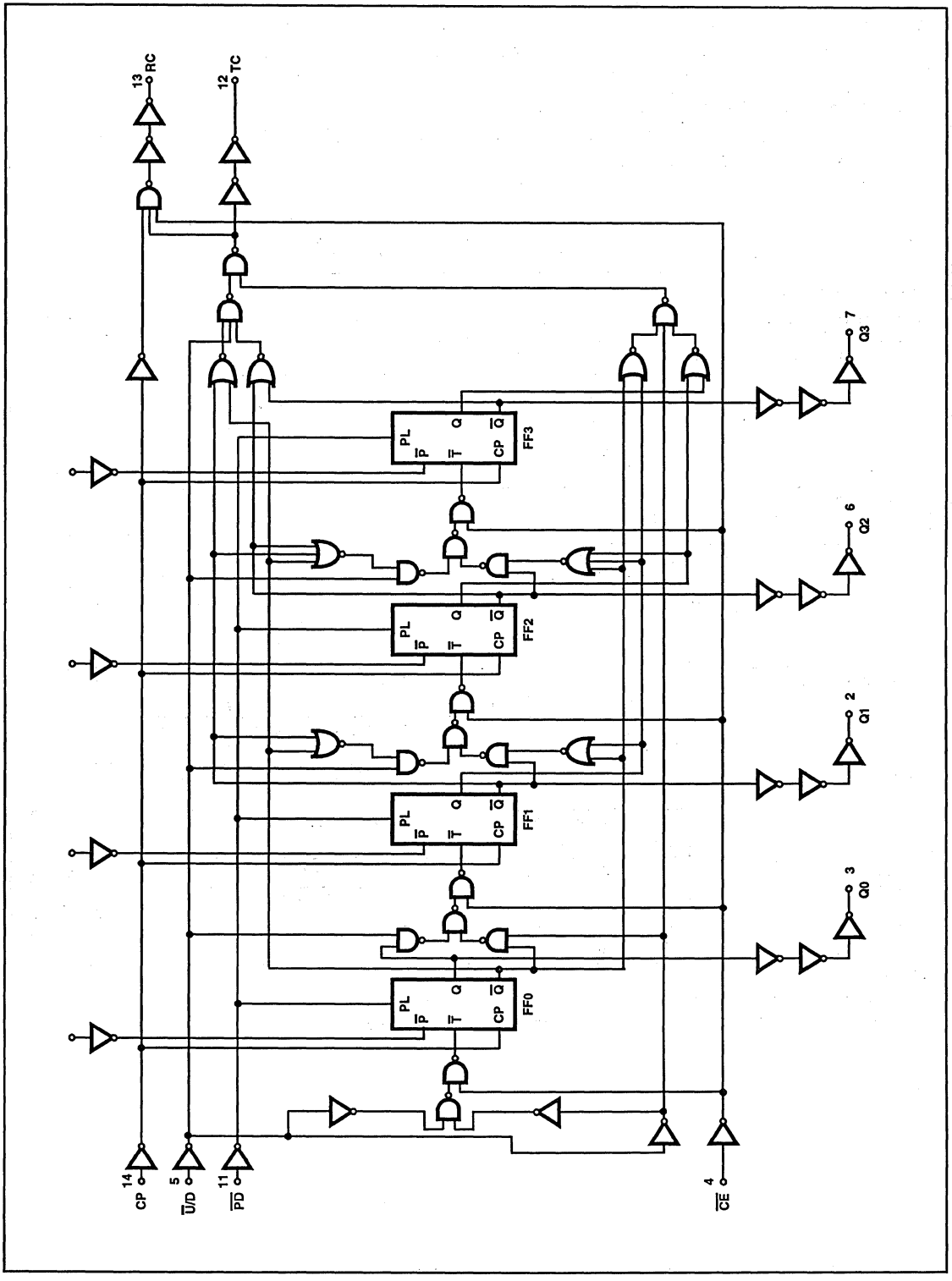
FUNCTION	$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP
Count Up	H	L	L	↗
Count Down	H	L	H	↗
Asynchronous Preset	L	X	X	X
No Change	H	H	X	X

H = High Level
L = Low Level
X = Immaterial
↗ = Transition from low to high

NOTE: $\overline{U}$/D or $\overline{CE}$ should be changed only when CLOCK (CP) is high.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2250.1**


13 RC
12 TC
7 Q3
6 Q2
2 Q1
3 Q0
14 CP
5 U/D
11 PD
4 CE
FF3
FF2
FF1
FF0
PL
P
T
CP
Q
Q

Absolute Maximum Ratings

Supply Voltage (VCC) ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC) ..... +4.5V to +5.5V
Input Rise and Fall Times at VCC = 4.5V (TR, TF) ..... 500ns Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
$\overline{PL}$ to Qn	TPLH	VCC = 4.5V	9	+25°C	2	34	ns
			10, 11	+125°C, -55°C	2	37	ns
	TPHL	VCC = 4.5V	9	+25°C	2	44	ns
			10, 11	+125°C, -55°C	2	49	ns
Pn to Qn	TPLH	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	31	ns
	TPHL	VCC = 4.5V	9	+25°C	2	39	ns
			10, 11	+125°C, -55°C	2	45	ns
CP to Qn	TPLH	VCC = 4.5V	9	+25°C	2	26	ns
			10, 11	+125°C, -55°C	2	30	ns
	TPHL	VCC = 4.5V	9	+25°C	2	29	ns
			10, 11	+125°C, -55°C	2	33	ns
CP to $\overline{RC}$	TPLH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	23	ns
	TPHL	VCC = 4.5V	9	+25°C	2	32	ns
			10, 11	+125°C, -55°C	2	34	ns
CP to TC	TPLH	VCC = 4.5V	9	+25°C	2	37	ns
			10, 11	+125°C, -55°C	2	42	ns
	TPHL	VCC = 4.5V	9	+25°C	2	40	ns
			10, 11	+125°C, -55°C	2	46	ns
$\overline{U}$/D to $\overline{RC}$	TPLH	VCC = 4.5V	9	+25°C	2	42	ns
			10, 11	+125°C, -55°C	2	45	ns
	TPHL	VCC = 4.5V	9	+25°C	2	38	ns
			10, 11	+125°C, -55°C	2	43	ns
$\overline{U}$/D to TC	TPLH	VCC = 4.5V	9	+25°C	2	34	ns
			10, 11	+125°C, -55°C	2	38	ns
	TPHL	VCC = 4.5V	9	+25°C	2	42	ns
			10, 11	+125°C, -55°C	2	45	ns
$\overline{CE}$ to $\overline{RC}$	TPLH	VCC = 4.5V	9	+25°C	2	22	ns
			10, 11	+125°C, -55°C	2	25	ns
	TPHL	VCC = 4.5V	9	+25°C	2	35	ns
			10, 11	+125°C, -55°C	2	38	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 36		pF
			1	+125°C	Typical 56		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C, -55°C	-	22	ns
Maximum Operating Frequency (CPU, CPD)	FMAX	VCC = 4.5V	1	+25°C	-	30	MHz
			1	+125°C, -55°C	-	20	MHz
Setup Time Pn to $\overline{PL}$	TSU	VCC = 4.5V	1	+25°C	12	-	ns
			1	+125°C, -55°C	18	-	ns
Setup Time $\overline{CE}$ to CP	TSU	VCC = 4.5V	1	+25°C	12	-	ns
			1	+125°C, -55°C	18	-	ns
Setup Time $\overline{U}$/D to CP	TSU	VCC = 4.5V	1	+25°C	18	-	ns
			1	+125°C, -55°C	27	-	ns
Hold Time Pn to $\overline{PL}$	TH	VCC = 4.5V	1	+25°C	2	-	ns
			1	+125°C, -55°C	2	-	ns
Hold Time $\overline{CE}$ to CP	TH	VCC = 4.5V	1	+25°C	2	-	ns
			1	+125°C, -55°C	2	-	ns
Hold Time $\overline{U}$/D to CP	TH	VCC = 4.5V	1	+25°C	0	-	ns
			1	+125°C, -55°C	0	-	ns
Recovery Time	TREC	VCC = 4.5V	1	+25°C	12	-	ns
			1	+125°C, -55°C	18	-	ns
CP Pulse Width	TW	VCC = 4.5V	1	+25°C	16	-	ns
			1	+125°C, -55°C	24	-	ns
$\overline{PL}$ Pulse Width	TW	VCC = 4.5V	1	+25°C	20	-	ns
			1	+125°C, -55°C	30	-	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
PL to Qn	TPLH	VCC = 4.5V	+25°C	2	37	2	47	ns
	TPHL	VCC = 4.5V	+25°C	2	49	2	62	ns
Pn to Qn	TPLH	VCC = 4.5V	+25°C	2	31	2	39	ns
	TPHL	VCC = 4.5V	+25°C	2	45	2	57	ns
CP to Qn	TPLH	VCC = 4.5V	+25°C	2	30	2	38	ns
	TPHL	VCC = 4.5V	+25°C	2	33	2	42	ns
Cp to $\overline{RC}$	TPLH	VCC = 4.5V	+25°C	2	23	2	29	ns
	TPHL	VCC = 4.5V	+25°C	2	34	2	43	ns
CP to TC	TPLH	VCC = 4.5V	+25°C	2	42	2	53	ns
	TPHL	VCC = 4.5V	+25°C	2	46	2	58	ns
$\overline{U}$/D to $\overline{RC}$	TPLH	VCC = 4.5V	+25°C	2	45	2	57	ns
	TPHL	VCC = 4.5V	+25°C	2	43	2	54	ns
$\overline{U}$/D to TC	TPLH	VCC = 4.5V	+25°C	2	38	2	48	ns
	TPHL	VCC = 4.5V	+25°C	2	45	2	57	ns
$\overline{CE}$ to $\overline{RC}$	TPLH	VCC = 4.5V	+25°C	2	25	2	32	ns
	TPHL	VCC = 4.5V	+25°C	2	38	2	48	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1,9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
2, 3, 6, 7, 12, 13	1, 4, 5, 8 - 11, 14, 15	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
2, 3, 6, 7, 12, 13	8	-	1, 4, 5, 9 - 11, 14 - 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	1, 4, 5, 8 - 10, 15	2, 3, 6, 7, 12, 13	11, 16	14	-

NOTES:

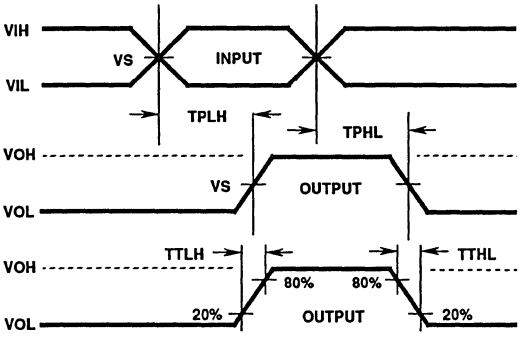
1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1kΩ ± 5% for dynamic burn-in

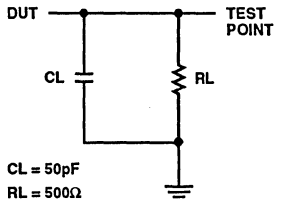
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
2, 3, 6, 7, 12, 13	8	1, 4, 5, 9 - 11, 14 - 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

AC Timing Diagram and Load Circuit





AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
104 x 86 mils

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

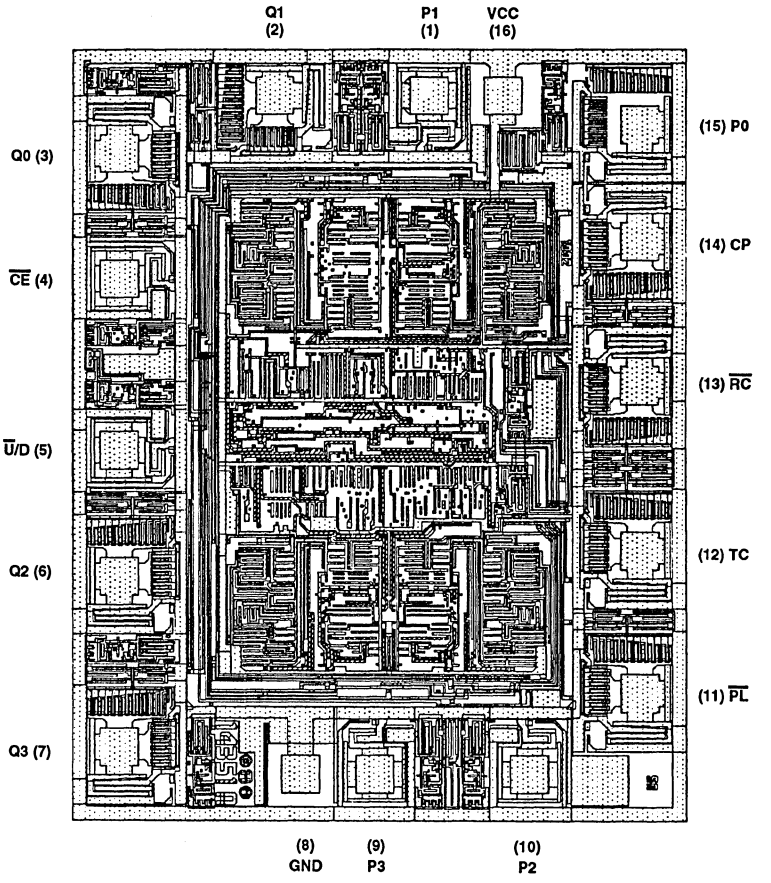
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
< $2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCTS191MS



HARRIS SEMICONDUCTOR

HCS193MS

Radiation Hardened Synchronous 4-Bit Up/Down Counter

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity 2 x 10^{-9} Error/Bit Day (Typ)
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.3 VCC Max
  - VIH = 0.7 VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

The Harris HCS193MS is a Radiation Hardened 4-bit binary UP/DOWN synchronous counter.

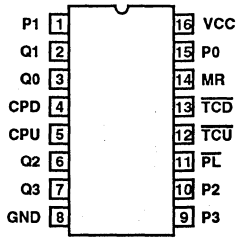
Presetting the counter to the number on the preset data inputs (P0 - P3) is accomplished by a low on the asynchronous parallel load input ($\overline{PL}$). The counter is incremented on the low to high transition of the clock-up input (high on the clock-down), decremented on the low to high transition of the clock-down input (high on the clock-up). A high level on the MR input overrides any other input to clear the counter to zero. The Terminal Count Up goes low half a clock period before the zero count is reached and returns high at the maximum count.

The HCS193MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

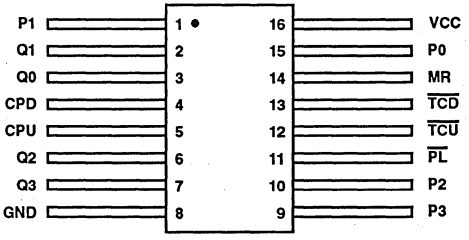
The HCS193MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F16, LEAD FINISH
TOP VIEW



Truth Table

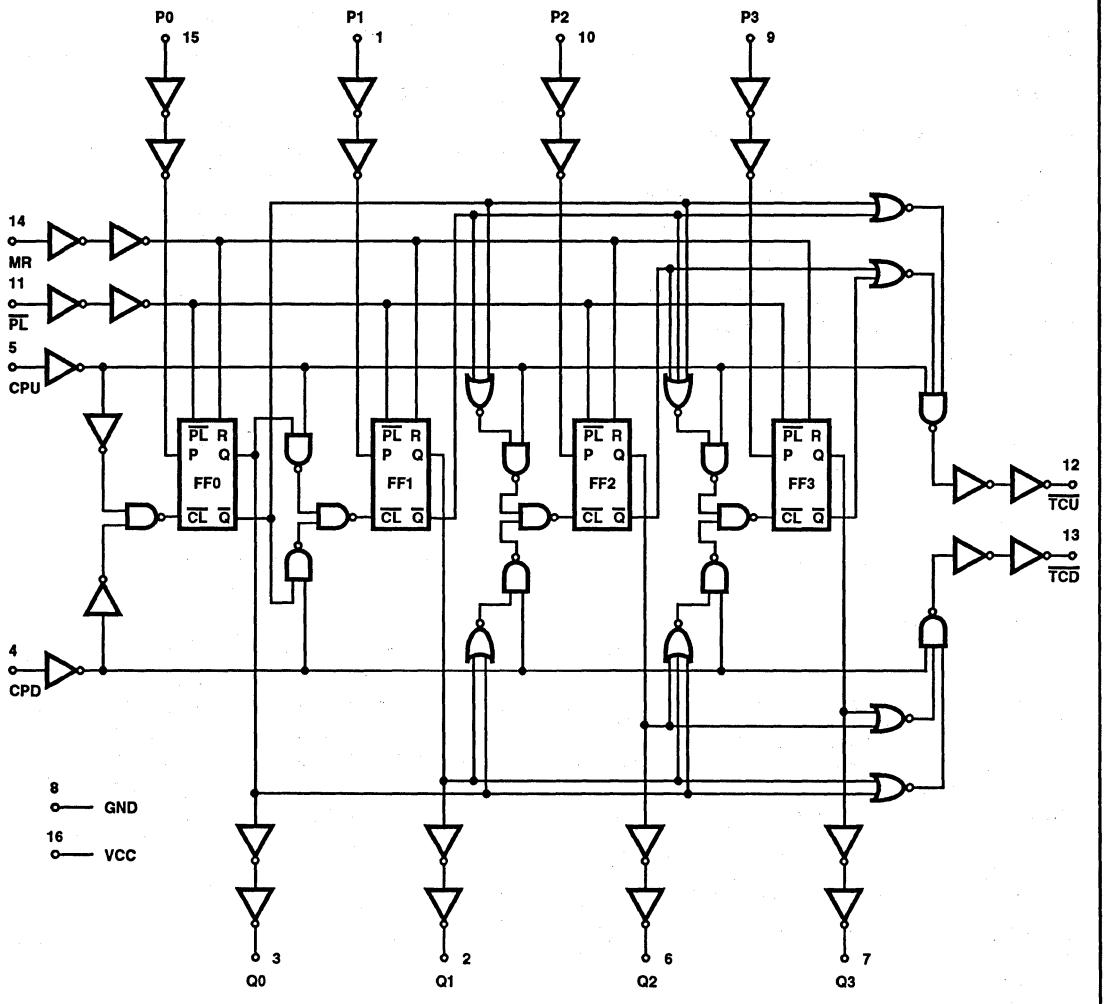
FUNCTION	CLOCK UP	CLOCK DOWN	RESET	PARALLEL LOAD
Count Up	⎍	H	L	H
Count Down	H	⎍	L	H
Reset	X	X	H	X
Load Preset Input	X	X	L	L

H = High Level, L = Low Level, X = Immaterial, ⎍ = Transition from low to high

7 LOGIC

File Number 3065

Functional Diagram



Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5 VCC (TR, TF) ..... 100ns Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 30% of VCC
Input High Voltage (VIH) ..... 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), (Note 2) VIL = 0.30(VCC)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CPU to Qn	TPLH	VCC = 4.5V	9	+25°C	2	31	ns
			10, 11	+125°C, -55°C	2	38	ns
	TPHL	VCC = 4.5V	9	+25°C	2	31	ns
			10, 11	+125°C, -55°C	2	36	ns
CPU to $\overline{TCU}$	TPLH TPHL	VCC = 4.5V	9	+25°C	2	23	ns
			10, 11	+125°C, -55°C	2	27	ns
CPD to $\overline{TCD}$	TPLH TPHL	VCC = 4.5V	9	+25°C	2	23	ns
			10, 11	+125°C, -55°C	2	27	ns
CPD to Qn	TPLH	VCC = 4.5V	9	+25°C	2	32	ns
			10, 11	+125°C, -55°C	2	39	ns
	TPHL	VCC = 4.5V	9	+25°C	2	31	ns
			10, 11	+125°C, -55°C	2	37	ns
$\overline{PL}$ to Qn	TPLH	VCC = 4.5V	9	+25°C	2	26	ns
			10, 11	+125°C, -55°C	2	31	ns
	TPHL	VCC = 4.5V	9	+25°C	2	34	ns
			10, 11	+125°C, -55°C	2	40	ns
MR to Qn	TPHL TPLH	VCC = 4.5V	9	+25°C	2	33	ns
			10, 11	+125°C, -55°C	2	38	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 35		pF
			1	+125°C	Typical 50		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns
Maximum Operating Frequency (CPU, CPD)	FMAX	VCC = 4.5V	1	+25°C		25	MHz
			1	+125°C		17	MHz
Setup Time Pn to $\overline{PL}$	TSU	VCC = 4.5V	1	+25°C	16	-	ns
			1	+125°C	24	-	ns
Hold Time Pn to $\overline{PL}$	TH	VCC = 4.5V	1	+25°C	0	-	ns
			1	+125°C	0	-	ns
Hold Time CPD to CPU or CPU to CPD	TH	VCC = 4.5V	1	+25°C	16	-	ns
			1	+125°C	24	-	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Pulse Width CPU to CPD	TW	VCC = 4.5V	1	+25°C	20	-	ns
			1	+125°C	30	-	ns
Pulse Width $\overline{PL}$	TW	VCC = 4.5V	1	+25°C	16	-	ns
			1	+125°C	24	-	ns
Pulse Width MR	TW	VCC = 4.5V	1	+25°C	20	-	ns
			1	+125°C	30	-	ns
Recovery Time $\overline{PL}$ to CPU, CPD	TREC	VCC = 4.5V	1	+25°C	16	-	ns
			1	+125°C	24	-	ns
Recovery Time MR to CPU, CPD	TREC	VCC = 4.5V	1	+25°C	5	-	ns
			1	+125°C	5	-	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
CPU to Qn	TPLH	VCC = 4.5V	+25°C	2	38	2	47.5	ns
CPU to Qn	TPHL	VCC = 4.5V	+25°C	2	36	2	45	ns
CPU to $\overline{TCU}$	TPHL TPLH	VCC = 4.5V	+25°C	2	27	2	34	ns
CPD to $\overline{TCD}$	TPHL TPLH	VCC = 4.5V	+25°C	2	25	2	31	ns

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
CPD to QN	TPLH	VCC = 4.5V	+25°C	2	36	2	45	ns
	TPHL		+25°C	2	37	2	46	ns
$\overline{PL}$ to Qn	TPLH	VCC = 4.5V	+25°C	2	31	2	39	ns
	TPHL		+25°C	2	40	2	50.5	ns
MR to Qn	TPHL	VCC = 4.5V	+25°C	2	38	2	47.5	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
2, 3, 6, 7, 12, 13	1, 4, 5, 8 - 11, 14, 15	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
2, 3, 6, 7, 12, 13	8	-	1, 4, 5, 9 - 11, 14 - 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	1, 4, 5, 8 - 10, 15	2, 3, 6, 7, 12, 13	11, 16	14	-

NOTES:

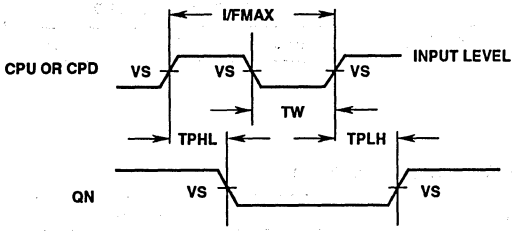
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

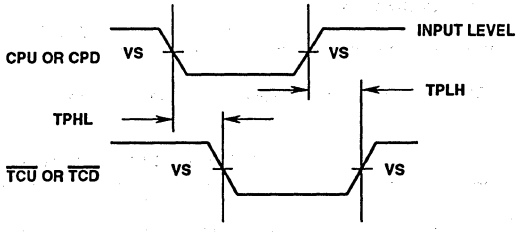
OPEN	GROUND	VCC = 5V ± 0.5V
2, 3, 6, 7, 12, 13	8	1, 4, 5, 9 - 11, 14 - 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

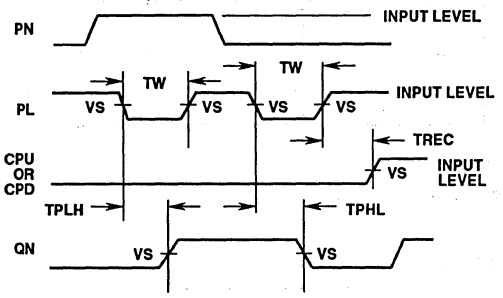
AC Timing Diagrams



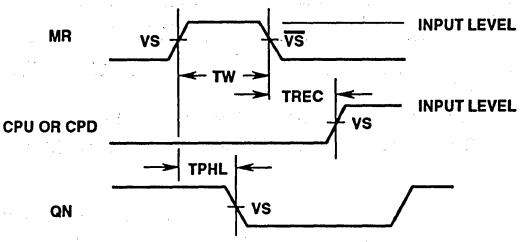
CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



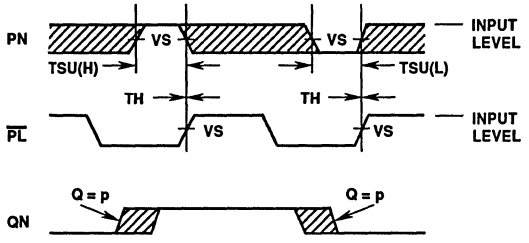
CLOCK TO TERMINAL COUNT DELAYS



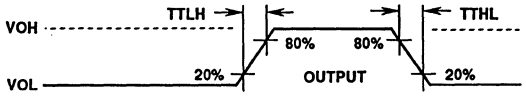
PARALLEL LOAD PULSE WIDTH, PARALLEL LOAD TO OUTPUT DELAYS, AND PARALLEL LOAD TO CLOCK RECOVERY TIME



MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



SETUP AND HOLD TIMES DATA TO PARALLEL LOAD (PL)



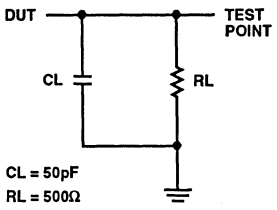
OUTPUT TRANSITION TIME

AC Timing Diagrams

AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
104 x 86 mils
2642µm x 2185µm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

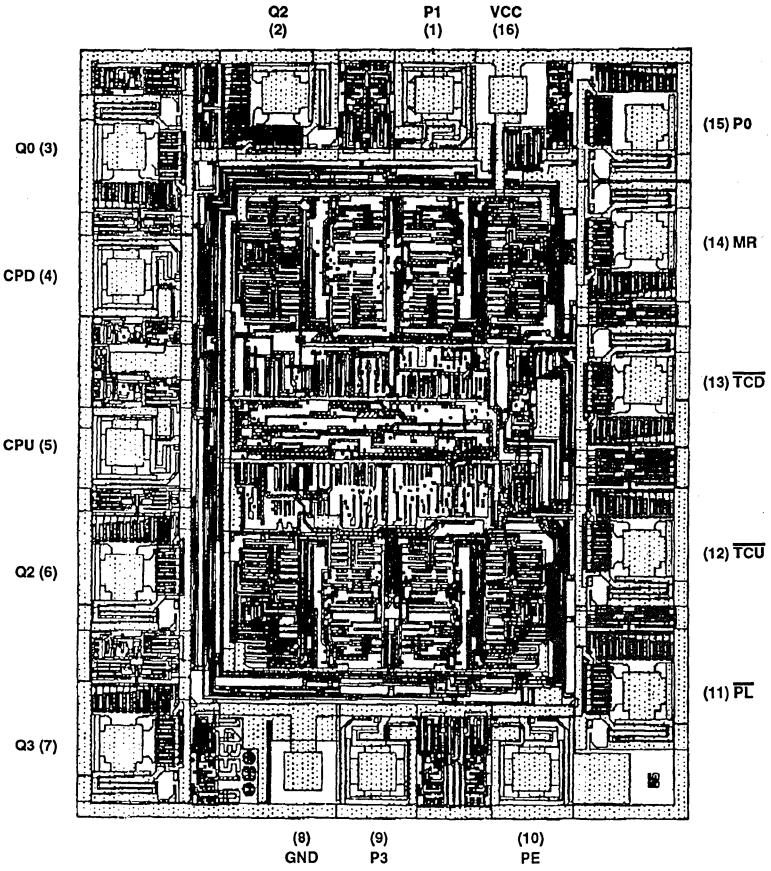
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$< 2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCS193MS



HARRIS SEMICONDUCTOR

HCTS193MS

Radiation Hardened Synchronous 4-Bit Up/Down Counter

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity 2 x 10^{-9} Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Standard Outputs - 10 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

The Harris HCTS193MS is a Radiation Hardened 4-bit binary UP/DOWN synchronous counter.

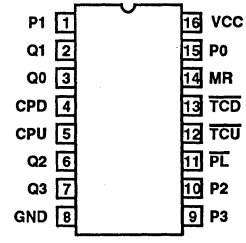
Presetting the counter to the number on the preset data inputs (P0 - P3) is accomplished by a low on the asynchronous parallel load input ($\overline{PL}$). The counter is incremented on the low to high transition of the clock-up input (high on the clock-down), decremented on the low to high transition of the clock-down input (high on the clock-up). A high level on the MR input overrides any other input to clear the counter to zero. The Terminal Count Up goes low half a clock period before the zero count is reached and returns high at the maximum count. The Terminal Count Down mode goes low half a clock period before the maximum count and returns high at the maximum count.

The HCTS193MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

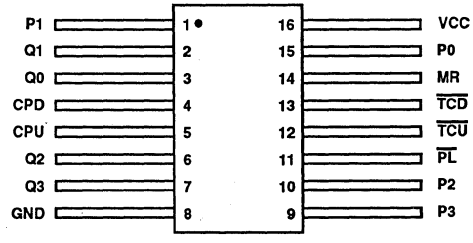
The HCTS193MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F16, LEAD FINISH C
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

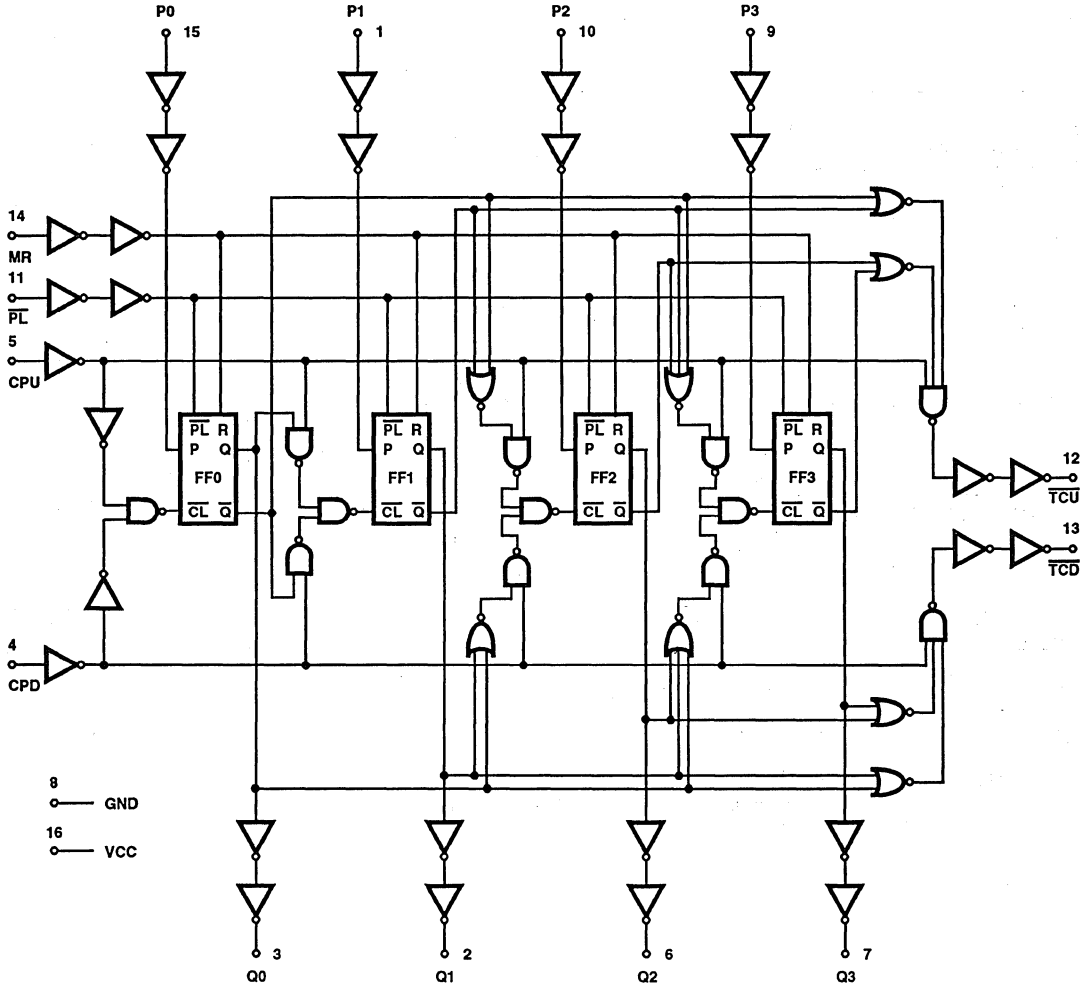
File Number 3066

Truth Table

FUNCTION	CLOCK UP	CLOCK DOWN	RESET	PARALLEL LOAD
Count Up	⎍	H	L	H
Count Down	H	⎍	L	H
Reset	X	X	H	X
Load Preset Inputs	X	X	L	L

H = High Level, L = Low Level, X = Immaterial, ⎍ = Transition from low to high

Functional Diagram



Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 500ns Max.
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.80V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.80V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	0.5	µA
			2, 3	+125°C, -55°C	-5.0	5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CPU to Qn	TPLH	VCC = 4.5V	9	+25°C	2	29	ns
			10, 11	+125°C, -55°C	2	34	ns
	TPHL	VCC = 4.5V	9	+25°C	2	35	ns
			10, 11	+125°C, -55°C	2	41	ns
CPD to Qn	TPLH	VCC = 4.5V	9	+25°C	2	31	ns
			10, 11	+125°C, -55°C	2	36	ns
	TPHL	VCC = 4.5V	9	+25°C	2	36	ns
			10, 11	+125°C, -55°C	2	42	ns
$\overline{PL}$ to Qn	TPLH	VCC = 4.5V	9	+25°C	2	32	ns
			10, 11	+125°C, -55°C	2	36	ns
	TPHL	VCC = 4.5V	9	+25°C	2	45	ns
			10, 11	+125°C, -55°C	2	53	ns
MR to Qn	TPHL	VCC = 4.5V	9	+25°C	2	37	ns
			10, 11	+125°C, -55°C	2	44	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 35		pF
			1	+125°C	Typical 50		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C, -55°C	-	22	ns
Maximum Operating Frequency (CPU, CPD)	FMAX	VCC = 4.5V	1	+25°C	-	25	MHz
			1	+125°C, -55°C	-	15	MHz
Setup Time Pn to $\overline{PL}$	TSU	VCC = 4.5V	1	+25°C	15	-	ns
			1	+125°C, -55°C	22	-	ns
Hold Time Pn to $\overline{PL}$	TH	VCC = 4.5V	1	+25°C	0	-	ns
			1	+125°C, -55°C	0	-	ns
Hold Time CPD to CPU or CPU to CPD	TH	VCC = 4.5V	1	+25°C	16	-	ns
			1	+125°C, -55°C	24	-	ns
Pulse Width CPU to CPD	TW	VCC = 4.5V	1	+25°C	23	-	ns
			1	+125°C, -55°C	35	-	ns
Pulse Width $\overline{PL}$	TW	VCC = 4.5V	1	+25°C	16	-	ns
			1	+125°C, -55°C	24	-	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Pulse Width MR	TW	VCC = 4.5V	1	+25°C	20	-	ns
			1	+125°C, 55°C	30	-	ns
Recovery Time $\overline{PL}$ to CPU, CPD	TREC	VCC = 4.5V	1	+25°C	15	-	ns
			1	+125°C, 55°C	22	-	ns
Recovery Time MR to CPU, CPD	TREC	VCC = 4.5V	1	+25°C	5	-	ns
			1	+125°C, 55°C	5	-	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
CPU to Qn	TPLH	VCC = 4.5V	+25°C	2	34	2	43	ns
	TPHL	VCC = 4.5V	+25°C	2	41	2	51	ns
CPD to Qn	TPLH	VCC = 4.5V	+25°C	2	36	2	45	ns
	TPHL	VCC = 4.5V	+25°C	2	42	2	53	ns
$\overline{PL}$ to Qn	TPLH	VCC = 4.5V	+25°C	2	36	2	45	ns
	TPHL	VCC = 4.5V	+25°C	2	53	2	66	ns
MR to Qn	TPHL	VCC = 4.5V	+25°C	2	44	2	55	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternate Group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE: 1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
2, 3, 6, 7, 12, 13	1, 4, 5, 8 - 11, 14, 15	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
2, 3, 6, 7, 12, 13	8	-	1, 4, 5, 9 - 11, 14 - 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	1, 4, 5, 8 - 10, 15	2, 3, 6, 7, 12, 13	11, 16	14	-

NOTES:

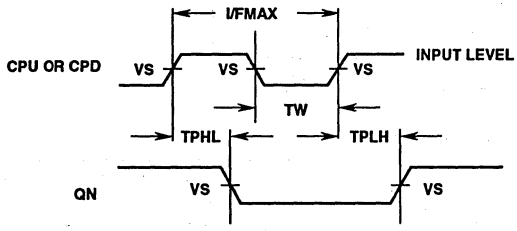
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

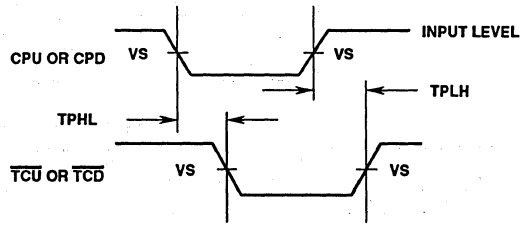
OPEN	GROUND	VCC = 5V ± 0.5V
2, 3, 6, 7, 12, 13	8	1, 4, 5, 9 - 11, 14 - 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

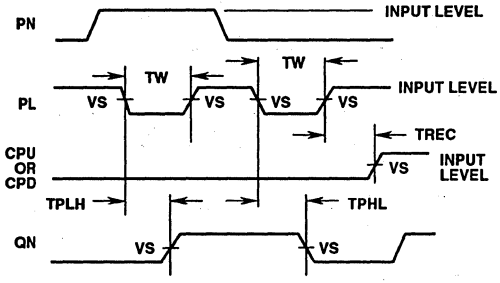
AC Timing Diagrams



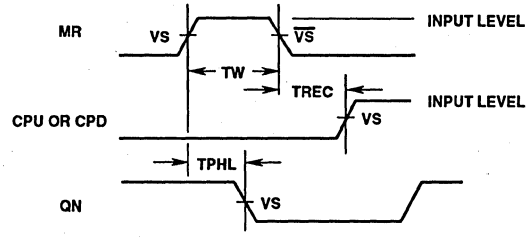
CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



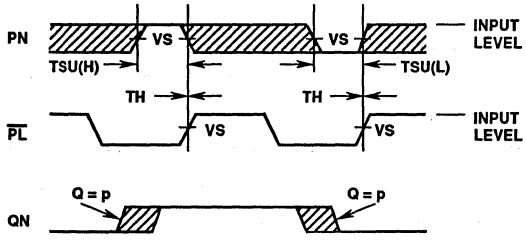
CLOCK TO TERMINAL COUNT DELAYS



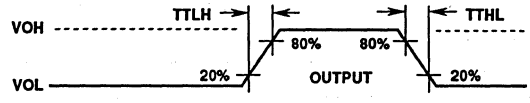
PARALLEL LOAD PULSE WIDTH, PARALLEL LOAD TO OUTPUT DELAYS, AND PARALLEL LOAD TO CLOCK RECOVERY TIME



MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



SETUP AND HOLD TIMES DATA TO PARALLEL LOAD (PL)



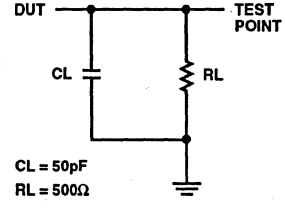
OUTPUT TRANSITION TIME

AC Timing Diagrams

AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
104 x 86 mils

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

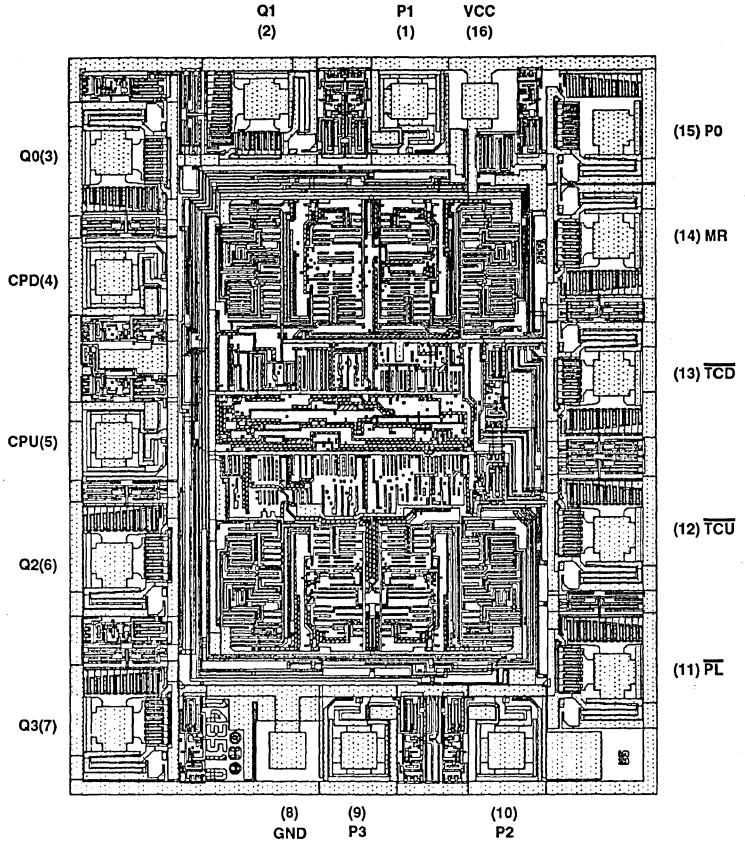
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$< 2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS193MS



HARRIS SEMICONDUCTOR

HCS195MS

Radiation Hardened Inverting 8-Bit Parallel-Input/Serial Output Shift Register

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity 2 x 10^{-9} Error/Bit Day (Typ)
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Standard Outputs - 10 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.3 VCC Max
  - VIH = 0.7 VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

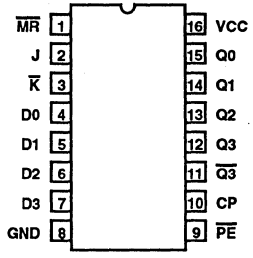
The Harris HCS195MS is a Radiation Hardened 8-Bit Parallel-In/Serial-Out Shift Register with complementary serial outputs and an asynchronous parallel load input.

The HCS195MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

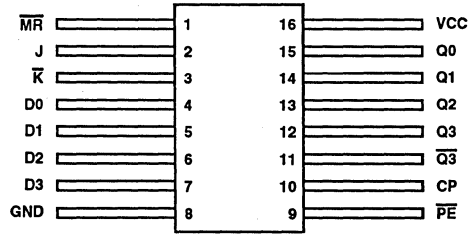
The HCS195MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR, CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR, CDFP4-F16, LEAD FINISH C
TOP VIEW



Truth Table

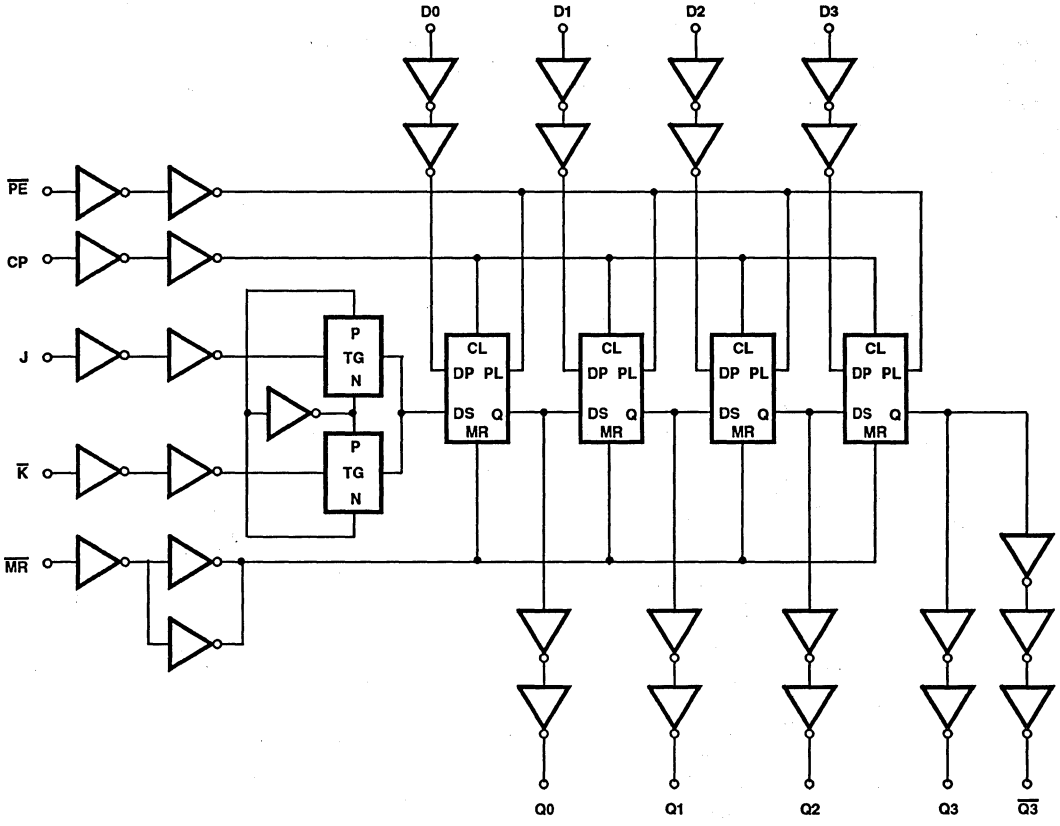
INPUTS						OUTPUTS				
$\overline{MR}$	CP	$\overline{PE}$	J	$\overline{K}$	Dn	Q0	Q1	Q2	Q3	$\overline{Q3}$
L	X	X	X	X	X	L	L	L	L	H
H	↗	h	h	h	X	H	q0	ql	q2	q3
H	↗	h	l	l	X	L	q0	ql	q2	q3
H	↗	h	h	l	X	$\overline{q0}$	q0	ql	q2	q3
H	↗	h	l	h	X	q0	q0	ql	q2	q3
H	↗	l	X	X	dn	d0	dl	d2	d3	$\overline{d3}$

Dn or Qn = referenced input (or output) one set-up time prior to clock
l or h = level one set-up time prior to clock
↗ = positive clock

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3385

Functional Diagram



Absolute Maximum Ratings

Supply Voltage (VCC) ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1
(All voltage reference to VSS)

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC) ..... +4.5V to +5.5V
Input Rise and Fall Times at VCC = 4.5V (TR, TF) ..... 10ns Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0V to 30% of VCC
Input High Voltage (VIH) ..... VCC to 70% of VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V (Note 2)	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V (Note 2)	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 3)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltages reference to device GND.
2. Force/measure functions may be interchanged.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay (CP - Qn)	TPHL1	VCC = 4.5V, VIH = 4.5V VIL = 0	9	+25°C	2	31	ns
			10, 11	+125°C, -55°C	2	37	ns
Propagation Delay (CP - Qn)	TPLH1	VCC = 4.5V, VIH = 4.5V VIL = 0	9	+25°C	2	34	ns
			10, 11	+125°C, -55°C	2	42	ns
Propagation Delay (MR - Q0-3)	TPHL2	VCC = 4.5V, VIH = 4.5V VIL = 0	9	+25°C	2	32	ns
			10, 11	+125°C, -55°C	2	39	ns
Propagation Delay (MR - $\overline{Q3}$)	TPLH2	VCC = 4.5V, VIH = 4.5V VIL = 0	9	+25°C	2	32	ns
			10, 11	+125°C, -55°C	2	39	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF.= 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, VIH = 5.0V, VIL = 0.0V, f = 1MHz	1	+25°C	Typical 60		pF
			1	+125°C	Typical 80		pF
Input Capacitance	CIN	VCC = 5.0V, VIH = 5.0V, VIL = 0.0V, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Capacitance	COUT	VCC = 5.0V, VIH = 5.0V, VIL = 0.0V, f = 1MHz	1	+25°C	-	20	pF
			1	+125°C	-	20	pF
Pulse Width Time (CP or MR)	TW	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	16	-	ns
			1	+125°C	24	-	ns
Setup Time	TSU	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	20	-	ns
			1	+125°C	20	-	ns
Hold Time	TH	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	3	-	ns
			1	+125°C	3	-	ns
MR to CP Removal Time	TREM	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	16	-	ns
			1	+125°C	24	-	ns
Recovery Time $\overline{PL}$ to CP	TREC	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	20	-	ns
			1	+125°C	30	-	ns
Maximum Clock Frequency	FMAX	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	30	-	MHz
			1	+125°C	20	-	MHz
Output Transition Time	TTHL TTLH	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	1	15	ns
			1	+125°C	1	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Propagation Delay (CP - Qn)	TPHL1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	37	2	46.3	ns
Propagation Delay (CP - Qn)	TPLH1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	42	2	52.5	ns
Propagation Delay (MR - Q0-3)	TPHL2	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	39	2	48.8	ns
Propagation Delay (MR - $\overline{Q3}$)	TPLH2	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	39	2	48.8	ns

NOTES:
1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternate Group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1,9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
11 - 15	1 - 10	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
11 - 15	8	-	1 - 7, 10, 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	8, 9	1 - 3, 16	11 - 15	10	4 - 7

NOTES:

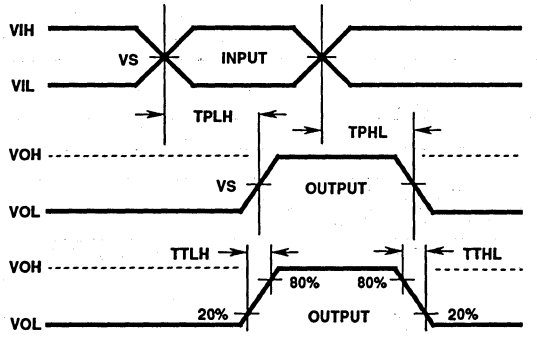
1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680kΩ ± 5% for dynamic burn-in

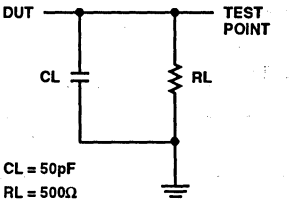
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
11 - 15	8	1 - 7, 10, 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

AC Timing Diagram and Load Circuit

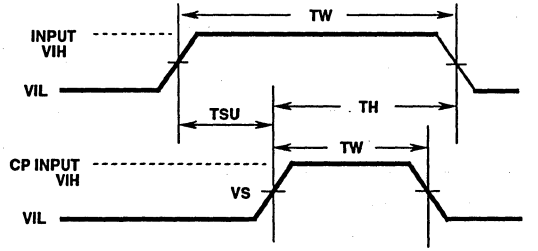




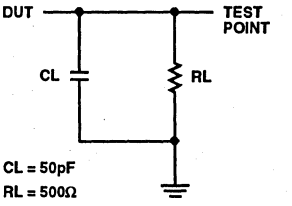
AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

Pulse Width, Setup, Hold Timing Diagram Positive Edge Trigger



TH = Hold Time
TSU = Setup Time
TW = Pulse Width



AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
95 x 94 mils
2.380 x 2.410mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

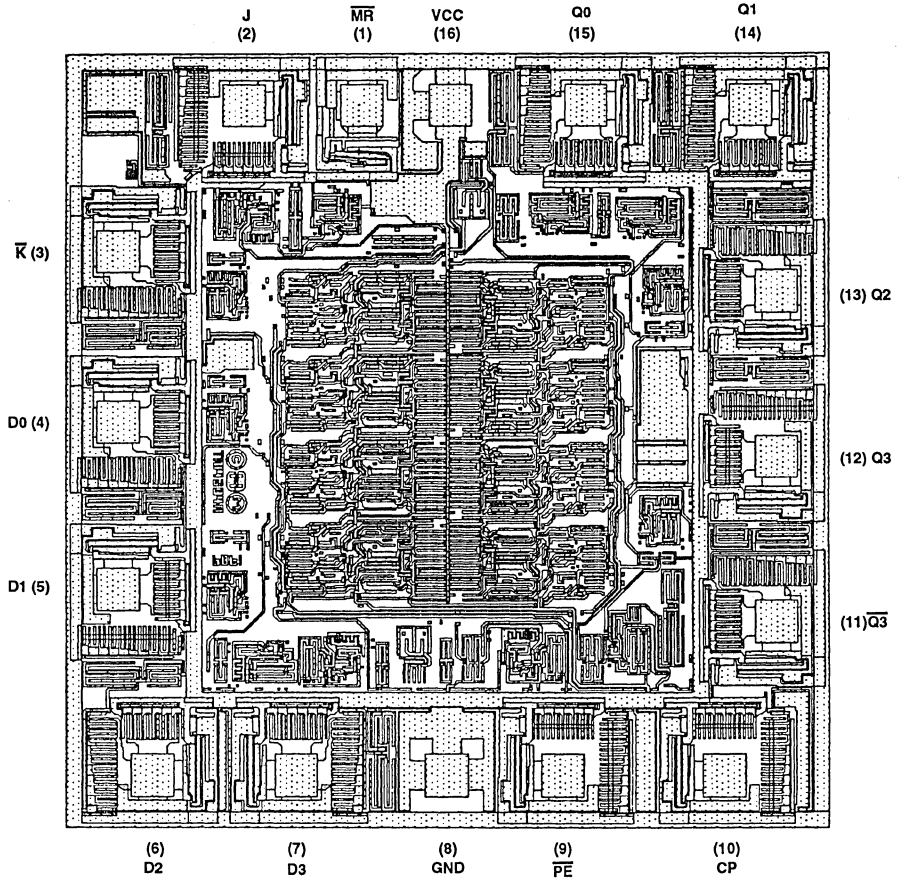
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCS195MS



HARRIS SEMICONDUCTOR

HCTS240MS

Radiation Hardened Octal Buffer/Line Driver, Tri-State

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Bus Driver Outputs ..... 15 LSTTL Loads
- Military Temperature Range ..... -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range ..... 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

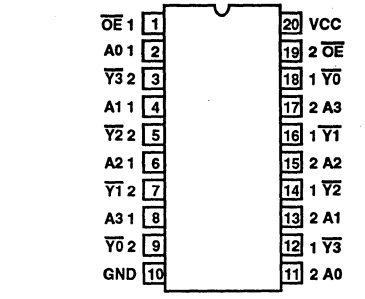
The Harris HCTS240MS is a Radiation Hardened inverting octal buffer/line driver, tri-state, with two active low output enables.

The HCTS240MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family .

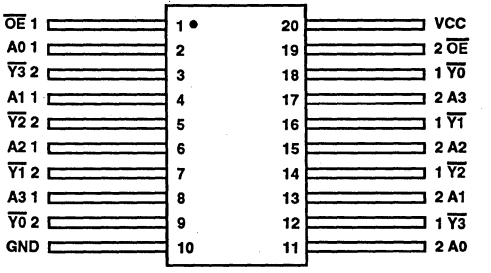
The HCTS240MS is supplied in a 20 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

20 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T20, LEAD FINISH C
TOP VIEW



20 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F20, LEAD FINISH C
TOP VIEW

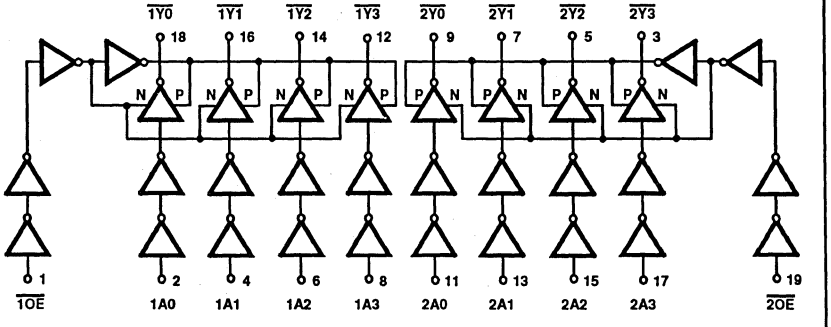


Truth Table

INPUTS		OUTPUT
$\overline{10E}$, $\overline{20E}$	A	Y
L	L	H
L	H	L
H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Functional Diagram



File Number 2105.1

Absolute Maximum Ratings

Supply Voltage (VCC) ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 500ns Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... 2.0V to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V	1	+25°C	-7.2	-	mA
			2, 3	+125°C, -55°C	-6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	0.5	µA
			2, 3	+125°C, -55°C	-5.0	5.0	µA
Tri-State Output Leakage Current	IOZ	VCC = 4.5V and 5.5V, Applied Voltage = 0V or VCC	1	+25°C	-1	+1	µA
			2, 3	+125°C, -55°C	-50	+50	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Output	TPHL TPLH	VCC = 4.5V	9	+25°C	2	15	ns
			10, 11	+125°C, -55°C	2	20	ns
Enable to Output	TPZL TPZH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	25	ns
Disable to Output	TPLZ TPHZ	VCC = 4.5V	9	+25°C	2	25	ns
			10, 11	+125°C, -55°C	2	35	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input tr = tf = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	+25°C	Typical 35		pF
			+125°C	Typical 60		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	+25°C	-	10	pF
			+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	+25°C	-	12	ns
			+125°C, -55°C	-	18	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	3.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	5.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-5.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	µA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Input to Output	TPHL TPLH	VCC = 4.5V	+25°C	2	20	2	25	ns
Enable to Output	TPZL TPZH	VCC = 4.5V	+25°C	2	25	2	32	ns
Disable to Output	TPLZ TPHZ	VCC = 4.5V	+25°C	2	35	2	44	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour
IOZL/IOZH	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A inspection in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
3, 5, 7, 9, 12, 14, 16, 18	1, 2, 4, 6, 8, 10, 11, 13, 15, 17, 19	-	20	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 5, 7, 9, 12, 14, 16, 18	10	-	1, 2, 4, 6, 8, 11, 13, 15, 17, 19, 20	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	1, 10, 19	3, 5, 7, 9, 12, 14, 16, 18	20	2, 4, 6, 8, 11, 13, 15, 17	-

NOTES:

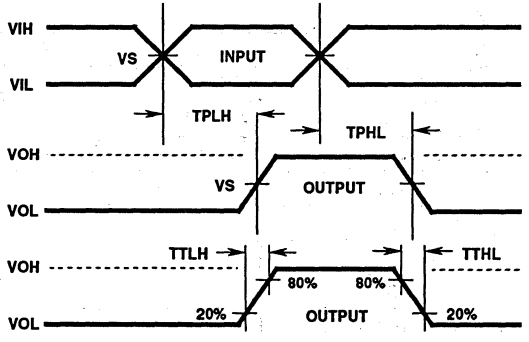
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680Ω ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 5, 7, 9, 12, 14, 16, 18	10	1, 2, 4, 6, 8, 11, 13, 15, 17, 19, 20

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

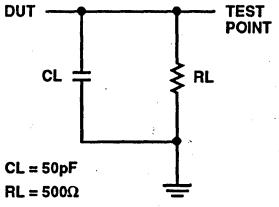
AC Timing Diagrams



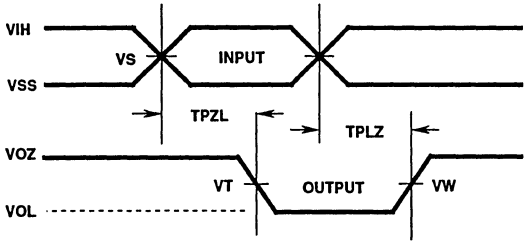
AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



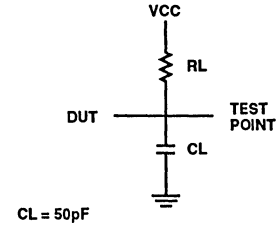
Tri-State Low Timing Diagrams



TRI-STATE LOW VOLTAGE LEVELS

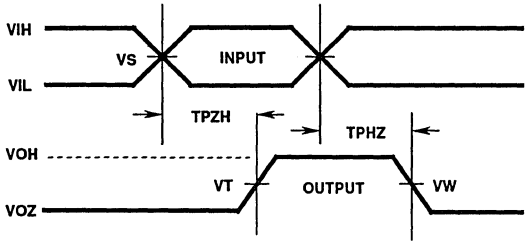
PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	0.90	V
GND	0	V

Tri-State Low Load Circuit



CL = 50pF
RL = 500Ω

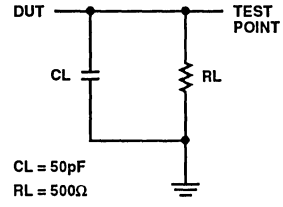
Tri-State High Timing Diagrams



TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	3.60	V
GND	0	V

Tri-State High Load Circuit



CL = 50pF
RL = 500Ω

Die Characteristics

DIE DIMENSIONS:
102 x 70 mils

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

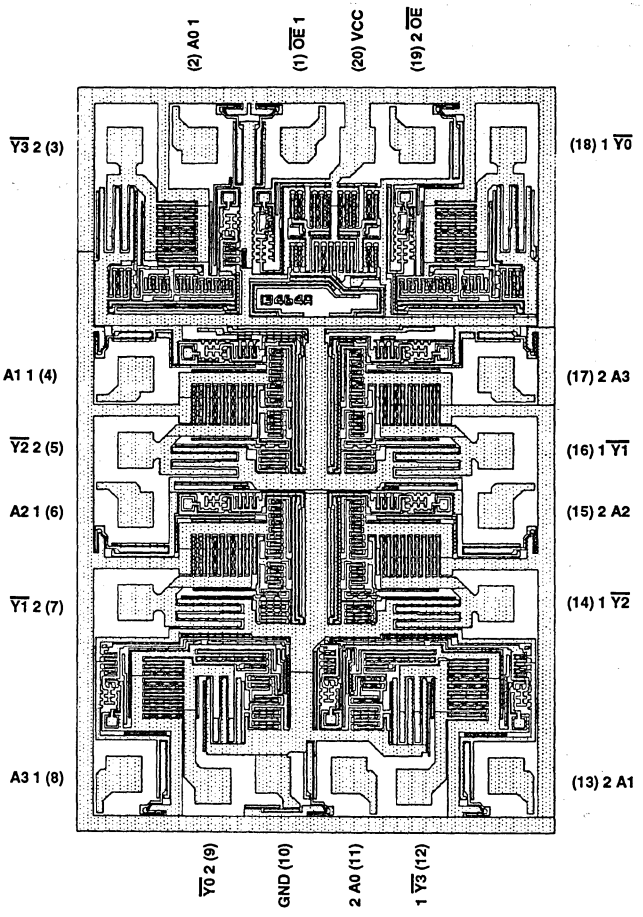
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS240MS



HARRIS SEMICONDUCTOR

HCS244MS

Radiation Hardened Octal Buffer/Line Driver, Tri-State

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)/s
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Bus Driver Outputs - 15 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.3 VCC Max
  - VIH = 0.7 VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

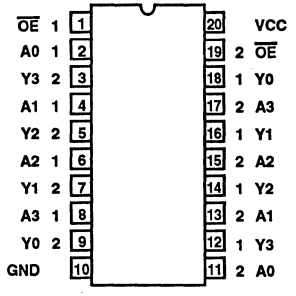
The Harris HCS244MS is a Radiation Hardened Non-Inverting Octal Buffer/Line Driver, Tri-State, with two active-low output enables.

The HCS244MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

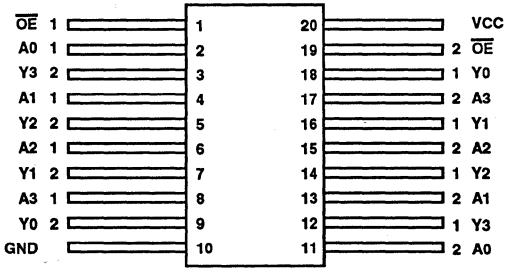
The HCS244MS is supplied in a 20 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

20 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T20, LEAD FINISH C
TOP VIEW



20 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F20, LEAD FINISH C
TOP VIEW

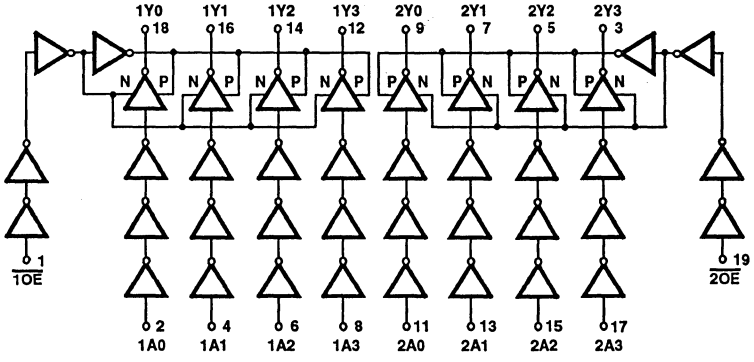


Truth Table

INPUTS		OUTPUT
$\overline{1OE}$, $\overline{2OE}$	A	Y
L	L	L
L	H	H
H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Functional Diagram



7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2132.1**

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 500ns Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 30% of VCC
Input High Voltage (VIH) ..... 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC, VCC = 4.5V and 5.5V	1	+25°C	-	±1	µA
			2, 3	+125°C, -55°C	-	±50	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Data to Output	TPLH TPHL	VCC = 4.5V	9	+25°C	2	21	ns
			10, 11	+125°C, -55°C	2	25	ns
Enable to Output	TPZL	VCC = 4.5V	9	+25°C	2	25	ns
			10, 11	+125°C, -55°C	2	30	ns
Enable to Output	TPZH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	24	ns
Disable to Output	TPLZ TPHZ	VCC = 4.5V	9	+25°C	2	25	ns
			10, 11	+125°C, -55°C	2	30	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 30		pF
			1	+125°C	Typical 30		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	12	ns
			1	+125°C, -55°C	-	18	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	3.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	5.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-5.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC	+25°C	-	±50	-	±100	μA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, (Note 3)	+25°C	-	-	-	-	-
Propagation Delay Data to Output	TPLH, TPHL	VCC = 4.5V	+25°C	2	25	2	32	ns
Enable to Output	TPZL	VCC = 4.5V	+25°C	2	30	2	38	ns
Enable to Output	TPZH	VCC = 4.5V	+25°C	2	24	2	30	ns
Disable to Output	TPLZ, TPHZ	VCC = 4.5V	+25°C	2	30	2	38	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour
IOZL/IOZH	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternate group A testing in accordance with Method 5005 of Mil-Std-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% go/no-go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC I BURN-IN (Note 1)					
3, 5, 7, 9, 12, 14, 16, 18	1, 2, 4, 6, 8, 10, 11, 13, 15, 17, 19	-	20	-	-
STATIC II BURN-IN (Note 1)					
3, 5, 7, 9, 12, 14, 16, 18	10	-	1, 2, 4, 6, 8, 11, 13, 15, 17, 19, 20	-	-
DYNAMIC BURN-IN (Note 2)					
-	1, 10, 19	3, 5, 7, 9, 12, 14, 16, 18	20	2, 4, 6, 8, 11, 13, 15, 17	-

NOTES:

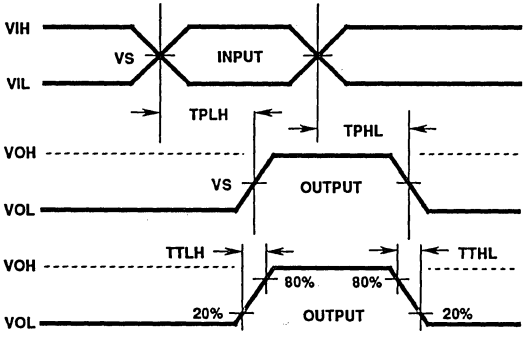
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for dynamic burn-in

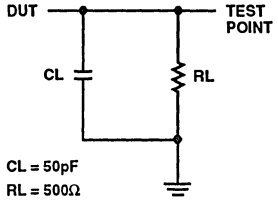
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 5, 7, 9, 12, 14, 16, 18	10	1, 2, 4, 6, 8, 11, 13, 15, 17, 19, 20

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

AC Timing Diagrams and Load Circuit

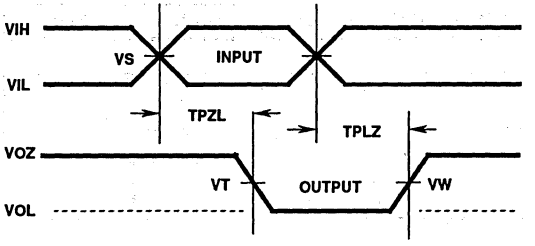


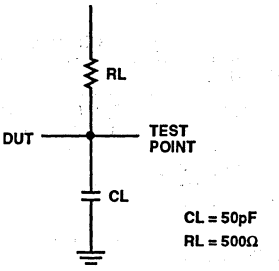


AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Tri-State Low Timing Diagrams and Load Circuit

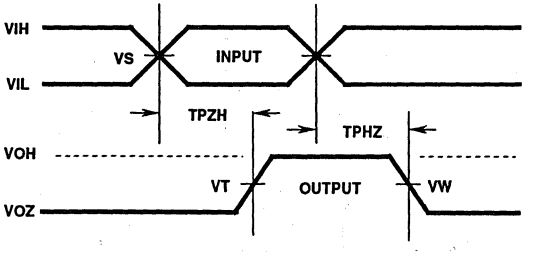


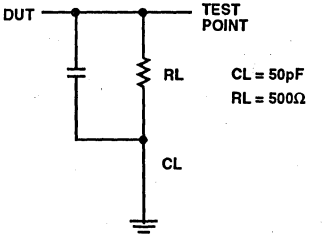


TRI-STATE LOW VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	0.90	V
GND	0	V

Tri-State High Timing Diagrams and Load Circuit





TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	3.60	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
108 x 106 mils

METALLIZATION:
Type: Al/Sil
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

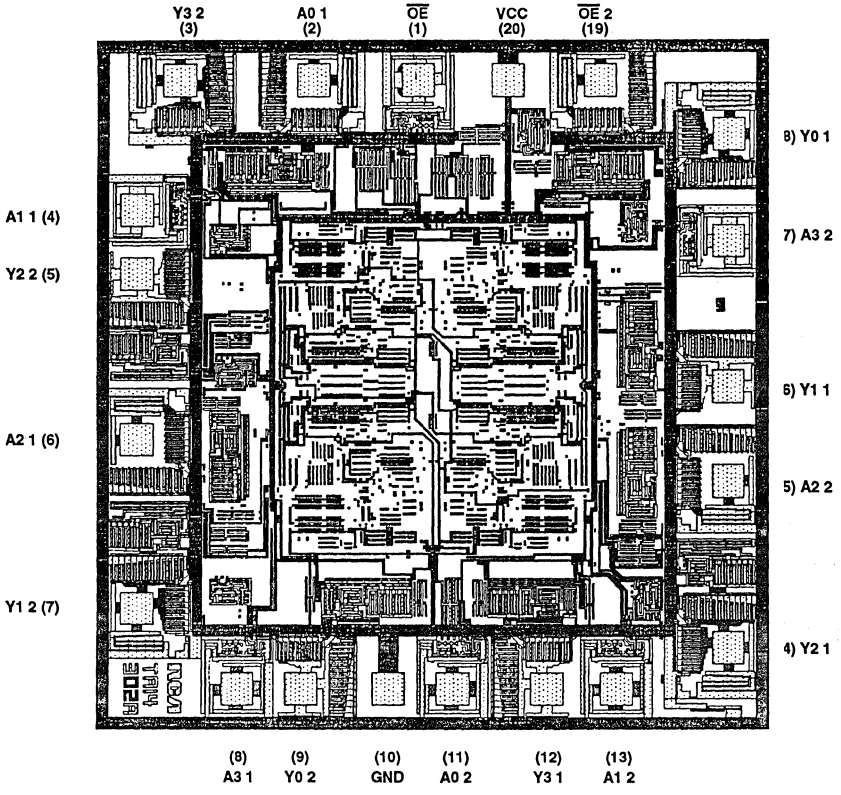
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCS244MS



HARRIS SEMICONDUCTOR

HCTS244MS

Radiation Hardened Octal Buffer/Line Driver, Tri-State

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Bus Driver Outputs - 15 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

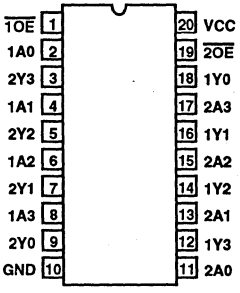
The Harris HCTS244MS is a Radiation Hardened Non-Inverting Octal Buffer/Line Driver, Tri-State, with two active-low output enables.

The HCTS244MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

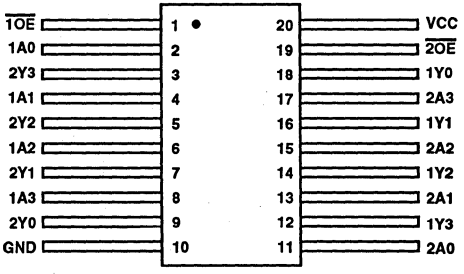
The HCTS244MS is supplied in a 20 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

20 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR, CDIP2-T20, LEAD FINISH C
TOP VIEW



20 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR, CDFP4-F20, LEAD FINISH C
TOP VIEW

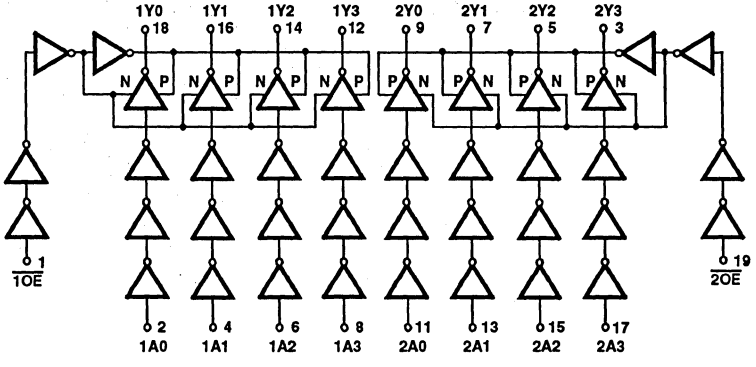


Truth Table

INPUTS		OUTPUT
$\overline{1OE}, \overline{2OE}$	A	Y
L	L	L
L	H	H
H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2133.1**

Absolute Maximum Ratings

Supply Voltage (VCC) ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC) ..... +4.5V to +5.5V
Input Rise and Fall Times at VCC = 4.5V (tr, tf) ..... 500ns Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-7.2	-	mA
			2, 3	+125°C, -55°C	-6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Tri-State Output Leakage Current	IOZ	VCC = 4.5V or 5.5V, Applied Voltage = 0V or VCC	1	+25°C	-1	+1	µA
			2, 3	+125°C, -55°C	-50	+50	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Data to Output	TPLH	VCC = 4.5V	9	+25°C	2	17	ns
			10, 11	+125°C, -55°C	2	20	ns
Data to Output	TPHL	VCC = 4.5V	9	+25°C	2	23	ns
			10, 11	+125°C, -55°C	2	26	ns
Enable to Output	TPZL	VCC = 4.5V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	32	ns
Enable to Output	TPZH	VCC = 4.5V	9	+25°C	2	22	ns
			10, 11	+125°C, -55°C	2	25	ns
Disable to Output	TPLZ TPHZ	VCC = 4.5V	9	+25°C	2	22	ns
			10, 11	+125°C, -55°C	2	25	ns

NOTES:
1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 30		pF
			1	+125°C	Typical 30		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	12	ns
			1	+125°C, -55°C	-	18	ns

NOTES:
1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	3.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	5.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-5.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	±5	-5	±5	μA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC	+25°C	-	±50	-	±100	μA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Propagation Delay Data to Output	TPLH	VCC = 4.5V	+25°C	2	20	2	25	ns
Data to Output	TPHL	VCC = 4.5V	+25°C	2	26	2	33	ns
Enable to Output	TPZL	VCC = 4.5V	+25°C	2	32	2	40	ns
Enable to Output	TPZH	VCC = 4.5V	+25°C	2	25	2	35	ns
Disable to Output	TPLZ TPHZ	VCC = 4.5V	+25°C	2	25	2	32	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour
IOZL/IOZH	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
3, 5, 7, 9, 12, 14, 16, 18	1, 2, 4, 6, 8, 10, 11, 13, 15, 17, 19	-	20	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 5, 7, 9, 12, 14, 16, 18	10	-	1, 2, 4, 6, 8, 11, 13, 15, 17, 19, 20	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	1, 10, 19	3, 5, 7, 9, 12, 14, 16, 18	20	2, 4, 6, 8, 11, 13, 15, 17	-

NOTES:

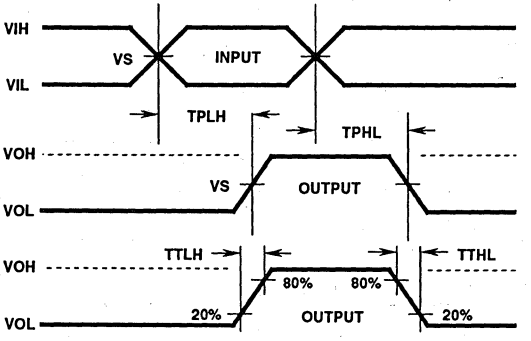
1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680kΩ ± 5% for dynamic burn-in

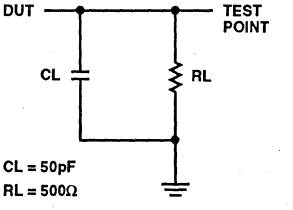
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 5, 7, 9, 12, 14, 16, 18	10	1, 2, 4, 6, 8, 11, 13, 15, 17, 19, 20

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

AC Timing Diagram and Load Circuit

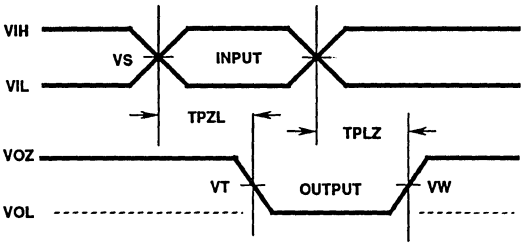


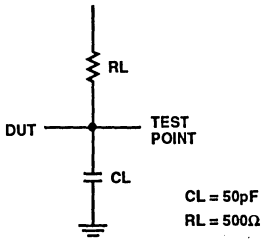


AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Tri-State Low Timing Diagram and Load Circuit

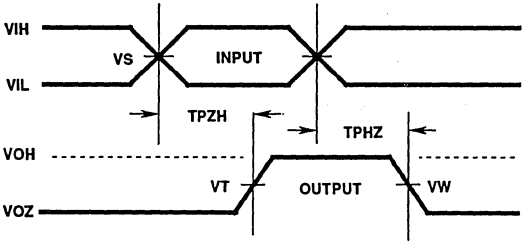


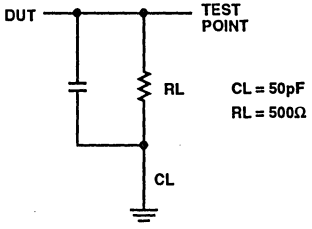


TRI-STATE LOW VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	0.90	V
GND	0	V

Tri-State High Timing Diagram and Load Circuit





TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	3.60	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
108 x 106 mils

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

DIE ATTACH:
Material: Silver Epoxy

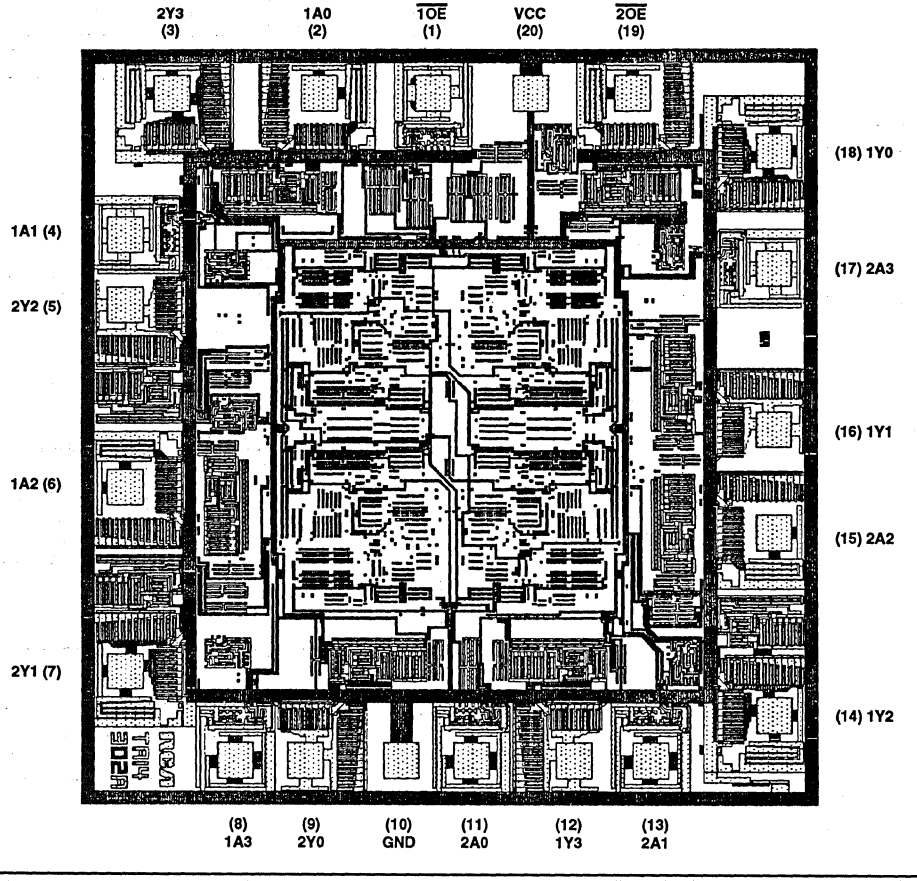
WORST CASE CURRENT DENSITY:
$2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm

4 x 4 mils

Metallization Mask Layout

HCTS244MS



HARRIS SEMICONDUCTOR

HCS245MS

Radiation Hardened Octal Bus Transceiver, Tri-State, Non-Inverting

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Bus Driver Outputs - 15 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

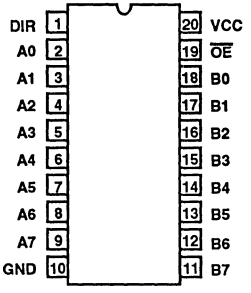
The Harris HCS245MS is a Radiation Hardened Non-Inverting Octal Bidirectional Bus Transceiver, Tri-State, intended for two-way asynchronous communication between data busses. The HCS245MS allows data transmission from the A bus to the B bus or from the B bus to the A bus. The logic level at the direction input (DIR) determines the data direction. The output enable input ($\overline{OE}$) puts the I/O port in the high-impedance state when high.

The HCS245MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

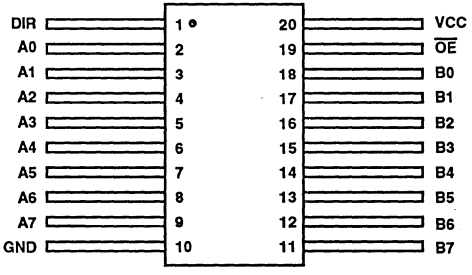
The HCS245MS is supplied in a 20 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

20 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T20, LEAD FINISH C
TOP VIEW



20 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F20, LEAD FINISH C
TOP VIEW



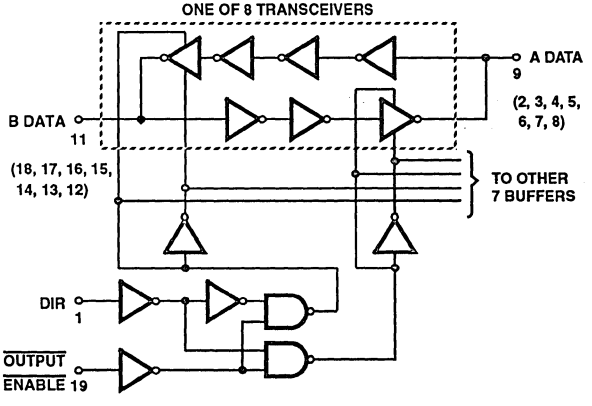
Truth Table

CONTROL INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

H = High Voltage Level, L = Low Voltage Level,
X = Immaterial

To prevent excess currents in the High-Z (Isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

Functional Diagram



7 LOGIC

File Number 2468.1

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 500ns Max.
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 30% of VCC
Input High Voltage (VIH) . . . . . 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND, VCC = 4.5V and 5.5V	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC	1	+25°C	-	±1	µA
			2, 3	+125°C, -55°C	-	±50	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Data to Output	TPLH TPHL	VCC = 4.5V	9	+25°C	2	19	ns
			10, 11	+125°C, -55°C	2	23	ns
Enable to Output	TPZL TPZH	VCC = 4.5V	9	+25°C	2	26	ns
			10, 11	+125°C, -55°C	2	30	ns
Disable to Output	TPLZ TPHZ	VCC = 4.5V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	33	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 45		pF
			1	+125°C, -55°C	Typical 45		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C, -55°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	12	ns
			1	+125°C, -55°C	-	18	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	3.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	5.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-5.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC	+25°C	-	±50	-	±100	µA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Propagation Delay Data to Output	TPLH TPHL	VCC = 4.5V	+25°C	2	23	2	28	ns
Enable to Output	TPZL TPZH	VCC = 4.5V	+25°C	2	30	2	36	ns
Enable to Output	TPLZ TPHZ	VCC = 4.5V	+25°C	2	33	2	33	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour
IOZL/IOZH	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC BURN-IN AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
2 - 9	1, 10 - 19	-	20	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
-	10	-	1 - 9, 11 - 20	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	10	11 - 18	1, 20	2 - 9	19

NOTES:

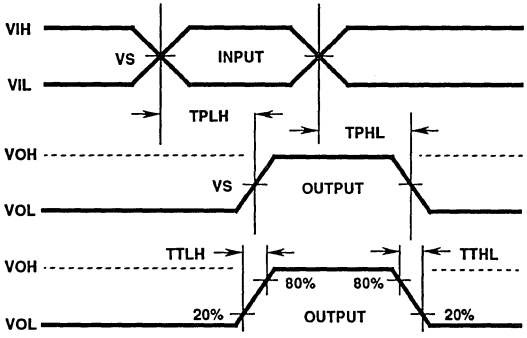
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 680Ω ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
-	10	1 - 9, 11 - 20

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

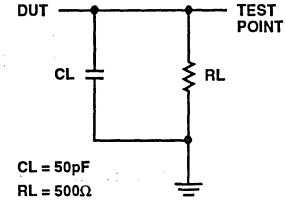
AC Timing Diagrams



AC VOLTAGE LEVELS

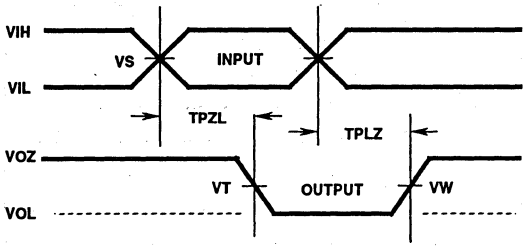
PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

AC Load Circuit



7 LOGIC

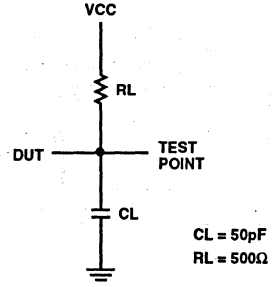
Tri-State Low Timing Diagrams



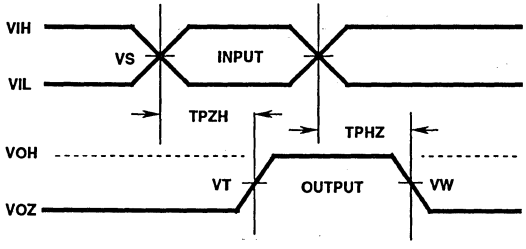
TRI-STATE LOW VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	0.90	V
GND	0	V

Tri-State Low Load Circuit



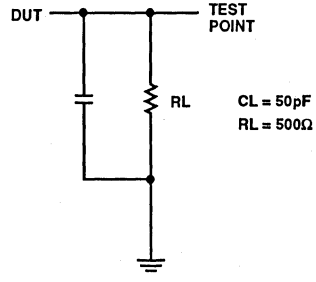
Tri-State High Timing Diagrams



TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	3.60	V
GND	0	V

Tri-State High Load Circuit



Die Characteristics

DIE DIMENSIONS:
124 x 110 mils

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± -2.6kÅ

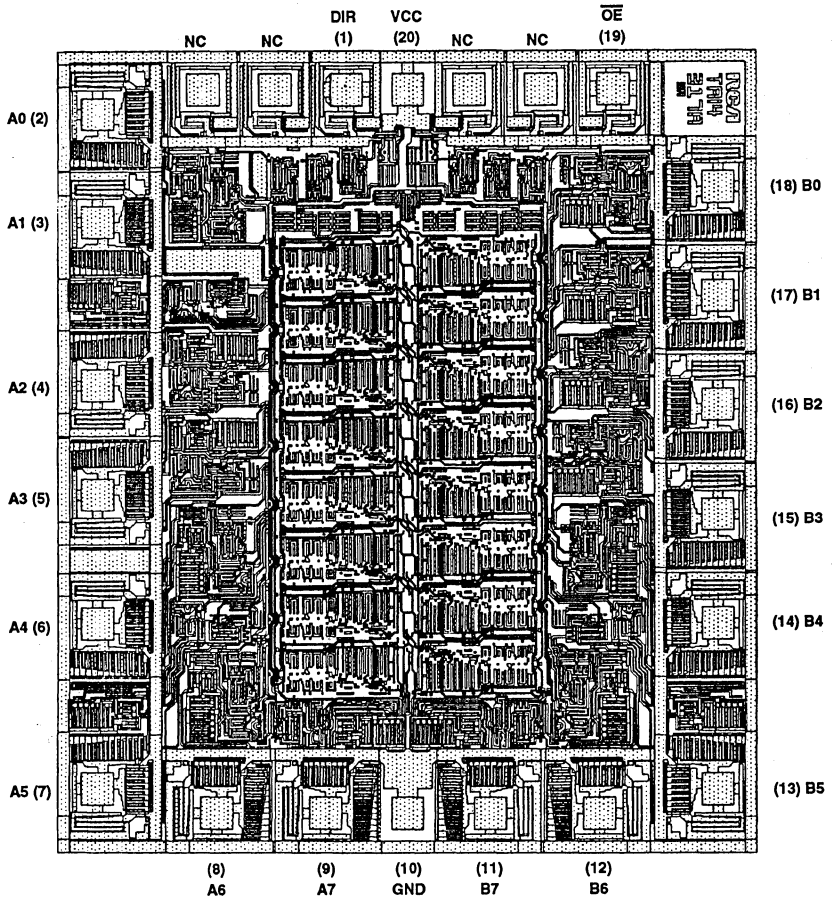
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCS245MS



HARRIS SEMICONDUCTOR

HCTS245MS

Radiation Hardened Octal Bus Transceiver, Tri-State, Non-Inverting

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Bus Driver Outputs - 15 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels II ≤ 5μA at VOL, VOH

Description

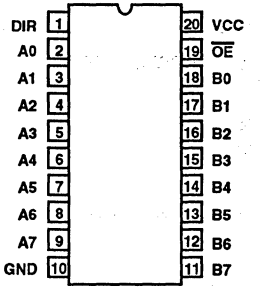
The Harris HCTS245MS is a Radiation Hardened Non-Inverting Octal Bidirectional Bus Transceiver, Tri-State, intended for two-way asynchronous communication between data busses. The HCTS245MS allows data transmission from the A bus to the B bus or from the B bus to the A bus. The logic level at the direction input ($\overline{DIR}$) determines the data direction. The output enable input ($\overline{OE}$) puts the I/O port in the high-impedance state when high.

The HCTS245MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

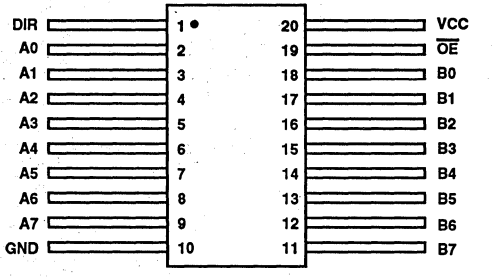
The HCTS245MS is supplied in a 20 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

20 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T20, LEAD FINISH C
TOP VIEW



20 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F20, LEAD FINISH C
TOP VIEW



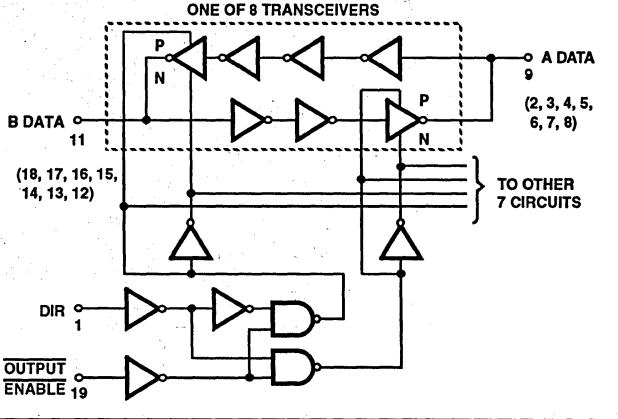
Truth Table

CONTROL INPUTS		
$\overline{OE}$	DIR	OPERATION
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

H = High Voltage Level, L = Low Voltage Level,
X = Immaterial

To prevent excess currents in the High-Z (Isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

Functional Diagram



File Number **2360.1**

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 500ns Max
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-7.2	-	mA
			2, 3	+125°C, -55°C	-6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Tri-State Output Leakage Current	IOZ	VCC = 4.5V or 5.5V, Applied Voltage = 0V or VCC	1	+25°C	-1	+1	µA
			2, 3	+125°C, -55°C	-50	+50	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Data to Output	TPLH	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	21	ns
	TPHL	VCC = 4.5V	9	+25°C	2	21	ns
			10, 11	+125°C, -55°C	2	24	ns
Enable to Output	TPZL	VCC = 4.5V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	33	ns
	TPZH	VCC = 4.5V	9	+25°C	2	26	ns
			10, 11	+125°C, -55°C	2	31	ns
Disable to Output	TPLZ TPHZ	VCC = 4.5V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	33	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 45		pF
			1	+125°C	Typical 45		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	12	ns
			1	+125°C, 55°C	-	18	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	3.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	µA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC, VCC = 4.5V and 5.5V	+25°C	-	±50	-	±100	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Propagation Delay Data to Output	TPLH TPHL	VCC = 4.5V	+25°C	2	21	2	26	ns
				2	24	2	30	
Enable to Output	TPZL TPZH	VCC = 4.5V	+25°C	2	33	2	39	ns
				2	31	2	37	ns
Disable to Output	TPLZ TPHZ	VCC = 4.5V		2	33	2	33	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour
IOZL/IOZH	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternate Group A Testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE: 1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
2 - 9	1, 10 - 19	-	20	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
-	10	-	1 - 9, 11 - 20	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	10	11 - 18	1, 20	2 - 9	19

NOTES:

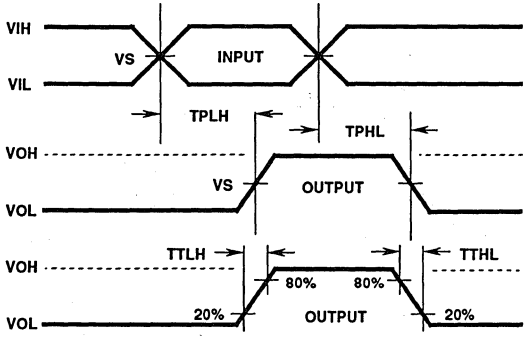
1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
-	10	1 - 9, 11 - 20

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

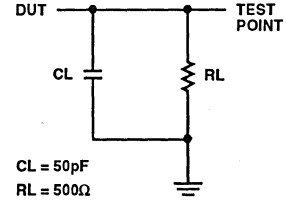
AC Timing Diagrams



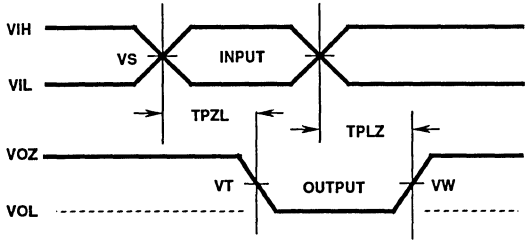
AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



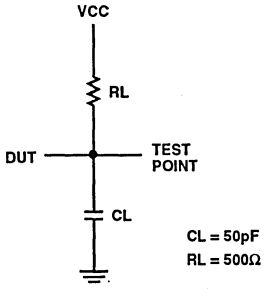
Tri-State Low Timing Diagrams



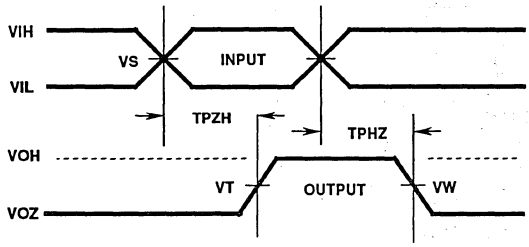
TRI-STATE LOW VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	0.90	V
GND	0	V

Tri-State Low Load Circuit



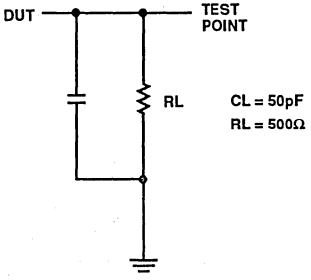
Tri-State High Timing Diagrams



TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	3.60	V
GND	0	V

Tri-State High Load Circuit



Die Characteristics

DIE DIMENSIONS:
124 x 110 mils

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

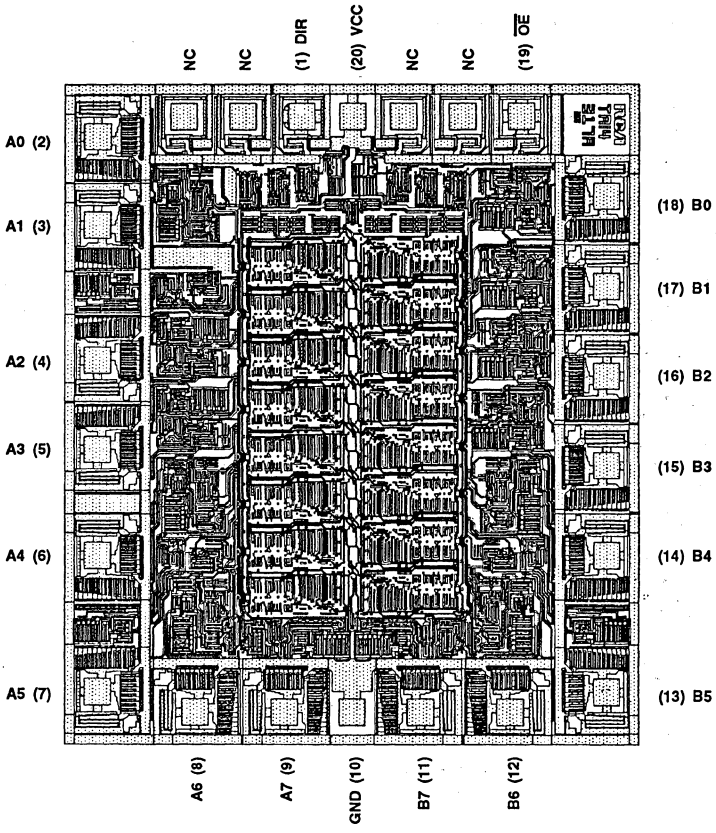
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS245MS



HARRIS SEMICONDUCTOR

HCS253MS

Radiation Hardened Dual 4-Input Multiplexer

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Bus Driver Outputs - 15 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.3 VCC Max
  - VIH = 0.7 VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

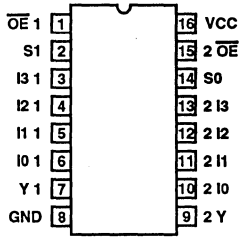
The Harris HCS253MS is a Radiation Hardened 4-to-1 line selector multiplexer having tri-state outputs. One of four sources for each section is selected by the common select inputs S0 and S1. When the output enable ($\overline{1OE}$ or $\overline{2OE}$) is HIGH, the output is in the high impedance state.

The HCS253MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

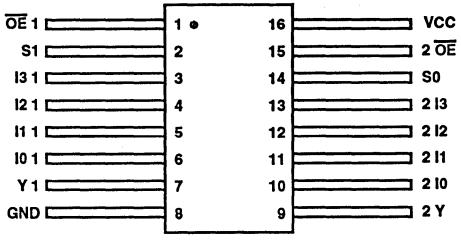
The HCS253MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP16-F16, LEAD FINISH C
TOP VIEW



Truth Table

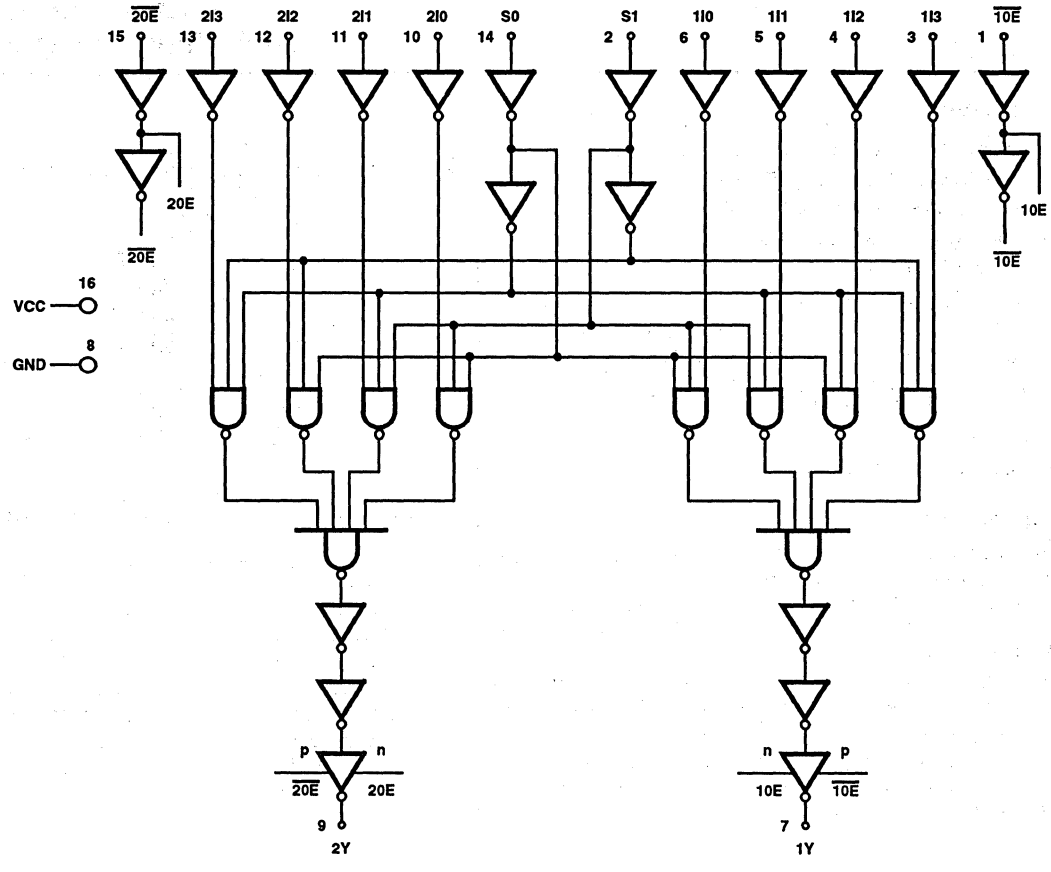
SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S1	S0	I0	I1	I2	I3	$\overline{OE}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs S0 and S1 are common to both sections
H = High Level, L = Low Level, X = Immaterial, Z = High Impedance (Off)

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3068

Functional Diagram



Absolute Maximum Ratings

Supply Voltage (VCC) ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 500ns Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 30% of VCC
Input High Voltage (VIH) ..... 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.7 (VCC), VIL = 0.3 (VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Select to Output	TPHL TPLH	VCC = 4.5V	9	+25°C	2	26	ns
			10, 11	+125°C, -55°C	2	31	ns
Data to Output	TPHL	VCC = 4.5V	9	+25°C	2	19	ns
			10, 11	+125°C, -55°C	2	22	ns
	TPLH	VCC = 4.5V	9	+25°C	2	21	ns
			10, 11	+125°C, -55°C	2	24	ns
Enable to Output	TPZH	VCC = 4.5V	9	+25°C	2	17	ns
			10, 11	+125°C, -55°C	2	20	ns
	TPZL	VCC = 4.5V	9	+25°C	2	15	ns
			10, 11	+125°C, -55°C	2	17	ns
Disable to Output	TPHZ	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	19	ns
	TPLZ	VCC = 4.5V	9	+25°C	2	16	ns
			10, 11	+125°C, -55°C	2	17	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	+25°C	Typical 30		pF
			+125°C	Typical 37		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	+25°C	-	10	pF
			+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	+25°C	-	12	ns
			+125°C, -55°C	-	18	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics..

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	3.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	5.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-5.0	-	mA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC	+25°C	-	±50	-	±100	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Select to Output	TPHL	VCC = 4.5V	+25°C	2	31	2	39	ns
	TPLH	VCC = 4.5V	+25°C	2	31	2	39	ns
Data to Output	TPHL	VCC = 4.5V	+25°C	2	22	2	28	ns
	TPLH	VCC = 4.5V	+25°C	2	24	2	30	ns
Enable to Output	TPZL	VCC = 4.5V	+25°C	2	17	2	22	ns
	TPZH	VCC = 4.5V	+25°C	2	20	2	25	ns
Disable to Output	TPHZ	VCC = 4.5V	+25°C	2	19	2	24	ns
	TPLZ	VCC = 4.5V	+25°C	2	17	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour
IOZL/IOZH	±200	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A inspection in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
7, 9	1 - 6, 8, 10 - 15	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
7, 9	8	-	1 - 6, 10 -16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	1, 8, 15	7, 9	16	3 - 6, 10 - 14	2

NOTES:

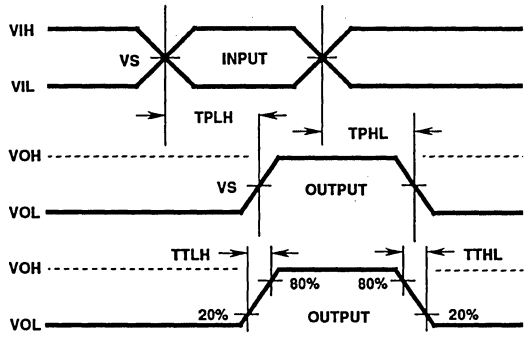
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680Ω ± 5% for dynamic burn-in

TABEL 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
7, 9	8	1 - 6, 10 - 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

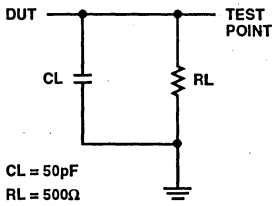
AC Timing Diagrams



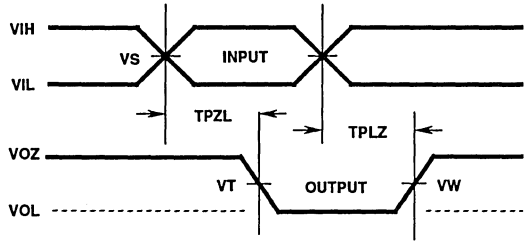
AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

AC Load Circuit



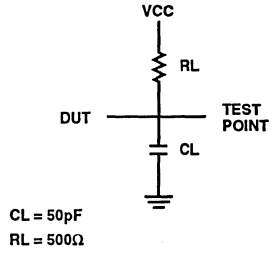
Tri-State Low Timing Diagrams



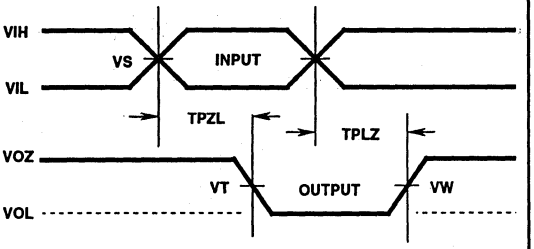
TRI-STATE LOW VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	0.90	V
GND	0	V

Tri-State Low Load Circuit



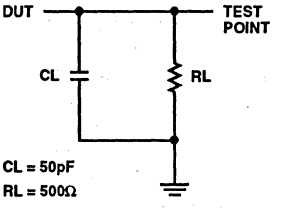
Tri-State High Timing Diagrams



TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	3.60	V
GND	0	V

Tri-State High Load Circuit



Die Characteristics

DIE DIMENSIONS:
84 x 84 mils

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

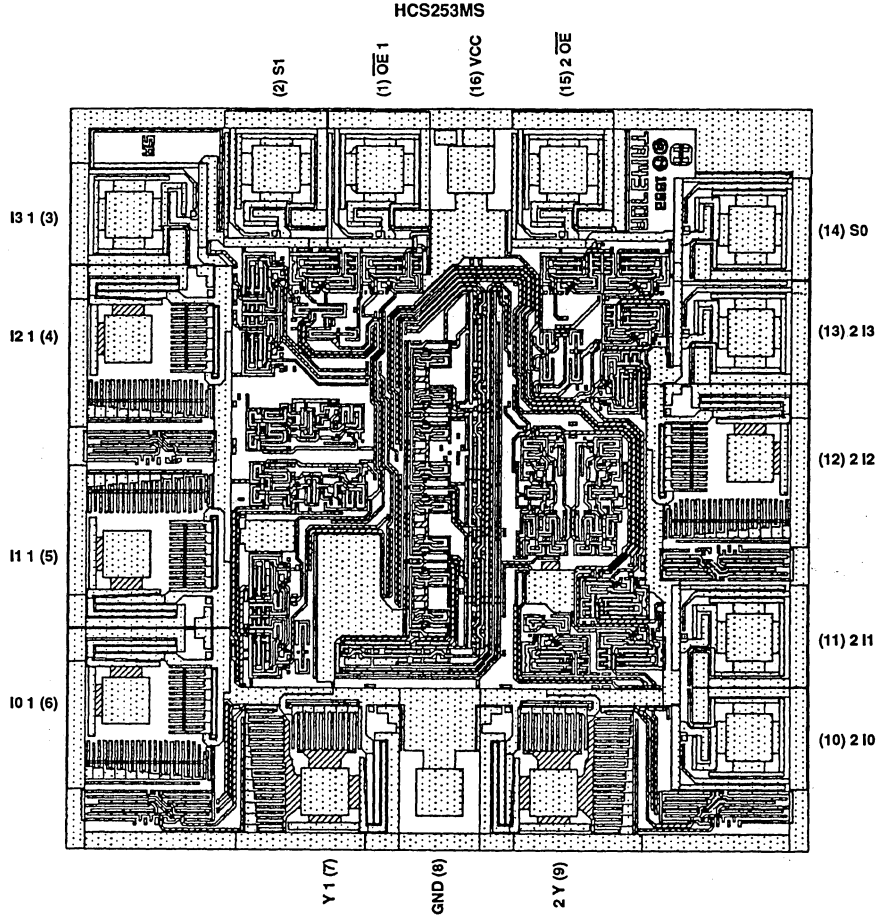
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HCS273MS

Radiation Hardened Octal D Flip-Flop

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity 2 x 10^{-9} Error/Bit Day (Typ)
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.3 VCC Max
  - VIH = 0.7 VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

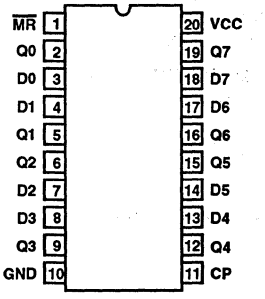
The Harris HCS273MS is a Radiation Hardened octal D flip-flop, positive edge triggered, with reset.

The HCS273MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

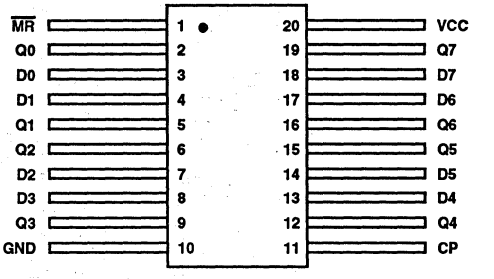
The HCS273MS is supplied in a 20 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

20 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T20, LEAD FINISH C
TOP VIEW



20 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F20, LEAD FINISH C
TOP VIEW



Truth Table

INPUTS			OUTPUT
RESET ($\overline{MR}$)	CLOCK CP	DATA Dn	Q
L	X	X	L
H	↗	H	H
H	↗	L	L
H	L	X	Q0

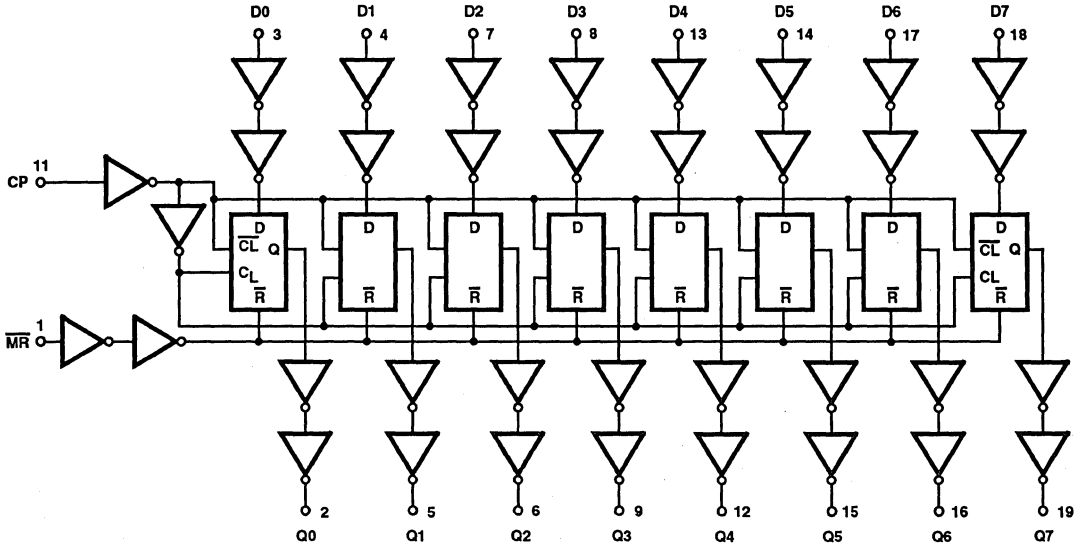
NOTE: Q0 = The level of Q established by the last low to high transition of the clock

H = High Level
L = Low Level
X = Immaterial
↗ = Transition from low to high

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2475.2**

Functional Diagram



Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 500ns Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 30% of VCC
Input High Voltage (VIH) . . . . . 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CP to Q	TPLH	VCC = 4.5V	9	+25°C	2	19	ns
			10, 11	+125°C, -55°C	2	22	ns
	TPHL	VCC = 4.5V	9	+25°C	2	23	ns
			10, 11	+125°C, -55°C	2	27	ns
$\overline{MR}$ to Q	TPHL	VCC = 4.5V	9	+25°C	2	25	ns
			10, 11	+125°C, -55°C	2	29	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical TBD		pF
			1	+125°C	Typical TBD		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns
Maximum Operating Frequency (CPU, CPD)	FMAX	VCC = 4.5V	1	+25°C		30	MHz
			1	+125°C		20	MHz
Setup Time Data to Clock	TSU	VCC = 4.5V	1	+25°C	12	-	ns
			1	+125°C	18	-	ns
Hold Time Data to Clock	TH	VCC = 4.5V	1	+25°C	3	-	ns
			1	+125°C	3	-	ns
Pulse Width $\overline{MR}$	TW	VCC = 4.5V	1	+25°C	16	-	ns
			1	+125°C	24	-	ns
Pulse Width Clock	TW	VCC = 4.5V	1	+25°C	16	-	ns
			1	+125°C	24	-	ns
Removal Time $\overline{MR}$ to Clock	TREM	VCC = 4.5V	1	+25°C	10	-	ns
			1	+125°C	15	-	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	3.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	5.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-5.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
CP to Q	TPLH	VCC = 4.5V	+25°C	2	22	2	28	ns
	TPHL	VCC = 4.5V	+25°C	2	27	2	34	ns
$\overline{MR}$ to Q	TPHL	VCC = 4.5V	+25°C	2	29	2	37	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: Alternate Group A testing in accordance with Method 5005 of Mil-Std-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE: Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC I BURN-IN (Note 1)					
2, 5, 6, 9, 12, 15, 16, 19	1, 3, 4, 7, 8, 10, 11, 13, 14, 17, 18	-	20	-	-
STATIC II BURN-IN (Note 1)					
2, 5, 6, 9, 12, 15, 16, 19	10	-	1, 3, 4, 7, 8, 11, 13, 14, 17, 18, 20	-	-
DYNAMIC BURN-IN (Note 2)					
-	10	2, 5, 6, 9, 12, 15, 16, 19	1, 20	11	3, 4, 7, 8, 13, 14, 17, 18

NOTES:

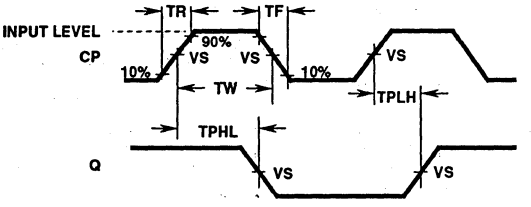
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

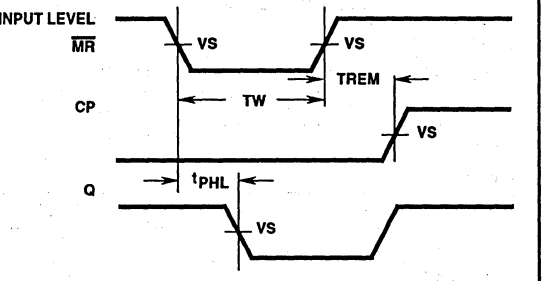
OPEN	GROUND	VCC = 5V ± 0.5V
2, 5, 6, 9, 12, 15, 16, 19	10	1, 3, 4, 7, 8, 11, 13, 14, 17, 18, 20

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

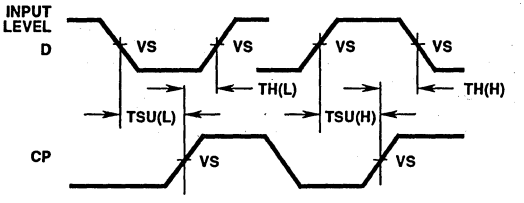
AC Timing Diagrams and Load Circuit



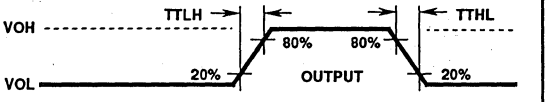
CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



MASTER RESET PULSE WIDTH. MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



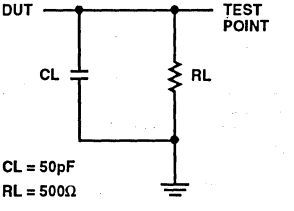
DATA SET-UP AND HOLD TIMES



OUTPUT TRANSITION TIME

AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V



Die Characteristics

DIE DIMENSIONS:
108 x 106 mils

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

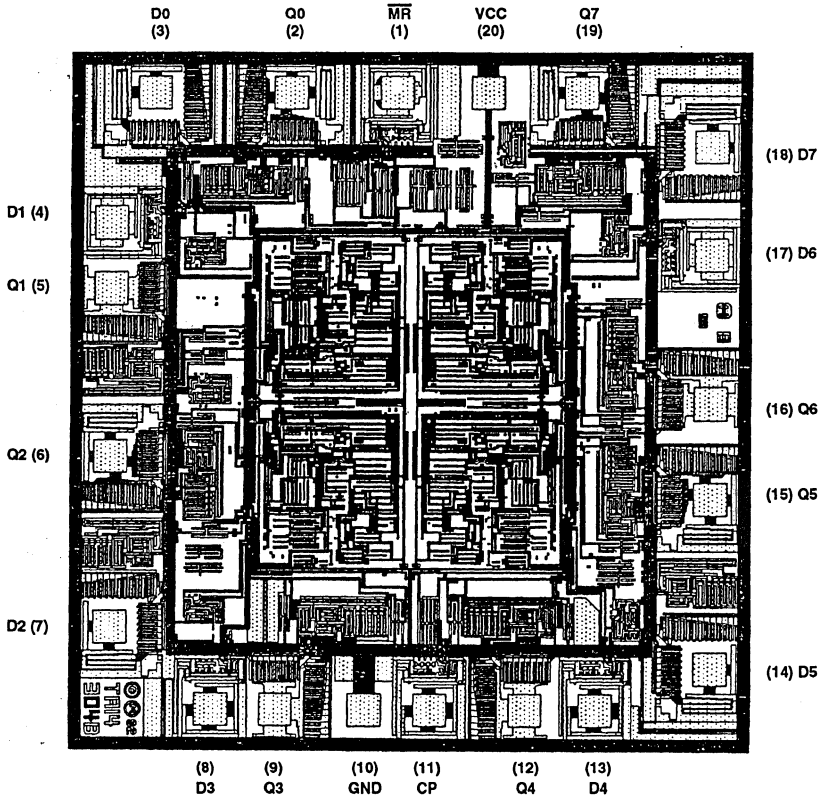
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCS273MS



HARRIS SEMICONDUCTOR

HCTS273MS

Radiation Hardened Octal D Flip-Flop

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s. 20ns Pulse
- Cosmic Ray Upset Rate 2 x 10^{-9} Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Bus Driver Outputs - 15 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

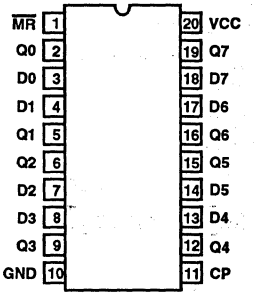
The Harris HCTS273MS is a Radiation Hardened octal D flip-flop, positive edge triggered, with reset.

The HCTS273MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

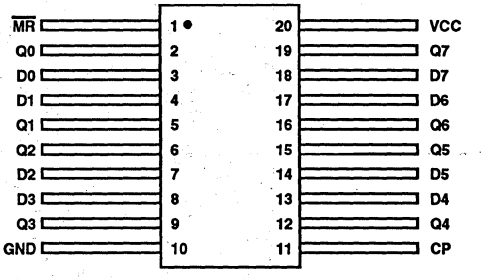
The HCTS273MS is supplied in a 20 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

20 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR, CDIP2-T20, LEAD FINISH C
TOP VIEW



20 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR, CDFP4-F20, LEAD FINISH C
TOP VIEW



Truth Table

INPUTS			OUTPUT
RESET ($\overline{MR}$)	CLOCK CP	DATA Dn	Q
L	X	X	L
H	⎍	H	H
H	⎍	L	L
H	L	X	Q0

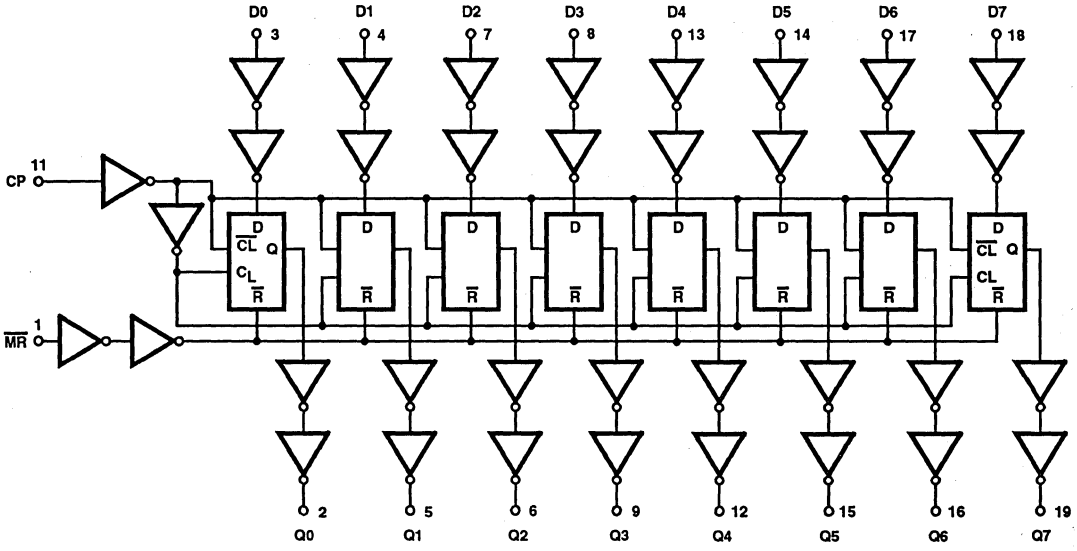
NOTE: Q0 = The level of Q established by the last low to high transition of the clock

H = High Level
L = Low Level
X = Immaterial
⎍ = Transition from low to high

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2274.1**

Functional Diagram



Absolute Maximum Ratings

Supply Voltage (VCC) ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC) ..... +4.5V to +5.5V
Input Rise and Fall Times at VCC = 4.5V (TR, TF) ..... 500ns Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-7.2	-	mA
			2, 3	+125°C, -55°C	-6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOH = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOL = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH =2.25V, VIL =0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CP to Q	TPLH	VCC = 4.5V	9	+25°C	2	19	ns
			10, 11	+125°C, -55°C	2	22	ns
	TPHL	VCC = 4.5V	9	+25°C	2	23	ns
			10, 11	+125°C, -55°C	2	27	ns
$\overline{MR}$ to Q	TPHL	VCC = 4.5V	9	+25°C	2	25	ns
			10, 11	+125°C, -55°C	2	29	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 40		pF
			1	+125°C	Typical 40		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C, -55°C	-	22	ns
Maximum Operating Frequency (CPU, CPD)	FMAX	VCC = 4.5V	1	+25°C		25	MHz
			1	+125°C, -55°C		16	MHz
Setup Time Data to Clock	TSU	VCC = 4.5V	1	+25°C	12	-	ns
			1	+125°C, -55°C	18	-	ns
Hold Time Data to Clock	TH	VCC = 4.5V	1	+25°C	3	-	ns
			1	+125°C, -55°C	3	-	ns
Pulse Width MRN	TW	VCC = 4.5V	1	+25°C	12	-	ns
			1	+125°C, -55°C	18	-	ns
Pulse Width Clock	TW	VCC = 4.5V	1	+25°C	20	-	ns
			1	+125°C, -55°C	30	-	ns
Removal Time $\overline{MR}$ to Clock	TREM	VCC = 4.5V	1	+25°C	10	-	ns
			1	+125°C, -55°C	15	-	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	3.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	5.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-5.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
CP to Q	TPLH	VCC = 4.5V	+25°C	2	22	2	28	ns
	TPHL	VCC = 4.5V	+25°C	2	27	2	34	ns
$\overline{MR}$ to Q	TPHL	VCC = 4.5V	+25°C	2	29	2	37	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
PDA	100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
PDA	100%/5004	1, 7, 9, Deltas	
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS					
2, 5, 6, 9, 12, 15, 16, 19	1, 3, 4, 7, 8, 10, 11, 13, 14, 17, 18	-	20	-	-
STATIC BURN-IN II TEST CONNECTIONS					
2, 5, 6, 9, 12, 15, 16, 19	10	-	1, 3, 4, 7, 8, 11, 13, 14, 17, 18, 20	-	-
DYNAMIC BURN-IN TEST CONNECTIONS					
-	10	2, 5, 6, 9, 12, 15, 16, 19	1, 20	11	3, 4, 7, 8, 13, 14, 17, 18

NOTES:

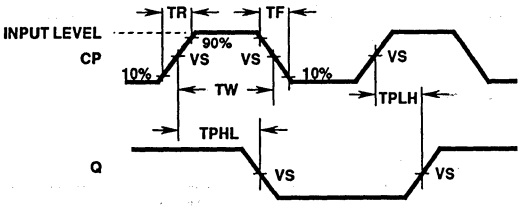
1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680kΩ ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

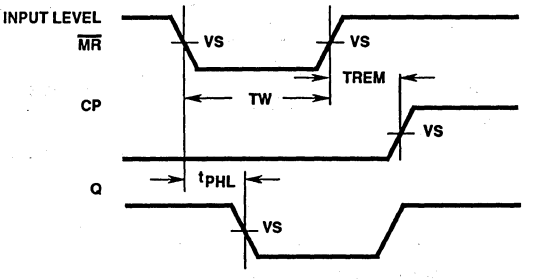
OPEN	GROUND	VCC = 5V ± 0.5V
2, 5, 6, 9, 12, 15, 16, 19	10	1, 3, 4, 7, 8 11, 13, 14, 17, 18, 20

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

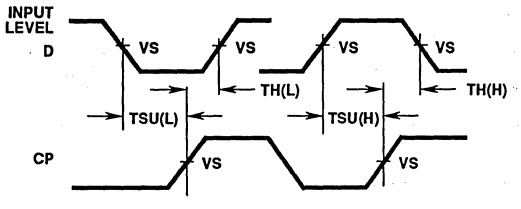
AC Timing Diagrams and Load Circuit



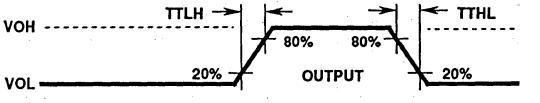
CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



MASTER RESET PULSE WIDTH. MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



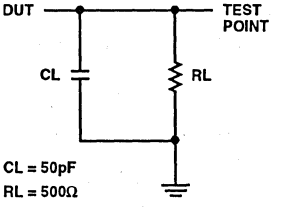
DATA SET-UP AND HOLD TIMES



OUTPUT TRANSITION TIME

AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V



Die Characteristics

DIE DIMENSIONS:
108 x 106 mils

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

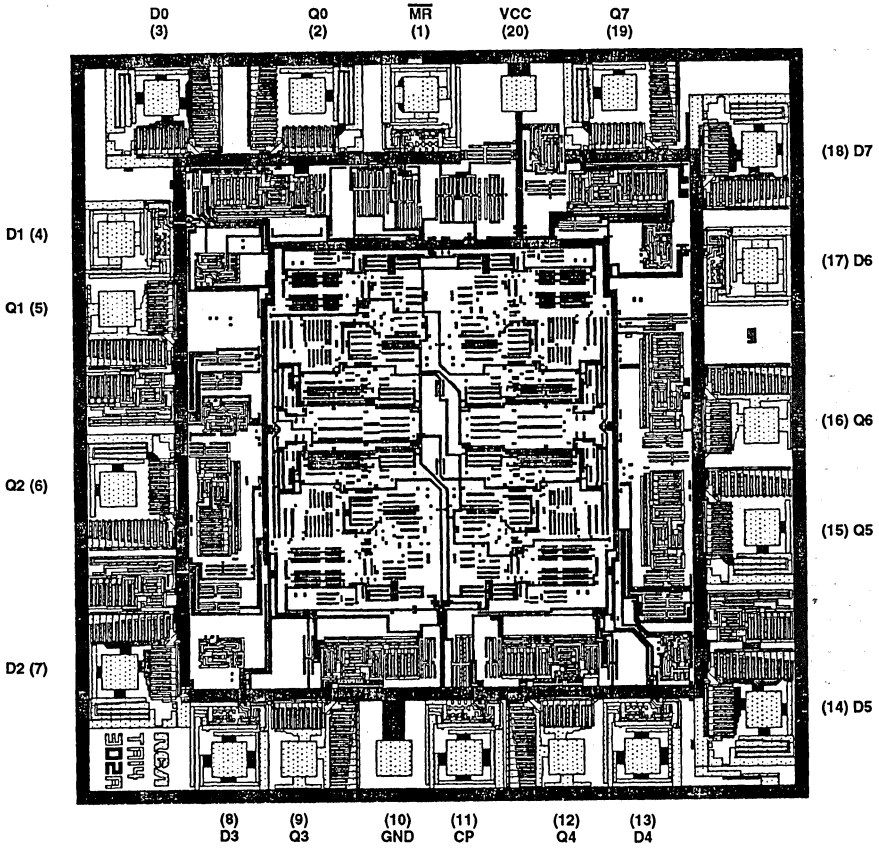
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCTS273MS



HARRIS SEMICONDUCTOR

HCTS283MS

Radiation Hardened 4 Bit Binary Full Adder with Fast Carry

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD (Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range ..... -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range .....4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2V Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

The Harris HCTS283MS is a Radiation Hardened 4 bit binary full adder with fast carry that adds two 4 bit binary numbers and generates a carry-out bit if the sum exceeds 15.

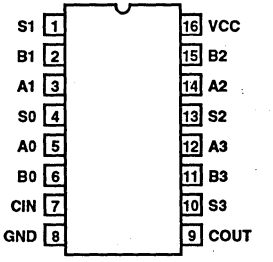
This device can be used in positive or negative logic. When using positive logic the carry-in input must be tied low, if there is no carry-in.

The HCTS283MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family .

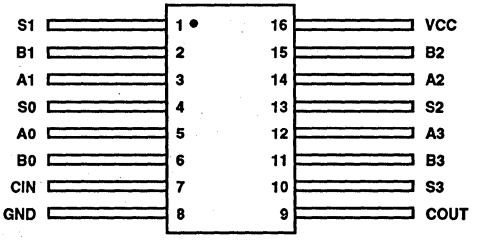
The HCTS283MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

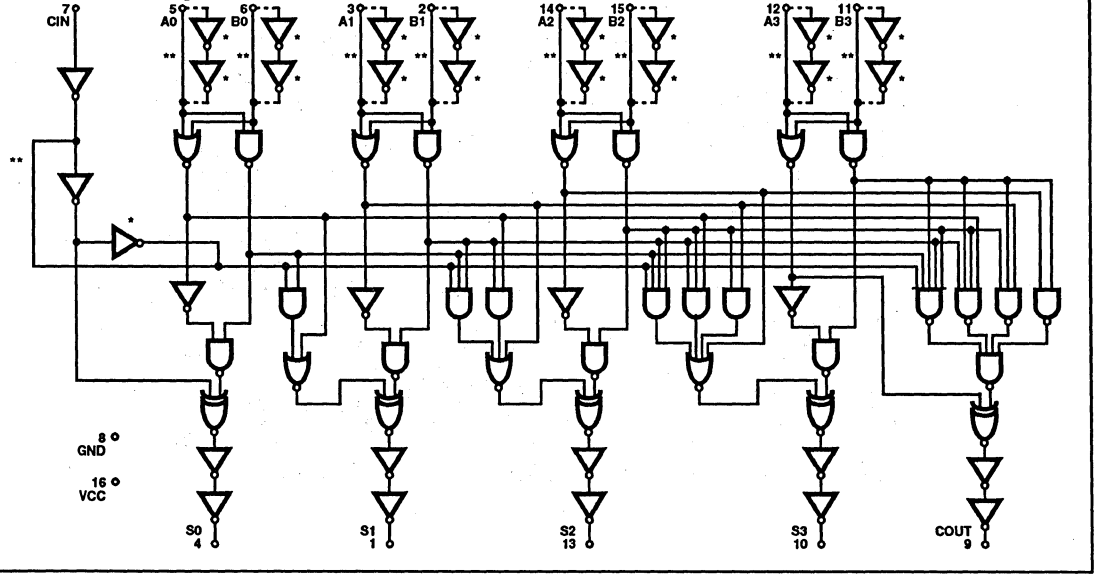
16 PIN CERAMIC DUAL-IN-LINE
CASE OUTLINE D-2, CONFIGURATION 3, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
CASE OUTLINE F5-A, CONFIGURATION 2, LEAD FINISH C
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3381

Absolute Maximum Ratings

Supply Voltage . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input. . . . . ±10mA
DC Drain Current, Any One Output. . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T = -55°C to +100°C 1W
For T = +100°C to +125°C. . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 10ns/V Max
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . 2.0V to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Delta ICC	DICC	VCC = 5.5V, VIN = VCC or GND, 1 Input at 2.4V	1	+25°C	-	1.6	mA
			2, 3	+125°C, -55°C	-	3.2	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V (Note 2)	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V (Note 2)	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.80V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.80V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	0.5	µA
			2, 3	+125°C, -55°C	-5.0	5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.80V (Note 3)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. Force/Measure functions may be interchanged.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay CIN to S0	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	23	ns
			10, 11	+125°C, -55°C	2	27	ns
	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	26	ns
			10, 11	+125°C, -55°C	2	30	ns
Propagation Delay CIN to S1	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	31	ns
	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	30	ns
			10, 11	+125°C, -55°C	2	35	ns
Propagation Delay CIN to S2 CIN to COUT	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	31	ns
			10, 11	+125°C, -55°C	2	37	ns
	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	34	ns
			10, 11	+125°C, -55°C	2	40	ns
Propagation Delay CIN to S3	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	38	ns
			10, 11	+125°C, -55°C	2	47	ns
	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	40	ns
			10, 11	+125°C, -55°C	2	48	ns
Propagation Delay An, Bn to COUT	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	53	ns
			10, 11	+125°C, -55°C	2	67	ns
	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	54	ns
			10, 11	+125°C, -55°C	2	63	ns
Propagation Delay An, Bn to Sn	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	50	ns
			10, 11	+125°C, -55°C	2	63	ns
	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	60	ns
			10, 11	+125°C, -55°C	2	73	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VCC = 5V, VIH = 5V, VIL = 0V, F = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL, TTLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	1	+25°C	-	15	ns
			1	+125°C, -55°C	-	22	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Delta ICC	DICC	VCC = 5.5V, VIN = VCC or GND, 1 Input at 2.4V	+25°C	-	3.2	-	3.2	mA
Output Current (Sink)	IOL	VCC = 4.5V, VOUT = 0.4V, VIL = 0V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VOUT = VCC -0.4V VIL = 0V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, VIL = 0.80V, VIL = 0.30V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, VIL = 0.80V, VIL = 0.30 at 1 M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, VIL = 0.80V, VIL = 0.30V at 1M RAD, IOL = 50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, VIL = 0.80V, VIL = 0.30 at 1 M RAD, IOL = 50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.80V , VIL = 0.30V at 1M RAD (Note 2)	+25°C	-	-	-	-	-
Propgation Delay CIN to S0	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	27	2	34	ns
	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	30	2	38	ns
Propagation Delay CIN to S1	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	31	2	39	ns
	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	35	2	44	ns
Propagation Delay CIN to S2, CIN to COUT	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	37	2	46	ns
	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	40	2	50	ns
Propagation Delay CIN to S3	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	47	2	59	ns
	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	48	2	60	ns
Propagation Delay An, Bn to COUT	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	67	2	84	ns
	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	63	2	79	ns
Propagation Delay An, Bn to Sn	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	63	2	79	ns
	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	73	2	91	ns

NOTES:

1. All voltages referenced to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternate Group A, in accordance with Method 5005 of MIL-STD-883, may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE: 1. Except FN Test which will be performed 100% Go/No-Go.

TABLE 8. STATIC BURN-IN AND DYNAMIC

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
1, 4, 9, 10, 13	2, 3, 5, 6, 7, 8, 11, 12, 14, 15	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
1, 4, 9, 10, 13	8	-	2, 3, 5, 6, 7, 11, 12, 14, 15, 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	8	1, 4, 9, 10, 13	16	2, 6, 11, 15	3, 5, 7, 12, 14

NOTES:

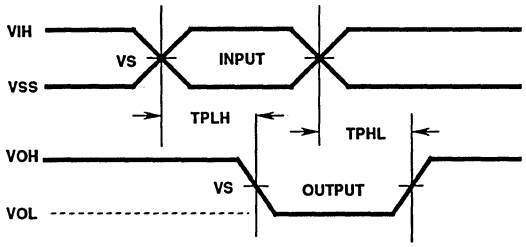
1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in

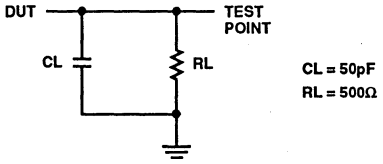
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
1, 4, 9, 10, 13	8	2, 3, 5, 6, 7, 11, 12, 14, 15, 16

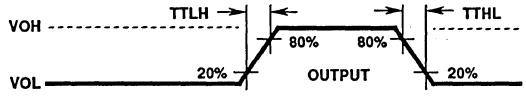
NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

Propagation Delay Timing Diagram and Load Circuit





Transition Timing Diagram



AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	3.00	V
VIL	0.0	V
VS	1.30	V
GND	0.0	V

Die Characteristics

DIE DIMENSIONS:
78 x 86 mils
2.21mm x 2.19mm

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

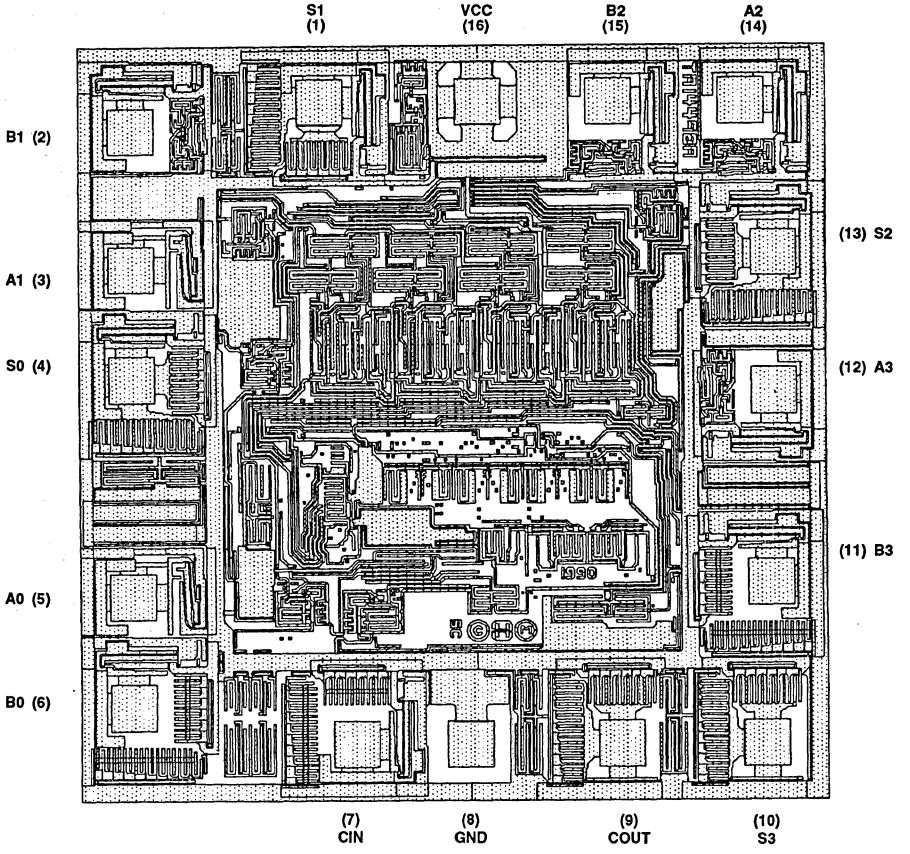
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCTS283MS



HARRIS SEMICONDUCTOR

HCTS299MS

Radiation Hardened 8-Bit Universal Shift Register; Tri-State

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD (Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Rate 2 x 10^{-9} Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Bus Driver Outputs ..... 15 LSTTL Loads
- Military Temperature Range ..... -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range ..... 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels II ≤ 5μA at VOL, VOH

Description

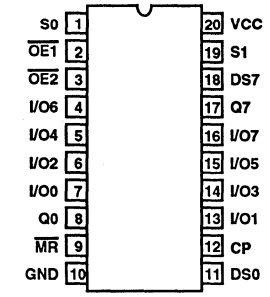
The Harris HCTS299MS is a Radiation Hardened 8-bit shift/storage register with tri-state bus interface capability. The register has four synchronous operating modes controlled by the two select inputs (S0, S1). The mode select, the serial data (DS0, DS7) and the parallel data (IO0 - IO7) respond only to the low to high transition of the clock (CP) pulse. S0, S1 and the data inputs must be one set up time period prior to the clocks positive transition. The master reset ($\overline{MR}$) is an asynchronous active low input.

The HCTS299MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family with TTL input compatibility.

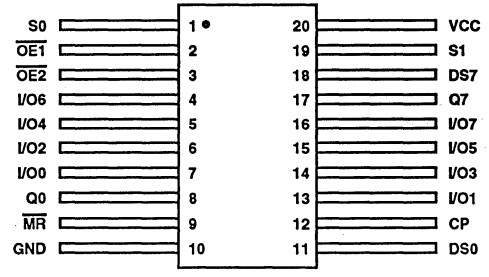
The HCTS299MS is supplied in a 20 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

20 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T20, LEAD FINISH C
TOP VIEW



20 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F20, LEAD FINISH C
TOP VIEW



7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3069

Truth Tables

Register Operating Modes

FUNCTION	INPUTS							REGISTER OUTPUTS				
	$\overline{MR}$	CP	S0	S1	DS0	DS7	I/On	Q0	Q1	...	Q6	Q7
Reset (Clear)	L	X	X	X	X	X	X	L	L	...	L	L
Shift Right	H	↗	h	l	l	X	X	L	q0	...	q5	q6
	H	↗	h	l	h	X	X	H	q0	...	q5	Q6
Shift Left	H	↗	l	h	X	l	X	q1	q2	...	q7	L
	H	↗	l	h	X	h	X	q1	q2	...	q7	H
Hold (Do Nothing)	H	↗	l	l	X	X	X	q0	q1	...	q6	q7
Parallel Load	H	↗	h	h	X	X	l	L	L	...	L	L
	H	↗	h	h	X	X	h	H	H	...	H	H

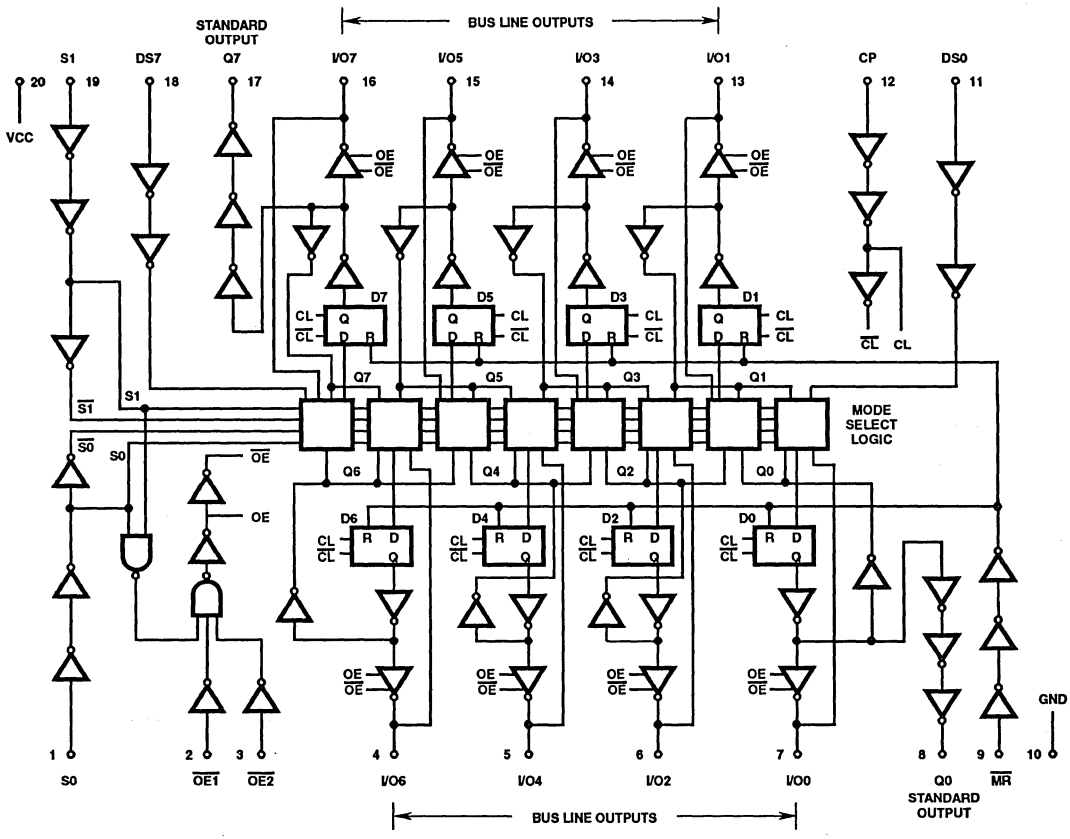
Tri-State I/O Port Operating Mode

FUNCTION	INPUTS					INPUTS/OUTPUTS
	$\overline{OE1}$	$\overline{OE2}$	S0	S1	Qn (REGISTER)	I/O0 . . . I/O7
Read Register	L	L	L	X	L	L
	L	L	L	X	H	H
	L	L	X	L	L	L
	L	L	X	L	H	H
Load Register	X	X	H	H	Qn = I/On	I/On = Inputs
Disable I/O	H	X	X	X	X	Z
	X	H	X	X	X	Z

H = HighVoltage Level
L = Low Voltage Level
X = Immaterial
Z = Output in High Impedance State
h = Input Voltage High One Setup Time Prior Clock Transition
l = Input voltage Low One Setup Time Prior Clock Transition
↗ = Low-to-High Clock Transition

qn = Lower Case Letter Indicates the State of the Referenced Output One Setup Time Prior Clock Transition

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage (VCC) ..... -0.5 to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) ..... +4.5V to +5.5V
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 500ns Max
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V	1	+25°C	-7.2	-	mA
			2, 3	+125°C, -55°C	-6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC	1	+25°C	-1	+1	µA
			2, 3	+125°C, -55°C	-50	+50	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CLK to I/On	TPHL, TPLH	VCC = 4.5V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	32	ns
CLK to Q0, Q7	TPHL, TPLH	VCC = 4.5V	9	+25°C	2	30	ns
			10, 11	+125°C, -55°C	2	34	ns
$\overline{MR}$ to Output	TPHL	VCC = 4.5V	9	+25°C	2	32	ns
			10, 11	+125°C, -55°C	2	36	ns
$\overline{OEn}$ to Output	TPZH	VCC = 4.5V	9	+25°C	2	23	ns
			10, 11	+125°C, -55°C	2	25	ns
	TPHZ		9	+25°C	2	25	ns
			10, 11	+125°C, -55°C	2	27	ns
	TPZL		9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	30	ns
	TPLZ		9	+25°C	2	30	ns
			10, 11	+125°C, -55°C	2	34	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 98		pF
			1	+125°C	Typical 114		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL, TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C, -55°C	-	22	ns
Max Operating Frequency	FMAX	VCC = 4.5V	1	+25°C	-	25	MHz
			1	+125°C, -55°C	-	16	MHz
Setup Time DS0, DS7, I/On to CLK	TSU	VCC = 4.5V	1	+25°C	20	-	ns
			1	+125°C, -55°C	30	-	ns
Setup Time S1, S0 to CLK	TSU	VCC = 4.5V	1	+25°C	27	-	ns
			1	+125°C, -55°C	41	-	ns
Hold Time DS0, DS7, I/On, S0, S1 to CLK	TH	VCC = 4.5V	1	+25°C	0	-	ns
			1	+125°C, -55°C	0	-	ns
Recovery Time $\overline{MR}$ to CLK	TREC	VCC = 4.5V	1	+25°C	5	-	ns
			1	+125°C, -55°C	5	-	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Pulse Width $\overline{MR}$	TW ($\overline{MR}$)	VCC = 4.5V	1	+25°C	15	-	ns
			1	+125°C, -55°C	22	-	ns
Pulse Width CLK	TW (CLK)	VCC = 4.5V	1	+25°C	20	-	ns
			1	+125°C, -55°C	30	-	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	5.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-5.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	µA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC	+25°C	-	±50	-	±100	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
CLK to I/On	TPHL, TPLH	VCC = 4.5V	+25°C	2	32	2	40	ns
CLK to Q0, Q7	TPHL, TPLH	VCC = 4.5V	+25°C	2	34	2	43	ns
$\overline{MR}$ to Output	TPHL	VCC = 4.5V	+25°C	2	36	2	45	ns
$\overline{OEn}$ to Output	TPZH	VCC = 4.5V	+25°C	2	25	2	32	ns
	TPHZ			2	27	2	33	ns
	TPZL	VCC = 4.5V	+25°C	2	30	2	43	ns
	TPLZ			2	34	2	43	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour
IOZL/IOZH	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternate Group A Inspection in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE: 1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC BURN-IN AND DYNAMIC

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
8, 17	1 - 7, 9 - 16, 18, 19	-	20	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
8, 17	10	-	1 - 7, 9, 11 - 16, 18 - 20	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	2, 3, 10, 18, 19	4 - 8, 13 - 17	1, 9, 20	12	11

NOTES:

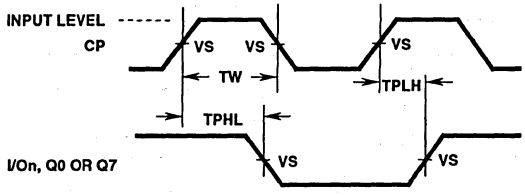
1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680Ω ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

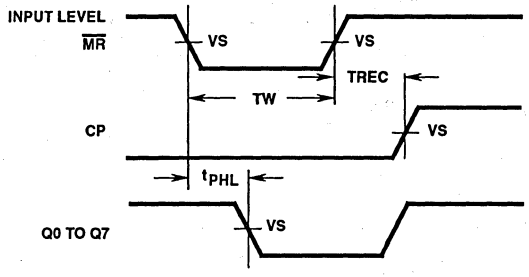
OPEN	GROUND	VCC = 5V ± 0.5V
8, 17	10	1 - 7, 9, 11 - 16, 18 - 20

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

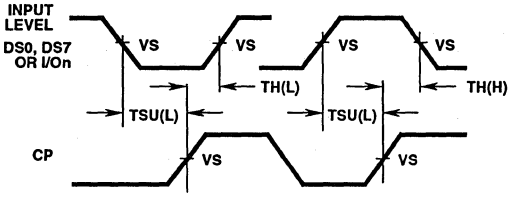
AC Timing Diagrams and Load Circuit



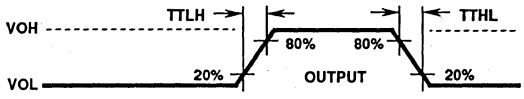
CLOCK PRE-REQUISITE AND PROPAGATION DELAYS



MASTER RESET PRE-REQUISITE AND PROPAGATION DELAYS



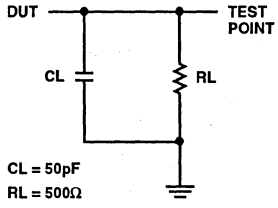
DATA PRE-REQUISITE TIMES



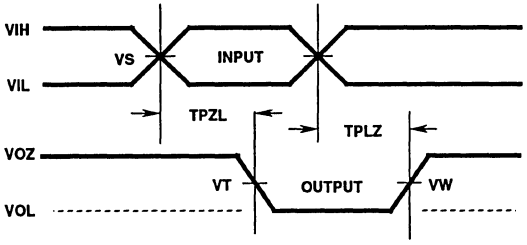
OUTPUT TRANSITION TIME

AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V



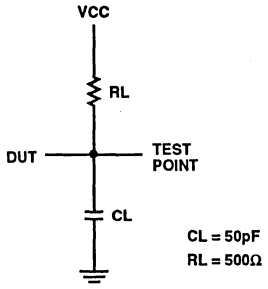
Tri-State Low Timing Diagrams



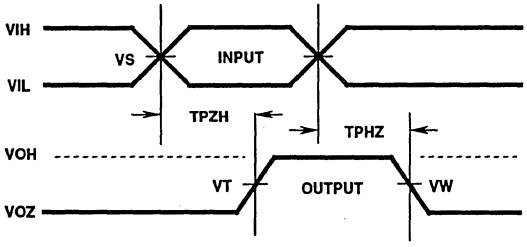
TRI-STATE LOW VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	0.90	V
VIL	0	V
GND	0	V

Tri-State Low Load Circuit



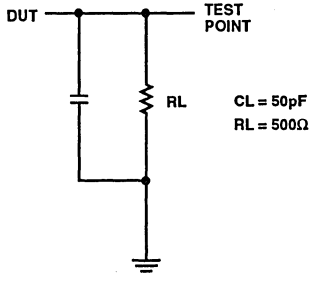
Tri-State High Timing Diagrams



TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	3.60	V
VIL	0	V
GND	0	V

Tri-State High Load Circuit



Die Characteristics

DIE DIMENSIONS:
123 x 94 mils

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

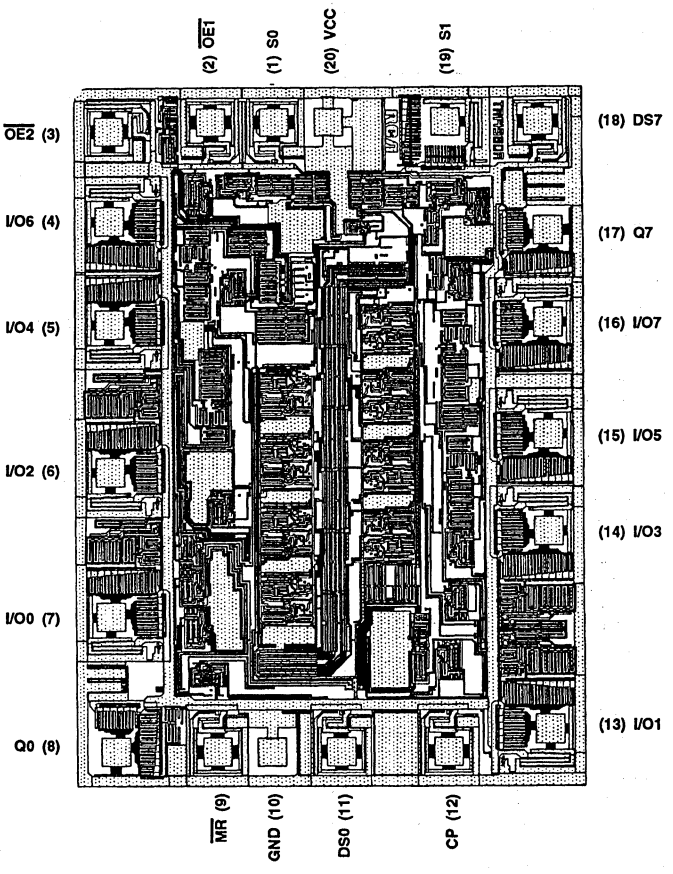
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS299MS



HARRIS SEMICONDUCTOR

HCTS365MS

Radiation Hardened Hex Buffer/Line Driver Non-Inverting

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Bus Driver Outputs ..... 15 LSTTL Loads
- Military Temperature Range ..... -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range ..... 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels II ≤ 5μA @ VOL, VOH

Description

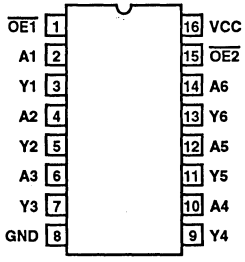
The Harris HCTS365MS is a Radiation Hardened non-inverting hex buffer and line driver with Tri-state outputs. The output enables ($\overline{OE1}$ and $\overline{OE2}$) control the tri-state outputs. If either $\overline{OE1}$ or $\overline{OE2}$ is high the outputs will be in a High impedance state. For Data, $\overline{OE1}$ and $\overline{OE2}$ must be Low.

The HCTS365MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family with TTL input compatibility.

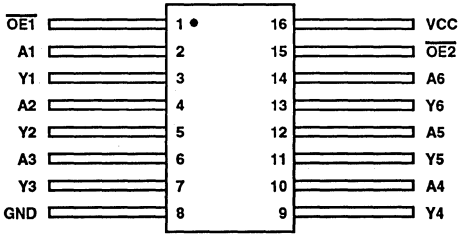
The HCTS365MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T16, LEAD FINISH C
TOP VIEW



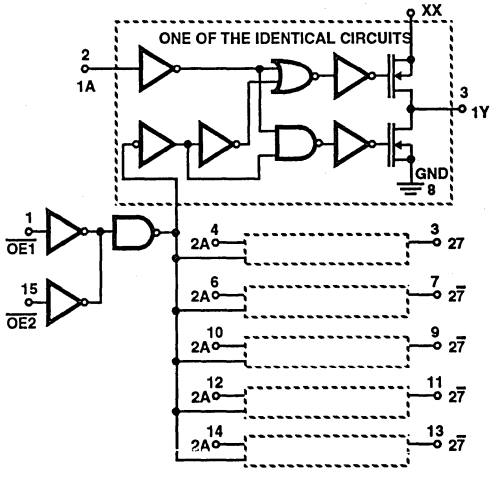
16 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F16, LEAD FINISH C
TOP VIEW



Truth Table

INPUTS			OUTPUTS
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

Functional Diagram



7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3070

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V (TR, TF) . . . . . 500ns Max.
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V	1	+25°C	-7.2	-	mA
			2, 3	+125°C, -55°C	-6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH =2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Tri-State Output Leakage Current	IOZ	VCC = 4.5V or 5.5V, Applied Voltage = 0V or VCC	1	+25°C	-1	+1	µA
			2, 3	+125°C, -55°C	-50	+50	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Data to Output	TPLH	VCC = 4.5V	9	+25°C	2	19	ns
			10, 11	+125°C, -55°C	2	23	ns
	TPHL	VCC = 4.5V	9	+25°C	2	19	ns
			10, 11	+125°C, -55°C	2	23	ns
Enable to Output	TPZL	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	33	ns
	TPZH	VCC = 4.5V	9	+25°C	2	22	ns
			10, 11	+125°C, -55°C	2	26	ns
Disable to Output	TPLZ	VCC = 4.5V	9	+25°C	2	24	ns
			10, 11	+125°C, -55°C	2	27	ns
	TPHZ	VCC = 4.5V	9	+25°C	2	22	ns
			10, 11	+125°C, -55°C	2	25	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 27		pF
			1	+125°C	Typical 35		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	12	12	ns
			1	+125°C, -55°C	18	18	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K LIMITS RAD MIN	200K LIMITS RAD MAX	1M LIMITS RAD MIN	1M LIMITS RAD MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	3.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	5.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-5.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K LIMITS RAD		1M LIMITS RAD		UNITS
				MIN	MAX	MIN	MAX	
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	±5	-5	±5	µA
Tri-State Output Leakage Current	IOZ	VCC = 4.5V or 5.5V Applied Voltage = 0V or VCC	+25°C	-50	+50	-100	+100	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Data to Output	TPLH	VCC = 4.5V	+25°C	2	23	2	29	ns
	TPHL	VCC = 4.5V	+25°C	2	23	2	29	ns
Enable to Output	TPZL	VCC = 4.5V	+25°C	2	33	2	42	ns
	TPZH	VCC = 4.5V	+25°C	2	26	2	33	ns
Disable to Output	TPLZ	VCC = 4.5V	+25°C	2	27	2	34	ns
	TPHZ	VCC = 4.5V	+25°C	2	25	2	32	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour
IOZL/IOZH	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC BURN-IN AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
4, 7, 9, 12	1 - 3, 5, 6, 8, 10, 11, 13 - 15	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
4, 7, 9, 12	8	-	1 - 3, 5, 6, 10, 11, 13 - 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	8, 15	4, 7, 9, 12	16	2, 3, 5, 6, 10, 11, 13, 14	1

NOTES:

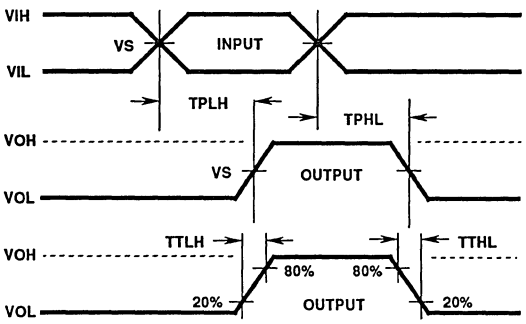
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 680Ω ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 5, 7, 9, 11, 13	8	1, 2, 4, 6, 10, 12, 14 - 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

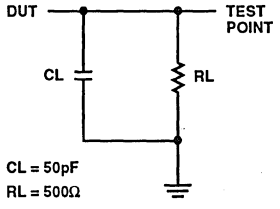
AC Timing Diagrams



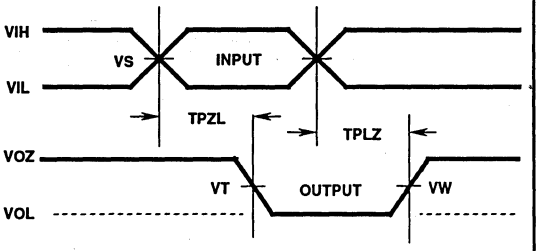
AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



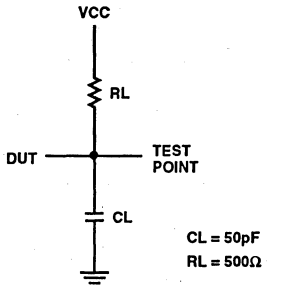
Tri-State Low Timing Diagrams



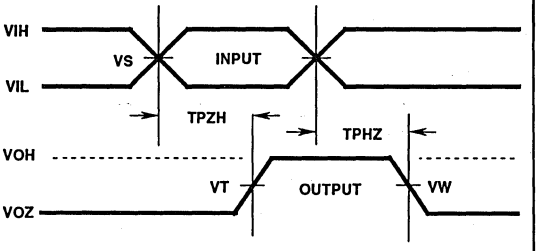
TRI-STATE LOW VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	0.90	V
GND	0	V

Tri-State Low Load Circuit



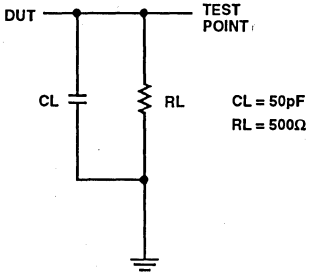
Tri-State High Timing Diagrams



TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	3.60	V
GND	0	V

Tri-State High Load Circuit



Die Characteristics

DIE DIMENSIONS:
108 x 106 mils

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

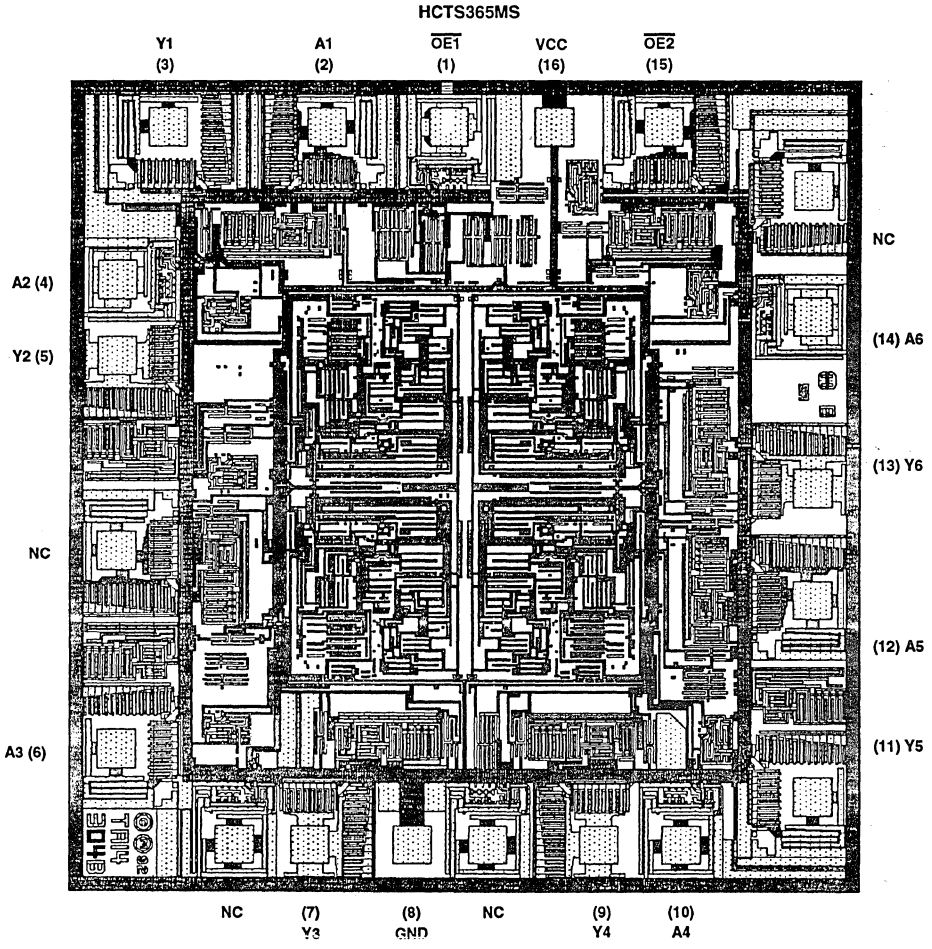
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HCS373MS

Radiation Hardened Octal Transparent Latch, Tri-State

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD (Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity 2 x 10^{-9} Error/Bit-Day (Typ)
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.3 VCC Max
  - VIH = 0.7 VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

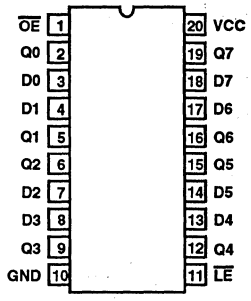
The Harris HCS373MS is a Radiation Hardened octal transparent tri-state latch with an active low output enable. The HCS373MS utilizes advanced CMOS/SOS technology. The outputs are transparent to the inputs when the Latch Enable ($\overline{LE}$) is HIGH. When the Latch Enable ($\overline{LE}$) goes LOW, the data is latched. The Output Enable ($\overline{OE}$) controls the tri-state outputs. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high impedance state. The latch operation is independent of the state of the Output Enable.

The HCS373MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

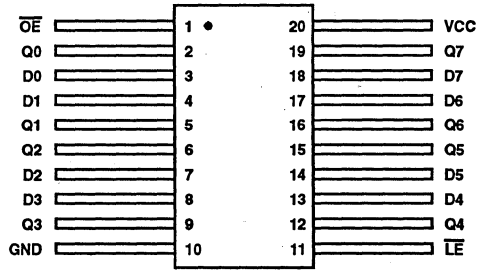
The HCS373MS is supplied in a 20 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

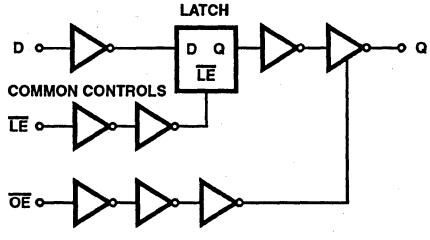
20 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T20, LEAD FINISH C
TOP VIEW



20 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F20, LEAD FINISH C
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2135.1**

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 100ns Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 30% of VCC
Input High Voltage (VIH) . . . . . 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Output Tri State Leakage	IOZ	VCC = 5.5V, VO = 0V or VCC	1	+25°C	-	±1.0	µA
			2, 3	+125°C, -55°C		±50	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Data to Qn	TPLH TPHL	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	24	ns
$\overline{LE}$ to Qn	TPLH TPHL	VCC = 4.5V	9	+25°C	2	24	ns
			10, 11	+125°C, -55°C	2	29	ns
Enable to Output	TPZL	VCC = 4.5V	9	+25°C	2	25	ns
			10, 11	+125°C, -55°C	2	31	ns
	TPZH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	24	ns
Disable to Output	TPLZ TPHZ	VCC = 4.5V	9	+25°C	2	25	ns
			10, 11	+125°C, -55°C	2	30	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	+25°C	Typical 38		pF
			+125°C	Typical 38		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	+25°C	-	10	pF
			+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	+25°C	-	12	ns
			+125°C	-	18	ns
Setup Time Data to $\overline{LE}$	TSU	VCC = 4.5V	+25°C	10	-	ns
			+125°C	15	-	ns
Hold Time Data to $\overline{LE}$	TH	VCC = 4.5V	+25°C	5	-	ns
			+125°C	5	-	ns
Pulse Width $\overline{LE}$	TW	VCC = 4.5V	+25°C	16	-	ns
			+125°C	24	-	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	3.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	5.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-5.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RADd, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC	+25°C	-	±50	-	±100	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD	+25°C	-	-	-	-	-
Data to Qn	TPHL, TPLH	VCC = 4.5V	+25°C	2	24	2	29	ns
LEN to Qn	TPHL, TPLH	VCC = 4.5V	+25°C	2	29	2	37	ns
Enable to Output	TPZL	VCC = 4.5V	+25°C	2	31	2	39	ns
	TPZH	VCC = 4.5V	+25°C	2	24	2	30	ns
Disable to Output	TPLZ, TPHZ	VCC = 4.5V	+25°C	2	30	2	38	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour
IOZL/IOZH	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE: Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC BURN-IN AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
2, 5, 6, 9, 12, 15, 16, 19	1, 3, 4, 7, 8, 10, 11, 13, 14, 17, 18	-	20	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
2, 5, 6, 9, 12, 15, 16, 19	10	-	1 , 3, 4, 7, 8, 11, 13, 14, 17, 18, 20	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	10	2, 5, 6, 9, 12, 15, 16, 19	1, 20	11	3, 4, 7, 8, 13, 14, 17, 18

NOTES:

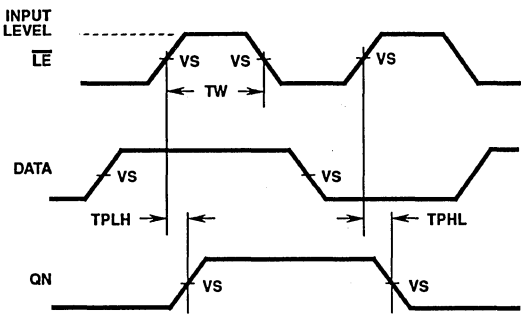
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 680Ω ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

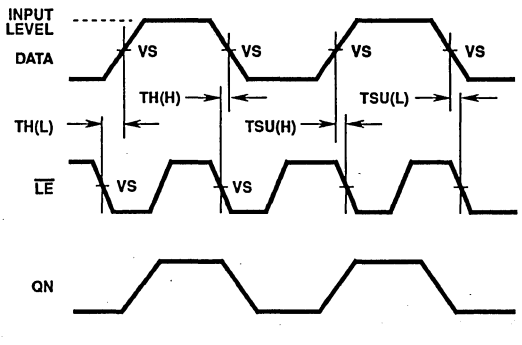
OPEN	GROUND	VCC = 5V ± 0.5V
2, 5, 6, 9, 12, 15, 16, 19	10	1, 3, 4, 7, 8, 11, 13, 14, 17, 18, 20

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

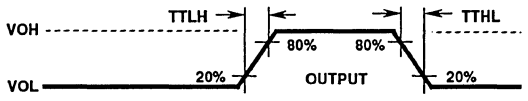
AC Timing Diagrams and Load Circuit



LATCH ENABLE PROPAGATION DELAYS



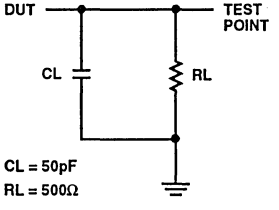
LATCH ENABLE PREREQUISITE TIMES



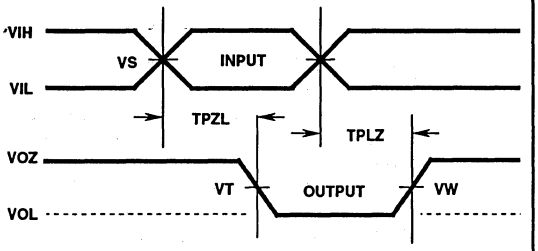
DATA SET-UP AND HOLD TIMES

AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V



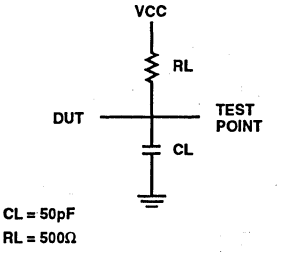
Tri-State Low Timing Diagrams



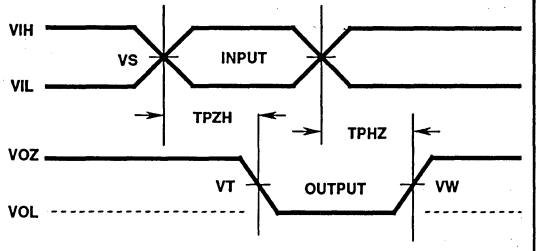
TRI-STATE LOW VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	0.90	V
GND	0	V

Tri-State Low Load Circuit



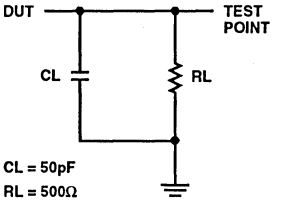
Tri-State High Timing Diagrams



TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	3.60	V
GND	0	V

Tri-State High Load Circuit



Die Characteristics

DIE DIMENSIONS:
2747 x 2693µm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

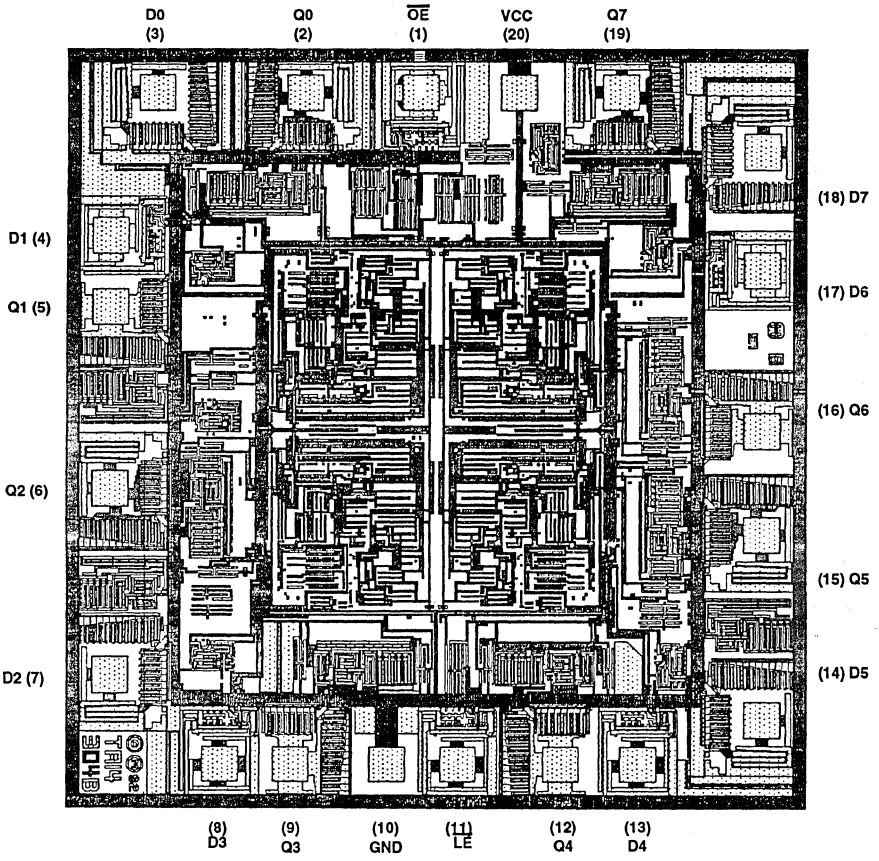
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCS373MS



HARRIS SEMICONDUCTOR

HCTS373MS

Radiation Hardened Octal Transparent Latch, Tri-State

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD)Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity 2 x 10^{-9} Errors/Bit-Day
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Bus Driver Outputs - 15 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

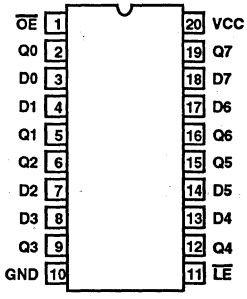
The Harris HCTS373MS is a Radiation Hardened octal transparent tri-state latch with an active-low output enable. The outputs are transparent to the inputs when the Latch Enable ($\overline{LE}$) is HIGH. When the Latch Enable ($\overline{LE}$) goes LOW, the data is latched. The Output Enable ($\overline{OE}$) controls the tri-state outputs. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high impedance state. The latch operation is independent of the state of the Output Enable.

The HCTS373MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

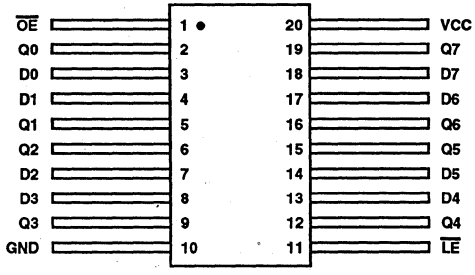
The HCTS373MS is supplied in a 20 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

20 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR, CDIP2-T20, LEAD FINISH C
TOP VIEW



20 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR, CDFP4-F20, LEAD FINISH C
TOP VIEW

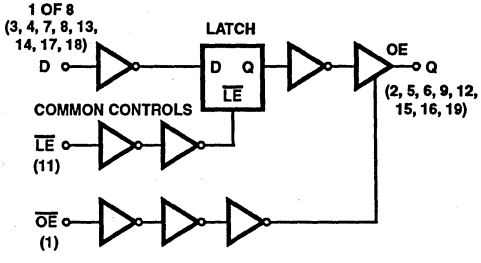


Truth Table

$\overline{OE}$	$\overline{LE}$	D	Q
L	H	H	H
L	H	L	L
L	L	l	L
L	L	h	H
H	X	X	Z

H = High Level, L = Low Level, h = High voltage level prior to the high-to-low latch enable transition
X = Immaterial, Z = High Impedance
l = Low voltage level prior to the high-to-low latch enable transition

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2131.1**

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Input Rise and Fall Times at VCC = 4.5V (TR, TF) . . . . . 500ns Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V	1	+25°C	-7.2	-	mA
			2, 3	+125°C, -55°C	-6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Output Tri State Leakage	IOZ	VCC = 5.5V, VO = 0V or VCC	1	+25°C	-	±1.0	µA
			2, 3	+125°C, -55°C		±50	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Data to Qn	TPLH	VCC = 4.5V	9	+25°C	2	19	ns
			10, 11	+125°C, -55°C	2	24	ns
	TPHL	VCC = 4.5V	9	+25°C	2	26	ns
			10, 11	+125°C, -55°C	2	30	ns
$\overline{LE}$ to Qn	TPLH	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	30	ns
	TPHL	VCC = 4.5V	9	+25°C	2	30	ns
			10, 11	+125°C, -55°C	2	34	ns
Enable to Output	TPZL	VCC = 4.5V	9	+25°C	2	32	ns
			10, 11	+125°C, -55°C	2	36	ns
	TPZH	VCC = 4.5V	9	+25°C	2	26	ns
			10, 11	+125°C, -55°C	2	29	ns
Disable to Output	TPLZ, TPHZ	VCC = 4.5V	9	+25°C	2	22	ns
			10, 11	+125°C, -55°C	2	25	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 38		pF
			1	+125°C, -55°C	Typical 38		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C, -55°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	12	ns
			1	+125°C, -55°C	-	18	ns
Setup Time Data to $\overline{LE}$	TSU	VCC = 4.5V	1	+25°C	13	-	ns
			1	+125°C, -55°C	20	-	ns
Hold Time Data to $\overline{LE}$	TH	VCC = 4.5V	1	+25°C	10	-	ns
			1	+125°C, -55°C	15	-	ns
Pulse Width $\overline{LE}$	TW	VCC = 4.5V	1	+25°C	16	-	ns
			1	+125°C, -55°C	24	-	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	3.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	5.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-5.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	μA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC	+25°C	-50	+50	-100	+100	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Data to Qn	TPLH	VCC = 4.5V	+25°C	2	24	2	30	ns
	TPHL	VCC = 4.5V	+25°C	2	30	2	38	ns
$\overline{LE}$ to Qn	TPLH	VCC = 4.5V	+25°C	2	30	2	38	ns
	TPHL	VCC = 4.5V	+25°C	2	34	2	43	ns
Enable to Output	TPZL	VCC = 4.5V	+25°C	2	36	2	45	ns
	TPZH	VCC = 4.5V	+25°C	2	29	2	37	ns
Disable to Output	TPLZ, TPHZ	VCC = 4.5V	+25°C	2	25	2	32	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour
IOZL/IOZH	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
2, 5, 6, 9, 12, 15, 16, 19	1, 3, 4, 7, 8, 10, 11, 13, 14, 17, 18	-	20	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
2, 5, 6, 9, 12, 15, 16, 19	10	-	1, 3, 4, 7, 8, 11, 13, 14, 17, 18, 20	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	1, 10	2, 5, 6, 9, 12, 15, 16, 19	20	11	3, 4, 7, 8, 13, 14, 17, 18

NOTES:

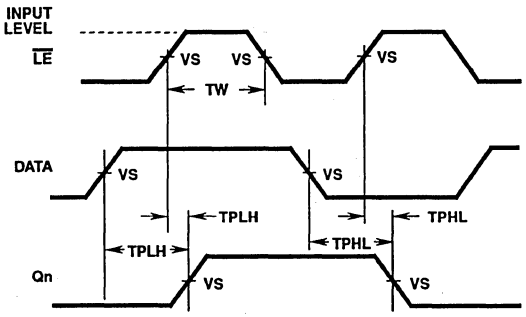
1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680kΩ ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

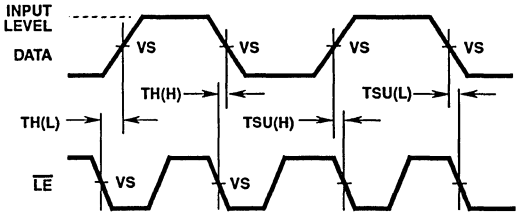
OPEN	GROUND	VCC = 5V ± 0.5V
2, 5, 6, 9, 12, 15, 16, 19	10	1, 3, 4, 7, 8, 11, 13, 14, 17, 18, 20

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

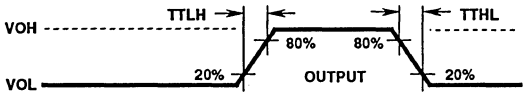
AC Timing Diagrams and Load Circuit



DATA AND LATCH ENABLE PROPAGATION DELAYS



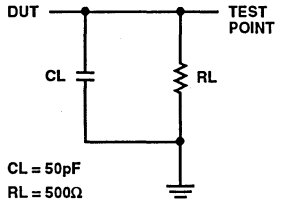
LATCH ENABLE PREREQUISITE TIMES



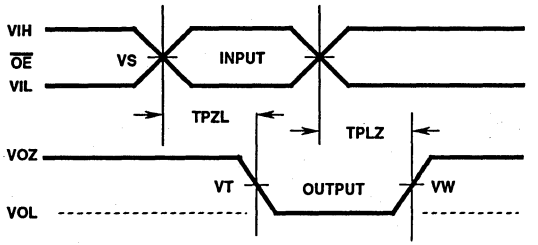
DATA SET-UP AND HOLD TIMES

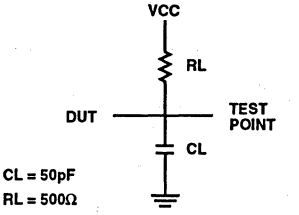
AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V



Tri-State Low Timing Diagram and Load Circuit

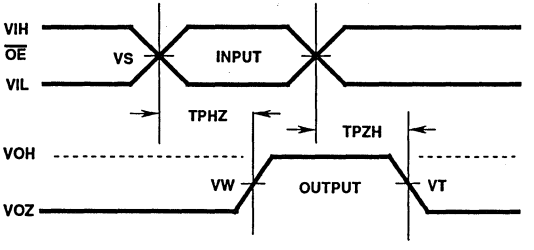


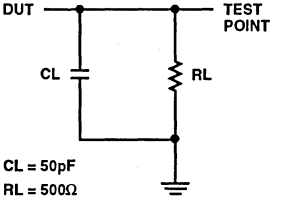


TRI-STATE LOW VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	0.90	V
VIL	0	V
GND	0	V

Tri-State High Timing Diagram and Load Circuit





TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	3.60	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
108 x 106 mils

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

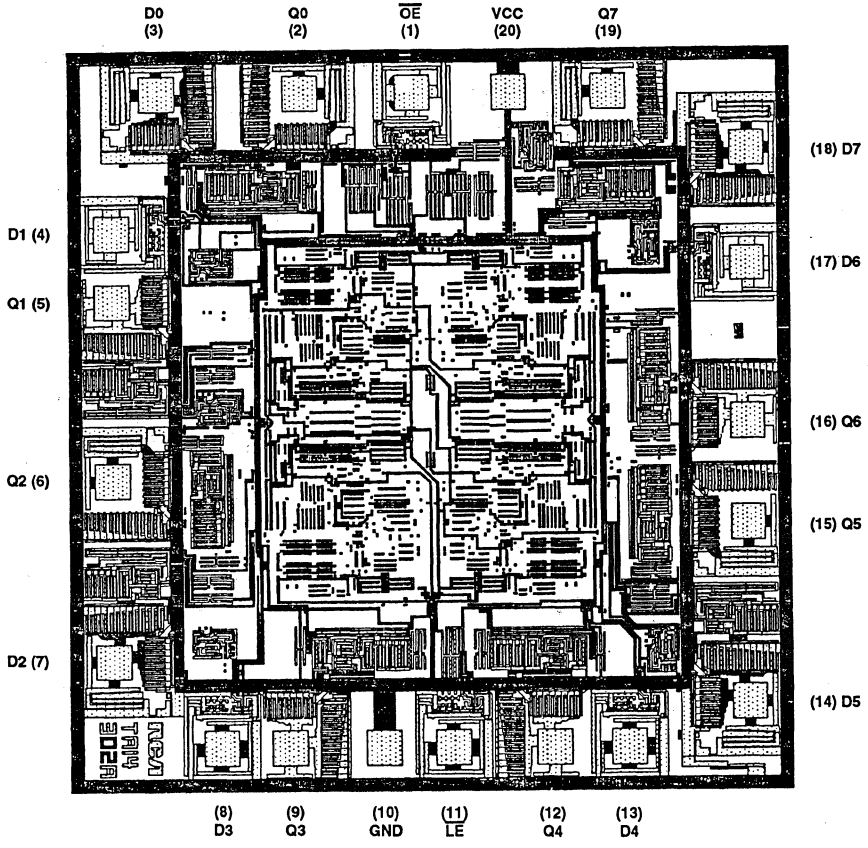
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCTS373MS



HARRIS SEMICONDUCTOR

HCS374MS

Radiation Hardened Octal D-Type Flip-Flop, Tri-State, Positive Edge Triggered

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity 2 x 10^{-9} Error/Bit Day (Typ)
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Bus Driver Outputs - 15 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.3 VCC Max
  - VIH = 0.7 VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

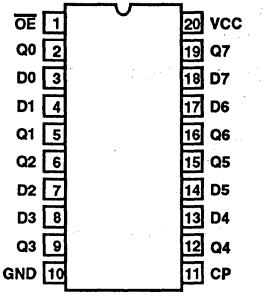
The Harris HCS374MS is a Radiation Hardened non-inverting octal D-type, positive edge triggered flip-flop with tri-stateable outputs. The HCS374MS utilizes advanced CMOS/SOS technology. The eight flip-flops enter data into their registers on the LOW-to-HIGH transition of the clock (CP). Data is also transferred to the outputs during this transition. The output enable ($\overline{OE}$) controls the tri-state outputs and is independent of the register operation. When the output enable is high, the outputs are in the high impedance state.

The HCS374MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

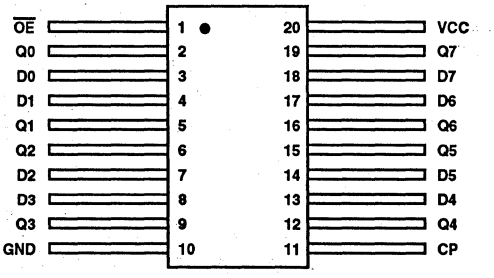
The HCS374MS is supplied in a 20 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

20 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T20, LEAD FINISH C
TOP VIEW



20 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F20, LEAD FINISH C
TOP VIEW

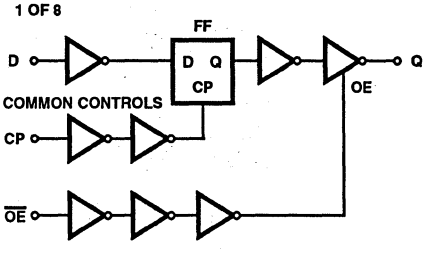


Truth Table

INPUTS			OUTPUTS
$\overline{OE}$	CP	Dn	Qn
L	↗	H	H
L	↗	L	L
L	X	X	Q0
H	X	X	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance
↗ = Transition from Low to High Level
Q0 = the level of Q before the indicated input conditions were established

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2470.1**

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 500ns Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 30% of VCC
Input High Voltage (VIH) . . . . . 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC, VCC = 4.5V and 5.5V.	1	+25°C	-	±1	µA
			2, 3	+125°C, -55°C	-	±50	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltages reference to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Clock to Q	TPLH TPHL	VCC = 4.5V	9	+25°C	2	22	ns
			10, 11	+125°C, -55°C	2	26	ns
Enable to Ouptput	TPZL TPZH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	23	ns
Disable to Output	TPLZ	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	23	ns
	TPHZ	VCC = 4.5V	9	+25°C	2	18	ns
			10, 11	+125°C, -55°C	2	20	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 7		pF
			1	+125°C	Typical 23		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	12	ns
			1	+125°C, -55°C	-	18	ns
Max Operating Frequencyt	FMAX	VCC = 4.5V	1	+25°C	-	30	MHz
			1	+125°C, -55°C	-	20	MHz
Setup Time Data to Clock	TSU	VCC = 4.5V	1	+25°C	12	-	ns
			1	+125°C, -55°C	18	-	ns
Hold Time Data to Clock	TH	VCC = 4.5V	1	+25°C	5	-	ns
			1	+125°C, -55°C	5	-	ns
Pulse Width Clocks	TW	VCC = 4.5V	1	+25°C	16	-	ns
			1	+125°C, -55°C	24	-	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	5.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-5.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V or 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V or 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC, VCC = 4.5V and 5.5V	+25°C	-	±50	-	±100	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Clock to Q	TPLH TPHL	VCC = 4.5V	+25°C	2	26	2	33	ns
Enable to Output	TPZL TPZH	VCC = 4.5V	+25°C	2	23	2	29	ns
Disable to Output	TPLZ	VCC = 4.5V	+25°C	2	23	2	28	ns
	TPHZ	VCC = 4.5V	+25°C	2	20	2	25	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.4V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour
IOZL/IOZH	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: Alternate Group A testing in accordance with Method 5005 of Mil-Std-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE: Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC I BURN-IN (Note 1)					
2, 5, 6, 9, 12, 15, 16, 19	1, 3, 4, 7, 8, 10, 11, 13, 14, 17, 18	-	20	-	-
STATIC II BURN-IN (Note 1)					
2, 5, 6, 9, 12, 15, 16, 19	10	-	1, 3, 4, 7, 8, 11, 13, 14, 17, 18, 20	-	-
DYNAMIC BURN-IN (Note 2)					
-	10	2, 5, 6, 9, 12, 15, 16, 19	1, 20	11	3, 4, 7, 8, 13, 14, 17, 18

NOTES:

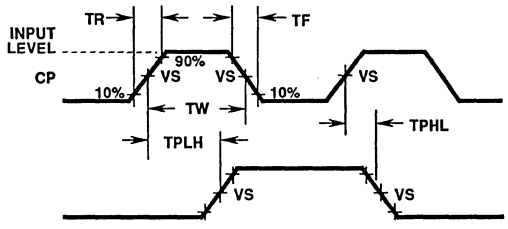
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 680Ω ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

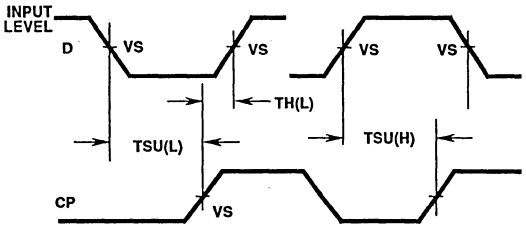
OPEN	GROUND	VCC = 5V ± 0.5V
2, 5, 6, 9, 12, 15, 16, 19	10	1, 3, 4, 7, 8 11, 13, 14, 17, 18, 20

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

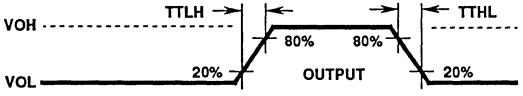
AC Timing Diagrams and Load Circuit



CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



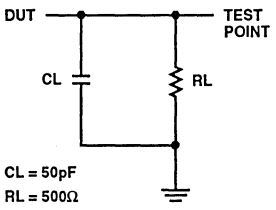
DATA SET-UP AND HOLD TIMES



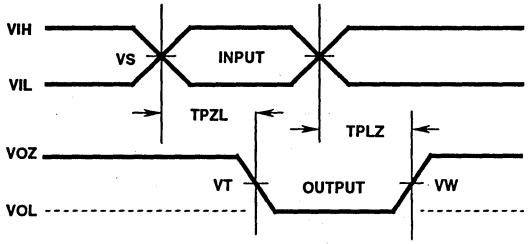
OUTPUT TRANSITION TIME

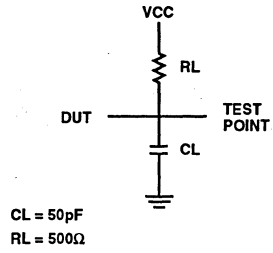
AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V



Tri-State Low Timing Diagrams and Load Circuit



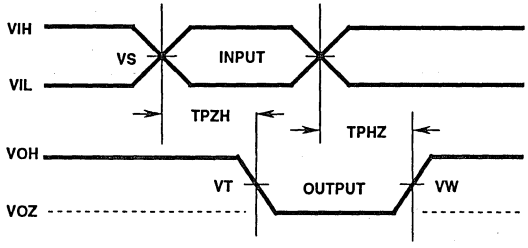


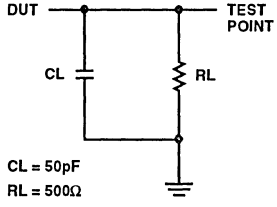
CL = 50pF
RL = 500Ω

TRI-STATE LOW VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	0.90	V
GND	0	V

Tri-State High Timing Diagrams and Load Circuit





CL = 50pF
RL = 500Ω

TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	3.60	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
108 x 106 mils

METALLIZATION:
Type: Al/Sil
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

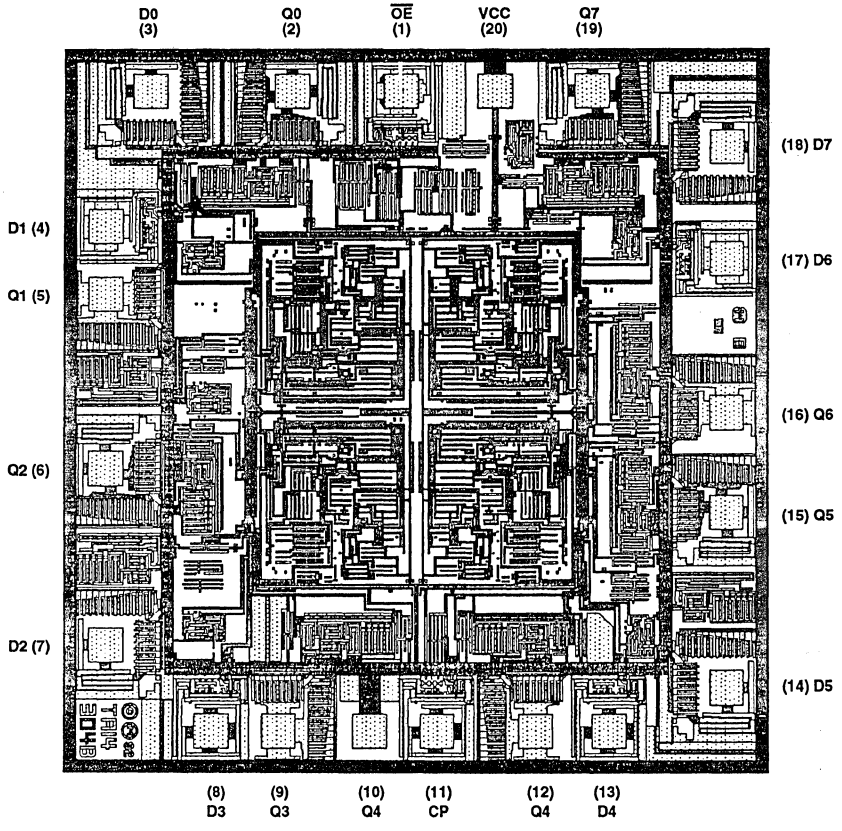
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCS374MS



HARRIS SEMICONDUCTOR

HCTS374MS

Radiation Hardened Octal D-Type Flip-Flop, Tri-State, Positive Edge Triggered

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity 2 x 10^{-9} Error/Bit-Day
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Bus Driver Outputs - 15 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

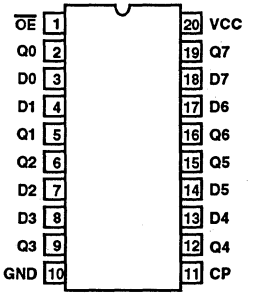
The Harris HCTS374MS is a Radiation Hardened non-inverting octal D-type, positive edge triggered flip-flop with tri-stateable outputs. The eight flip-flops enter data into their registers on the LOW-to-HIGH transition of the clock (CP). Data is also transferred to the outputs during this transition. The output enable ($\overline{OE}$) controls the tri-state outputs and is independent of the register operation. When the output enable is high, the outputs are in the high impedance state.

The HCTS374MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

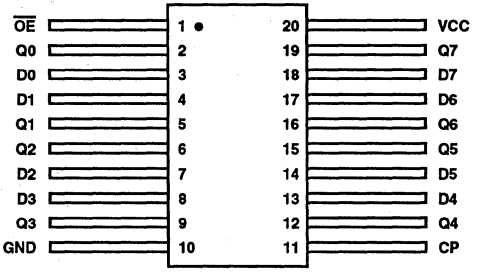
The HCTS374MS is supplied in a 20 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

20 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T20, LEAD FINISH C
TOP VIEW



20 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F20, LEAD FINISH C
TOP VIEW

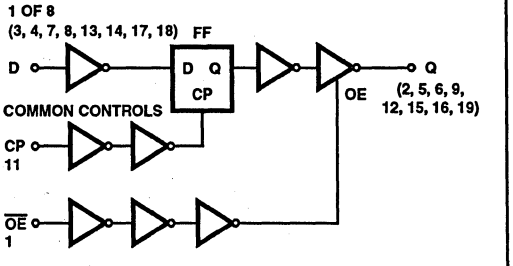


Truth Table

INPUTS			OUTPUTS
$\overline{OE}$	CP	Dn	Qn
L	↑	H	H
L	↑	L	L
L	L	X	Q0
H	X	X	Z

H = High Level (Steady State)
L = Low Level (Steady State)
X = Immaterial
Z = High Impedance
↑ = Transition from Low to High Level
Q0 = The level of Q before the indicated input conditions were established

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2134.1**

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 500ns Max.
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC	1	+25°C	-1	+1	µA
			2, 3	+125°C, -55°C	-50	+50	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Clock to Q	TPLH	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	31	ns
	TPHL	VCC = 4.5V	9	+25°C	2	31	ns
			10, 11	+125°C, -55°C	2	35	ns
Enable to Output	TPZL	VCC = 4.5V	9	+25°C	2	32	ns
			10, 11	+125°C, -55°C	2	36	ns
	TPZH	VCC = 4.5V	9	+25°C	2	26	ns
			10, 11	+125°C, -55°C	2	29	ns
Disable to Output	TPLZ, TPHZ	VCC = 4.5V	9	+25°C	2	22	ns
			10, 11	+125°C, -55°C	2	25	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 40		pF
			1	+125°C	Typical 40		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	12	ns
			1	+125°C, -55°C	-	18	ns
Max Operating Frequency	FMAX	VCC = 4.5V	1	+25°C	-	30	MHz
			1	+125°C, -55°C	-	20	MHz
Setup Time Data to Clock	TSU	VCC = 4.5V	1	+25°C	12	-	ns
			1	+125°C, -55°C	18	-	ns
Hold Time Data to Clock	TH	VCC = 4.5V	1	+25°C	5	-	ns
			1	+125°C, -55°C	5	-	ns
Pulse Width Clock	TW	VCC = 4.5V	1	+25°C	16	-	ns
			1	+125°C, -55°C	24	-	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	3.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	5.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-5.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	µA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC	+25°C	-50	+50	-100	+100	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Clock to Q	TPLH	VCC = 4.5V	+25°C	2	31	2	39	ns
	TPHL	VCC = 4.5V	+25°C	2	35	2	44	ns
Enable to Output	TPZL	VCC = 4.5V	+25°C	2	36	2	45	
	TPZH	VCC = 4.5V	+25°C	2	29	2	37	ns
Disable to Output	TPLZ, TPHZ	VCC = 4.5V	+25°C	2	25	2	32	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour
IOZL/IOZH	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC BURN-IN AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
2, 5, 6, 9, 12, 15, 16, 19	1, 3, 4, 7, 8, 10, 11, 13, 14, 17, 18	-	20	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
2, 5, 6, 9, 12, 15, 16, 19	10	-	1, 3, 4, 7, 8, 11, 13, 14, 17, 18, 20	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	10	2, 5, 6, 9, 12, 15, 16, 19	1, 20	11	3, 4, 7, 8, 13, 14, 17, 18

NOTES:

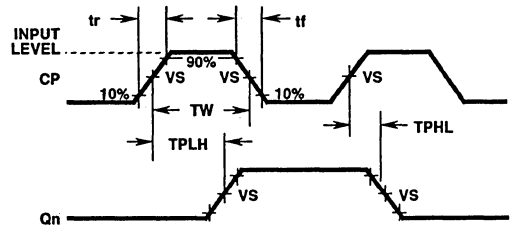
1. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in.
2. Each pin except VCC and GND will have a resistor of 680Ω ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

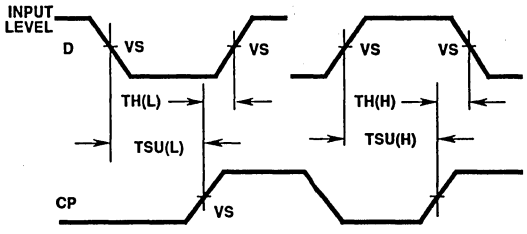
OPEN	GROUND	VCC = 5V ± 0.5V
2, 5, 6, 9, 12, 15, 16, 19	10	1, 3, 4, 7, 8, 11, 13, 14, 17, 18, 20

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

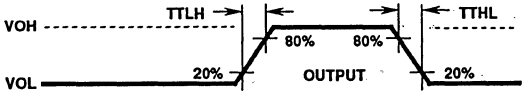
AC Timing Diagrams and Load Circuit



CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



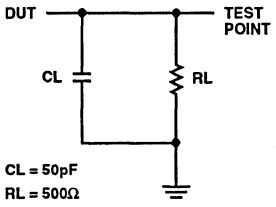
DATA SET-UP AND HOLD TIMES



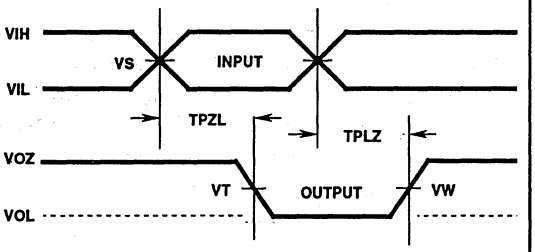
OUTPUT TRANSITION TIME

AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V



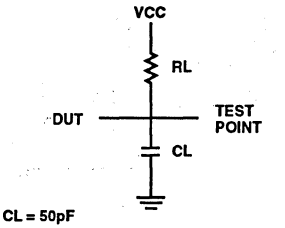
Tri-State Low Timing Diagrams



TRI-STATE LOW VOLTAGE LEVELS

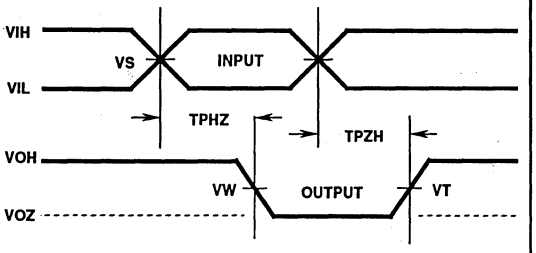
PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	0.90	V
VIL	0	V
GND	0	V

Tri-State Low Load Circuit



CL = 50pF
RL = 500Ω

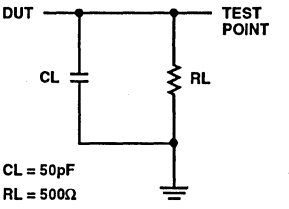
Tri-State High Timing Diagrams



TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	3.60	V
VIL	0	V
GND	0	V

Tri-State High Load Circuit



CL = 50pF
RL = 500Ω

Die Characteristics

DIE DIMENSIONS:
108 x 106 mils

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

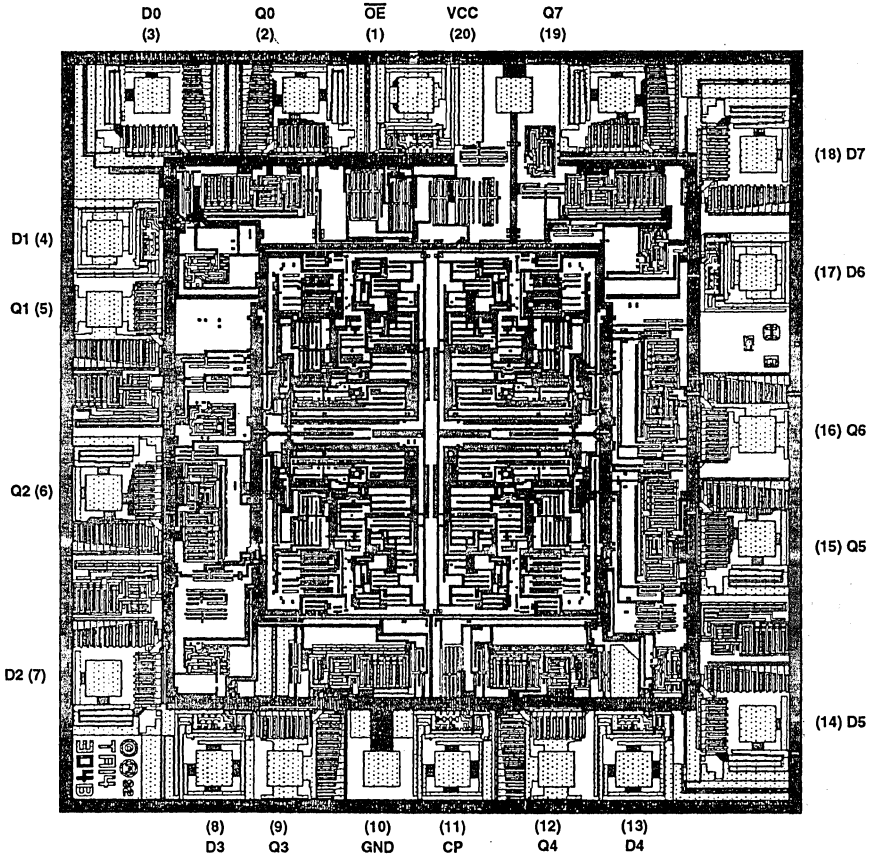
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS374MS



HARRIS SEMICONDUCTOR

HCTS390MS

Radiation Hardened Dual Decade Ripple Counter

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Rate 2 x 10^{-9} Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Military Temperature Range ..... -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range ..... 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = 2.0V Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

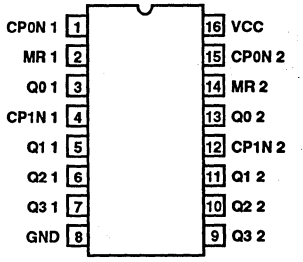
The Harris HCTS390MS is a Radiation Hardened dual decade ripple counter.

The HCTS390MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family .

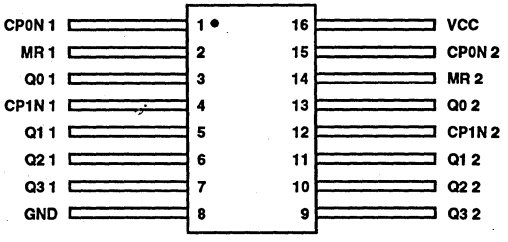
The HCTS390MS is supplied in a 16 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

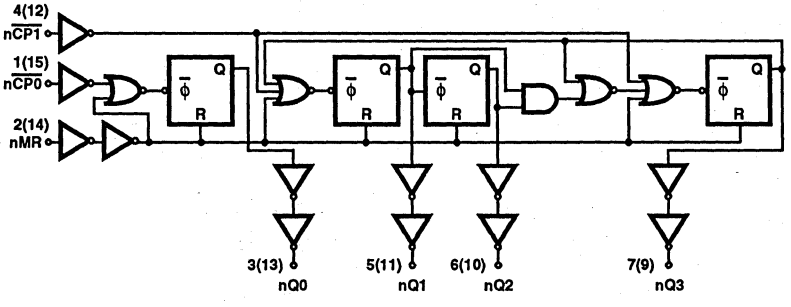
16 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T16, LEAD FINISH C
TOP VIEW



16 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F16, LEAD FINISH C
TOP VIEW



Functional Diagram



TRUTH TABLE

INPUTS		
CP	MR	ACTION
↗	L	No Change
↘	L	Count
H	H	All Qs Low

H = High Level
L = Low Logic Level
X = Immaterial
↗ = Low-to-High
↘ = High-to-Low

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2476.1**

Absolute Maximum Ratings

Supply Voltage (VCC) ..... -0.5 to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Rise and Fall Time at 4.5V VCC (tr, tf) ..... 500ns Max
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... 2.0V to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V (Standard Driver)	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = VCC or GND (Bus Driver)	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V (Standard Driver)	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VOUT = VCC - 0.4V (Bus Driver)	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	0.5	µA
			2, 3	+125°C, -55°C	-5.0	5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.80V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CP0N to Q0n	TPHL TPLH	VCC = 4.5V	9	+25°C	2	22	ns
			10, 11	+125°C, -55°C	2	27	ns
CP1Nn to Q1n	TPHL TPLH	VCC = 4.5V	9	+25°C	2	29	ns
			10, 11	+125°C, -55°C	2	35	ns
CP1Nn to Q2n	TPHL TPLH	VCC = 4.5V	9	+25°C	2	34	ns
			10, 11	+125°C, -55°C	2	41	ns
CP1Nn to Q3n	TPHL TPLH	VCC = 4.5V	9	+25°C	2	29	ns
			10, 11	+125°C, -55°C	2	35	ns
MR to QNn	TPHL	VCC = 4.5V	9	+25°C	2	23	ns
			10, 11	+125°C, -55°C	2	29	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1, 2, 3	+25°C	Typical 33		pF
			1, 2, 3	+125°C	Typical 37		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1, 2, 3	+25°C	-	10	pF
			1, 2, 3	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1, 2, 3	+25°C	-	15	ns
			1, 2, 3	+125°C	-	22	ns
Max Operating Frequency	FMAX	VCC = 4.5V	1, 2, 3	+25°C	-	27	MHz
			1, 2, 3	+125°C, -55°C	-	18	MHz
Pulse Width CP0Nn, CP1Nn	TW	VCC = 4.5V	1, 2, 3	+25°C	15	-	ns
			1, 2, 3	+125°C, -55°C	22	-	ns
Pulse Width Reset	TW	VCC = 4.5V	1, 2, 3	+25°C	13	-	ns
			1, 2, 3	+125°C, -55°C	20	-	ns
Removal Time Reset	TREM	VCC = 4.5V	1, 2, 3	+25°C	15	-	ns
			1, 2, 3	+125°C, -55°C	22	-	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.
2. Applies to DIC packaged devices.
3. Applies to Flatpack packaged devices.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	5.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-5.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 2.25V, VIL = 0.80V at 200K RAD, VIL = 0.30V at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 2.25V, VIL = 0.80V at 200K RAD, VIL = 0.30V at 1M RAD, IOL = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.80V at 200K RAD, VIL = 0.30V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
CP0Nn to Q0n	TPHL TPLH	VCC = 4.5V	+25°C	2	27	2	34	ns
CP1Nn to Q1n	TPHL TPLH	VCC = 4.5V	+25°C	2	35	2	44	ns
CP1Nn to Q2n	TPHL TPLH	VCC = 4.5V	+25°C	2	41	2	52	ns
CP1Nn to Q3n	TPHL TPLH	VCC = 4.5V	+25°C	2	35	2	44	ns
MR to Qn	TPHL	VCC = 4.5V	+25°C	2	29	2	37	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternate Group A in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 7, 9	Table 4 (Note 1)

NOTE: 1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
3, 5 - 7, 9 - 11, 13	1, 2, 4, 8,12, 14, 15	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 5 - 7, 9 - 11, 13	8	-	1, 2, 4, 12, 14 - 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	8	3, 5 - 7, 9 - 11, 13	2, 14, 16	1, 4, 12, 15	-

NOTES:

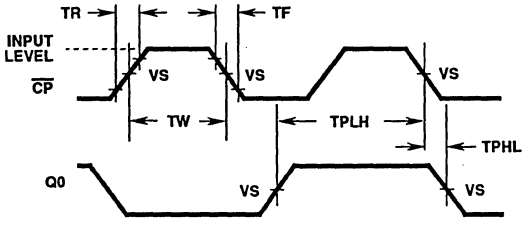
1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

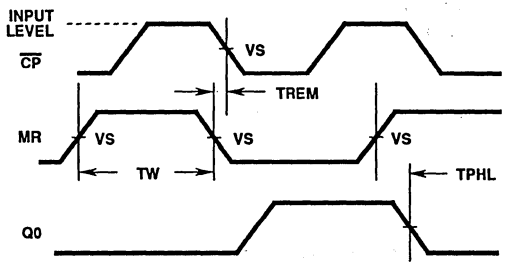
OPEN	GROUND	VCC = 5V ± 0.5V
3, 5 - 7, 9 - 11, 13	8	1, 2, 4, 12, 14 - 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

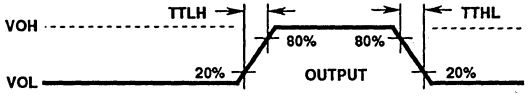
AC Timing Diagrams and Load Circuit



INPUT PULSE PRE-REQUISITE, PROPAGATION-DELAY, AND OUTPUT-TRANSITION TIMES



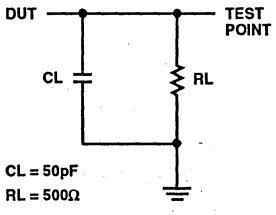
MASTER RESET PRE-REQUISITE AND PROPAGATION DELAYS



OUTPUT TRANSITION TIME

AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
VSS	0	V



Die Characteristics

DIE DIMENSIONS:
86 x 86 mils
2190µm x 2190µm

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

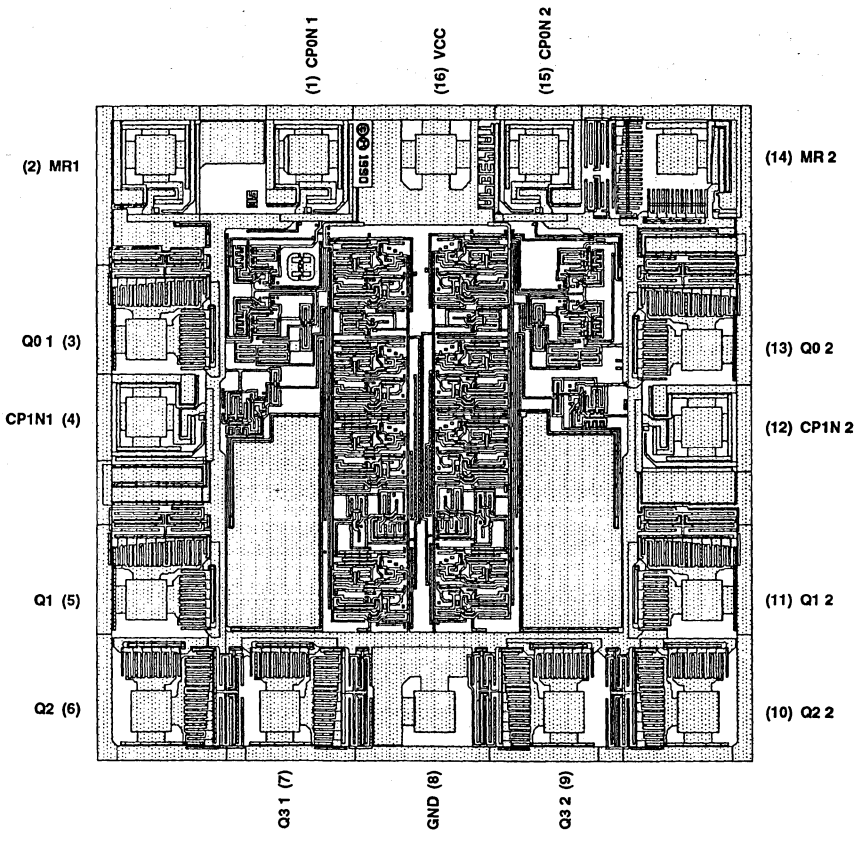
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS390MS



HARRIS SEMICONDUCTOR

HCTS393MS

Radiation Hardened Dual 4-Stage Binary Counter

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD (Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Rate 2 x 10^{-9} Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Standard Outputs..... 10 LSTTL Loads
- Military Temperature Range ..... -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range .....4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

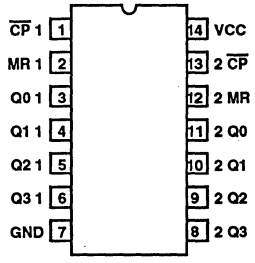
The Harris HCTS393MS is a Radiation Hardened 4-stage riple-carry binary counter. All counter stages are master-slave flip-flop. The state of the stage advances one count on the negative transition of each clock pulse. A high voltage level on the MR line resets all counters to their zero state. All inputs and outputs are buffered.

The HCTS393MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

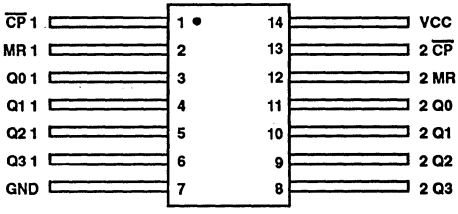
The HCTS393MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
CASE OUTLINE F-2A, CONFIGURATION 2,
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW



7 LOGIC

File Number 3071

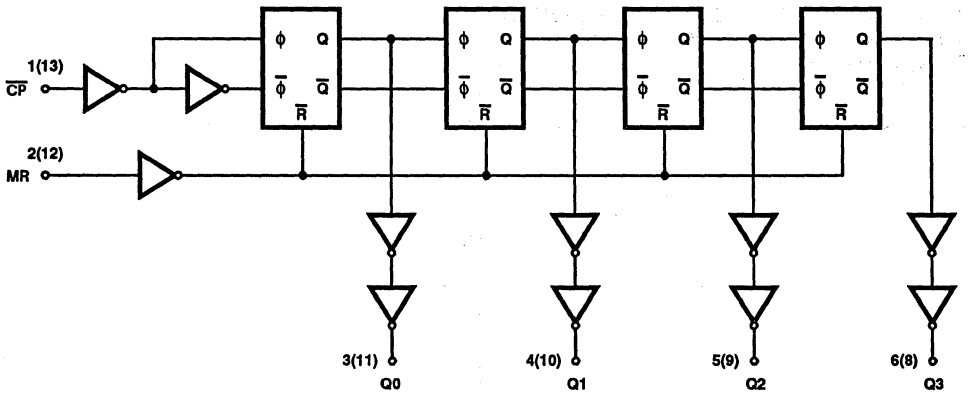
Truth Table

$\overline{CP}$ COUNT	OUTPUTS			
	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

$\overline{CP}$	MR	OUTPUT
⌐‾	L	No Change
‾⌐	L	Count
X	H	LLLL

H = High Lvel
L = Low Logic Level
X = Immaterial
⌐‾ = Low-to-High
‾⌐ = High-to-Low

Functional Diagram



Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (tr, tf) . . . . . 500ns Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
$\overline{CP}$n to Q0	TPHL TPLH	VCC = 4.5V	9	+25°C	2	29	ns
			10, 11	+125°C, -55°C	2	34	ns
$\overline{CP}$n to Q1	TPHL TPLH	VCC = 4.5V	9	+25°C	2	36	ns
			10, 11	+125°C, -55°C	2	43	ns
$\overline{CP}$n to Q2	TPHL TPLH	VCC = 4.5V	9	+25°C	2	43	ns
			10, 11	+125°C, -55°C	2	52	ns
$\overline{CP}$n to Q3	TPHL TPLH	VCC = 4.5V	9	+25°C	2	49	ns
			10, 11	+125°C, -55°C	2	59	ns
MR to Qn	TPHL	VCC = 4.5V	9	+25°C	2	30	ns
			10, 11	+125°C, -55°C	2	34	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 26		pF
			1	+125°CC	Typical 40		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL, TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C, -55°C	-	22	ns
Max Operating Frequency	FMAX	VCC = 4.5V	1	+25°C	-	27	MHz
			1	+125°C, -55°C	-	18	MHz
Pulse Width Clock	TW (CP)	VCC = 4.5V	1	+25°C	19	-	ns
			1	+125°C, -55°C	29	-	ns
Pulse Width Reset	TW (R)	VCC = 4.5V	1	+25°C	16	-	ns
			1	+125°C, -55°C	24	-	ns
Recovery Time Reset	TREC	VCC = 4.5V	1	+25°C	5	-	ns
			1	+125°C, -55°C	5	-	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
$\overline{CP}$n to Q0	TPHL TPLH	VCC = 4.5V	+25°C	2	34	2	43	ns
$\overline{CP}$n to Q1	TPHL TPLH	VCC = 4.5V	+25°C	2	43	2	53	ns
$\overline{CP}$n to Q2	TPHL TPLH	VCC = 4.5V	+25°C	2	52	2	65	ns
$\overline{CP}$n to Q3	TPHL TPLH	VCC = 4.5V	+25°C	2	59	2	73	ns
MR to Qn	TPHL	VCC = 4.5V	+25°C	2	34	2	43	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate group A inspection in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABEL 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
3 - 6, 8 - 11	1, 2, 7, 12, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3 - 6, 8 - 11	7	-	1, 2, 12 - 14	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	7	3 - 6, 8 - 11	2, 12, 14	1, 13	-

NOTES:

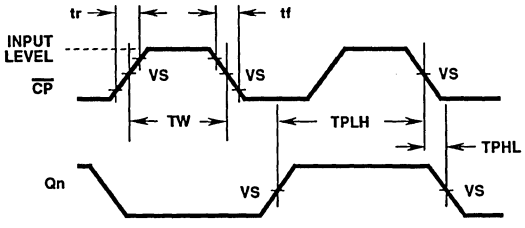
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

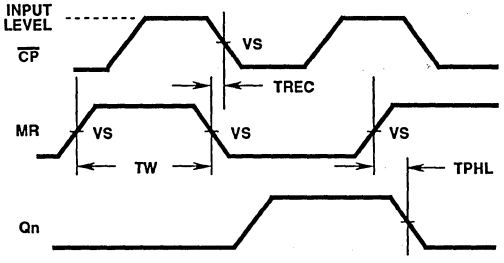
OPEN	GROUND	VCC = 5V ± 0.5V
3 - 6, 8 - 11	7	1, 2, 12 - 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

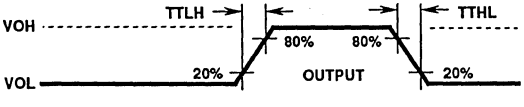
AC Timing Diagrams and Load Circuit



CLOCK PRE-REQUISITE AND PROPAGATION DELAY, AND OUTPUT-TRANSITION TIMES



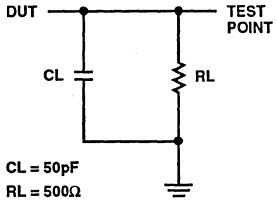
MASTER RESET PRE-REQUISITE AND PROPAGATION DELAYS



OUTPUT TRANSITION TIME

AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V



Die Characteristics

DIE DIMENSIONS:
86 x 86 mils

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

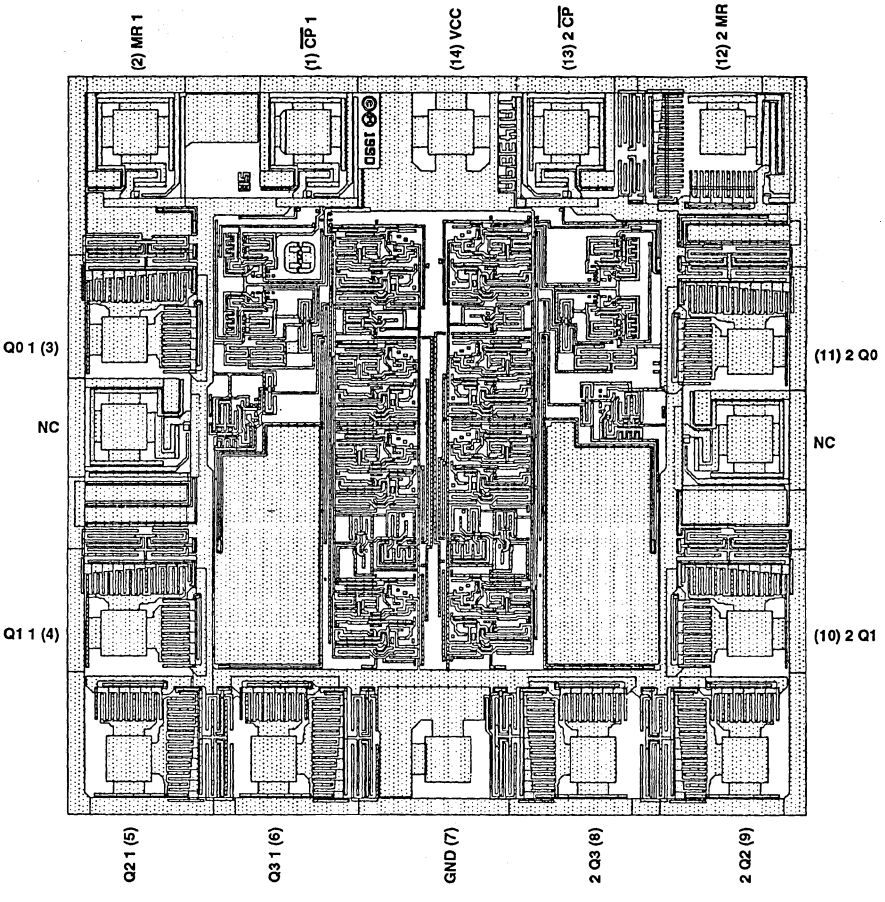
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS393MS



HARRIS SEMICONDUCTOR

HCTS540MS

Radiation Hardened Inverting Octal Buffer/Line Driver, Tri-State

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Bus Driver Outputs 15 LSTTL Loads
- Military Temperature Range -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

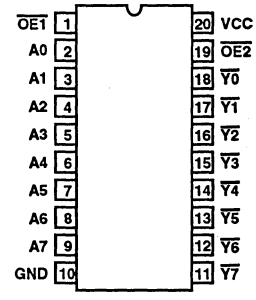
The Harris HCTS540MS is a Radiation Hardened inverting Octal Buffer/Line Driver, with two active-low output enables. The output enable pins ($\overline{OE1}$ and $\overline{OE2}$) control the tri-state outputs. If either enable is high the outputs will be in the high impedance state. For data output both enables ($\overline{OE1}$ and $\overline{OE2}$) must be low.

The HCTS540MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

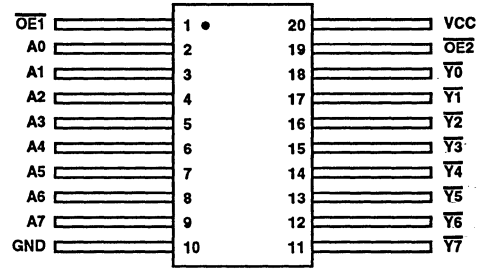
The HCTS540MS is supplied in a 20 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

20 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T20, LEAD FINISH C
TOP VIEW



20 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F20, LEAD FINISH C
TOP VIEW

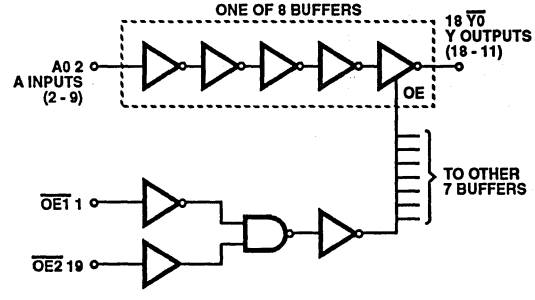


Truth Table

$\overline{OE1}$	$\overline{OE2}$	AN	OUTPUT
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

H = High Level
L = Low Level
X = Don't Care
Z = High Impedance

Functional Diagram



7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 2232.1

Absolute Maximum Ratings

Supply Voltage (VCC) ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) ..... +4.5V to +5.5V
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 500ns Max.
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V	1	+25°C	-7.2	-	mA
			2, 3	+125°C, -55°C	-6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC	1	+25°C	-1	+1	µA
			2, 3	+125°C, -55°C	-50	+50	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Data to Output	TPHL	VCC = 4.5V	9	+25°C	2	21	ns
	TPLH	VCC = 4.5V	10, 11	+125°C, -55°C	2	25	ns
Enable to Output	TPZL	VCC = 4.5V	9	+25°C	2	30	ns
			10, 11	+125°C, -55°C	2	35	ns
	TPZH	VCC = 4.5V	9	+25°C	2	26	ns
			10, 11	+125°C, -55°C	2	30	ns
Disable to Output	TPLZ, TPHZ	VCC = 4.5V	9	+25°C	2	26	ns
			10, 11	+125°C, -55°C	2	30	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 30		pF
			1	+125°C	Typical 30		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL, TTLH	VCC = 4.5V	1	+25°C	-	12	ns
			1	+125°C, -55°C	-	18	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	5.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-5.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	µA
Tri-State Ouptut Leakage Current	IOZ	Applied Voltage = 0V or VCC	+25°C	-50	+50	-100	+100	µA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Data to Output	TPLH, TPHL	VCC = 4.5V	+25°C	2	25	2	32	ns
Enable to Output	TPZL	VCC = 4.5V	+25°C	2	35	2	44	ns
	TPZH		+25°C	2	30	2	38	ns
Disable to Output	TPLZ, TPHZ	VCC = 4.5V	+25°C	2	30	2	38	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour
IOZL/IOZH	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC BURN-IN AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
11 - 18	1 - 10, 19	-	20	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
11 - 18	10	-	1 - 9, 19, 20	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	10	11 - 18	20	1, 19	2 - 9

NOTES:

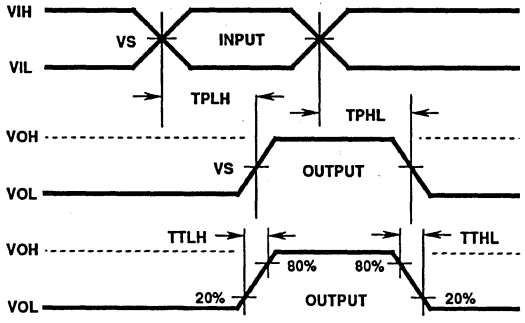
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 680Ω ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
11 - 18	10	1 - 9, 19, 20

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

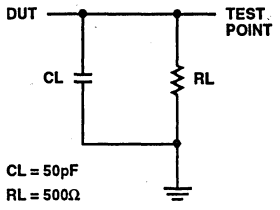
AC Timing Diagrams



AC VOLTAGE LEVELS

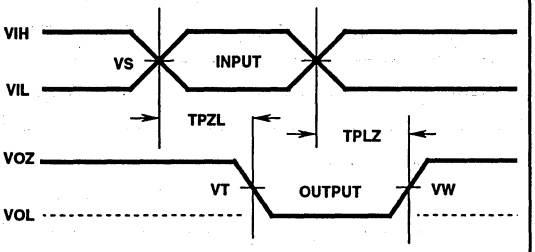
PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



7 LOGIC

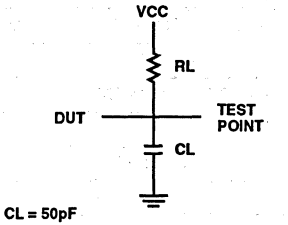
Tri-State Low Timing Diagrams



TRI-STATE LOW VOLTAGE LEVELS

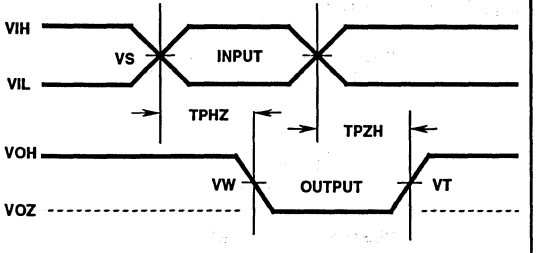
PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	0.90	V
VIL	0	V
GND	0	V

Tri-State Low Load Circuit



CL = 50pF
RL = 500Ω

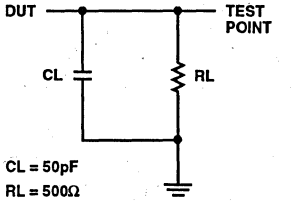
Tri-State High Timing Diagrams



TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	3.60	V
VIL	0	V
GND	0	V

Tri-State High Load Circuit



CL = 50pF
RL = 500Ω

Die Characteristics

DIE DIMENSIONS:
101 x 85mils

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

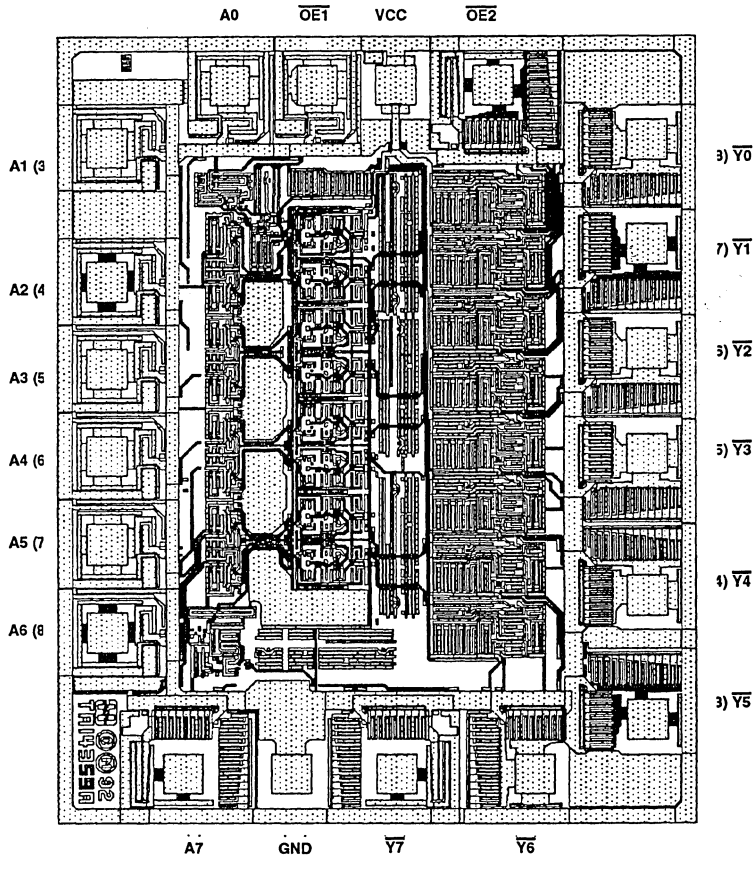
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS540MS



HARRIS SEMICONDUCTOR

HCTS541MS

Radiation Hardened Non-Inverting Octal Buffer/Line Driver, Tri-State

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Bus Driver Outputs - 15 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

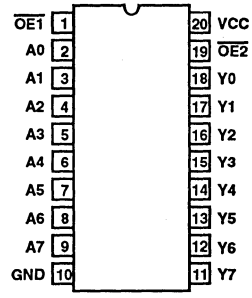
The Harris HCTS541MS is a Radiation Hardened non-inverting octal buffer/line driver, tri-state outputs. The output enable pins (OEN1 and OEN2) control the tri-state outputs. If either enable is high the outputs will be in the high impedance state. For data output both enables (OEN1 and OEN2) must be low.

The HCTS541MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

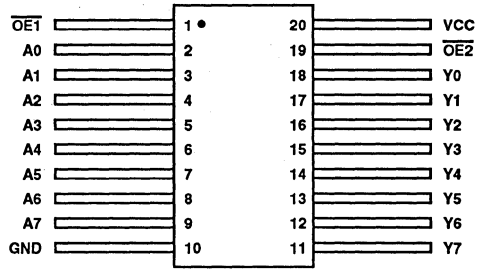
The HCTS54 is supplied in a 20 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

20 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T20, LEAD FINISH C
TOP VIEW



20 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F20, LEAD FINISH C
TOP VIEW



Truth Table

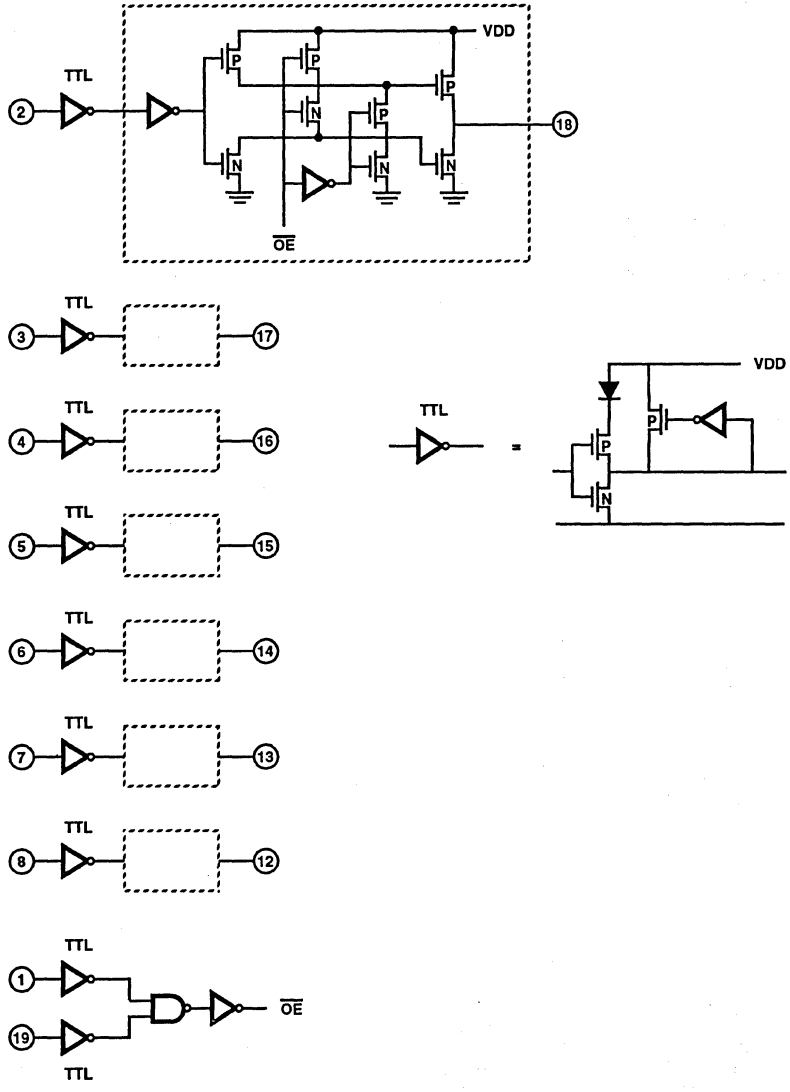
INPUTS			OUTPUTS
$\overline{OE1}$	$\overline{OE2}$	An	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3073**

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage (VCC) ..... -0.5 to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) ..... +4.5V to +5.5V
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 500ns Max
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	4.0	µA
			2, 3	+125°C, -55°C	-	7.50	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V	1	+25°C	-7.2	-	mA
			2, 3	+125°C, -55°C	-6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC	1	+25°C	-1	+1	µA
			2, 3	+125°C, -55°C	-50	+50	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Data to Output	TPHL, TPLH	VCC = 4.5V	9	+25°C	2	20	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	22	ns
$\overline{\text{Enable}}$ to Output	TPZL	VCC = 4.5V	9	+25°C	2	23	ns
			10, 11	+125°C, -55°C	2	26	ns
	TPZH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	21	ns
$\overline{\text{Disable}}$ to Output	TPLZ	VCC = 4.5V	9	+25°C	2	22	ns
			10, 11	+125°C, -55°C	2	23	ns
	TPHZ	VCC = 4.5V	9	+25°C	2	21	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 25		pF
			1	+125°C	Typical 40		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL, TTLH	VCC = 4.5V	1	+25°C	-	12	ns
			1	+125°C, -55°C	-	18	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	3.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	5.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-5.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Output Voltage High	VOH	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-5	+5	-5	+5	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Data to Output	TPHL, TPLH	VCC = 4.5V	+25°C	2	22	2	28	ns
Enable to Output	TPZL	VCC = 4.5V	+25°C	2	26	2	33	ns
	TPZH	VCC = 4.5V	+25°C	2	21	2	27	ns
Disable to Output	TPLZ	VCC = 4.5V	+25°C	2	23	2	29	ns
	TPHZ	VCC = 4.5V	+25°C	2	22	2	28	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour
IOZL/IOZH	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternated Group A Inspection in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE: 1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
11 - 18	1, 10 - 19	-	20	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
11 - 18	10	-	1 - 9, 19, 20	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	10	11 - 18	20	1, 19	2 - 9

NOTES:

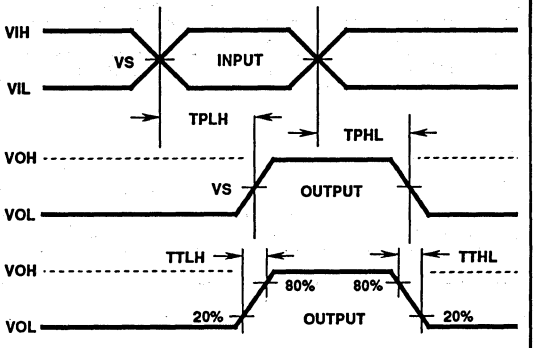
1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680Ω ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
11 - 18	10	1 - 9, 19, 20

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

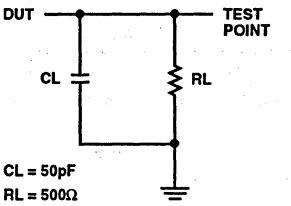
AC Timing Diagrams



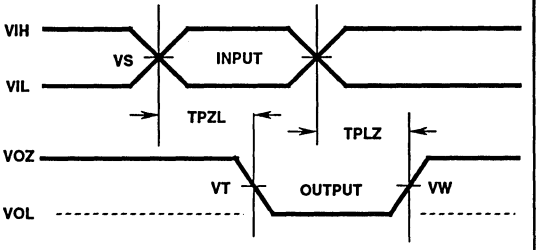
AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
VSS	0	V

AC Load Circuit



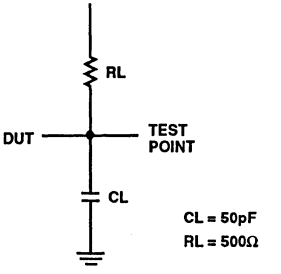
Tri-State Low Timing Diagrams



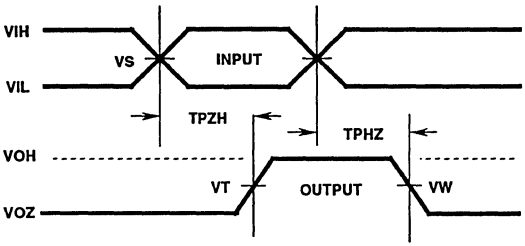
TRI-STATE LOW VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	0.90	V
GND	0	V

Tri-State Low Load Circuit



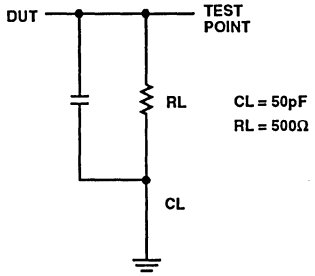
Tri-State High Timing Diagrams



TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	3.60	V
GND	0	V

Tri-State High Load Circuit



Die Characteristics

DIE DIMENSIONS:
101 x 85 mils

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

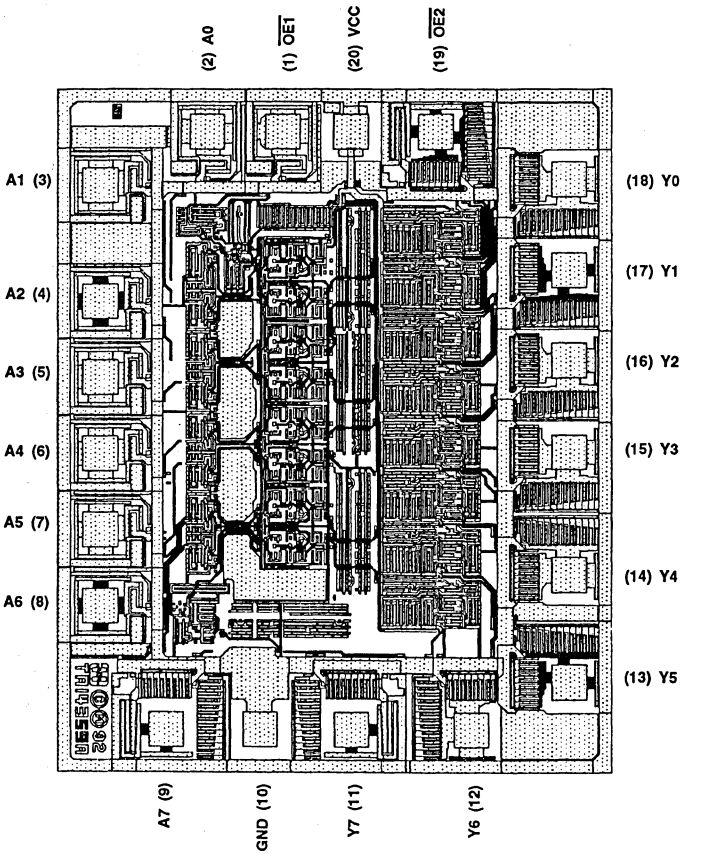
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS541MS



HARRIS SEMICONDUCTOR

HCS573MS

Radiation Hardened Octal Transparent Latch, Tri-State

December 1992

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity 2 x 10^{-9} Error/Bit Day (Typ)
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Bus Driver Outputs - 15 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.3 VCC Max
  - VIH = 0.7 VCC Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

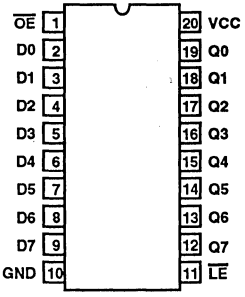
The Harris HCS573MS is a Radiation Hardened octal transparent tri-state latch with an active low output enable. The HCS573MS utilizes advanced CMOS/SOS technology. The outputs are transparent to the inputs when the Latch Enable ($\overline{LE}$) is HIGH. When the Latch Enable ($\overline{LE}$) goes LOW, the data is latched. The Output Enable ($\overline{OE}$) controls the tri-state outputs. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high impedance state. The latch operation is independent of the state of the Output Enable.

The HCS573MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

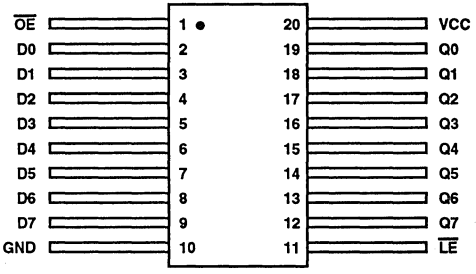
The HCS573MS is supplied in a 20 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

20 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR, CDIP2-T20, LEAD FINISH C
TOP VIEW



20 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR, CDFP4-F20, LEAD FINISH C
TOP VIEW

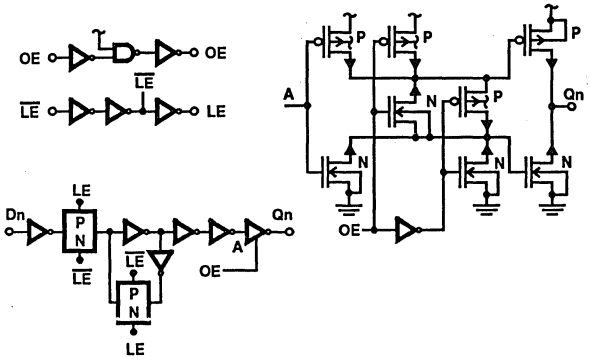


Truth Table

$\overline{OUTPUT\ ENABLE}$	$\overline{LATCH\ ENABLE}$	DATA	OUTPUT
L	H	H	H
L	H	L	L
L	L	l	L
L	L	h	H
H	X	X	Z

H = High Level X = Immaterial
L = Low Level Z = High Impedance
l = Low voltage level prior to the high-to-low latch enable transition
h = High voltage level prior to the high-to-low latch enable transition

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2135.1**

Absolute Maximum Ratings

Supply Voltage (VCC) ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC) ..... +4.5V to +5.5V
Input Rise and Fall Times at VCC = 4.5V (TR, TF) ..... 500ns Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 30% of VCC
Input High Voltage (VIH) ..... 70% of VCC to VCC

TABLE 1. DC. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Output Leakage Current	IOZ	VCC = 4.5V and 5.5V, VO = VCC or GND	1	+25°C	-1.0	+1.0	µA
			2, 3	+125°C, -55°C	-50	+50	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Data to Qn	TPLH TPHL	VCC = 4.5V	9	+25°C	2	24	ns
			10, 11	+125°C, -55°C	2	29	ns
$\overline{LE}$ to Qn	TPLH	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	35	ns
	TPHL	VCC = 4.5V	9	+25°C	2	31	ns
			10, 11	+125°C, -55°C	2	40	ns
Enable to Output	TPZL	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	33	ns
	TPZH	VCC = 4.5V	9	+25°C	2	24	ns
			10, 11	+125°C, -55°C	2	29	ns
Disable to Output	TPLZ	VCC = 4.5V	9	+25°C	2	25	ns
			10, 11	+125°C, -55°C	2	29	ns
	TPZL	VCC = 4.5V	9	+25°C	2	21	ns
			10, 11	+125°C, -55°C	2	25	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 20		pF
			1	+125°C	Typical 40		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	12	ns
			1	+125°C, -55°C	-	18	ns
Setup Time Data to $\overline{LE}$	TSU	VCC = 4.5V	1	+25°C	10	-	ns
			1	+125°C, -55°C	15	-	ns
Hold Time Data to $\overline{LE}$	TH	VCC = 4.5V	1	+25°C	8	-	ns
			1	+125°C, -55°C	12	-	ns
Pulse Width $\overline{LE}$	TW	VCC = 4.5V	1	+25°C	16	-	ns
			1	+125°C, -55°C	24	-	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	5.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-5.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V or 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V or 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC, VCC = 4.5V and 5.5V	+25°C	-	±50	-	±100	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) at 200K RAD, VIL = 0.12(VCC) at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Data to Qn	TPHL TPLH	VCC = 4.5V	+25°C	2	29	2	36.5	ns
LEN to Qn	TPLH	VCC = 4.5V	+25°C	2	35	2	43.8	ns
	TPHL	VCC = 4.5V	+25°C	2	40	2	50	ns
Enable to Output	TPZL	VCC = 4.5V	+25°C	2	33	2	41.3	ns
	TPZH	VCC = 4.5V	+25°C	2	29	2	36.3	ns
Disable to Output	TPLZ	VCC = 4.5V	+25°C	2	29	2	36.3	ns
	TPHZ	VCC = 4.5V	+25°C	2	25	2	31.3	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour
IOZL/IOZH	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
12 - 19	1 - 11	-	20	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
12 - 19	10	-	1 - 9, 11, 20	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	1, 10	12 - 19	20	11	2 - 9

NOTES:

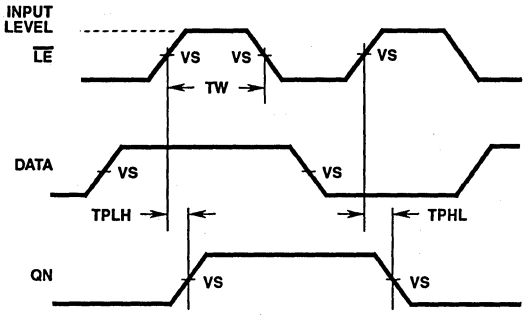
1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680kΩ ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

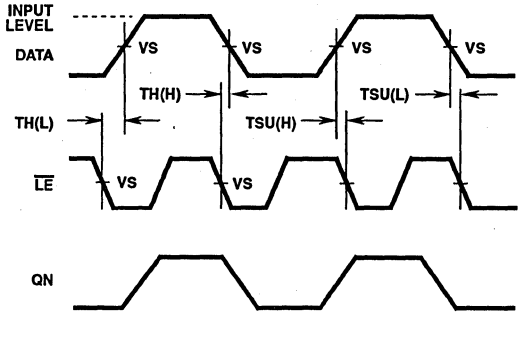
OPEN	GROUND	VCC = 5V ± 0.5V
12 - 19	10	1 - 9, 11, 20

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

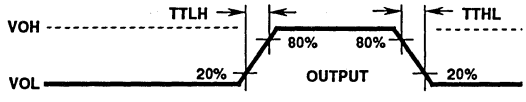
AC Timing Diagrams and Load Circuit



LATCH ENABLE PROPAGATION DELAYS



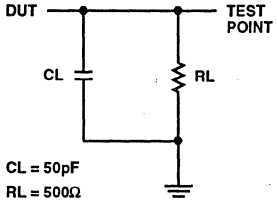
LATCH ENABLE PREREQUISITE TIMES



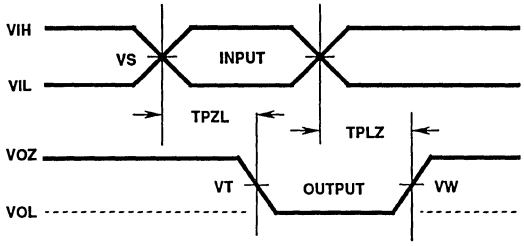
DATA SET-UP AND HOLD TIMES

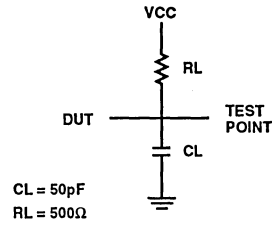
AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V



Tri-State Low Timing Diagram and Load Circuit

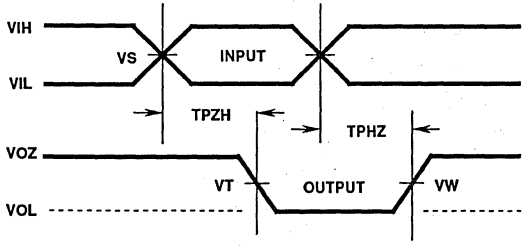


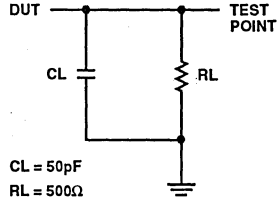


TRI-STATE LOW VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	0.90	V
GND	0	V

Tri-State High Timing Diagram and Load Circuit





TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	3.60	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
101 x 85 mils

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

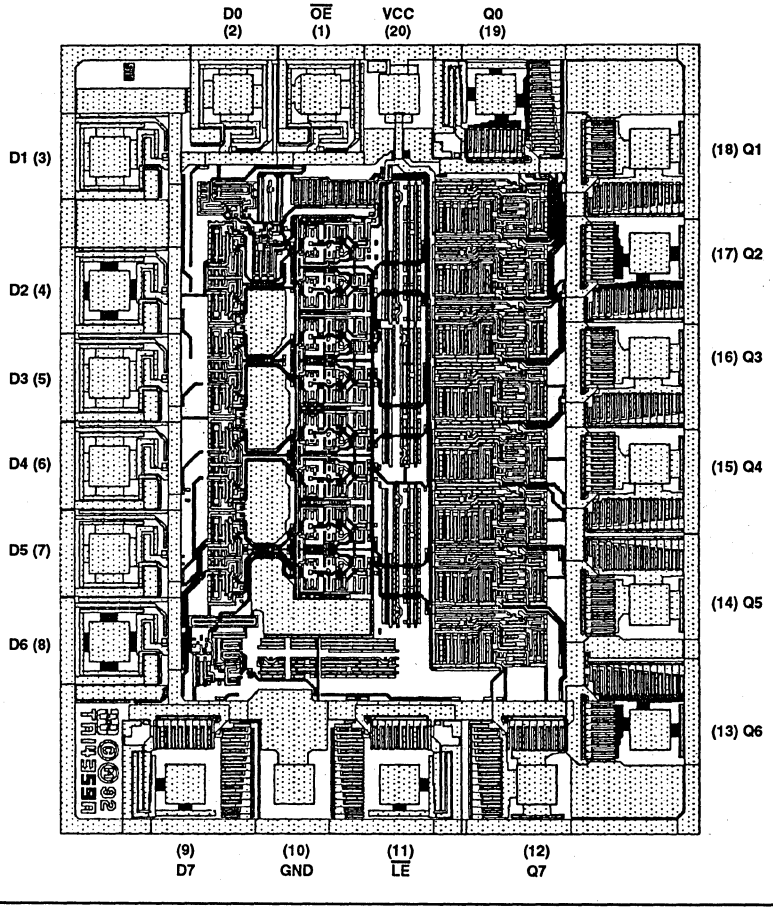
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCS573MS



HARRIS SEMICONDUCTOR

HCTS574MS

Radiation Hardened Octal D-Type Flip-Flop, Tri-State, Positive Edge Triggered

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Immunity 2 x 10^{-9} Error/Bit-Day
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Bus Driver O11utputs - 15 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

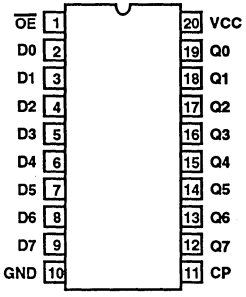
The Harris HCTS574MS is a Radiation Hardened non-inverting octal D-type, positive edge triggered flip-flop with tri-stateable outputs. The HCTS574MS utilizes advanced CMOS/SOS technology. The eight flip-flops enter data into their registers on the LOW-to-HIGH transition of the clock (CP). Data is also transferred to the outputs during this transition. The output enable ($\overline{OE}$) controls the tri-state outputs and is independent of the register operation. When the output enable is high, the outputs are in the high impedance state.

The HCTS574MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

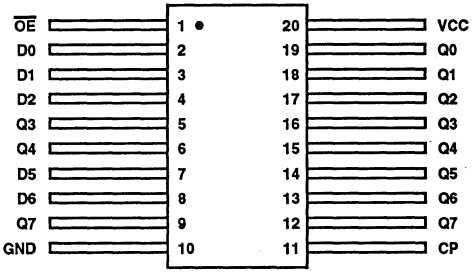
The HCTS574MS is supplied in a 20 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

20 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T20
TOP VIEW



20 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F20
TOP VIEW

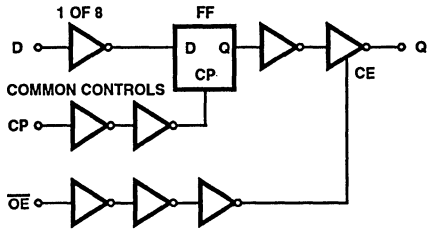


Truth Table

INPUTS			OUTPUTS
$\overline{OE}$	CP	Dn	Qn
L	↑	H	H
L	↑	L	L
L	L	X	Q0
L	H	X	Q0
H	X	X	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance
↑ = Transition from Low to High Level
Q0 = the level of Q before the indicated input conditions were established

Functional Diagram



7 LOGIC

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Rise and Fall Times at 4.5V VCC(TR, TF) . . . . . 500ns Max.
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC	1	+25°C	-1	+1	µA
			2, 3	+125°C, -55°C	-50	+50	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Clock to Q	TPLH, TPHL	VCC = 4.5V	9	+25°C	2	29	ns
			10, 11	+125°C, -55°C	2	36	ns
Enable to Ouptput	TPZL	VCC = 4.5V	9	+25°C	2	32	ns
			10, 11	+125°C, -55°C	2	39	ns
	TPZH	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	32	ns
Disable to Output	TPLZ, TPHZ	VCC = 4.5V	9	+25°C	2	23	ns
			10, 11	+125°C, -55°C	2	28	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, FQ = 1MHz	1	+25°C	Typical 26		pF
			1	+125°C	Typical 38		pF
Input Capacitance	CIN	VCC = Open, FQ = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	12	ns
			1	+125°C, -55°C	-	18	ns
Max Operating Frequency	FMAX	VCC = 4.5V	1	+25°C	-	30	MHz
			1	+125°C, -55°C	-	20	MHz
Setup Time Data to Clock	TSU	VCC = 4.5V	1	+125°C, -55°C	12	-	ns
			1	+125°C, -55°C	18	-	ns
Hold Time Data to Clock	TH	VCC = 4.5V	1	+125°C, -55°C	5	-	ns
			1	+125°C, -55°C	5	-	ns
Pulse Width Clocks	TW	VCC = 4.5V	1	+125°C, -55°C	16	-	ns
			1	+125°C, -55°C	24	-	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	3.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	5.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-5.0	-	mA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Output Voltage Low	VOL	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	μA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC	+25°C	-	±50	-	±100	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Clock to Q	TPLH, TPHL	VCC = 4.5V	+25°C	2	36	2	45	ns
Enable to Output	TPZL	VCC = 4.5V	+25°C	2	39	2	49	ns
	TPZH	VCC = 4.5V	+25°C	2	32	2	40	ns
Disable to Output	TPLZ	VCC = 4.5V	+25°C	2	28	2	35	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUB-GROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour
IOZL/IOZH	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
PDA	100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
PDA	100%/5004	1, 7, 9, Deltas	
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUPS	METHOD	GROUP A SUBGROUPS	READ AND RECORD
Group D	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC BURN-IN AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
12 - 19	1 - 11	-	20	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
12 - 19	10	-	1 - 9, 11, 20	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	1, 10	12 - 19	20	11	2 - 9

NOTES:

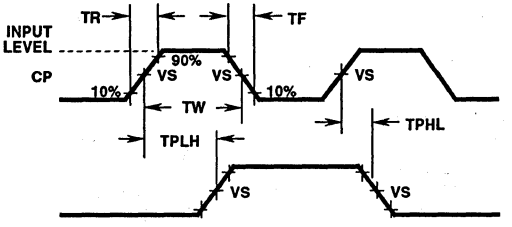
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 680Ω ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

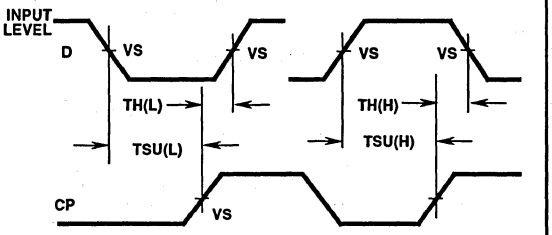
OPEN	GROUND	VCC = 5V ± 0.5V
12 - 19	10	1 - 9, 11, 20

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

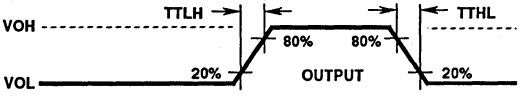
AC Timing Diagrams



CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



DATA SET-UP AND HOLD TIMES

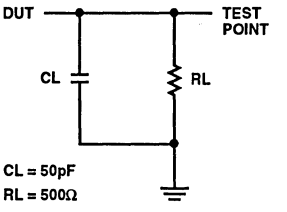


OUTPUT TRANSITION TIME

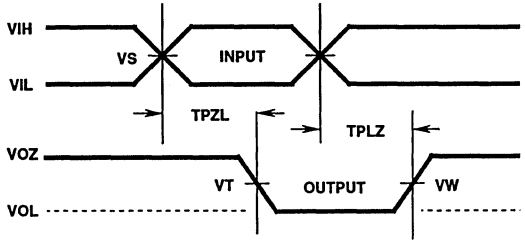
AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



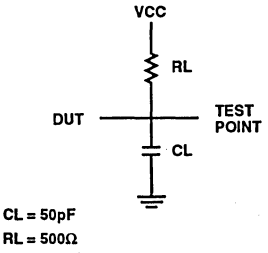
Tri-State Low Timing Diagrams



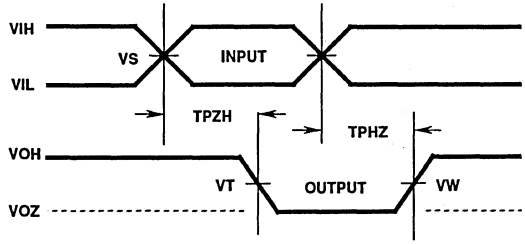
TRI-STATE LOW VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	0.90	V
GND	0	V

Tri-State Low Load Circuit



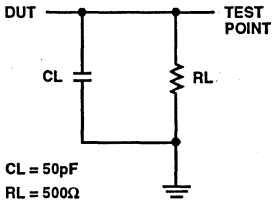
Tri-State High Timing Diagrams



TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	3.60	V
GND	0	V

Tri-State High Load Circuit



Die Characteristics

DIE DIMENSIONS:
101 x 85 mils

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

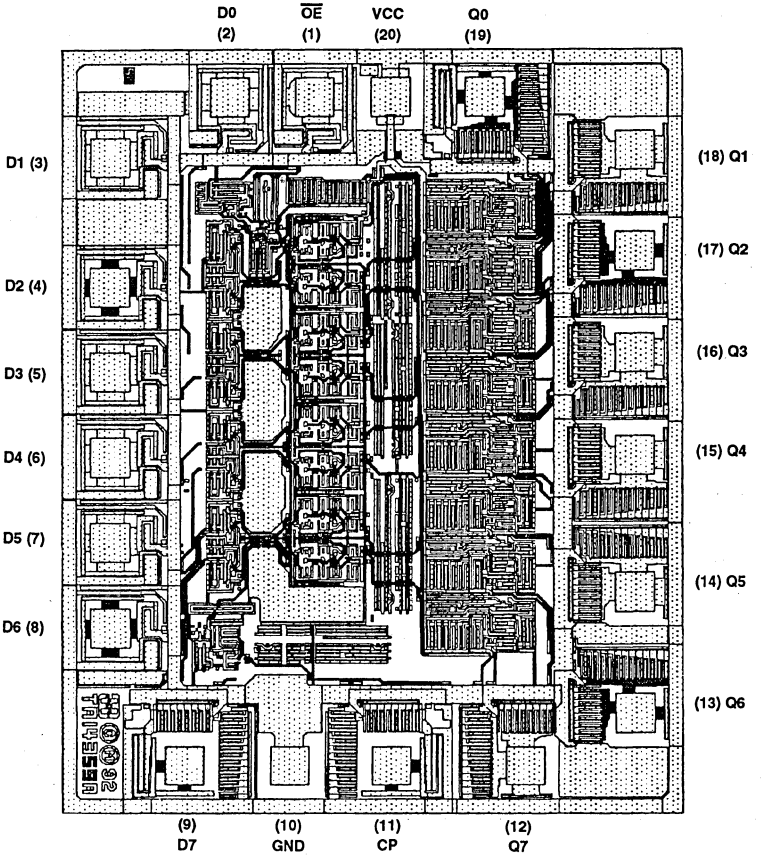
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS574MS



HARRIS SEMICONDUCTOR

HCTS646MS

Radiation Hardened Octal Bus Transceiver/Register, Tri-State

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Rate 2 x 10^{-9} Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Bus Driver Outputs - 15 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

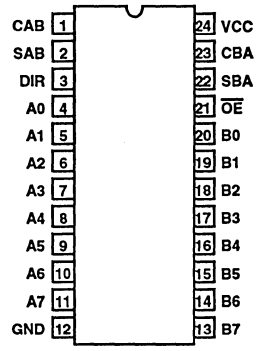
The Harris HCTS646MS is a Radiation Hardened Tri-state Octal Bus Tranceiver/Register with Non-Inverting outputs. This device is a bus transceiver with D-type flip-flops which act as internal storage registers. Data on the A bus or the B bus can be clocked into the registers on a High-to-Low transition of either CAB ro CBA clock inputs. Output enable ($\overline{OE}$) and Direction (DIR) inputs control the transceiver functions. Data present at the high impedance output can be stored in either register or both but only one of the two buses can be enabled as outputs at any one time. The select controls (SAB and SBA) can multiplex stored and transparent (real time) data. The direction control determines which data bus will receive data when the $\overline{OE}$ pin is LOW. In the high impedance mode ($\overline{OE}$ high), A data can be stored in one register and B data in the other register. Data at the A or B terminals can be clocked into the storage flip-flops at any time.

The HCTS646MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

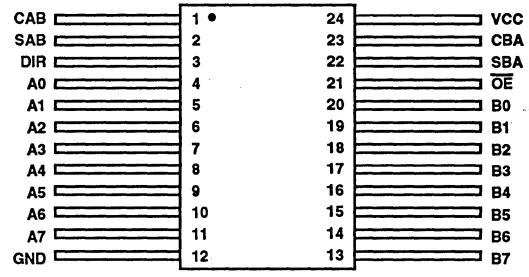
The HCTS646MS is supplied in a 24 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

24 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T24, LEAD FINISH C
TOP VIEW



24 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F24, LEAD FINISH C
TOP VIEW

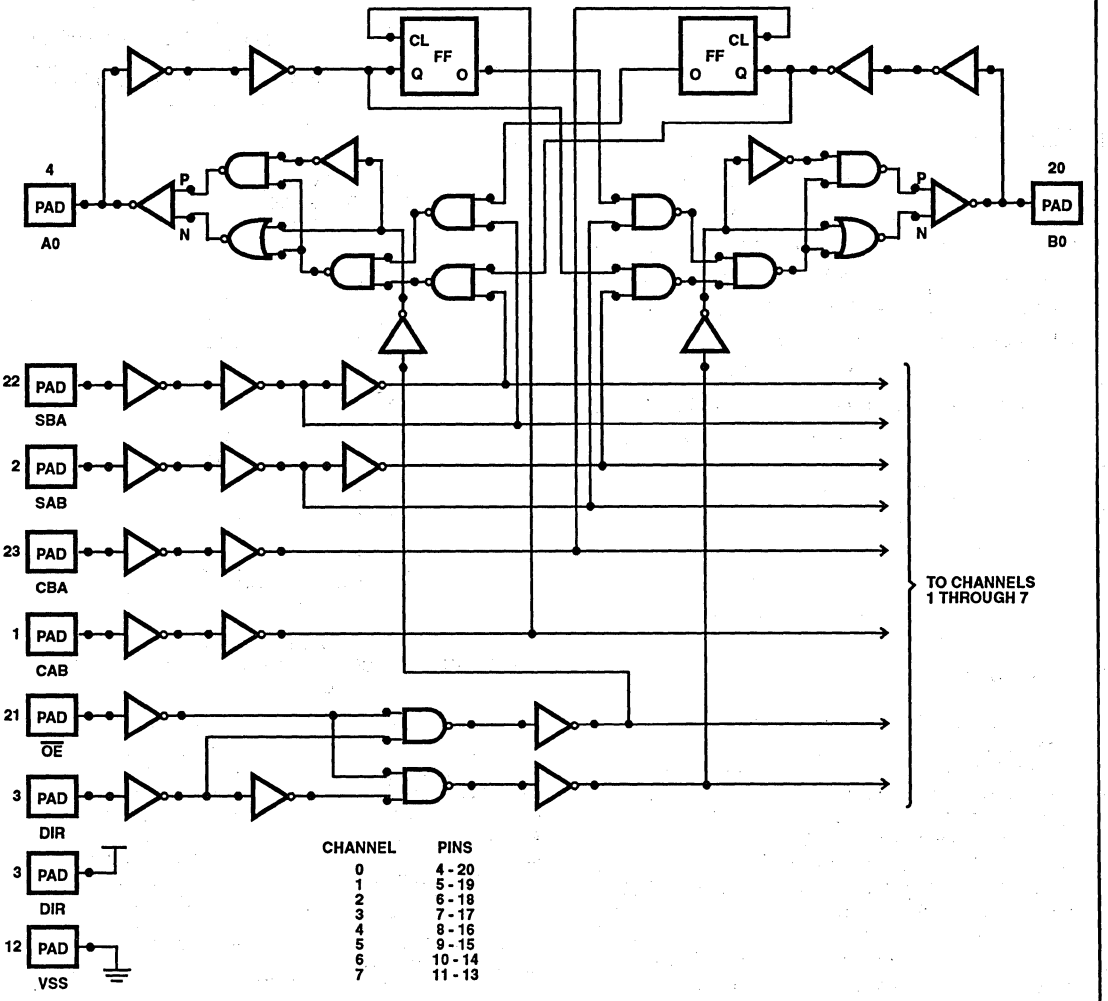


7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3074

Functional Diagram



Truth Table

INPUTS						DATA I/O*		
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	OPERATION OR FUNCTION
X	X	↑	X	X	X	Input Not Specified	Not Specified Input	Store A, B Unspecified
X	X	X	↑	X	X	Input Not Specified	Input	Store B, A Unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H or L	H or L	X	X	Input	Input	Isolation, Hold Storage
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X	Input	Output	Stored $\overline{A}$ Data to B Bus

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

	θ_{ja}	θ_{jc}
Thermal Impedance		
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 500ns Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	0.5	µA
			2, 3	+125°C, -55°C	-5.0	5.0	µA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC	1	+25°C	-1	+1	µA
			2, 3	+125°C, -55°C	-50	+50	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
A Data to B Bus (Store)	TPLH, TPHL	VCC = 4.5V	9	+25°C	2	31	ns
			10, 11	+125°C, -55°C	2	36	ns
B Data to A Bus (Store)	TPLH, TPHL	VCC = 4.5V	9	+25°C	2	32	ns
			10, 11	+125°C, -55°C	2	37	ns
A Data to B Bus	TPLH, TPHL	VCC = 4.5V	9	+25°C	2	24	ns
			10, 11	+125°C, -55°C	2	27	ns
B Data to A Bus	TPLH, TPHL	VCC = 4.5V	9	+25°C	2	24	ns
			10, 11	+125°C, -55°C	2	27	ns
Select to Data	TPLH, TPHL	VCC = 4.5V	9	+25°C	2	30	ns
			10, 11	+125°C, -55°C	2	34	ns
DIR to Output	TPLZ, TPHZ	VCC = 4.5V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	31	ns
$\overline{\text{Enable}}$ to Output	TPLZ, TPHZ	VCC = 4.5V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	31	ns
DIR to Output	TPZL, TPZH	VCC = 4.5V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	34	ns
$\overline{\text{Enable}}$ to Output	TPZL, TPZH	VCC = 4.5V	9	+25°C	2	30	ns
			10, 11	+125°C, -55°C	2	36	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 36		pF
			1	+125°C	Typical 82		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL, TTLH	VCC = 4.5V	1	+25°C	-	12	ns
			1	+125°C, -55°C	-	18	ns
Max Operating Frequency	FMAX	VCC = 4.5V	1	+25°C	-	25	MHz
			1	+125°C, -55°C	-	17	MHz
Setup Time Data to Clock	TSU	VCC = 4.5V	1	+25°C	12	-	ns
			1	+125°C, -55°C	18	-	ns
Hold Time Data to Clock	TH	VCC = 4.5V	1	+25°C	5	-	ns
			1	+125°C, -55°C	5	-	ns
Pulse Width Clocks	TW	VCC = 4.5V	1	+25°C	25	-	ns
			1	+125°C, -55°C	38	-	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	-	2.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	5.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	-5.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
A Data to B Bus (Store)	TPLH, TPHL	VCC = 4.5V	+25°C	2	36	2	45	ns
B Data to A Bus (Store)	TPLH, TPHL	VCC = 4.5V	+25°C	2	37	2	46	ns
A Data to B Bus	TPLH, TPHL	VCC = 4.5V	+25°C	2	27	2	34	ns
B Data to A Bus	TPLH, TPHL	VCC = 4.5V	+25°C	2	27	2	34	ns
Select to Data	TPLH, TPHL	VCC = 4.5V	+25°C	2	34	2	42	ns
DIR to Output	TPLZ, TPHZ	VCC = 4.5V	+25°C	2	31	2	39	ns
Enable to Output	TPLZ, TPHZ	VCC = 4.5V	+25°C	2	31	2	39	ns
DIR to Output	TPZL, TPZH	VCC = 4.5V	+25°C	2	34	2	42	ns
Enable to Output	TPZL, TPZH	VCC = 4.5V	+25°C	2	36	2	45	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour
IOZL/IOZH	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternate Group A inspection in accordance with Method 5005 of Mil-Std-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE: Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC I BURN-IN (Note 1)					
4 - 11	1 - 3, 12 - 23	-	24	-	-
STATIC II BURN-IN (Note 1)					
-	12	-	1 - 11, 13 - 24	-	-
DYNAMIC BURN-IN (Note 2)					
-	1 - 3, 12, 21, 22	4 - 11	24	23	13 - 20

NOTES:

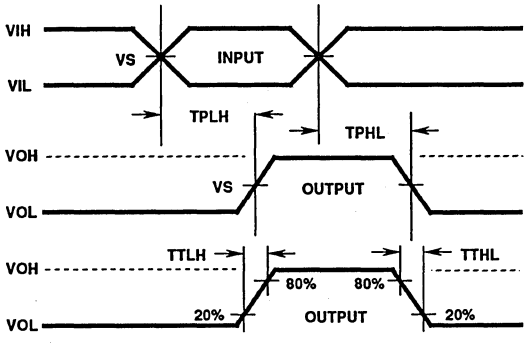
1. Each pin except VCC and GND will have a resistor of 680Ω ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in

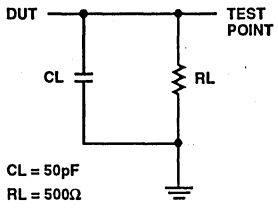
TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
-	12	1 - 11, 13 - 24

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

AC Timing Diagrams and Load Circuit

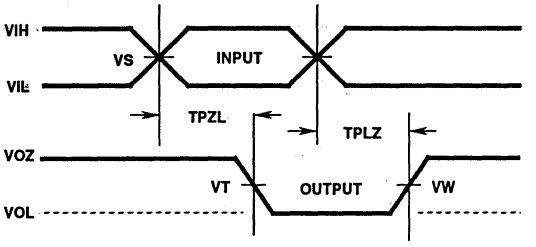


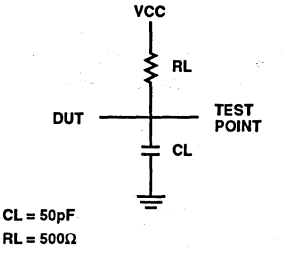


AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Tri-State Low Timing Diagrams and Load Circuit

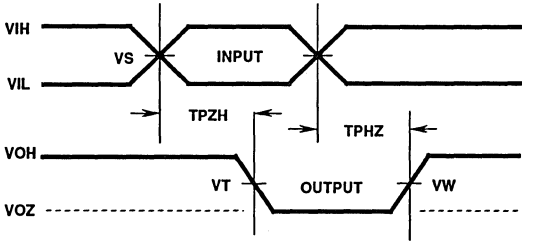


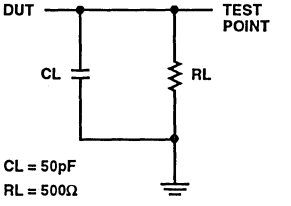


TRI-STATE LOW VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	0.90	V
GND	0	V

Tri-State High Timing Diagrams and Load Circuit





TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	3.60	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:
124 x 110 mils

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

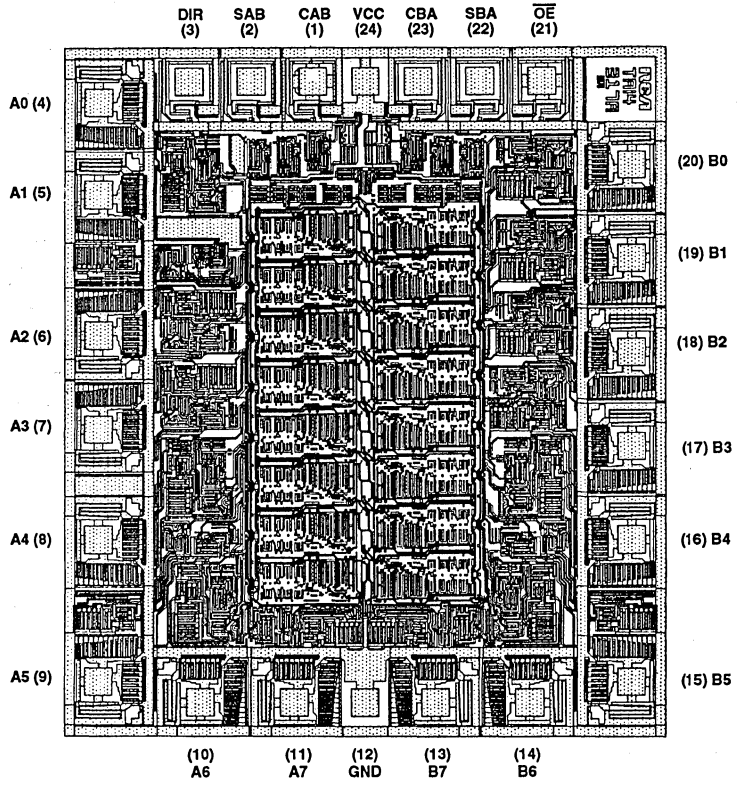
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS646MS



HARRIS SEMICONDUCTOR

HCTS4002MS

Radiation Hardened Dual 4-Input NOR Gate

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

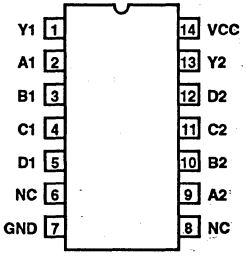
The Harris HCTS4002MS is a Radiation Hardened Dual 4-Input NOR Gate. A high on any input forces the output to a low state.

The HCTS4002MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

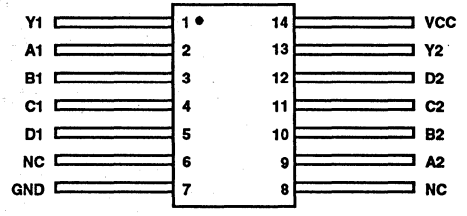
The HCTS4002MS is supplied in a 14 lead Weld Seal Ceramic flatpack (K suffix) or a Weld Seal Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW

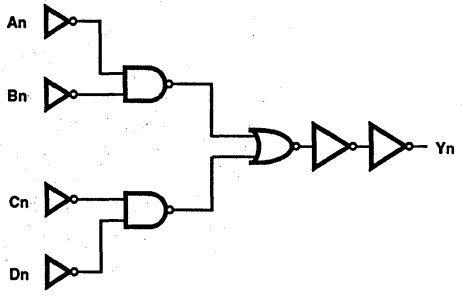


Truth Table

INPUTS				OUTPUTS
An	Bn	Cn	Dn	Yn
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

NOTE: L = Logic Level Low, H = Logic level High, X = Don't Care

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3075

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5 to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input. . . . . ±10mA
DC Drain Current, Any One Output. . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC) . . . . . +4.5V to +5.5V
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 500ns Max
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-0.5	+0.5	µA
			2, 3	+125°C, -55°C	-5.0	+5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input to Output	TPHL, TPLH	VCC = 4.5V	9	+25°C	2	22	ns
			10, 11	+125°C, -55°C	2	25	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	Typical 25		pF
			1	+125°C	Typical 31		pF
Input Capacitance	CIN	VCC = Open, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50µA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V or 5.5V, VIH =VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50µA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	µA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD (Note 3)	+25°C	-	-	-	-	-
Input to Output	TPHL, TPLH	VCC = 4.5V	+25°C	2	25	2	36	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	3μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE: 1. Alternate Group A Inspection in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE: 1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
1, 6, 8, 13	2 - 5, 7, 9 - 12	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
1, 6, 8, 13	7	-	2 - 5, 9 - 12, 14	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
6, 8	7	1, 13	14	2 - 5, 9 - 12	-

NOTES:

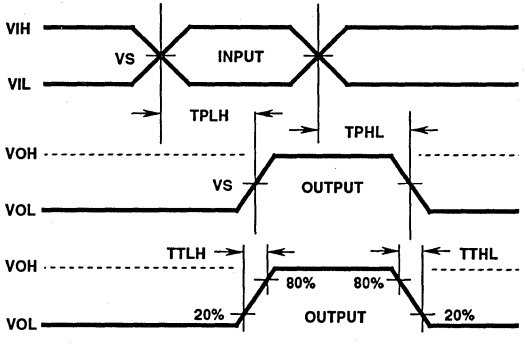
1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
1, 6, 8, 13	7	2 - 5, 9 - 12, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

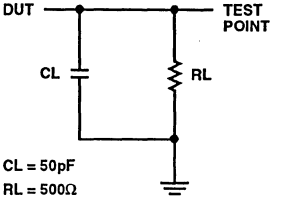
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
87 x 88 mils
2.20mm x 2.24mm

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

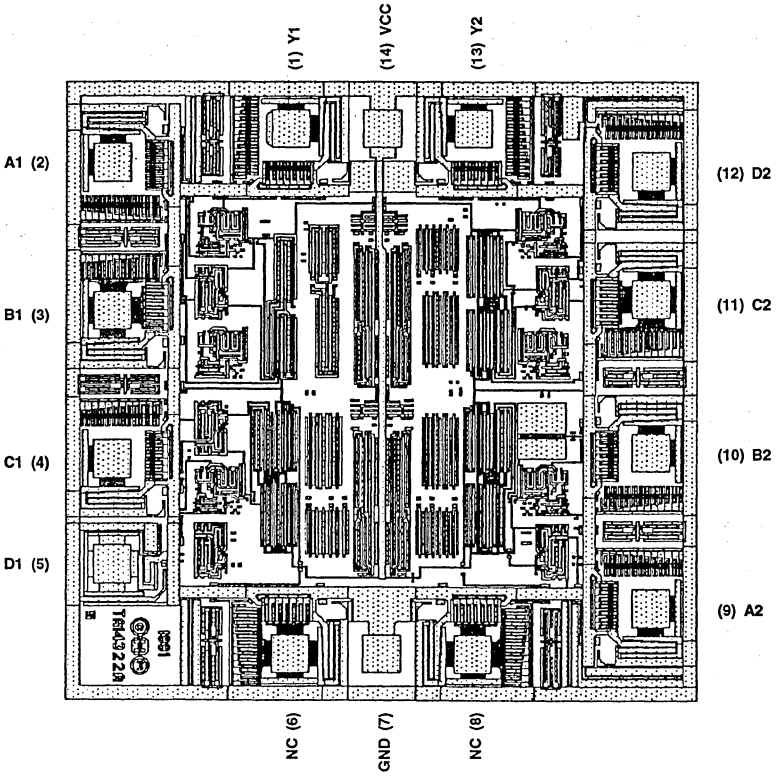
DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 mils x 4 mils

Metallization Mask Layout

HCTS4002MS



HARRIS SEMICONDUCTOR

HCTS7266MS

Radiation Hardened Quad 2-Input Exclusive NOR Gate

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Rate 2 x 10^{-9} Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = 2.0V Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

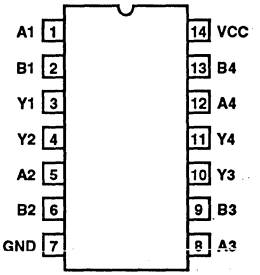
The Harris HCTS7266MS is a Radiation Hardened quad 2-Input exclusive NOR Gate. A logic level high on either one of the inputs (A or B) will force the output (y) low. A high on both inputs, or a low on both inputs will force the output to a logic high.

The HCTS7266MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family with TTL input compatibility.

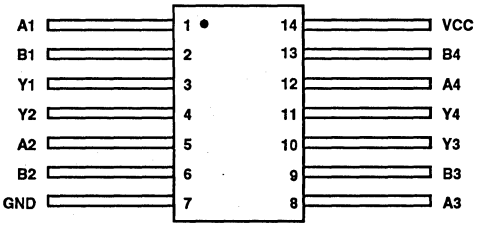
The HCTS7266MS is supplied in a 14 lead Ceramic flatpack (K suffix) or a Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 CDFP3-F14, LEAD FINISH C
TOP VIEW

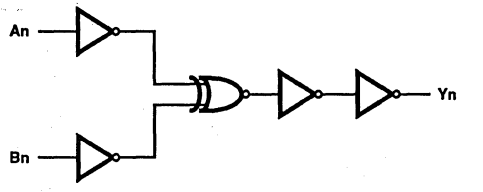


Truth Table

INPUTS		OUTPUTS
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

NOTE: L = Logic Level Low, H = Logic level High

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3384

Absolute Maximum Ratings

Supply Voltage . . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input. . . . . ±10mA
DC Drain Current, Any One Output. . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +265°C
Junction Temperature . . . . . +175°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 500ns Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Delta ICC	ΔICC	VCC = 5.5V, VIN = VCC or GND 1 Input = 2.4V	1	+25°C	-	1.6	mA
			2, 3	+125°C, -55°C	-	3.2	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V (Note 2)	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V (Note 2)	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.80V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.80V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.80V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.80V (Note 3)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. Force/Measure functions may be interchanged.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Input to Output	TPHL	VCC = 4.5V, VIH = 3.0V VIL = 0V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns
	TPLH	VCC = 4.5V, VIH = 3.0V VIL = 0V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	29	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, VIH = 5.0V, VIL = 0.0V, F = 1MHz	1	+25°C	Typical 20		pF
			1	+125°C	Typical 30		pF
Input Capacitance	CIN	VCC = 5.0V, VIH = 5.0V, VIL = 0.0V, F = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	1	15	ns
			1	+125°C, -55°C	1	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	1M RAD LIMITS MIN	1M RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Delta ICC	ΔICC	VCC = 5.5V, VIN = VCC or GND 1 Input = 2.4V	+25°C	-	3.2	-	3.2	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC-0.4V, VIL = 0V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	μA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.80V @ 200K RAD, VIL = 0.30V @ 1M RAD (Note 3)	+25°C	-	-	-	-	-
Propagation Delay Input to Outputt	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	22	2	28	ns
Propagation Delay Input to Output	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	29	2	37	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	+3	µA
IOL/IOH	-15	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
3, 4, 10, 11	1, 2, 5, 6, 7, 8, 9, 12, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 4, 10, 11	7	-	1, 2, 4, 5, 8, 9, 12, 13, 14	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	7	3, 4, 10, 11	14	1, 5, 8, 12	2, 6, 9, 13

NOTES:

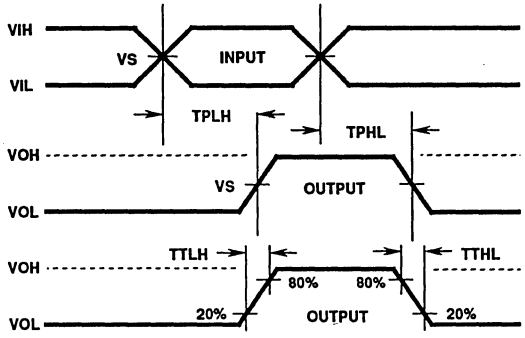
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

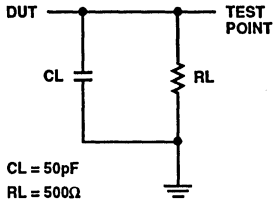
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



7 LOGIC

Die Characteristics

DIE DIMENSIONS:
84 x 84 mils
2.20 x 2.24mm

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

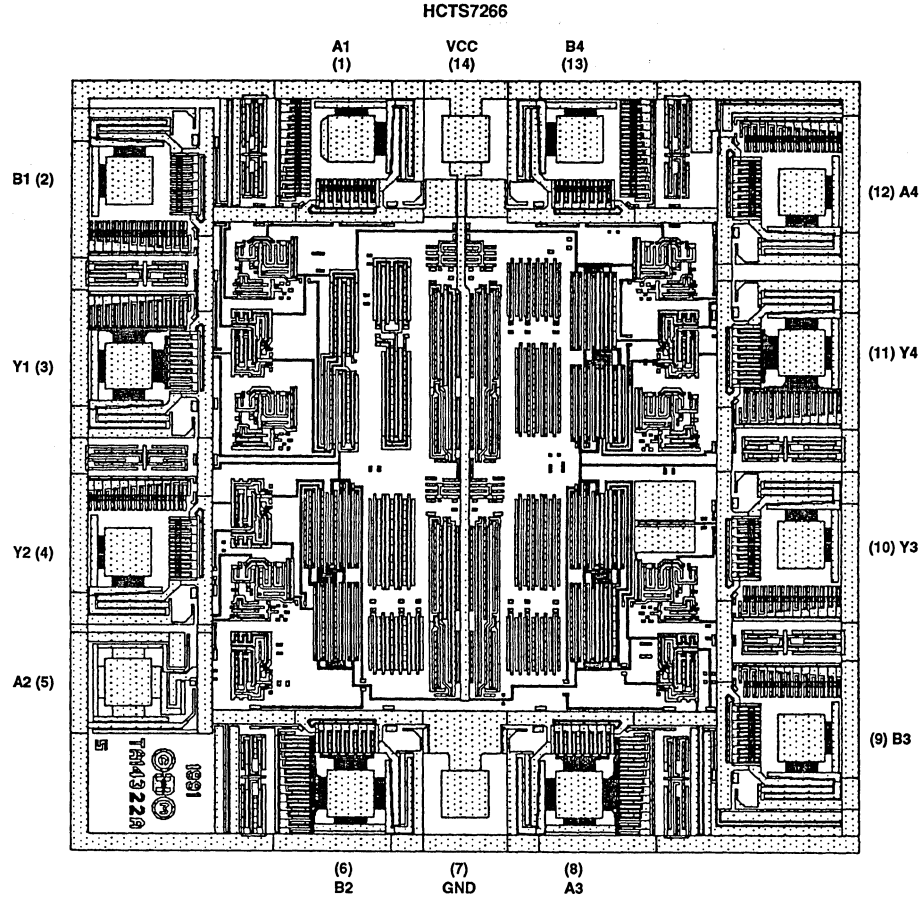
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4mm

Metallization Mask Layout



CD4000 MS Screening

Wafer Lot Acceptance	(All Lots)	Method 5007 (Includes SEM)
Radiation Verification	(Each Wafer)	Method 1019, 4 Samples/Wafer, 0 Rejects
Nondestructive Bond Pull	100%	Method 2023
Internal Visual Inspection	100%	Method 2010
Temperature Cycling	100%	Method 1010 Condition C (-65°C to +150°C)
Constant Acceleration	100%	
PIND Testing	100%	
External Visual Inspection	100%	
Serialization	100%	
Initial Electrical Test	100%	
Static Burn-In I	100%	Method 1015, 24 Hours, +125°C Minimum
Interim Electrical Test I	100%	(Note 1)
Static Burn-In II	100%	Method 1015, 24 Hours, +125°C Minimum
Interim Electrical Test II	100%	(Note 1)
Dynamic Burn-In	100%	Method 1015, 240 Hours, +125°C or Equivalent
Interim Electrical Test III	100%	(Note 1)
Final Electrical Test	100%	
Fine and Gross Seal	100%	Method 1014
Radiographics	100%	Method 2012 (2 Views)
External Visual	100%	Method 2009
Group A (All Tests)		Method 5005 (Class S)
Group B (Optional)		Method 5005 (Class S) (Note 2)
Group D (Optional)		Method 5005 (Class S) (Note 2)
CSI and/or GSI (Optional)		(Note 2)
Data Package Generation		(Note 3)

NOTES:

1. Failure from interim electrical tests I and II are combined for determining PDA (PDA = 5% for subgroups 1, 7 and delta failures combined, PDA = 3% for subgroup 7 failures). Interim electrical tests III PDA (PDA = 5% for subgroups 1, 7 and delta failures combined, PDA = 3% for subgroup 7 failures.
2. These steps are optional, and should be listed on the purchase order if required.
3. Data Package Contents:
   Cover Sheet (P.O. #, Customer #, Lot Data Code, Harris #, Lot #, Quantity.
   Certificate of Conformance (as found on shipper).
   Lot Serial Number Sheet (Good Unit(s), Serial # and Lot #).
   Variables Data (All Read, Record and Delata Operations).
   Group A Attributes Data Summary.
   Wafer Lot Acceptance Report (Method 5007) to include SEM photos. NOTE: SEM photos to include % of step coverage.
   X-Ray Report and file(s), including parameter measurements.
   GAMMA Radiation Report with initial shipment of devices from the same wafer lot; Containing a cover page, Disposition, Rad Dose, Lot #, Test Package, Spec #(s), Test Equipment, etc.
   Irradiation Read and Record data will be on file at Harris.

HARRIS SEMICONDUCTOR

CD14538BMS

CMOS Dual Precision Monostable Multivibrator

December 1992

Features

- High-Voltage Type (20V Rating)
- Retriggerable/Resettable Capability
- Trigger and Reset Propagation Delays Independent of RX, CX
- Triggering From Leading or Trailing Edge
- Q and $\overline{Q}$ Buffered Outputs Available
- Separate Resets
- Wide Range of Output-Pulse Widths
- Schmitt-Trigger Input Allows Unlimited Rise and Fall Times On +TR and -TR Inputs
- 100% Tested For Maximum Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package-Temperature Range:
  - 100nA at 18V and +25°C
- Noise Margin (Full Package-Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- 5V, 10V and 15V Parametric Ratings
- Standardized Symmetrical Output Characteristics
- Meets All Requirements of JEDEC Tentative Standards No. 13B, "Standard Specifications for Description of "B" Series CMOS Device's

Applications

- Pulse Delay and Timing
- Pulse Shaping

Description

CD14538BMS dual precision monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

An external resistor (R_X) and an external capacitor (C_X) control the timing and accuracy for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of R_X and C_X. Precision control of output pulse widths is achieved through linear CMOS techniques.

Leading-edge-triggering (+TR) and trailing-edge-triggering (-TR) inputs are provided for triggering from either edge of an input pulse. An unused +TR input should be tied to VSS. An unused -TR input should be tied to VDD. A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to VDD. However, if an entire section of the CD14538BMS is not used, its inputs must be tied to either VDD or VSS. See Table 1.

In normal operation the circuit retriggers (extends the output pulse one period) on the application of each new trigger pulse. For operation in the non-retriggerable mode, $\overline{Q}$ is connected to -TR when leading-edge triggering (+TR) is used or Q is connected to +TR when trailing-edge triggering (-TR) is used. The time period (T) for this multivibrator can be calculated by: $T = R_X C_X$.

The minimum value of external resistance, R_X is 4KΩ. The minimum and maximum values of external capacitance, C_X, are 0pF and 100μF, respectively.

The CD14538BMS is interchangeable with type MC14538 and is similar to and pin-compatible with the CD4098B* and CD4538B**.

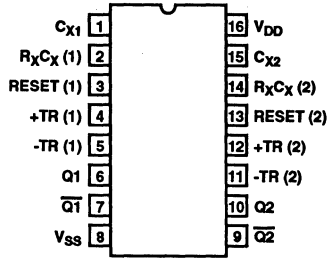
* $T = 0.5\ R_X C_X$ for $C_X \geq 1000$pF.
* $T = R_X C_X$; C_X min = 5000pF.

The CD14538BMS is supplied in these 16-lead outline packages:

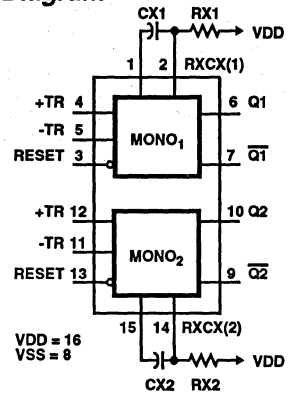
Braze Seal DIP	H4X
Frit Seal DIP	H1L
Ceramic Flatpack	H6W

Pinout

CD14538BMS
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3192

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (Note 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay +TR or -TR to Q or $\overline{Q}$	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Propagation Delay Reset to Q or $\overline{Q}$	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL1	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay +TR OR -TR to Q or $\overline{Q}$	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	300	ns
		VDD = 15V	1, 2, 3	+25°C	-	220	ns
Propagation Delay Reset to Q or $\overline{Q}$	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	250	ns
		VDD = 15V	1, 2, 3	+25°C	-	190	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Output Pulse Width Q or $\overline{Q}$ C_X =.002µF, R_X = 100K	TW	VDD = 5V	1, 2, 3	+25°C	-	230	µs
		VDD = 10V	1, 2, 3	+25°C	-	232	µs
		VDD = 15V	1, 2, 3	+25°C	-	234	µs
Output Pulse Width C_X = 0.1µF R_X = 100K	TW		1, 2, 3	+25°C	-	10.5	ms
		VDD = 10V	1, 2, 3	+25°C	-	10.6	ms
		VDD = 15V	1, 2, 3	+25°C	-	10.6	ms
Output Pulse Width C_X = 10µF R_X = 100K	TW	VDD = 5V	1, 2, 3	+25°C	-	1.06	s
		VDD = 10V	1, 2, 3	+25°C	-	1.06	s
		VDD = 15V	1, 2, 3	+25°C	-	1.07	s
Minimum Retrigger Time	TRR	VDD = 5V	1, 2, 3	+25°C	0	-	ns
		VDD = 10V	1, 2, 3	+25°C	0	-	ns
		VDD = 15V	1, 2, 3	+25°C	0	-	ns
Minimum Input Pulse Width +TR, -TR, or Reset	TW	VDD = 5V	1, 2, 3	+25°C	-	140	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	6, 7, 9, 10	1, 3 - 5, 8, 11 - 13, 15	2, 14, 16			
Static Burn-In 2 (Note 1)	6, 7, 9, 10	1, 8, 15	2 - 5, 11 - 13, 14, 16			
Dynamic Burn-In (Note 1)	-	1, 4, 8, 12, 15	2, 14, 16	6, 7, 9, 10	5, 11	3, 13

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS (Continued)

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Irradiation (Note 2)	2, 6, 7, 9, 10, 14	1, 8, 15	3 - 5, 11 - 13, 16			

NOTE:

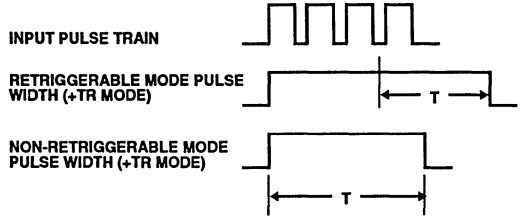
1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

TABLE 9. FUNCTIONAL TERMINAL CONNECTIONS

FUNCTION	VDD TO TERM #		VSS TO TERM #		INPUT PULSE TO TERM #		OTHER CONNECTIONS	
	MONO1	MONO2	MONO1	MONO2	MONO1	MONO2	MONO1	MONO2
Leading-Edge Trigger/ Retriggerable	3, 5	11, 13			4	12		
Leading-Edge Trigger/ Non-Retriggerable	3	13			4	12	5 - 7	11 - 9
Trailing-Edge Trigger/ Retriggerable	3	13	4	12	5	11		
Trailing-Edge Trigger/ Non-Retriggerable	3	13			5	11	4 - 6	12 - 10

NOTE:

1. A triggerable one-shot multivibrator has an output pulse width which is extended one full time period (T) after application of the last trigger pulse.
2. A non-triggerable one-shot multivibrator has a time period (T) referenced from the application of the first trigger pulse.



Power-Down Mode

During a rapid power-down condition, as would occur with a power-supply short circuit or with a poorly filtered power supply, the energy stored in C_X could discharge into Pin 2 or 14. To avoid possible device damage in this mode, when C_X is ≥ 0.5 microfarad, a protection diode with a 1-ampere or higher rating (1N5395 or equivalent) and a separate ground return for C_X should be provided as shown in Figure 1.

An alternate protection method is shown in Figure 2, where a 51-ohm current-limiting resistor is inserted in series with C_X. Note that a small pulse width decrease will occur however, and R_X must be appropriately increases to obtain the originally desired pulse width.

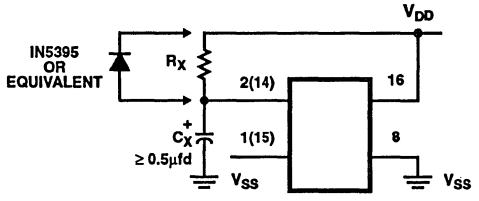


FIGURE 1. RAPID POWER-DOWN PROTECTION CIRCUIT

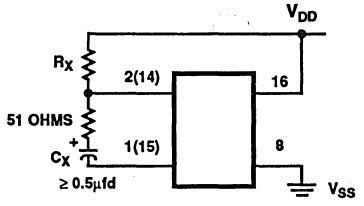


FIGURE 2. ALTERNATE RAPID POWER-DOWN PROTECTION CIRCUIT

7 LOGIC

Logic Diagram

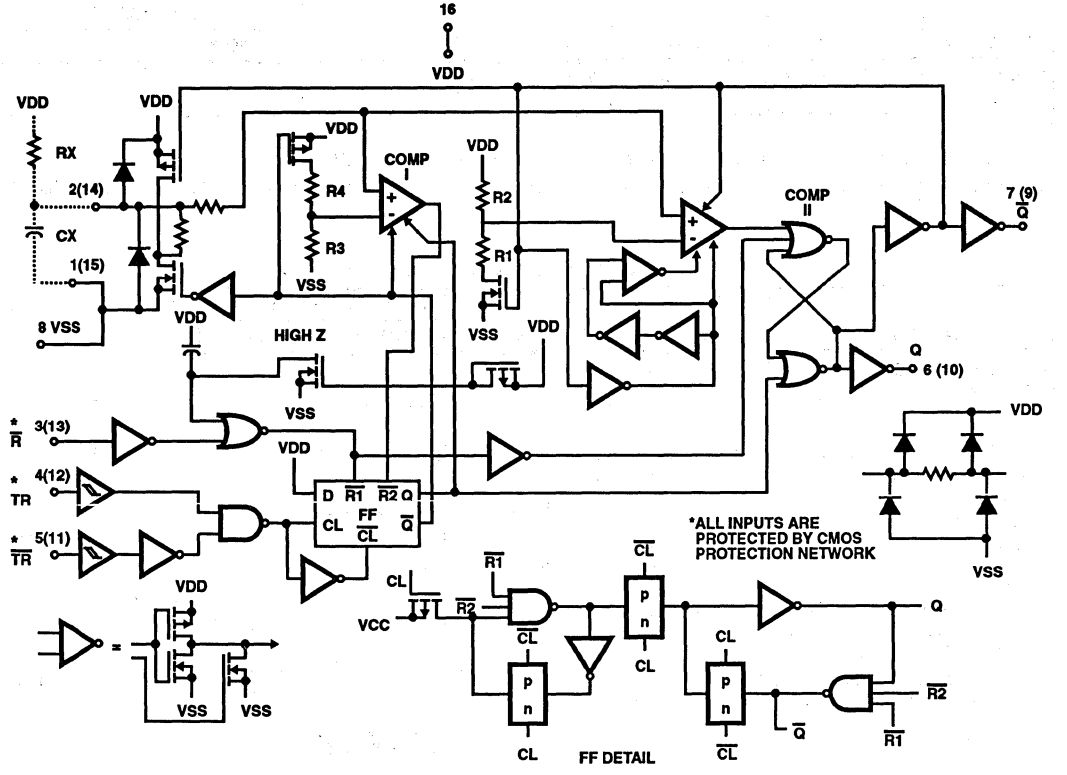


FIGURE 3. 1/2 OF DEVICE SHOWN

Typical Performance Characteristics

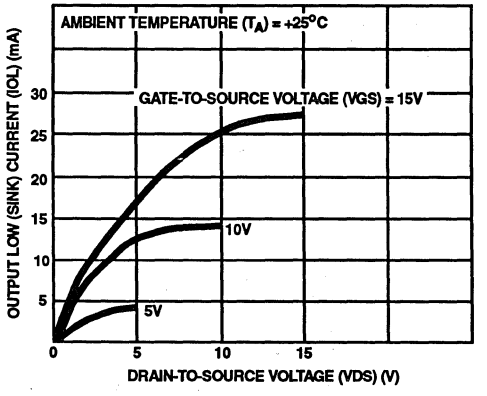


FIGURE 4. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

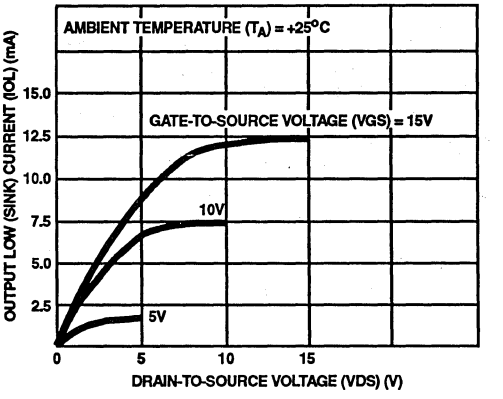


FIGURE 5. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

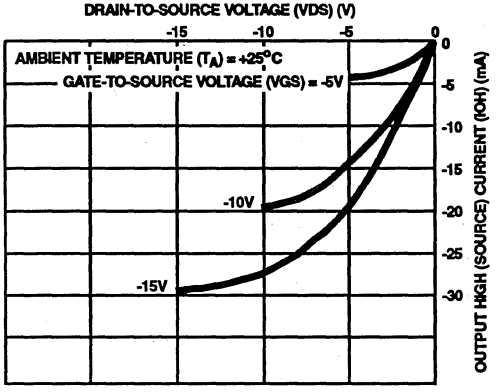


FIGURE 6. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

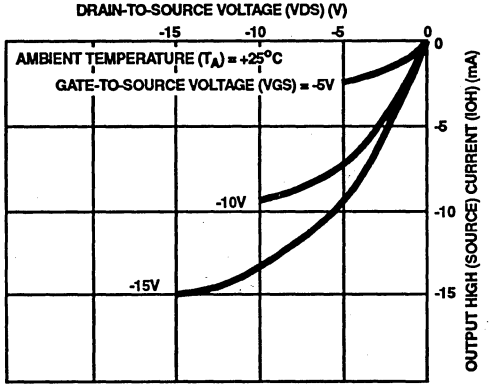


FIGURE 7. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

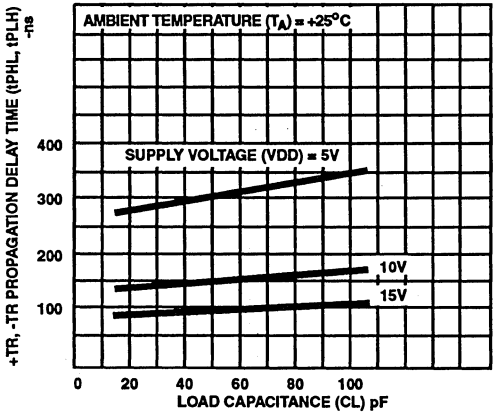


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (+TR OR -TR TO Q OR $\overline{Q}$)

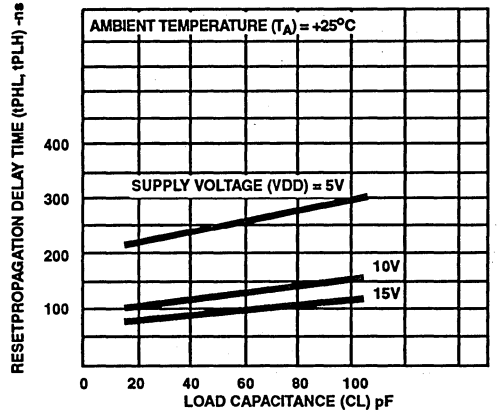


FIGURE 9. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (RESET TO Q OR $\overline{Q}$)

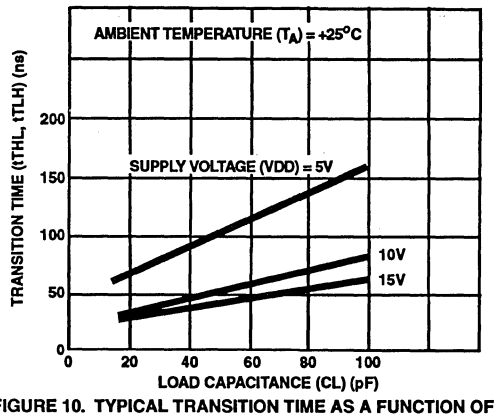


FIGURE 10. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

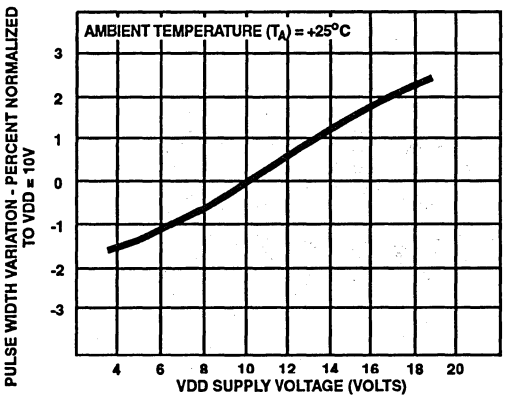


FIGURE 11. TYPICAL PULSE-WIDTH VARIATION AS A FUNCTION OF SUPPLY VOLTAGE

Typical Performance Characteristics (Continued)

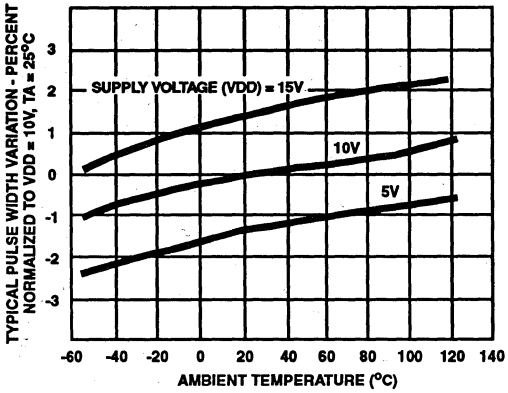


FIGURE 12. TYPICAL PULSE-WIDTH VARIATION AS A FUNCTION OF TEMPERATURE (RX = 100 KΩ, CX = 0.1μF)

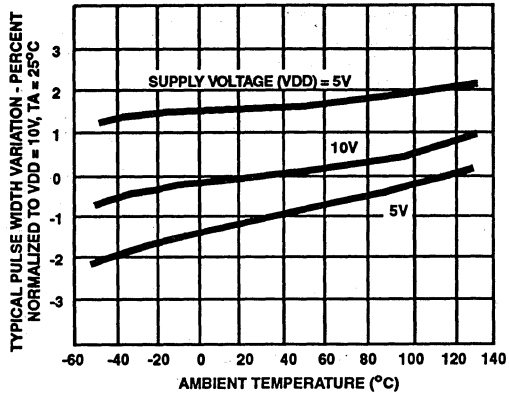


FIGURE 13. TYPICAL PULSE-WIDTH VARIATION AS A FUNCTION OF TEMPERATURE (RX = 100 KΩ, CX = 2000pF)

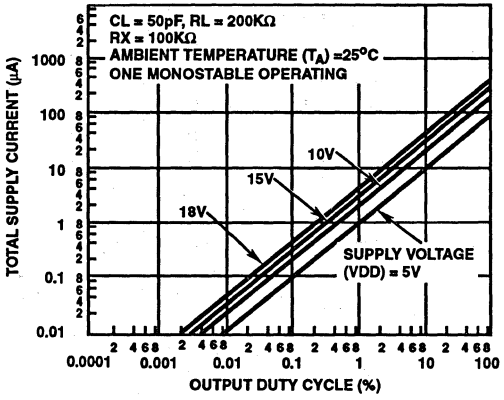


FIGURE 14. TYPICAL TOTAL SUPPLY CURRENT AS A FUNCTION OF OUTPUT DUTY CYCLE

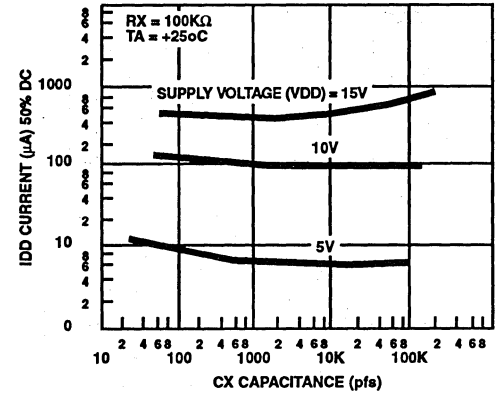
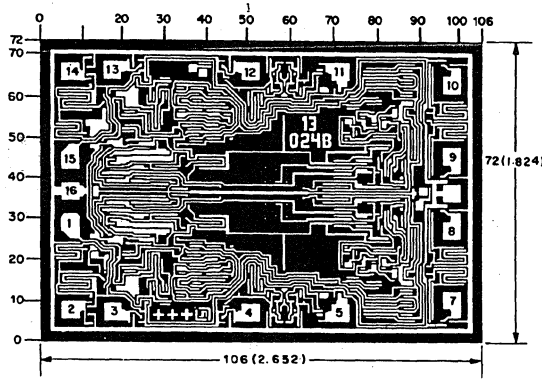


FIGURE 15. TYPICAL TOTAL SUPPLY CURRENT AS A FUNCTION OF LOAD CAPACITANCE

Chip Dimension and Pad Layout



METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

CD4000BMS, CD4001BMS CD4002BMS, CD4025BMS

December 1992

CMOS NOR Gate

Features

- High-Voltage Types (20V Rating)
- Propagation Delay Time = 60ns (typ.) at CL = 50pF, VDD = 10V
- Buffered Inputs and Outputs
- Standard Symmetrical Output Characteristics
- 100% Tested for Maximum Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package-Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standards No. 13B, "Standard Specifications for Description of "B" Series CMOS Device's

Description

CD4000BMS - Dual 3 Plus Inverter

CD4001BMS - Quad 2 Input

CD4002BMS - Dual 4 Input

CD4025BMS - Triple 3 Input

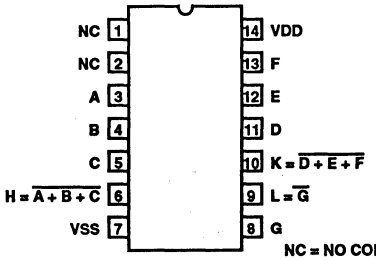
CD4000BMS, CD4001BMS, CD4002BMS, and CD4025BMS NOR gates provide the system designer with direct implementation of the NOR function and supplement the existing family of CMOS gates. All inputs and outputs are buffered.

The CD4000BMS, CD4001BMS, CD4002BMS and the CD4025BMS is supplied in these 14 lead outline packages:

	CD4000B	CD4001B	CD4002B	CD4025B
Braze Seal DIP	H4X	H4Q	H4Q	H4Q
Frit Seal DIP	H1B	H1B	H1B	H1B
Ceramic Flatpack	H3W	H3W	H3W	H3W

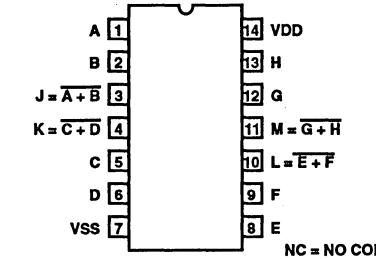
Pinouts

CD4000BMS
TOP VIEW



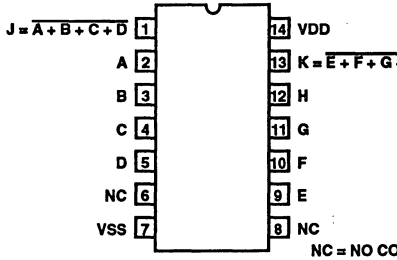
NC = NO CONNECTION

CD4001BMS
TOP VIEW



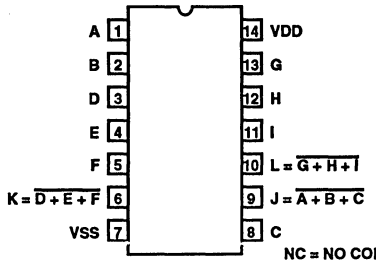
NC = NO CONNECTION

CD4002BMS
TOP VIEW



NC = NO CONNECTION

CD4025BMS
TOP VIEW



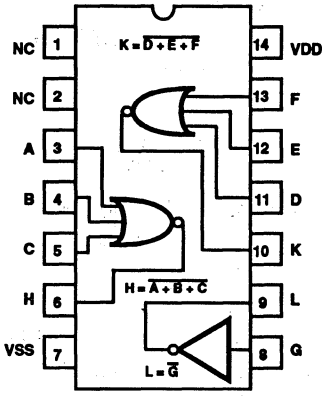
NC = NO CONNECTION

7 LOGIC

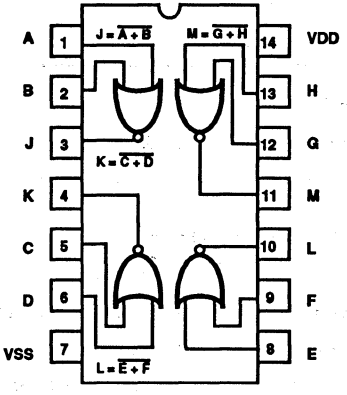
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3289

Functional Diagrams



CD4000BMS



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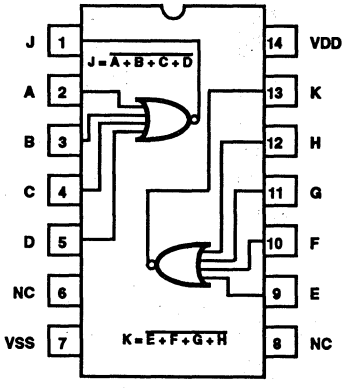

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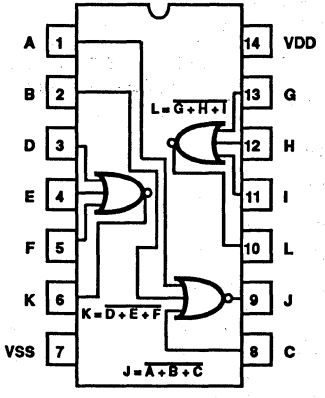


CD4025BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	0.5	µA
				2	+125°C	-	50	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	0.5	µA
Input Leakage	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	250	ns
			10, 11	+125°C, -55°C	-	338	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.25	µA
				+125°C	-	7.5	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	1.5	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	3.0	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	120	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	2.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - SSI	IDD	±0.1µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Final Test	100% 5004	2, 3, 8A, 8B, 10, 11	
Group A	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

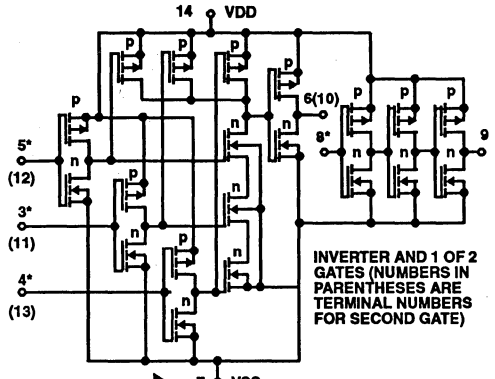
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

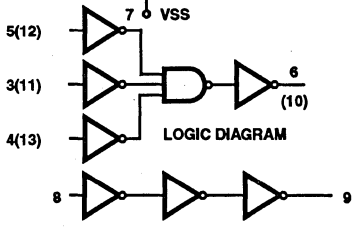
FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR 50kHz	OSCILLATOR 25kHz
PART NUMBER CD4000BMS						
Static Burn-In 1 Note 1	1, 2, 6, 9, 10	3 - 5, 7, 8, 11 - 13	14			
Static Burn-In 2 Note 1	1, 2, 6, 9, 10	7	3 - 5, 8, 11 - 14			
Dynamic Burn-In Note 1	1, 2	7	14	6, 9, 10	3 - 5, 8, 11 - 13	
Irradiation Note 2	1, 2, 6, 9, 10	7	3 - 5, 8, 11 - 14			
PART NUMBER CD4001BMS						
Static Burn-In 1 Note 1	3, 4, 10, 11	1, 2, 5 - 9, 12, 13	14			
Static Burn-In 2 Note 1	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12 - 14			
Dynamic Burn-In Note 1	-	7	14	3, 4, 10, 11	1, 2, 5, 6, 8, 9, 12, 13	
Irradiation Note 2	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12 - 14			
PART NUMBER CD4002BMS						
Static Burn-In 1 Note 1	1, 6, 8, 13	2 - 5, 7, 9 - 12	14			
Static Burn-In 2 Note 1	1, 6, 8, 13	7	2 - 5, 9 - 12, 14			
Dynamic Burn-In Note 1	6, 8	7	14	1, 13	2 - 5, 9 - 12	
Irradiation Note 2	1, 6, 8, 13	7	2 - 5, 9 - 12, 14			
PART NUMBER CD4025BMS						
Static Burn-In 1 Note 1	6, 9, 10	1 - 5, 7, 8, 11 - 13	14			
Static Burn-In 2 Note 1	6, 9, 10	7	1 - 5, 8, 11 - 14			
Dynamic Burn-In Note 1	-	7	14	6, 9, 10	1 - 5, 8, 11 - 13	
Irradiation Note 2	6, 9, 10	7	1 - 5, 8, 11 - 14			

NOTE:

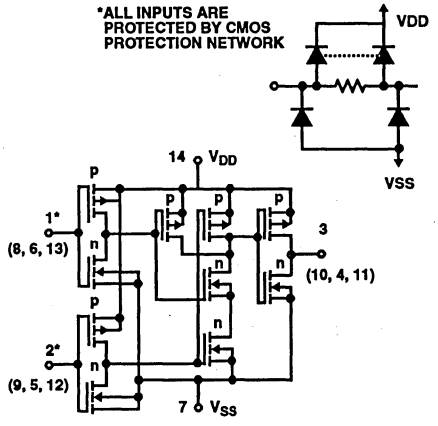
1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Schematic and Logic Diagrams

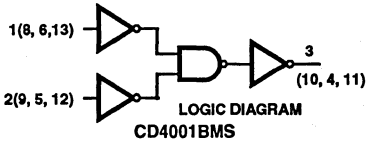




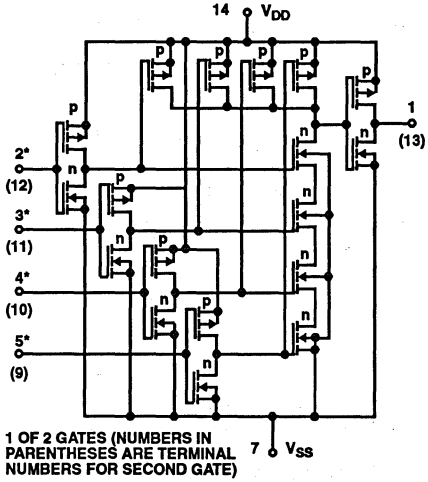
CD4000BMS

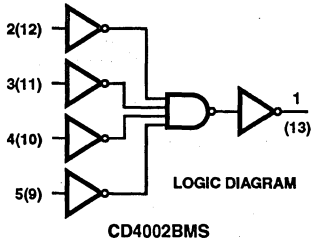


1 OF 4 GATES (NUMBERS IN PARANTHESES ARE TERMINAL NUMBERS FOR OTHER GATES)

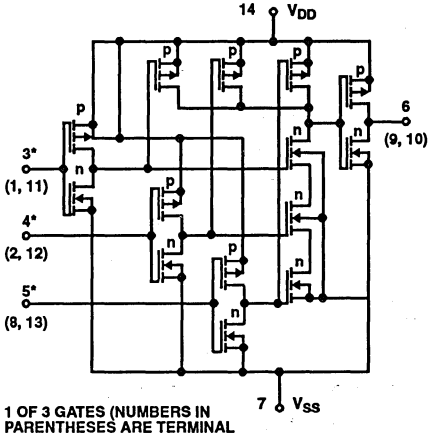


CD4001BMS





CD4002BMS



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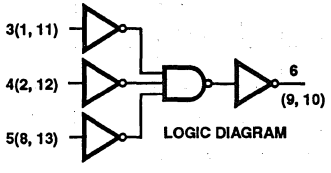


CD4025BMS

Typical Performance Characteristics

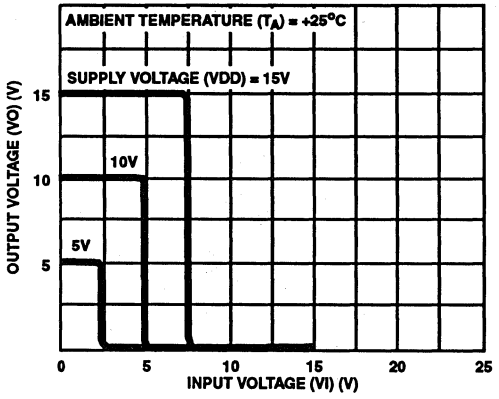


FIGURE 1. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS

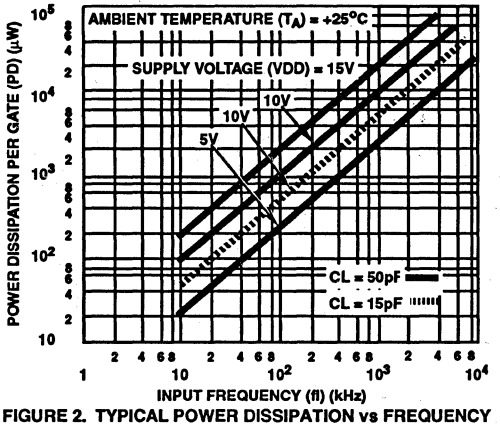


FIGURE 2. TYPICAL POWER DISSIPATION vs FREQUENCY

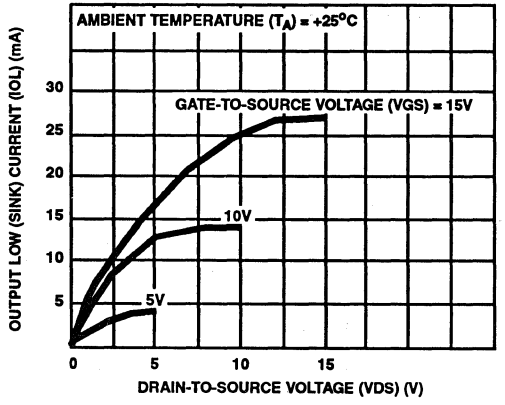


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

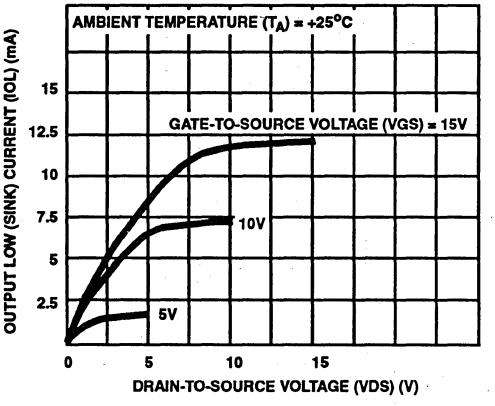


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

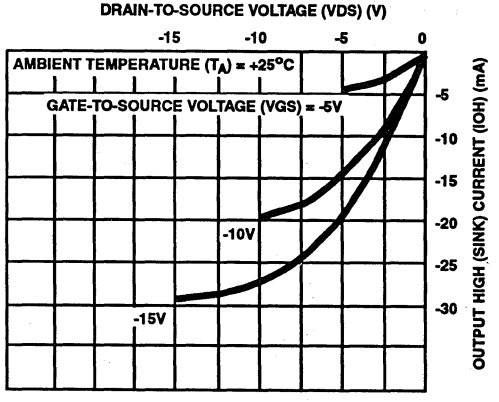


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

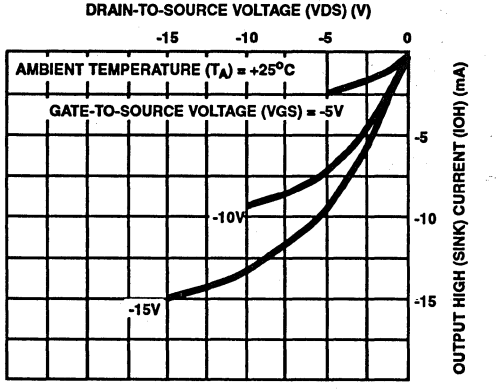


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

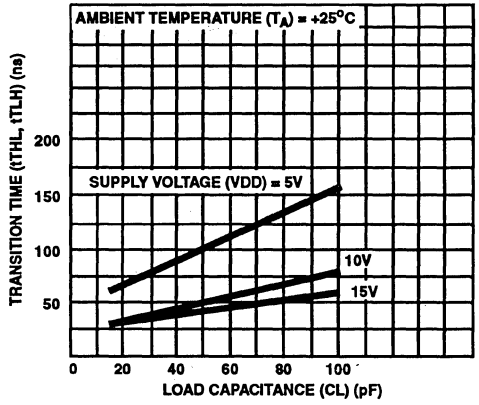


FIGURE 7. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

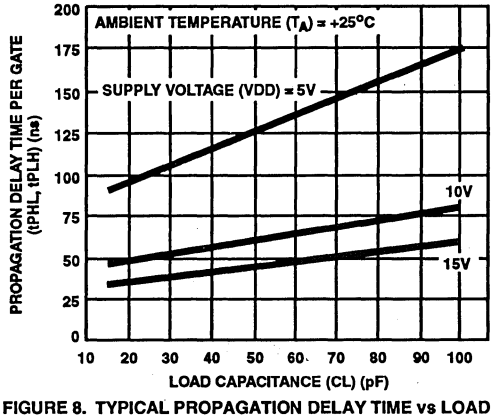
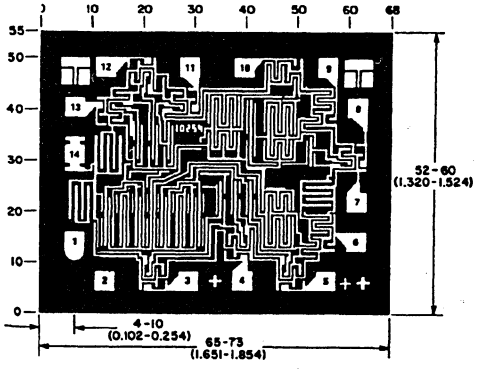
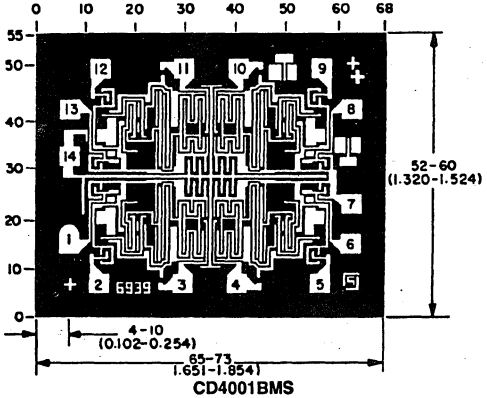


FIGURE 8. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE

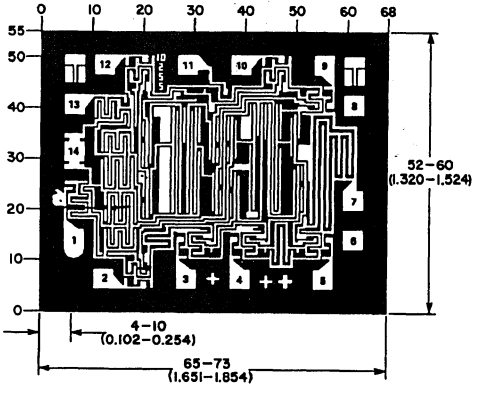
Chip Dimensions and Pad Layouts



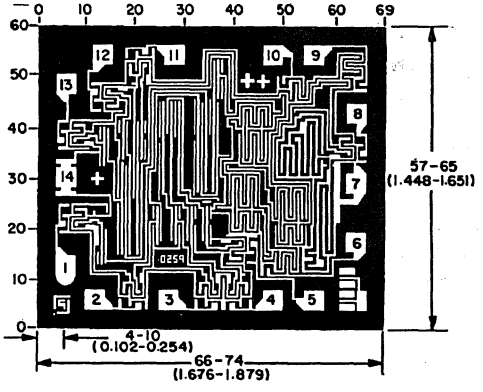
CD4000BMS



CD4001BMS



CD4002BMS



CD4025BMS

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

7 LOGIC

HARRIS SEMICONDUCTOR

CD4006BMS

December 1992

CMOS 18-Stage Static Register

Features

- High-Voltage Type (20V Rating)
- Fully Static Operation
- Shifting Rates Up to 12MHz at 10V (typ)
- Permanent Register Storage with Clock Line High or Low - No Information Recirculation Required
- 100% Tested for Quiescent Current at 20V
- Standardized, Symmetrical Output Characteristics
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package-Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Full Package-Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standards No. 13B, "Standard Specifications for Description of "B" Series CMOS Devices"

Applications

- Serial Shift Registers
- Frequency Division
- Time Delay Circuits

Description

CD4006BMS types are composed of 4 separate shift register sections: two sections of four stages and two sections of five stages with an output tap at the fourth stage. Each section has an independent single-rail data path.

A common clock signal is used for all stages. Data are shifted to the next stages on negative-going transitions of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages or single register sections of 10, 12, 13, 14, 16, 17 and 18 stages can be implemented using one CD4006BMS package. Longer shift register sections can be assembled by using more than one CD4006BMS.

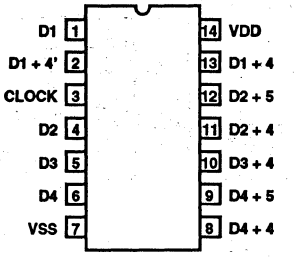
To facilitate cascading stages when clock rise and fall times are slow, an optional output (D1 + 4') that is delayed one-half clock-cycle, is provided (see Truth Table for Output from Term. 2).

The CD4006BMS is supplied in these 14 lead outline packages:

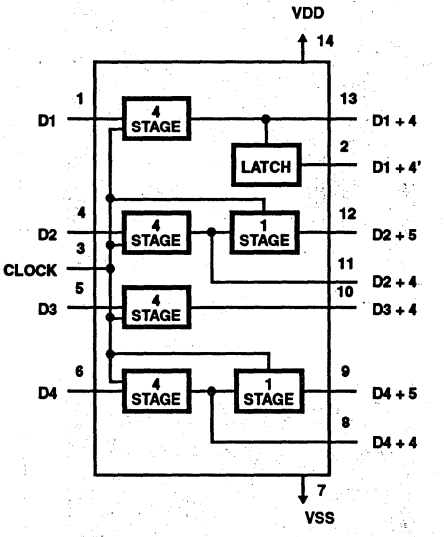
Braze Seal DIP	H4Q
Frit Seal DIP	H6D
Ceramic Flatpack	H4F

Pinout

CD4006BM
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3290

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range.....-55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG).....-65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V	9	+25°C	2.5	-	MHz
		VIN = VDD or GND	10, 11	+125°C, -55°C	1.85	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. 55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	160	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	5	-	MHz
		VDD = 15V	1, 2, 3	+25°C	7	-	MHz
Minimum Data Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	100	ns
		VDD = 10V	1, 2, 3	+25°C	-	50	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	180	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

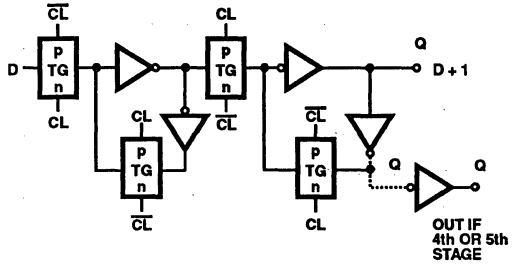
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	2, 8 - 13	1, 3 - 7	14			
Static Burn-In 2 Note 1	2, 8 - 13	7	1, 3 - 6, 14			
Dynamic Burn-In Note 1	2	7	14	8 - 13	3	1, 4 - 6
Irradiation Note 2	2, 8 - 13	7	1, 3 - 6, 14			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram and Truth Table



LOGIC DIAGRAM AND TRUTH TABLE (ONE REGISTER STAGE)

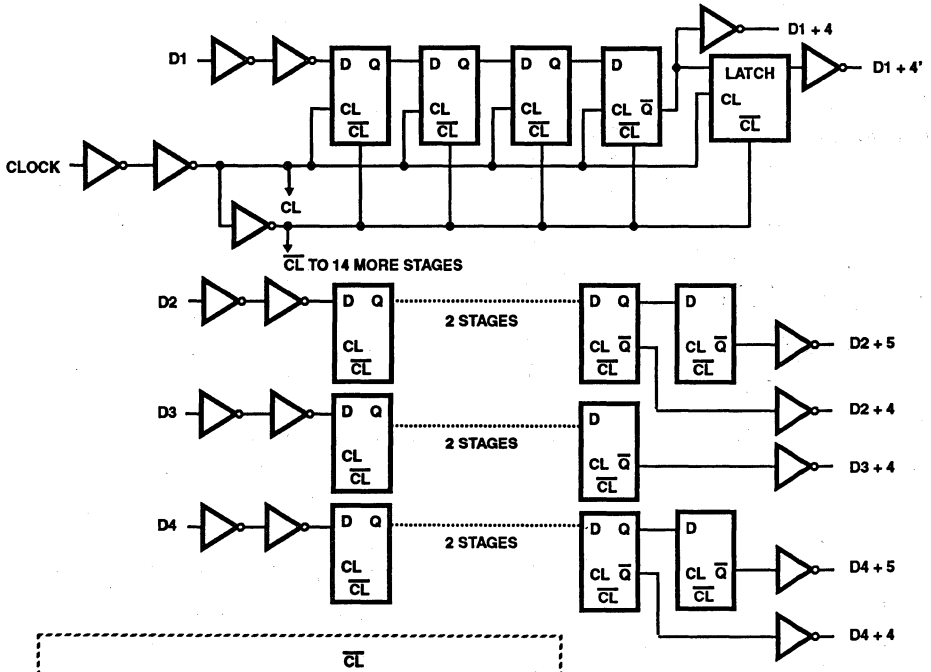
TRUTH TABEL FOR SHIFT REGISTER STAGE

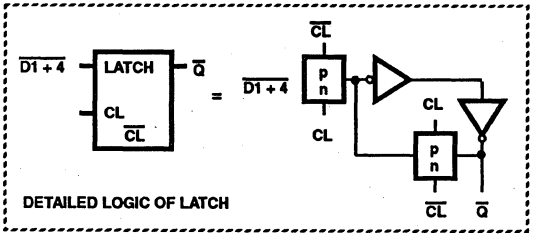
D	CL*	D + 1
0	↓	0
1	↓	1
X	↑	NC

TRUTH TABLE FOR OUTPUT FROM TERM 2

D1 + 4	CL*	D1 + 4'
0	↑	0
1	↑	1
X	↓	NC

1 = HIGH
0 = LOW
NC= NO CHANGE
X = DON'T CARE
* = LEVEL CHANGE





LOGIC DIAGRAM WITH DETAIL OF LATCH

Typical Performance Characteristics

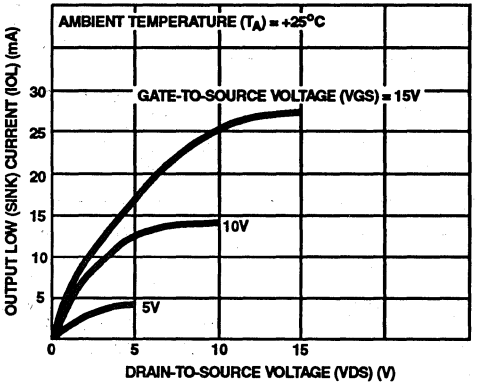


FIGURE 1. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

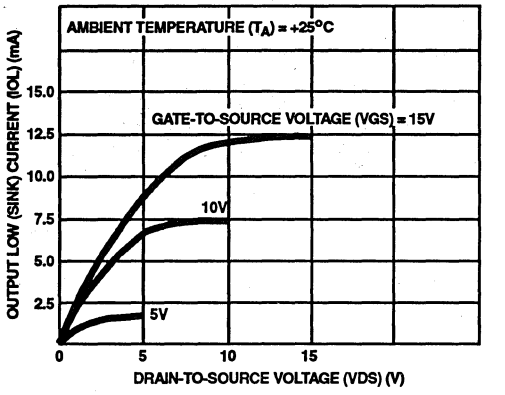


FIGURE 2. MIMIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

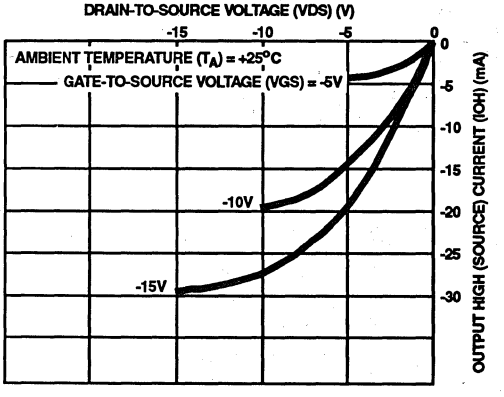


FIGURE 3. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

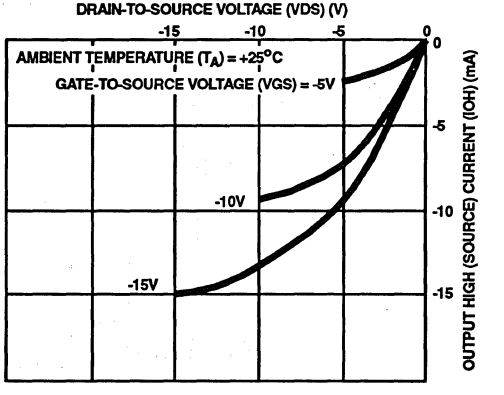


FIGURE 4. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

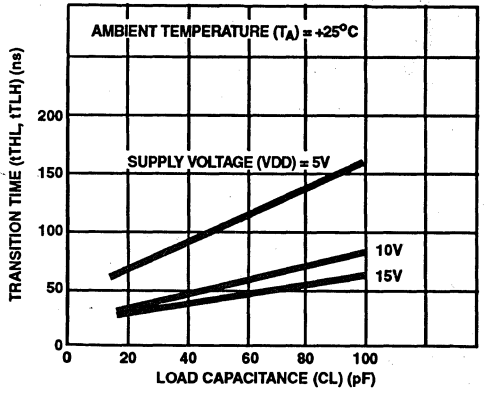


FIGURE 5. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

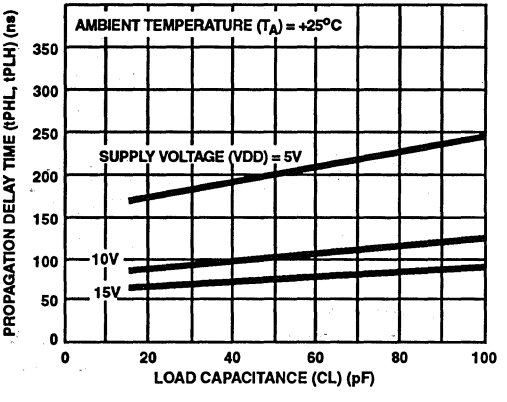


FIGURE 6. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

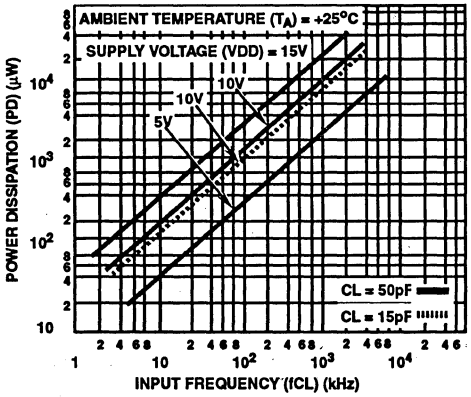
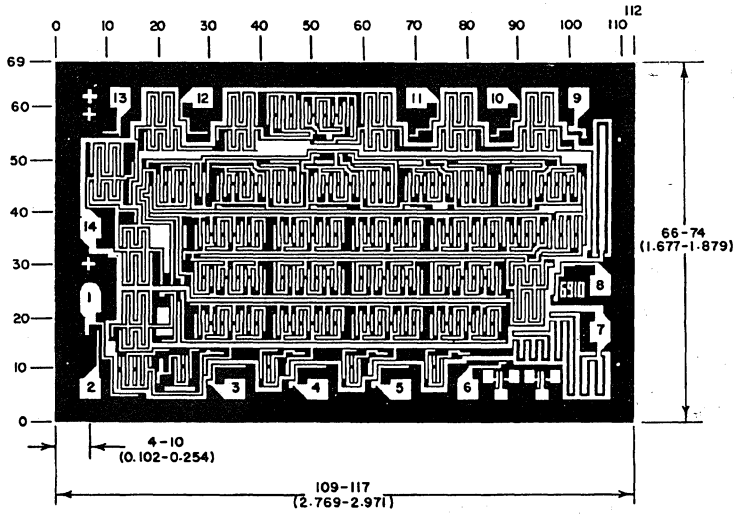


FIGURE 7. TYPICAL DYANAMIC POWER DISSIPATION AS A FUNCTION OF CLOCK FREQUENCY

Chip Dimensions and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4007UBMS

December 1992

CMOS Dual Complementary Pair Plus Inverter

Features

- High-Voltage Type (20V Rating)
- Standardized Symmetrical Output Characteristics
- Medium Speed Operation
  - tPHL, tPLH = 30 ns (typ) at 10V
- 100% Tested for Maximum Quiescent Current at 20V
- Meets All Requirements of JEDEC Tentative Standards No. 13B, "Standard Specifications for Description of "B" Series CMOS Devices"
- Maximum Input Current of 1μA at 18V Over Full Package-Temperature Range; 100nA at 18V and +25°C

Applications

- Extremely High-Input Impedance Amplifiers
- Shapers
- Inverters
- Threshold Detector
- Linear Amplifiers
- Crystal Oscillators

Description

CD4007BMS types are comprised of three n-channel and three p-channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits as shown in Figure 2.

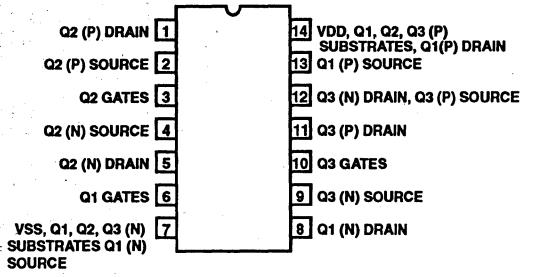
More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the various configurations listed.

The CD4007BMS is supplied in these 14 lead outline packages:

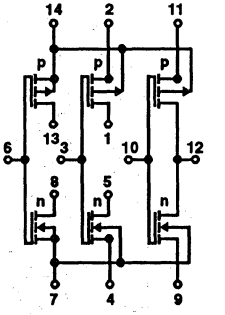
Braze Seal DIP	H4Q
Frit Seal DIP	H1B
Ceramic Flatpack	H3W

Pinout

CD4007UBMS
TOP VIEW



Functional Diagram



TERMINAL NO. 14 - VDD

TERMINAL NO. 7 - VSS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3291

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	0.5	µA
				2	+125°C	-	50	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	0.5	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.0	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	4.0	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	2.5	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	12.5	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	110	ns
			10, 11	+125°C, -55°C	-	149	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. 55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.25	µA
				+125°C	-	7.5	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	15	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	30	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	2	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	8	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	60	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	15.0	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	2.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - SSI	IDD	±0.1µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Final Test	100% 5004	2, 3, 8A, 8B, 10, 11	
Group A	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	1, 5, 8, 12, 13	3, 4, 6, 7, 9, 10	2, 11, 14			
Static Burn-In 2 Note 1	1, 5, 8, 12, 13	4, 7, 9	2, 3, 6, 10, 11, 14			
Dynamic Burn-In Note 1	-	4, 7, 9	2, 11, 14	1, 5, 8, 12, 13	3, 6, 10	-
Irradiation Note 2	1, 5, 8, 12, 13	4, 7, 9	2, 3, 6, 10, 11, 14			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ±5%, VDD = 18V ±0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ±0.5V

Schematic Diagram

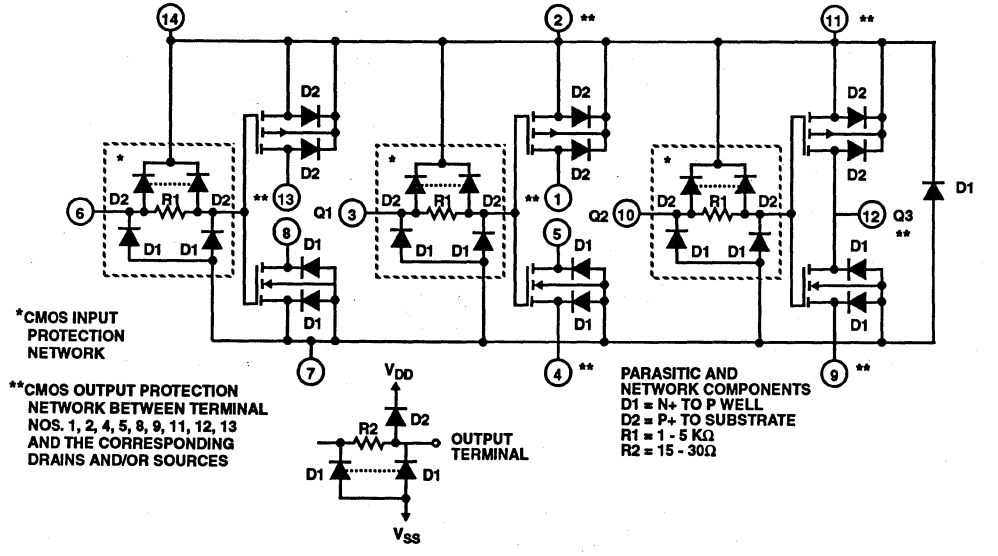
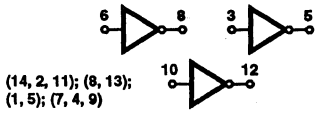
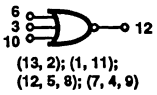


FIGURE 1. DETAILED SCHEMATIC DIAGRAM OF CD4007UBMS SHOWING INPUT, OUTPUT, AND PARASITIC DIODES

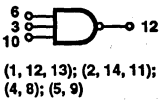
Logic Circuits



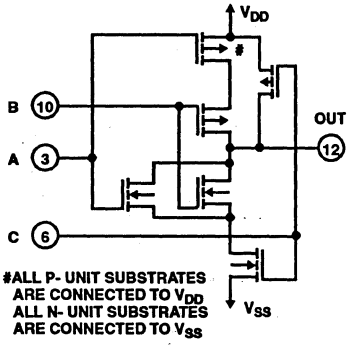
a) TRIPLE INVERTERS

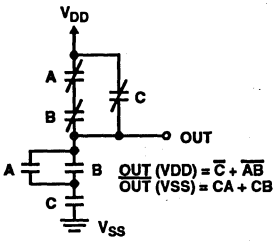


b) 3 - INPUT NOR GATE

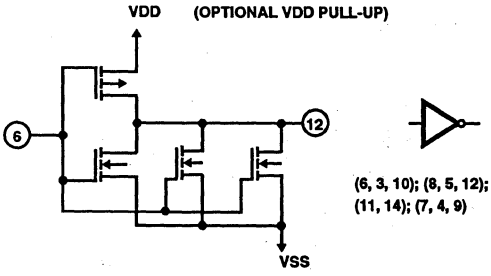


c) 3 - INPUT NAND GATE

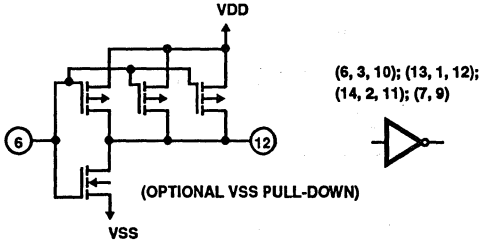




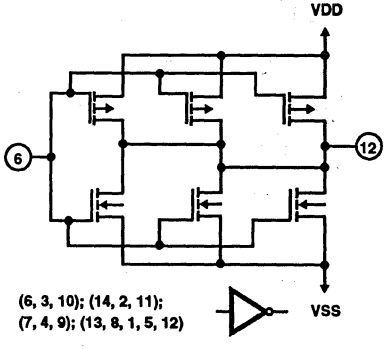
d) TREE (RELAY) LOGIC



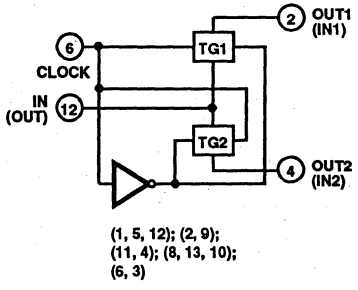
e) HIGH SINK-CURRENT DRIVER



f) HIGH SOURCE-CURRENT DRIVER



g) HIGH SINK - AND SOURCE-CURRENT DRIVER



h) DUAL BI-DIRECTIONAL TRANSMISSION GATING

7 LOGIC

Typical Performance Characteristics

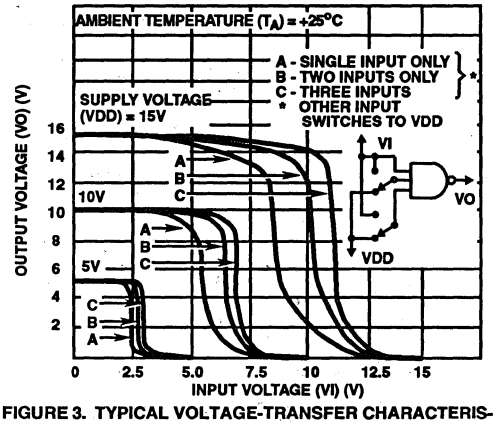


FIGURE 3. TYPICAL VOLTAGE-TRANSFER CHARACTERISTICS FOR NAND GATE

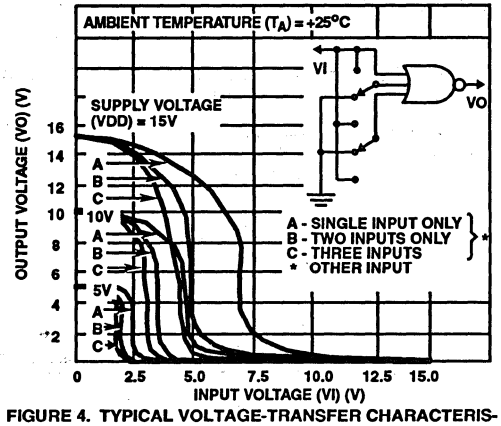


FIGURE 4. TYPICAL VOLTAGE-TRANSFER CHARACTERISTICS FOR NOR GATE

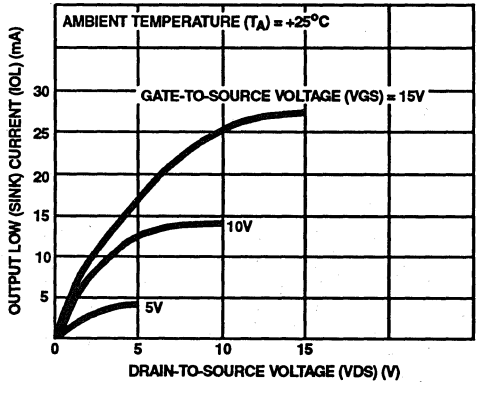


FIGURE 5. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

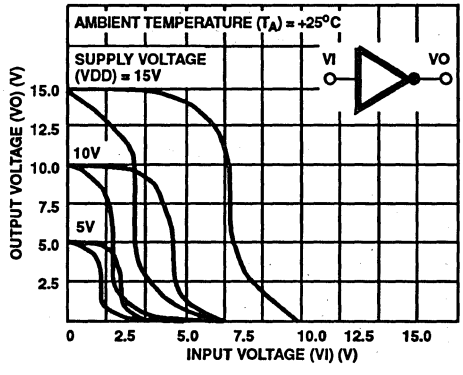


FIGURE 6. MINIMUM AND MAXIMUM VOLTAGE-TRANSFER CHARACTERISTICS FOR INVERTER

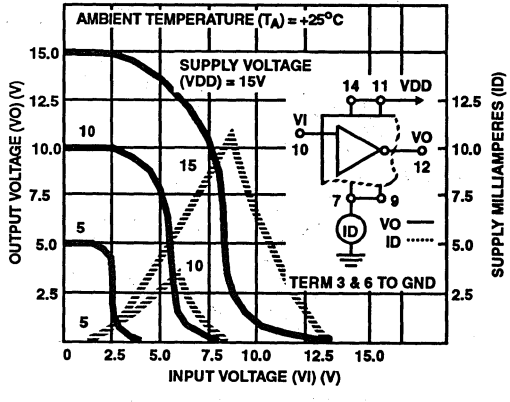


FIGURE 7. TYPICAL CURRENT AND VOLTAGE-TRANSFER CHARACTERISTICS FOR INVERTER

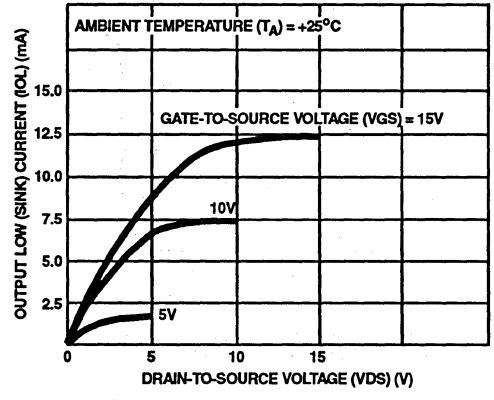


FIGURE 8. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

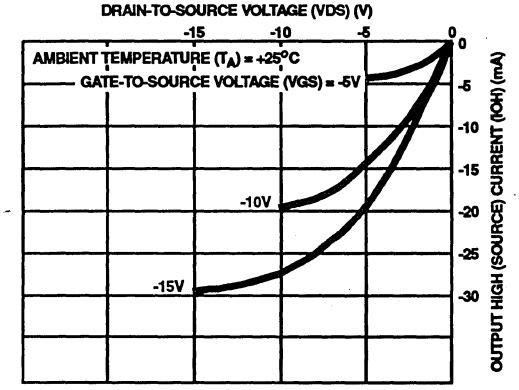


FIGURE 9. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

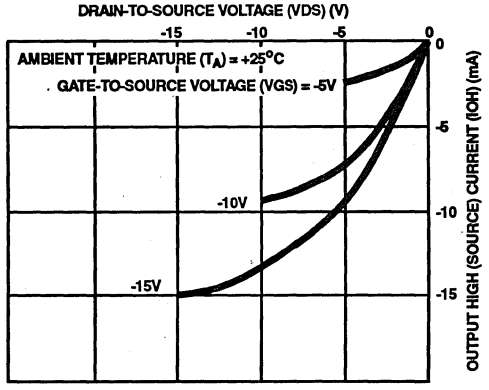


FIGURE 10. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

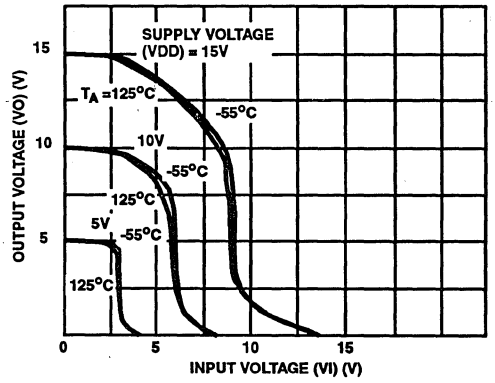


FIGURE 11. TYPICAL VOLTAGE-TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE

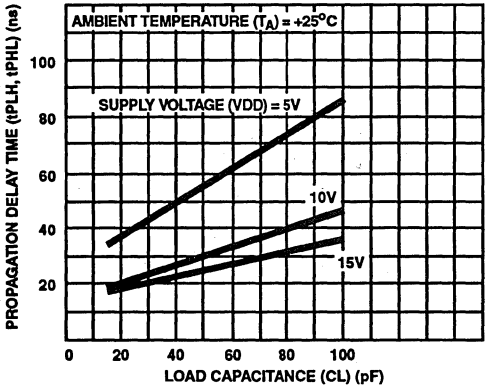


FIGURE 12. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE

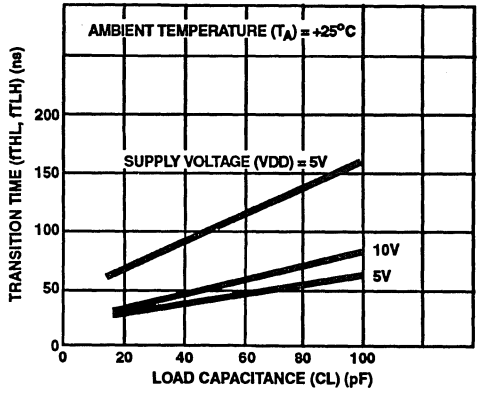


FIGURE 13. TYPICAL TRANSISTION TIME vs LOAD CAPACITANCE

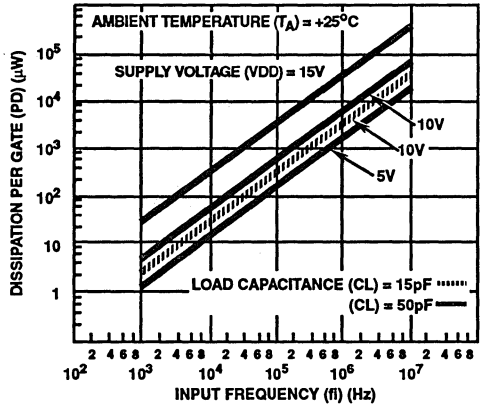
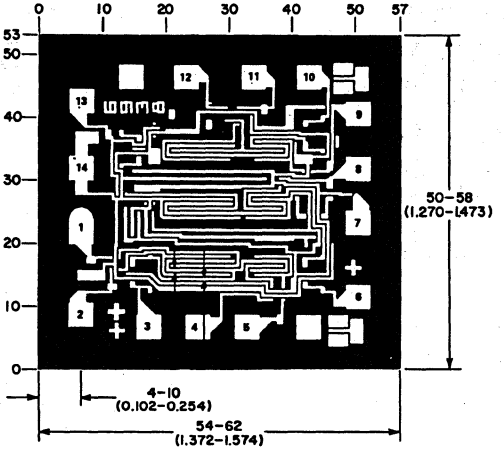


FIGURE 14. TYPICAL DISSIPATION vs FREQUENCY CHARACTERISTICS

Chip Dimension and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4008BMS

CMOS 4-Bit Full Adder With Parallel Carry Out

December 1992

Features

- High-Voltage Type (20V Rating)
- 4 Sum Outputs Plus Parallel Look-ahead Carry-Output
- High-Speed Operation - Sum In-To-Sum Out, 160ns Typ; Carry In-To-Carry Out, 5ns Typ. At VDD = 10V, CL=50pF
- Standardized Symmetrical Output Characteristics
- 100% Tested For Quiescent Current At 20V
- Maximum Input Current of 1μa at 18V Over Full Package-Temperature Range;
  - 100nA at 18V and 25°C
- Noise Margin (Over Full Package Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Binary Addition/Arithmetic Units

Description

CD4008BMS types consist of four full adder stages with fast look ahead carry provision from stage to stage. Circuitry is included to provide a fast "parallel-carry-out" but to permit high-speed operation in arithmetic sections using several CD4008BMS's.

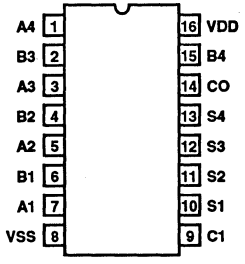
CD4008BMS inputs include the four sets of bits to be added, A1 to A4 and B1 to B4, in addition to the "Carry In" bit from a previous section. CD4008BMS outputs include the four sum bits, S1 to S4. In addition to the high speed "parallel-carry-out" which may be utilized at a succeeding CD4008BMS section.

The CD4008BMS is supplied in these 16-lead outline packages:

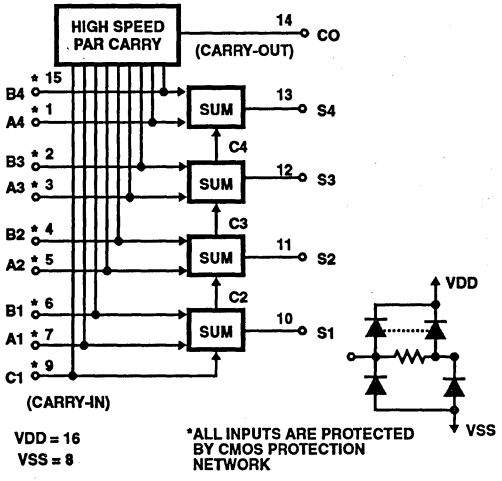
Braze Seal DIP	H4T
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

Pinout

CD4008BMS
TOP VIEW



Logic Diagram



TRUTH TABLE

A_I	B_I	C_I	C_O	SUM
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

7 LOGIC

File Number 3292

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Sum In to Sum Out	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	800	ns
			10, 11	+125°C, -55°C	-	1080	ns
Propagation Delay Carry In To Cum Out	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	740	ns
			10, 11	+125°C, -55°C	-	999	ns
Propagation Delay Sum In To Carry Out	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay Carry In To Carry Out	TPHL4 TPLH4	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Sum In To Sum Out	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	320	ns
		VDD = 15V	1, 2, 3	+25°C	-	230	ns
Propagation Delay Carry In To Sum Out	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	310	ns
		VDD = 15V	1, 2, 3	+25°C	-	230	ns
Propagation Delay Sum In To Carry Out	TPLH3 TPHL3	VDD = 10V	1, 2, 3	+25°C	-	180	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Propagation Delay Carry In To Carry Out	TPHL4 TPLH4	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	10 - 14	1 - 9, 15	16			
Static Burn-In 2 Note 1	10 - 14	8	1 - 7, 9, 15, 16			
Dynamic Burn-In Note 1	-	8	16	10 - 14	2, 4, 6, 15	1, 3, 5, 7, 9

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Irradiation Note 2	10 - 14	8	1 - 7, 9, 15, 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Typical Propagation Delay

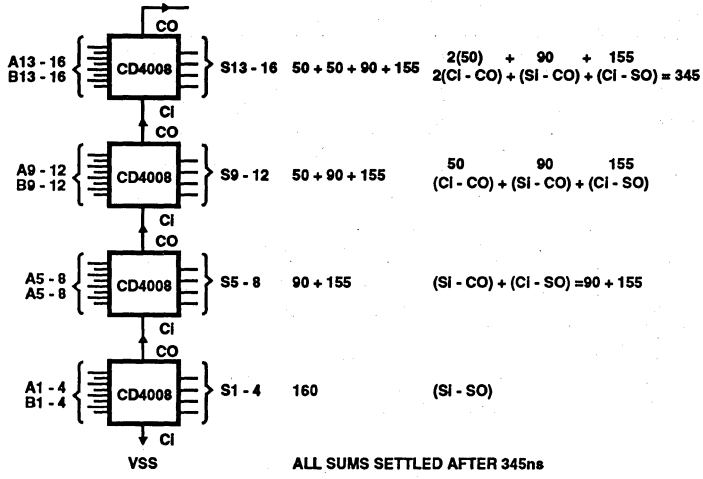


FIGURE 1. PROPAGATION DELAY FOR A 16 BIT ADDER (10V OPERATION)

Typical Performance Characteristics

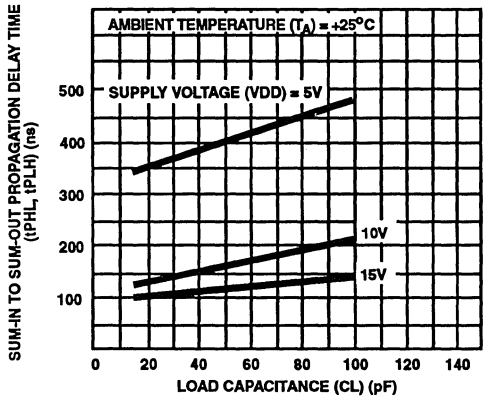


FIGURE 2. TYPICAL SUM-IN TO SUM-OUT PROPAGATION DELAY TIME vs LOAD CAPACITANCE

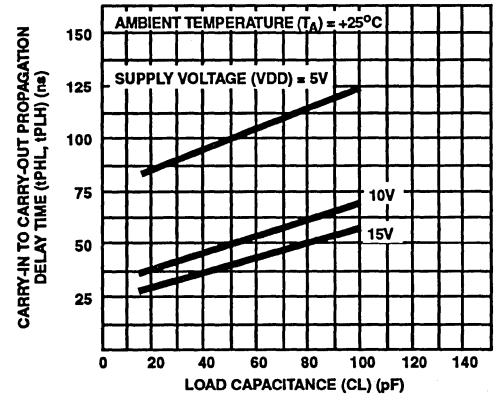


FIGURE 3. TYPICAL CARRY-IN TO CARRY-OUT PROPAGATION DELAY TIME vs LOAD CAPACITANCE

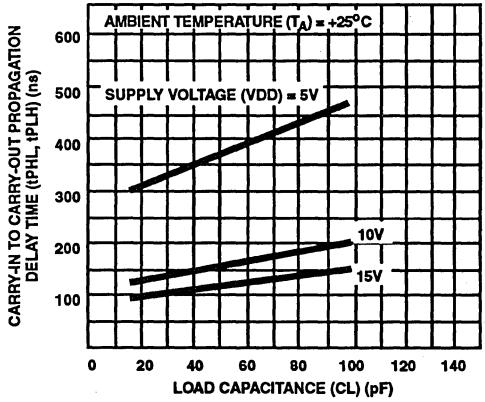


FIGURE 4. TYPICAL CARRY-IN TO SUM-OUT PROPAGATION DELAY TIME vs LOAD CAPACITANCE

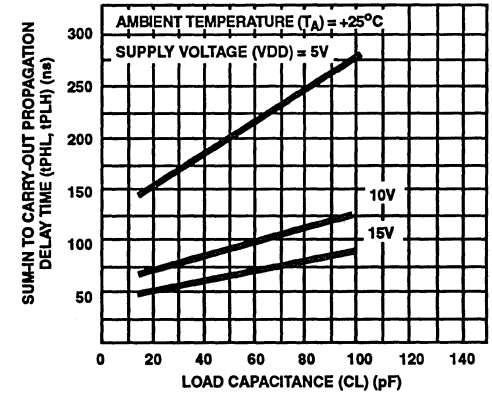


FIGURE 5. TYPICAL SUM-IN TO CARRY-OUT PROPAGATION DELAY TIME vs LOAD CAPACITANCE

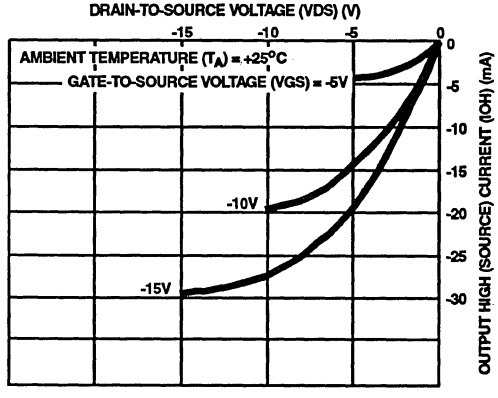


FIGURE 6. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

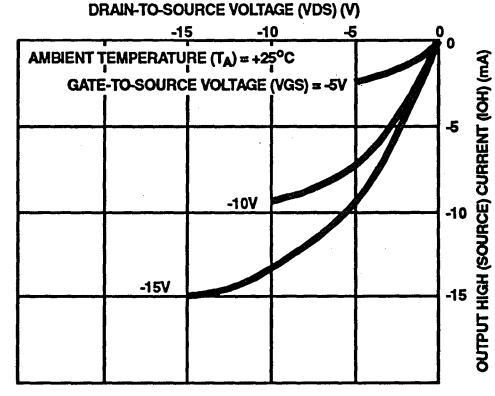


FIGURE 7. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

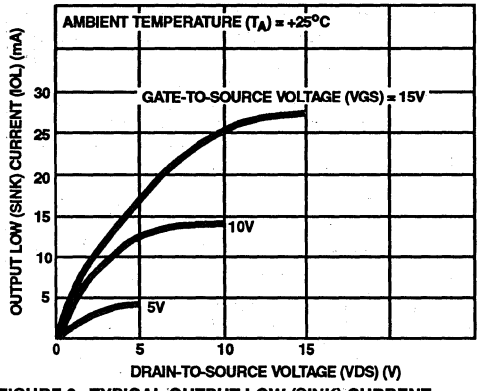


FIGURE 8. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

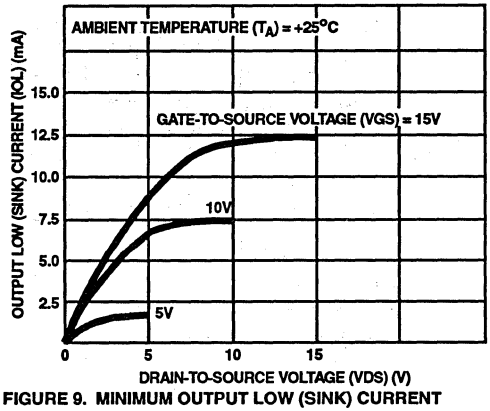


FIGURE 9. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

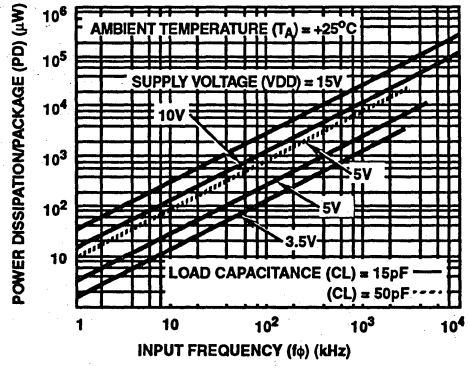
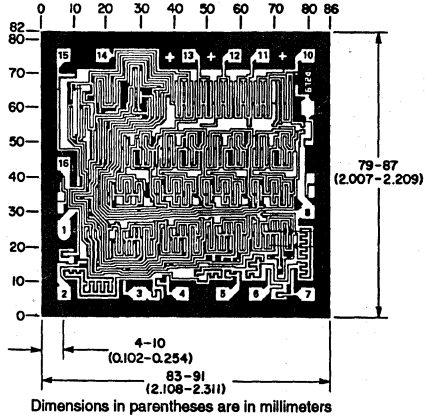


FIGURE 10. TYPICAL DISSIPATION CHARACTERISTICS

Chip Dimensions and Pad Layouts



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4009UBMS

CMOS Hex Buffers/Converter

December 1992

Features

- Inverting Type
- High-Voltage Type (20V Rating)
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package-Temperature Range;
  - 10nA at 18V and +25°C
- 5V, 10V and 15V Parametric Ratings

Applications

- CMOS To DTL/TTL Hex Converter
- CMOS Current "Sink" or "Source" Driver
- CMOS High-to-Low Logic-Level Converter
- Multiplexer - 1 to 6 or 6 to 1

Description

CD4009UBMS Hex Buffer/Converter may be used as a CMOS to TTL or DTL logic-level converter or a CMOS high-sink-current driver.

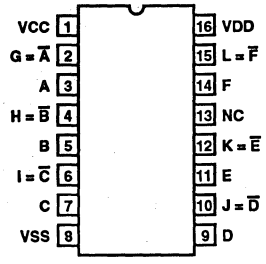
The CD4049UB is the preferred hex buffer replacement for the CD4009UBMS in all applications except multiplexers. For applications not requiring high sink current or voltage conversion, the CD4069UB Hex Inverter is recommended.

The CD4009UBMS is supplied in these 16 lead outline packages:

Braze Seal DIP	H4S
Frit Seal DIP	H1E
Ceramic Flatpack	H3X

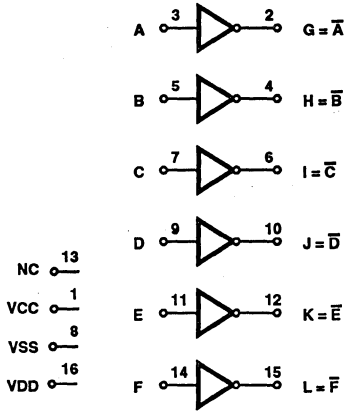
Pinout

CD4009UBMS
TOP VIEW



NC = NO CONNECTION

Functional Diagram



NC = NO CONNECTION

7 LOGIC

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	3.0	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	8.0	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	24.0	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.2	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-0.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-0.45	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-1.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.0	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	4.0	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	2.5	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	12.5	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL	VDD = 5V, VIN = VDD or GND	9	+25°C	-	60	ns
			10, 11	+125°C, -55°C	-	81	ns
Propagation Delay	TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	140	ns
			10, 11	+125°C, -55°C	-	189	ns
Transition Time	TTHL	VDD = 5V, VIN = VDD or GND	9	+25°C	-	70	ns
			10, 11	+125°C, -55°C	-	95	ns
Transition Time	TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	350	ns
			10, 11	+125°C, -55°C	-	473	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL4	VDD = 4.5V, VOUT = 0.4V	1, 2	+25°C	2.6	-	mA
				+125°C	1.8	-	mA
				-55°C	3.2	-	mA
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	2.1	-	mA
				-55°C	3.75	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	5.6	-	mA
				-55°C	10.0	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	16.0	-	mA
				-55°C	30.0	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.15	mA
				-55°C	-	-0.25	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-0.58	mA
				-55°C	-	-1.0	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.33	mA
				-55°C	-	-0.55	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-1.1	mA
				-55°C	-	-1.65	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	2	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	8	-	V
Propagation Delay	TPHL	VDD = 10V, VCC = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V, VCC = 15V	1, 2, 3	+25°C	-	30	ns
Propagation Delay	TPLH	VDD = 10V, VCC = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V, VCC = 15V	1, 2, 3	+25°C	-	60	ns
Propagation Delay	TPHL	VDD = 10V, VCC = 5V	1, 2, 3	+25°C	-	30	ns
		VDD = 15V, VCC = 5V	1, 2, 3	+25°C	-	20	ns
Propagation Delay	TPLH	VDD = 10V, VCC = 5V	1, 2, 3	+25°C	-	70	ns
		VDD = 15V, VCC = 5V	1, 2, 3	+25°C	-	60	ns
Transition Time	TTHL	VDD = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V	1, 2, 3	+25°C	-	30	ns
Transition Time	TTLH	VDD = 10V	1, 2, 3	+25°C	-	150	ns
		VDD = 15V	1, 2, 3	+25°C	-	110	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	22.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V, VCC = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2μA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

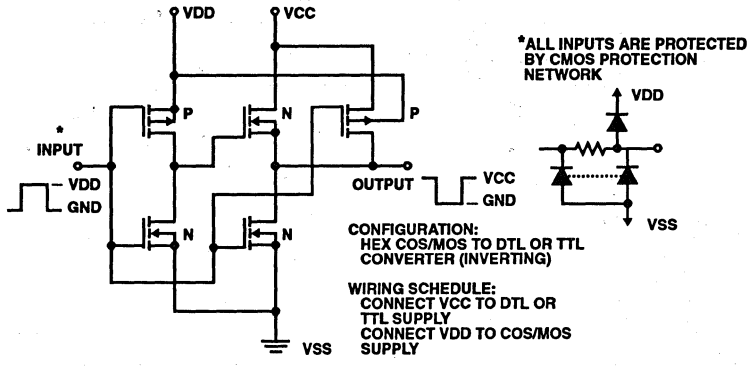
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	2, 4, 6, 10, 12, 13, 15	3, 5, 7 - 9, 11, 14	1, 16			
Static Burn-In 2 Note 1	2, 4, 6, 10, 12, 13, 15	8	1, 3, 5, 7, 9, 11, 14, 16			
Dynamic Burn-In Note 1	13	8	1, 16	2, 4, 6, 10, 12, 15	3, 5, 7, 9, 11, 14	
Irradiation Note 2	2, 4, 6, 10, 12, 13, 15	8	1, 3, 5, 7, 9, 11, 14, 16			

NOTE:

1. Each pin except VDD and Pin 1 and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and Pin 1 and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Schematic Diagram



Typical Performance Characteristics

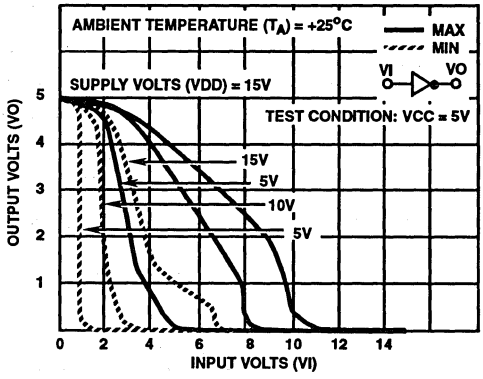


FIGURE 1. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS

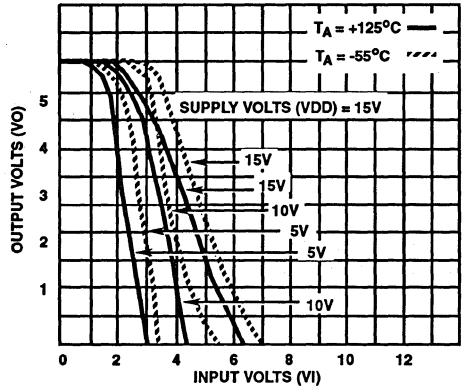


FIGURE 2. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS AS FUNCTION OF TEMPERATURE

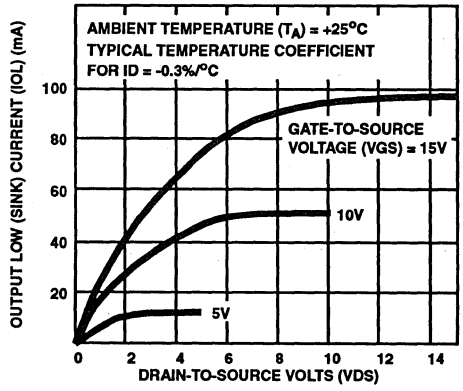


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISITICS

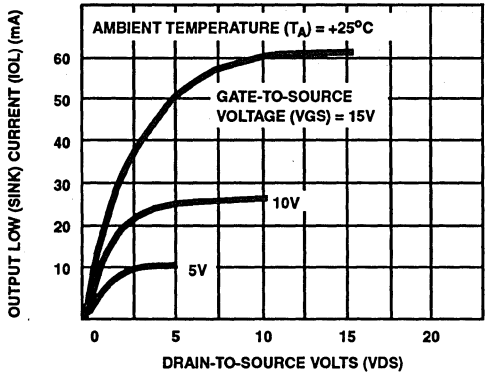


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

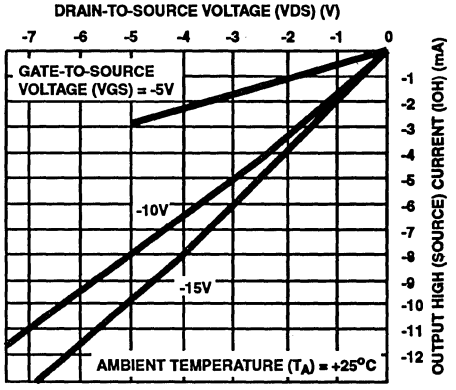


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

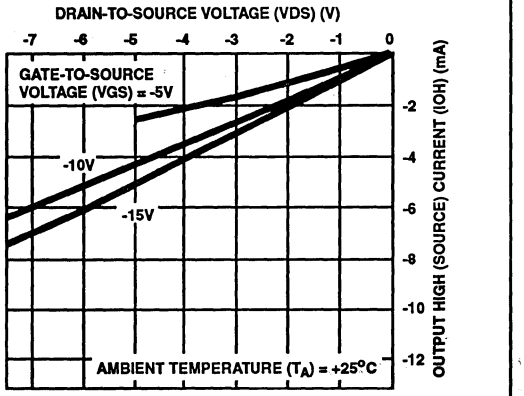


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

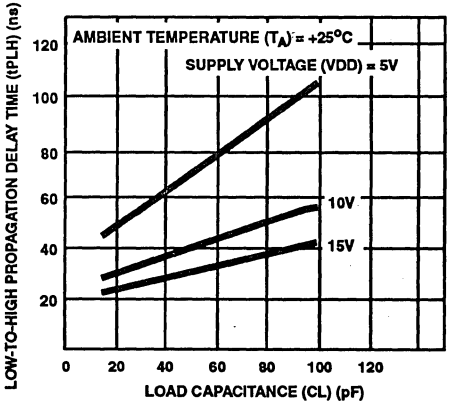


FIGURE 7. TYPICAL LOW-TO-HIGH PROPAGATION DELAY TIME vs LOAD CAPACITANCE

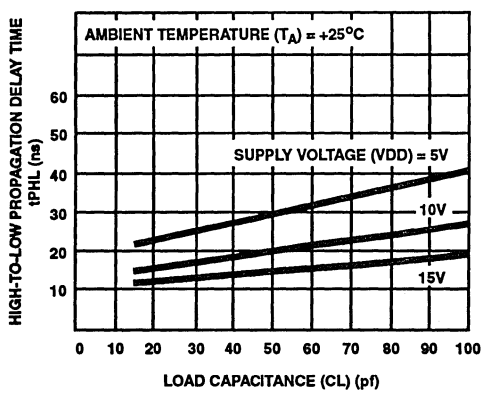


FIGURE 8. TYPICAL HIGH-TO-LOW PROPAGATION DELAY TIME vs LOAD CAPACITANCE

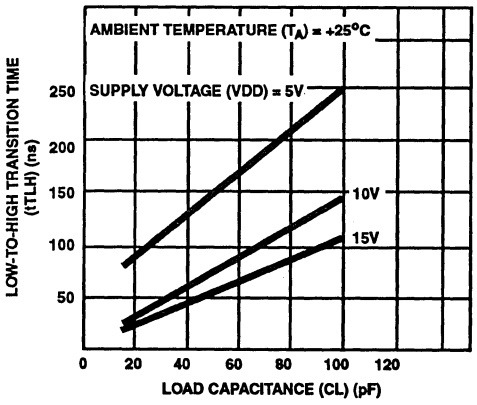


FIGURE 9. TYPICAL LOW-TO-HIGH TRANSITION TIME vs LOAD CAPACITANCE

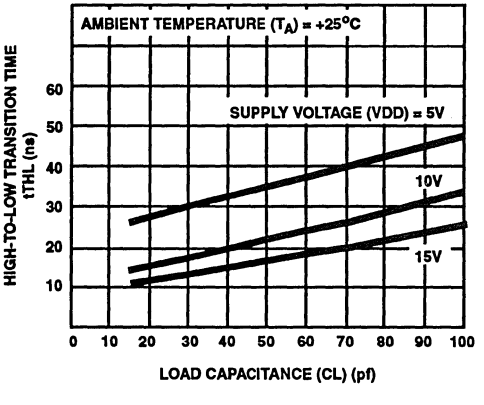


FIGURE 10. TYPICAL HIGH-TO-LOW TRANSISTION TIME vs LOAD CAPACITANCE

7 LOGIC

Typical Performance Characteristics (Continued)

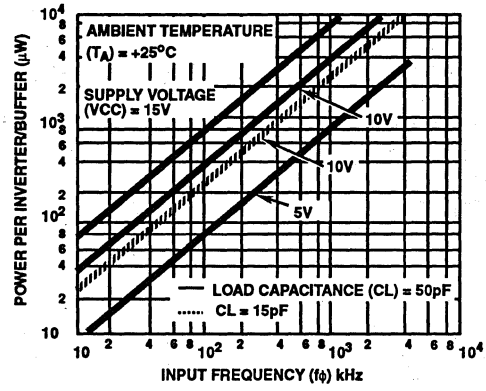
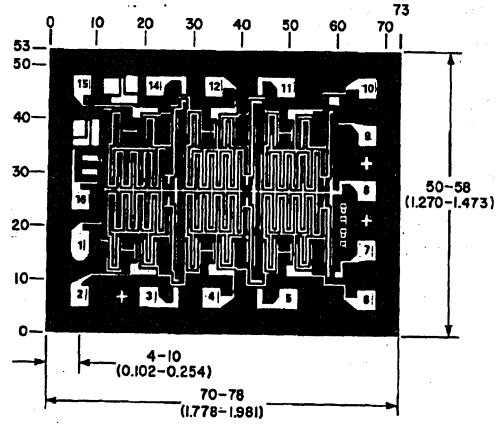


FIGURE 11. TYPICAL DISSIPATION CHARACTERISTICS

Chip Dimensions and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4010BMS

CMOS Hex Buffer/Converter

December 1992

Features

- Non-Inverting Type
- High-Voltage Type (20V Rating)
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package-Temperature Range;
  - 100nA at 18V and +25°C
- 5V, 10V and 15V Parametric Ratings

Applications

- CMOS To DTL/TTL Hex Converter
- CMOS Current "Sink" or "Source" Driver
- CMOS High-to-Low Logic-Level Converter
- Multiplexer - 1 to 6 or 6 to 1

Description

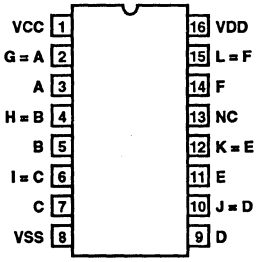
CD4010BMS Hex Buffer/Converter may be used as CMOS to TTL or DTL logic-level converter or CMOS high-sink-current driver.

The CD4050B is the preferred hex buffer replacement for the CD4010BMS in all applications except multiplexers.The CD4010BMS is supplied in these 16 lead outline packages:

Braze Seal DIP	H4S
Frit Seal DIP	H1E
Ceramic Flatpack	H6W

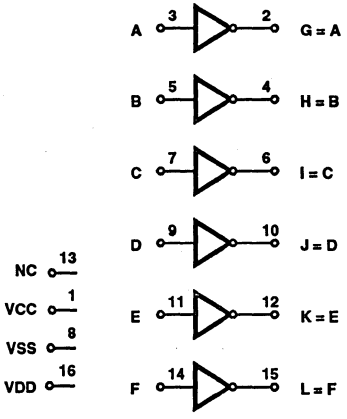
Pinout

CD4010BMS
TOP VIEW



NC = NO CONNECTION

Functional Diagram



NC = NO CONNECTION

7 LOGIC

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range:..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K)..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	3.0	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	8.0	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	24.0	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.2	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-0.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-0.45	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-1.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C		1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5		V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C		4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11		V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL	VDD = 5V, VIN = VDD or GND	9	+25°C	-	130	ns
			10, 11	+125°C, -55°C	-	175	ns
Propagation Delay	TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Transition Time	TTHL	VDD = 5V, VIN = VDD or GND	9	+25°C	-	70	ns
			10, 11	+125°C, -55°C	-	94	ns
Transition Time	TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	350	ns
			10, 11	+125°C, -55°C	-	473	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL4	VDD = 4.5V, VOUT = 0.4V	1, 2	+25°C	2.6	-	mA
				+125°C	1.8	-	mA
				-55°C	3.2	-	mA
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	2.1	-	mA
				-55°C	3.75	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	5.6	-	mA
				-55°C	10.0	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	16.0	-	mA
				-55°C	30.0	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.15	mA
				-55°C	-	-0.25	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-0.58	mA
				-55°C	-	-1.0	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.33	mA
				-55°C	-	-0.55	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-1.1	mA
				-55°C	-	-1.65	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay	TPHL	VDD = 10V, VCC = 10V	1, 2, 3	+25°C	-	70	ns
		VDD = 15V, VCC = 15V	1, 2, 3	+25°C	-	50	ns
Propagation Delay	TPLH	VDD = 10V, VCC = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V, VCC = 15V	1, 2, 3	+25°C	-	70	ns
Propagation Delay	TPHL	VDD = 10V, VCC = 5V	1, 2, 3	+25°C	-	70	ns
		VDD = 15V, VCC = 5V	1, 2, 3	+25°C	-	40	ns
Propagation Delay	TPLH	VDD = 10V, VCC = 5V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V, VCC = 5V	1, 2, 3	+25°C	-	70	ns
Transition Time	TTHL	VDD = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V	1, 2, 3	+25°C	-	30	ns
Transition Time	TTLH	VDD = 10V	1, 2, 3	+25°C	-	150	ns
		VDD = 15V	1, 2, 3	+25°C	-	110	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V, VCC = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RON
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RON
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RON
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RON
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

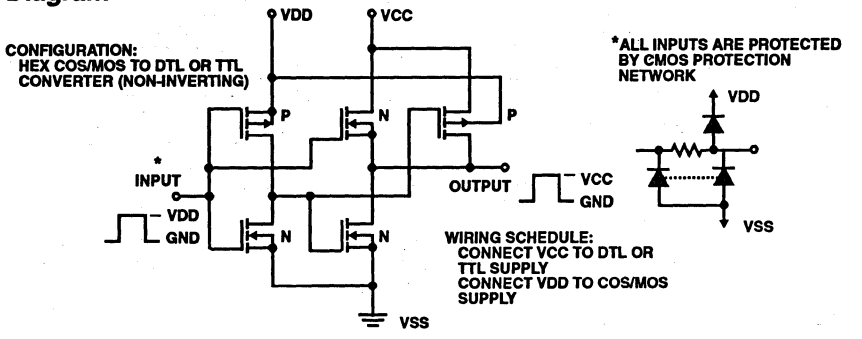
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	2, 4, 6, 10, 12, 13, 15	3, 5, 7 - 9, 11, 14	1, 16			
Static Burn-In 2 (Note 1)	2, 4, 6, 10, 12, 13, 15	8	1, 3, 5, 7, 9, 11, 14, 16			
Dynamic Burn-In (Note 3)	13	8	1, 16	2, 4, 6, 10, 12, 15	3, 5, 7, 9, 11, 14	
Irradiation (Note 2)	2, 4, 6, 10, 12, 13, 15	8	1, 3, 5, 7, 9, 11, 14, 16			

NOTE:

1. Each pin except VDD and Pin 1 and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and Pin 1 and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V
3. Each pin except VDD and Pin 1 and GND will have a series resistor of 4.75K ± 5%, VDD = 18V ± 0.5V

Schematic Diagram



Typical Performance Characteristics

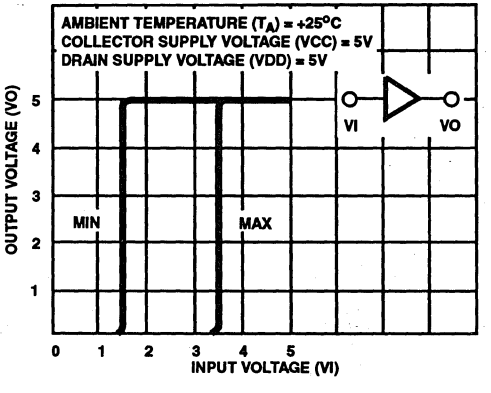


FIGURE 1. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS (VDD = 5)

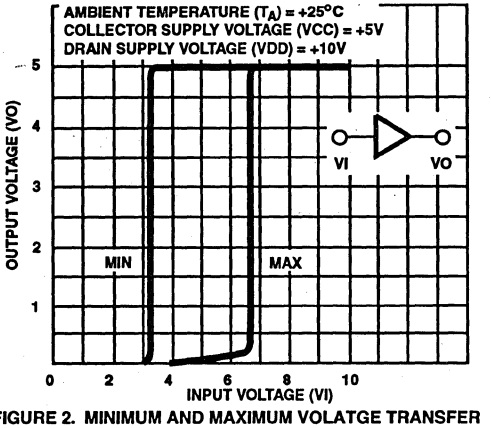


FIGURE 2. MINIMUM AND MAXIMUM VOLATGE TRANSFER CHARACTERISTICS (VDD = 10)

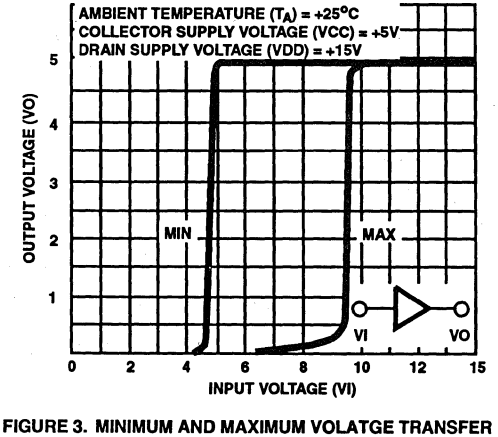


FIGURE 3. MINIMUM AND MAXIMUM VOLATGE TRANSFER CHARACTERISTICS (VDD = 15)

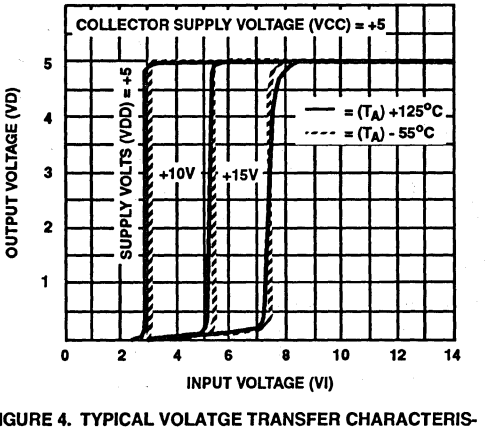


FIGURE 4. TYPICAL VOLATGE TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE

Typical Performance Characteristics (Continued)

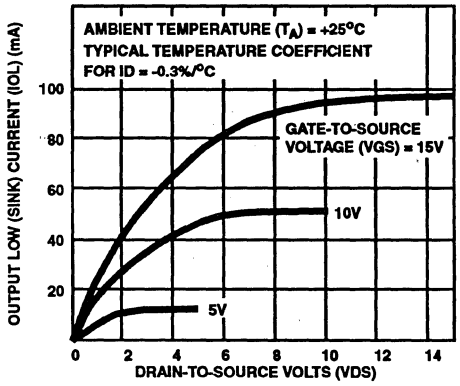


FIGURE 5. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

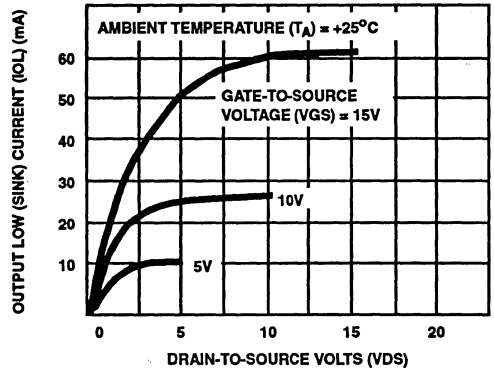


FIGURE 6. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

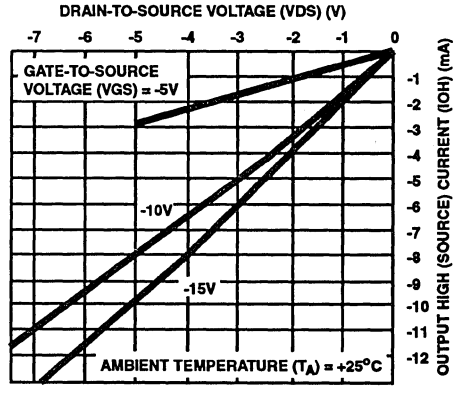


FIGURE 7. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

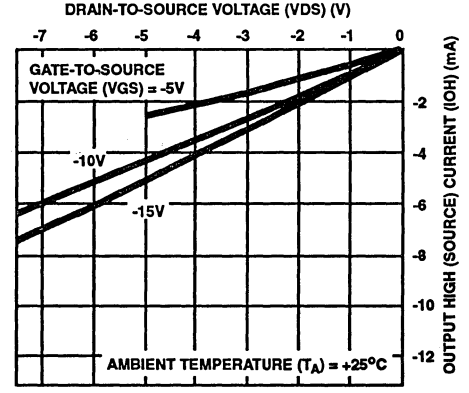


FIGURE 8. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

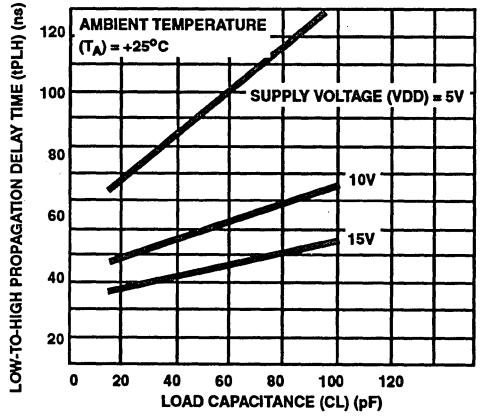


FIGURE 9. TYPICAL LOW-TO-HIGH PROPAGATION DELAYTIME vs LOAD CAPACITANCE

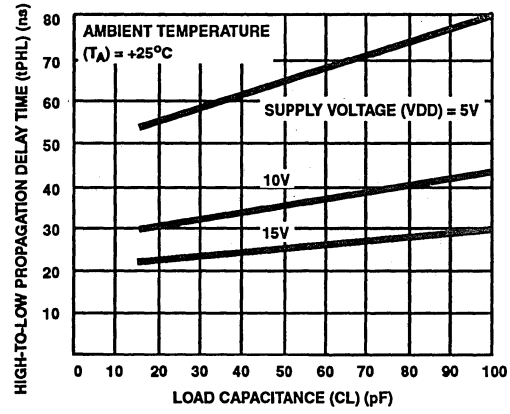


FIGURE 10. TYPICAL HIGH-TO-LOW PROPAGATION DELAYTIME vs LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

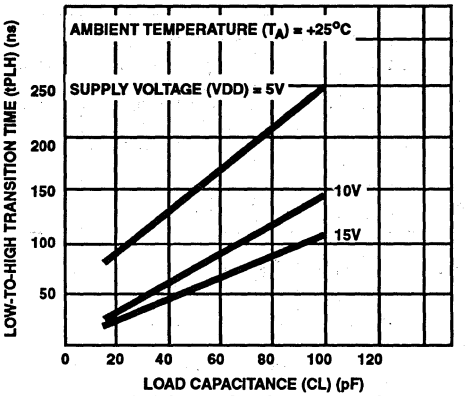


FIGURE 11. TYPICAL LOW-TO-HIGH TRANSITION TIME vs LOAD CAPACITANCE

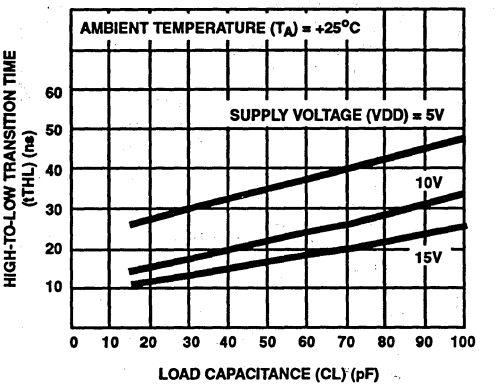


FIGURE 12. TYPICAL HIGH-TO-LOW TRANSITION TIME vs LOAD CAPACITANCE

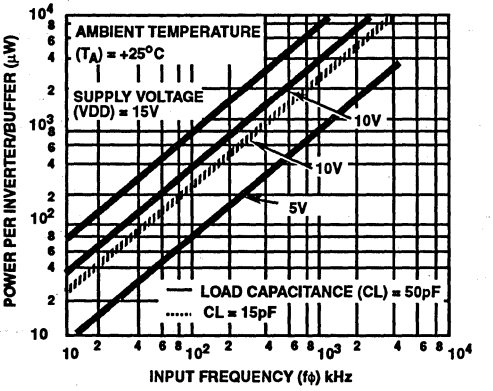
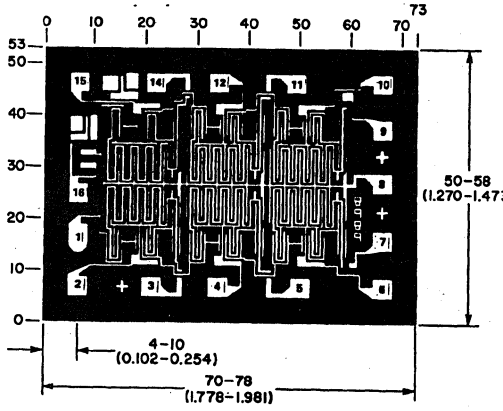


FIGURE 13. TYPICAL DISSIPATION CHARACTERISTICS

Chip Dimensions and Pad Layouts



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

CD4011BMS, CD4012BMS CD4023BMS

December 1992

CMOS NAND Gates

Features

- High-Voltage Types (20V Rating)
- Propagation Delay Time = 60ns (typ.) at CL = 50pF, VDD = 10V
- Buffered Inputs and Outputs
- Standardized Symmetrical Output Characteristics
- Maximum Input Current of 1μA at 18V Over Full Package-Temperature Range; 100nA at 18V and +25°C
- 100% Tested for Maximum Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Noise Margin (Over Full Package Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standards No. 13B, "Standard Specifications for Description of "B" Series CMOS Device's

Description

CD4011BMS - Quad 2 Input

CD4012BMS - Dual 4 Input

CD4023BMS - Triple 3 Input

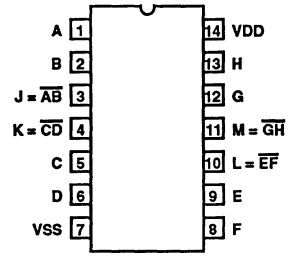
CD4011BMS, CD4012BMS, and CD4023BMS NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of CMOS gates. All inputs and outputs are buffered.

The CD4011BMS, CD4012BMS and the CD4023BMS is supplied in these 14 lead outline packages:

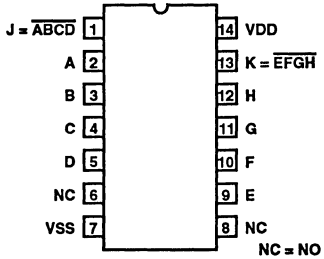
	CD4011B	CD4012B	CD4023B
Braze Seal DIP	H4Q	H4H	H4Q
Frit Seal DIP	H1B	H1B	H1B
Ceramic Flatpack	H3W	H3W	H3W

Pinouts

CD4011BMS
TOP VIEW

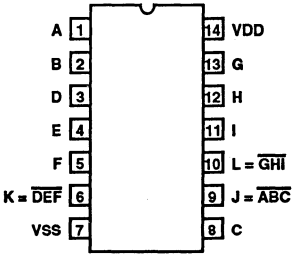


CD4012BMS
TOP VIEW



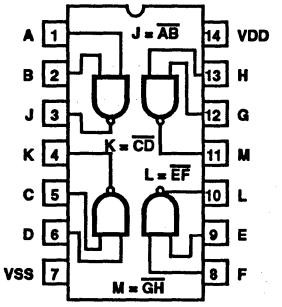
NC = NO CONNECTION

CD4023BMS
TOP VIEW

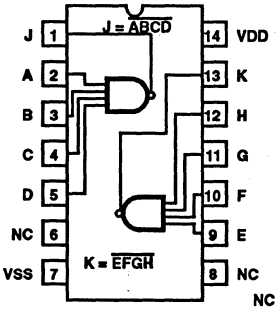


7 LOGIC

Functional Diagrams

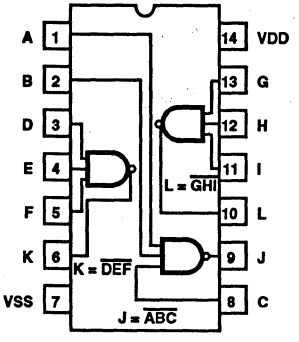


CD4011BMS



NC = NO CONNECTION

CD4012BMS



CD4023BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K)..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	0.5	µA
				2	+125°C	-	50	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	0.5	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	250	ns
			10, 11	+125°C, -55°C	-	338	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.25	µA
				+125°C	-	7.5	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	15	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	30	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	120	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	2.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - SSI	IDD	± 0.1µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

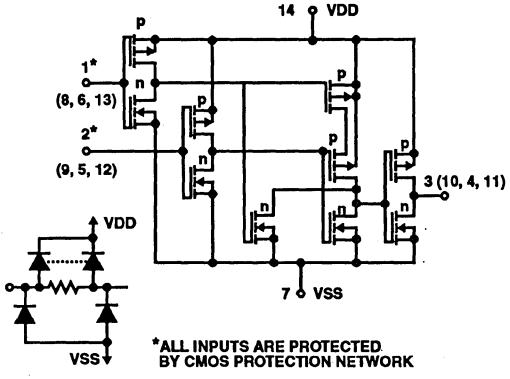
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

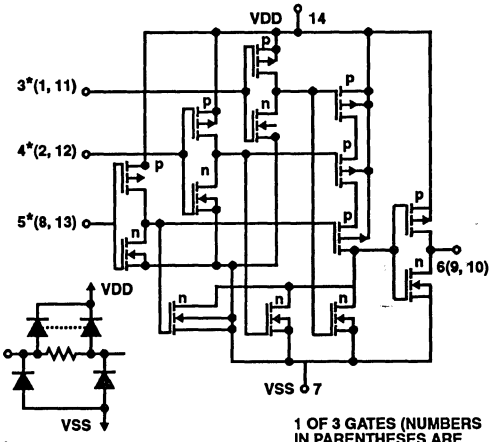
FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
PART NUMBER CD4011B						
Static Burn-In 1 Note 1	3, 4, 10, 11	1, 2, 5 - 9, 12, 13	14			
Static Burn-In 2 Note 1	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12 - 14			
Dynamic Burn-In Note 1	-	7	14	3, 4, 10, 11	1, 2, 5, 6, 8, 9, 12, 13	
Irradiation Note 2	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12 - 14			
PART NUMBER CD4012B						
Static Burn-In 1 Note 1	1, 6, 8, 13	2 - 5, 7, 9 - 12	14			
Static Burn-In 2 Note 1	1, 6, 8, 13	7	2 - 5, 9 - 12, 14			
Dynamic Burn-In Note 1	6, 8	7	14	1, 13	2 - 5, 9 - 12	
Irradiation Note 2	1, 6, 8, 13	7	2 - 5, 9 - 12, 14			
PART NUMBER CD4023B						
Static Burn-In 1 Note 1	6, 9, 10	1 - 5, 7, 8, 11 - 13	14			
Static Burn-In 2 Note 1	6, 9, 10	7	1 - 5, 8, 11 - 14			
Dynamic Burn-In Note 1	-	7	14	6, 9, 10	1 - 5, 8, 11 - 13	
Irradiation Note 2	6, 9, 10	7	1 - 5, 8, 11 - 14			

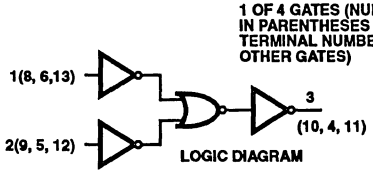
NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

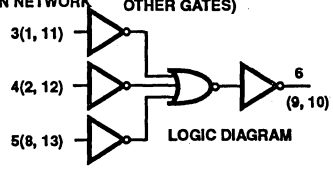
Schematic and Logic Diagrams



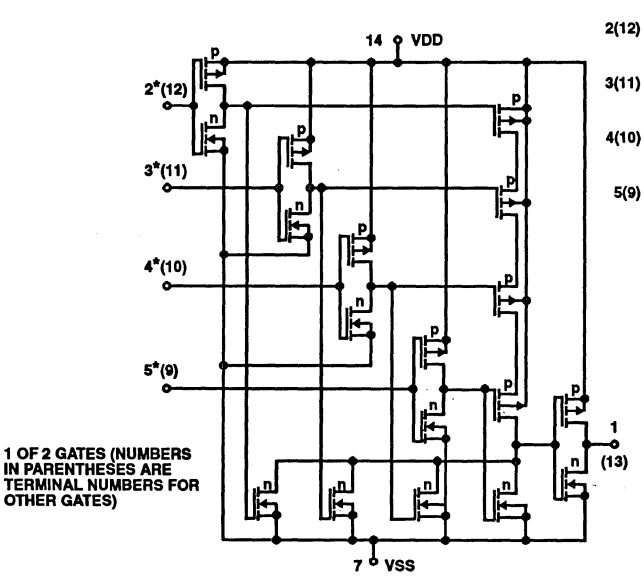


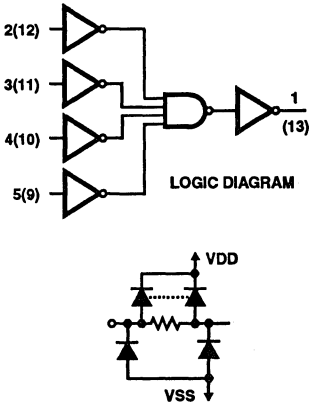


CD4011BMS



CD4023BMS





CD4012BMS

Typical Performance Characteristics

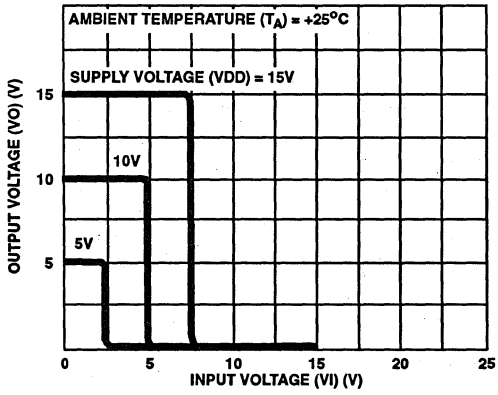


FIGURE 1. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS

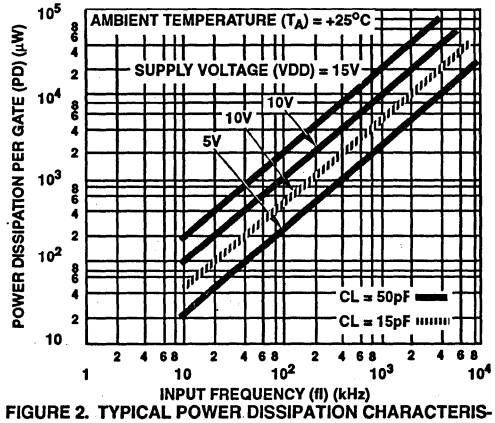


FIGURE 2. TYPICAL POWER DISSIPATION CHARACTERISTICS

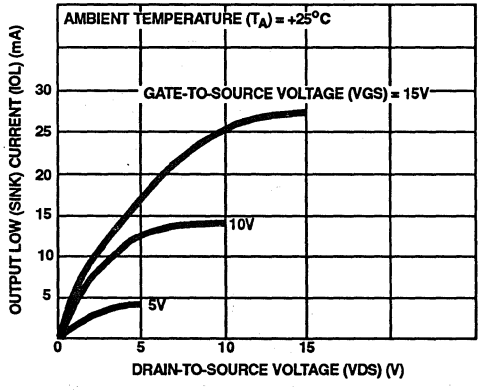


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

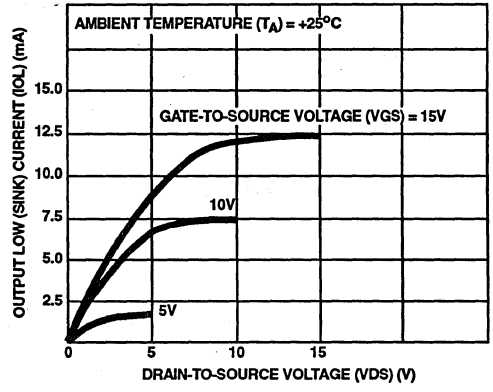


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

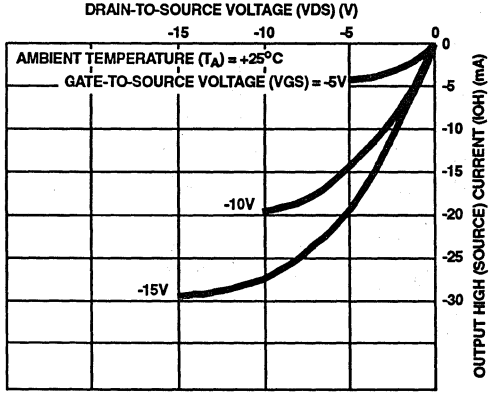


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

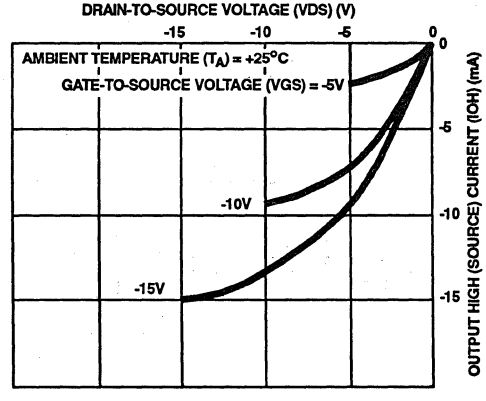


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

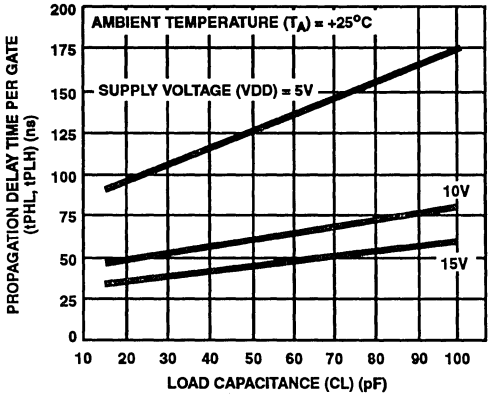


FIGURE 7. TYPICAL PROPAGATION DELAY TIME PER GATE AS A FUNCTION OF LOAD CAPACITANCE

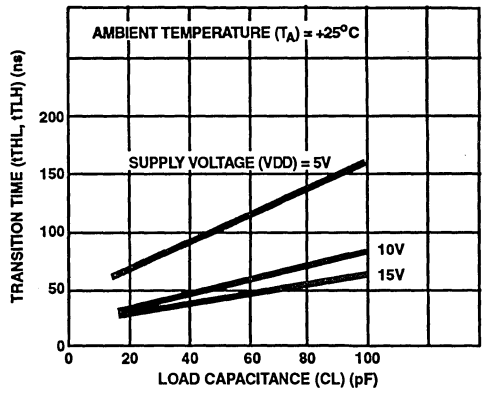
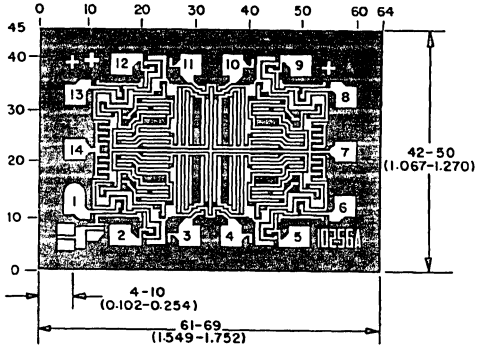
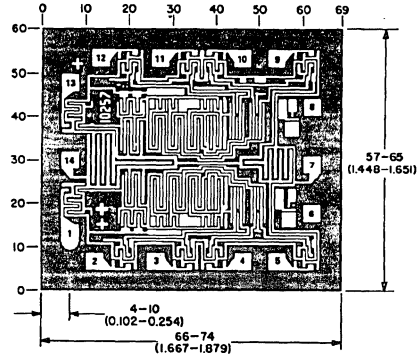


FIGURE 8. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

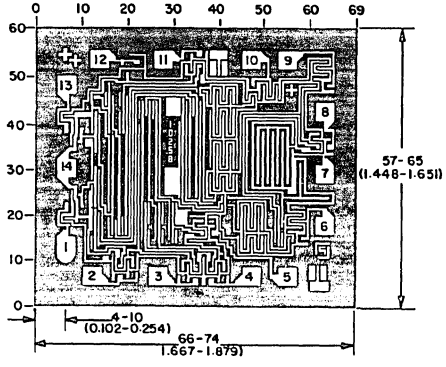
Chip Dimensions and Pad Layouts



CD4011BMSH



CD4012BMSH



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

CD4023BMSH

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4013BMS

December 1992

CMOS Dual 'D'-Type Flip-Flop

Features

- High-Voltage Type (20V Rating)
- Set-Reset Capability
- Static Flip-Flop Operation - Retains State Indefinitely With Clock Level Either "High" Or "Low"
- Medium-Speed Operation - 16 MHz (typ.) Clock Toggle Rate at 10V
- Standardized Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Registers
- Counters
- Control Circuits

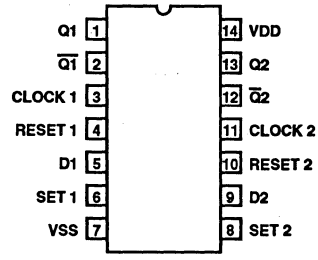
Description

CD4013BMS consists of two identical, independent data type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, and, by connecting $\overline{Q}$ output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

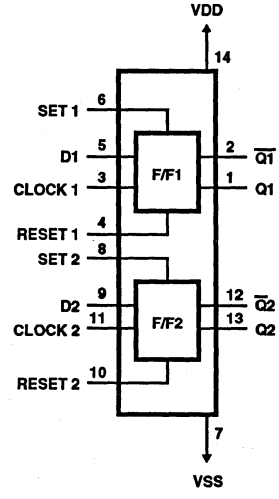
The CD4013BMS is supplied in these 14 lead outline packages:

Braze Seal DIP	H4Q
Frit Seal DIP	H1B
Ceramic Flatpack	H3W

Pinout



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3080

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Q, $\overline{Q}$	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	300	ns
			10, 11	+125°C, -55°C	-	405	ns
Propagation Delay Set to $\overline{Q}$, Reset to Q	TPHL2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay Set to Q, Reset to $\overline{Q}$	TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	300	ns
			10, 11	+125°C, -55°C	-	405	ns
Transition Time Clock to Q, $\overline{Q}$	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	3.5	-	MHz
			10, 11	+125°C, -55°C	3.5/1.35	-	MHz

NOTES:

1. VDD = 5V, CL = 50pF, RL = 200K
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1.0	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2.0	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2.0	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-1.6	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-4.2	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Clock to Q, $\overline{Q}$	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	130	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns
Propagation Delay Set to $\overline{Q}$ Reset to Q	TPHL2	VDD = 10V	1, 2, 3	+25°C	-	170	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Propagation Delay Set to Q Reset to $\overline{Q}$	TPLH2	VDD = 10V	1, 2, 3	+25°C	-	130	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns
Transition Time Clock to Q, $\overline{Q}$	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	8	-	MHz
		VDD = 15V	1, 2, 3	+25°C	12	-	MHz
Minimum Data Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	40	ns
		VDD = 10V	1, 2, 3	+25°C	-	20	ns
		VDD = 15V	1, 2, 3	+25°C	-	15	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	140	ns
		VDD = 10V	1, 2, 3	+25°C	-	60	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Minimum Set or Reset Pulse Width	TW	VDD = 5V	2, 3	+25°C	-	180	ns
		VDD = 10V	2, 3	+25°C	-	80	ns
		VDD = 15V	2, 3	+25°C	-	50	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST PRE-IRRAD	TEST POST-IRRAD	READ AND RECORD PRE-IRRAD	READ AND RECORD POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	1, 2, 12, 13	3-11	14			
Static Burn-In 2 (Note 1)	1, 2, 12, 13	7	3-6, 8-11, 14			
Dynamic Burn-In (Note 1)	-	4, 6-8, 10	14	1, 2, 12, 13	3, 11	5, 9
Irradiation (Note 2)	1, 2, 12, 13	7	3-6, 8-11, 14			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram

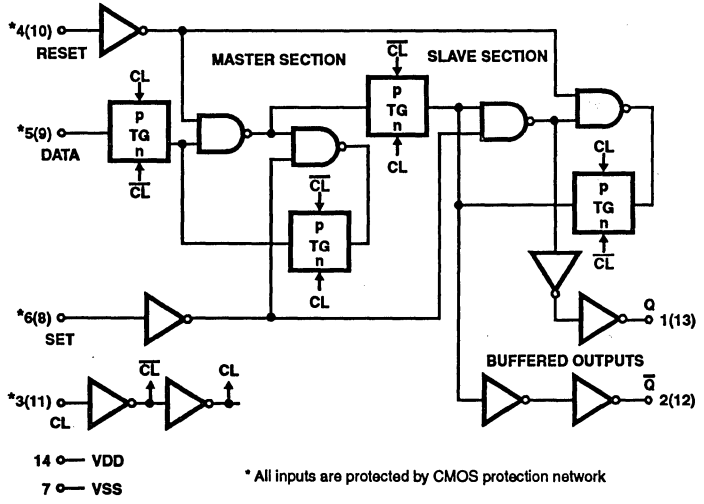


FIGURE 1. ONE OF TWO IDENTICAL FLIP-FLOPS

TRUTH TABLE

CL*	D	R	S	Q	$\overline{Q}$	
⎍	0	0	0	0	1	
⎍	1	0	0	1	0	
⎎	X	0	0	Q	$\overline{Q}$	No Change
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

Logic 0 = Low * = Level change
Logic 1 = High X = Don't care

N(N) = FF1/FF2 terminal assignments

Typical Performance Characteristics

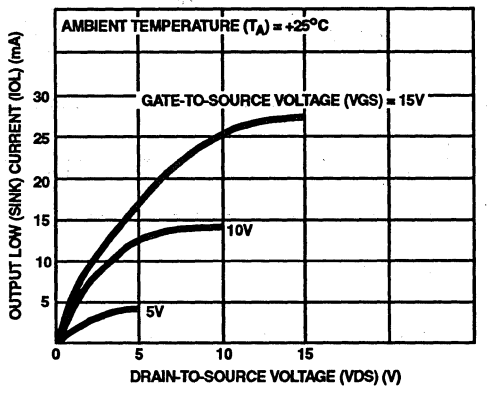


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

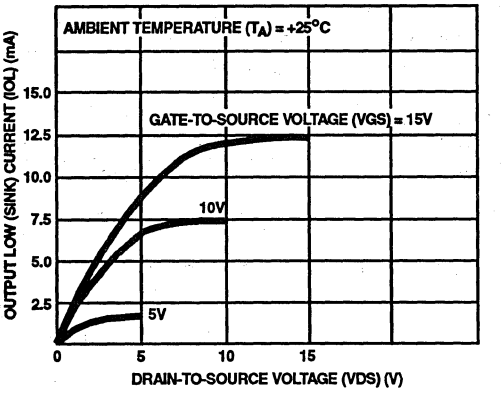


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

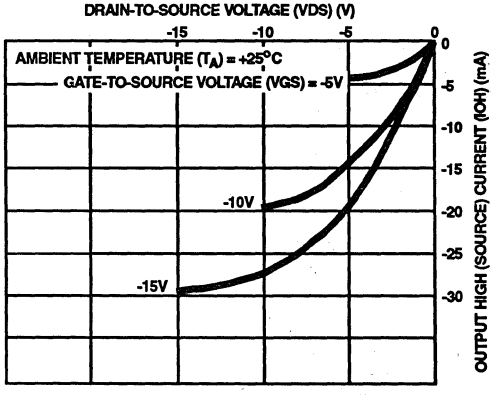


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

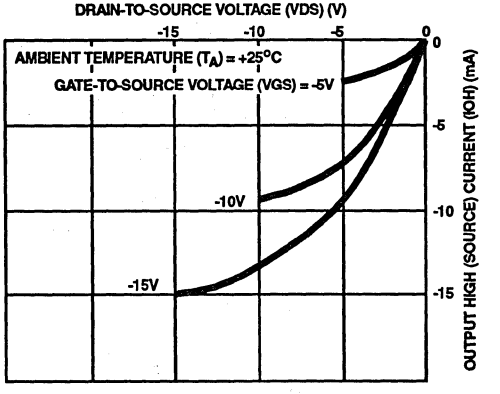


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

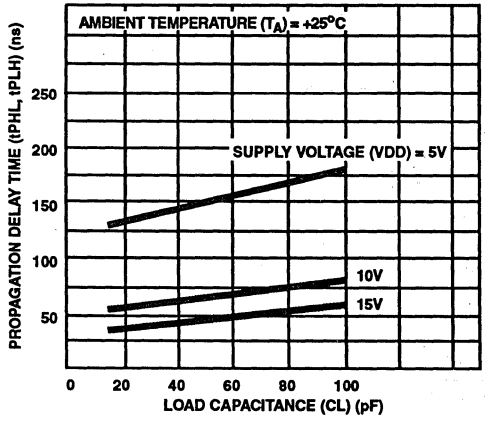


FIGURE 6. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE (CLOCK OR SET TO Q, CLOCK OR RESET TO $\overline{Q}$)

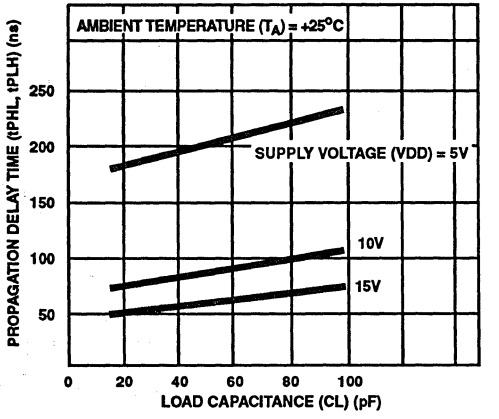


FIGURE 7. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE (SET TO $\overline{Q}$ OR RESET TO Q)

Typical Performance Characteristics (Continued)

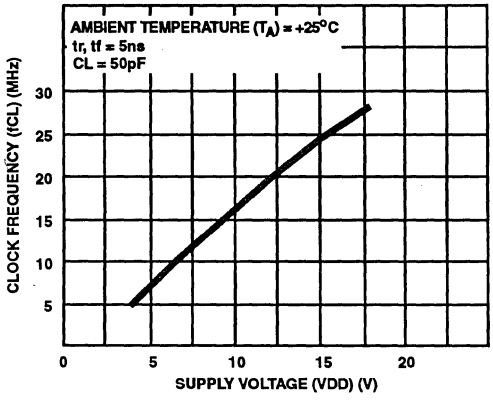


FIGURE 8. TYPICAL MAXIMUM CLOCK FREQUENCY vs SUPPLY VOLTAGE

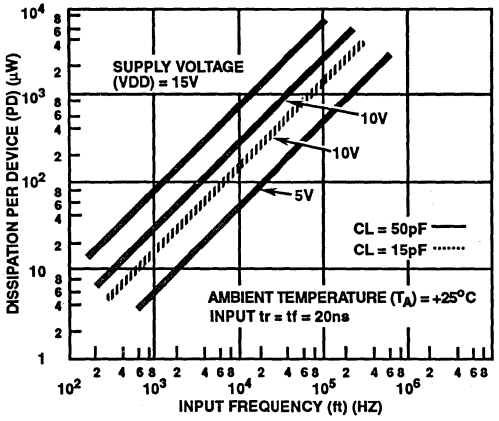
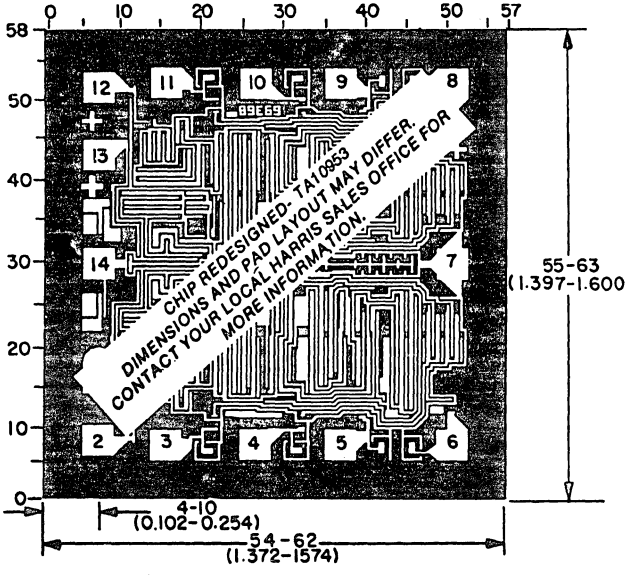


FIGURE 9. TYPICAL POWER DISSIPATION vs FREQUENCY

Chip Dimensions and Pad Layout



Dimension in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4014BMS
CD4021BMS

December 1992

CMOS 8-Stage Static Shift Registers

Features

- High Voltage Types (20V Rating)
- Medium Speed Operation 12MHz (Typ.) Clock Rate at VDD-VSS = 10V
- Fully Static Operation
- 8 Master-Slave Flip-Flops Plus Output Buffering and Control Gating
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Full Package Temperature Range)
- 1V at VDD = 5V
- 2V at VDD = 10V
- 2.5V at VDD = 15V
- Standardized Symmetrical Output Characteristics
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices

Applications:

- Parallel Input/Serial Output Data Queueing
- Parallel to Serial Data Conversion
- General Purpose Register

Description

CD4014BMS -Synchronous Parallel or Serial Input/Serial Output

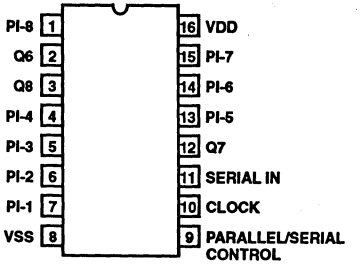
CD4021BMS -Asynchronous Parallel Input or Synchronous Serial Input/Serial Output

CD4014BMS and CD4021BMS series types are 8-stage parallel- or serial-input/serial output registers having common CLOCK and PARALLEL/SERIAL CONTROL inputs, a single SERIAL data input, and individual parallel "JAM" inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. In addition to an output from stage 8, "Q" outputs are also available from stages 6 and 7. Parallel as well as serial entry is made into the register synchronously with the positive clock line transition in the CD4014BMS. In the CD4021BMS serial entry is synchronous with the clock but parallel entry is asynchronous. In both types, entry is controlled by the PARALLEL/SERIAL CONTROL input. When the PARALLEL/SERIAL CONTROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the PARALLEL/SERIAL CONTROL input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line. In the CD4021BMS, the CLOCK input of the internal stage is "forced" when asynchronous parallel entry is made. Register expansion using multiple packages is permitted.

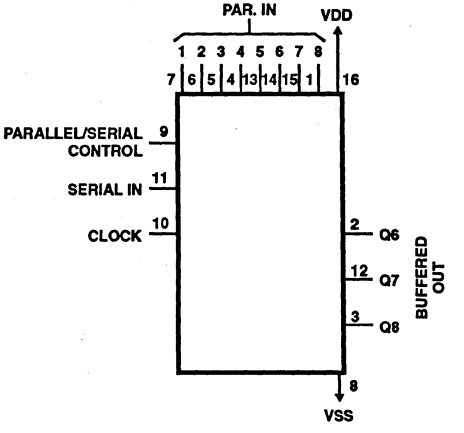
The CD4014BMS and CD4021BMS are supplied in these 16 lead outline packages:

Braze Seal DIP	H4T
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

Pinout



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3294

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	320	ns
			10, 11	+125°C, -55°C	-	432	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	3	-	MHz
			10, 11	+125°C, -55°C	2.22	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	6	-	MHz
		VDD = 15V	1, 2, 3	+25°C	8.5	-	MHz
Clock Rise and Fall Time (Note 4)	TRCL TFCL	VDD = 5V	3, 5	+25°C	-	15	µs
		VDD = 10V	3, 5	+25°C	-	15	µs
		VDD = 15V	3, 5	+25°C	-	15	µs
Minimum Hold Time Serial In, Parallel In Parallel/Serial Control	TH	VDD = 5V	1, 2, 3	+25°C	-	0	ns
		VDD = 10V	1, 2, 3	+25°C	-	0	ns
		VDD = 15V	1, 2, 3	+25°C	-	0	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	180	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Setup Time Serial Input (Ref. to CL)	TS	VDD = 5V	2, 3	+25°C	-	120	ns
		VDD = 10V	2, 3	+25°C	-	80	ns
		VDD = 15V	2, 3	+25°C	-	60	ns
Minimum Setup Time Parallel Inputs CD4014BMS (Ref. to CL)	TS	VDD = 5V	2, 3	+25°C	-	80	ns
		VDD = 10V	2, 3	+25°C	-	50	ns
		VDD = 15V	2, 3	+25°C	-	40	ns
Minimum Setup Time Parallel Inputs CD4021BMS (Ref. to P/S)	TS	VDD = 5V	2, 3	+25°C	-	50	ns
		VDD = 10V	2, 3	+25°C	-	30	ns
		VDD = 15V	2, 3	+25°C	-	20	ns
Minimum Setup Time Parallel/Serial Control CD4014BMS (Ref. to CL)	TS	VDD = 5V	2, 3	+25°C	-	180	ns
		VDD = 10V	2, 3	+25°C	-	80	ns
		VDD = 15V	2, 3	+25°C	-	60	ns
Minimum P/S Pulse Width (CD4021BMS)	TWH	VDD = 5V	2, 3	+25°C	-	160	ns
		VDD = 10V	2, 3	+25°C	-	80	ns
		VDD = 15V	2, 3	+25°C	-	50	ns
Minimum P/S Removal Time CD4021BMS (Ref. to CL)	TREM	VDD = 5V	2, 3	+25°C	-	280	ns
		VDD = 10V	2, 3	+25°C	-	140	ns
		VDD = 15V	2, 3	+25°C	-	100	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. If more than one unit is cascaded, TRCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST PRE-IRRAD	TEST POST-IRRAD	READ AND RECORD PRE-IRRAD	READ AND RECORD POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	2, 3, 12	1,4-11, 13-15	16			
Static Burn-In 2 (Note 1)	2, 3, 12	8	1, 4-7, 9-11, 13-6			
Dynamic Burn-In (Note 1)	-	1, 4-9, 13 -15	16	2, 3, 12	10	11
Irradiation (Note 2)	2, 3, 12	8	1, 4-7, 9-11, 13-16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram

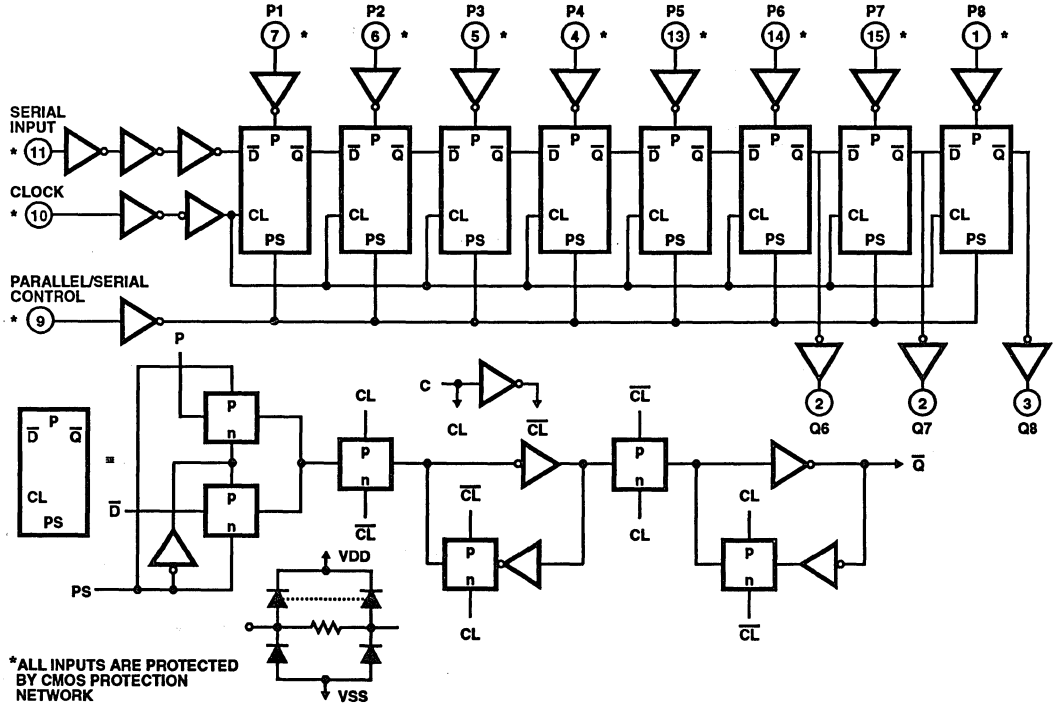


FIGURE 1. CD4014BM LOGIC DIAGRAM

TRUTH TABLE - CD4014BMS

CL	SERIAL INPUT	PARALLEL/SERIAL CONTROL	PI-1	PI-n	Q1 (INTERNAL)	Qn	
↑	X	1	0	0	0	0	
↑	X	1	1	0	1	0	
↑	X	1	0	1	0	1	
↑	X	1	1	1	1	1	
↑	0	0	X	X	0	Qn-1	
↑	1	0	X	X	1	Qn-1	
↓	X	X	X	X	Q1	Qn	NC

X = Don't Care Case NC = No Change

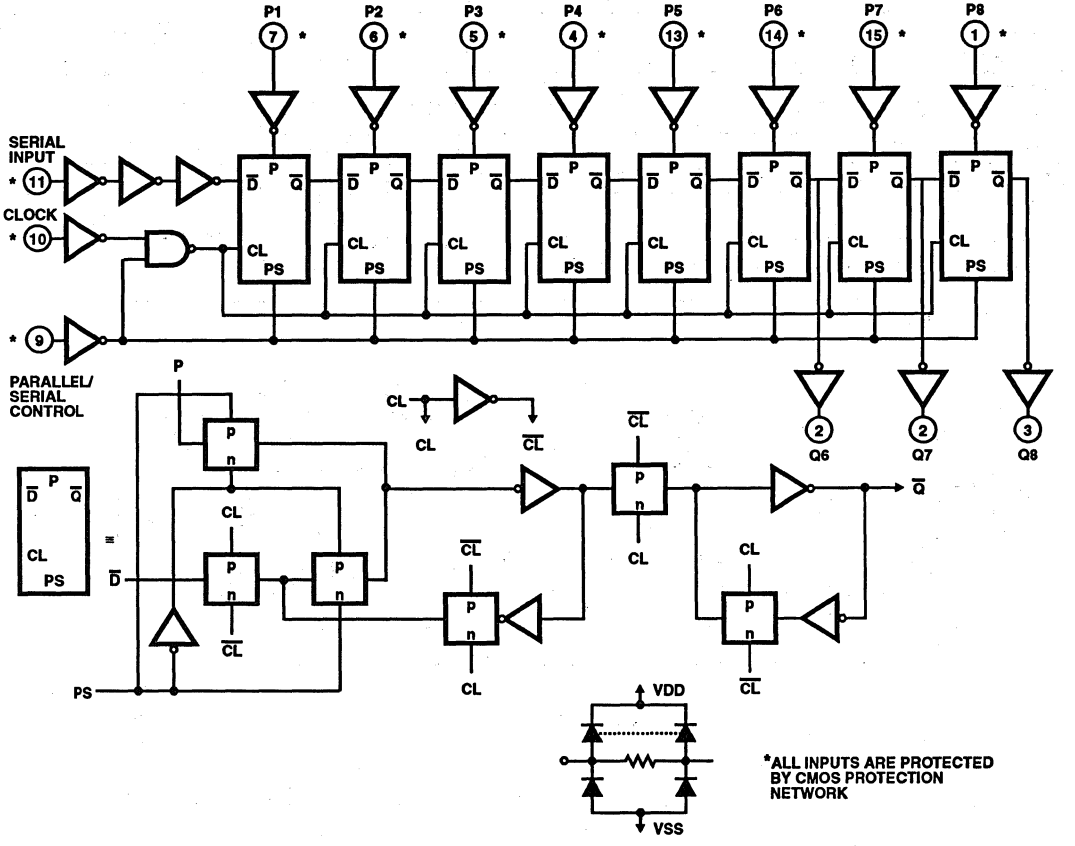


FIGURE 2. CD4021BMS LOGIC DIAGRAM

TRUTH TABLE - CD4021BMS

CL	SERIAL INPUT	PARALLEL/SERIAL CONTROL	PI-1	PI-n	Q1 (INTERNAL)	Qn	
X	X	1	0	0	0	0	
X	X	1	0	1	0	1	
X	X	1	1	0	1	0	
X	X	1	1	1	1	1	
↑	0	0	X	X	0	Qn-1	
↑	1	0	X	X	1	Qn-1	
↓	X	0	X	X	Q1	Qn	NC

X = Don't Care Case

Typical Performance Characteristics

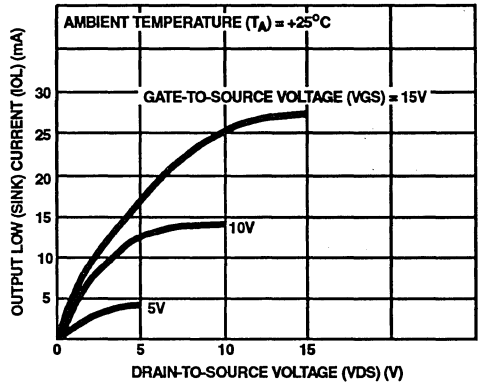


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

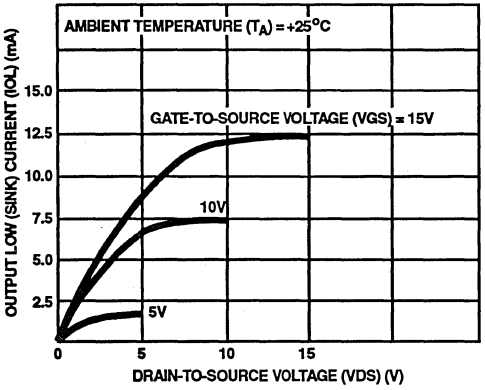


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

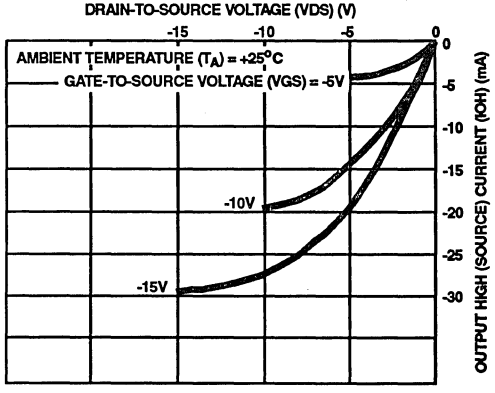


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

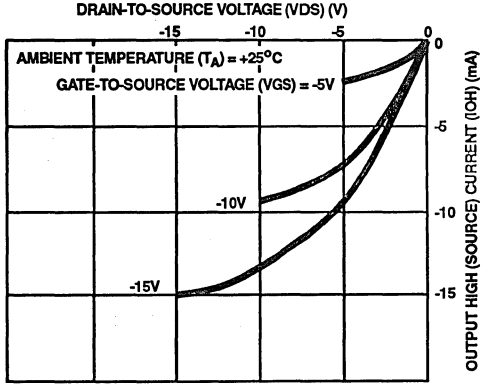


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

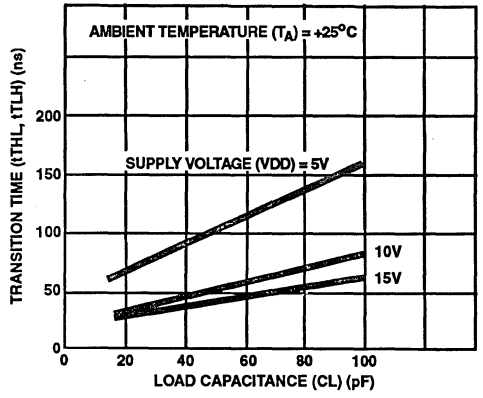


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

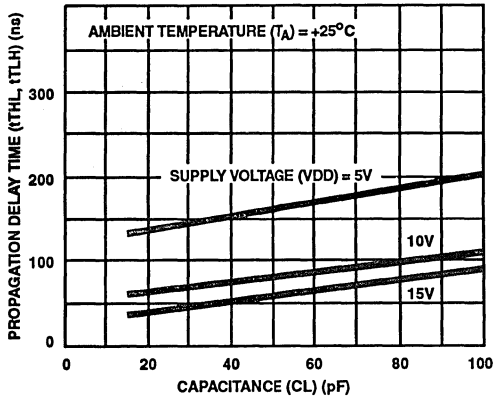


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

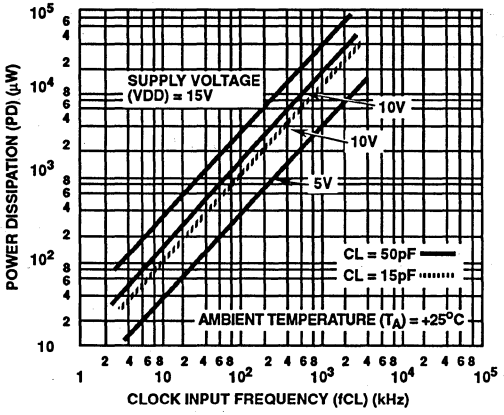
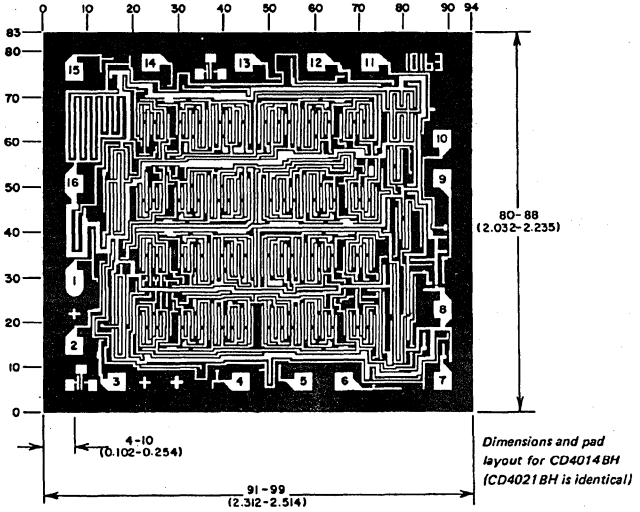


FIGURE 9. TYPICAL POWER DISSIPATION AS A FUNCTION OF FREQUENCY

Chip Dimensions and Pad Layouts



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4015BMS

CMOS Dual 4-Stage Static Shift Register With Serial Input/Parallel Output

December 1992

Features

- High-Voltage Type (20V Rating)
- Medium Speed Operation 12MHz (typ.) Clock Rate at VDD - VSS = 10V
- Fully Static Operation
- 8 Master-Slave Flip-Flops Plus Input and Output Buffering
- 100% Tested For Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Standardized Symmetrical Output Characteristics
- Maximum Input Current of 1μA at 18V Over Full Package-Temperature Range; 100nA at 18V and 25°C
- Noise Margin (Full Package-Temperature Range) =
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Serial-Input/Parallel-Output Data Queueing
- Serial to Parallel Data Conversion
- General-Purpose Register

Description

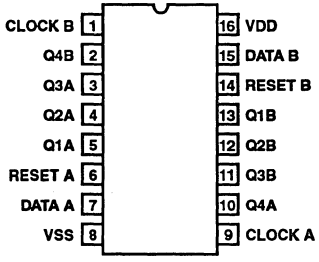
CD4015BMS consists of two identical, independent, 4-stage serial-input/parallel output registers. Each register has independent CLOCK and RESET inputs as well as a single serial DATA input. "Q" outputs are available from each of the four stages on both registers. All register stages are D type, master-slave flip-flops. The logic level present at the DATA input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one CD4015BMS package, or to more than 8 stages using additional CD4015BMS's is possible.

The CD4015BMS is supplied in these 16 lead outline packages:

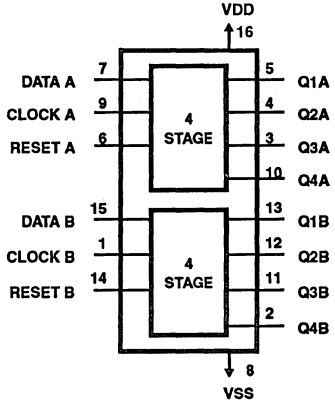
Braze Seal DIP	H4X
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

Pinout

CD4015BMS
TOP VIEW



Functional Diagram



7 LOGIC

File Number 3295

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

	θ_{ja}	θ_{jc}
Thermal Resistance		
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K)..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock To Q	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	320	ns
			10, 11	+125°C, -55°C	-	432	ns
Propagation Delay Reset To Q	TPHL2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	3	-	MHz
			10, 11	+125°C, -55°C	3/1.35	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Clock To Q	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Propagation Delay Reset To Q	TPHL2	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	160	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	6	-	MHz
		VDD = 15V	1, 2, 3	+25°C	8.5	-	MHz
Minimum Data Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	70	ns
		VDD = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V	1, 2, 3	+25°C	-	30	ns
Clock Rise and Fall Time	TRCL TFCL	VDD = 5V	1, 2, 3	+25°C	-	15	µs
		VDD = 10V	1, 2, 3	+25°C	-	15	µs
		VDD = 15V	1, 2, 3	+25°C	-	15	µs
Minimum Clock Pulse Width	TWCL	VDD = 5V	1, 2, 3	+25°C	-	180	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Reset Pulse Width	TWR	VDD = 5V	2, 3	+25°C	-	200	ns
		VDD = 10V	2, 3	+25°C	-	80	ns
		VDD = 15V	2, 3	+25°C	-	60	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS= -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	2 - 5, 10 - 13	1, 6 - 9, 14, 15	16			
Static Burn-In 2 Note 1	2 - 5, 10 - 13	8	1, 6, 7, 9, 14 - 16			

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS (Continued)

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Dynamic Burn-In Note 1	-	6, 8, 14	16	2 - 5, 10 - 13	1, 9	7, 15
Irradiation Note 2	2 - 5, 10 - 13	8	1, 6, 7, 9, 14 - 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram

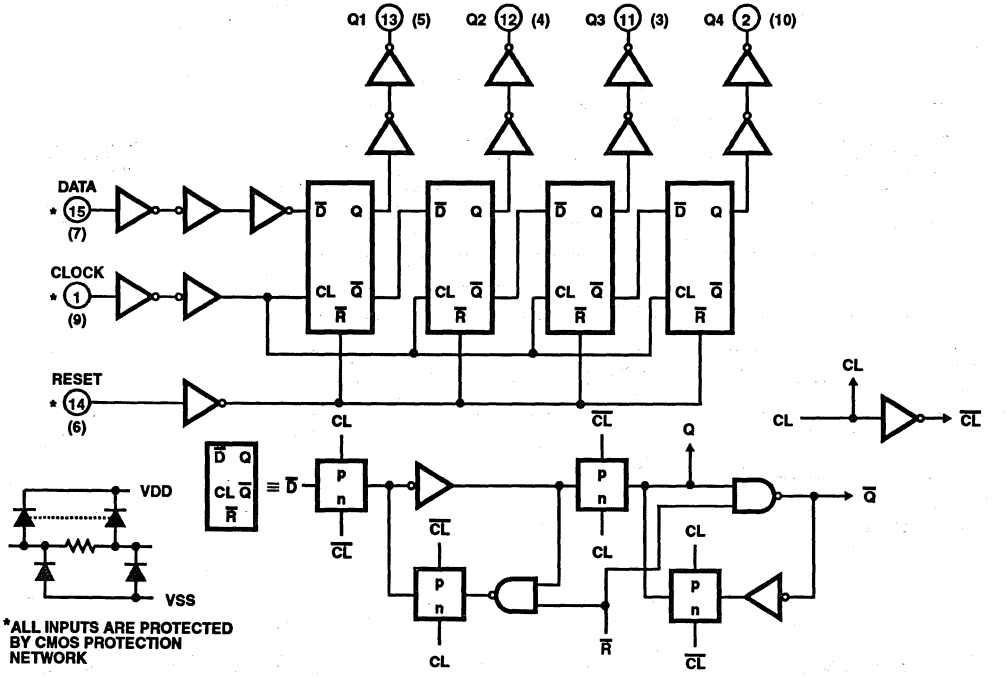


FIGURE 1. CD4015BMS LOGIC DIAGRAM

TRUTH TABLE

CL	D	R	Q1	Qn	
↗	0	0	0	Qn-1	
↗	1	0	1	Qn-1	
↘	X	0	Q1	Qn	(No Change)
X	X	1	0	0	

X = Don't care Case

Typical Performance Characteristics

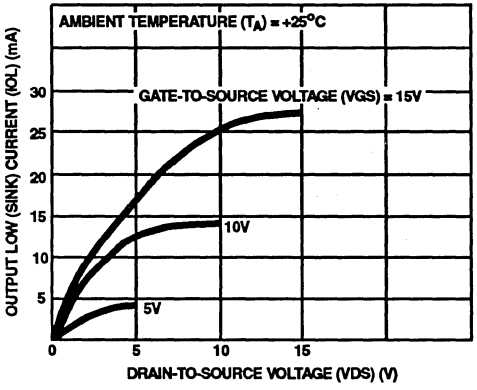


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

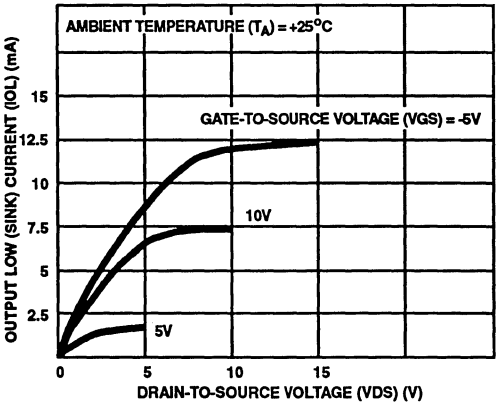


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

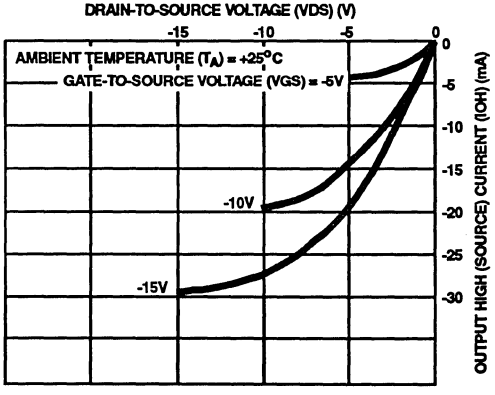


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

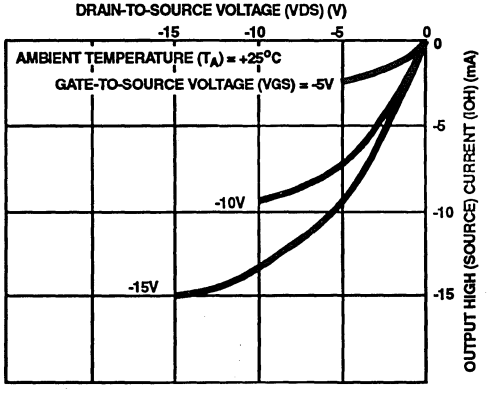


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

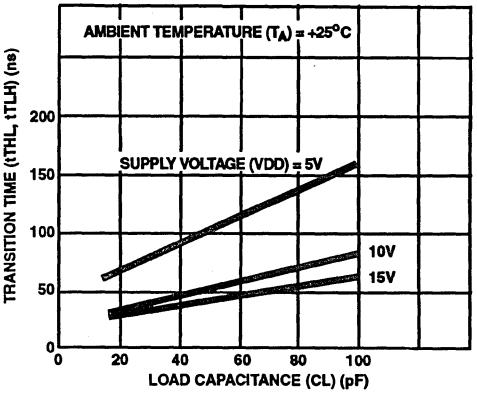


FIGURE 6. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

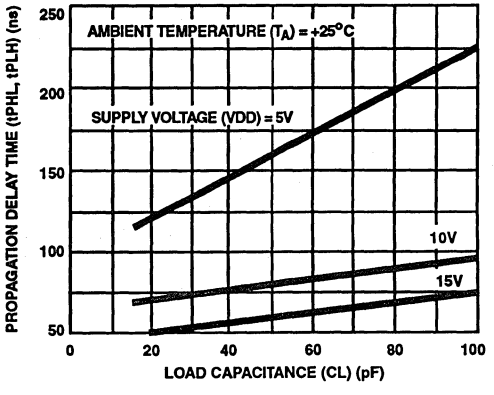


FIGURE 7. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

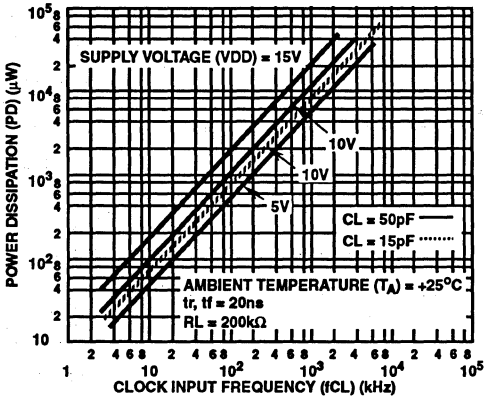
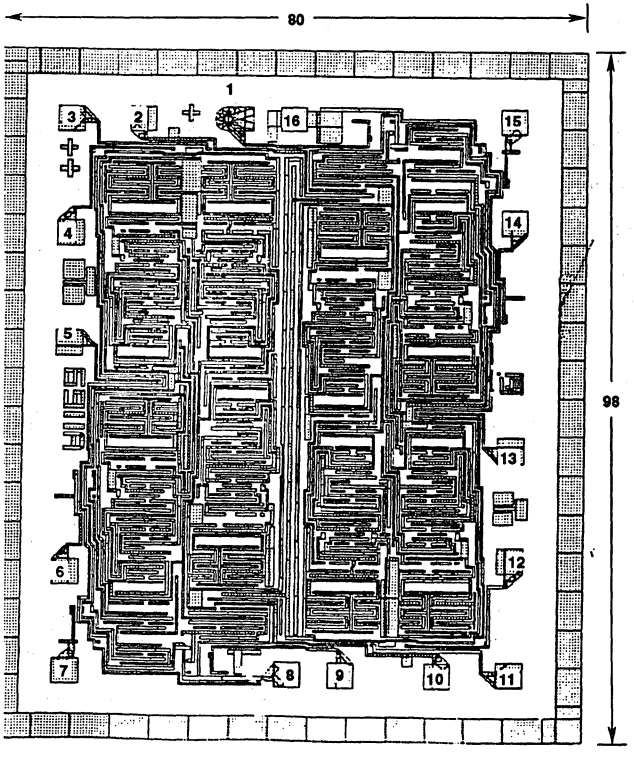


FIGURE 8. TYPICAL POWER DISSIPATION AS A FUNCTION OF FREQUENCY

Chip Dimensions and Pad Layout



METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

DIE SIZE: X = 80 (77 - 85) = (1.956 - 2.159)
Y = 98 (95 - 103) = (2.413 - 2.616)

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

HARRIS SEMICONDUCTOR

CD4016BMS

CMOS Quad Bilateral Switch

December 1992

Features

- Transmission or Multiplexing of Analog or Digital Signals
- High Voltage Type (20V Rating)
- 20V Digital or ±10V Peak-to-Peak Switching
- 280Ω Typical On-State Resistance for 15V Operation
- Switch On-State Resistance Matched to Within 10Ω Typ. Over 15V Signal Input Range
- High On/Off Output Voltage Ratio: 65dB Typ. at FIS = 10kHz, RL = 10kΩ
- High Degree of Linearity: <0.5% Distortion Typ. at FIS = 1kHz, VIS = 5Vp-p, VDD-VSS ≥ 10V, RL = 10kΩ
- Extremely Low Off State Switch Leakage Resulting in Very Low Offset Current and High Effective Off State Resistance: 100pA Typ. at VDD-VSS = 18V, T_A = 25°C
- Extremely High Control Input Impedance (Control circuit Isolated from Signal Circuit: $10^{12}\Omega$ Typ.
- Low Crosstalk Between Switches: -50dB Typ. at FIS = 0.9MHz, RL = 1kΩ
- Matched Control Input to Signal Output Capacitance: Reduces Output Signal Transients
- Frequency Response, Switch On = 40MHz (Typ.)
- 100% Tested for Quiescent Current at 20V
- Maximum Control Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V at +25°C
- 5V, 10V and 15V Parametric Ratings

Applications

- Analog Signal Switching/Multiplexing
- Signal Gating
- Squelch Control
- Chopper
- Modulator
- Demodulator
- Commutating Switch
- Digital Signal Switching/Multiplexing
- CMOS Logic Implementation
- Analog to Digital & Digital to Analog Conversion
- Digital Control of Frequency, Impedance, Phase, and Analog Signal Gain

Description

CD4016BMS Series types are quad bilateral switches intended for the transmission or multiplexing of analog or digital signals. Each of the four independent bilateral switches has a single control signal input which simultaneously biases both the p and n device in a given switch on or off.

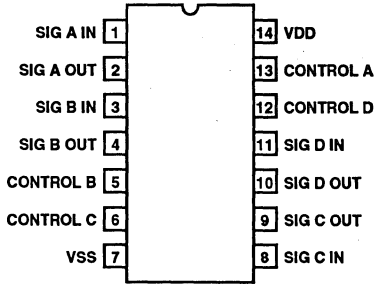
The CD4016BMS is supplied in these 14 lead outline packages:

Braze Seal DIP	H4Q
Frit Seal DIP	H1B
Ceramic Flatpack	H3W

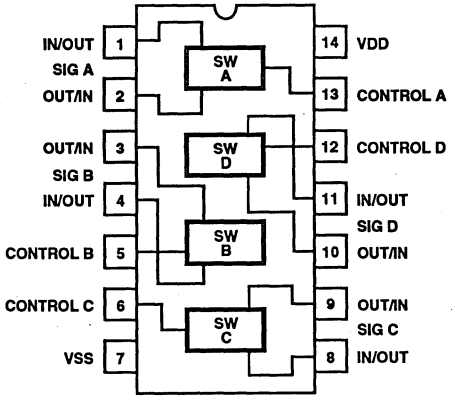
7 LOGIC

Pinout

CD4016BMS
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3296

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	0.5	µA
				2	+125°C	-	50	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	0.5	µA
Input Leakage Current	IIL	VC = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VC = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Input/Output Leakage Current (Switch Off)	IOZL	VDD = 18V, VC = 0V, VIS = 18V, VOS = 0V		1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
				3	-55°C	-100	-	nA
Input/Output Leakage Current (Switch Off)	IOZH	VDD = 18V, VIS = 18V, VOS = 0V		1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
				3	-55°C	-	100	nA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
On-State Resistance RL = 10K Returned to VDD-VSS/2	RON10	VIS = VDD or VSS, VDD = 10V		1	+25°C	-	660	Ω
				2	+125°C	-	960	Ω
				3	-55°C	-	600	Ω
	RON10	VIS = 4.75V or 5.75V, VDD = 10V		1	+25°C	-	2000	Ω
				2	+125°C	-	2600	Ω
				3	-55°C	-	1870	Ω
	RON15	VIS = VDD or VSS, VDD = 15V		1	+25°C	-	400	Ω
				2	+125°C	-	600	Ω
				3	-55°C	-	360	Ω
	RON15	VIS = 7.25 or 7.75, VDD = 15V		1	+25°C	-	850	Ω
				2	+125°C	-	1230	Ω
				3	-55°C	-	775	Ω
Functional (Note 3)	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Switch Threshold RL = 100K to VDD	SWTHRH5	VDD = 5V, VC = 1.5V, VIS = GND		1, 2, 3	+25°C, +125°C, -55°C	4.1	-	V
	SWTHRH15	VDD = 15V, VC = 2V, VIS = GND		1, 2, 3	+25°C, +125°C, -55°C	14.1	-	V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage Control, Low (Note 2)	VILC	VDD = 5V, VOS = VDD, VIS = VSS, and VDD = 5V, VOS = VSS, VIS = VDD, IIISI < 10µA	1	+25°C	-	0.7	V
			2	+125°C	-	0.4	V
			3	-55°C	-	0.9	V
Control Input High Voltage (Note 2, Figure 12) VIS = VSS, and VIS = VDD	VIHC	VDD = 5V, IIISI = .16mA, 4.6V < VOS < 0.4V	1	+25°C	3.5	-	V
		VDD = 5V, IIISI = .14mA, 4.6V < VOS < 0.4V	2	+125°C	3.5	-	V
		VDD = 5V, IIISI = .25mA, 4.6V < VOS < 0.4V	3	-55°C	3.5	-	V
	VIHC	VDD = 15V, IIISI = 1.2mA, 13.5V < VOS < 1.5V	1	+25°C	11	-	V
		VDD = 15V, IIISI = 1.1mA, 13.5V < VOS < 1.5V	2	+125°C	11	-	V
		VDD = 15V, IIISI = 1.8mA, 13.5V < VOS < 1.5V	3	-55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs
3. VDD = 2.8V/3V, RL = 100K to VDD
VDD = 20V/18V, RL = 10K to VDD

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Signal Input to Signal Output	TPHL TPLH	VDD = 5V, VIN = VDD or GND (Notes 1, 2)	9	+25°C	-	100	ns
			10, 11	+125°C, -55°C	-	135	ns
Propagation Delay Turn On	TPZH TPZL	VDD = 5V, VIN = VDD or GND (Notes 2, 3)	9	+25°C	-	70	ns
			10, 11	+125°C, -55°C	-	95	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.
3. CL = 50pF, RL = 1K, TR, TF < 20ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.25	µA
				+125°C	-	7.5	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	15	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	30	µA
Input Voltage Control, Low	VILC	VDD = 10V, VOS = VDD, VIS = VSSand VOS = VSS, VIS = VDD IIISI < 10µA	1, 2	+25°C-55°C	-	0.7	V
				+125°C	-	0.4	V
				-55°C	-	0.9	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage Control, High (See Figure 12)	VIHC	VDD = 10V, VIS = VDD or GND	1, 2	+25°C-55°C	7	-	V
			1, 2	+125°C	7	-	V
			1, 2	-55°C	7	-	V
Propagation Delay Signal Input to Signal Output	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V	1, 2, 3	+25°C	-	30	ns
Propagation Delay Turn On	TPZH TPZL	VDD = 10V	1, 2, 4	+25°C	-	40	ns
		VDD = 15V	1, 2, 4	+25°C	-	30	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K. Input TR, TF < 20ns.
4. CL = 50pF, RL = 1K

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	2.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - SSI	IDD	±0.1µA
ON Resistance	RONDEL10	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		METHOD	GROUP A SUBGROUPS	READ AND RECORD
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

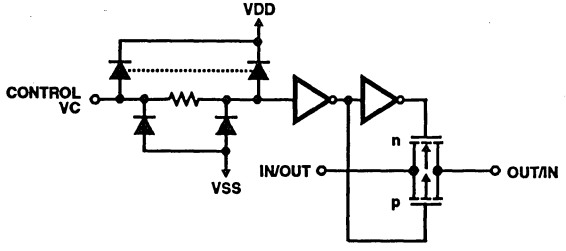
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	2, 3, 9, 10	1, 4-8, 11-13	14			
Static Burn-In 2 Note 1	2, 3, 9, 10	7	1, 4-6, 8, 11-14			
Dynamic Burn-In Note 1	-	7	14	2, 3, 9, 10	5, 6, 12, 13	1, 4, 8, 11
Irradiation Note 2	2, 3, 9, 10	7	1, 4-6, 8, 11-14			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Schematic Diagram



Typical Performance Characteristics

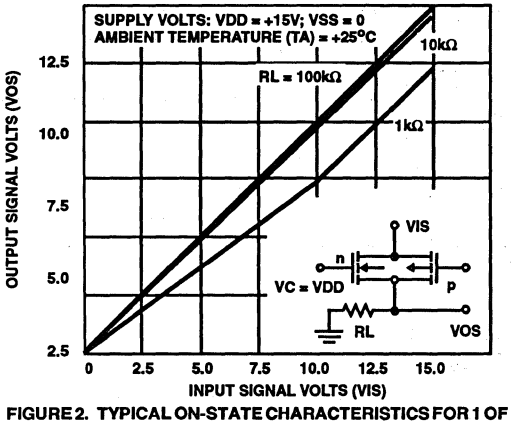


FIGURE 2. TYPICAL ON-STATE CHARACTERISTICS FOR 1 OF 4 SWITCHES WITH VDD = +15V, VSS = 0V

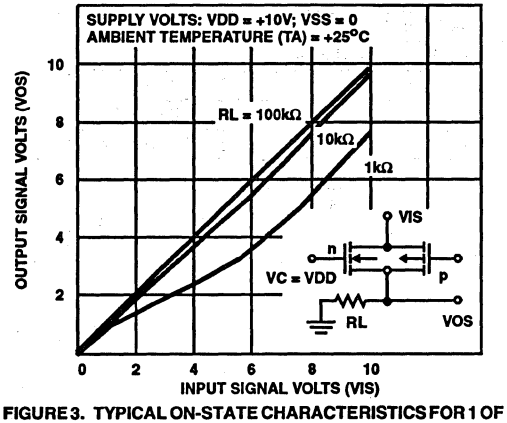


FIGURE 3. TYPICAL ON-STATE CHARACTERISTICS FOR 1 OF 4 SWITCHES WITH VDD = +10V, VSS = 0V

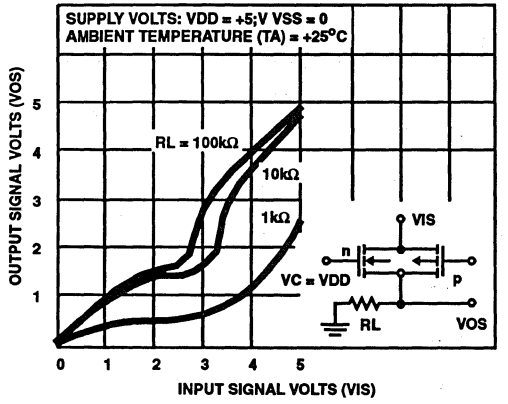


FIGURE 4. TYPICAL ON-STATE CHARACTERISTICS FOR 1 OF 4 SWITCHES WITH VDD = +5V, VSS = 0V

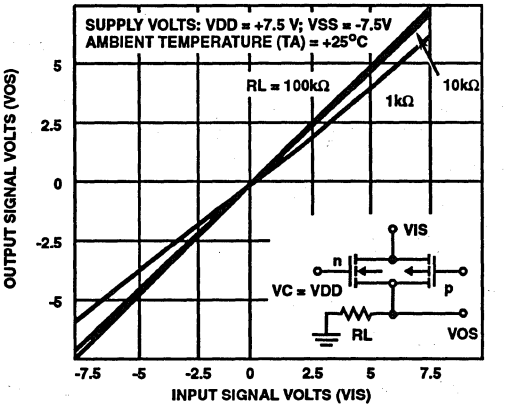


FIGURE 5. TYPICAL ON-STATE CHARACTERISTICS FOR 1 OF 4 SWITCHES WITH VDD = +7.5V, VSS = -7.5V

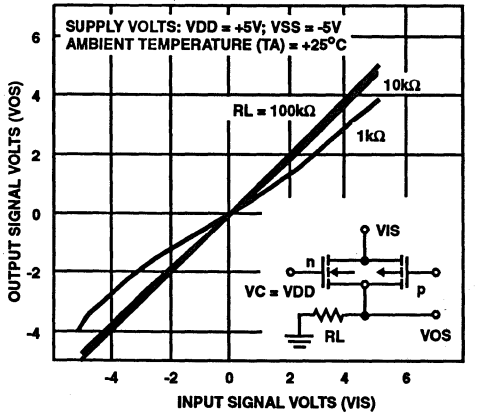


FIGURE 6. TYPICAL ON-STATE CHARACTERISTICS FOR 1 OF 4 SWITCHES WITH VDD = +5V, VSS = -5V

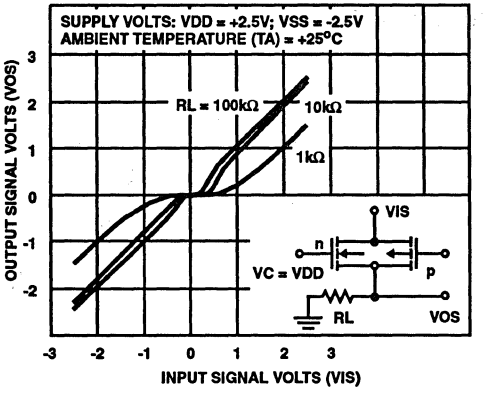


FIGURE 7. TYPICAL ON-STATE CHARACTERISTICS FOR 1 OF 4 SWITCHES WITH VDD = +2.5V, VSS = -2.5V

Typical Performance Characteristics (Continued)

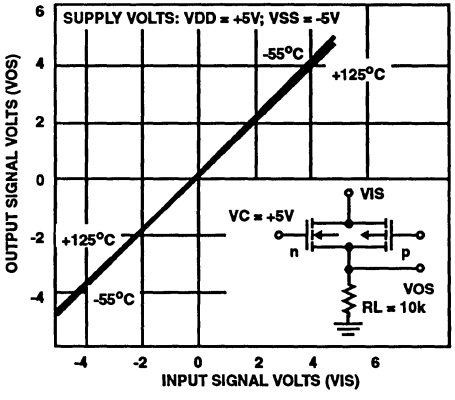


FIGURE 8. TYPICAL ON-STATE CHARACTERISTICS AS A FUNCTION OF TEMPERATURE FOR 1 OF 4 SWITCHES WITH VDD = +5V, VSS = -5V

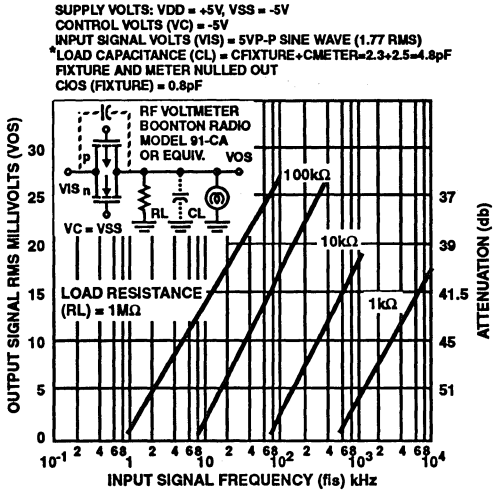


FIGURE 9. TYPICAL FEEDTHRU vs FREQUENCY - SWITCH OFF

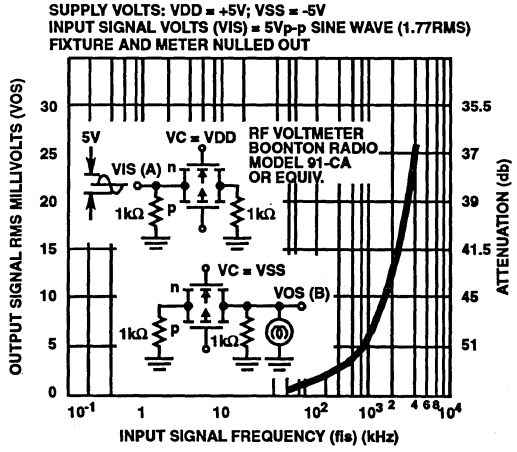


FIGURE 10. TYPICAL CROSSTALK BETWEEN SWITCH CIRCUITS IN THE SAME PACKAGE

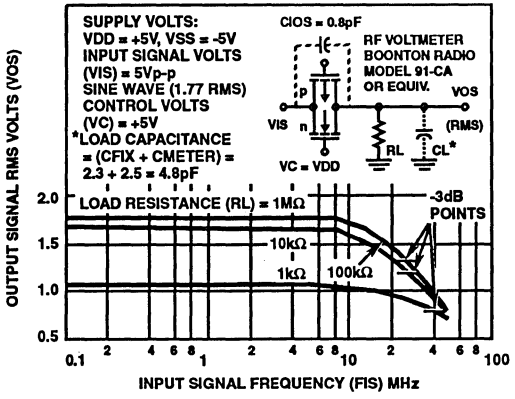
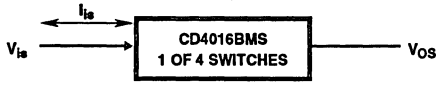


FIGURE 11. TYPICAL FREQUENCY RESPONSE - SWITCH ON



$$r_{on} = \frac{[\ V_{is} - V_{oe}\ ]}{[\ I_{is}\ ]}$$

FIGURE 12. DETERMINATION OF RON AS A TEST CONDITION FOR CONTROL INPUT HIGH VOLTAGE (VIHC) SPECIFICATION

TYPICAL ON-STATE RESISTANCE CHARACTERISTICS, T_A = +25°C

CHARACTERISTICS*	SUPPLY CONDITIONS		LOAD CONDITIONS					
			RL = 1kΩ		RL = 10kΩ		RL = 100kΩ	
	VDD (V)	VSS (V)	VALUE (Ω)	Vis (V)	VALUE (Ω)	Vis (V)	VALUE (Ω)	Vis (V)
RON	+15	0	200	+15	200	+15	180	+15
			200	0	200	0	200	0
RON (max.)	+15	0	300	+11	300	+9.3	320	+9.2
RON	+10	0	290	+10	250	+10	240	+10
			290	0	250	0	300	0
RON (max.)	+10	0	500	+7.4	560	+5.6	610	+5.5
RON	+5	0	860	+5	470	+5	450	+5
			600	0	580	0	800	0
RON (max.)	+5	0	1.7k	+4.2	7k	+2.9	33k	+2.7
RON	+7.5	-7.5	200	+7.5	200	+7.5	180	+7.5
			200	-7.5	200	-7.5	180	-7.5
RON (max.)	+7.5	-7.5	290	±0.25	280	±0.25	400	±0.25
RON	+5	-5	260	+5	250	+5	240	+5
			310	-5	250	-5	240	-5
RON (max.)	+5	-5	600	±0.25	580	±0.25	760	±0.25
RON	+2.5	-2.5	590	+2.5	450	+2.5	490	+2.5
			720	-2.5	520	-2.5	520	-2.5
RON (max.)	+2.5	-2.5	232k	±0.25	300k	±0.25	870k	±0.25

*Variation from perfect switch, ron = 0Ω

Typical Wave Response

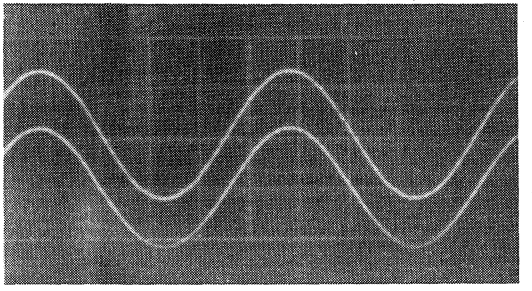


FIGURE 13. TYPICAL SINE WAVE RESPONSE OF VDD = +7.5V, VSS = -7.5V

Scale X = 0.2ms/Div Y = 2.0V/Div
VDD = VC = +7.5V, RL = 10KΩ
CL = 15pF
fis = 1kHz VIS = 5Vp-p
Distortion = 0.2%

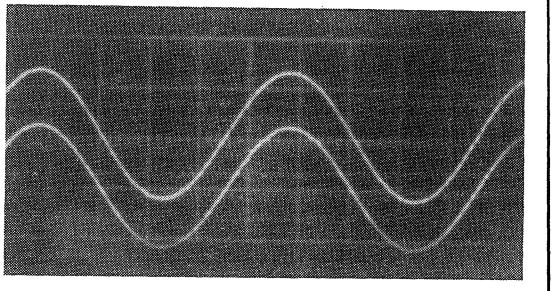


FIGURE 14. TYPICAL SINE WAVE RESPONSE OF VDD = +5V, VSS = -5V

Scale X = 0.2ms/Div Y = 2.0V/Div
VDD = VC = +5V, RL = 10KΩ
CL = 15pF
fis = 1kHz VIS = 5Vp-p
Distortion = 0.4%

Typical Wave Response (Continued)

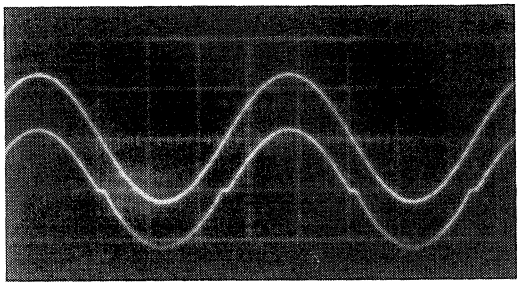


FIGURE 15. TYPICAL SINE WAVE RESPONSE OF VDD = +2.5V, VSS = -2.5V

Scale: X = 0.2ms/Div Y = 2.0V/Div

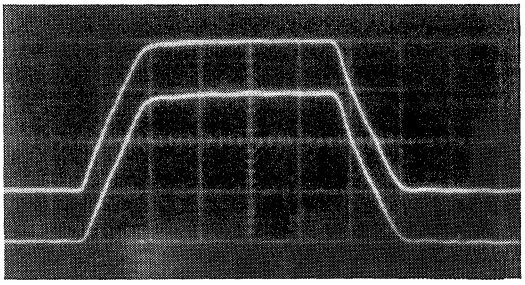


FIGURE 16. TYPICAL SQUARE WAVE RESPONSE AT VDD = VC = +15V, VSS = GND

Scale: X = 100ns/Div Y = 5.0V/Div

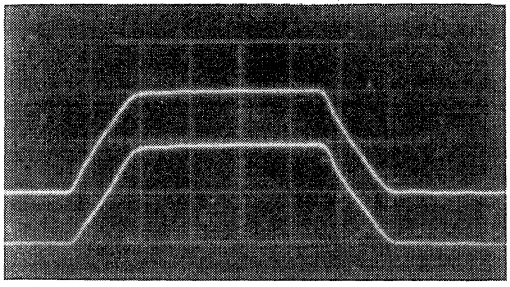


FIGURE 17. TYPICAL SQUARE WAVE RESPONSE AT VDD = VC = +10V, VSS = GND

Scale: X = 100ns/Div Y = 5.0V/Div

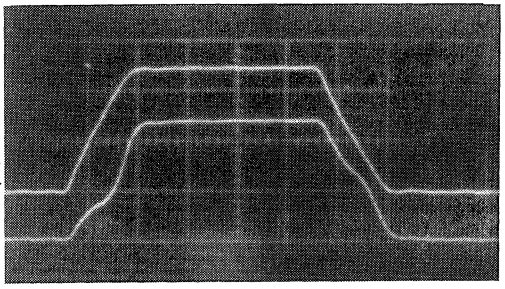
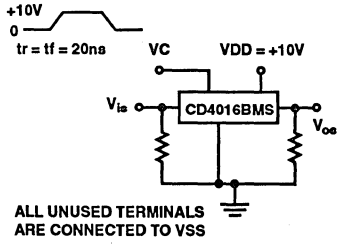
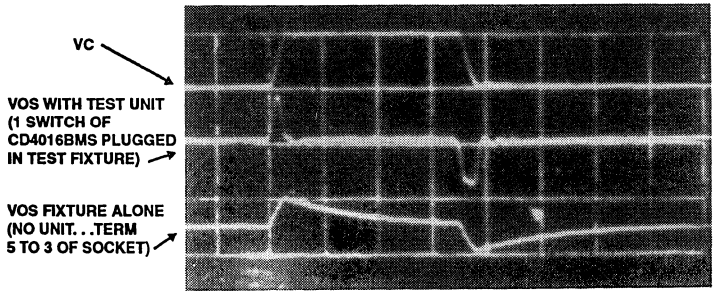


FIGURE 18. TYPICAL SQUARE WAVE RESPONSE AT VDD = VC = +5V, VSS = GND

Scale: X = 100ns/Div Y = 2.0V/Div



(a)



(b)

VC = 10V/Div
VOS = 0.2V/Div
t = 100ns/Div

FIGURE 19. CROSSTALK-CONTROL INPUT TO SIGNAL OUTPUT

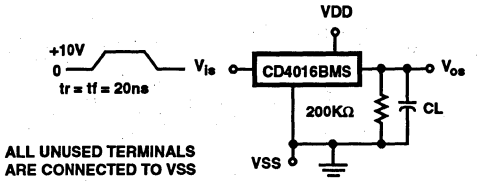


FIGURE 20. PROPAGATION DELAY TIME SIGNAL INPUT (VIS) TO SIGNAL OUTPUT (VOS)

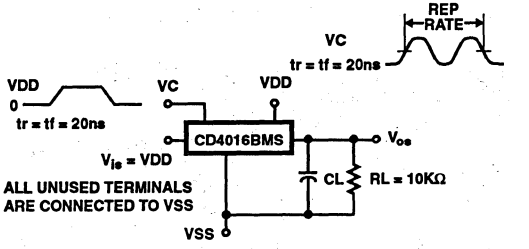
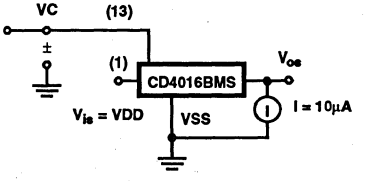


FIGURE 21. MAXIMUM CONTROL-INPUT REPETITION RATE



SWITCH THRESHOLD VOLTAGE IS DEFINED AS THE VOLTAGE APPLIED TO A TRANSMISSION GATE CONTROL WHICH CAUSES 10μA OF TRANSMISSION GATE CURRENT

FIGURE 22. SWITCH THRESHOLD VOLTAGE

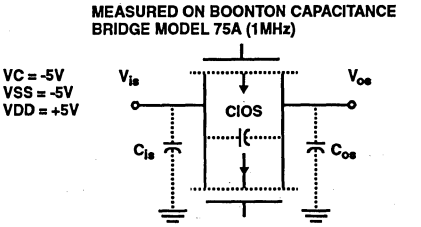
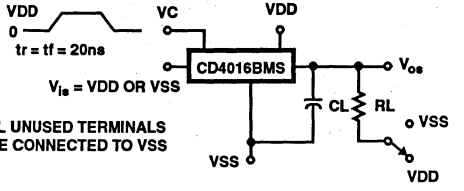


FIGURE 23. CAPACITANCE CIOS AND COS



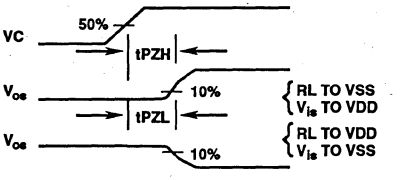
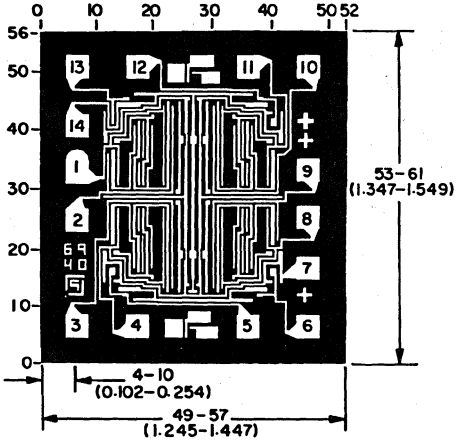


FIGURE 24. TURN-ON PROPAGATION DELAY CONTROL INPUT

Chip Dimensions and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 i

HARRIS SEMICONDUCTOR

CD4017BMS CD4022BMS

December 1992

CMOS Counter/Dividers

Features

- High Voltage Types (20V Rating)
- Fully Static Operation
- Medium-Speed Operation 10MHz (Typ) at VDD = 10V
- Standardized Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard Number 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Decade Counter/Decimal Decode Display (CD4017BMS)
- Binary Counter/Decoder
- Frequency Division
- Counter Control/Timers
- Divide-by-N Counting
- For Further Application Information, See ICAN-6166 "COS/MOS MSI Counter and Register Design and Applications"

Description

CD4017BMS - Decade Counter with 10 Decoded Outputs
CD4022BMS - Octal Counter with 8 Decoded Outputs

CD4017BMS and CD4022BMS are 5-stage and 4-stage Johnson counters having 10 and 8 decoded outputs, respectively. Inputs include a CLOCK, a RESET, and a CLOCK INHIBIT signal. Schmitt trigger action in the CLOCK input circuit provides pulse shaping that allows unlimited clock input pulse rise and fall times.

These counters are advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. A high RESET signal clears the counter to its zero count. Use of the Johnson counter configuration permits high speed operation, 2-input decode gating and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counter sequence. The decoded output are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A CARRY-OUT signal completes one cycle every 10 clock input cycles in the CD4017BMS or every 8 clock input cycles in the CD4022BMS and is used to ripple-clock the succeeding device in a multi-device counting chain.

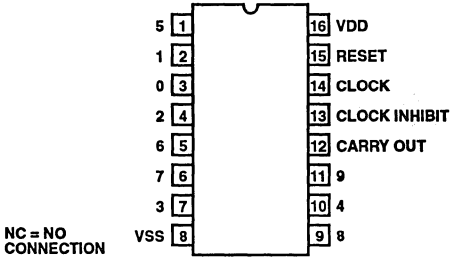
The CD4017BMS and CD4022BMS series types are supplied in these 16 lead outline packages

Braze Seal DIP	*H4W	†H4X
Frit Seal DIP	*H1F	†H1E
Ceramic Flatpack	H6W	

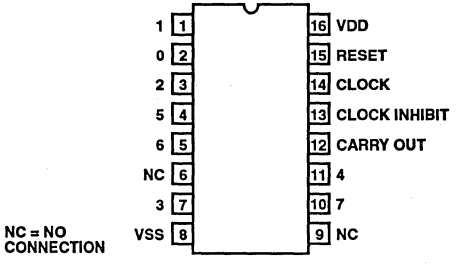
*CD4017B Only † CD4022B Only

Pinouts

CD4017BMS
TOP VIEW

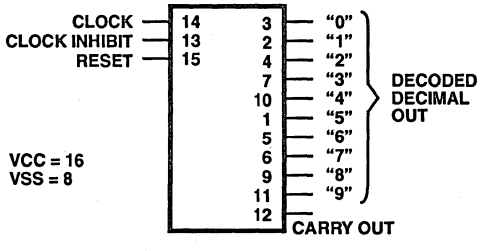


CD4022BMS
TOP VIEW

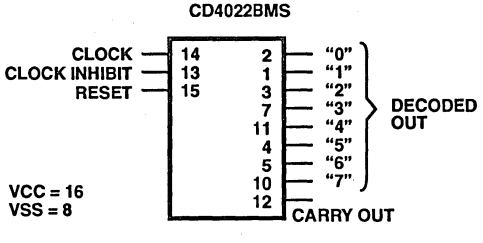


Functional Diagrams

CD4017BMS



CD4022BMS



7 LOGIC

File Number 3297

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (Note 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Decode Out	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	650	ns
			10, 11	+125°C, -55°C	-	878	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (Note 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Carry Out	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Propagation Delay Reset to Out	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	530	ns
			10, 11	+125°C, -55°C	-	716	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	2.5	-	MHz
			10, 11	+125°C, -55°C	1.85	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Clock to Decode Out	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	270	ns
		VDD = 15V	1, 2, 3	+25°C	-	170	ns
Propagation Delay Clock to Carry Out	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	250	ns
		VDD = 15V	1, 2, 3	+25°C	-	160	ns
Propagation Delay Reset to out	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25°C	-	230	ns
		VDD = 15V	1, 2, 3	+25°C	-	170	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	5.0	-	MHz
		VDD = 15V	1, 2, 3	+25°C	5.5	-	MHz
Minimum Setup Time Clock Inhibit to Clock Setup	TS	VDD = 5V	1, 2, 3	+25°C	-	230	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	70	ns
Minimum Reset Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	260	ns
		VDD = 10V	1, 2, 3	+25°C	-	110	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	90	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.7	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

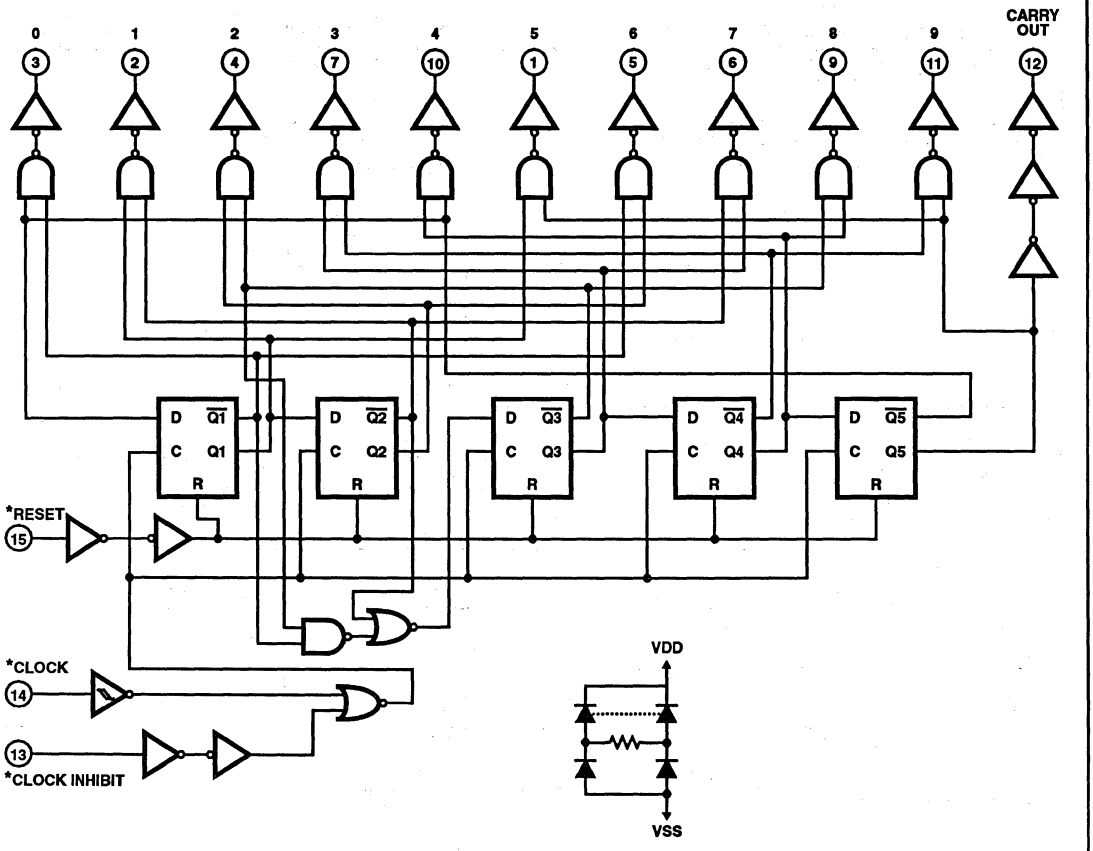
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
PART NUMBER CD4017BMS AND CD4002B						
Static Burn-In 1 Note 1	1 - 7, 9 - 12	8, 13, 15	14, 16	-	-	-
Static Burn-In 2 Note 1	1 - 7, 9 - 12	8, 14	13, 15, 16	-	-	-
Dynamic Burn-In Note 1	-	8, 13, 15	16	1 - 7, 9 - 12	14	-
Irradiation Note 2	1 - 7, 9 - 12	8	13 - 16	-	-	-

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram



* All Inputs Protected by CMOS Protection Network

FIGURE 1. CD4017BMS

Logic Diagram (Continued)

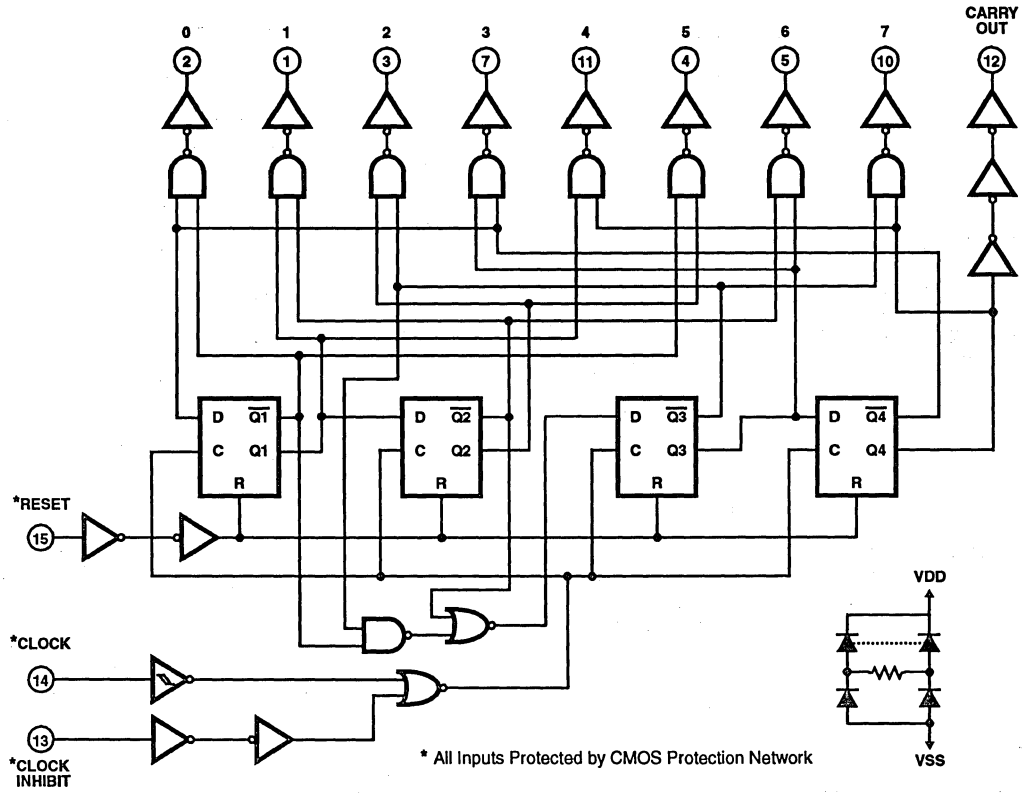


FIGURE 2. CD4022BMS

Timing Diagram

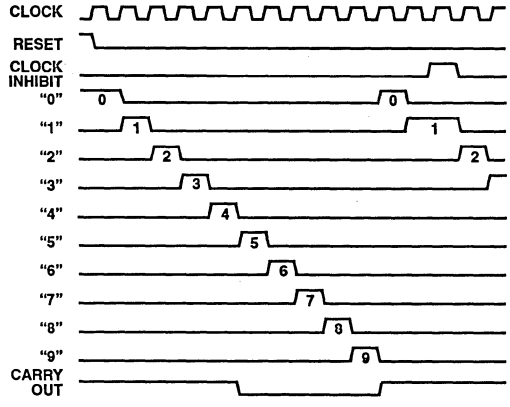


FIGURE 3. CD4017BMS

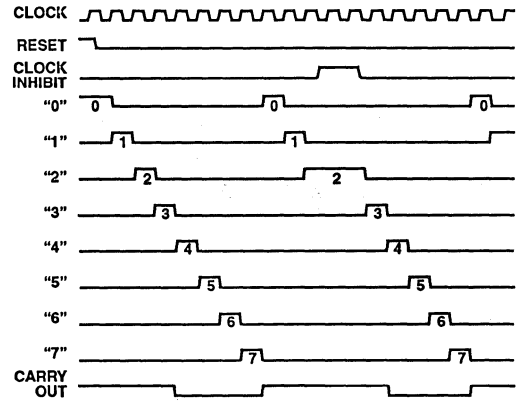


FIGURE4. CD4022BMS

Typical Performance Characteristics

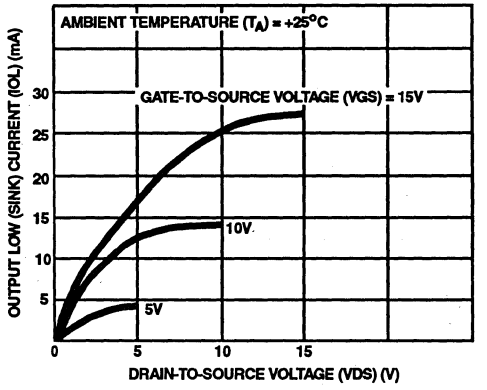


FIGURE 5. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

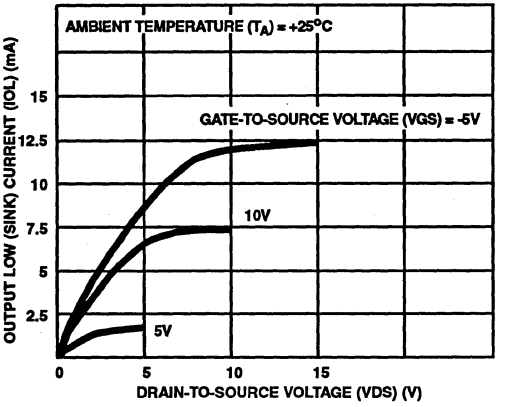


FIGURE 6. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

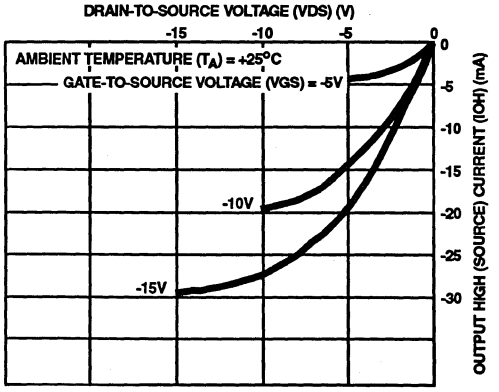


FIGURE 7. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

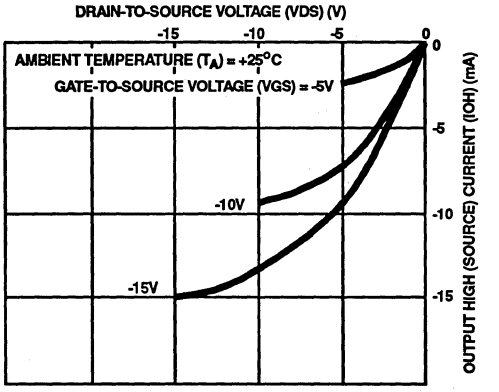


FIGURE 8. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

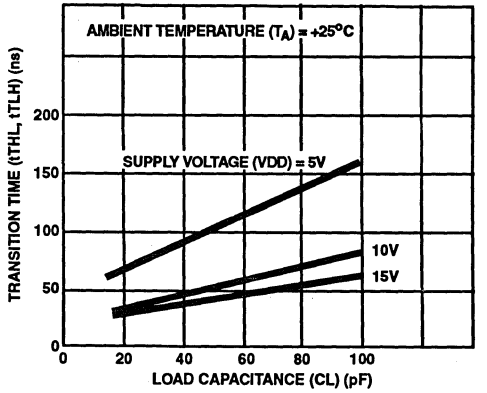


FIGURE 9. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

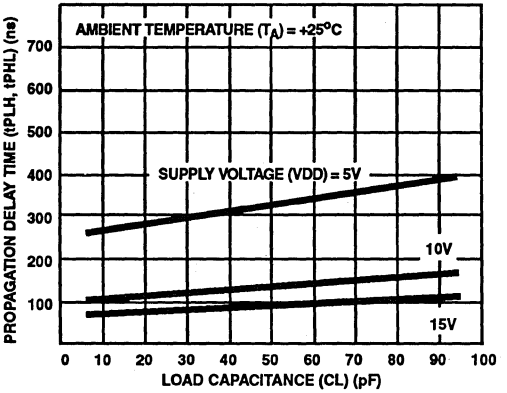


FIGURE 10. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (CLOCK TO DECODE OUTPUT)

Typical Performance Characteristics (Continued)

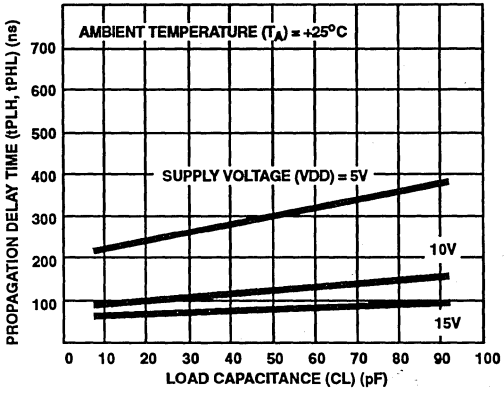


FIGURE 11. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (CLOCK TO CARRY OUT)

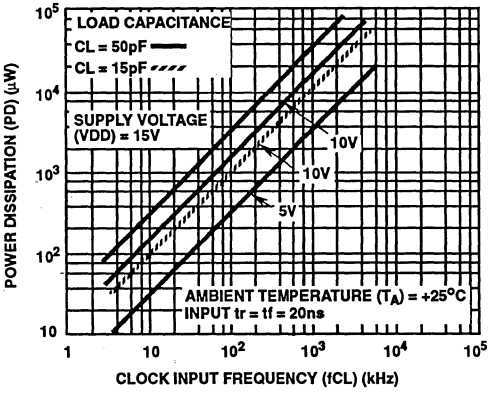
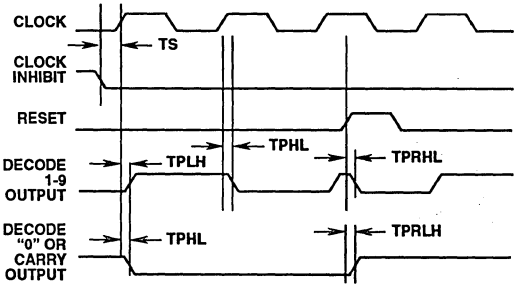


FIGURE 12. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF CLOCK INPUT FREQUENCY

When the N^{th} decoded output is reached (N^{th} clock pulse) the S-R flip-flop (constructed from two NOR gates of the CD4001B) generates a reset pulse which clears the CD4017BMS or CD4022BMS to its zero count. At this time, if the N^{th} decoded output is greater than or equal to 6 in the CD4017BMS or 5 in the CD4022BMS, the C_{OUT} line goes high to clock the next CD4017BMS or CD4022BMS counter section. The "0" decoded output also goes high at this time. Coincidence of the clock low and decoded "0" output low resets the S-R flip-flop to enable the CD4017BMS or CD4022BMS. If the N^{th} decoded output is less than 6 (CD4017BMS) or 5 (CD4022BMS), the C_{OUT} line will not go high and, therefore, cannot be used. In this case "0" decoded output may be used to perform the clocking function for the next counter.



Delays Measured Between 50% levels on All Waveforms

FIGURE 13. PROPAGATION DELAY, SETUP, AND RESET REMOVAL TIME WAVEFORMS

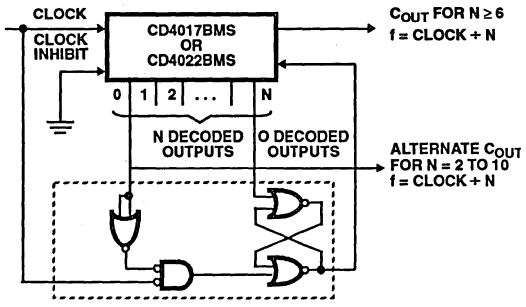


FIGURE 14. DIVIDE BY N COUNTER (N ≤ 10) WITH N DECODED OUTPUTS

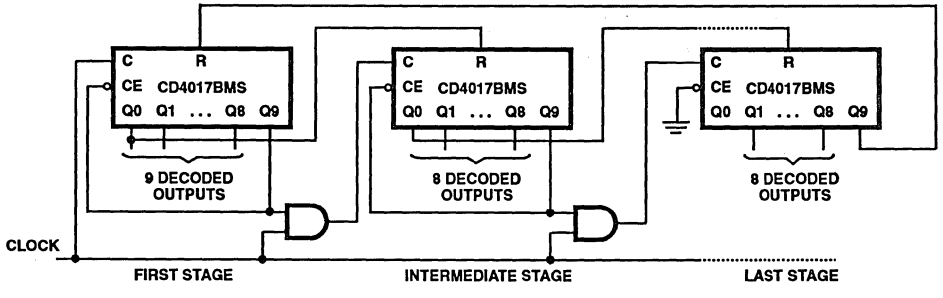
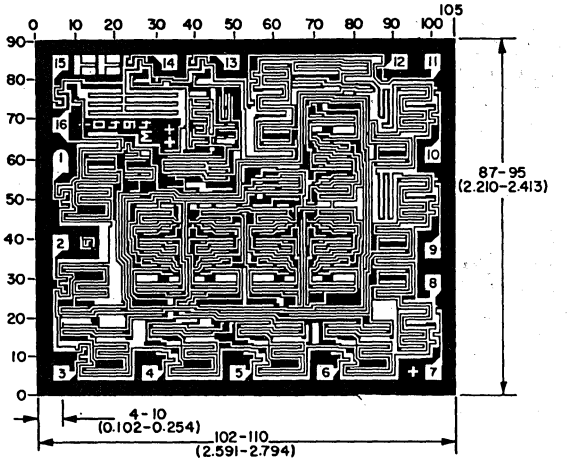
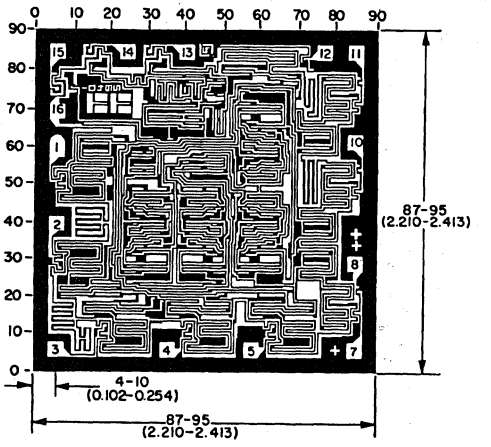


FIGURE 15. CASCADING THE CD4017BMS

Chip Dimensions and Pad Layouts



CD4017BMSH



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

CD4022BMSH

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218

HARRIS SEMICONDUCTOR

CD4018BMS

CMOS Presettable Divide-By- "N" Counter

December 1992

Features

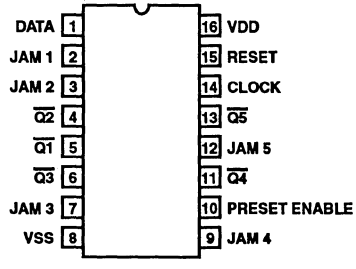
- High Voltage Type (20V Rating)
- Medium Speed Operation 10MHz (typ.) at VDD - VSS = 10V
- Fully Static Operation
- 100% Tested for Quiescent Current at 20V
- Standardized Symmetrical Output Characteristics
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μa at 18V Over Full Package-Temperature Range;
  - 100nA at 18V and 25°C
- Noise Margin (Over Full Package Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Fixed and Programmable Divided- By-10, 9, 8, 7, 6, 5, 4, 3, 2 Counters
- Fixed and Programmable Counters Greater Than 10
- Programmable Decade Counters
- Divide-By- "N" Counters/Frequency Synthesizers
- Frequency Division
- Counter Control/Timers

Pinout

CD4018BMS
TOP VIEW



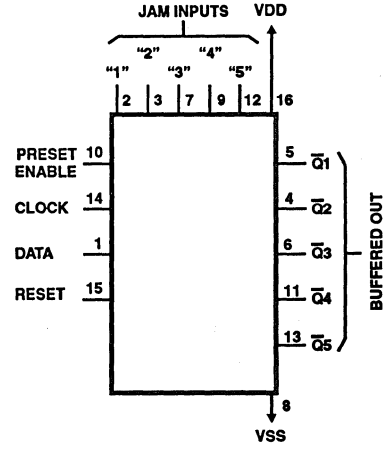
Description

CD4018BMS types consist of 5 Johnson-Counter stages, buffered Q outputs from each stage, and counter preset control gating. CLOCK, RESET, DATA, PRESET ENABLE, and 5 individual JAM inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the $\overline{Q5}$, $\overline{Q4}$, $\overline{Q3}$, $\overline{Q2}$, $\overline{Q1}$ signals, respectively, back to the DATA input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by the use of a CD4011B to gate the feedback connection to the DATA input. Divide-by functions greater than 10 can be achieved by use of multiple CD4018BMS units. The counter is advanced one count at the positive clock-signal transition. Schmitt Trigger action on the clock line permits unlimited clock rise and fall times. A high RESET signal clears the counter to an all-zero condition. A high PRESET-ENABLE signal allows information on the JAM inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

The CD4018BMS is supplied in these 16-lead outline packages:

Braze Seal DIP	H4T
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

Functional Diagram



7 LOGIC

File Number 3298

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

	θ_{ja}	θ_{jc}
Thermal Resistance		
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock To $\overline{Q}$	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay Preset To $\overline{Q}$	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	550	ns
			10, 11	+125°C, -55°C	-	743	ns
Propagation Delay Reset To $\overline{Q}$	TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	550	ns
			10, 11	+125°C, -55°C	-	743	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Clock To $\overline{Q}$	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	180	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Propagation Delay Preset To $\overline{Q}$	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	250	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Reset to $\overline{Q}$	TPLH3	VDD = 10V	1, 2, 3	+25°C	-	250	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 5V	1, 2, 3	+25°C	3	-	MHz
		VDD = 10V	1, 2, 3	+25°C	7	-	MHz
		VDD = 15V	1, 2, 3	+25°C	8.5	-	MHz
Minimum Data Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	40	ns
		VDD = 10V	1, 2, 3	+25°C	-	12	ns
		VDD = 15V	1, 2, 3	+25°C	-	6	ns
Minimum Data Hold Time	TH	VDD = 5V	1, 2, 3	+25°C	-	140	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	160	ns
		VDD = 10V	1, 2, 3	+25°C	-	70	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Preset/Reset Removal Time	TREM	VDD = 5V	1, 2, 3	+25°C	-	80	ns
		VDD = 10V	1, 2, 3	+25°C	-	30	ns
		VDD = 15V	1, 2, 3	+25°C	-	20	ns
Minimum Preset/Reset Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	160	ns
		VDD = 10V	1, 2, 3	+25°C	-	70	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTND	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTPD	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	4 - 6, 11, 13	1 - 3, 7 - 9, 10, 12, 14, 15	16			
Static Burn-In 2 Note 1	4 - 6, 11, 13	8	1 - 3, 7, 9, 10, 12, 14 - 16			
Dynamic Burn-In Note 1	-	2, 8, 9, 15	1, 3, 12, 16	4 - 6, 11, 13	7, 14	10
Irradiation Note 2	4 - 6, 11, 13	8	1 - 3, 7, 9, 10, 12, 14 - 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram

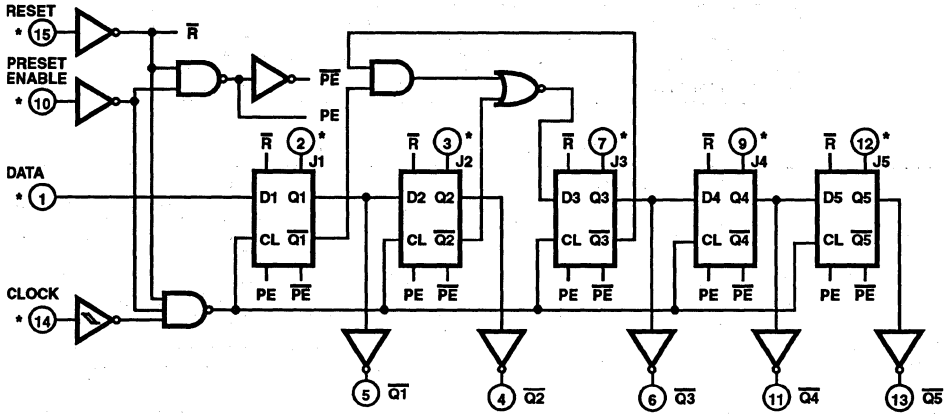


FIGURE 1. LOGIC DIAGRAM

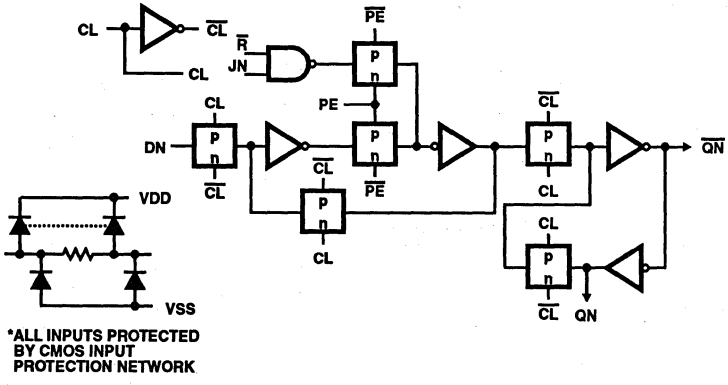


FIGURE 2. DETAIL OF A TYPICAL STAGE

Typical Performance Characteristics

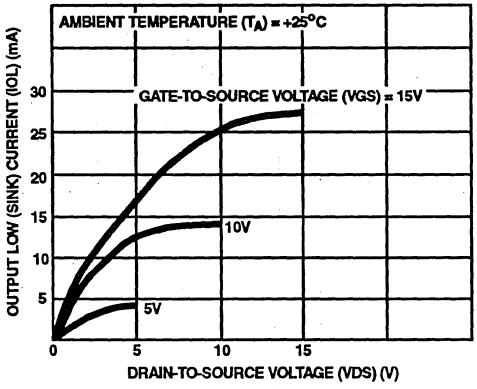


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

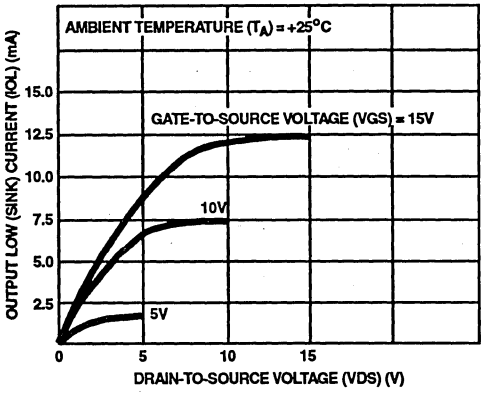


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

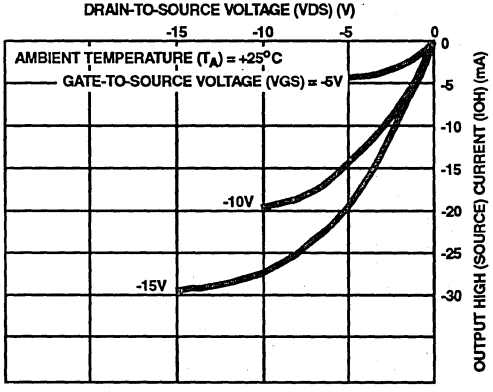


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

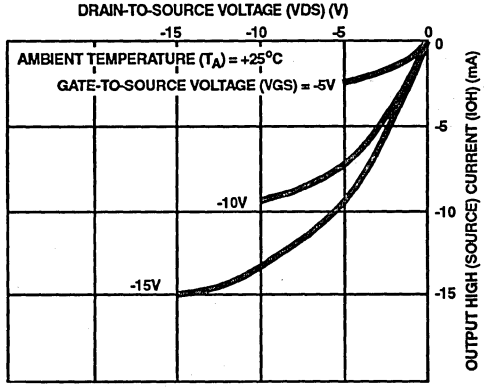


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

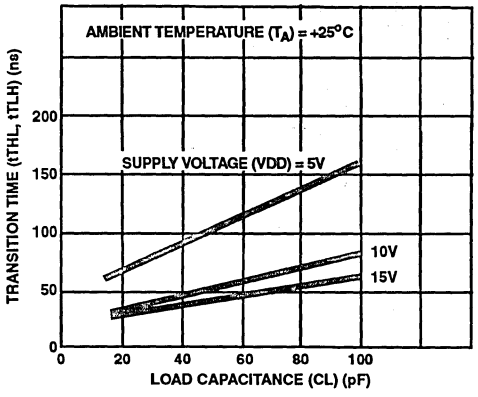


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

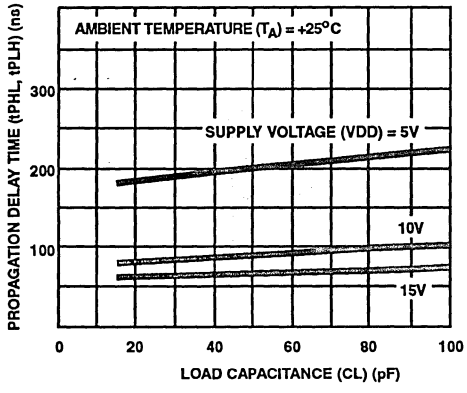


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (CLOCK TO Q)

Typical Performance Characteristics (Continued)

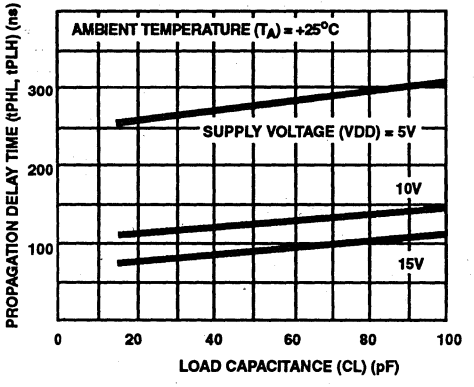


FIGURE 9. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (RESET TO Q)

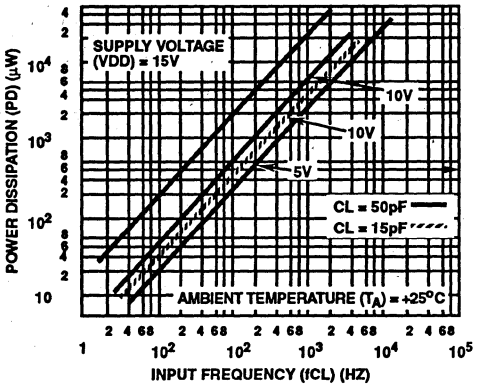


FIGURE 10. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF CLOCK INPUT FREQUENCY

Timing Diagram

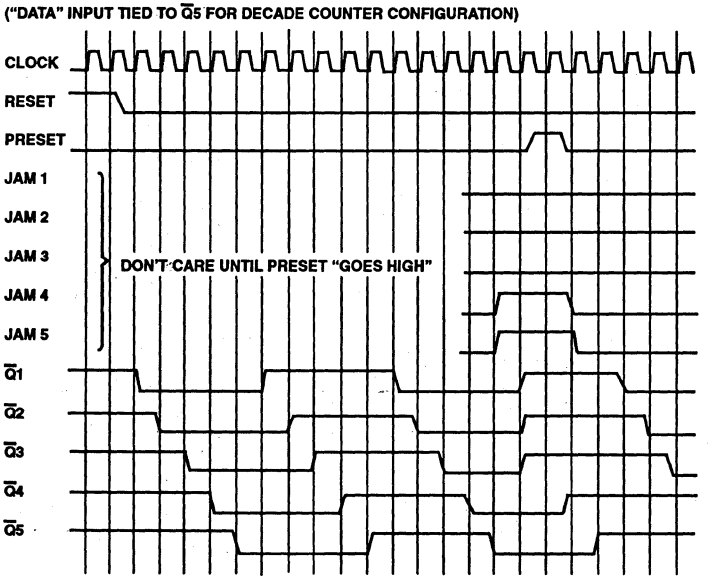
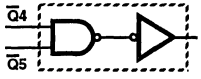


FIGURE 11. TIMING DIAGRAM

EXTERNAL CONNECTIONS FOR DIVIDE BY 10, 9, 8, 7, 6, 5, 4, 3, OPERATION

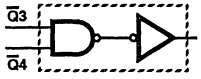
DIVIDE BY 10	$\overline{Q5}$	Connected Back To "Data"	No External Components Required
DIVIDE BY 8	$\overline{Q4}$	Connected Back To "Data"	No External Components Required
DIVIDE BY 6	$\overline{Q3}$	Connected Back To "Data"	No External Components Required
DIVIDE BY 4	$\overline{Q2}$	Connected Back To "Data"	No External Components Required
DIVIDE BY 2	$\overline{Q1}$		

DIVIDE BY 9
1/2 CD4011B



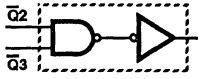
CONNECTED BACK TO "DATA" (SKIPS "ALL-1's" STATE)

DIVIDE BY 7
1/2 CD4011B



CONNECTED BACK TO "DATA" (SKIPS "ALL-1's" STATE)

DIVIDE BY 5
1/2 CD4011B



CONNECTED BACK TO "DATA" (SKIPS "ALL-1's" STATE)

DIVIDE BY 3
1/2 CD4011B

CONNECTED BACK TO "DATA" (SKIPS "ALL-1's" STATE)

FIGURE 12. EXTERNAL CONNECTIONS FOR DIVIDE BY 10, 9, 8, 7, 6, 5, 4, 3, 2 OPERATION

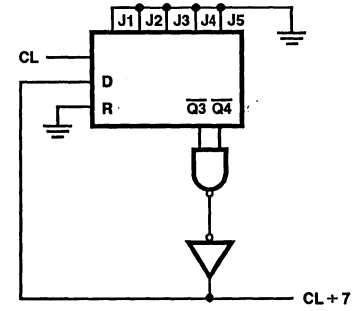
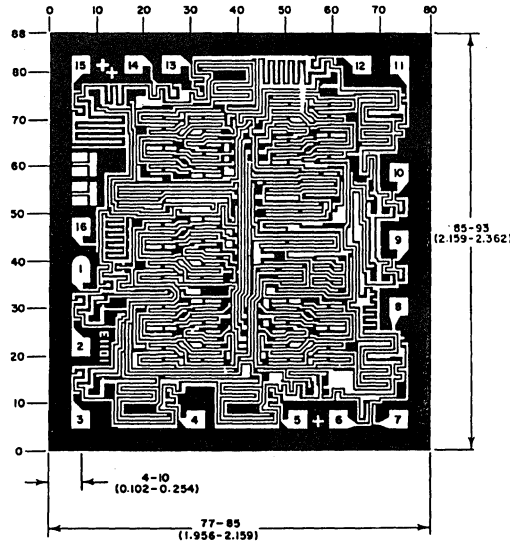


FIGURE 13. EXAMPLE OF DIVIDE BY 7

Chip Dimensions and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4019BMS

December 1992

CMOS Quad AND/OR Select Gate

Features

- High Voltage Type (20V Rating)
- Medium Speed Operation tPHL = tPLH = 60ns (typ.) at CL = 50pF, VDD = 10V
- Standardized Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Maximum Input Current of 1μa at 18V Over Full Package-Temperature Range;
  - 100nA at 18V and 25°C
- Noise Margin (Over Full Package Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V

Applications

- And/Or Select Gating
- Shift-Right/Shift-Left Registers
- True/Complement Selection
- AND/OR/Exclusive-OR Selection

Description

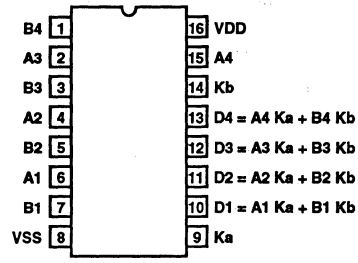
CD4019BMS types consist of four AND/OR select gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits Ka and Kb. In addition to selection of either channel A or channel B information, the control bits can be applied simultaneously to accomplish the logical A + B function.

The CD4019BMS is supplied in these 16-lead outline packages:

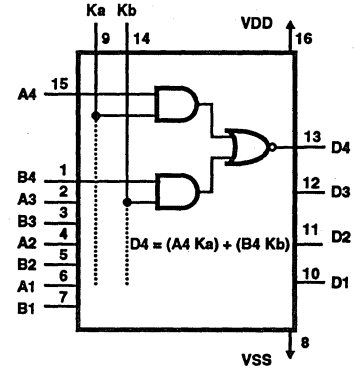
Braze Seal DIP	H4T
Frit Seal DIP	H1E
Ceramic Flatpack	H3X

Pinout

CD4019BMS
TOP VIEW



Functional Diagram



File Number 3299

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	300	ns
			10, 11	+125°C, -55°C	-	405	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	120	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	All A and B Inputs	1, 2	+25°C	-	7.5	pF
Input Capacitance	CIN	KA and KB Inputs	1, 2	+25°C	-	15.0	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	10 -13	1 - 9, 14, 15	16			
Static Burn-In 2 Note 1	10 -13	8	1 - 7, 9, 14 - 16			
Dynamic Burn-In Note 1	-	8	16	10 - 13	-	1 - 7, 9, 14, 15
Irradiation Note 2	10 -13	8	1 - 7, 9, 14 - 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

TRUTH TABLE

Ka	Kb	An	Bn	Dn
1	0	1	X	1
1	0	0	X	0
0	1	X	1	1
0	1	X	0	0
0	0	X	X	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

X = Don't Care Case

Typical Performance Characteritics

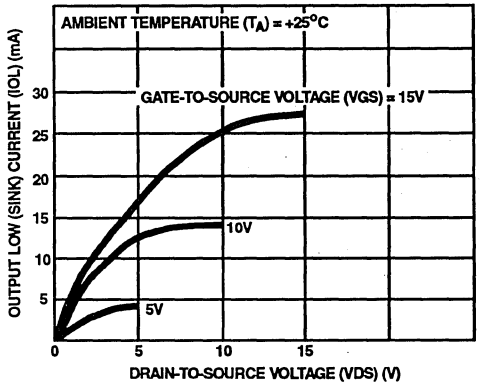


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

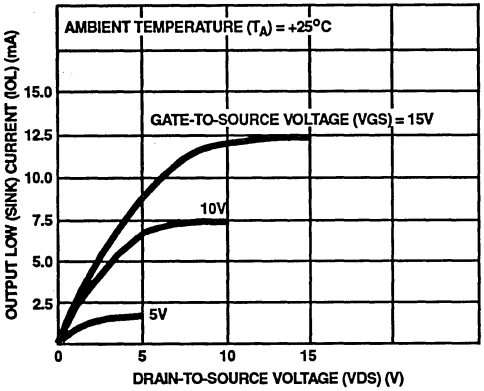


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

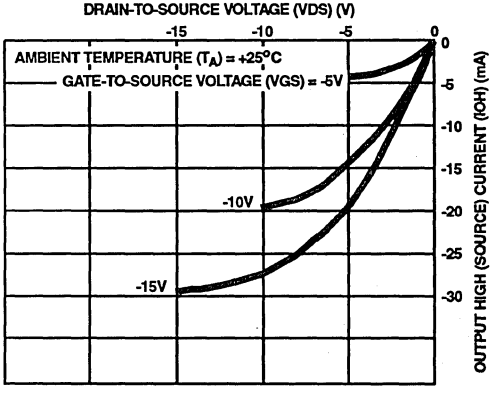


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

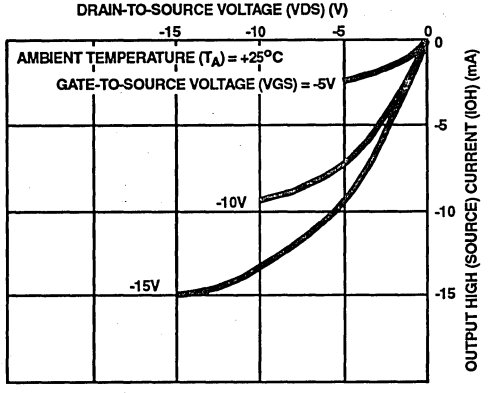


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

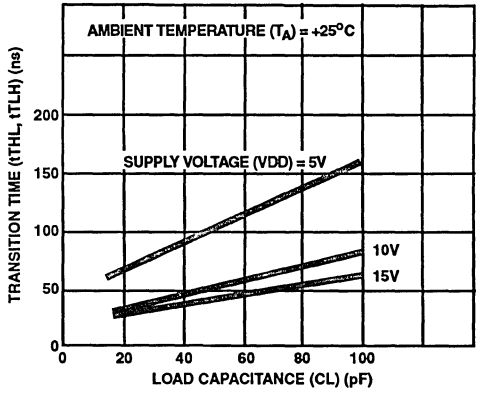


FIGURE 6. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

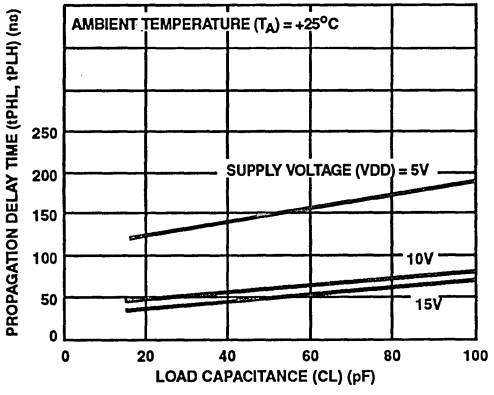


FIGURE 7. PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteritics (Continued)

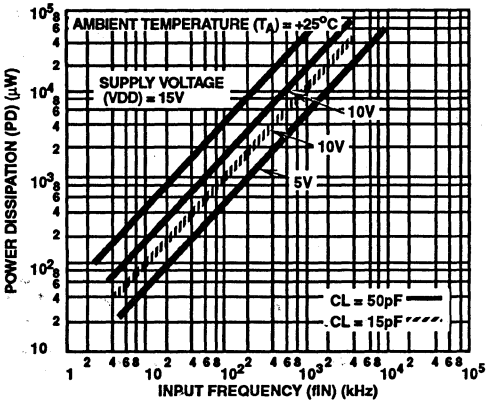


FIGURE 8. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

Typical Applications

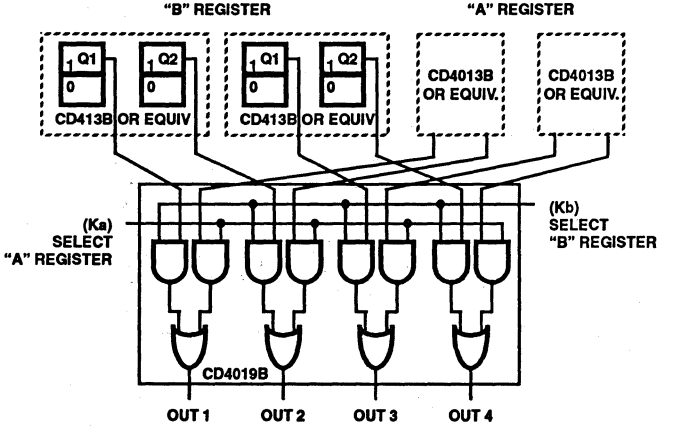


FIGURE 9. AND/OR SELECT GATING

Typical Applications (Continued)

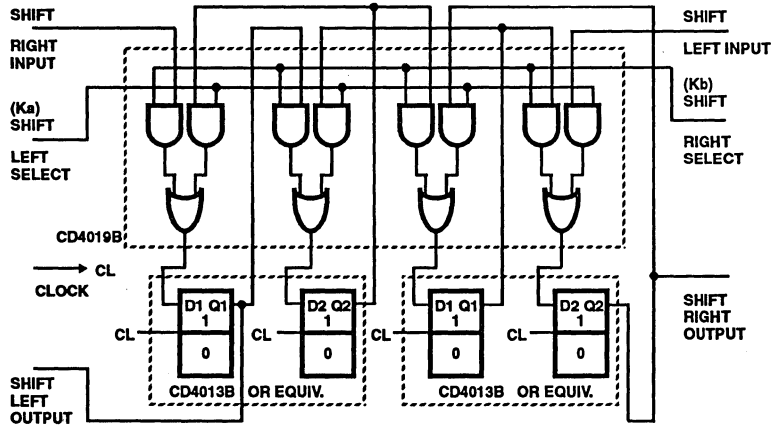


FIGURE 10. "SHIFT LEFT/SHIFT RIGHT" REGISTER

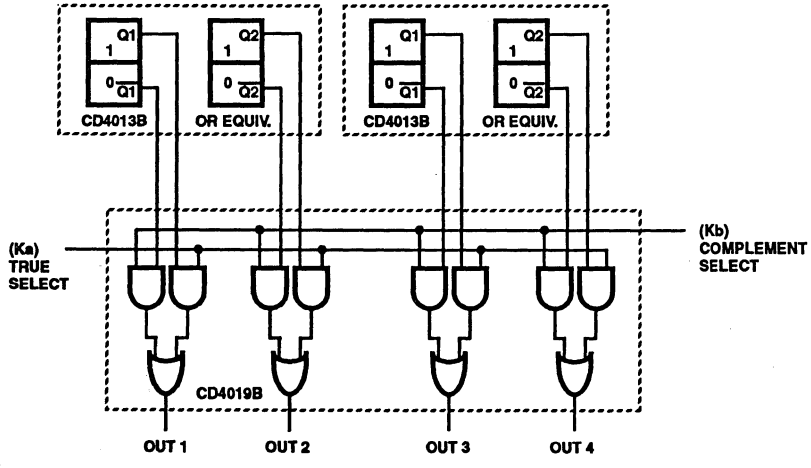


FIGURE 11. "TRUE COMPLEMENT" SELECTOR

Typical Applications (Continued)

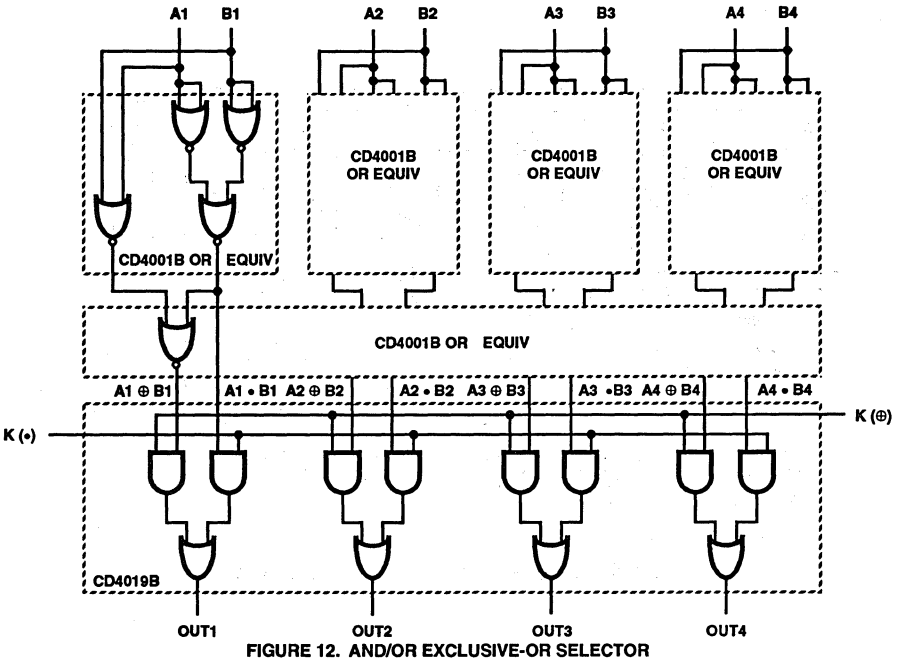
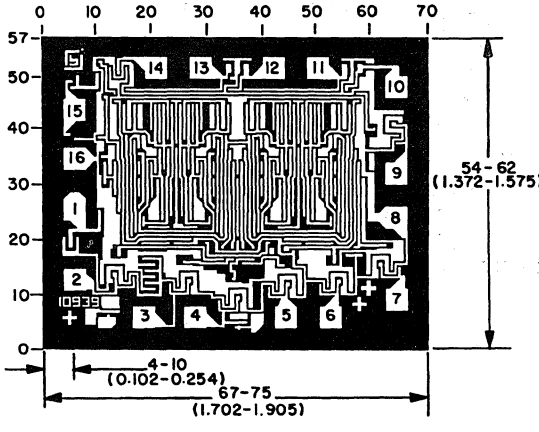


FIGURE 12. AND/OR EXCLUSIVE-OR SELECTOR

TRUTH TABLE

K (•)	K (⊕)	OUT
0	0	0
1	0	A • B
0	1	A ⊕ B
1	1	A + B

Chip Dimensions and Pad Layout



METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

CD4020BMS, CD4024BMS CD4040BMS

CMOS Ripple-Carry Binary Counter/Dividers

December 1992

Features

- High Voltage Types (20V Rating)
- Medium Speed Operation
- Fully Static Operation
- Buffered Inputs and Outputs
- 100% Tested for Quiescent Current at 20V
- Standardized Symmetrical Output Characteristics
- Common Reset
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μa at 18V Over Full Package-Temperature Range;
  - 100nA at 18V and 25°C
- Noise Margin (Over Full Package Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications For Description Of 'B' Series CMOS Devices"

Applications

- Control Counters
- Timers
- Frequency Dividers
- Time-Delay Circuits

Description

CD4020BMS - 14 Stage

CD4024BMS - 7 Stage

CD4040BMS - 12 Stage

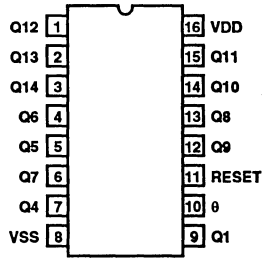
CD4020BMS, CD4024BMS, and CD4040BMS are ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of a counter advances one count on the negative transition of each input pulse; a high level on the RESET line resets the counter to its all zeros state. Schmitt trigger action on the input-pulse line permits unlimited rise and fall times. All inputs and outputs are buffered.

The CD4020BMS, CD4024BMS and the CD4040BMS is supplied in these 14 lead outline packages:

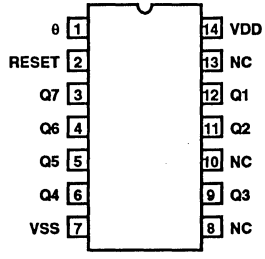
	CD4020B	CD4024B	CD4040B
Braze Seal DIP	H4W	H4Q	H4X
Frit Seal DIP	H1F	H1B	H1F
Ceramic Flatpack	H6W	H3W	H6W

Pinouts

CD4020BMS
TOP VIEW

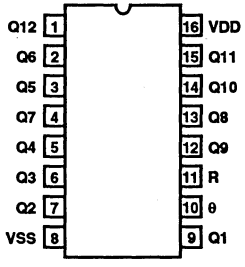


CD4024BMS
TOP VIEW



NC = NO CONNECTION

CD4040BMS
TOP VIEW



7 LOGIC

File Number 3300

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay 0 To Q1	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	360	ns
			10, 11	+125°C, -55°C	-	486	ns
Propagation Delay Qn To Qn + 1	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	330	ns
			10, 11	+125°C, -55°C	-	446	ns
Propagation Delay Reset To Q	TPLH3 TPHL3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	280	ns
			10, 11	+125°C, -55°C	-	378	ns
Transition Time Q1	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	3.5	-	MHz
			10, 11	+125°C, -55°C	2.22	-	MHz

NOTES:

1. VDD = 5V, CL = 50pF, RL = 200K
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Input To Q1	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Propagation Delay QN To QN + 1	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Propagation Delay Reset To Q	TPHL3	VDD = 10V	1, 2, 3	+25°C	-	120	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Transition Time	TTHL TTLH	VDD = 10V	2, 3	+25°C	-	100	ns
		VDD = 15V	2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	8	-	MHz
		VDD = 15V	1, 2, 3	+25°C	12	-	MHz
Minimum Reset Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Reset Removal Time	TREM	VDD = 5V	1, 2, 3	+25°C	-	350	ns
		VDD = 10V	1, 2, 3	+25°C	-	150	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Minimum Input Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	140	ns
		VDD = 10V	1, 2, 3	+25°C	-	60	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTND	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTPD	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
PART NUMBER CD4020BMS						
Static Burn-In 1 Note 1	1 - 7, 9, 12 - 15	8, 10, 11	16			
Static Burn-In 2 Note 1	1 - 7, 9, 12 - 15	8	10, 11, 16			
Dynamic Burn-In Note 1	-	8, 11	16	1 - 7, 9, 12 - 15	10	
Irradiation Note 2	1 - 7, 9, 12 - 15	8	10, 11, 16			

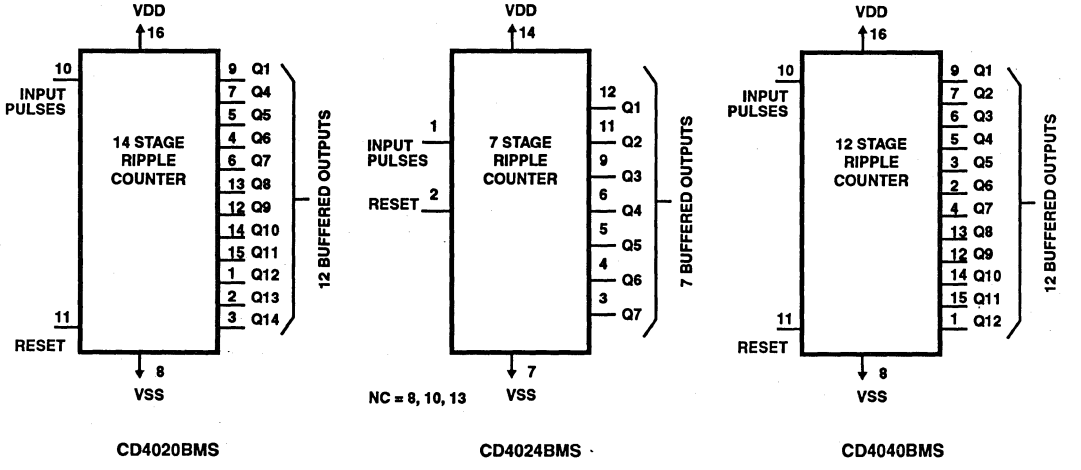
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS (Continued)

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
PART NUMBER CD4024BMS						
Static Burn-In 1 Note 1	3 - 6, 8 - 13	1, 2, 7	14			
Static Burn-In 2 Note 1	3 - 6, 8 - 13	7	1, 2, 14			
Dynamic Burn-In Note 1	8, 10, 13	2, 7	14	3 - 6, 9, 11, 12	1	
Irradiation Note 2	3 - 6, 8 - 13	7	1, 2, 14			
PART NUMBER CD4040BMS						
Static Burn-In 1 Note 1	1 - 7, 9, 12 - 15	8, 10, 11	16			
Static Burn-In 2 Note 1	1 - 7, 9, 12 - 15	8	10, 11, 16			
Dynamic Burn-In Note 1	-	8, 11	16	1 - 7, 9, 12 - 15	10	
Irradiation Note 2	1 - 7, 9, 12 - 15	8	10, 11, 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Functional Diagrams



Logic Diagrams

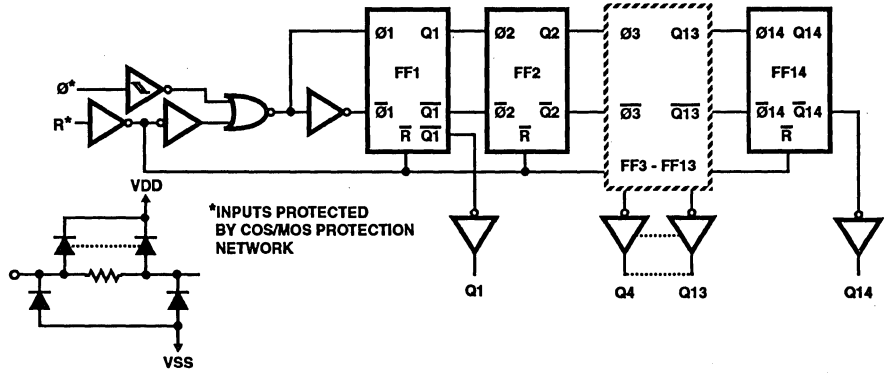


FIGURE 1. LOGIC DIAGRAM FOR CD4020BMS

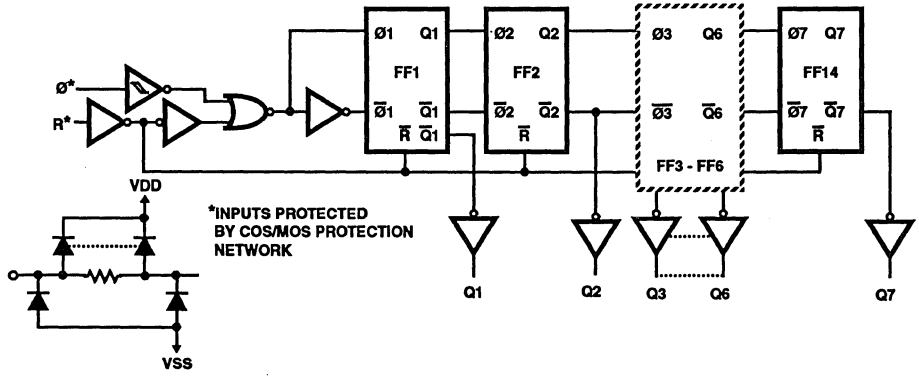


FIGURE 2. LOGIC DIAGRAM FOR CD4024BMS

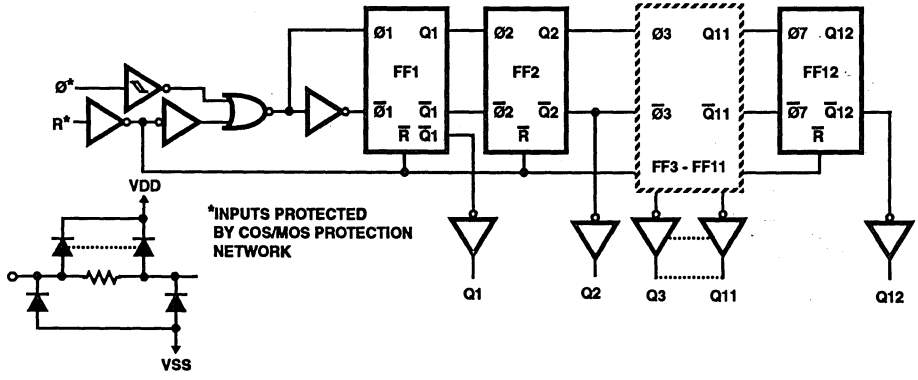


FIGURE 3. LOGIC DIAGRAM FOR CD4040BMS

Typical Performance Characteristics

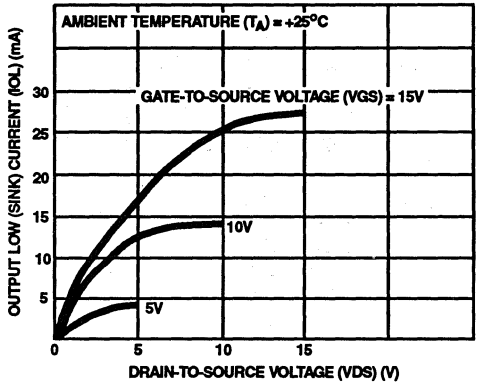


FIGURE 4. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

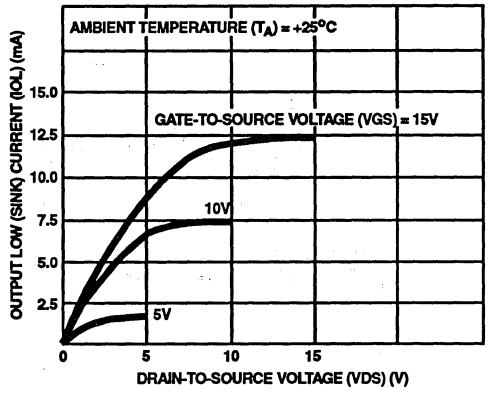


FIGURE 5. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

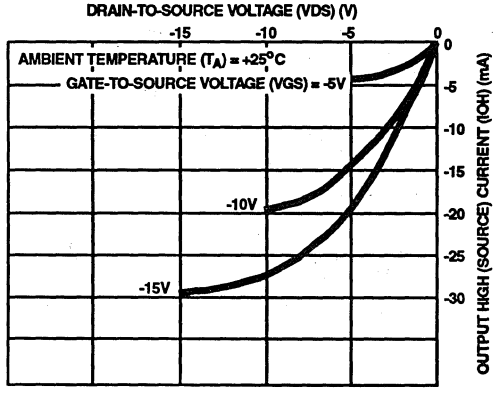


FIGURE 6. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

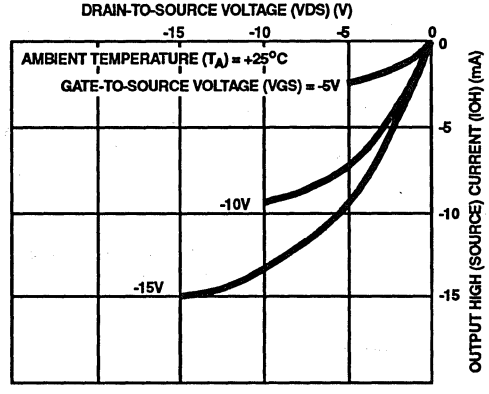


FIGURE 7. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

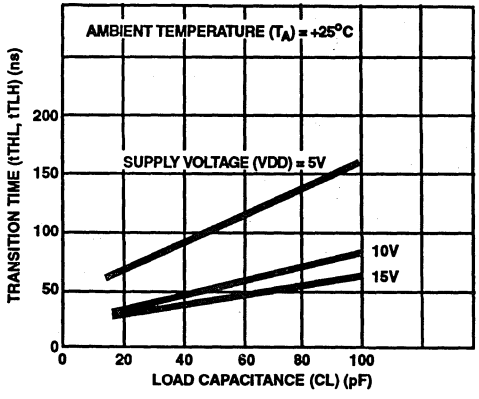


FIGURE 8. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

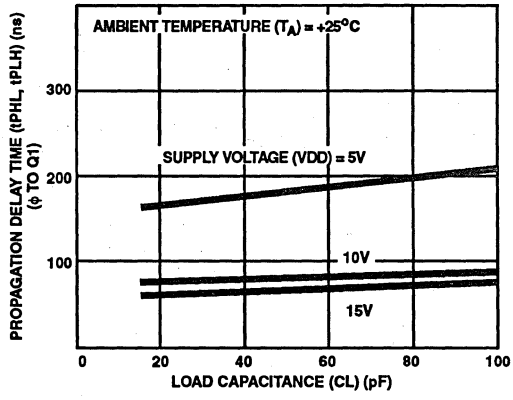


FIGURE 9. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (ϕ TO Q1))

Typical Performance Characteristics (Continued)

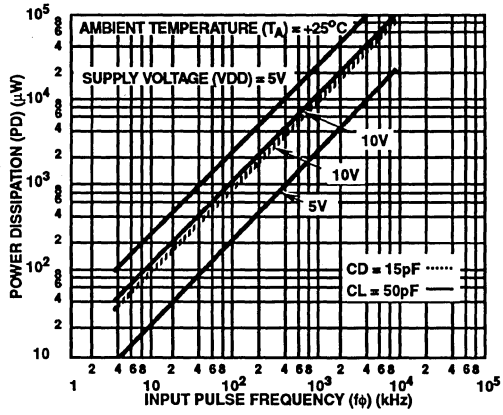


FIGURE 10. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT PULSE FREQUENCY FOR CD4020BMS

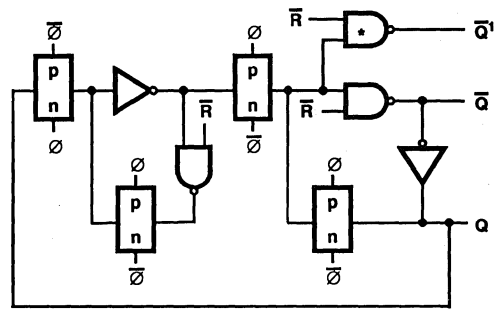
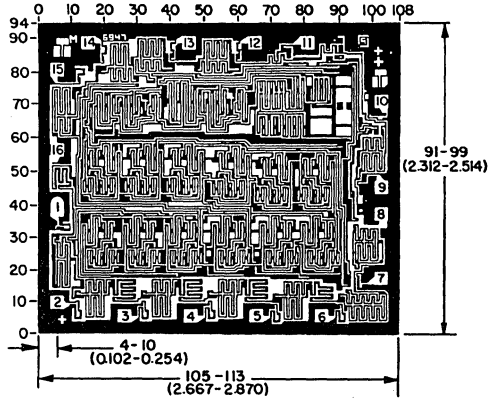
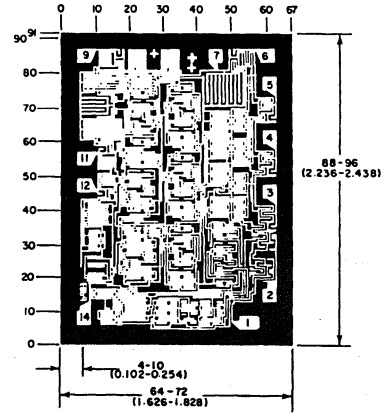


FIGURE 11. DETAIL OF TYPICAL FLIP-FLOP STAGES

Chip Dimensions and Pad Layouts





Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

DIMENSIONS AND PAD LAYOUT FOR CD4020BMS. DIMENSIONS AND PAD LAYOUT FOR CD4040BMS ARE IDENTICAL

DIMENSIONS AND PAD LAYOUT FOR CD4024BMSH

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4027BMS

CMOS Dual J-K Master-Slave Flip-Flop

December 1992

Features

- High Voltage Type (20V Rating)
- Set - Reset Capability
- Static Flip-Flop Operation - Retains State Indefinitely with Clock Level Either "High" or "Low"
- Medium Speed Operation - 16MHz (typ.) Clock Toggle Rate at 10V
- Standardized Symmetrical Output Characteristics
- 100% Tested For Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package-Temperature Range;
  - 100nA at 18V and +25°C
- Noise Margin (Over Full Package Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Registers, Counters, Control Circuits

Description

CD4027BMS is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K master-slave flip-flops. Each flip-flop has provisions for individual J, K, Set Reset, and Clock input signals. Buffered Q and $\overline{Q}$ signals are provided as outputs. This input-output arrangement provides for compatible operation with the Harris CD4013B dual D type flip-flop.

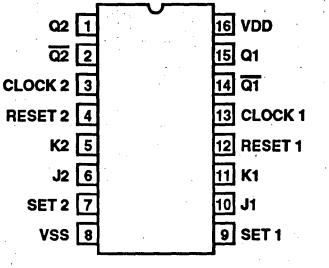
The CD4027BMS is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.

The CD4027BMS is supplied in these 16-lead outline packages:

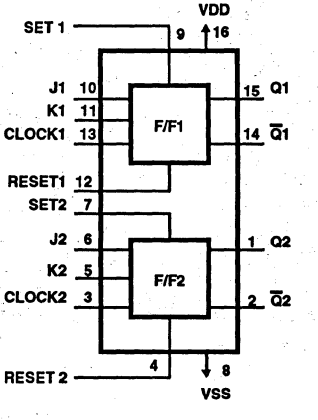
Braze Seal DIP	H4T
Frit Seal DIP	H1E
Ceramic Flatpack	H6W

Pinout

CD4027BMS
TOP VIEW



Functional Diagram



File Number 3302

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock To Q, $\overline{Q}$	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	300	ns
			10, 11	+125°C, -55°C	-	405	ns
Propagation Delay Set To Q Reset To $\overline{Q}$	TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	300	ns
			10, 11	+125°C, -55°C	-	405	ns
Propagation Delay Set To $\overline{Q}$, Reset To Q	TPHL3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Transition Time	TTLH TTHL	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	3.5	-	MHz
			10, 11	+125°C, -55°C	3.5/1.35	-	MHz

NOTES:

1. VDD = 5V, CL = 50pF, RL = 200K
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Clock To Q, $\overline{Q}$	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	130	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns
Propagation Delay Set To Q, Reset To $\overline{Q}$	TPLH2	VDD = 10V	1, 2, 3	+25°C	-	130	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns
Propagation Delay Set To $\overline{Q}$, Reset To Q	TPHL3	VDD = 10V	1, 2, 3	+25°C	-	170	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency Toggle Mode Input TR, TF = 5ns	FCL	VDD = 10V	1, 2, 3	+25°C	8	-	MHz
		VDD = 15V	1, 2, 3	+25°C	12	-	MHz
Minimum Data Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	75	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Set or Reset Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	180	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	140	ns
		VDD = 10V	1, 2, 3	+25°C	-	60	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Clock Input Rise Or Fall Time (Note 5)	TRCL TFCL	VDD = 5V	1, 2, 3, 4	+25°C	-	45	µs
		VDD = 10V	1, 2, 3, 4	+25°C	-	5	µs
		VDD = 15V	1, 2, 3, 4	+25°C	-	2	µs
Input Capacitance	CIN		1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. If more than one unit is cascaded in a parallel clocked operation, trCL should be made less than or equal to the sum of the fixed propagation delay time at 15pF and the transition time of the output driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

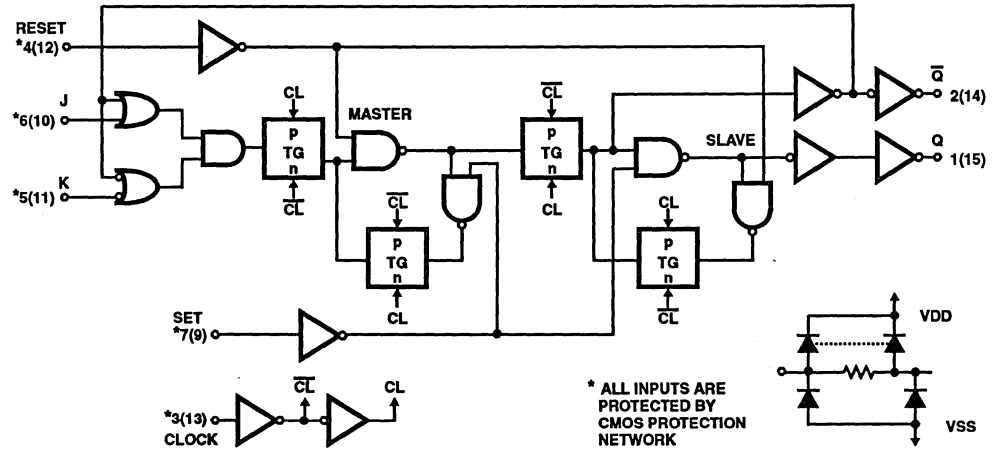
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	1, 2, 14, 15	3 - 13	16			
Static Burn-In 2 Note 1	1, 2, 14, 15	8	3 - 7, 9 - 13, 16			
Dynamic Burn-In Note 2	-	4, 7 - 9, 12	5, 6, 10, 11, 16	12, 14, 15	3, 13	
Irradiation Note 3	1, 2, 14, 15	8	3 - 7, 9 - 13, 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 4.75K ± 5%, VDD = 18V ± 0.5V
3. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram



LOGIC DIAGRAM AND TRUTH TABLE FOR CD4027BMS (ONE OF TWO IDENTICAL J-K FLIP-FLOPS)

TRUTH TABLE

PRESENT STATE						NEXT STATE		
INPUTS				OUTPUT		OUTPUTS		
J	K	S	R	Q	CL*	Q	$\overline{Q}$	
1	X	0	0	0	↑	1	0	
X	0	0	0	1	↑	1	0	
0	X	0	0	0	↑	0	1	
X	1	0	0	1	↑	0	1	
X	X	0	0	X	↓			No Change
X	X	1	0	X	X	1	0	
X	X	0	1	X	X	0	1	
X	X	1	1	X	X	1	1	

Logic 1 = High Level
Logic 0 = Low Level

* = Level change
X = Don't care

Typical Performance Characteristics

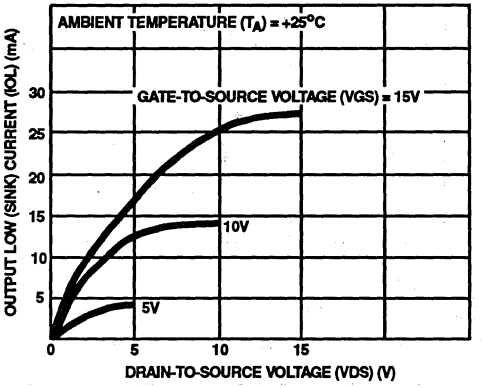


FIGURE 1. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

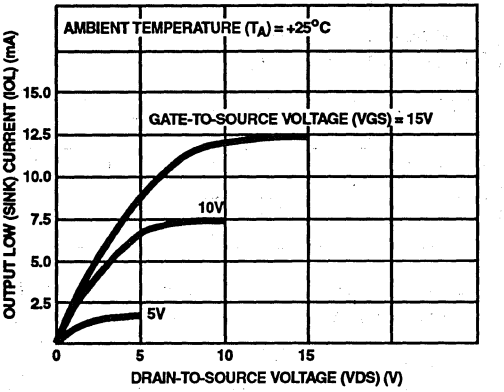


FIGURE 2. MINIMUM N OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

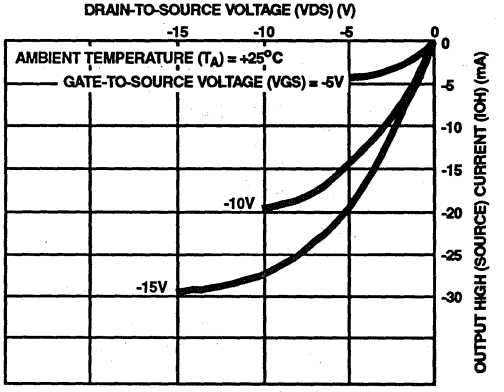


FIGURE 3. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

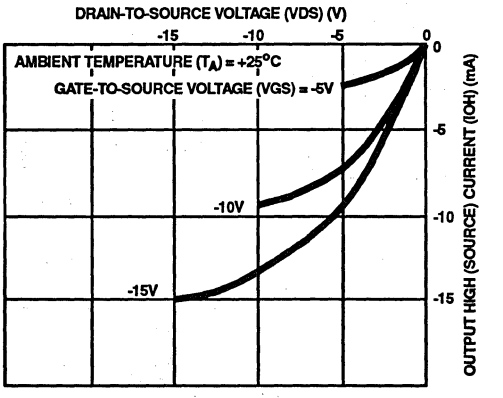


FIGURE 4. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

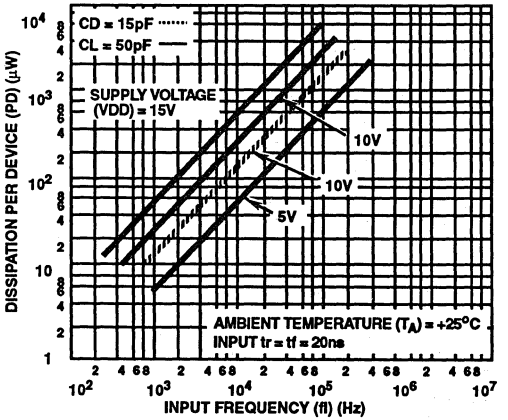


FIGURE 5. TYPICAL POWER DISSIPATION vs FREQUENCY

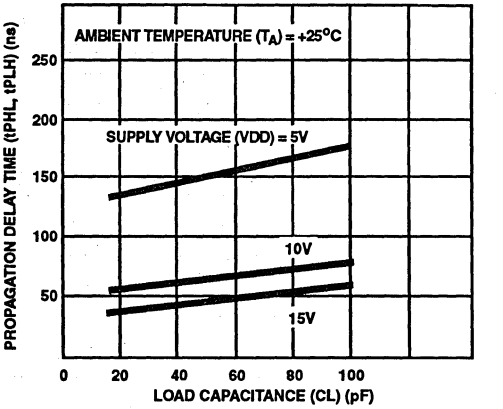


FIGURE 6. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE (CLOCK OR SET TO Q, CLOCK OR RESET TO $\overline{Q}$)

Typical Performance Characteristics (Continued)

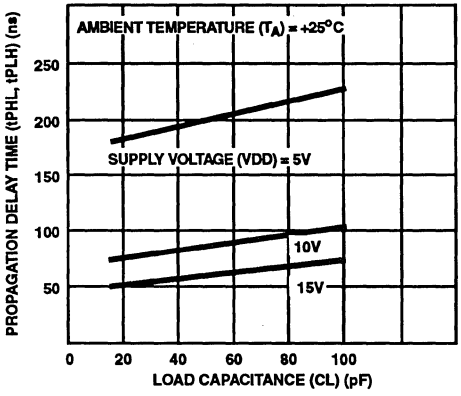


FIGURE 7. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE (SET TO $\overline{Q}$, OR RESET TO Q)

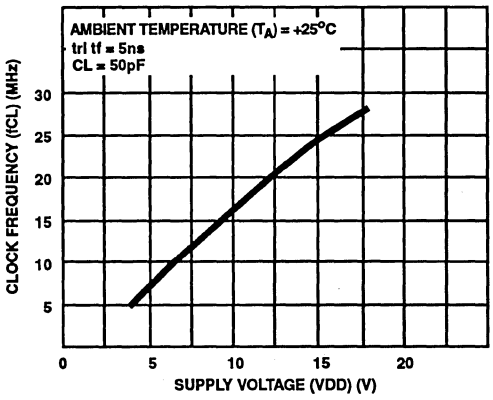
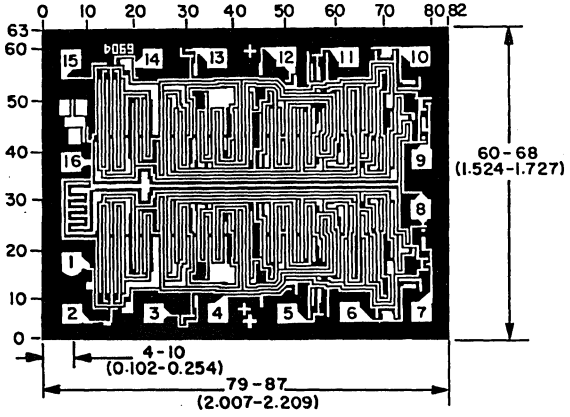


FIGURE 8. TYPICAL MAXIMUM CLOCK FREQUENCY vs SUPPLY VOLTAGE (TOGGLE MODE)

Chip Dimensions and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4028BMS

December 1992

CMOS BCD-To-Decimal Decoder

Features

- High Voltage Type (20V Rating)
- BCD-to-Decimal Decoding or Binary-to-Octal Decoding
- High Decoded Output Drive Capability
- "Positive Logic" Inputs and Outputs - Decoded Outputs Go High On Selection
- Medium-Speed Operation
  - tPHL, tPLH = 80ns (typ) at VDD = 10V
- Standardized Symmetrical Output Characteristics
- 100% Tested For Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package-Temperature Range;
  - 100nA at 18V and +25°C
- Noise Margin (Over Full Package Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Code Conversion
- Indication-Tube Decoder
- Address Decoding - Memory Selection Control

Description

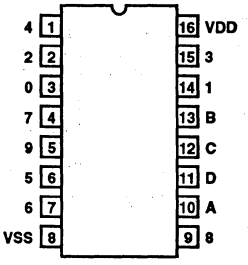
CD4028BMS types are BCD-to-decimal or binary-to-octal decoders consisting of buffering on all 4 inputs, decoding logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a high level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7 if D = "0". High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications.

The CD4028BMS is supplied in these 16-lead outline packages:

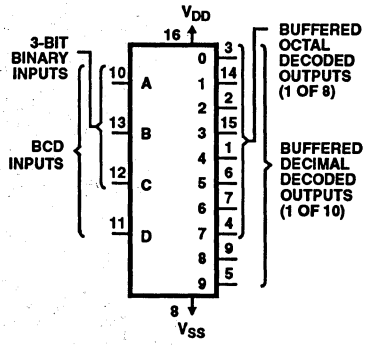
Braze Seal DIP	H4S
Frit Seal DIP	H1E
Ceramic Flatpack	H3X

Pinout

CD4028BMS
TOP VIEW



Functional Diagram



File Number 3303

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	350	ns
			10, 11	+125°C, -55°C	-	473	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN		1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	1 - 7, 9, 14, 15	8, 10 - 13	16			
Static Burn-In 2 Note 1	1 - 7, 9, 14, 15	8	10 - 13, 16			
Dynamic Burn-In Note 1	-	8	16	1 - 7, 9, 14, 15	10, 12, 13	11
Irradiation Note 2	1 - 7, 9, 14, 15	8	10 - 13, 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram

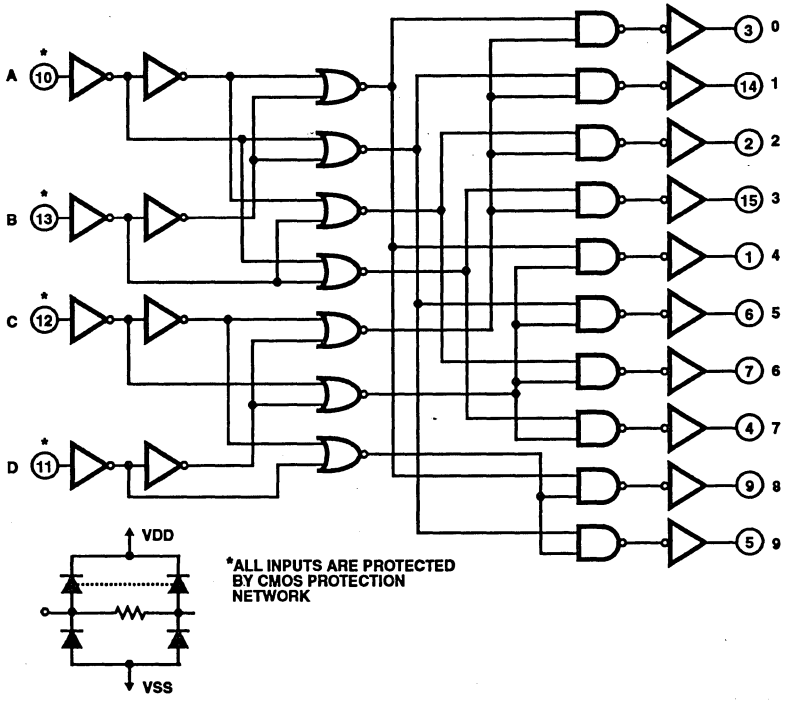


TABLE 1. TRUTH TABLE

D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

1 = HIGH LEVEL 0 = LOW LEVEL

Typical Performance Characteristics

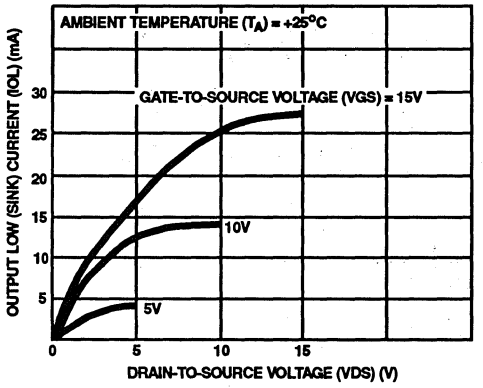


FIGURE 1. TYPICAL OUTPUT LOW (SINK) CURRENT CAPACITANCE

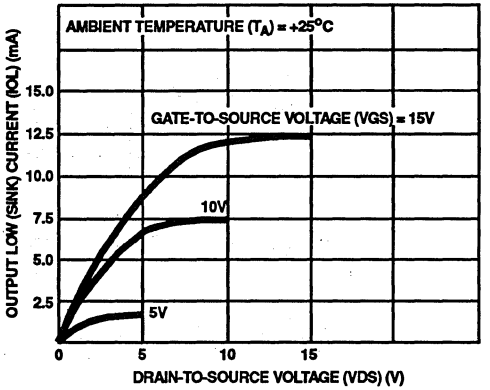


FIGURE 2. MINIMUM OUTPUT LOW (SINK) CURRENT CAPACITANCE

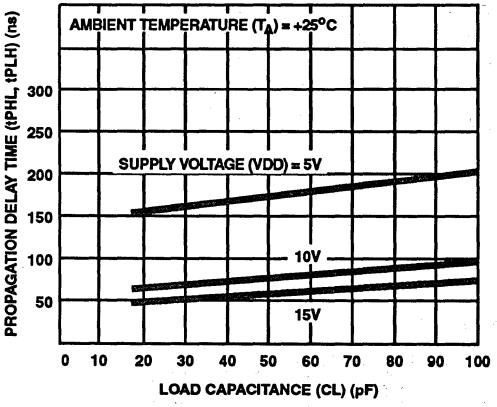


FIGURE 3. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

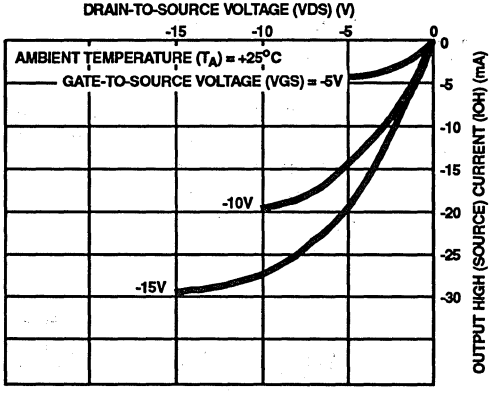


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

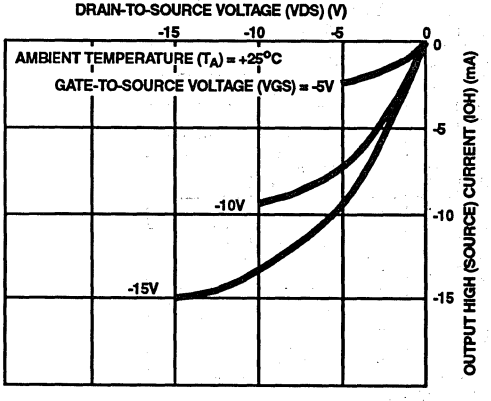


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

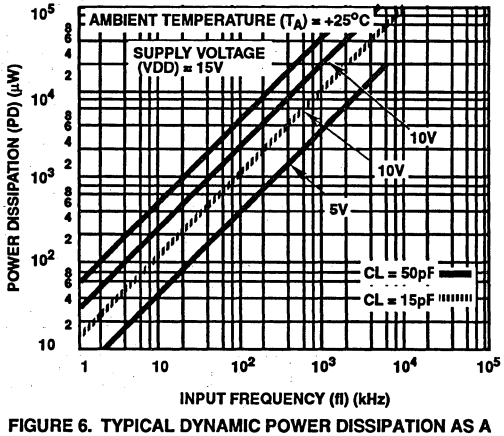


FIGURE 6. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

Typical Performance Characteristics (Continued)

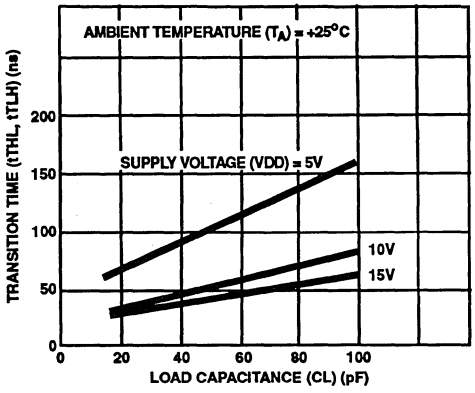


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Applications

The circuit shown in Figure 8 converts any 4-bit code to a decimal or hexadecimal code. Table 2 shows a number of codes and the decimal or hexadecimal number in these codes which must be applied to the input terminals of the CD4028BMS to select a particular output. For example: in order to get a high on output number 8 the input must be either an 8 expressed in 4-bit Binary code, a 15 expressed in 4-Bit Gray code, or a 5 expressed in Excess-3 code.

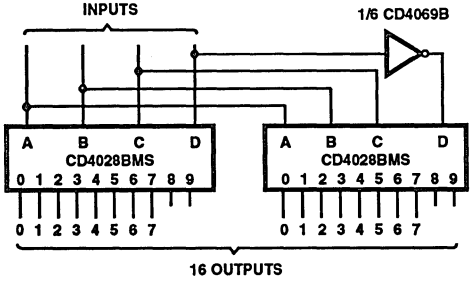


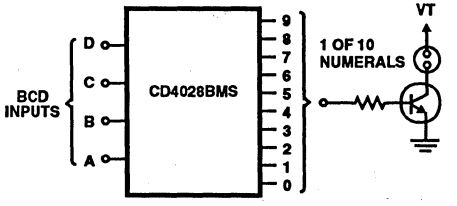
FIGURE 8. CODE CONVERSION CIRCUIT

TABLE 2. CODE CONVERSION CHART

INPUTS				INPUT CODES						OUTPUT NUMBER																
				HEXA-DECIMAL		DECIMAL																				
D	C	B	A	4-BIT BINARY	4-BIT GRAY	EXCESS-3	EXCESS-3 GRAY	AIKEN	4-2-2-1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0			0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1			1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	2	3		0	2	2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	3	2	0	3	3		0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	4	7	1	4	4		0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	5	6	2			3	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	6	4	3	1		4	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	1	1	7	5	4	2			0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	0	8	15	5				0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	9	14	6			5	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	10	12	7	9		6	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

TABLE 2. CODE CONVERSION CHART (Continued)

INPUTS				INPUT CODES						OUTPUT NUMBER															
				HEXA-DECIMAL		DECIMAL																			
D	C	B	A	4-BIT BINARY	4-BIT GRAY	EXCESS-3	EXCESS-3 GRAY	AIKEN	4-2-2-1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	0	1	1	11	13	8		5		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	12	8	9	5	6		0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	13	9		6	7	7	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	0	14	11		8	8	8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	15	10		7	9	9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1



*(TRADEMARK) BURROUGHS CORP.

TUBE REQUIREMENTS

TYPE		VT(Vdc)	NUMERAL mA/
BURROUGHS	B4081	170	14
	B4336/ 718	170	2
	B4032	170	14
	B4021	120	14
TRANSISTOR CHARACTERISTICS			
Leakage with transistor cutoff ≤ 0.05mA			
V(BR)CEO ≥ 70V			

FIGURE 9. NEON READOUT (NIXIE TUBE*) DISPLAY APPLICATION

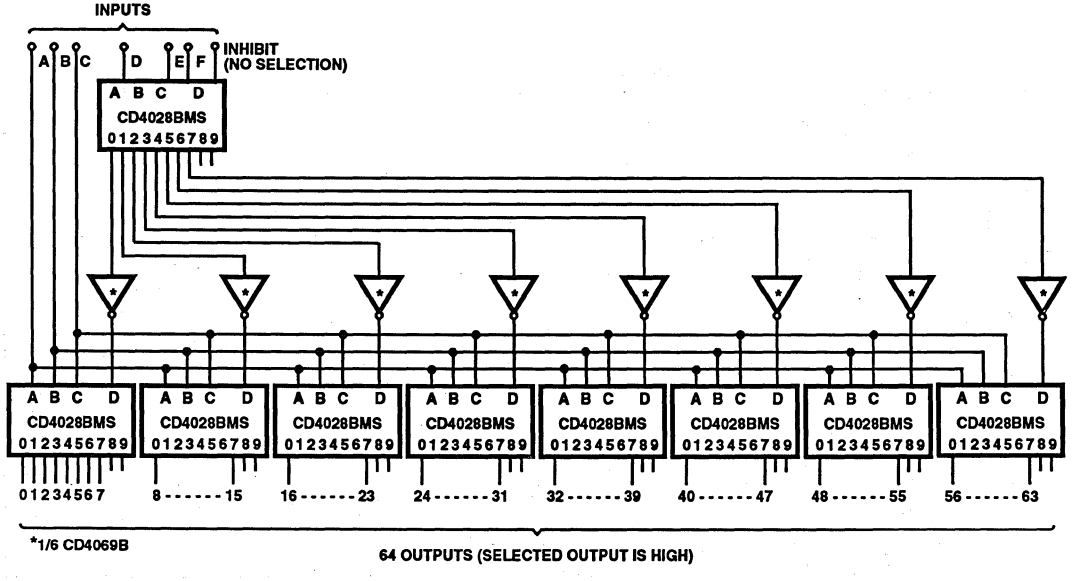
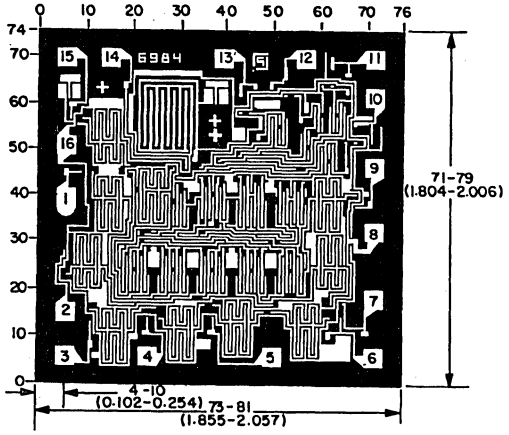


FIGURE 10. 6-BIT BINARY TO 1-OF-64 ADDRESS DECODER

Chip Dimensions and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4029BMS

CMOS Presettable Up/Down Counter

December 1992

Features

- High-Voltage Type (20V Rating)
- Medium Speed Operation: 8MHz (Typ.) at CL = 50pF and VDD - VSS = 10V
- Multi-Package Parallel Clocking for Synchronous High Speed Output Response or Ripple Clocking for Slow Clock Input Rise and Fall Times
- "Preset Enable" and Individual "Jam" Inputs Provided
- Binary or Decade Up/Down Counting
- BCD Outputs in Decade Mode
- 100% Tested for Maximum Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Standardized Symmetrical Output Characteristics
- Maximum Input Current of 1μA at 18V Over Full Package-Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standards No. 13B, "Standard Specifications for Description of "B" Series CMOS Device's

Applications

- Programmable Binary and Decade Counting/Frequency Synthesizers-BCD Output
- Analog to Digital and Digital to Analog Conversion
- Up/Down Binary Counting
- Difference Counting
- Magnitude and Sign Generation
- Up/Down Decade Counting

Description

CD4029BMS consists of a four-stage binary or BCD-decade up/down counter with provisions for look-ahead carry in both counting modes. The inputs consist of a single CLOCK, $\overline{\text{CARRY-IN}}$ ($\overline{\text{CLOCK ENABLE}}$), BINARY/DECADE, UP/DOWN, PRESET ENABLE, and four individual JAM signals. Q1, Q2, Q3, Q4 and a $\overline{\text{CARRY OUT}}$ signal are provided as outputs.

A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock. A low on each JAM line, when the PRESET-ENABLE signal is high, resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the $\overline{\text{CARRY-IN}}$ and PRE-SET ENABLE signals are low. Advancement is inhibited when the $\overline{\text{CARRY-IN}}$ or PRESET ENABLE signals are high. The $\overline{\text{CARRY-OUT}}$ signal is normally high and goes low when the counter reaches its maximum count in the UP mode or the minimum count in the DOWN mode provided the $\overline{\text{CARRY-IN}}$ signal is low. The $\overline{\text{CARRY-IN}}$ signal in the low state can thus be considered a $\overline{\text{CLOCK ENABLE}}$. The $\overline{\text{CARRY-IN}}$ terminal must be connected to VSS when not in use.

Binary counting is accomplished when the BINARY/DECADE input is high; the counter counts in the decade mode when the BINARY/DECADE input is low. The counter counts up when the UP/DOWN input is high, and down when the UP/DOWN input is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement as shown in Figure 17.

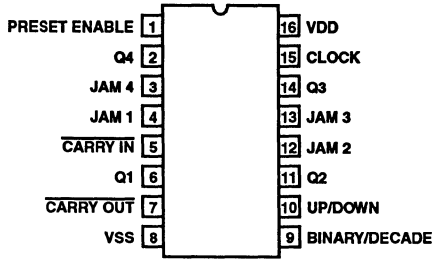
Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

The CD4029BMS is supplied in these 16-lead outline packages:

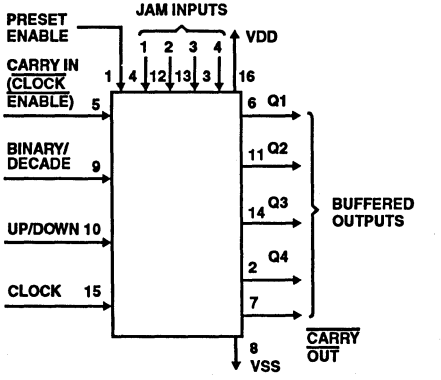
Braze Seal DIP	H4X
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

Pinout

CD4029BMS
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3304

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K)..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock To Q Output	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Propagation Delay Clock To Carry Out	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	560	ns
			10, 11	+125°C, -55°C	-	756	ns
Propagation Delay Preset Enable To Q	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	470	ns
			10, 11	+125°C, -55°C	-	635	ns
Propagation Delay Preset Enable To Carry-Out	TPHL4 TPLH4	VDD = 5V, VIN = VDD or GND	9	+25°C	-	640	ns
			10, 11	+125°C, -55°C	-	864	ns
Propagation Delay Carry-In To Carry-Out	TPHL5 TPLH5	VDD = 5V, VIN = VDD or GND	9	+25°C	-	340	ns
			10, 11	+125°C, -55°C	-	459	ns
Transition Time Q Output	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	2	-	MHz
			10, 11	+125°C, -55°C	1.48	-	MHz

NOTES:

1. VDD = 5V, CL = 50pF, RL = 200K
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-2.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Q Output	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	240	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns
Propagation Delay Carry Output	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	260	ns
		VDD = 15V	1, 2, 3	+25°C	-	190	ns
Propagation Delay Preset Enable To Q	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	160	ns
Propagation Delay Preset Enable To Carry-Out	TPHL4 TPLH4	VDD = 10V	1, 2, 3	+25°C	-	290	ns
		VDD = 15V	1, 2, 3	+25°C	-	210	ns
Propagation Delay Carry In To Carry Out	TPHL5 TPLH5	VDD = 10V	1, 2, 3	+25°C	-	140	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	4	-	MHz
		VDD = 15V	1, 2, 3	+25°C	5.5	-	MHz
Minimum Data Setup Time Note 4	TS	VDD = 5V	1, 2, 3	+25°C	-	340	ns
		VDD = 10V	1, 2, 3	+25°C	-	140	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Clock Rise And Fall Time Note 5	TRCL TFCL	VDD = 5V	1, 2, 3	+25°C	-	15	µs
		VDD = 10V	1, 2, 3	+25°C	-	15	µs
		VDD = 15V	1, 2, 3	+25°C	-	15	µs
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	180	ns
		VDD = 10V	1, 2, 3	+25°C	-	90	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Minimum Carry In Setup Time Note 6	TS	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	70	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Minimum Carry Input Hold Time Note 6	TH	VDD = 5V	1, 2, 3	+25°C	-	50	ns
		VDD = 10V	1, 2, 3	+25°C	-	30	ns
		VDD = 15V	1, 2, 3	+25°C	-	25	ns
Minimum Preset Enable Removal Time Note 4	TREM	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	110	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Minimum Preset Enable Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	130	ns
		VDD = 10V	1, 2, 3	+25°C	-	70	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. From Up/Down, Binary/Decode, Carry In, or Preset Enable Control Inputs to Clock Edge.
5. If more than one unit is cascaded in the parallel clocked application, tr CL should be made ≤ the sum of the fixed propagation delay at 15pF and the transition time of the carry output driving stage for the estimated capacitive load. This measurement was made with a decoupling capacitor (>1μF) between VDD and VSS.
6. From Carry In to Clock Edge.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	μA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10μA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0μA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

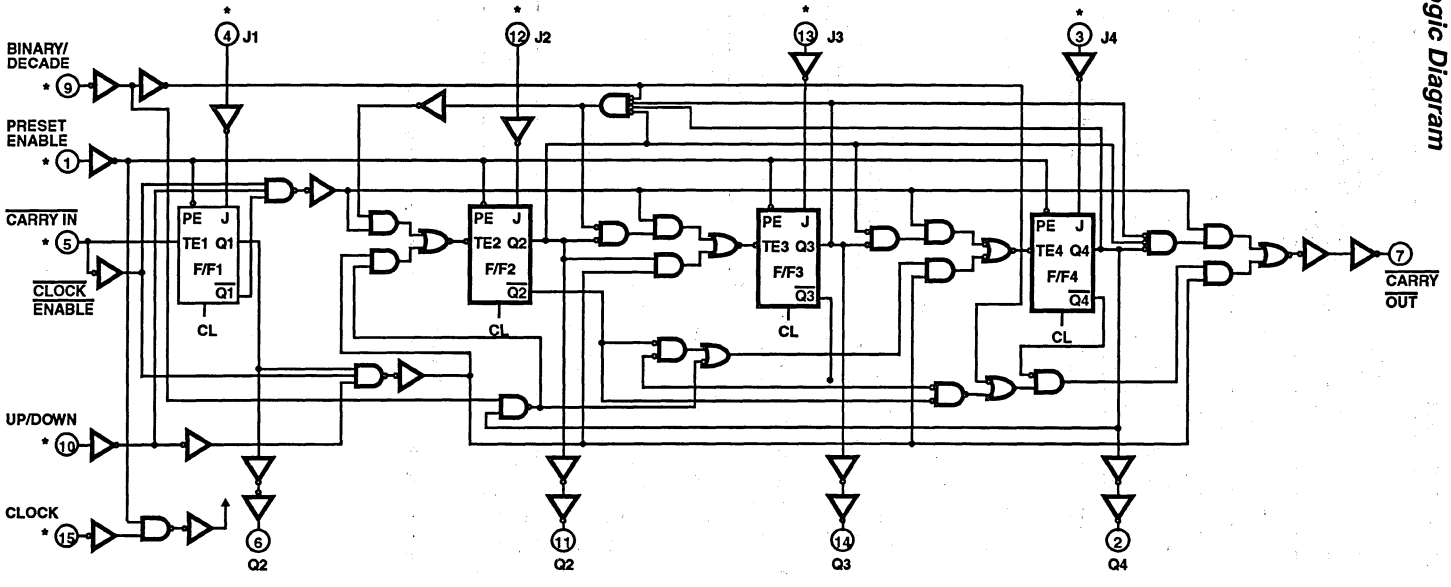
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

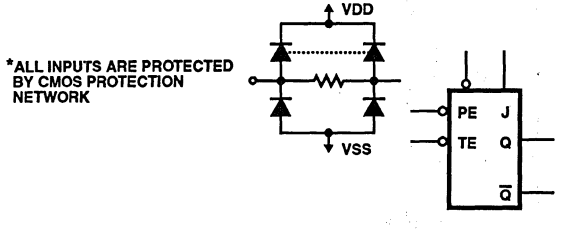
FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	2, 6, 7, 11, 14	1, 3 - 5, 8 - 10, 12, 13, 15	16			
Static Burn-In 2 Note 1	2, 6, 7, 11, 14	8	1, 3 - 5, 9, 10, 12, 13, 15, 16			
Dynamic Burn-In Note 1	-	1, 3 - 5, 8, 12, 13	9, 10, 16	2, 6, 7, 11, 14	15	-
Irradiation Note 2	2, 6, 7, 11, 14	8	1, 3 - 5, 9, 10, 12, 13, 15, 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram





TRUTH TABLE

CLOCK	TE	PE	J	Q	$\overline{Q}$	
X	X	0	0	0	1	
↘	0	1	X	$\overline{Q}$	Q	
X	X	0	1	1	0	
↘	1	1	X	Q	$\overline{Q}$	NC
↗	X	1	X	Q	Q	NC

X = Don't Care

FUNCTION TABLE

CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC (B/D)	1	Binary Count
	0	Decade Count
UP/DOWN (U/D)	1	Up Count
	0	Down Count
Preset Enable (PE)	1	Jam In
	0	No Jam
$\overline{\text{CARRY IN}}$ ($\overline{\text{CI}}$) ($\overline{\text{CLOCK ENABLE}}$)	1	No Counter Advance at POS Clock Transition
	0	Advance Counter at POS Clock Transition

FIGURE 1.

Typical Performance Characteristics

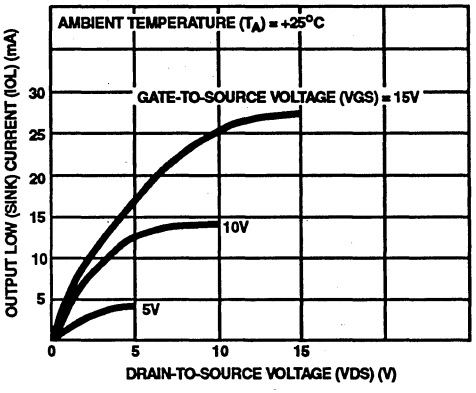


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

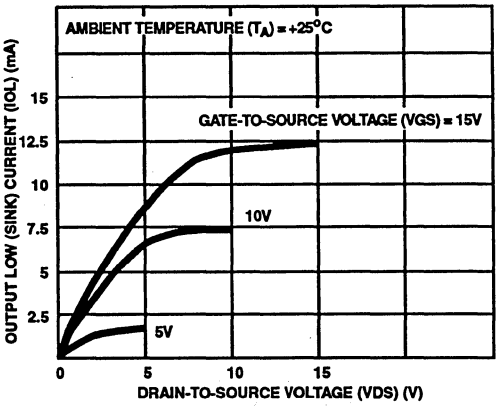


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

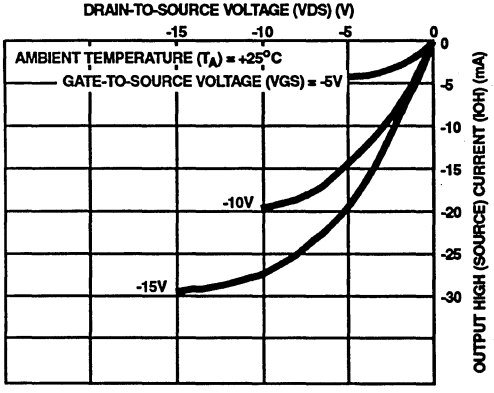


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

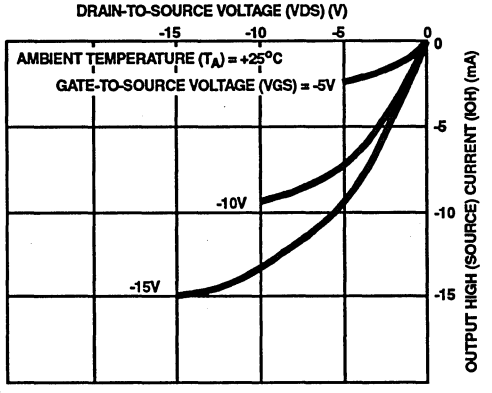


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

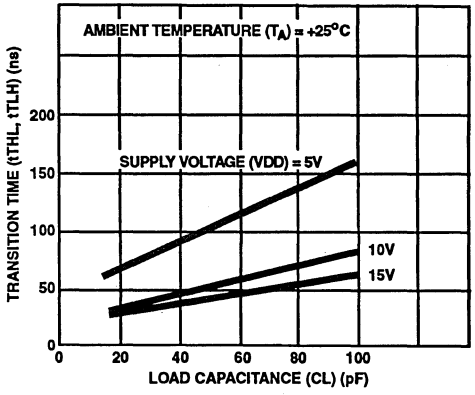


FIGURE 6. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

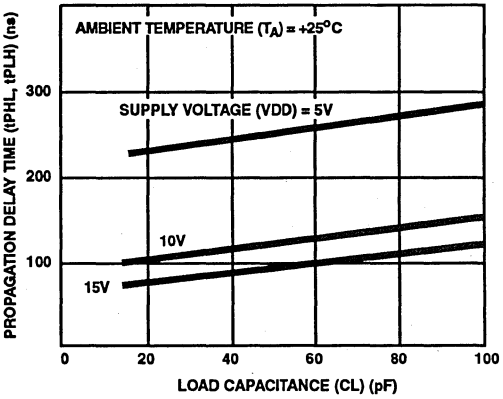


FIGURE 7. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (Q OUTPUT)

Typical Performance Characteristics (Continued)

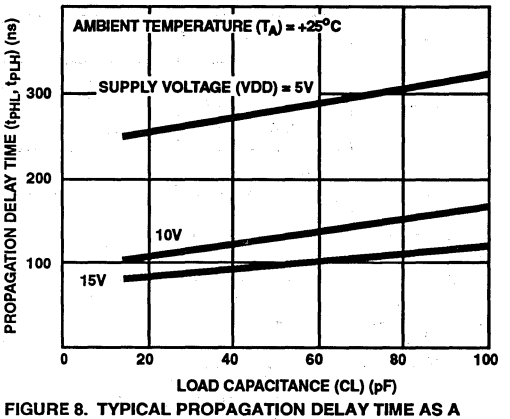


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (CARRY OUTPUT)

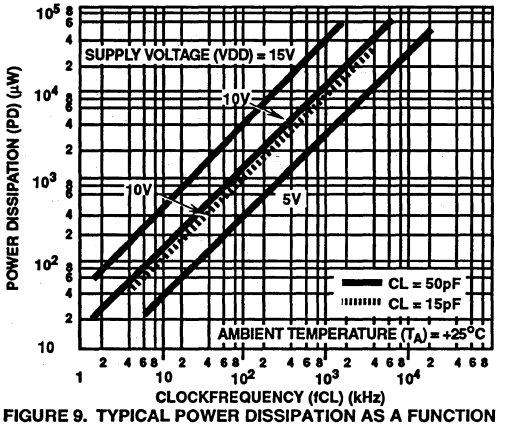
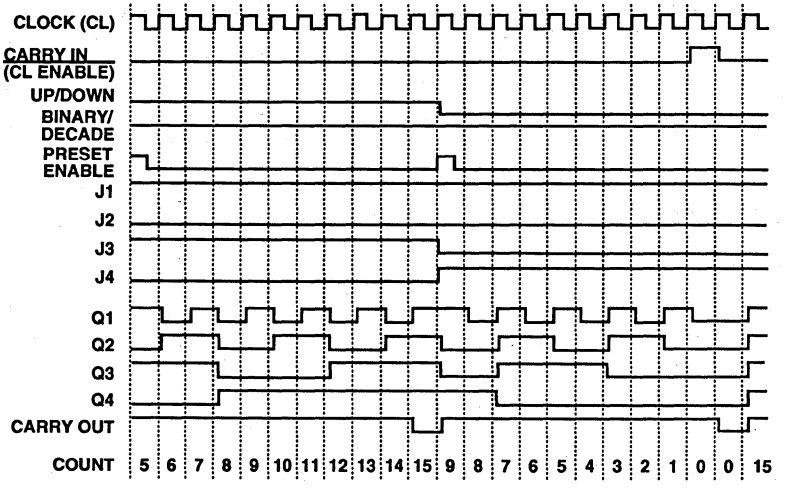


FIGURE 9. TYPICAL POWER DISSIPATION AS A FUNCTION OF FREQUENCY

Timing Diagrams



The CD4029BMS CLOCK and UP/DOWN inputs are used directly in most applications. In applications where CLOCK UP and CLOCK DOWN inputs are provided, conversion to the CD4029BMS CLOCK and UP/DOWN inputs can easily be realized by use of the circuit in Figure 11.

CD4029BMS changes count on positive transitions of CLOCK UP or CLOCK DOWN inputs. For the gate configuration in Figure 12, when counting up the CLOCK DOWN input must be maintained high and conversely when counting down the CLOCK UP input must be maintained high.

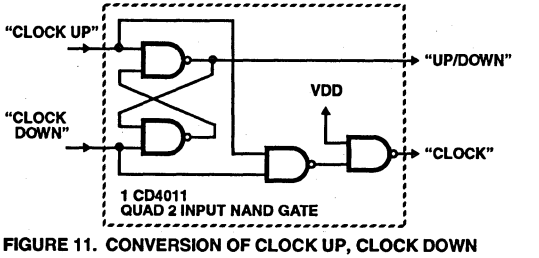


FIGURE 11. CONVERSION OF CLOCK UP, CLOCK DOWN INPUT SIGNALS TO CLOCK AND UP/DOWN INPUT SIGNALS

Timing Diagrams (Continued)

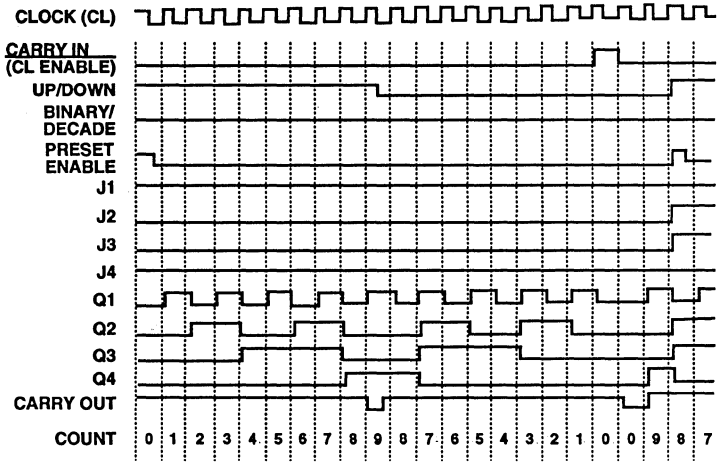
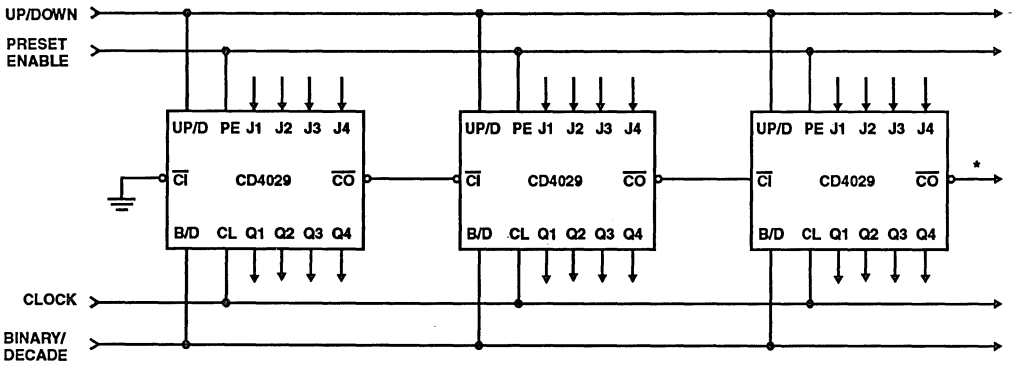


FIGURE 12. TIMING DIAGRAM-DECADE MODE

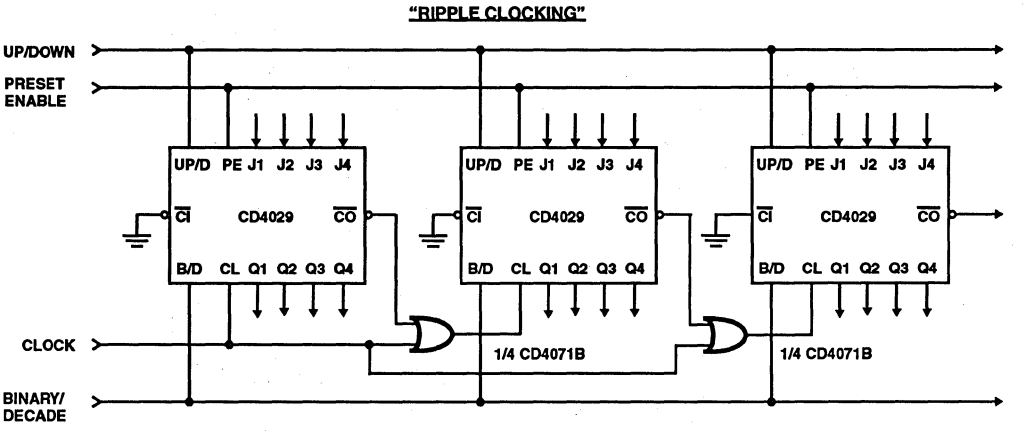
"PARALLEL CLOCKING"



*$\overline{\text{CARRY OUT}}$ LINES AT THE 2ND, 3RD, ETC, STAGES MAY HAVE A NEGATIVE-GOING GLITCH PULSE RESULTING FROM DIFFERENTIAL DELAYS OF DIFFERENT CD4029BMS IC'S. THESE NEGATIVE GOING GLITCHES DO NOT AFFECT PROPER CD4029BMS OPERATION. HOWEVER, IF THE $\overline{\text{CARRY OUT}}$ SIGNALS ARE USED TO TRIGGER OTHER EDGE-SENSITIVE LOGIC DEVICES, SUCH AS FF'S OR COUNTERS, THE $\overline{\text{CARRY OUT}}$ SIGNALS SHOULD BE GATED WITH THE CLOCK SIGNAL USING A 2-INPUT OR GATE SUCH AS CD4071BMS.

FIGURE 13. CASCADING COUNTER PACKAGES

Timing Diagrams (Continued)

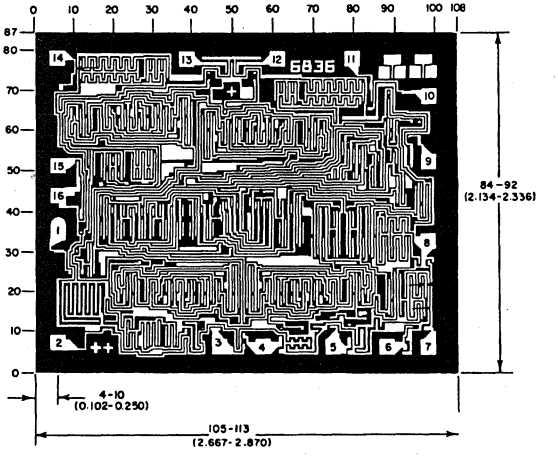


RIPPLE CLOCKING MODE:

THE UP/DOWN CONTROL CAN BE CHANGED AT ANY COUNT. THE ONLY RESTRICTION ON CHANGING THE UP/DOWN CONTROL IS THAT THE CLOCK INPUT TO THE FIRST COUNTING STAGE MUST BE HIGH. FOR CASCADING COUNTERS OPERATING IN A FIXED UP-COUNT OR DOWN-COUNT MODE, THE OR GATES ARE NOT REQUIRED BETWEEN STAGES, AND $\overline{CO}$ IS CONNECTED DIRECTLY TO THE CL INPUT OF THE NEXT STAGE WITH $\overline{CI}$ GROUNDED.

FIGURE 13. CASCADING COUNTER PACKAGES (Continued)

Chip Dimensions and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

CD4030BMS

CMOS Quad Exclusive-OR Gate

December 1992

Features

- High Voltage Type (20V Rating)
- Medium-Speed Operation
  - tPHL, tPLH = 65ns (typ) at VDD = 10V, CL = 50pF
- 100% Tested for Quiescent Current at 20V
- Standardized Symmetrical Output Characteristics
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current Of 1μA at 18V Over Full Package-Temperature Range;
  - 100nA at 18V and +25°C
- Noise Margin (Over Full Package Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Even and Odd-Parity Generators and Checkers
- Logical Comparators
- Adders/Subtractors
- General Logic Functions

Description

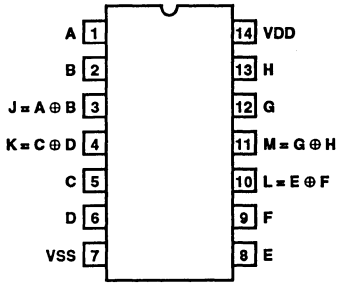
The CD4030BMS types consist of four independent Exclusive-OR gates. The CD4030BMS provides the system designer with a means for direct implementation of the Exclusive-OR function.

The CD4030BMS is supplied in these 14-lead outline packages:

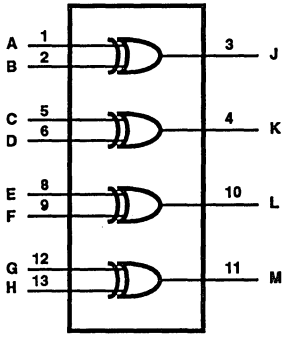
Braze Seal DIP	H4H
Frit Seal DIP	H1B
Ceramic Flatpack	H3W

Pinout

CD4030BMS
TOP VIEW



Functional Diagram



J = A ⊕ B
K = C ⊕ D
M = G ⊕ H
L = E ⊕ F
VSS = 7
VDD = 14

7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3305

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C//W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	280	ns
			10, 11	+125°C, -55°C	-	378	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	130	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Final Test	100% 5004	2, 3, 8A, 8B, 10, 11	
Group A	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

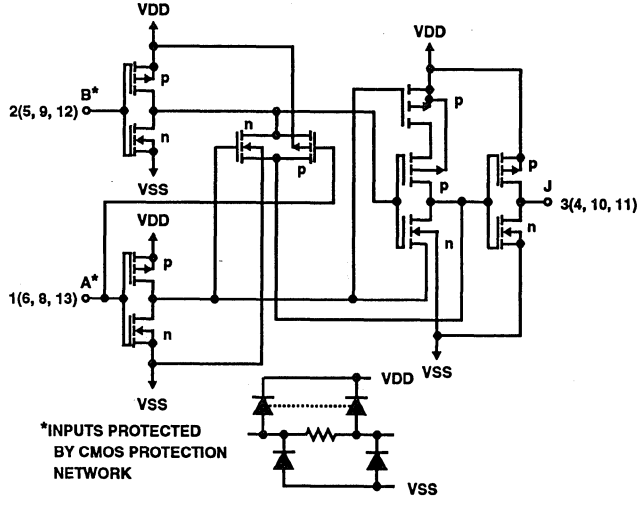
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	3, 4, 10, 11	1, 2, 5 - 9, 12, 13	14			
Static Burn-In 2 Note 1	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12 - 14			
Dynamic Burn-In Note 1	-	7	14	3, 4, 10, 11	2, 6, 9, 13	1, 5, 8, 12
Irradiation Note 2	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12 - 14			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Schematic Diagram



TRUTH TABLE FOR 1 OF 4 INDENTICAL GATES

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

1 = High Level
0 = Low Level

FIGURE 1. 1 OF 4 IDENTICAL GATES

Typical Performance Characteristics

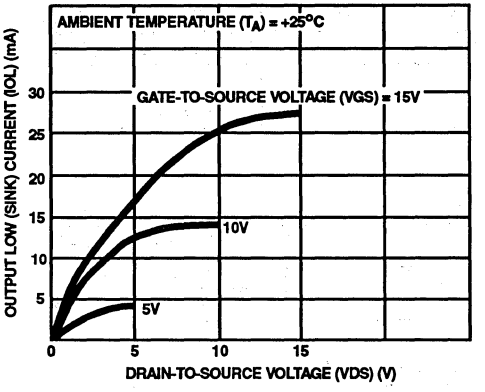


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

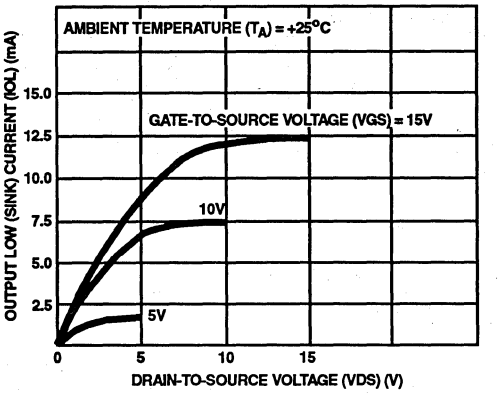


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

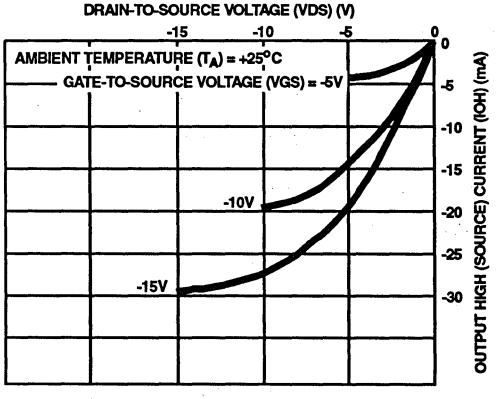


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

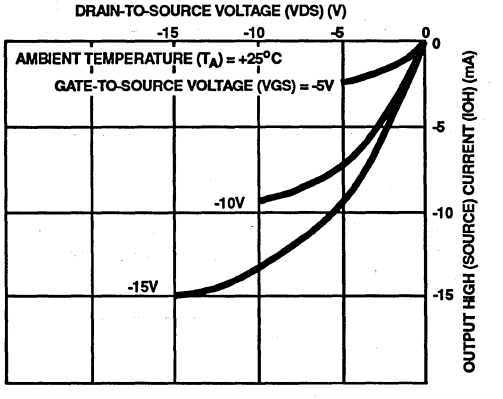


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

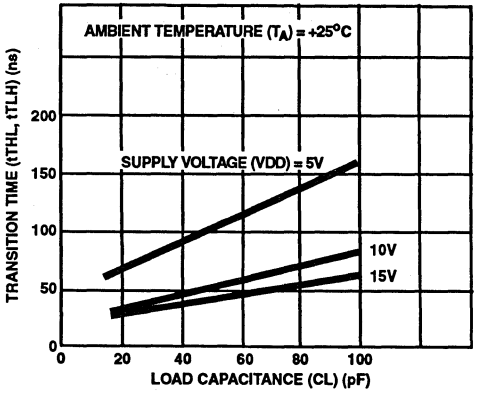


FIGURE 6. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

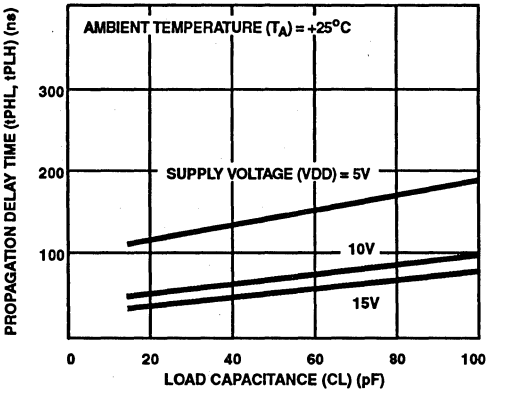


FIGURE 7. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

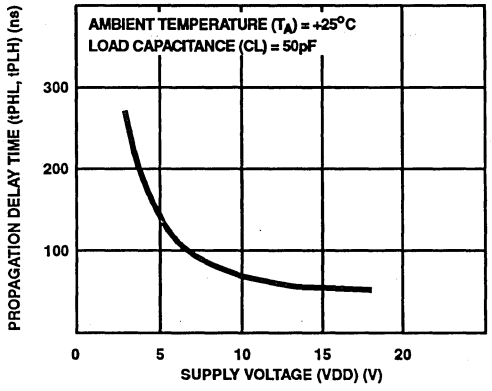


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF SUPPLY VOLTAGE

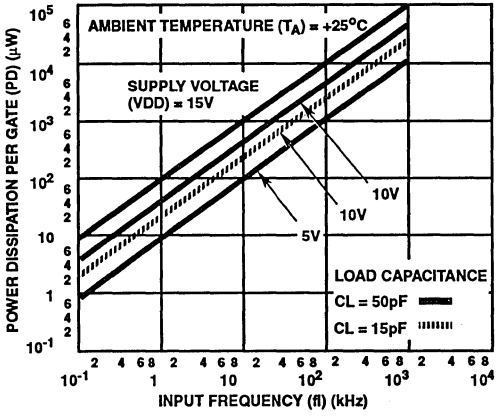
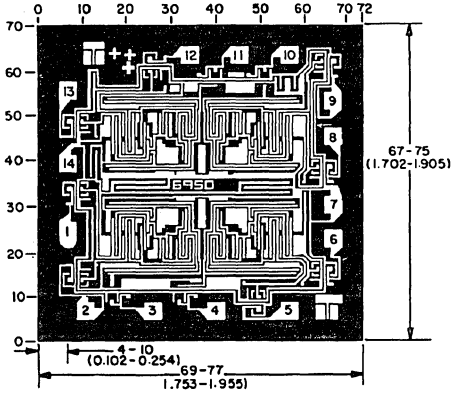


FIGURE 9. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

Chip Dimensions and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4031BMS

CMOS 64-Stage Static Shift Register

December 1992

Features

- High Voltage Type (20V Rating)
- Fully Static Operation: DC to 12MHz (typ.) at VDD - VSS = 15V
- Standard TTL Drive Capability on Q Output
- Recirculation Capability
- Three Cascading Modes:
  - Direct Clocking for High-Speed Operation
  - Delayed Clocking for Reduced Clock Drive Requirements
  - Additional 1/2 Stage for Slow Clocks
- 100% Tested For Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package-Temperature Range;
  - 100nA at 18V and +25°C
- Noise Margin (Over Full Package Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Serial Shift Registers
- Time Delay Circuits

Description

The CD4031BMS is a static shift register that contains 64 D-type, master-slave flip-flop stages and one stage which is a D-type master flip-flop only (referred to as a 1/2 stage).

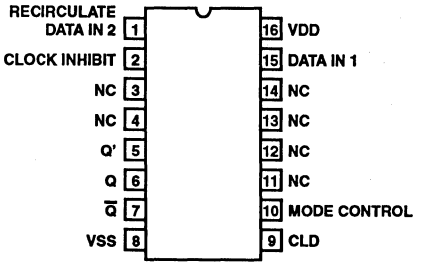
The logic level present at the DATA input is transferred into the first stage and shifted one stage at each positive-going clock transition. Maximum clock frequencies up to 12MHz (typical) can be obtained. Because fully static operation is allowed, information can be permanently stored with the clock line in either the low or high state. The CD4031BMS has a MODE CONTROL input that, when in the high state, allows operation in the recirculating mode. The MODE CONTROL input can also be used to select between two separate data sources. Register packages can be cascaded and the clock lines driven directly for high-speed operation. Alternatively, a delayed clock output (CLD) is provided that enables cascading register packages while allowing reduced clock drive fan-out and transition-time requirements. A third cascading option makes use of the Q' output from the 1/2 stage, which is available on the next negative-going transition of the clock after the Q output occurs. This delayed output, like the delayed clock CLD, is used with clocks having slow rise and fall times.

The CD4031BMS is supplied in these 16 lead outline packages:

Braze Seal DIP	H4X
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

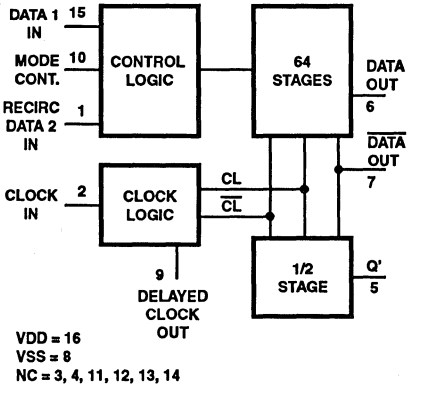
Pinout

CD4031BMS
TOP VIEW



NC = NO CONNECTION

Functional Diagram



File Number 3306

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current $\overline{Q}$, Q', CLD	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.51	-	mA
	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.3	-	mA
	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.4	-	mA
Output Current Q	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	2.04	-	mA
Output Current Q	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	5.2	-	mA
Output Current Q	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	13.6	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.51	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.6	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.3	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.4	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH> VDD/2	VOL< VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to $\overline{Q}$	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Propagation Delay Clock to Q	TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Propagation Delay Clock to Q	TPHL2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	380	ns
			10, 11	+125°C, -55°C	-	513	ns
Propagation Delay Clock to Q'	TPLH3 TPHL3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	380	ns
			10, 11	+125°C, -55°C.	-	513	ns
Propagation Delay Clock to CLD	TPHL4 TPLH4	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency (See Note 5; Table 3)	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	2	-	MHz
			10, 11	+125°C, -55°C	1.48	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink) $\overline{Q}$, Q', CLD Outputs	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink) $\overline{Q}$, Q', CLD Outputs	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink) $\overline{Q}$, Q', CLD Outputs	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Sink) Q Outputs	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	1.44	-	mA
				-55°C	2.56	-	mA
Output Current (Sink) Q Outputs	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	3.6	-	mA
				-55°C	6.4	-	mA
Output Current (Sink) Q Outputs	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	9.6	-	mA
				-55°C	16.8	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Clock to $\overline{Q}$	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	220	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns
Propagation Delay Clock to Q	TPLH2	VDD = 10V	1, 2, 3	+25°C	-	220	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns
Propagation Delay Clock to Q	TPHL2	VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Propagation Delay Clock to CLD	TPLH3 TPHL3	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Propagation Delay Clock to Q'	TPLH4 TPHL4	VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency (Note 5)	FCL	VDD = 10V	1, 2, 3	+25°C	-	5	MHz
		VDD = 15V	1, 2, 3	+25°C	-	6	MHz
Clock Input Rise or Fall Time (Note 4)	TRCL TFCL	VDD = 5V	1, 2, 3	+25°C	-	1000	µs
		VDD = 10V	1, 2, 3	+25°C	-	1000	µs
		VDD = 15V	1, 2, 3	+25°C	-	200	µs
Minimum Data Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	60	ns
		VDD = 10V	1, 2, 3	+25°C	-	30	ns
		VDD = 15V	1, 2, 3	+25°C	-	20	ns
Minimum Data Hold Time	TH	VDD = 5V	1, 2, 3	+25°C	-	60	ns
		VDD = 10V	1, 2, 3	+25°C	-	30	ns
		VDD = 15V	1, 2, 3	+25°C	-	20	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	240	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. If more than one unit is cascaded in the parallel clocked application, TRCL should be made ≤ the sum of the propagation delay at 50pF and the transition time of the output driving stage.
5. Maximum clock frequency for cascaded units;

   a) Using Delayed Clock feature in recirculation mode:

   $$FMAX = \frac{1}{(n\text{-}1)\,CL,\ \text{prop delay and Q prop delay and set} - \text{up time}}$$ where n = number of packages

   b) Not using Delayed Clock:

   $$FMAX = \frac{1}{\text{propagation delay and set} - \text{up time}}$$

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V (Worst Case)	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES:

1. All voltages referenced to device GND.
2. VDD = 5V, CL = 50pF, RL = 200K
3. See Table 2 for +25°C limit.

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

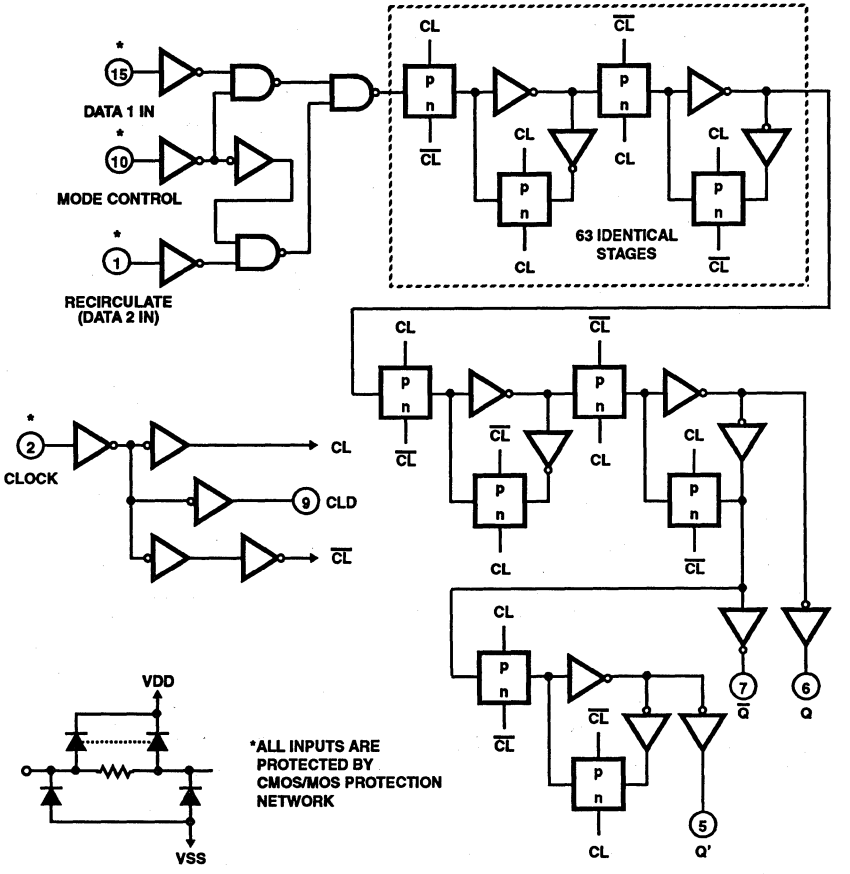
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	3 - 7, 9, 11 - 14	1, 2, 8, 10, 15	16			
Static Burn-In 2 Note 1	3 - 7, 9, 11 - 14	8	1, 2, 10, 15, 16			
Dynamic Burn-In Note 1	3 - 5, 11 - 14	8, 15	1, 16	6, 7, 9	2	10
Irradiation Note 2	3 - 7, 9, 11 - 14	8	1, 2, 10, 15, 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram



INPUT CONTROL CIRCUIT TRUTH TABLE

DATA	RECIR	MODE	BIT INTO STAGE 1
1	X	0	1
0	X	0	0
X	1	1	1
X	0	1	0

1 = High Level
X = Don't Care
0 = Low Level
NC = No Change

TYPICAL STAGE TRUTH TABLE

DATA	CL	DATA + 1
0	⌐	0
1	⌐	1
X	⌐	NC

1 = High Level
X = Don't Care
0 = Low Level
NC = No Change

TRUTH TABLE FOR OUTPUT FROM Q' (TERMINAL 5)

DATA + 64	CL	DATA + 64 1/2
0	⌐	0
1	⌐	1
X	⌐	NC

1 = High Level
X = Don't Care
0 = Low Level
NC = No Change

Typical Performance Characteristics

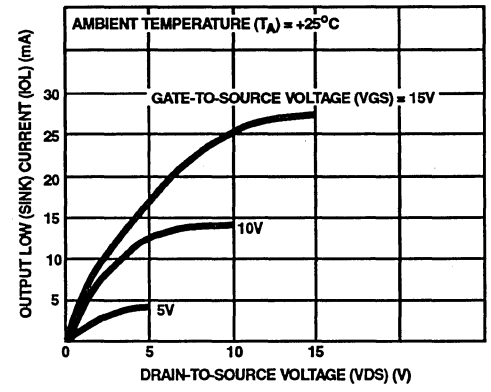


FIGURE 1 . TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS (Q SINK CURRENT = 4X ORDINATE)

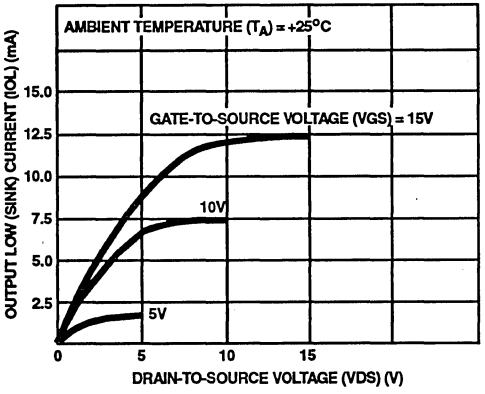


FIGURE 2. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS (Q SINK CURRENT = 4X ORDINATE)

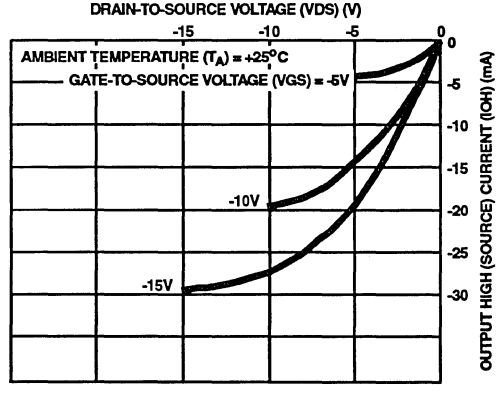


FIGURE 3. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

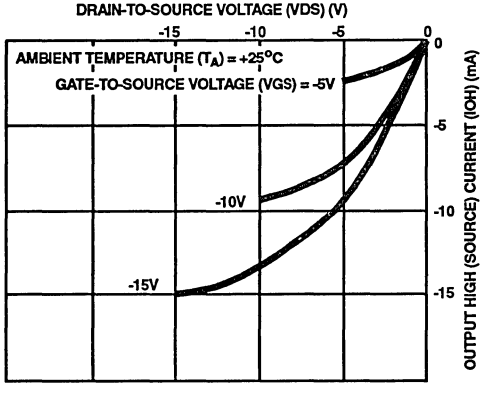


FIGURE 4. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

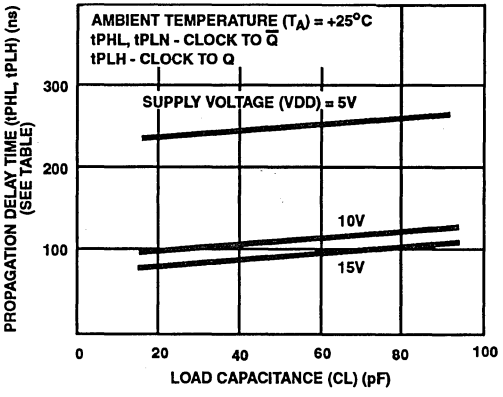


FIGURE 5. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (SEE TABLE)

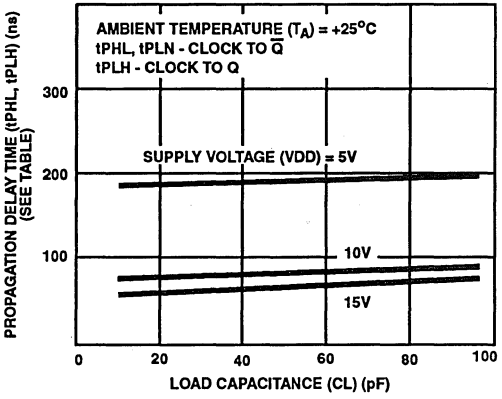


FIGURE 6. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (SEE TABLE)

Typical Performance Characteristics (Continued)

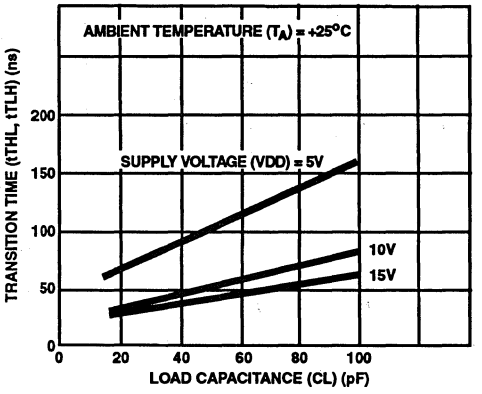


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE (EXCEPT Q, tTHL)

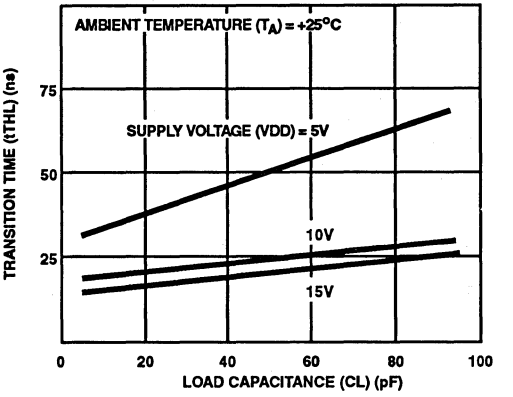


FIGURE 8. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE (Q, tTHL)

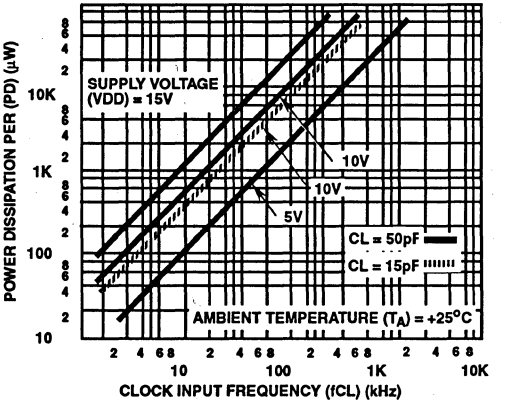


FIGURE 9. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF CLOCK INPUT FREQUENCY

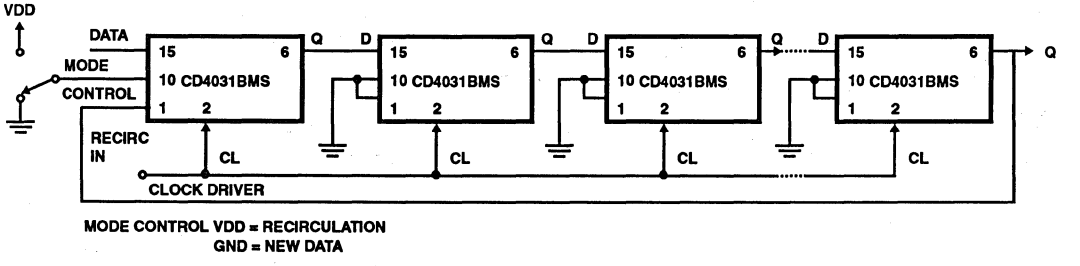


FIGURE 10. CASCADING USING DIRECT CLOCKING FOR HIGH-SPEED OPERATION (SEE CLOCK RISE AND FALL TIME REQUIREMENT)

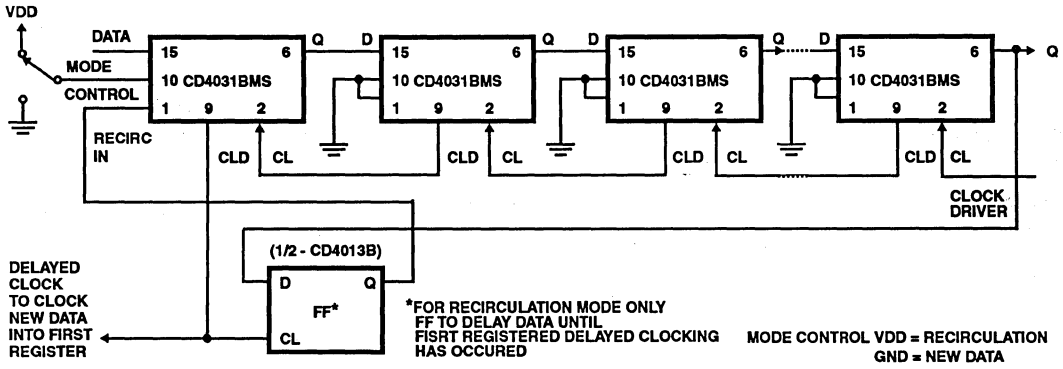


FIGURE 11. CASCADING USING DELAYED CLOCKING FOR REDUCED CLOCK DRIVE REQUIREMENTS

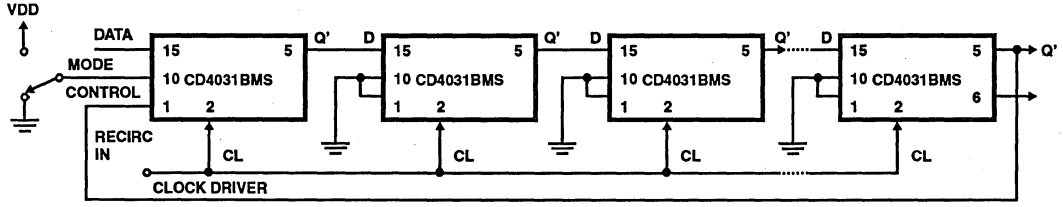
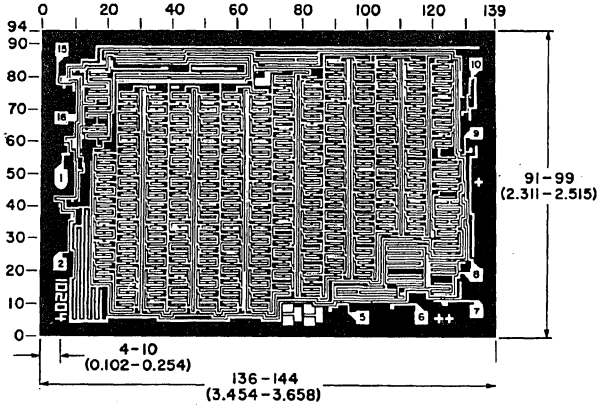


FIGURE 12. CASCADING USING HALF-CLOCK-PULSE DELAYED OUTPUT (Q') TO PERMIT USE OF SLOW RISE AND FALL CLOCK INPUTS

Chip Dimensions and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4033BMS

December 1992

CMOS Decade Counter/Divider

Features

- High Voltage Types (20V Rating)
- Decoded 7 Segment Display Outputs and Ripple Blanking
- Counter and 7 Segment Decoding In One Package
- Easily Interfaced with 7 Segment Display Types
- Fully Static Counter Operation DC to 6MHz (typ.) at VDD = 10V
- Ideal for Low-Power Displays
- "Ripple Blanking" and Lamp Test
- 100% Tested for Quiescent Current at 20V
- Standardized Symmetrical Output Characteristics
- 5V, 10V and 15V Parametric Ratings
- Schmitt-Triggered Clock Inputs
- Meets All Requirements of JEDEC Tentative Standards No. 13B, "Standard Specifications for Description of "B" Series CMOS Device's

Applications

- Decade Counting 7 Segment Decimal Display
- Frequency Division 7 Segment Decimal Displays
- Clocks, Watches, Timers (e.g. + 60, + 60, +12 Counter/Display
- Counter/Display Driver For Meter Applications

Description

CD4033BMS consists of a 5 stage Johnson decade counter and an output decoder which converts the Johnson code to a 7 segment decoded output for driving one stage in a numerical display.

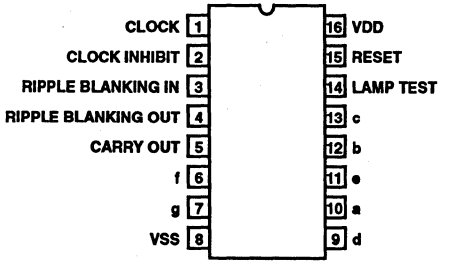
This device is particularly advantageous in display applications where low power dissipation and/or low package count is important.

A high RESET signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. The CLOCK INHIBIT signal can be used as a negative-edge clock if the clock line is held high. Antilock gating is provided on the JOHNSON counter, thus assuring proper counting sequence. The CARRY-OUT (Cout) signal completes one cycle every ten CLOCK INPUT cycles and is used to clock the succeeding decade directly in a multi-decade counting chain.

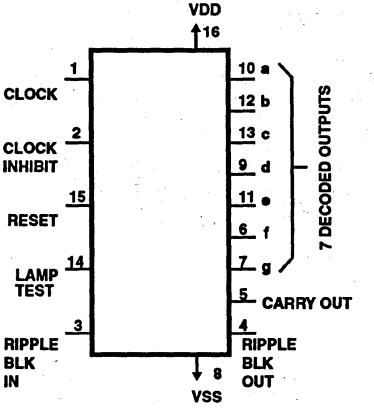
The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven segment display device used for representing the decimal numbers 0 to 9. The 7 segment outputs go high on selection.

Pinout

CD4033BMS
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3301

The CD4033BMS has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.0700 in an eight digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the CD4033BMS associated with the most significant digit in the display to a low-level voltage and connecting the RBO terminal of that stage to the RBI terminal of the CD4033BMS in the next-lower significant position in the display. This procedure is continued for each succeeding CD4033BMS on the interger side of the display.

On the fraction side of the display the RBI of the CD4033BMS associated with the least significant bit is connected to a low-level voltage and the RBO of that CD4033BMS is connected to the RBI terminal of the CD4033BMS in the next more-significant-bit position. Again, this procedure is continued for all CD4033BMS's on the fraction side of the display.

In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a high level voltage (instead of to the RBO of the next more-significant-stage). For example: optional zero → 0.7346. Likewise, the zero in a number such as 763.0 can be displayed by connecting the RBI of the CD4033BMS associated with it to a high-level voltage.

Ripple blanking of non-significant zeros provides an appreciable savings in display power.

The CD4033BMS has a LAMP TEST input which, when connected to a high-level voltage, overrides normal decoder operation and enables a check to be made on possible display malfunctions by putting the seven outputs in the high state.

The CD4033BMS are supplied in these 16 lead outline packages:

Braze Seal DIP	H4W
Frit Seal DIP	H2R
Ceramic Flatpack	H6W

Logic Diagram

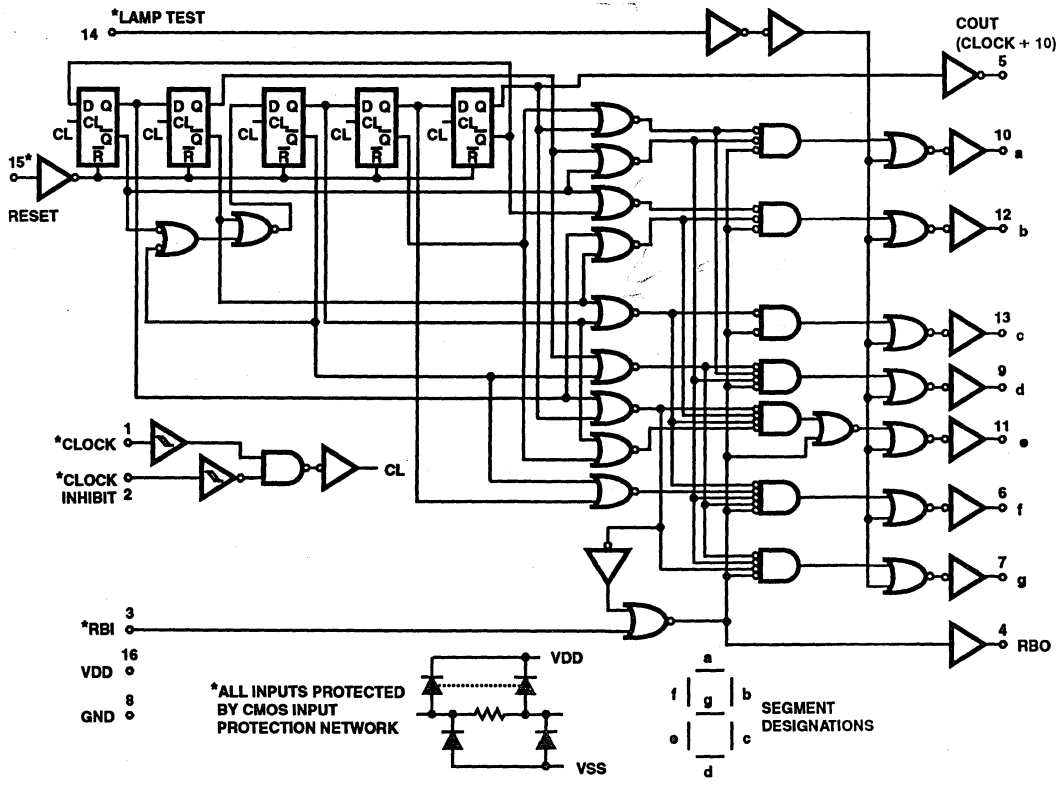


FIGURE 1. CD4033BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range.....-55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG) .....-65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature .....+175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock To Carry Out	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Propagation Delay Clock To Decode Out	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	700	ns
			10, 11	+125°C, -55°C	-	945	ns
Propagation Delay Reset To Carry Out	TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	550	ns
			10, 11	+125°C, -55°C	-	743	ns
Propagation Delay Reset To Decode Out	TPHL4 TPLH4	VDD = 5V, VIN = VDD or GND	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	2.5	-	MHz
			10, 11	+125°C, -55°C	1.85	-	MHz

NOTES:

1. VDD = 5V, CL = 50pF, RL = 200K
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-2.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Clock To Carry Out	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	150	ns
Propagation Delay Clock To Decode Out	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	250	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns
Propagation Delay Reset To Carry Out	TPLH3	VDD = 10V	1, 2, 3	+25°C	-	240	ns
		VDD = 15V	1, 2, 3	+25°C	-	160	ns
Propagation Delay Reset To Decode Out	TPHL4 TPLH4	VDD = 10V	1, 2, 3	+25°C	-	250	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	5.5	-	MHz
		VDD = 15V	1, 2, 3	+25°C	8	-	MHz
Minimum Reset Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	120	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Reset Removal Time	TREM	VDD = 5V	1, 2, 3	+25°C	-	30	ns
		VDD = 10V	1, 2, 3	+25°C	-	15	ns
		VDD = 15V	1, 2, 3	+25°C	-	10	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	220	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. ~~CL = 50pF, RL = 200K, Input TR, TF < 20ns.~~

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9(	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
PART NUMBER						
Static Burn-In 1 (Note 1)	4 - 7, 9 - 14	1 - 3, 8, 15	16			
Static Burn-In 2 (Note 1)	1, 2, 14, 15	3 - 6, 8, 10 - 13	7, 9, 16			
Dynamic Burn-In (Note 1)	-	2, 8, 15	3, 16	4 - 7, 9 - 13	1	

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Irradiation (Note 2)	4 - 7, 9 - 14	8	1 - 3, 15, 16			
PART NUMBER CD4033BMS						
Static Burn-In 1 Note 1	4 - 7, 9 - 13	1 - 3, 8, 14, 15	16			
Static Burn-In 2 Note 1	4 - 7, 9 - 13	8	1 - 3, 14 - 16			
Dynamic Burn-In Note 1	-	2, 3, 8, 14, 15	16	4 - 7, 9 - 13	1	
Irradiation Note 2	4 - 7, 9 - 13	8	1 - 3, 14 - 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Timing Diagram

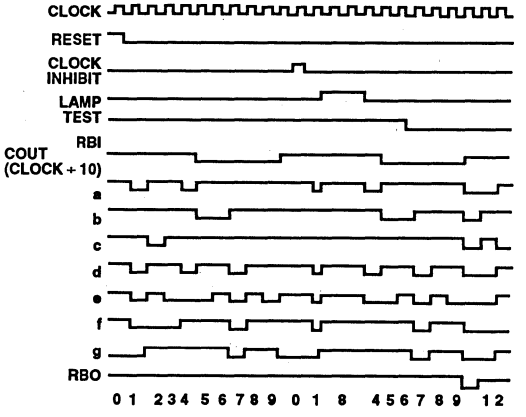


FIGURE 2. CD4033BMS TIMING DIAGRAM

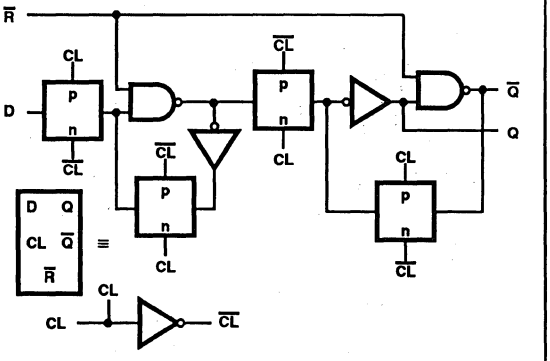


FIGURE 3. DETAIL OF TYPICAL FLIP-FLOP STAGE

Typical Performance Characteristics

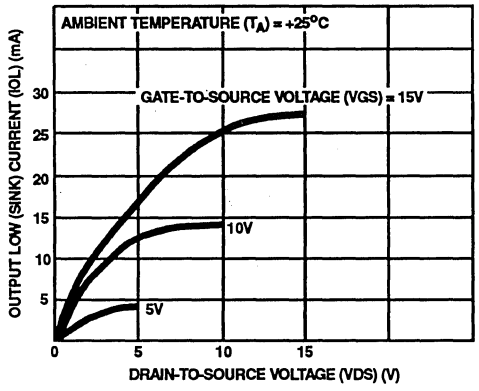


FIGURE 4. TYPICAL N-CHANNEL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

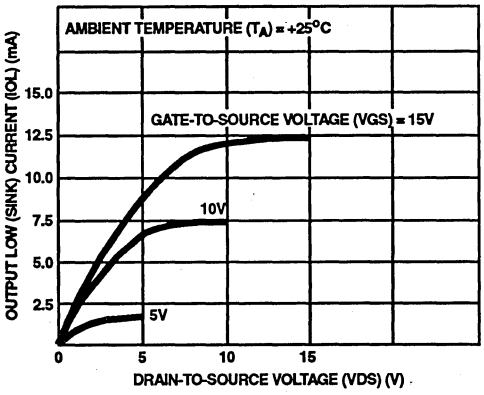


FIGURE 5. MINIMUM N-CHANNEL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

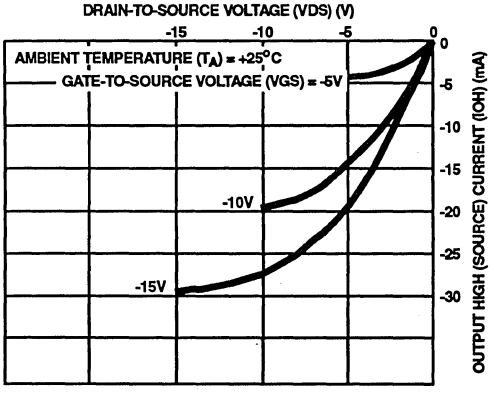


FIGURE 6. TYPICAL P-CHANNEL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

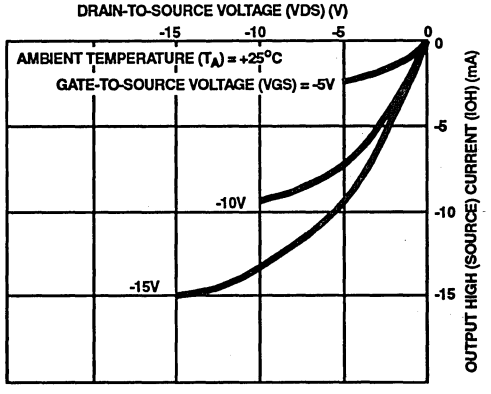


FIGURE 7. MINIMUM P-CHANNEL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

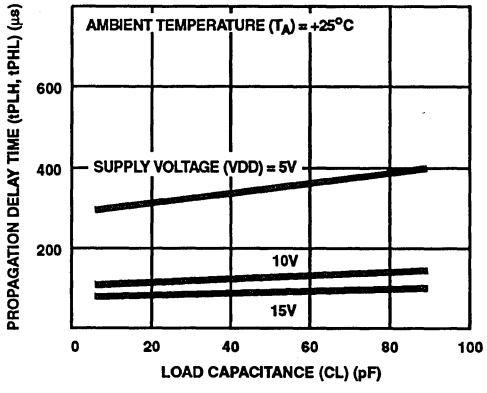


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE FOR DECODED OUTPUTS

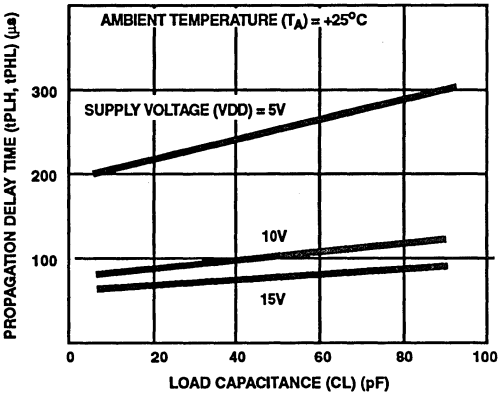


FIGURE 9. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE FOR CARRY-OUT OUTPUTS

Typical Performance Characteristics (Continued)

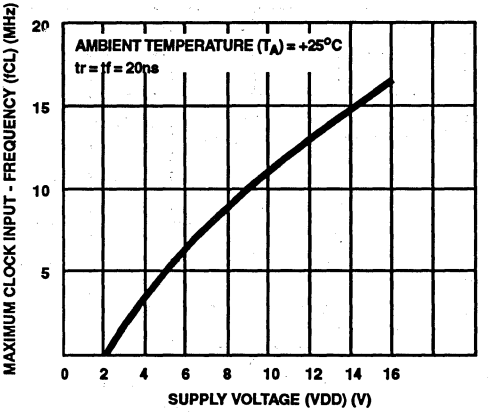


FIGURE 10. TYPICAL MAXIMUM CLOCK INPUT FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

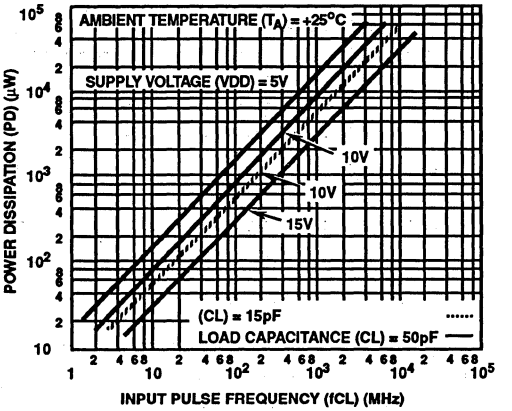


FIGURE 11. TYPICAL POWER DISSIPATION AS A FUNCTION OF CLOCK INPUT FREQUENCY

Light Emitting Diode Displays

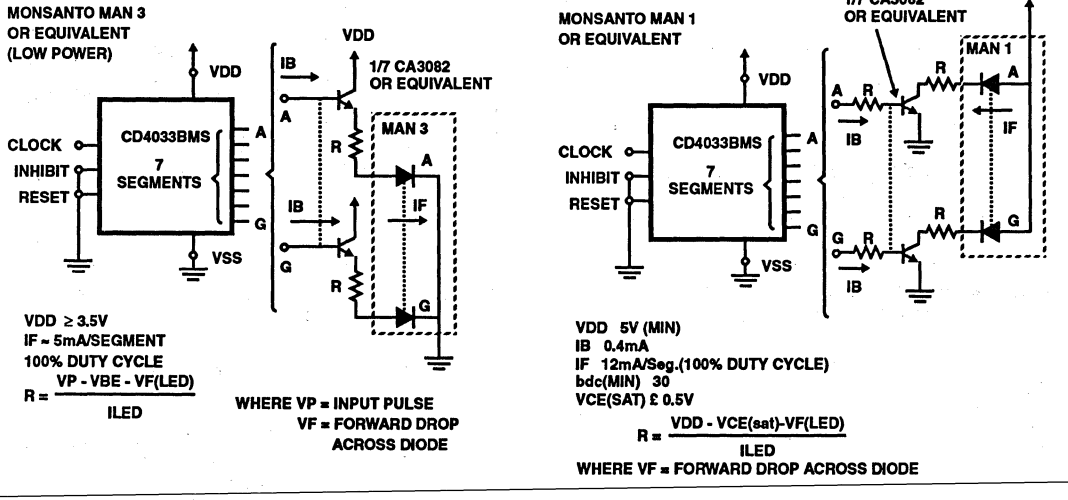
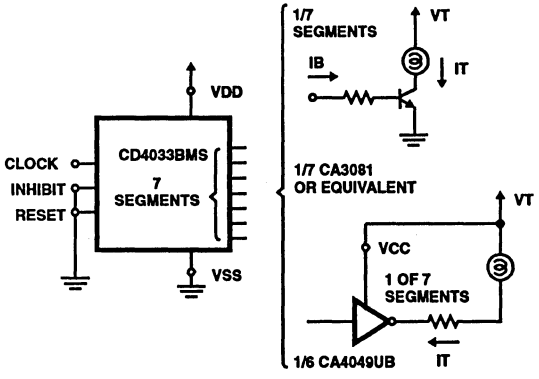


FIGURE 12. INTERFACING THE CD4033BMS WITH COMMERCIALLY AVAILABLE LIGHT EMITTING DIODE DISPLAYS

7-Segment Display Devices



INCANDESCENT READOUTS
Numitron DR2000 Series
TUBE REQUIREMENTS
VT = 3.5 - 5V
IT = 24mA Segment

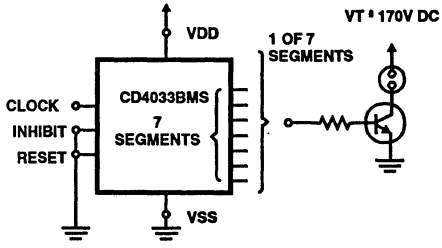
ASSUMED TRANSISTOR CHARACTERISTICS	CD4049UB
	at VCC = 10V (min) Vo "0" ≤ 2V
βdc (min) ≥ 25 VCE (sat) ≤ 0.5V VDD = 8V (min) IB = 1mA (min) IT = 24mA (min)	IT = 8mA (min) VT ≈ 3.5V to 6V
	CD4049UB
	at VCC = 10V (min) Vo "0" ≤ 0.6V IT = 8mA (min)
	at VCC = 6V (min) Vo "0" ≤ 1V IT = 5mA (min) VT ≈ 1.5V to 3.5V

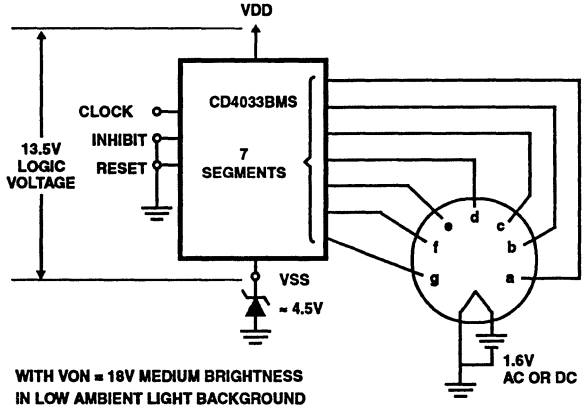
LOW-POWER INCANDESCENT READOUTS
PINLITES INC-Series O and R

TUBE REQUIREMENTS	VT(V)	mA/Segment
0-03-15	1.5	8
0-04-30	3	8
0-06-30	3	8
R-R3-20	2	4.3
R-R4-30	3	4.3

ASSUMED TRANSISTOR CHARACTERISTICS
βdc (min) ≥ 30
VCE (sat) ≤ 0.5V
VCC ≥ 3.5V (min)
IB ≥ 0.25mA (min)
IT ≤ 7.5mA (min)

*The interfacing buffers shown, while a necessity with the CD4033A, are not required when using the "B" devices; the "B" outputs (≈ 10 times the "A" outputs) can drive most display devices directly especially at voltages above 10V.





NEON READOUT (NIXIE TUBE)**
1. Alco Electronics - MG19
2. Burroughs - B5971, B7971, B8971

TUBE REQUIREMENTS	VT(Vdc)	mA/Segment
Alco MG19	180	0.5
Burroughs B5971	170	3
Burroughs B7971, B8971	170	6

**(Trademark) Burroughs Corp.
TRANSISTOR CHARACTERISTICS
Leakage with transistor cutoff - 0.05mA
V(BR)CER ..... >VT
βdc (min) ≥ 30

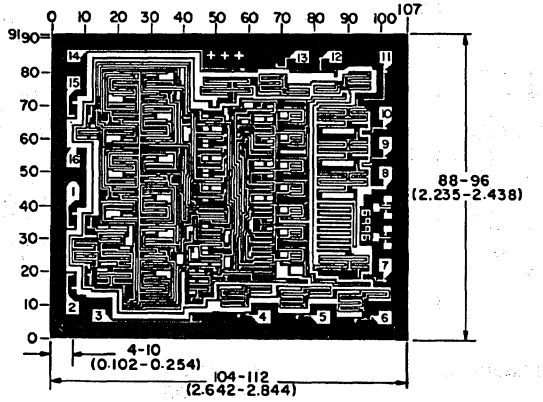
WITH VON ≈ 18V MEDIUM BRIGHTNESS IN LOW AMBIENT LIGHT BACKGROUND WILL RESULT. THE POINT OF NO NOTICEABLE GLOW IS VOFF ≈ 4.5V

LOW VOLTAGE VACUUM FLORESCENT READOUTS
1. Tung-Sol DIGIVAC S/G ‡ Type DT1704A or DT1705C
2. Nippon Electric (NEC): Type DG12E or LD915
   TUBE REQUIREMENTS: 100 to 300 μA/segment at tube voltages of 12V to 25V depending on required brightness Filament requirement 45mA at 1.6V, ac or dc.

‡ (Trademark) Wagner Electric Co.

FIGURE 13. INTERFACING THE CD4033BMS WITH COMMERCIALLY AVAILABLE 7-SEGMENT DISPLAY DEVICES*

Chip Dimensions and Pad Layouts



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4034BMS

CMOS 8-Stage Static Bidirectional Parallel/Serial Input/Output Bus Register

December 1992

Features

- High Voltage Types (20V Rating)
- Bidirectional Parallel Data Input
- Parallel or Serial Inputs/Parallel Outputs
- Asynchronous or Synchronous Parallel Data Loading
- Parallel Data-Input Enable on "A" Data Lines (3-State Output)
- Data Recirculation for Register Expansion
- Multipackage Register Expansion
- Fully Static Operation DC-to-10MHz (typ.) at VDD = 10V
- Standardized Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package-Temperature Range;
  - 100nA at 18V and +25°C
- Noise Margin (Over Full Package Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Parallel Input/Parallel Output, Serial Input/Parallel Output, Serial Input/Serial Output Register
- Shift Right/Shift Left Register
- Shift Right/Shift Left With Parallel Loading
- Address Register
- Buffer Register
- Bus System Register with Enable Parallel Lines at Bus Side
- Double Bus Register System
- Up-Down Johnson or Ring Counter
- Pseudo-Random Code Generators
- Sample and Hold Register (Storage, Counting, Display)
- Frequency and Phase Comparator

Description

CD4034BMS is a static eight-stage parallel-or serial-input parallel-output register. It can be used to:

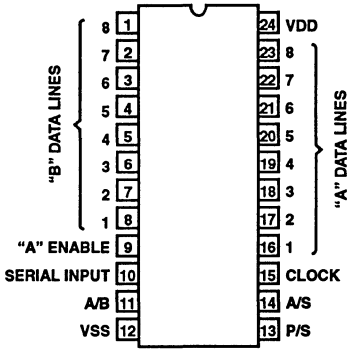
1) bidirectionally transfer parallel information between two buses, 2) convert serial data to parallel form and direct the parallel data to either of two buses, 3) store (recirculate) parallel data, or 4) accept parallel data from either of two buses and convert that data to serial form. Inputs that control the operations include a single-phase CLOCK (CL), A DATA ENABLE (AE), ASYNCHRONOUS/SYNCHRONOUS (A/S), A-BUS-TO-B-BUS/B-BUS-TO-A-BUS (A/B), and PARALLEL/SERIAL (P/S).

Data inputs include 16 bidirectional parallel data lines of which the eight A data lines are inputs (3-state outputs) and the B data lines are outputs (inputs) depending on the signal level on the A/B input. In addition, an input for SERIAL DATA is also provided.

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave. Isolation from external noise and the effects of loading is provided by output buffering.

Pinout

CD4034BMS
TOP VIEW



7 LOGIC

File Number 3307

Parallel Operation

A high P/S input signal allows data transfer into the register via the parallel data lines synchronously with the positive transition of the clock provided the A/S input is low. If the A/S input is high the transfer is independent of the clock. The direction of data flow is controlled by the A/B input. When this signal is high the A data lines are inputs (and B data lines are outputs); a low A/B signal reverses the direction of data flow.

The AE input is an additional feature which allows many registers to feed data to a common bus. The A DATA lines are enabled only when this signal is high.

Data storage through recirculation of data in each register stage is accomplished by making the A/B signal high and the AE signal low.

Serial Operation

A low P/S signal allows serial data to transfer into the register synchronously with the positive transition of the clock. The A/S input is internally disabled when the register is in the serial mode (asynchronous serial operation is not allowed).

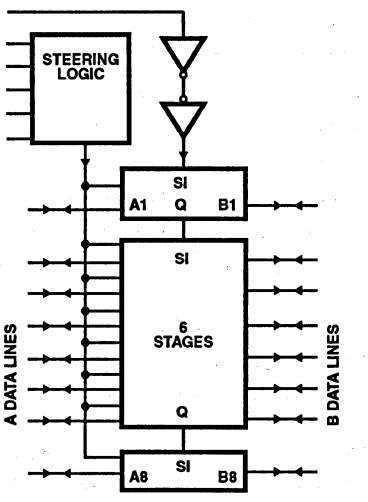
The serial data appears as output data on either the B lines (when A/B is high) or the A lines (when A/B is low and the AE signal is high).

Register expansion can be accomplished by simply cascading CD4034BMS packages.

The CD4034BMS is supplied in these 24 lead outline packages:

Braze Seal DIP	H4V
Ceramic Flatpack	H4P

Functional Diagram



Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range.....-55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG).....-65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current Except A and B Lines	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current Except A and B Lines	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.4	-	µA
				2	+125°C	-12	-	µA
			VDD = 18V	3	-55°C	-0.4	-	µA
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.4	µA
				2	+125°C	-	12	µA
			VDD = 18V	3	-55°C	-	0.4	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Parallel In to Parallel Out	TPHL TPLH	VDD = 5V, VIN = VDD or GND (Notes 1, 2)	9	+25°C	-	700	ns
			10, 11	+125°C, -55°C	-	945	ns
Propagation Delay 3 State AE to Out 'A'	TPLZ TPHZ	VDD = 5V, VIN = VDD or GND (Notes 2, 3)	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay 3-State AE to Out 'A'	TPZL TPZH	VDD = 5V, VIN = VDD or GND (Notes 2, 3)	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND (Notes 1, 2)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND (Note 2)	9	+25°C	2	-	MHz
			10, 11	+125°C, -55°C	1.48	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.
3. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Parallel In to Parallel Out	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	240	ns
		VDD = 15V	1, 2, 3	+25°C	-	170	ns
Propagation Delay Serial to Parallel Out	TPHL TPLH	VDD = 5V	1, 2, 3	+25°C	700	-	ns
		VDD = 10V	1, 2, 3	+25°C	-	240	ns
		VDD = 15V	1, 2, 3	+25°C	-	170	ns
Propagation Delay 3-State AE to Out 'A'	TPLZ TPHZ	VDD = 10V	1, 2, 3, 4	+25°C	-	160	ns
		VDD = 15V	1, 2, 3, 4	+25°C	-	120	ns
Propagation Delay 3-State AE to Out 'A'	TPZL TPZH	VDD = 10V	1, 2, 3, 4	+25°C	-	160	ns
		VDD = 15V	1, 2, 3, 4	+25°C	-	120	ns
Transition Time	TTLH TTHL	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	5	-	MHz
		VDD = 15V	1, 2, 3	+25°C	7	-	MHz
Minimum Data Setup Time Serial Data to Clock	TS	VDD = 5V	1, 2, 3	+25°C	-	160	ns
		VDD = 10V	1, 2, 3	+25°C	-	60	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Minimum Data Setup Time Parallel Data to Clock	TS	VDD = 5V	1, 2, 3	+25°C	-	50	ns
		VDD = 10V	1, 2, 3	+25°C	-	30	ns
		VDD = 15V	1, 2, 3	+25°C	-	20	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	250	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	70	ns
Maximum Clock Rise and Fall Time (Note 5)	TRCL TFCL	VDD = 5V	1, 2, 3	+25°C	-	15	µs
		VDD = 10V	1, 2, 3	+25°C	-	15	µs
		VDD = 15V	1, 2, 3	+25°C	-	15	µs
Minimum High Level Pulse Width AE, P/S, A/S	TW	VDD = 5V	1, 2, 3	+25°C	-	350	ns
		VDD = 10V	1, 2, 3	+25°C	-	140	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. CL = 50pF, RL = 1K, Input TR, TF < 20ns.
5. If more than one unit is cascaded, tRCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2, 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST PRE-IRRAD	TEST POST-IRRAD	READ AND RECORD PRE-IRRAD	READ AND RECORD POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

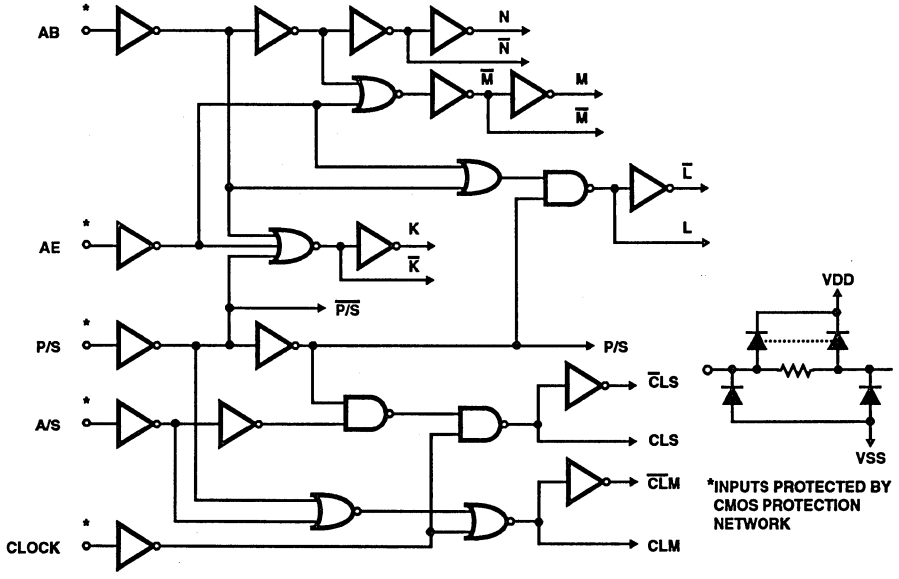
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	1 - 8	12, 15 - 23	9 - 11, 13, 14, 24			
Static Burn-In 2 Note 1	1 - 8	12	9 - 11, 13 - 24			
Dynamic Burn-In Note 1	-	1 - 8, 11 - 14	9, 24	16 - 23	15	10
Irradiation Note 2	1 - 8	12	9 - 11, 13 - 24			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram



FLIP-FLOP TRUTH TABLE

INPUTS			OUTPUT
$\overline{CLM}$	$\overline{CLS}$	D	Q
↓	↓	0	0
↑	↓	0	0
↓	↑	0	Invalid Condition
↑	↑	X	0
↓	↓	1	1
↑	↓	1	1
↓	↑	1	Invalid Condition

1 = High Level 0 = Low Level X = Don't Care

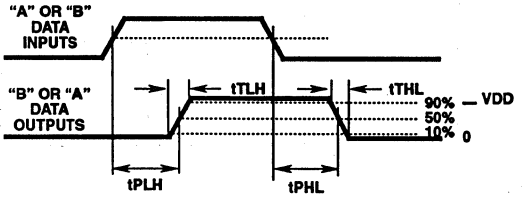
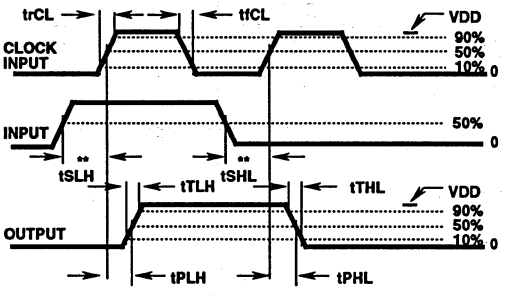


FIGURE 1. ASYNCHRONOUS OPERATION PROPAGATION DELAY TIME AND TRANSITION TIME



*Input refers to any of the "A" or "B" data inputs, "A" ENABLE, SERIAL INPUT, A/B, P/S, or A/S inputs

**tSLH and tSHL are Set-Up times

FIGURE 2. SYNCHRONOUS OPERATION PROPAGATION DELAY TIMES, TRANSITION TIMES, AND SET-UP TIMES

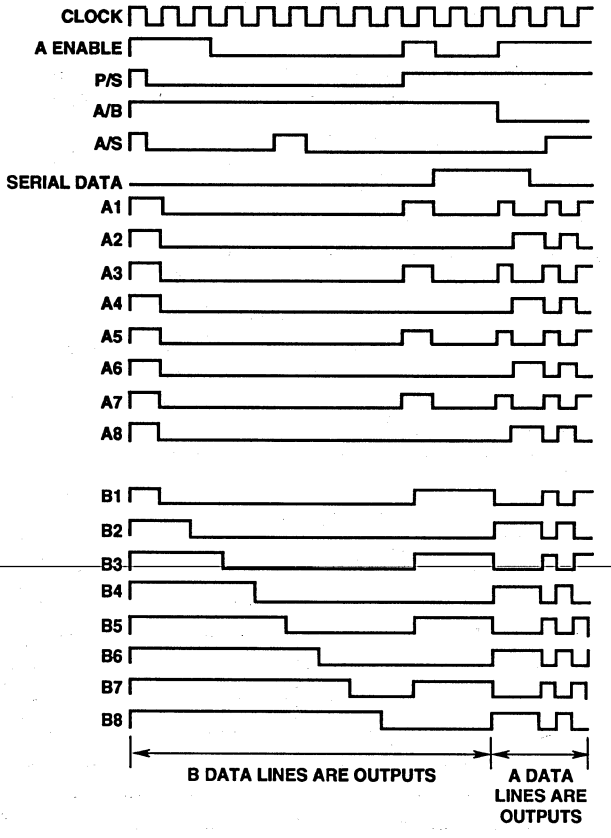


FIGURE 3. TIMING DIAGRAM

Typical Performance Characteristics

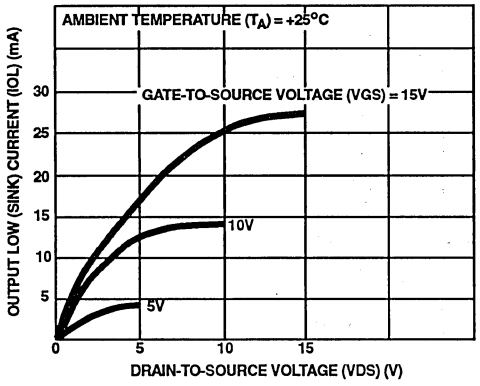


FIGURE 4. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

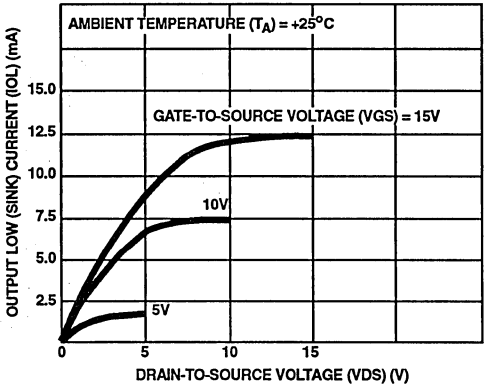


FIGURE 5. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

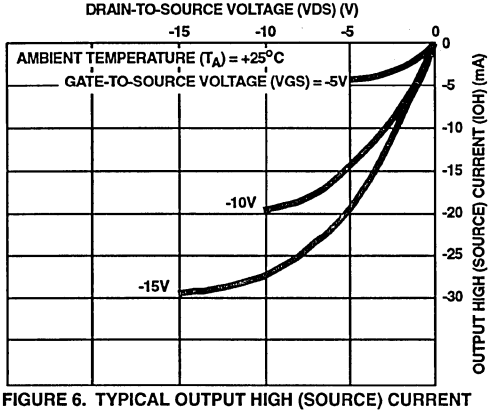


FIGURE 6. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

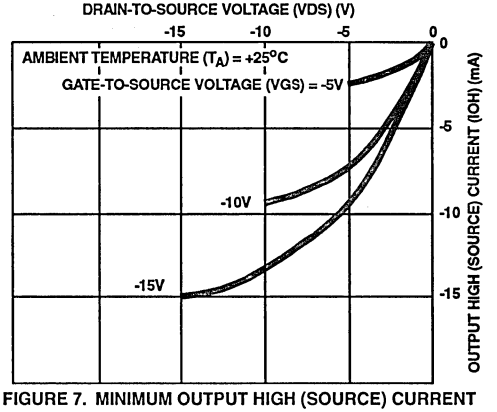


FIGURE 7. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

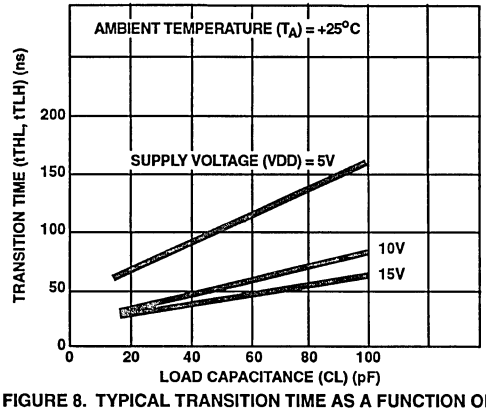


FIGURE 8. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

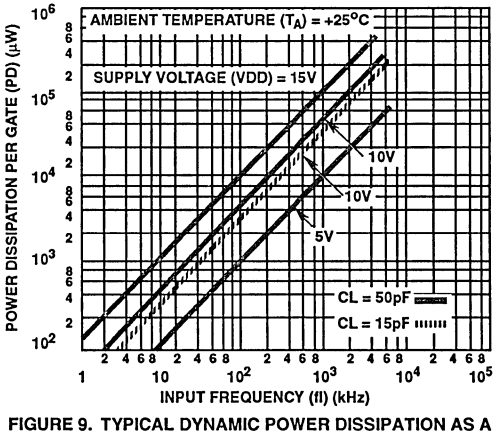


FIGURE 9. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF CLOCK FREQUENCY

Typical Performance Characteristics (Continued)

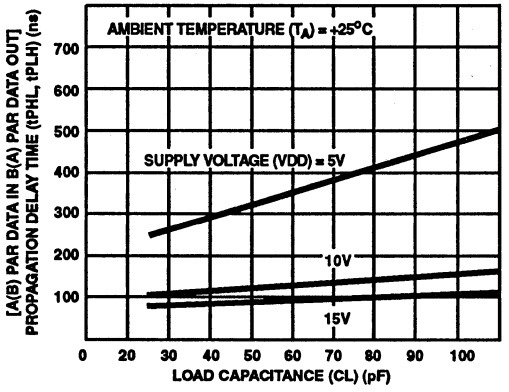


FIGURE 10. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE [A(B) PARALLEL DATA INPUT TO B(A) PARALLEL DATA OUTPUT, SYNCHRONOUS OR ASYNCHRONOUS])

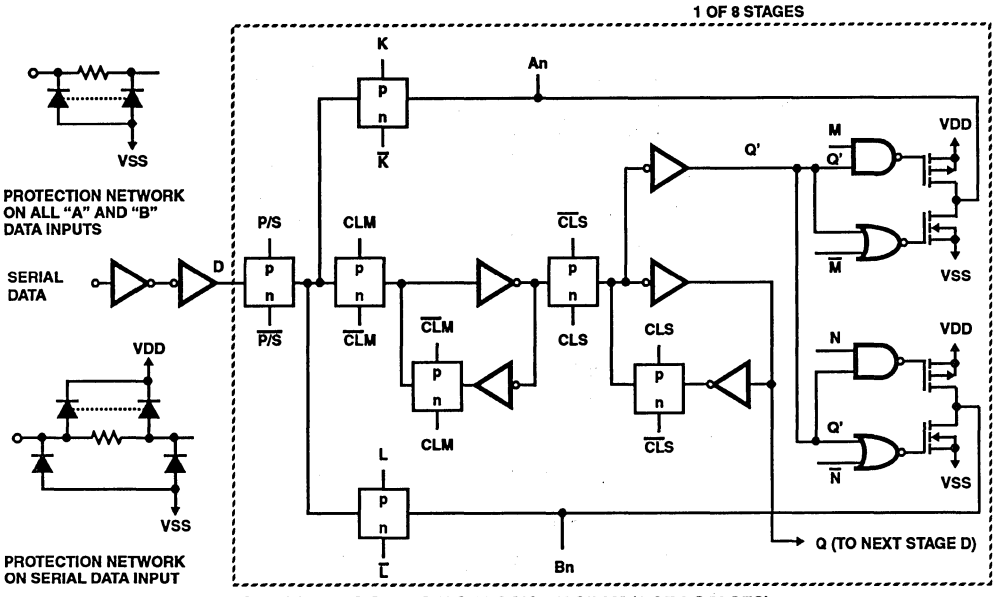


FIGURE 11. REGISTER STAGE LOGIC DIAGRAM (1 OF 8 STAGES)

TRUTH TABLE REGISTER INPUT-LEVELS AND RESULTING REGISTER OPERATION

"A" ENABLE	P/S	A/B	A/S	OPERATION*
0	0	0	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Outputs Disabled
0	0	1	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
0	1	0	0	Parallel Mode; "B" Synch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
0	1	0	1	Parallel Mode; "B" Asynch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
0	1	1	0	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Synch. Data Recirculation
0	1	1	1	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Asynch. Data Recirculation
1	0	0	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Output
1	0	1	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
1	1	0	0	Parallel Mode; "B" Synch. Parallel Data Input, "A" Parallel Data Output
1	1	0	1	Parallel Mode; "B" Asynch. Parallel Data Input, "A" Parallel Data Output
1	1	1	0	Parallel Mode; "A" Synch, Parallel Data Input, "B" Parallel Data Output
1	1	1	1	Parallel Mode; "A" Asynch. Parallel Data Input, "B" Parallel Data Output

*Outputs change at positive transition of clock in the serial mode and when the A/S control input is "low" in the parallel mode. During transfer from parallel to serial operation A/S should remain low in order to prevent DS transfer into Flip Flops.

1 = High Level 0 = Low Level X = Don't Care

Applications

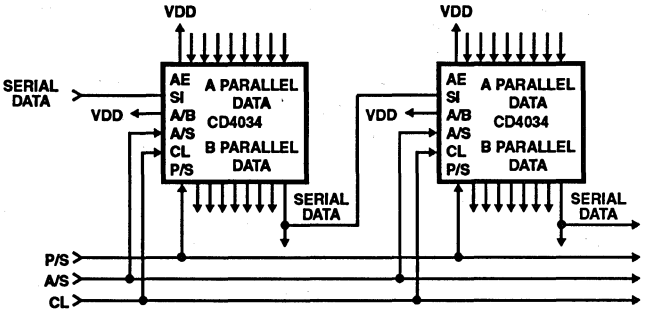


FIGURE 12. 16-BIT PARALLEL IN/PARALLEL OUT, PARALLEL IN/SERIAL OUT, SERIAL IN/PARALLEL OUT SERIAL IN/SERIAL OUT REGISTER

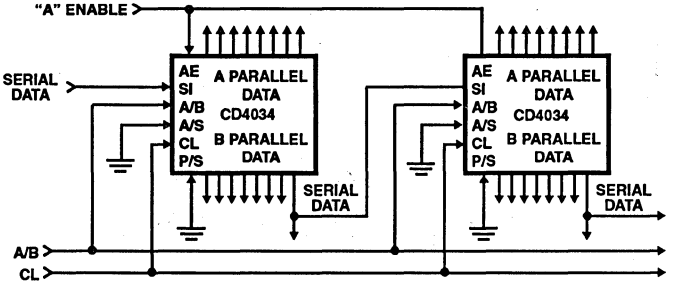
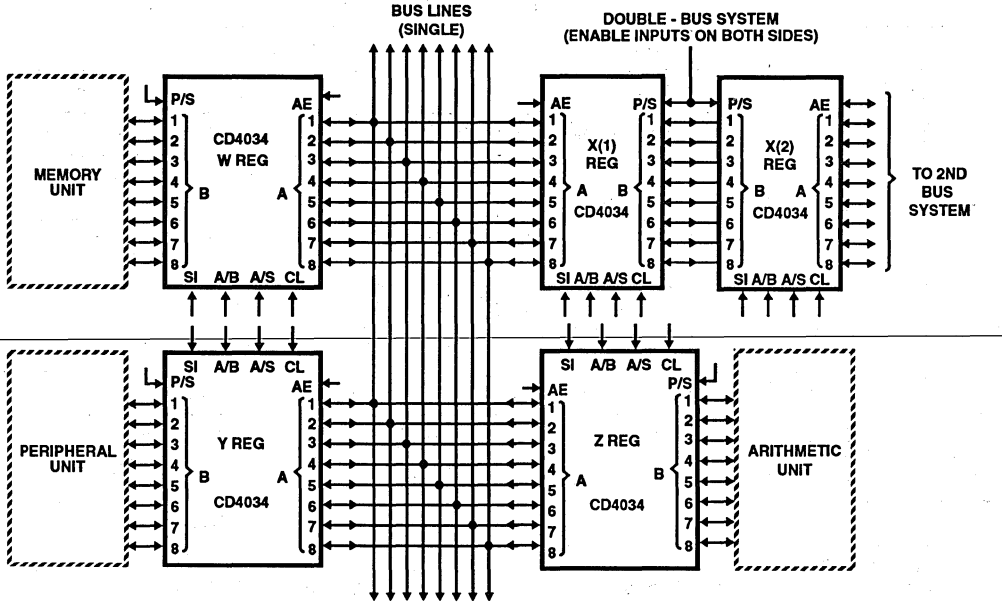


FIGURE 13. 16-BIT SERIAL IN/GATED PARALLEL OUT REGISTER



THE "A" ENABLE (AE) AND A/B SIGNALS CONTROL ALL COMBINATIONS OF TRANSFER BETWEEN THE REGISTERS AND BUS SYSTEMS

FIGURE 14. SINGLE AND DOUBLE-BUS SYSTEMS

Applications (Continued)

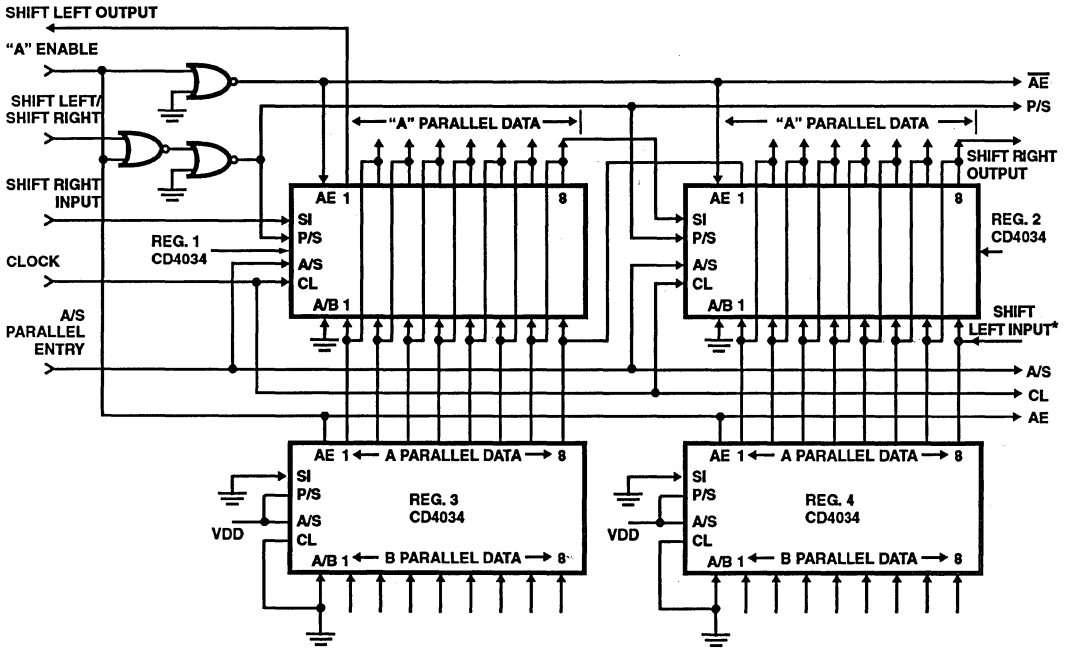


FIGURE 15. SHIFT RIGHT/SHIFT LEFT WITH PARALLEL INPUTS

A "High" ("Low") on the shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines Reg. 1 and 2 and enables the "A" data lines on registers 3 and 4 and allows parallel data into registers 1 and 2.

Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Reg. 3 and 4 and associated logic are not required.

* Shift left input must be disabled during parallel entry.

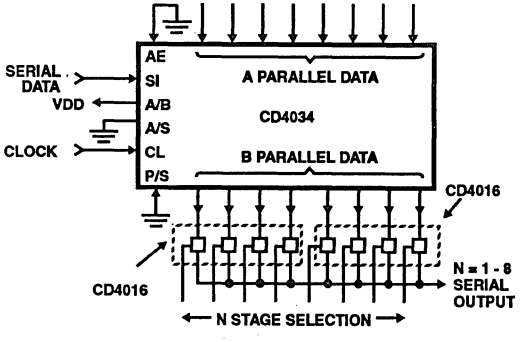


FIGURE 16. N-STAGE SHIFT REGISTER WITH FIXED SERIAL OUTPUT LINE

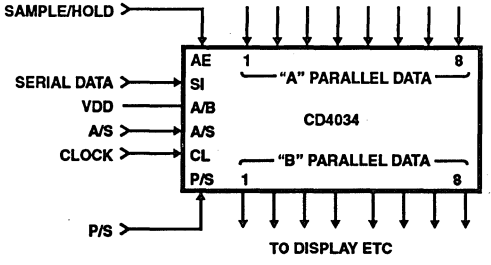
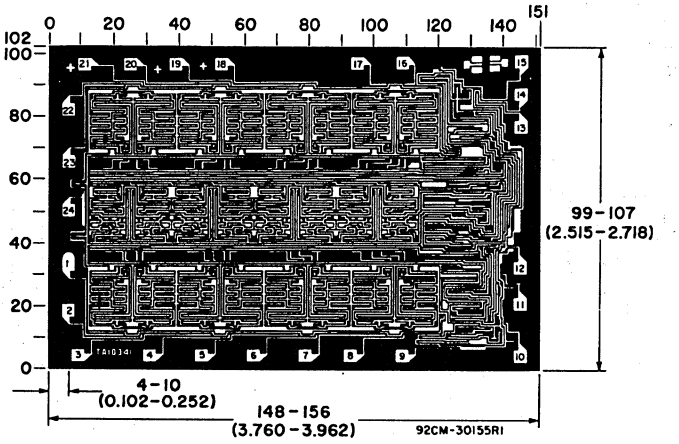


FIGURE 17. SAMPLE AND HOLD REGISTER - SERIAL/PARALLEL IN - PARALLEL OUT

7 LOGIC

Chip Dimensions and Pad Layout



Dimension in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4035BMS

CMOS 4 -Stage Parallel In/Parallel Out Shift Register

December 1992

Features

- J - $\overline{K}$ Serial Inputs and True/Complement Outputs
- High Voltage Type (20V Rating)
- 4-Stage Clocked Shift Operation
- Synchronous Parallel Entry on All 4 Stages
- J$\overline{K}$ Inputs on First Stage
- Asynchronous True/Complement Control on All Outputs
- Static Flip-Flop Operation; Master-Slave Configuration
- Buffered Inputs and Outputs
- High Speed Operation 12MHz (Typ) at VDD = 10V
- 100% Tested for Quiescent Current at 20V
- Standardized, Symmetrical Output Characteristics
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard Number 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Counters, Registers
  - Arithmetic-Unit Registers
  - Shift Left/Shift Right Registers
  - Serial-to-Parallel/Parallel-to-Serial Conversions
- Sequence Generation
- Control Circuits
- Code Conversion

Description

CD4035BMS is a four stage clocked signal serial register with provision for synchronous PARALLEL inputs to each stage and SERIAL inputs to the first stage via J$\overline{K}$ logic. Register stages 2, 3, and 4 are coupled in a serial D flip-flop configuration when the register is in the serial mode (PARALLEL/SERIAL control low).

Parallel entry into each register stage is permitted when the PARALLEL/SERIAL control is high.

In the parallel or serial mode information is transferred on positive clock transitions.

When the TRUE/COMPLEMENT control is high, the true contents of the register are available at the output terminals. When the TRUE/COMPLEMENT control is low, the outputs are the complements of the data in the register. The TRUE/COMPLEMENT control functions asynchronously with respect to the CLOCK signal.

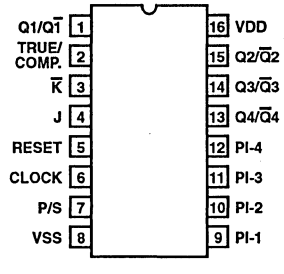
J$\overline{K}$ input logic is provided on the first stage SERIAL input to minimize logic requirements particularly in counting and sequence-generation applications. With J$\overline{K}$ inputs connected together, the first stage becomes a D flip-flop. An asynchronous common, RESET is also provided.

The CD4035BMS series type is supplied in these 16 lead outline packages

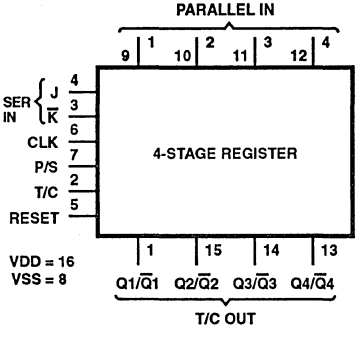
Braze Seal DIP	H4T
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

Pinout

CD4035BMS
TOP VIEW



Functional Diagram



FIRST STAGE TRUTH TABLE

CL	tn-1 (INPUT) J	K̄	R	Qn-1	tn (OUTPUT) Qn
⌐	0	X	0	0	0
⌐	1	X	0	0	1
⌐	X	0	0	1	0
⌐	1	0	0	Qn-1	Qn-1 Toggle Mode
⌐	X	1	0	1	1
¬	X	X	0	Qn-1	Qn-1
X	X	X	1	X	0

7 LOGIC

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Q	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Propagation Delay Reset to Q	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	460	ns
			10, 11	+125°C, -55°C	-	621	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	2	-	MHz
			10, 11	+125°C, -55°C	1.48	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Clock to Q	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	150	ns
Propagation Delay Reset tO Q	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	160	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Minimum Reset Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	250	ns
		VDD = 10V	1, 2, 3	+25°C	-	110	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	6	-	MHz
		VDD = 15V	1, 2, 3	+25°C	8	-	MHz
Maximum Clock Rise and Fall Time (Note 4)	TRCL TFCL	VDD = 5V	1, 2, 3	+25°C	-	15	µs
		VDD = 10V	1, 2, 3	+25°C	-	15	µs
		VDD = 15V	1, 2, 3	+25°C	-	15	µs
Minimum Data Setup Time J/$\overline{K}$ Lines	TS	VDD = 5V	1, 2, 3	+25°C	-	220	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Minimum Data Setup Time Parallel-In Lines	TS	VDD = 5V	1, 2, 3	+25°C	-	140	ns
		VDD = 10V	1, 2, 3	+25°C	-	50	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	90	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. If more than one unit is cascaded, tRCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
P Threshold Voltage	VTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0μA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE:
1. 5% parametric, 3% functional; cumulative for static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	1, 13 - 15	2 - 12	16			

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 2 Note 1	1, 13 - 15	8	2 - 7, 9 - 12, 16			
Dynamic Burn-In Note 1	1, 3, 4	2, 5, 7 - 12	16	13 - 15	6	-
Irradiation Note 2	1, 13 - 15	8	2 - 7, 9 - 12, 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram

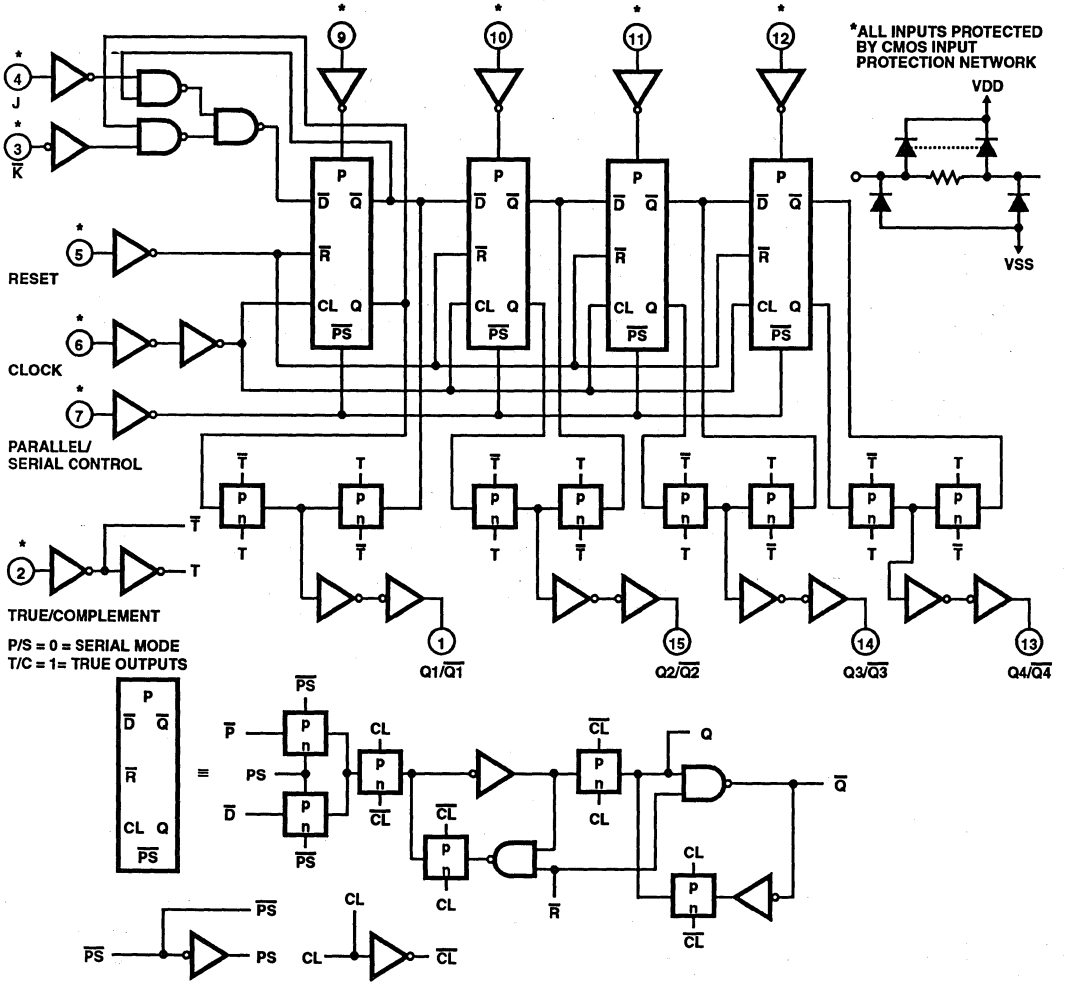


FIGURE 1. TYPICAL STAGE DETAIL LOGIC

Typical Performance Characteristics

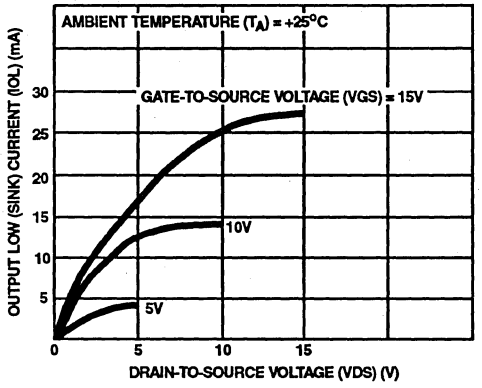


FIGURE 1 . TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

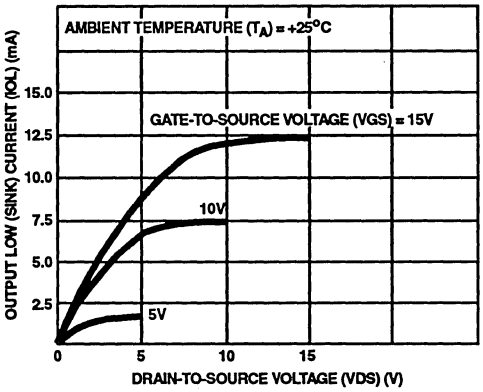


FIGURE 2. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

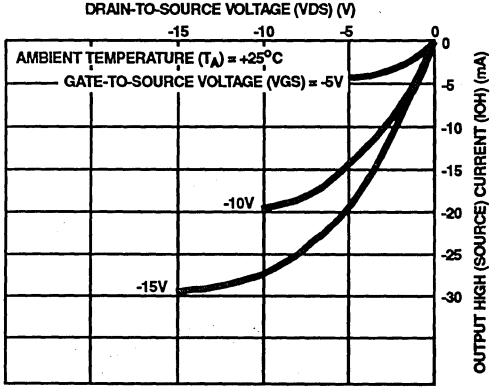


FIGURE 3. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

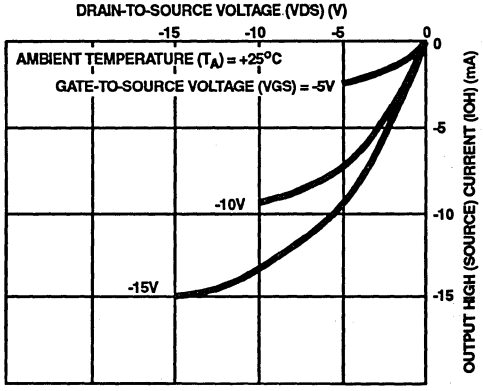


FIGURE 4. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

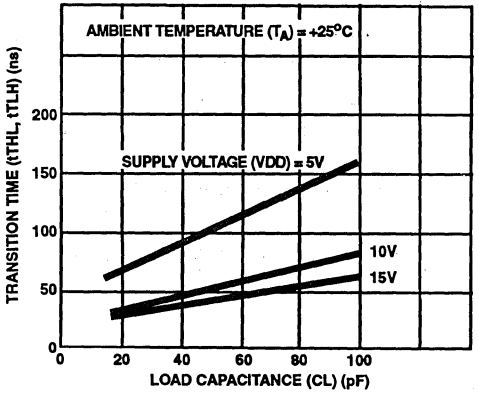


FIGURE 5. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

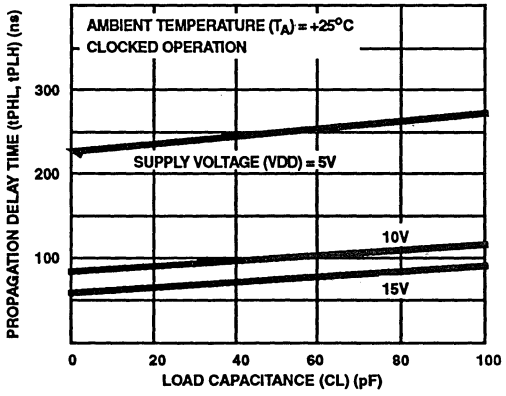


FIGURE 6. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (Q OUTPUT)

Typical Performance Characteristics (Continued)

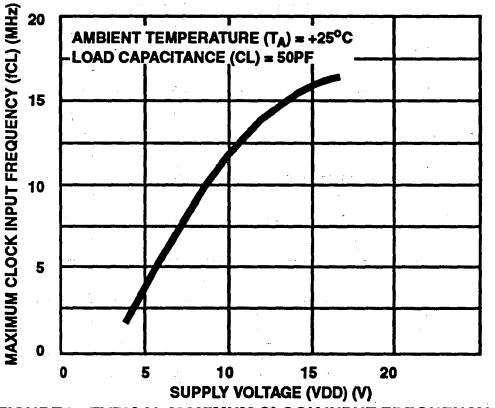


FIGURE 7. TYPICAL MAXIMUM CLOCK INPUT FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

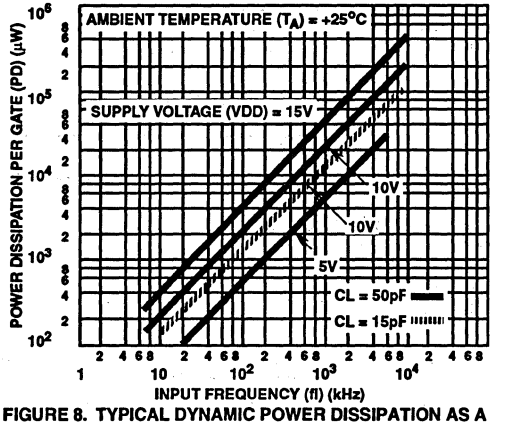


FIGURE 8. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF CLOCK INPUT FREQUENCY

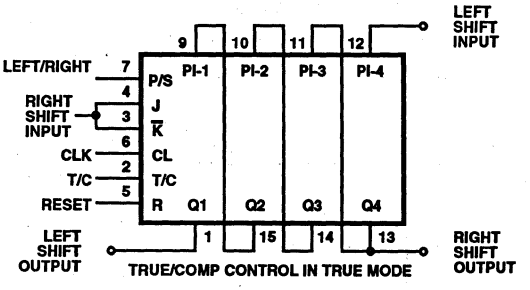
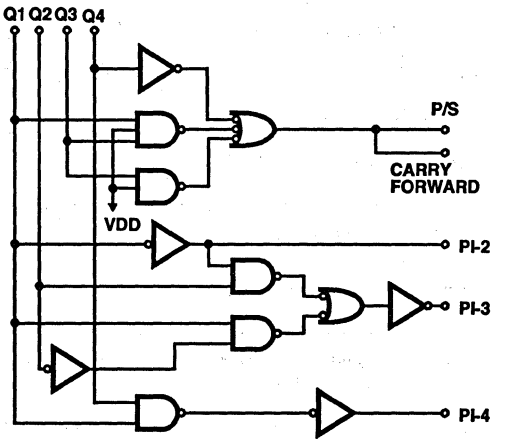


FIGURE 9. SHIFT LEFT/SHIFT RIGHT REGISTER



Using Couleur's Technique (BIDEC)*, a binary number (most significant bit, MSB) first is shifted and processed, such that the BCD equivalent is obtained when the last binary bit is clocked into the register. The CD4035BMS, with the correct conversion logic, can also be used as a BCD-to-binary converter.

*NOTE: The basic rule is: If a 4 or less is in a decade, shift with the next clock pulse; if a 5 or greater is in a decade, add 3 and then shift at the next clock pulse. For more information refer to "IRE TRANSACTIONS ON ELECTRONIC COMPUTERS", Dec. 1958, pages 313-316.

FIGURE 10. BIDEC LOGIC

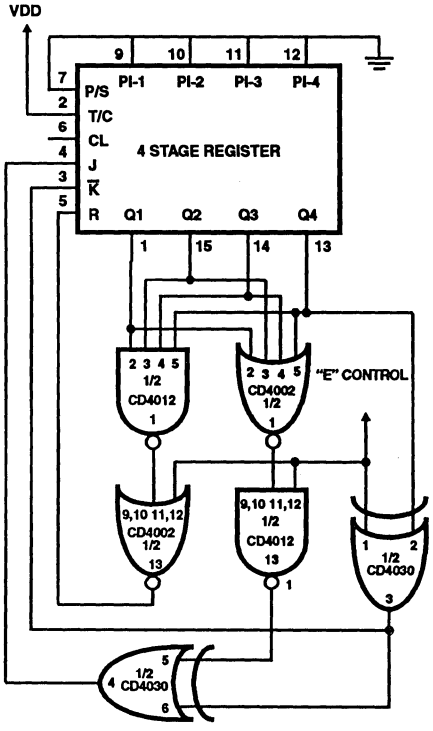


FIGURE 11(a). DOUBLE SEQUENCE GENERATOR

Control = E = 0					1				
	Q1 A	Q2 B	Q3 C	Q4 D		Q1 A	Q2 B	Q3 C	Q4 D
0	0	0	0	0	15	1	1	1	1
1	1	0	0	0	14	0	1	1	1
2	0	1	0	0	13	1	0	1	1
5	1	0	1	0	10	0	1	0	1
10	0	1	0	1	5	1	0	1	0
4	0	0	1	0	11	1	1	0	1
9	1	0	0	1	6	0	1	1	0
3	1	1	0	0	12	0	0	1	1
6	0	1	1	0	9	1	0	0	1
13	1	0	1	1	2	0	1	0	0
11	1	1	0	1	4	0	0	1	0
7	1	1	1	0	8	0	0	0	1
14	0	1	1	1	1	1	0	0	0
12	0	0	1	1	3	1	1	0	0
8	0	0	0	1	7	1	1	1	0

Using a control line (E) two different state sequences can be generated. For example, suppose the following two sequences are desired on command (control line E).

FIGURE 11(b). STATE SEQUENCES

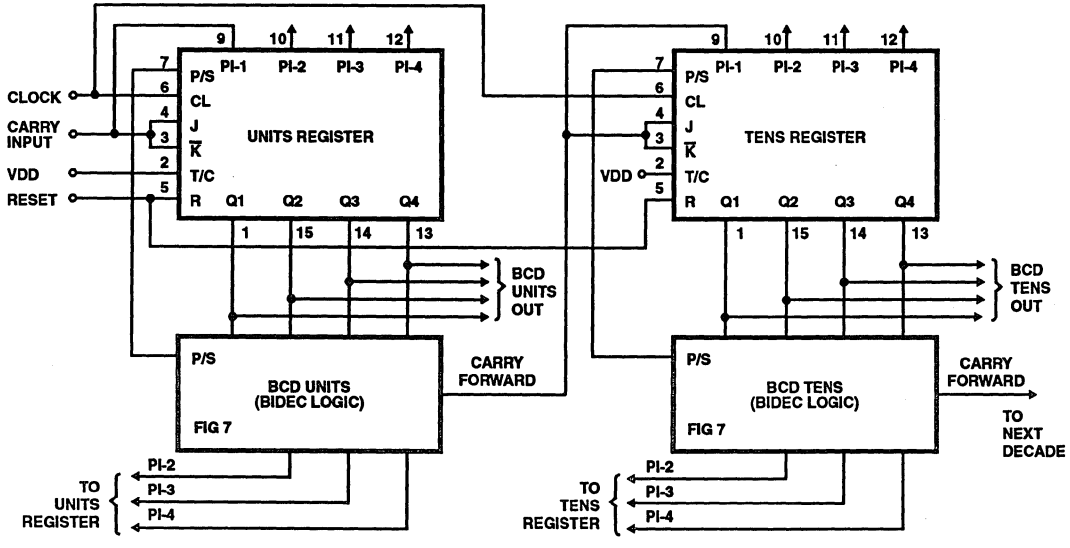
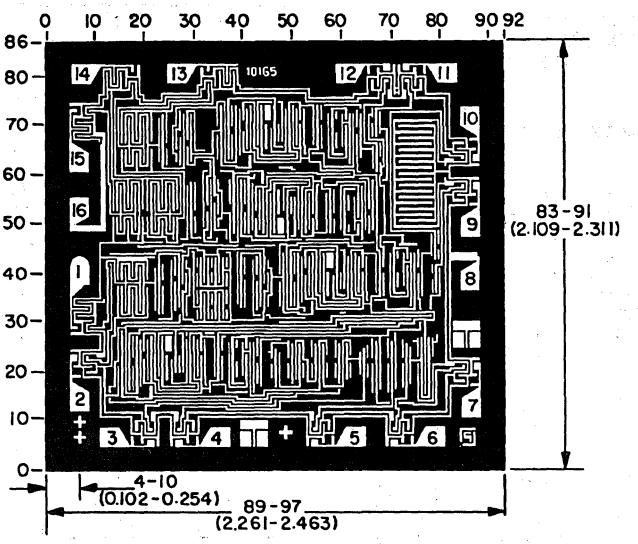


FIGURE 12. BINARY-TO-BCD CONVERTER

Chip Dimensions and Pad Layout



Dimensions in parantheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4041UBMS

December 1992

CMOS Quad True/Complement Buffer

Features

- High Voltage Type (20V Rating)
- Balanced Sink and Source Current; Approximately 4 Times Standard "B" Drive
- Equalized Delay to True and Complement Outputs
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package-Temperature Range;
  - 100nA at 18V and +25°C
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specificationsfor Description of 'B' Series CMOS Devices"

Applications

- High Current Source/Sink Driver
- CMOS-to-DTL/TTL Converter Buffer
- Display Driver
- MOS Clock Driver
- Resistor Network Driver (Ladder or Weighted R)
- Buffer
- Transmission Line Driver

Description

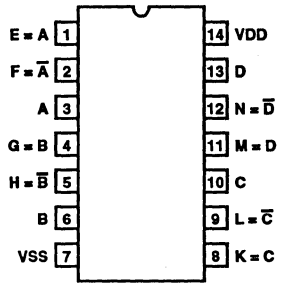
CD4041UBMS types are quad true/complement buffers consisting of n- and p- channel units having low channel resistance and high current (sourcing and sinking) capability. The CD4041UBMS is intended for use as a buffer, line driver, or CMOS-to-TTL driver. It can be used as an ultra-low power resistor-network driver for A/D and D/A conversion, as a transmission-line driver, and in other applications where high noise immunity and low power dissipation are primary design requirements.

The CD4041UBMS is supplied in these 14 lead outline packages:

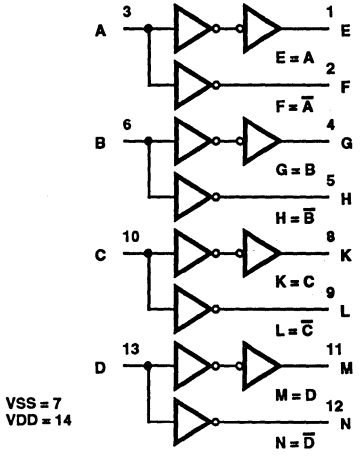
Braze Seal DIP	H4Q
Frit Seal DIP	H1B
Ceramic Flatpack	H3W

Pinout

CD4041UBMS
TOP VIEW



Functional Diagram



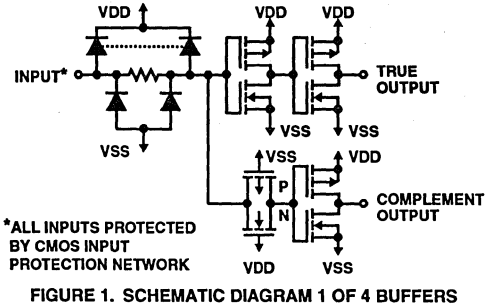


FIGURE 1. SCHEMATIC DIAGRAM 1 OF 4 BUFFERS

7 LOGIC

File Number 3309

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K).....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature .....+175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	1.6	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	5.0	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	19	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-1.6	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-6.4	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-5.0	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-19	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.0	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	4.0	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	2.5	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	12.5	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	120	ns
			10, 11	+125°C, -55°C	-	162	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	80	ns
			10, 11	+125°C, -55°C	-	108	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	1.2	-	mA
				-55°C	2.1	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	3.5	-	mA
				-55°C	6.25	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	13	-	mA
				-55°C	24	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-1.2	mA
				-55°C	-	-2.1	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-4.6	mA
				-55°C	-	-8.4	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-3.5	mA
				-55°C	-	-6.25	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-13	mA
				-55°C	-	-24	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	2	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	8	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	70	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V	1, 2, 3	+25°C	-	30	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	22.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9, Deltas	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	1, 2, 4, 5, 8, 9, 11, 12	3, 6, 7, 10, 13	14			
Static Burn-In 2 (Note 1)	1, 2, 4, 5, 8, 9, 11, 12	7	3, 6, 10, 13, 14			
Dynamic Burn-In (Note 2)	-	7	14	1, 2, 4, 5, 8, 9, 11, 12	3, 6, 10, 13	
Irradiation (Note 3)	1, 2, 4, 5, 8, 9, 11, 12	7	3, 6, 10, 13, 14			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 4.75K ± 5%; VDD = 18V ± 0.5V
3. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Typical Performance Characteristics

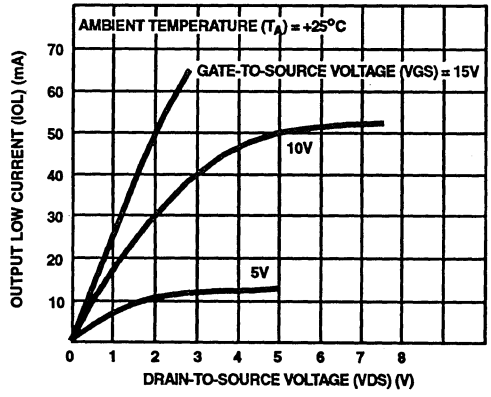


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

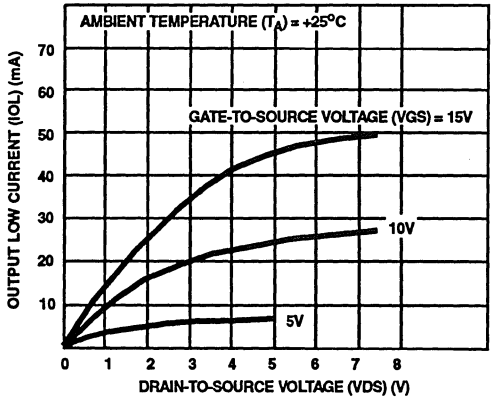


FIGURE 3. MINIMUM LOW (SINK) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

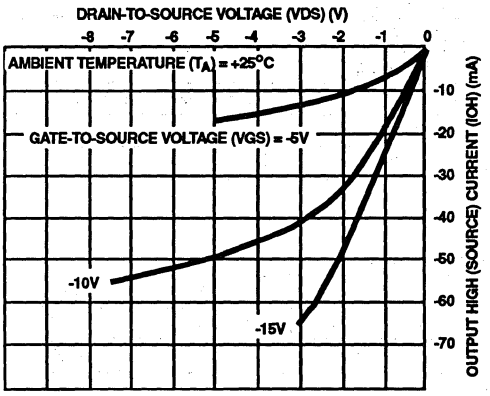


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

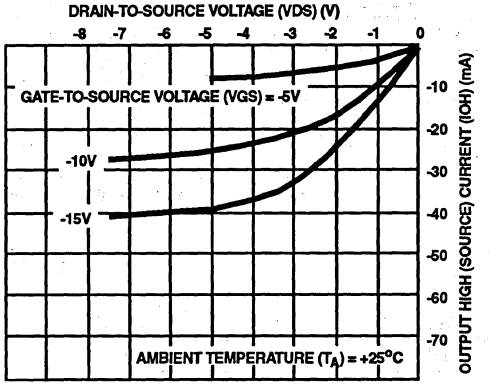


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

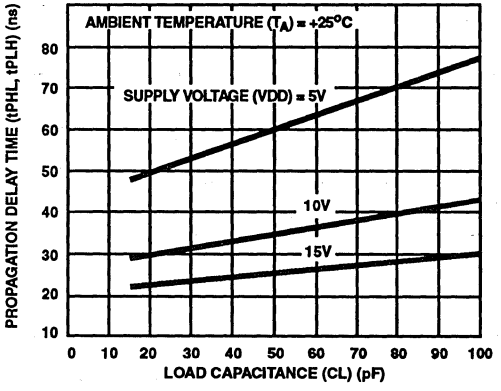


FIGURE 6. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE

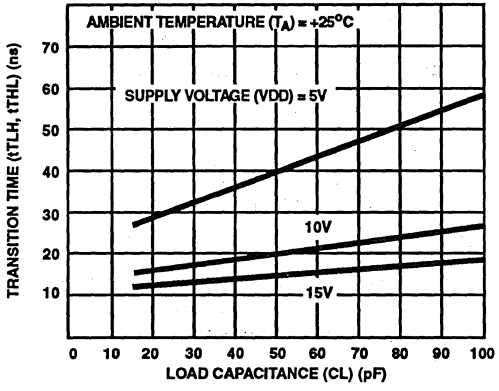


FIGURE 7. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

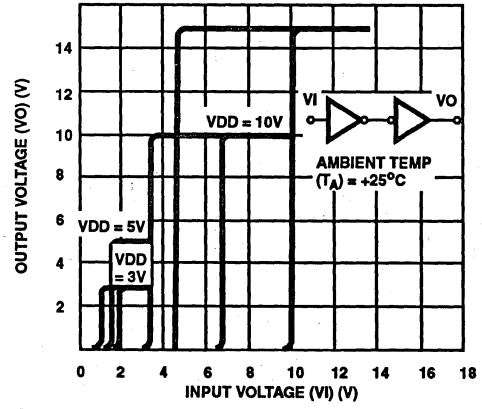


FIGURE 8. MINIMUM AND MAXIMUM TRANSFER CHARACTERISTICS - TRUE OUTPUT

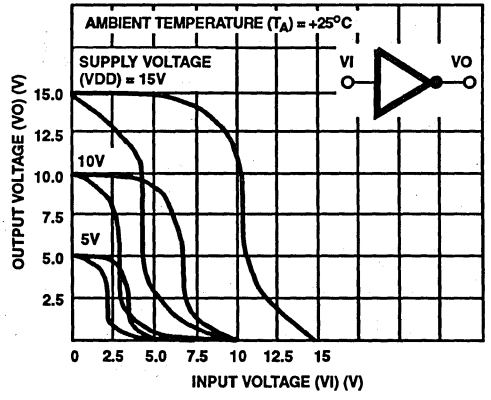


FIGURE 9. MINIMUM AND MAXIMUM TRANSFER CHARACTERISTICS - COMPLEMENT OUTPUT

Typical Performance Characteristics (Continued)

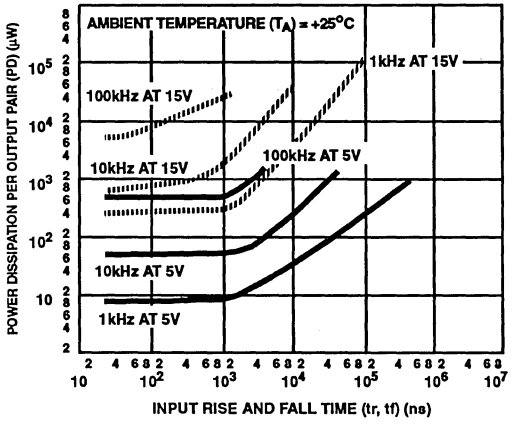


FIGURE 10. TYPICAL POWER DISSIPATION vs INPUT RISE AND FALL TIME PER OUTPUT PAIR

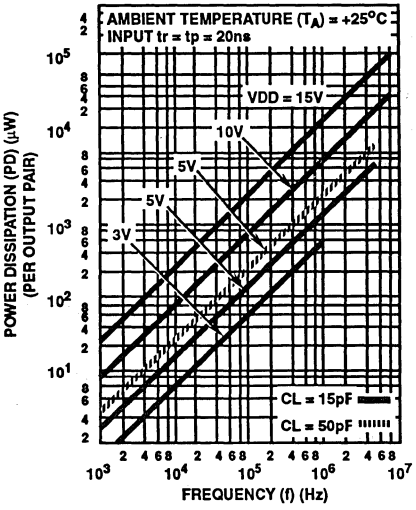
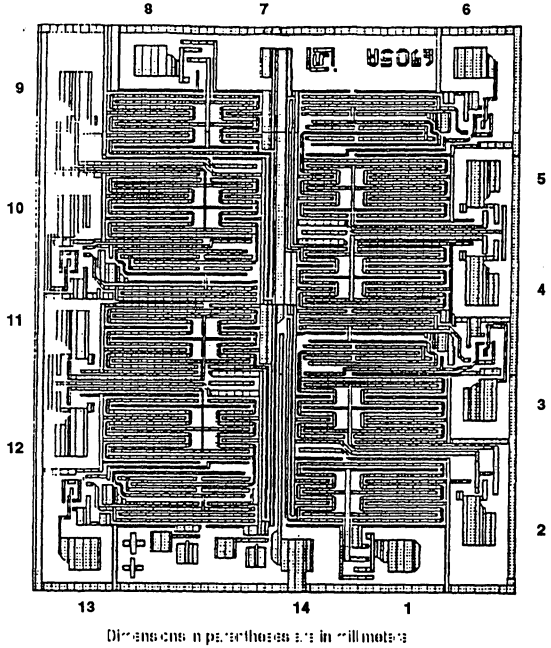


FIGURE 11. TYPICAL POWER DISSIPATION vs FREQUENCY PER OUTPUT PAIR

Chip Dimensions and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches
DIE SIZE: X = 72 (69 - 77)
Y = 82 (79 - 87)

7 LOGIC

HARRIS SEMICONDUCTOR

CD4042BMS

December 1992

CMOS Quad Clocked "D" Latch

Features

- High-Voltage Type (20V Rating)
- Clock Polarity Control
- Q and $\overline{Q}$ Outputs
- Common Clock
- Low Power TTL Compatible
- Standardized Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- 5V, 10V and 15V Parametric Ratings
- Noise Margin (Over Full Package Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Buffer Storage
- Holding Register
- General Digital Logic

Description

CD4042BMS types contain four latch circuits, each strobed by a common clock. Complementary buffered outputs are available from each circuit. The impedance of the n- and p- channel output devices is balanced and all outputs are electrically identical.

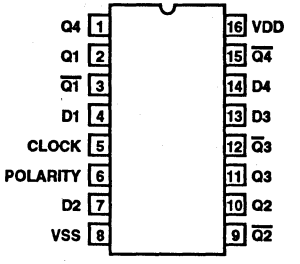
Information present at the data input is transferred to outputs Q and Q during the CLOCK level which is programmed by the POLARITY input. For POLARITY = 0 the transfer occurs during the 0 CLOCK level and for POLARITY = 1 the transfer occurs during the 1 CLOCK level. The outputs follow the data input defined above are present. When a CLOCK transition occurs (positive for POLARITY = 0 and negative for POLARITY = 1) the information present at the input during the CLOCK transition is retained at the outputs until an opposite CLOCK transition occurs.

The CD4042BMS is supplied in these 16 lead outline packages:

Braze Seal DIP	H4T
Frit Seal DIP	H1E
Ceramic Flatpack	H6W

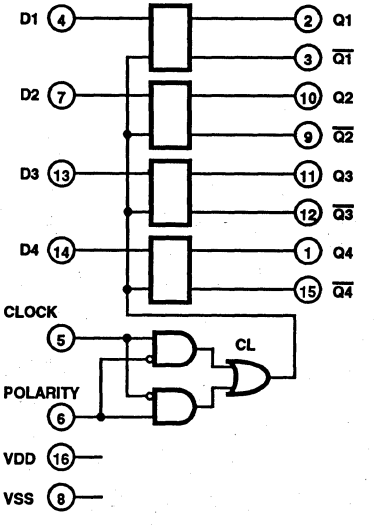
Pinout

CD4042BMS
TOP VIEW



NC = NO CONNECTION

Functional Diagram



Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND.
2. Go/no go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTES 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay (Note 2) Data in to Q	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	220	ns
			10, 11	+125°C, -55°C	-	297	ns
Propagation Delay (Note 2) Data in to $\overline{Q}$	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	300	ns
			10, 11	+125°C, -55°C	-	405	ns
Propagation Delay (Note 2) Clock to Q	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	450	ns
			10, 11	+125°C, -55°C	-	608	ns
Propagation Delay (Note 2) Clock to $\overline{Q}$	TPHL4 TPLH4	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Transition Time (Note 2)	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. VDD = 5V, CL = 50pF, RL = 200K, input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Data in to Q	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	110	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Propagation Delay Data in to $\overline{Q}$	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	150	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Propagation Delay Clock to Q	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	160	ns
Propagation Delay Clock to $\overline{Q}$	TPLH4 TPHL4	VDD = 10V	1, 2, 3	+25°C	-	230	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns
Transition Time	TTHL	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Clock Input Rise and Fall Time (Note 4)	TRCL TFCL	VDD = 5V	1, 2, 3	+25°C	-	*	-
		VDD = 10V	1, 2, 3	+25°C	-	*	-
		VDD = 15V	1, 2, 3	+25°C	-	*	-
Minimum Data Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	50	ns
		VDD = 10V	1, 2, 3	+25°C	-	30	ns
		VDD = 15V	1, 2, 3	+25°C	-	25	ns
Minimum Data Hold Time	TH	VDD = 5V	1, 2, 3	+25°C	-	120	ns
		VDD = 10V	1, 2, 3	+25°C	-	60	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K.
4. * Not sensitive

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE:
1. 1.5% parametric, 3% functional; cumulative for static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

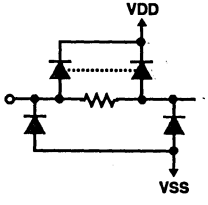
FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	1 - 3, 9 - 12, 15	4 - 8, 13, 14	16			
Static Burn-In 2 Note 1	1 - 3, 9 - 12, 15	8	4 - 7, 13, 14, 16			
Dynamic Burn-In Note 1	-	8	6, 16	1 - 3, 9 - 12, 15	5	4, 7, 13, 14
Irradiation Note 2	1 - 3, 9 - 12, 15	8	4 - 7, 13, 14, 16			

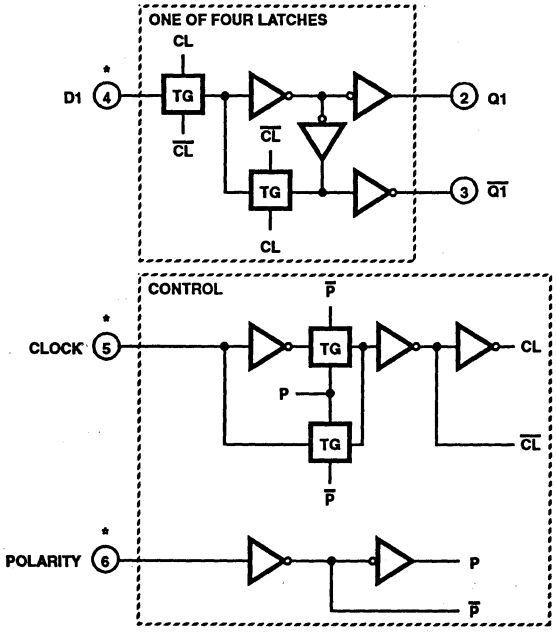
NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram

*ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK





LOGIC BLOCK DIAGRAM

TRUTH TABLE

CLOCK	POLARITY	Q
0	0	D
↗	0	LATCH
1	1	D
↘	1	LATCH

Typical Performance Characteristics

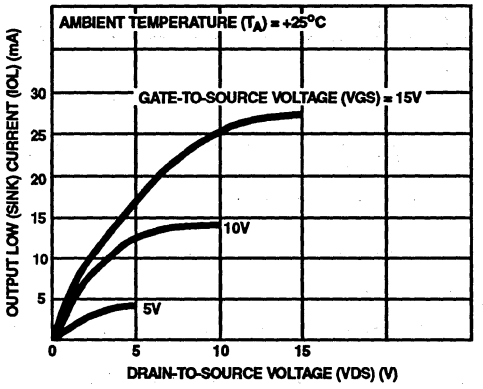


FIGURE 1. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

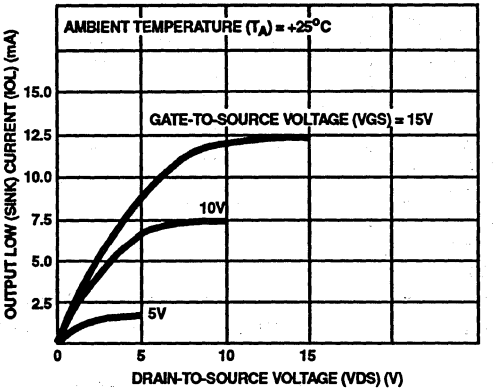


FIGURE 2. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

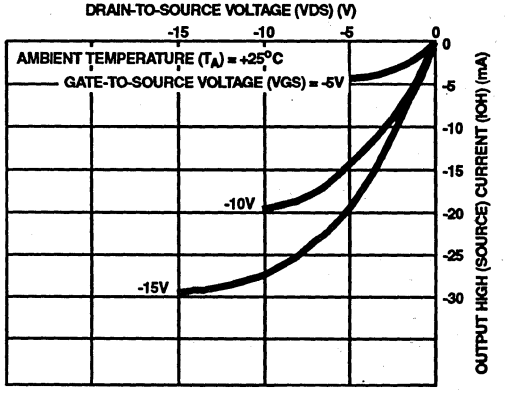


FIGURE 3. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

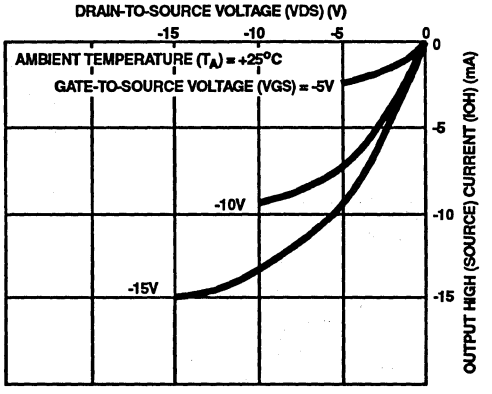


FIGURE 4. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

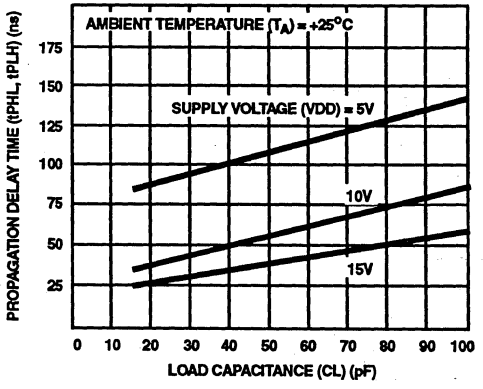


FIGURE 5. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE - DATA TO Q

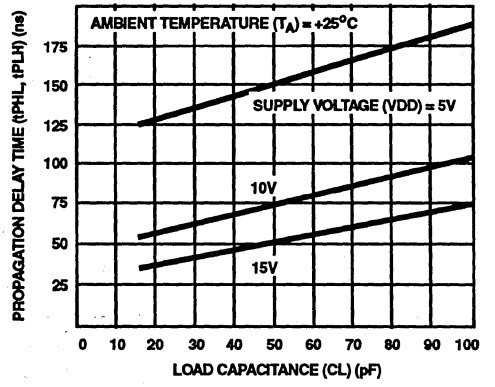


FIGURE 6. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE - DATA TO $\overline{Q}$

Typical Performance Characteristics (Continued)

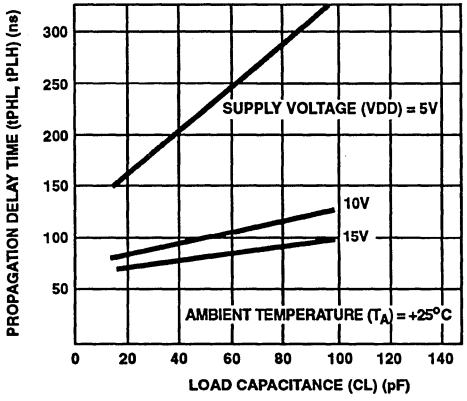


FIGURE 7. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE - CLOCK TO Q

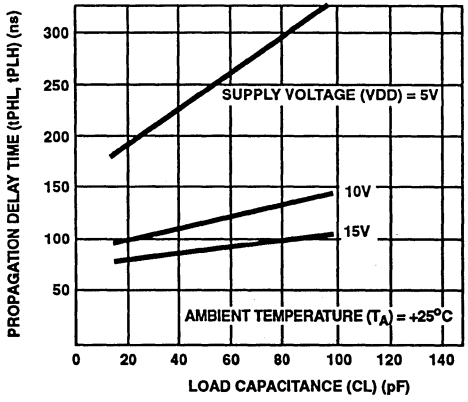


FIGURE 8. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE - CLOCK TO $\overline{Q}$

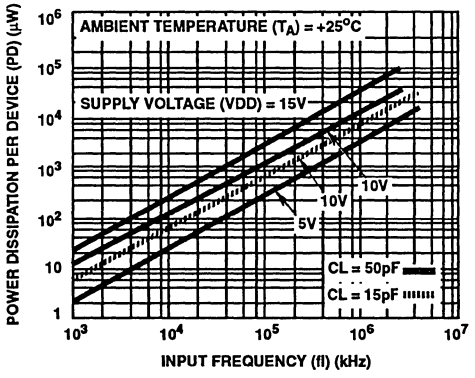


FIGURE 9. TYPICAL POWER DISSIPATION vs FREQUENCY

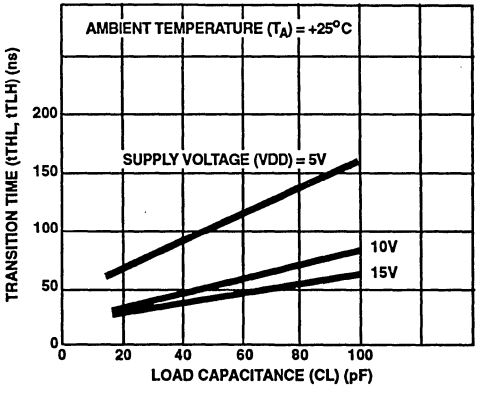
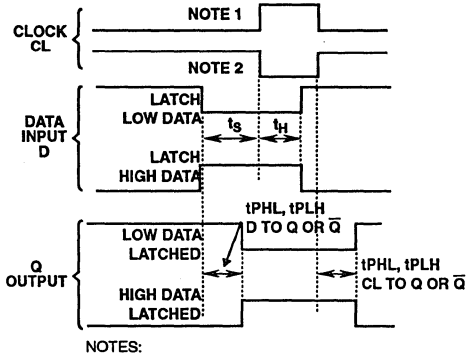


FIGURE 10. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

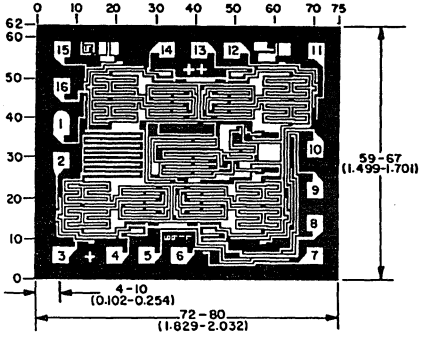


NOTES:

1. For positive clock edge, input data is latched when polarity is low.
2. For negative clock edge, input data is latched when polarity is high.

FIGURE 11. DYNAMIC TEST PARAMETERS

Chip Dimensions and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated Grid graduations are in mils (10^{-3} inch).

HARRIS SEMICONDUCTOR

CD4043BMS
CD4044BMS

December 1992

CMOS Quad 3 State R/S Latches

Features

- High Voltage Types (20V Rating)
- Quad NOR R/S Latch- CD4043BMS
- Quad NAND R/S Latch - CD4044BMS
- 3 State Outputs with Common Output ENABLE
- Separate SET and RESET Inputs for Each Latch
- NOR and NAND Configuration
- 5V, 10V and 15V Parametric Ratings
- Standardized Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μa at 18V Over Full Package-Temperature Range;
  - 100nA at 18V and 25°C
- Noise Margin (Over Full Package Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Holding Register in Multi-Register System
- Four Bits of Independent Storage with Output ENABLE
- Strobed Register
- General Digital Logic
- CD4043BMS for Positive Logic Systems
- CD4044BMS for Negative Logic Systems

Description

CD4043BMS types are quad cross-coupled 3-state CMOS NOR latches and the CD4044BMS types are quad cross-coupled 3-state CMOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are controlled by a common ENABLE input. A logic "1" or high on the ENABLE input connects the latch states to the Q outputs. A logic "0" or low on the ENABLE input disconnects the latch states from the Q outputs, results in an open circuit feature allows common busing of the outputs.

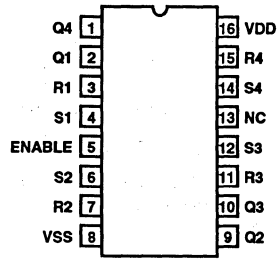
The CD4043BMS and CD4044BMS are supplied in these 16-lead outline packages:

Braze Seal DIP	*H4T	†H4T
Frit Seal DIP	*H1C	†HIE
Ceramic Flatpack	*H3X	†H6W

*CD4043B Only †CD4044B Only

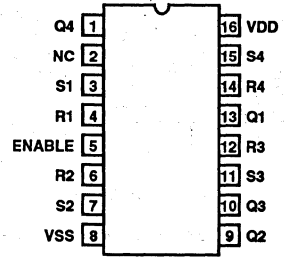
Pinout

CD4043BMS
TOP VIEW



NC = NO CONNECTION

CD4044BMS
TOP VIEW



NC = NO CONNECTION

File Number 3311

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K).....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature .....+175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.4	-	µA
				2	+125°C	-12	-	µA
			VDD = 18V	3	-55°C	-0.4	-	µA
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.4	µA
				2	+125°C	-	12	µA
			VDD = 18V	3	-55°C	-	0.4	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Set or Reset to Q	TPHL TPLH	VDD = 5V, VIN = VDD or GND (Notes 1, 2)	9	+25°C	-	300	ns
			10, 11	+125°C, -55°C	-	405	ns
Propagation Delay 3 - State Enable to Q	TPHZ TPZH	VDD = 5V, VIN = VDD or GND (Notes 2, 3)	9	+25°C	-	230	ns
			10, 11	+125°C, -55°C	-	311	ns
Propagation Delay 3 - State Enable to Q	TPLZ TPZL	VDD = 5V, VIN = VDD or GND (Notes 2, 3)	9	+25°C	-	180	ns
			10, 11	+125°C, -55°C	-	243	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND (Notes 1, 2)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.
1. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Set or Reset to Q	TPLH TPHL	VDD = 10V	1, 2, 3	+25°C	-	140	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Propagation Delay 3 State Enable to Q	TPHZ TPZH	VDD = 10V	1, 2, 4	+25°C	-	110	ns
		VDD = 15V	1, 2, 4	+25°C	-	80	ns
Propagation Delay 3 State Enable to Q	TPLZ TPZL	VDD = 10V	1, 2, 4	+25°C	-	100	ns
		VDD = 15V	1, 2, 4	+25°C	-	70	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Minimum Set or Reset Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	160	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

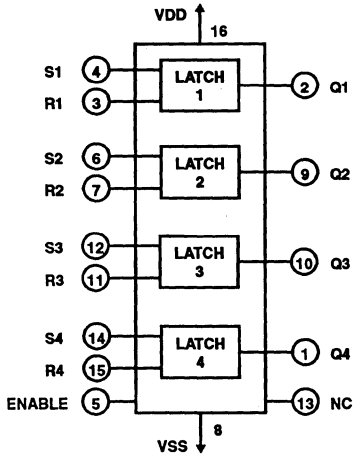
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
PART NUMBER	CD4043BMS					
Static Burn-In 1 Note 1	1, 2, 9, 10, 13	3 - 8, 11, 12, 14, 15	16			
Static Burn-In 2 Note 1	1, 2, 9, 10, 13	8	3 - 7, 11, 12, 14 - 16			
Dynamic Burn-In Note 1	13	8	5, 16	1, 2, 9, 12	4, 6, 12, 14	3, 7, 11, 15
Irradiation Note 2	1, 2, 9, 10, 13	8	3 - 7, 11, 12, 14 - 16			
PART NUMBER	CD4044BMS					
Static Burn-In 1 Note 1	1, 2, 9, 10, 13	3 - 8, 11, 12, 14, 15	16			
Static Burn-In 2 Note 1	1, 2, 9, 10, 13	8	3 - 7, 11, 12, 14 - 16			
Dynamic Burn-In Note 1	2	8	5, 16	1, 9, 10, 13	4, 6, 12, 14	3, 7, 11, 15
Irradiation Note 2	1, 2, 9, 10, 13	8	3 - 7, 11, 12, 14 - 16			

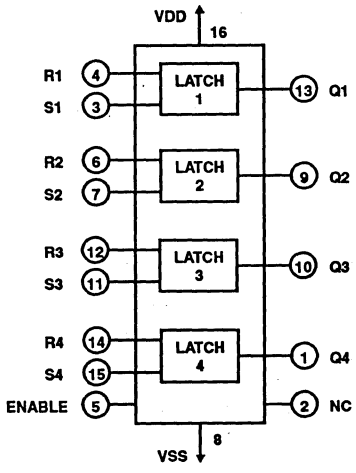
NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Functional Diagram

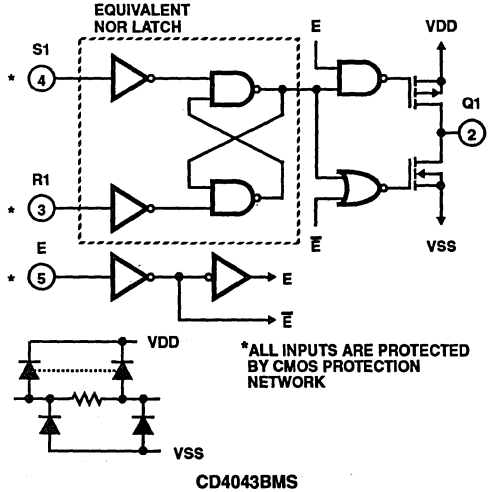


CD4043BMS

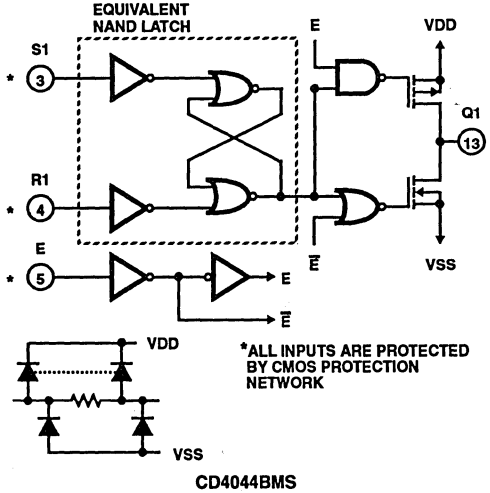


CD4044BMS

Logic Diagram



CD4043BMS



CD4044BMS

TRUTH TABLE

CD4043BMS

S	R	E	Q
X	X	O	OC*
O	O	1	NC**
1	O	1	1
O	1	1	O
1	1	1	Δ

* Open Circuit

** No Change

Δ Dominated by S = 1 input

CD4044BMS

S	R	E	Q
X	X	O	OC*
1	1	1	NC**
O	1	1	1
1	O	1	O
O	O	1	ΔΔ

* Open Circuit

** No Change

ΔΔ Dominated by R = O input

Typical Performance Characteristics

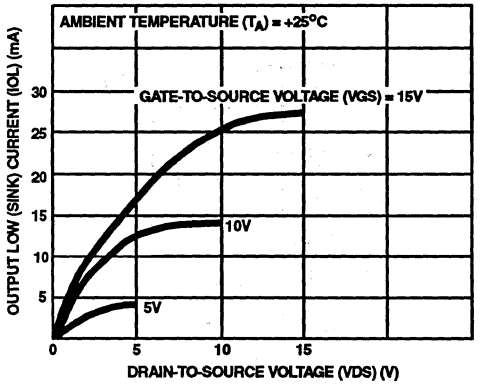


FIGURE 1. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

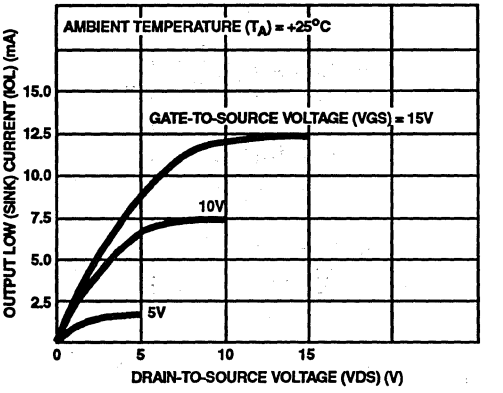


FIGURE 2. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

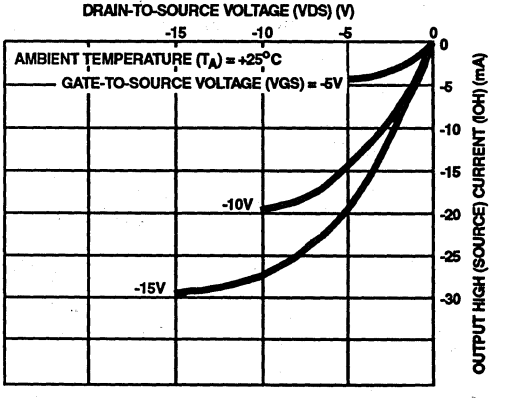


FIGURE 3. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

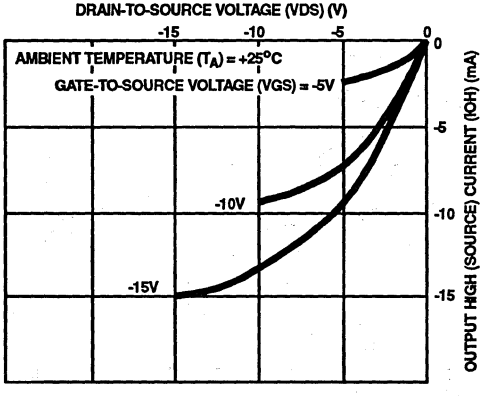


FIGURE 4. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

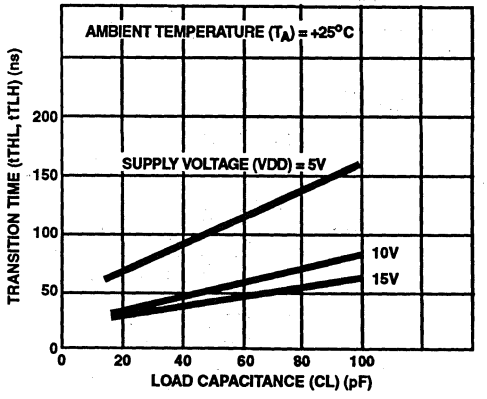


FIGURE 5. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

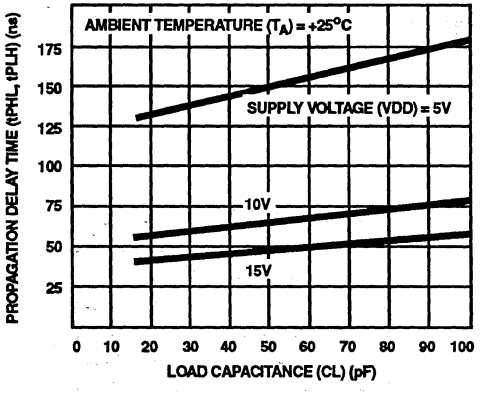


FIGURE 6. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE - SET, RESET, to Q, $\overline{Q}$

Typical Performance Characteristics (Continued)

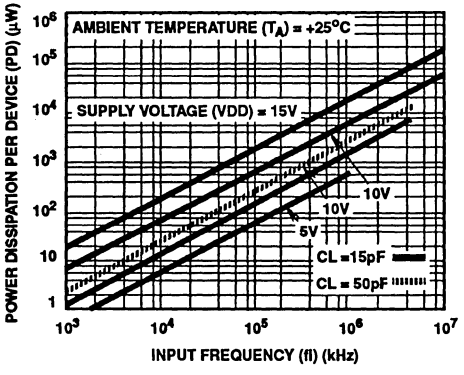


FIGURE 7. TYPICAL POWER DISSIPATION vs FREQUENCY

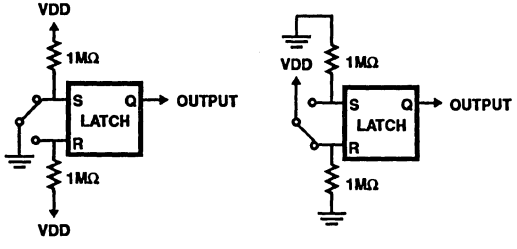


FIGURE 8. SWITCH BOUNCE ELIMINATOR

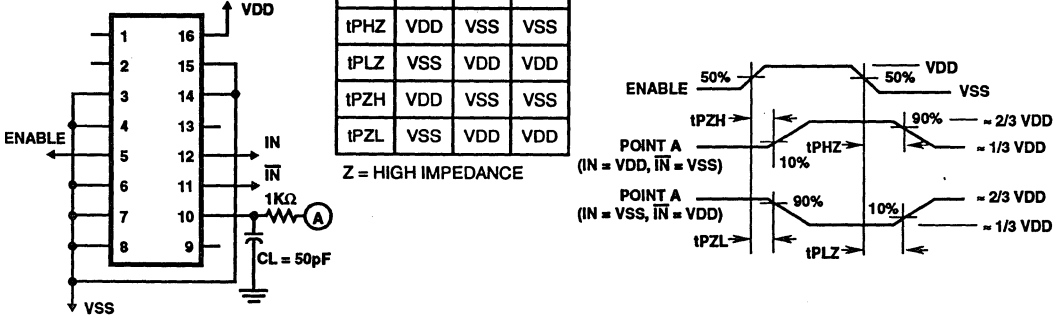


FIGURE 9. ENABLE PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORM

7 LOGIC

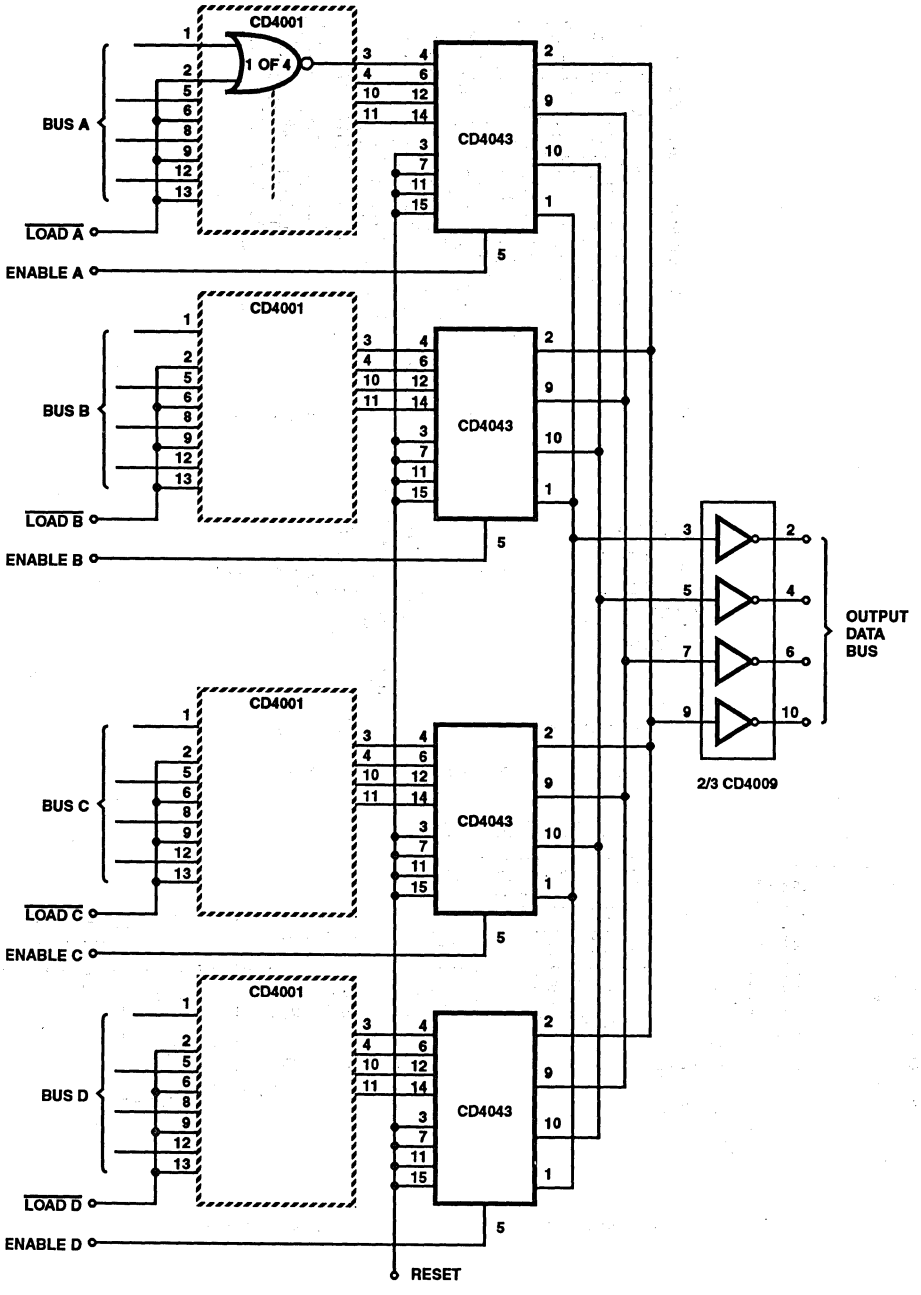
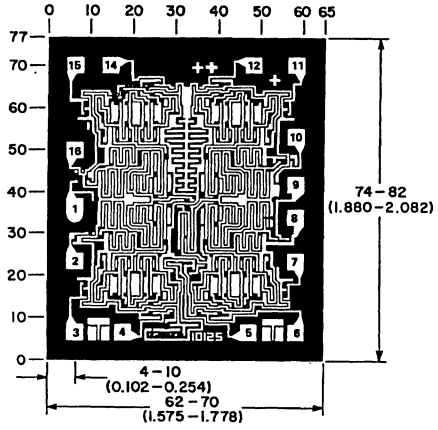


FIGURE 10. MULTIPLE BUS STORAGE

Chip Dimensions and Pad Layouts



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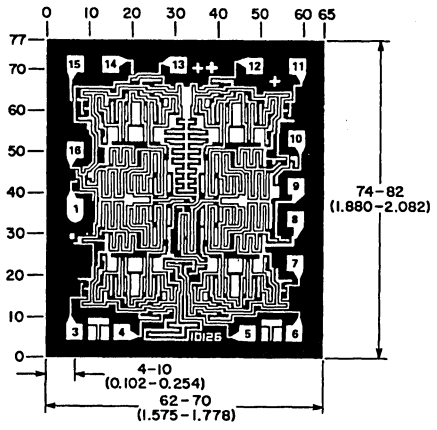


CD4044BMSH

Dimensions in parentheses are in millimeters
and are derived from the basic inch dimensions
as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4046BMS

December 1992

CMOS Micropower Phase Locked Loop

Features

- Very Low Power Consumption: 70μW (typ.) at VCO fo = 10kHz, VDD = 5V
- Operating Frequency Range Up to 1.4 MHz (typ.) at VDD = 10V, RI = 5kΩ
- Low Frequency Drift: 0.04%/°C (typ.) at VDD = 10V
- Choice of Two Phase Comparators:
  - Exclusive-OR Network (I)
  - Edge-Controlled Memory Network with Phase-Pulse Output for Lock Indication (II)
- High VCO Linearity: <1% (typ.) at VDD = 10V
- VCO Inhibit Control for ON-OFF Keying and Ultra-Low Standby Power Consumption
- Source-Follower Output of VCO Control Input (Demod. Output)
- Zener Diode to Assist Supply Regulation
- Standardize, Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- FM Demodulator and Modulator
- Frequency Synthesis and Multiplication
- Frequency Discriminator
- Data Synchronization
- Voltage-to-Frequency Conversion
- Tone Decoding
- FSK - Modems
- Signal Conditioning

Description

CD4046BMS CMOS Micropower Phase-Locked Loop (PLL) consists of a low power linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2V zener diode is provided for supply regulation if necessary.

The CD4046BMS is supplied in these 16-lead outline packages:

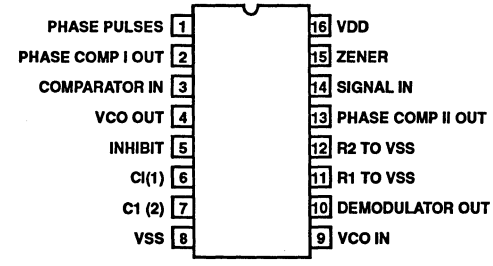
Braze Seal DIP	H4W
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

VCO Section

The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{12\Omega}$) of the VCO simplifies the design of low pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor (RS) of 10kΩ or more should be connected from this terminal to VSS. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full CMOS logic swing is available at the output of the VCO and allows direct coupling to CMOS frequency dividers such as the Harris CD4024, CD4018, CD4020, CD4029, and CD4050. One or more CD4018 (Preset Table Divide-By-N Counter) or CD4029 (Presettable Up/Down Counter) or CD4029 (Presettable Divide-by-N Counter) or CD4029 (Presettable Up/Down Counter), or CD4059A (Programmable Divide-by "N" Counter), together with the CD4046BMS (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

Pinout

CD4046BMS
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3312

Phase Comparators

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within CMOS logic levels (logic "0" ≤30% (VDD-VSS). logic "1" ≥70% (VDD - VSS)]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input.

Phase-comparator I is an exclusive -OR network; it operates analogously to an overdriven balanced mixer. To maximize the lock range, the signal and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to VDD/2. The low-pass filter connected to the output of phase-comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_o).

The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range (2fc).

The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range (2fL). The capture range is ≤ the lock range.

With phase-comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Figure 1 shows the typical, triangular, phase-to-output response characteristic of phase comparator I. Typical waveforms for a CMOS phase-locked-loop employing phase comparator I in locked condition of f_o is shown in Figure 2.

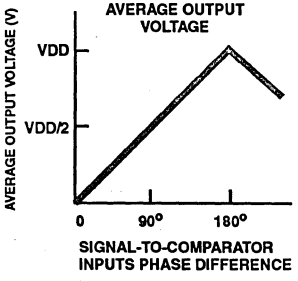


FIGURE 1. PHASE-COMPARATOR I CHARACTERISTICS AT LOW-PASS FILTER OUTPUT

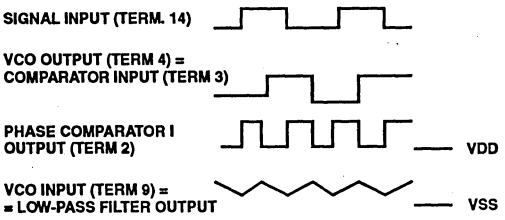


FIGURE 2. TYPICAL WAVEFORMS FOR CMOS PHASE-LOCKED LOOP EMPLOYING PHASE COMPARATOR IN LOCKED CONDITION OF f_o.

Phase comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-state output circuit comprising p- and n- type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to VDD or down to VSS, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3 state) the remainder of the time. If the signal and comparator input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase differences. If the signal and comparator-input frequencies are the same, but the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p- and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Figure 15 shows typical waveforms for a CMOS PLL employing phase comparator II in a locked condition.

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V
3 State Leakage Current	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
3 State Leakage Current	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Leakage Phase Comparator (Bias Amp Leakage)	BIAS LKG	VDD = 20V, VIN = VDD or GND PIN 14 Open Pin 5 = VDD	1	+25°C	-	4	mA
			3	-55°C	-	4	mA
		VDD = 20V, VIN = VDD or GND PIN 14 = VSS or VDD Pin 5 = VDD	1	+25°C	-	160	µA
			3	-55°C	-	160	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
AC Coupled Signal Input Voltage Sensitivity (Peak to Peak)	VS	VDD = 5V, Input Frequency = 100kHz Sine Wave	9	+25°C	-	360	mV

NOTES:
1. Go/No Go test with limits applied to inputs.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS		NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Leakage Phase Comparator (Bias Amp Leakage)	BIAS LKG	VDD = 5 VIN = VDD or GND	Pin 14 Open Pin 5 = VDD	1, 2	+25°C/-55°C	-	0.2	mA
			Pin 14 = VSS or VDD Pin 5 = VDD	1, 2	+25°C/-55°C	-	20	µA
		VDD = 10 VIN = VDD or GND	Pin 14 Open Pin 5 = VDD	1, 2	+25°C/-55°C	-	1.0	mA
			Pin 14 = VSS or VDD Pin 5 = VDD	1, 2	+25°C/-55°C	-	40	µA
		VDD = 15 VIN = VDD or GND	Pin 14 Open Pin 5 = VDD	1, 2	+25°C/-55°C	-	1.5	mA
			Pin 14 = VSS or VDD Pin 5 = VDD	1, 2	+25°C/-55°C	-	80	µA
AC Coupled Signal Input Voltage Sensitivity (Peak to Peak)	VS	VDD = 10V, Input Frequency = 100kHz Sine Wave		1, 2	+25°C	-	660	mV
		VDD = 15V, Input Frequency = 100kHz Sine Wave		1, 2	+25°C	-	1800	mV

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
AC Coupled Signal Input Voltage Sensitivity	VS	VDD = 5V Input Frequency = 100kHz Sine Wave	1, 2, 3	+25°C	-	1.35 x +25°C Limit	mV

NOTES:

1. All voltages referenced to device GND.
2. Go/No Go test with limits applied to inputs.
3. See Table 2 for +25°C limit.

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	1, 2, 4, 6, 7, 10, 11, 13, 15	3, 5, 8, 9, 14	12, 16			
Static Burn-In 2 Note 1	1, 2, 4, 6, 7, 10, 11, 13, 15	8	3, 5, 9, 12, 14, 16			
Dynamic Burn-In Note 1	1, 2, 4, 6, 7, 10, 11, 13, 15	8, 9	3, 5, 12, 16	2	14	-
Irradiation Note 2	1, 2, 4, 6, 7, 10, 11, 13, 15	8	3, 5, 9, 12, 14, 16			

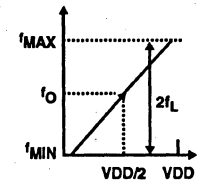
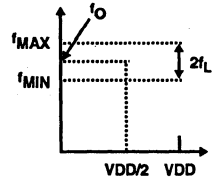
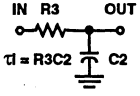
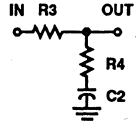
NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Design Information

This information is a guide for approximating the values of external components for the CD4046BMS in a Phase-Locked-Loop system. The selected external components must be within the following ranges:

$5k\Omega \leq R1, R2, RS \leq 1M\Omega$ $\quad C1 \geq 100pF$ at $VDD \geq 5V$ $\quad C1 \geq 50pF$ at $VDD \geq 10V$

CHARACTERISTICS	PHASE COMPARATOR USED	DESIGN INFORMATION
VCO Frequency	1	VCO Without Offset R2 = ∞  VCO INPUT VOLTAGE / VCO With Offset  VCO INPUT VOLTAGE
	2	Same as for Number 1
For Number Signal Input	1	VCO will adjust to center frequency, fo
	2	VCO will adjust to lowest operating frequency, fmin
Frequency Lock Range, 2fL	1, 2	2fL = full VCO frequency range
	1, 2	2fL = fmax - fmin
Frequency Capture Range, 2fC	1	 $\tau 1 = R3C2$ (1), (2) $2fC \approx \frac{1}{\pi}\sqrt{\frac{2\pi fL}{\tau 1}}$
Loop Filter Component Selection		 For 2 fC, see Ref. (2)
	2	fC = fL
Phase Angle Between Signal and Comparator	1	90° at center frequency (fo) approximating 0° and 180° at ends of lock range (2fL)
	2	Always 0° in lock
Locks On Harmonic of Center Frequency	1	Yes
	2	No
Signal Input Noise Rejection	1	High
	2	Low

For further information, see

(1) F. Gardner, "Phase-Lock Techniques" John Wiley and Sons, New York 1966
(2) G. S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965

Block Diagram

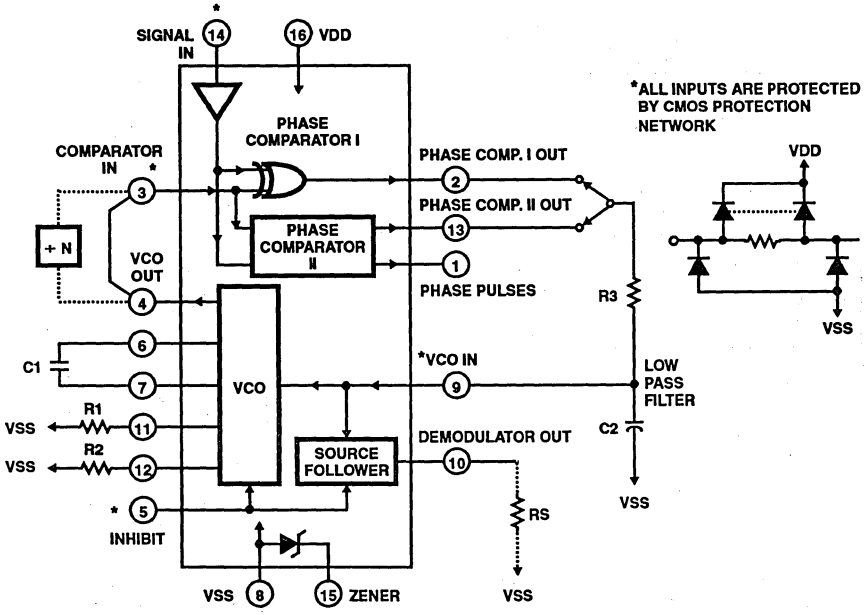
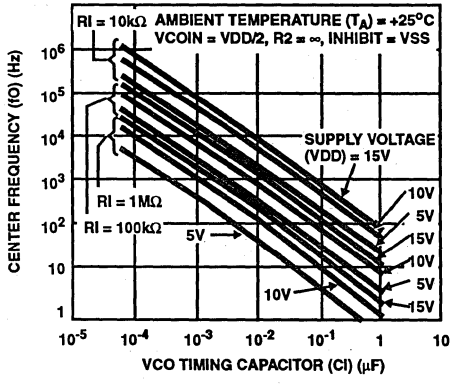


FIGURE 3. CMOS PHASE-LOCKED LOOP BLOCK DIAGRAM

Typical Performance Characteristics



TYPICAL CENTER FREQUENCY UNIT-TO-UNIT VARIATION

VDD (V)	Δf/fO (%)
5	±50
10	±30
15	±35

FIGURE 4. TYPICAL CENTER FREQUENCY AS A FUNCTION OF C1 AND R1 AT VDD = 5V, 10V, AND 15V

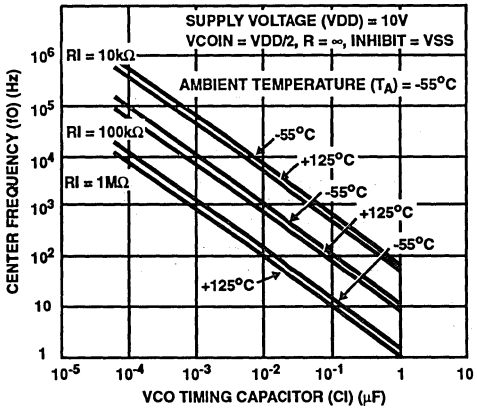


FIGURE 5. CENTER FREQUENCY AS A FUNCTION OF C1 AND R1 FOR AMBIENT TEMPERATURE OF -55°C to +125°C

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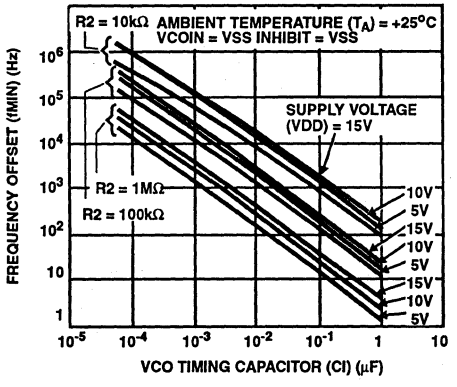
Typical Performance Characteristics (Continued)



TYPICAL fMIN UNIT-TO-UNIT VARIATION

VDD (V)	ΔfMIN/fMIN (%)
5	±25
10	±20
15	±25

FIGURE 6. TYPICAL FREQUENCY OFFSET AS A FUNCTION OF C1 AND R2 FOR VDD = 5V, 10V, AND 15V

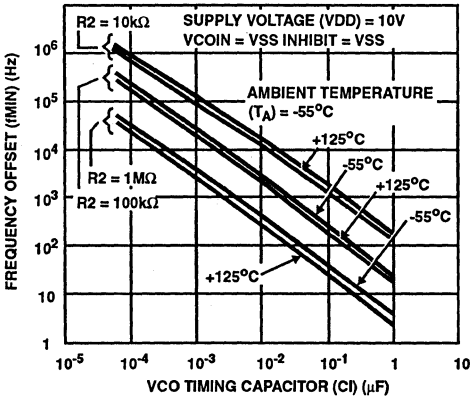
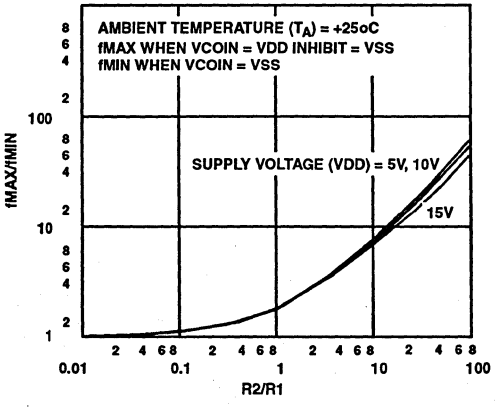


FIGURE 7. FREQUENCY OFFSET AS A FUNCTION OF C1 AND R2 FOR AMBIENT TEMPERATURES OF -55°C to 125°C



TYPICAL fMAX/fMIN UNIT-TO-UNIT VARIATION

VDD (V)	fMAX/fMIN (%)
5	±12
10	±8
15	±12

FIGURE 8. TYPICAL fMAX/fMIN AS A FUNCTION OF R2/R1

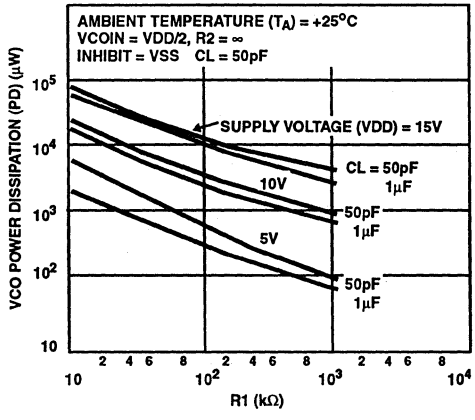


FIGURE 9. TYPICAL VCO POWER DISSIPATION AT CENTER FREQUENCY AS A FUNCTION OF R1

Typical Performance Characteristics (Continued)

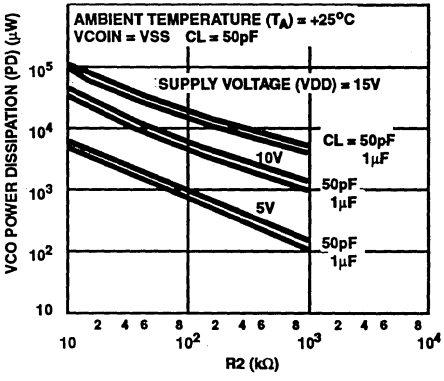


FIGURE 10. TYPICAL VCO POWER DISSIPATION AT fMIN AS A FUNCTION OF R2

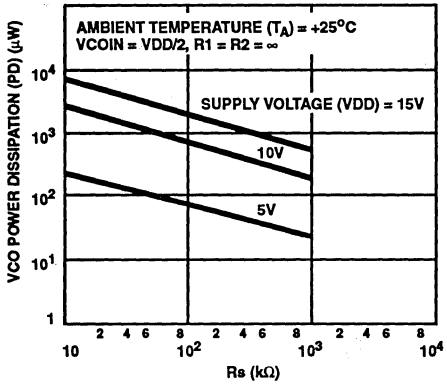


FIGURE 11. TYPICAL SOURCE FOLLOWER POWER DISSIPATION AS A FUNCTION OF RS

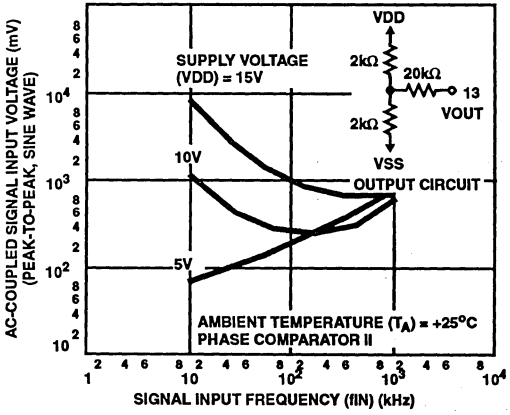


FIGURE 12. AC-COUPLED SIGNAL INPUT VOLTAGE AS A FUNCTION OF SIGNAL INPUT FREQUENCY

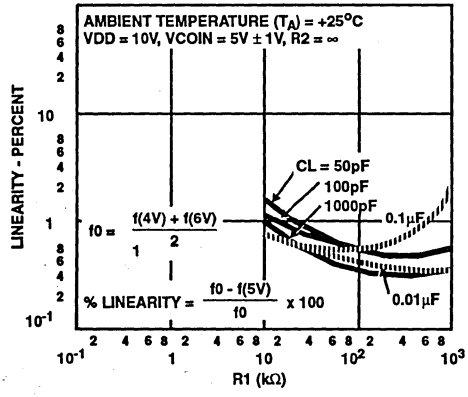


FIGURE 13. TYPICAL VCO LINEARITY AS A FUNCTION OF R1 AND C1 AT VDD = 10V

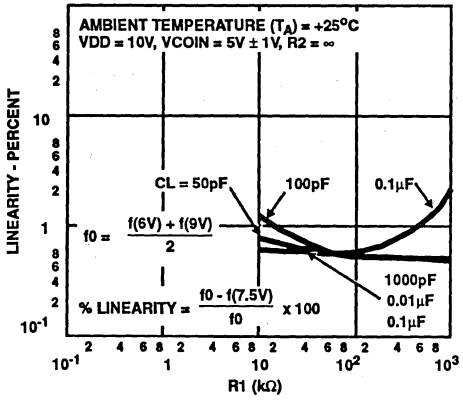


FIGURE 14. TYPICAL VCO LINEARITY AS A FUNCTION OF R1 AND C1 AT VDD = 15V

7 LOGIC

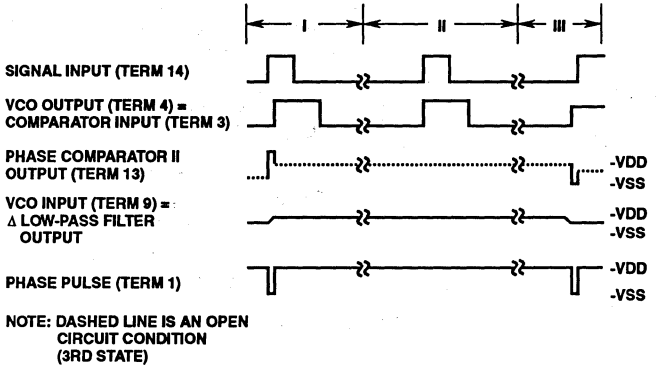


FIGURE 15. TYPICAL WAVEFORMS FOR COS/MOS PHASE-LOCKED LOOP EMPLOYING PHASE COMPARATOR II IN LOCKED CONDICTION

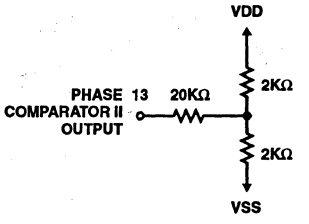
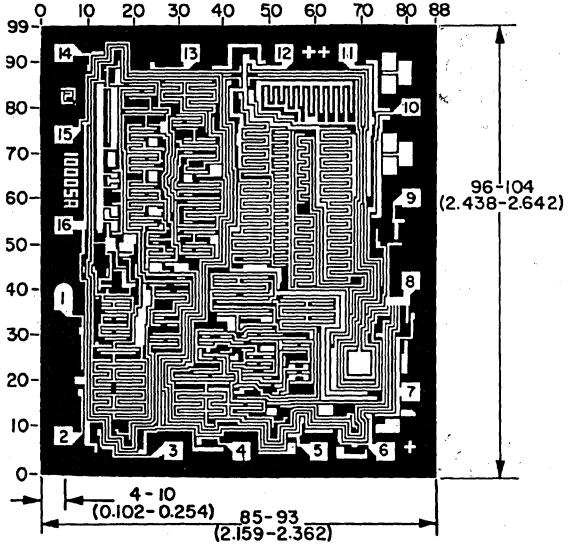


FIGURE 16. PHASE COMPARATOR II OUTPUT LOADING CIRCUIT

Chip Dimensions and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4047BMS

CMOS Low-Power Monostable/Astable Multivibrator

December 1992

Features

- High Voltage Type (20V Rating)
- Low Power Consumption: Special CMOS Oscillator Configuration
- Monostable (One-Shot) or Astable (Free-Running) Operation
- True and Complemented Buffered Outputs
- Only One External R and C Required
- Buffered Inputs
- 100% Tested for Quiescent Current at 20V
- Standardized, Symmetrical Output Characteristics
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Monostable Multivibrator Features

- Positive or Negative Edge Trigger
- Output Pulse Width Independent of Trigger Pulse Duration
- Retriggerable Option for Pulse Width Expansion
- Internal Power-On Reset Circuit
- Long Pulse Widths Possible Using Small RC Components by Means of External Counter Provision
- Fast Recovery Time Essentially Independent of Pulse Width
- Pulse-Width Accuracy Maintained at Duty Cycles Approaching 100%

Astable Multivibrator Features

- Free-Running or Gatable Operating Modes
- 50% Duty Cycle
- Oscillator Output Available
- Good Astable Frequency Stability: Frequency Deviation:
  - = ±2% + 0.03%/°C at 100kHz
  - = ±0.5% + 0.015%/°C at 10kHz (Circuits "Trimmed" to Frequency VDD = 10V ± 10%

Applications

Digital equipment where low power dissipation and/or high noise immunity are primary design requirements

- Envelope Detection
- Frequency Discriminators
- Frequency Multiplication
- Timing Circuits
- Frequency Division
- Time Delay Applications

Description

CD4047BMS consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge triggered monostable multivibrator action with retriggering and external counting options.

Inputs include +TRIGGER, -TRIGGER, ASTABLE, $\overline{\text{ASTABLE}}$, RETRIGGER, and EXTERNAL RESET. Buffered outputs are Q, $\overline{Q}$, and OSCILLATOR. In all modes of operation, an external capacitor must be connected between C-Timing and RC-Common terminals, and an external resistor must be connected between the R-Timing and RC-Common terminals.

Astable operation is enabled by a high level on the ASTABLE input or a low level on the $\overline{\text{ASTABLE}}$ input, or both. The period of the square wave at the Q and $\overline{Q}$ Outputs in this mode of operation is a function of the external components employed. "True" input pulses on the ASTABLE input or "Complement" pulses on the $\overline{\text{ASTABLE}}$ input allow the circuit to be used as a gatable multivibrator. The OSCILLATOR output period will be half of the Q terminal output in the astable mode. However, a 50% duty cycle is not guaranteed at this output.

The CD4047BMS triggers in the monostable mode when a positive going edge occurs on the +TRIGGER input while the -TRIGGER is held low. Input pulses may be of any duration relative to the output pulse.

If retrigger capability is desired, the RETRIGGER input is pulsed. The retriggerable mode of operation is limited to positive going edge. The CD4047BMS will retrigger as long as the RETRIGGER input is high, with or without transitions (See Figure 31)

An external countdown option can be implemented by coupling "Q" to an external "N" counter and resetting the counter with trigger pulse. The counter output pulse is fed back to the $\overline{\text{ASTABLE}}$ input and has a duration equal to N times the period of the multivibrator.

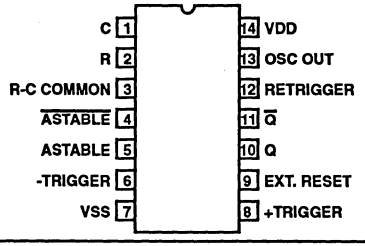
A high level on the EXTERNAL RESET input assures no output pulse during an "ON" power condition. This input can also be activated to terminate the output pulse at any time. For monostable operation, whenever VDD is applied, an internal power on reset circuit will clock the Q output low within one output period (tM).

The CD4047BMS is supplied in these 14-lead outline packages:

Braze Seal DIP	H4Q
Frit Seal DIP	H1B
Ceramic Flatpack	H3W

Pinout

CD4047BMS
TOP VIEW



7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3313

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs ..... -0.5V to VDD +0.5V
DC Input Current, Any One Input ..... ±10mA
Operating Temperature Range ..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Input Leakage Curent (Pin 3)	IIL	VDD = 24V, VIN = 11V or GND		1	+25°C	-300	-	nA
				2	+125°C	-10	-	µA
Input Leakage Current (Pin 3)	IIH	VDD = 26V, VIN = 13V or GND		1	+25°C	-	300	nA
				2	+125°C	-	10	µA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink) Q, $\overline{Q}$, OSC Out	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink) Q, $\overline{Q}$, OSC Out	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink) Q, $\overline{Q}$, OSC Out	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source) Q, $\overline{Q}$, OSC Out	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source) Q, $\overline{Q}$, OSC Out	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source) Q, $\overline{Q}$, OSC Out	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source) Q, $\overline{Q}$, OSC Out	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
Output Current (Sink)	IOL5RC	VDD = 5V, VOUT = 0.4V		1	+25°C	0.78	-	mA
Output Current (Sink)	IOL10RC	VDD = 10V, VOUT = 0.5V		1	+25°C	2.0	-	mA
Output Current (Sink)	IOL15RC	VDD = 15V, VOUT = 1.5V		1	+25°C	5.2	-	mA
Output Current (Source)	IOH5RC	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.78	mA
Output Current (Source)	IOH10RC	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-2	mA
Output Current (Source)	IOH15RC	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-5.2	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10μA	1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND	7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND	7	+25°C			
		VDD = 18V, VIN = VDD or GND	8A	+125°C			
		VDD = 3V, VIN = VDD or GND	8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V	1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V	1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V	1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V	1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES:

1. All voltages referenced to device GND, 100% testing being implemented
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max..

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Astable, $\overline{\text{Astable}}$ to OSC	TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay Trigger to Q, $\overline{Q}$	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	1000	ns
			10, 11	+125°C, -55°C	-	1350	ns
Propagation Delay (Note 2) $\overline{\text{Astable}}$ or Astable to Q, $\overline{Q}$	TPLH2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	700	ns
			10, 11	+125°C, -55°C	-	945	ns
Propagation Delay (Note 2) Retrigger to Q, $\overline{Q}$	TPHL4 TPLH4	VDD = 5V, VIN = VDD or GND	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Propagation Delay (Note 2) Reset to Q, $\overline{Q}$	TPLH5 TPLH5	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. VDD = 5V, CL = 50pF, RL = 200K; input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Astable, $\overline{\text{Astable}}$ to OSC	TPLH1	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	160	ns
Propagation Delay Astable or $\overline{\text{Astable}}$ to Q, $\overline{Q}$	TPLH2 TPHL2	VDD = 10V	1, 2, 3	+25°C	-	350	ns
		VDD = 15V	1, 2, 3	+25°C	-	250	ns
Propagation Delay Trigger to Q, $\overline{Q}$	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25°C	-	450	ns
		VDD = 15V	1, 2, 3	+25°C	-	300	ns
Propagation Delay Retrigger to Q, $\overline{Q}$	TPHL4 TPLH4	VDD = 10V	1, 2, 3	+25°C	-	300	ns
		VDD = 15V	1, 2, 3	+25°C	-	200	ns
Propagation Delay Reset to Q, $\overline{Q}$	TPLH5 TPHL5	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	140	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Q or $\overline{Q}$ Deviation from 50% Duty Factor	QD	VDD = 5V	1, 2, 3	+25°C	-	±1	%
		VDD = 10V	1, 2, 3	+25°C	-	±1	%
		VDD = 15V	1, 2, 3	+25°C	-	±0.5	%
Minimum Pulse Width + Trigger - Trigger	TW	VDD = 5V	1, 2, 3	+25°C	-	400	ns
		VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Minimum Pulse Width Reset	TW	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Minimum Retrigger Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	600	ns
		VDD = 10V	1, 2, 3	+25°C	-	230	ns
		VDD = 15V	1, 2, 3	+25°C	-	150	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.7	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	1, 2, 10, 11, 13	3-9, 12	14			
Static Burn-In 2 Note 1	1, 2, 10, 11, 13	7	3-6, 8, 9, 12, 14			
Dynamic Burn-In Note 1	-	7, 9, 12	4, 5, 14	1, 2, 10, 11, 13	6, 8	3
Irradiation Note 2	1, 2, 10, 11, 13	7	3-6, 8, 9, 12, 14			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

TABLE 9. FUNCTIONAL TERMINAL CONNECTIONS

In all cases External resistor between terminals 2 and 3 (Note 1)
External capacitor between terminals 1 and 3 (Note 1)

FUNCTION	TERMINAL CONNECTIONS			OUTPUT PULSE FROM	OUTPUT PERIOD OR PULSE WIDTH
	TO VDD	TO VSS	INPUT TO		
ASTABLE MULTIVIBRATOR					
Free Running	4, 5, 6, 14	7, 8, 9, 12	-	10, 11, 13	T_A (10, 11) = 4.40 RC
True Gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	T_A (13) = 2.20 RC (Note 2)
Complement Gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	
MONOSTABLE MULTIVIBRATOR					
Positive Edge Trigger	4, 14	5, 6, 7, 9, 12	8	10, 11	tM (10, 11) = 2.48 RC
Negative Edge Trigger	4, 8, 14	5, 7, 9, 12	6	10, 11	
Retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	
External Countdown (Note 3)	14	5, 6, 7, 8, 9, 12	-	10, 11	

NOTES:

1. See text.
2. First positive $^1/_2$ cycle pulse width = 2.48 RC. See note follow Monostable Mode Design Information.
3. Input Pulse to Reset of External Counting Chip External Counting Chip Output to Terminal 4.

Logic Diagrams

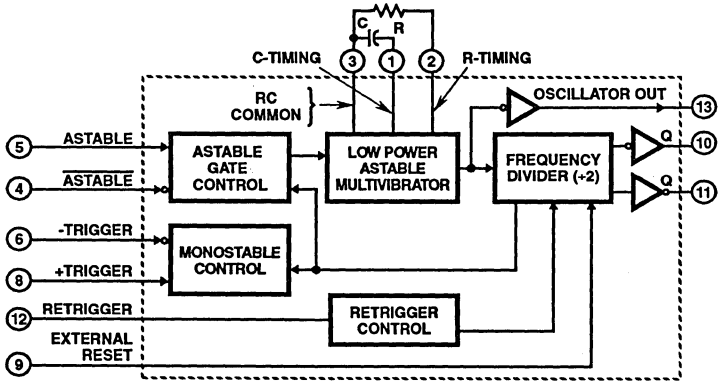


FIGURE 1. CD4047BMS LOGIC BLOCK DIAGRAM

Logic Diagrams (Continued)

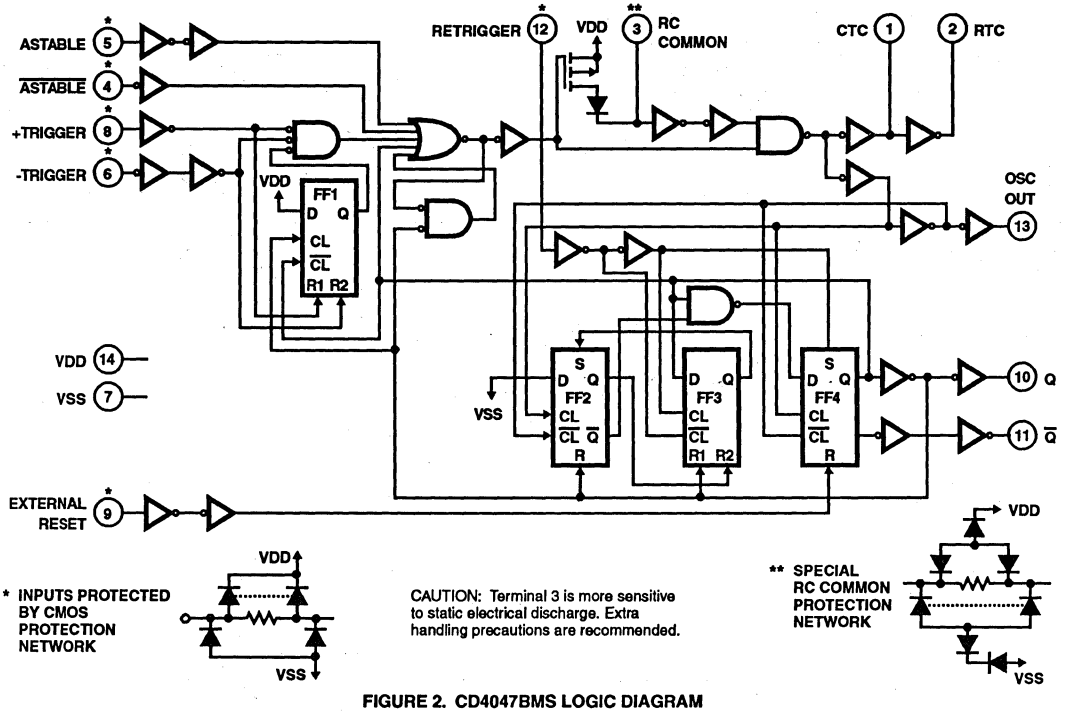


FIGURE 2. CD4047BMS LOGIC DIAGRAM

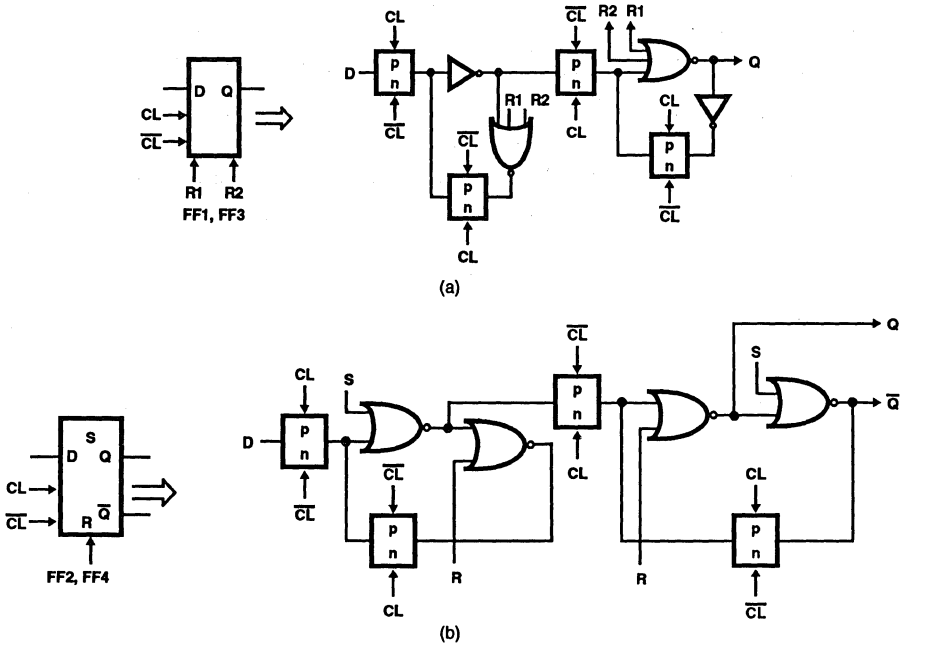


FIGURE 3. DETAIL LOGIC DIAGRAM FOR FLIP-FLOPS FF1 AND FF3 (a) AND FOR FLIP-FLOPS FF2 AND FF4 (b)

Typical Performance Characteristics

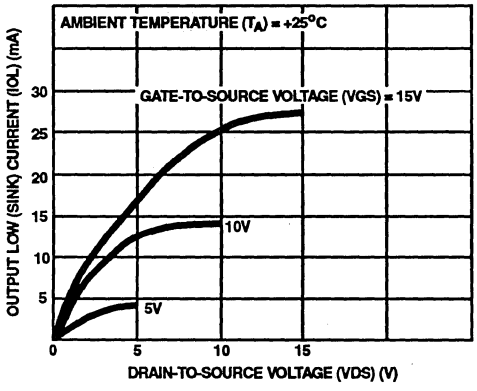


FIGURE 4. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

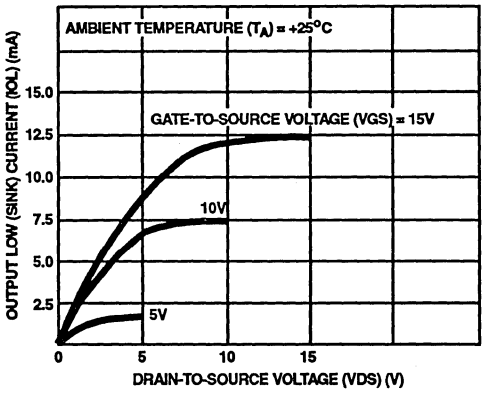


FIGURE 5. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

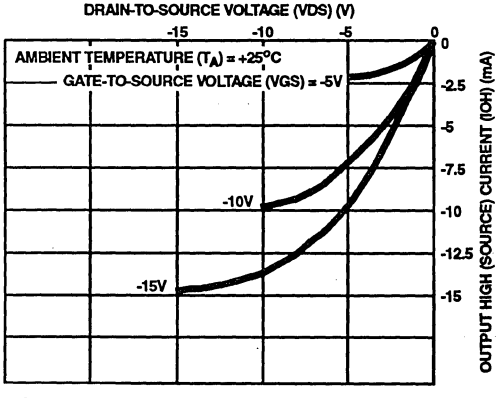


FIGURE 6. TYP. OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

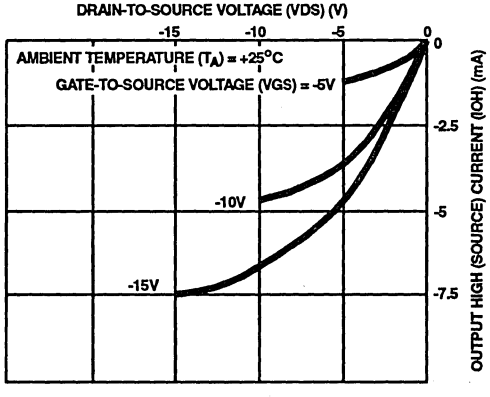


FIGURE 7. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

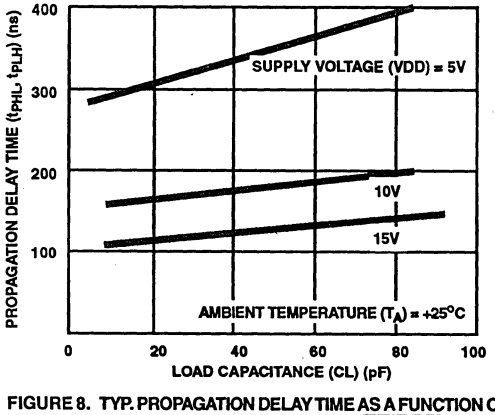


FIGURE 8. TYP. PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (ASTABLE, $\overline{\text{ASTABLE}}$ TO Q, $\overline{Q}$)

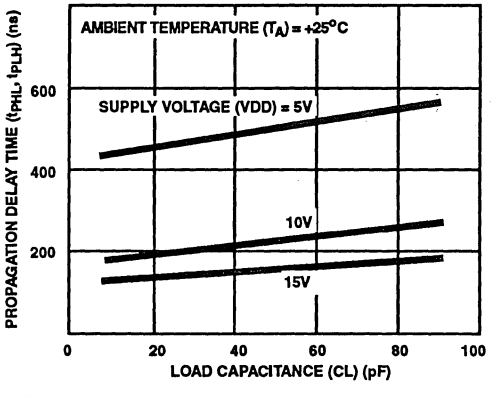


FIGURE 9. TYP. PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (+ OR - TRIGGER TO Q, $\overline{Q}$)

Typical Performance Characteristics (Continued)

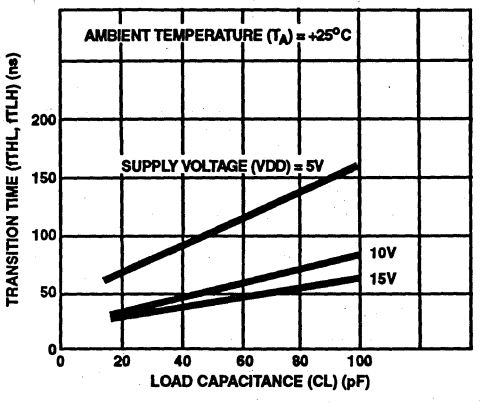


FIGURE 10. TYP. TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

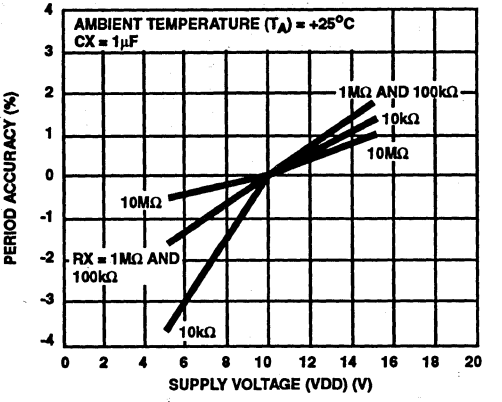


FIGURE 11. TYP. ASTABLE OSCILLATOR OR Q, $\overline{Q}$ PERIOD ACCURACY vs SUPPLY VOLTAGE

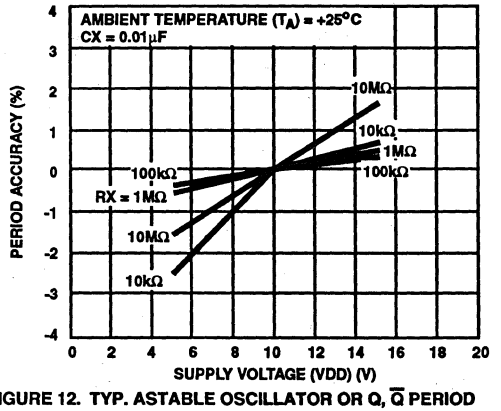


FIGURE 12. TYP. ASTABLE OSCILLATOR OR Q, $\overline{Q}$ PERIOD ACCURACY vs SUPPLY VOLTAGE

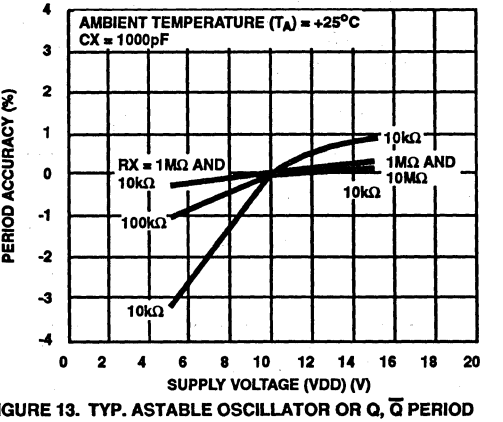


FIGURE 13. TYP. ASTABLE OSCILLATOR OR Q, $\overline{Q}$ PERIOD ACCURACY vs SUPPLY VOLTAGE

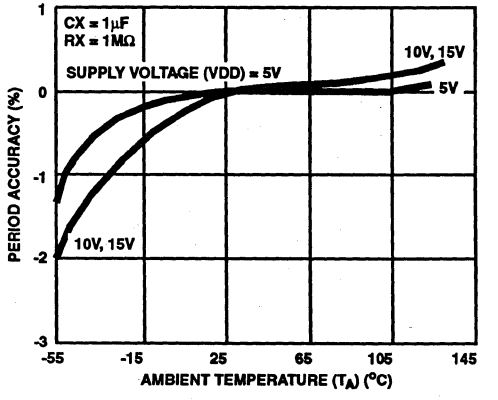


FIGURE 14. TYP. ASTABLE OSCILLATOR OR Q, Q PERIOD ACCURACY vs AMBIENT TEMPERATURE (ULTRA LOW FREQ.)

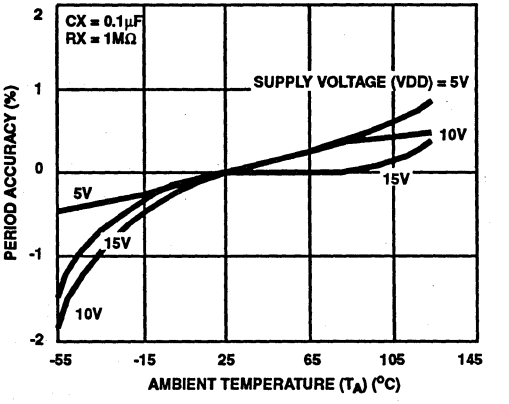


FIGURE 15. TYP. ASTABLE OSCILLATOR OR Q, Q PERIOD ACCURACY vs AMBIENT TEMPERATURE (LOW FREQ.)

Typical Performance Characteristics (Continued)

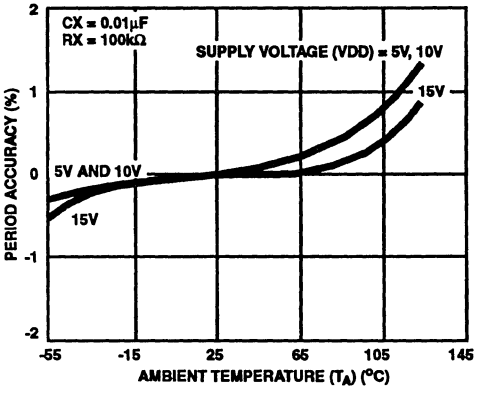


FIGURE 16. TYP. ASTABLE OSCILLATOR OR Q, $\overline{Q}$ PERIOD ACCURACY vs AMBIENT TEMPERATURE (MEDIUM FREQ.)

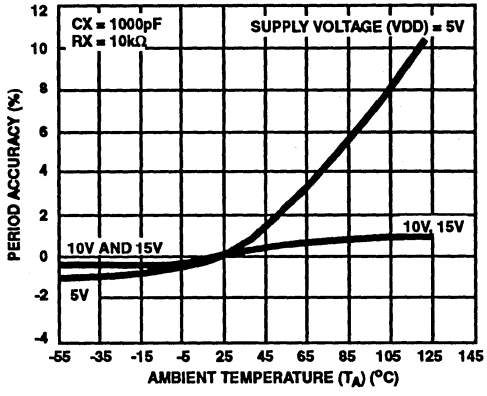


FIGURE 17. TYP. ASTABLE OSCILLATOR OR Q, $\overline{Q}$ PERIOD ACCURACY vs AMBIENT TEMPERATURE (HIGH FREQ.)

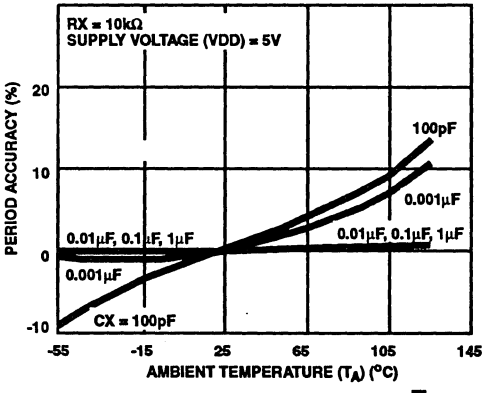


FIGURE 18. TYPICAL ASTABLE OSCILLATOR OR Q, $\overline{Q}$ PERIOD ACCURACY vs AMBIENT TEMPERATURE

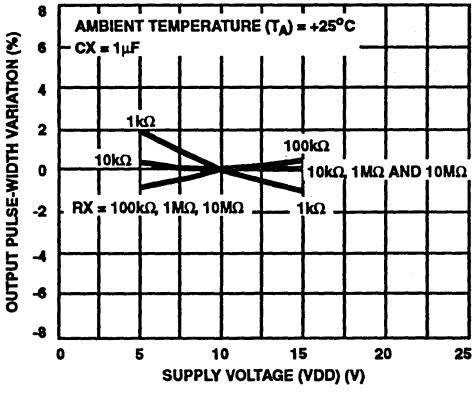


FIGURE 19. TYPICAL OUTPUT PULSE WIDTH VARIATIONS vs SUPPLY VOLTAGE

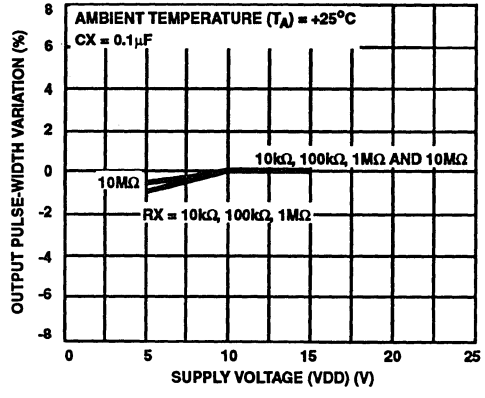


FIGURE 20. TYPICAL OUTPUT PULSE WIDTH VARIATIONS vs SUPPLY VOLTAGE

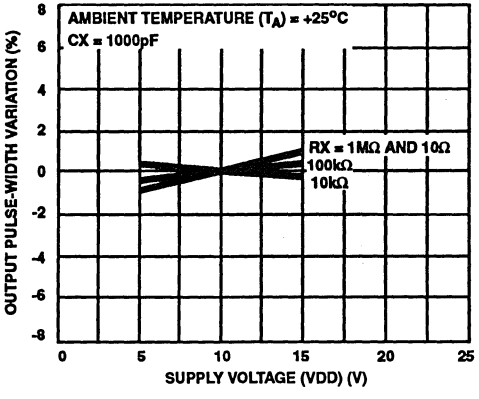


FIGURE 21. TYPICAL OUTPUT PULSE WIDTH VARIATIONS vs SUPPLY VOLTAGE

7 LOGIC

Typical Performance Characteristics (Continued)

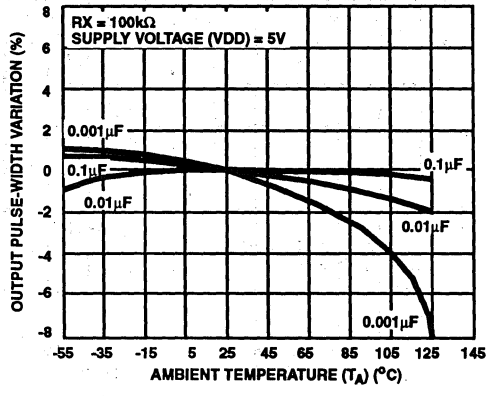


FIGURE 22. TYPICAL OUTPUT PULSE WIDTH VARIATIONS vs AMBIENT TEMPERATURE

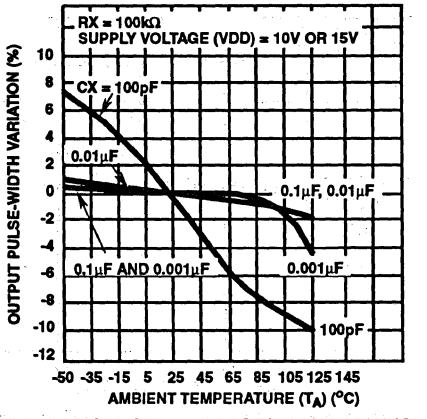


FIGURE 23. TYPICAL OUTPUT PULSE WIDTH VARIATIONS vs AMBIENT TEMPERATURE

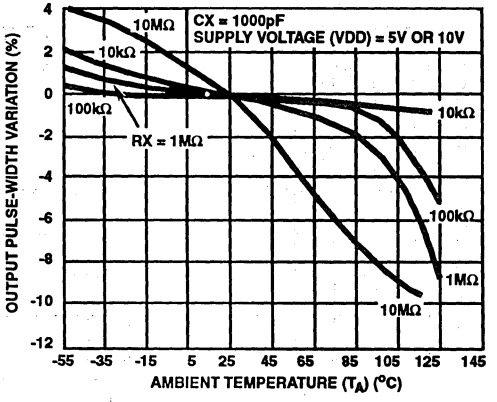


FIGURE 24. TYPICAL OUTPUT PULSE WIDTH VARIATIONS vs AMBIENT TEMPERATURE

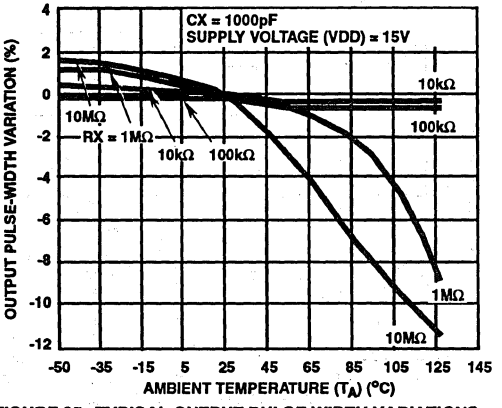


FIGURE 25. TYPICAL OUTPUT PULSE WIDTH VARIATIONS vs AMBIENT TEMPERATURE

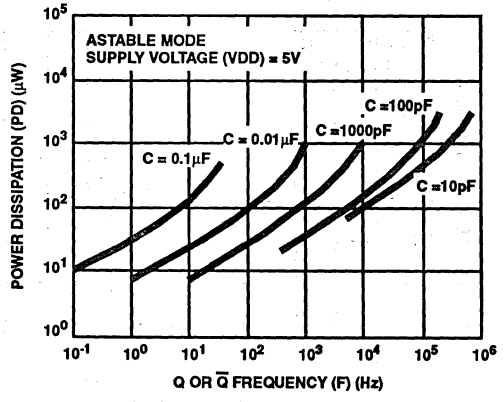


FIGURE 26. TYPICAL POWER DISSIPATION vs OUTPUT FREQUENCY (VDD = 5V)

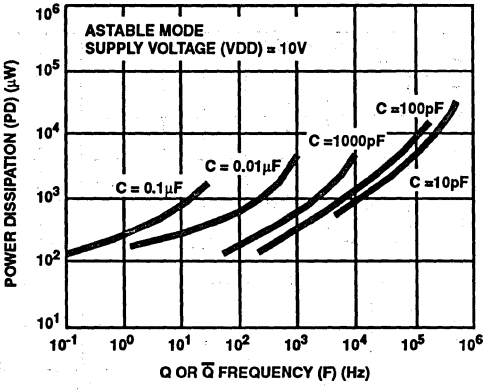


FIGURE 27. TYPICAL POWER DISSIPATION vs OUTPUT FREQUENCY (VDD = 10V)

Typical Performance Characteristics (Continued)

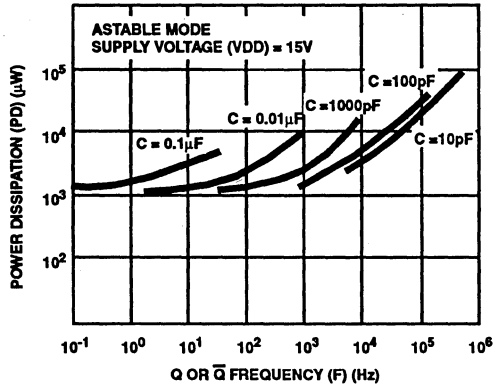


FIGURE 28. TYPICAL POWER DISSIPATION vs OUTPUT FREQUENCY (VDD = 15V)

Astable Mode Design Information

Unit-to-Unit Transfer Voltage Variations

The following analysis presents variations from unit to unit as a function of transfer voltage (VTR) shift (33%-67% VDD) for free running (astable) operation.

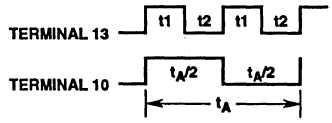


FIGURE 29. ASTABLE MODE WAVEFORMS

$$t1 = -RC \ln \frac{VTR}{VDD + VTR};$$

typically, $t1 = 1.1RC$

$$t2 = -RC \ln \frac{VDD - VTR}{2VDD - VTR};$$

typically, $t2 = 1.1RC$

$$t_A = 2(t1 + t2)$$

$$= -2RC \ln \frac{(VTR)(VDD - VTR)}{(VDD + VTR)(2VDD - VTR)}$$

Typ:	VTR = 0.5VDD	$t_A = 4.40RC$
Min:	VTR = 0.33VDD	$t_A = 4.62RC$
Max:	VTR = 0.67VDD	$t_A = 4.62RC$

thus if $\boxed{t_A = 4.40RC}$ is used, the variation will be +5%, -0% due to variations in transfer voltage.

Variations Due to VDD and Temperature Changes

In addition to variations from unit to unit, the astable period varies with VDD and temperature, Typical variations are presented in graphical form in Figures 11 to 18 with 10V as reference for voltage variations curves and +25°C as reference for temperature variations curves.

Monostable Mode Design Information

The following analysis presents variations from unit to unit as a function of transfer voltage (VTR) shift (33% - 67% VDD) for one shot (monostable) operation.

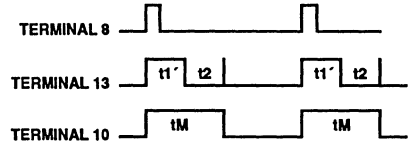


FIGURE 30. MONOSTABLE WAVEFORMS

$$t1' = -RC \ln \frac{VTR}{2VDD};$$

typically, $t1' = 1.38RC$

$$tM = (t1' + t2)$$

$$tM = -RC \ln \frac{(VTR)(VDD - VTR)}{(2VDD - VTR)(2VDD)}$$

where tM = Monostable mode pulse width.
Values for tM are as follows:

Typ:	VTR = 0.5VDD	tM = 2.48RC
Min:	VTR = 0.33VDD	tM = 2.71RC
Max:	VTR = 0.67VDD	tM = 2.48RC

thus if $\boxed{tM = 2.48RC}$ is used, the variation will be +9.3%, -0% due to variations in transfer voltage.

NOTES:

1. In the astable mode, the first positive half cycle has a duration of tM; succeeding durations are t_A/s.
2. In addition to variations from unit to unit, the monostable pulse width varies with VDD and temperature. These variations are presented in graphical form in Figures 19 to 26 with 10V as reference for voltage variation curves and +25°C as reference for temperature variation curves.

Retrigger Mode Operation

The CD4047BMS can be used in the retrigger mode to extend the output pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to terminal 12, and the output is taken from terminal 10 or 11. As shown in Figure 31 normal monostable action is obtained when one retrigger pulse is applied. Extended pulse duration is obtained when more than one pulse is applied.

For two input pulses, tRE = t1′ + t1 + 2t2. For more than two pulses, the output pulse width is an integral number of time periods, with the first time period being t1′ + t2, typically, 2.48RC, and all subsequent time periods being t1 + t2, typically, 2.2RC.

External Counter Option

Time tM can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time. A typical implementation is shown in Figure 32. The pulse duration at the output is

$$text = (N - 1)(t_A) + (tM + t_A/2)$$

where text = pulse duration of the circuitry, and N is the number of counts used.

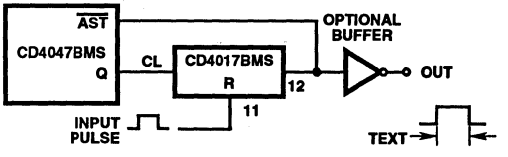


FIGURE 32. IMPLEMENTATION OF EXTERNAL COUNTER OPTION

Timing Component Limitations

The capacitor used in the circuit should be non polarized and have low leakage (i.e. the parallel resistance of the capacitor should be at least an order of magnitude greater than the external resistor used). There is no upper or lower limit for either R or C value to maintain oscillation.

However, in consideration of accuracy, C must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account). R must be much larger than the CMOS "ON" resistance in series with it, which typically is hundreds of Ω. In addition, with very large values of R, some short term instability with respect to time may be noted.

The recommended values for these components to maintain agreement with previously calculated formulas without trimming should be:

C ≥ 100pF, up to any practical value, for astable modes;

C ≥ 1000pF, up to any practical value for monostable modes.

10kΩ ≤ R ≤ 1MΩ

Power Consumption

In the standby mode (Monostable or Astable), power dissipation will be a function of leakage current in the circuit, as shown in the static electrical characteristics. For dynamic operation, the power needed to charge the external timing capacitor C is given by the following formula:

Astable Mode:

$P = 2CV^2f$. (Output at terminal No. 13)

$P = 4CV^2f$. (Output at terminal Nos. 10 and 11)

Monostable Mode:

$$P = \frac{(2.9CV^2)\ (\text{Duty Cycle})}{T}$$

(Output at terminal Nos. 10 to 11)

The circuit is designed so that most of the total power is consumed in the external components. In practice, the lower the values of frequency and voltage used, the closer the actual power dissipation will be to the calculated value.

Because the power dissipation does not depend on R, a design for minimum power dissipation would be a small value of C. The value of R would depend on the desired period (within the limitations discussed above). See Figures 26, 27, and 28 for typical power consumption in astable mode.

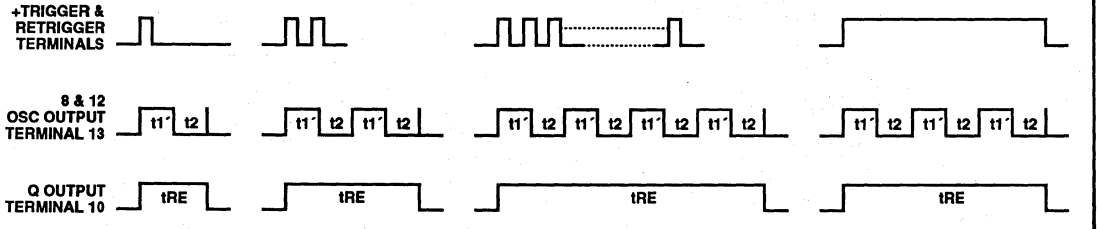
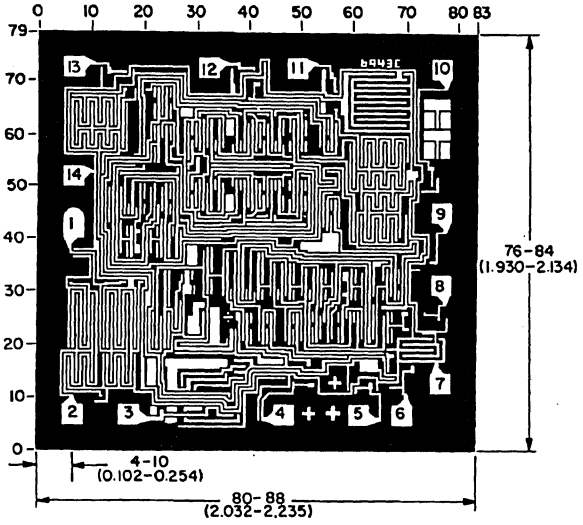


FIGURE 31. RETRIGGER MODE WAVEFORMS

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4048BMS

CMOS Multifunction Expandable 8 Input Gate

December 1992

Features

- High-Voltage Type (20V Rating)
- Three State Output
- Many Logic Functions Available in One Package
- Standardize, Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Selection of Up to 8 Logic Functions
- Digital Control of Logic
- General Purpose Gating Logic
  - Decoding
  - Encoding

Description

CD4048BMS is an 8-input gate having four control inputs. Three binary control inputs - Ka, Kb, and Kc - provide the implementation of eight different logic functions. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR and AND/NOR.

A fourth control input, Kd, provides the user with a 3-state output. When control input Kd is high, the output is either a logic 1 or a logic 0 depending on the inner states. When control input Kd is low, the output is an open circuit. This feature enables the user to connect this device to a common bus line.

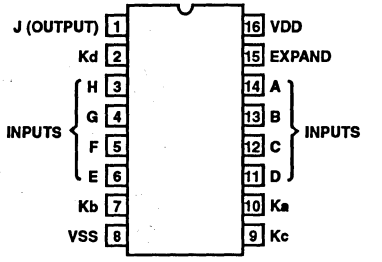
In addition to the eight input lines, an EXPAND input is provided that permits the user to increase the number of inputs into a CD4048BMS (see Figure 2). For example, two CD4048BMS's can be cascaded to provided a 16-input multifunction gate. When the EXPAND input is not used, it should be connected to VSS.

The CD4048BMS is supplied in these 16 lead outline packages:

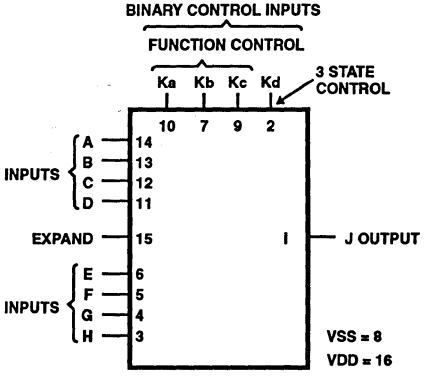
Braze Seal DIP	H4S
Frit Seal DIP	H1E
Ceramic Flatpack	H6W

Pinout

CD4048BMS
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3314**

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	0.5	µA
				2	+125°C	-	50	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	0.5	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.4	-	µA
				2	+125°C	-12	-	µA
			VDD = 18V	3	-55°C	-0.4	-	µA
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.4	µA
				2	+125°C	-	12	µA
			VDD = 18V	3	-55°C	-	0.4	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Ka to Output	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.25	µA
				+125°C	-	7.5	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	15	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	30	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Ka to Output	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	300	ns
		VDD = 15V	1, 2, 3	+25°C	-	240	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Inputs to Output	TPHL2 TPLH2	VDD = 5V	1, 2, 3	+25°C	-	600	ns
		VDD = 10V	1, 2, 3	+25°C	-	300	ns
		VDD = 15V	1, 2, 3	+25°C	-	240	ns
Propagation Delay Kb to Output	TPHL3 TPLH3	VDD = 5V	1, 2, 3	+25°C	-	450	ns
		VDD = 10V	1, 2, 3	+25°C	-	170	ns
		VDD = 15V	1, 2, 3	+25°C	-	110	ns
Propagation Delay Kc to Output	TPHL4 TPLH4	VDD = 5V	1, 2, 3	+25°C	-	280	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Propagation Delay Expand Input to Output	TPHL5 TPLH5	VDD = 5V	1, 2, 3	+25°C	-	380	ns
		VDD = 10V	1, 2, 3	+25°C	-	180	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Propagation Delay 3 State Kd to Output	TPHZ, LZ TPZH, ZL	VDD = 5V	1, 2, 4	+25°C	-	160	ns
		VDD = 10V	1, 2, 4	+25°C	-	70	ns
		VDD = 15V	1, 2, 4	+25°C	-	50	ns
Transition Time	TTLH TTHL	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7	pF
3 State Output Capacitance	CO		1, 2	+25°C	-	10	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - SSI	IDD	±0.1μA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	1	2 - 15	16			
Static Burn-In 2 Note 1	1	8	2 - 7, 9 - 16			
Dynamic Burn-In Note 1	-	8, 15	2, 16	1	9 - 14	3 - 7
Irradiation Note 2	1	8	2 - 7, 9 - 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%; VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagrams

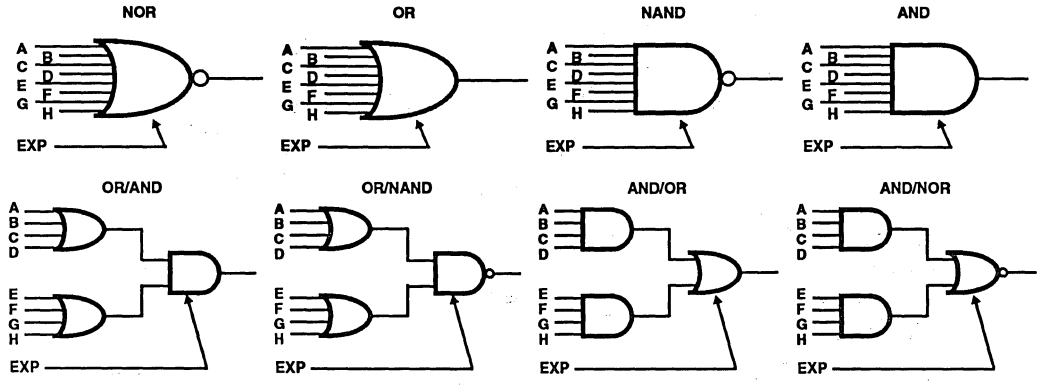


FIGURE 1. BASIC LOGIC CONFIGURATIONS

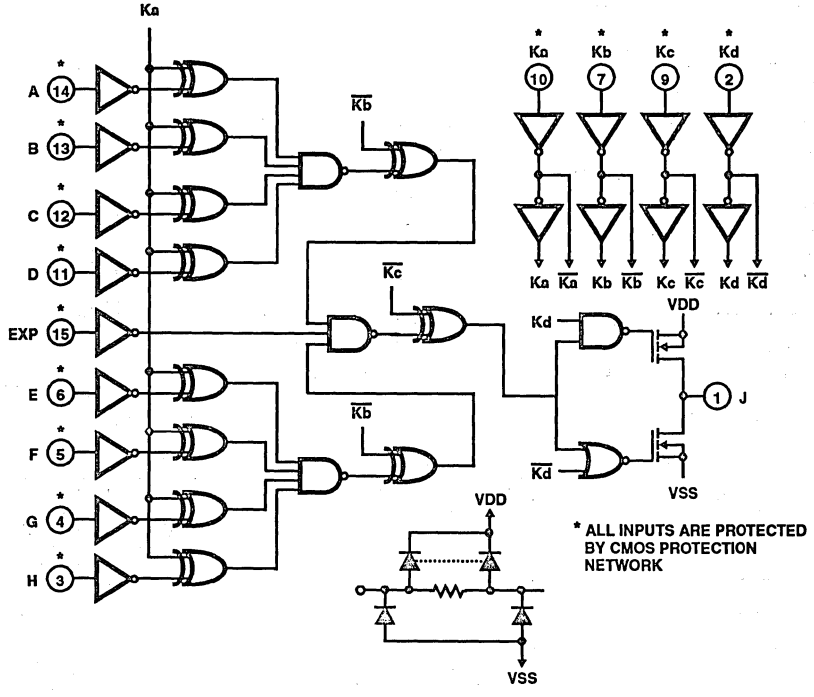


FIGURE 2. LOGIC DIAGRAM

Logic Diagrams (Continued)

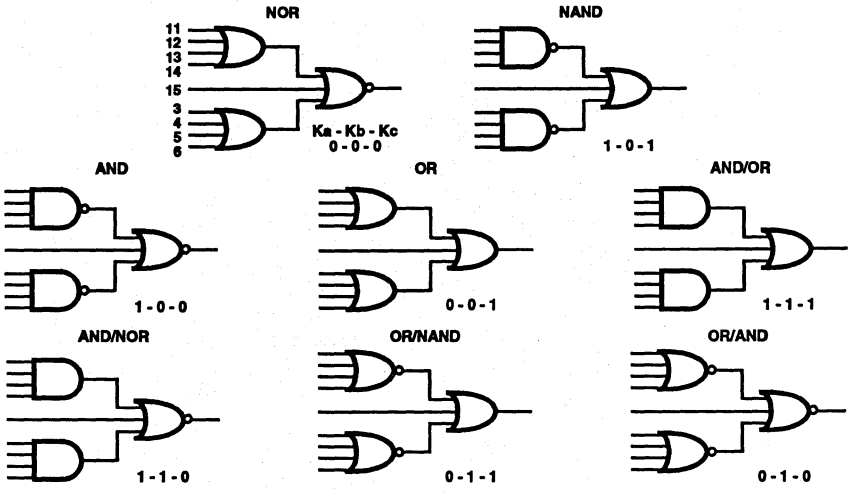


FIGURE 3. ACTUAL CIRCUIT LOGIC CONFIGURATIONS

Applications of Expand Input

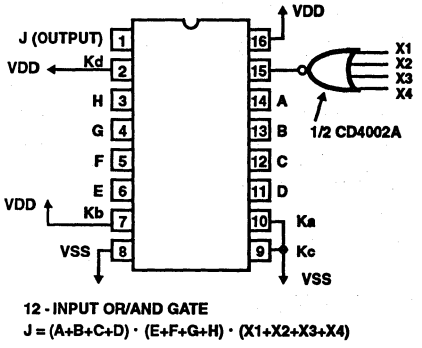


FIGURE 4. 12 INPUT OR/AND GATE

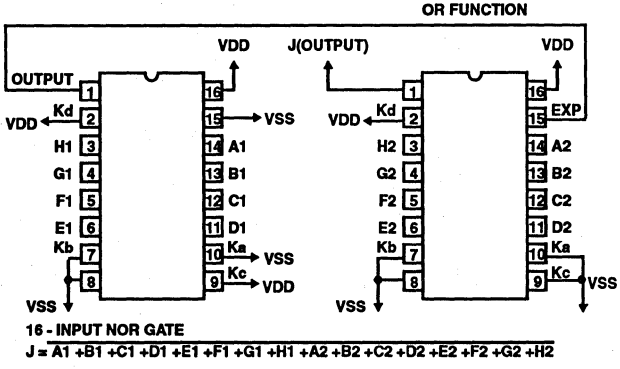


FIGURE 5. 16 INPUT NOR GATE

IMPLEMETATION OF EXPAND INPUT FOR 9 OR MORE INPUTS

OUTPUT FUNCTION	FUNCTION NEEDED AT EXPAND INPUT	OUTPUT BOOLEAN EXPRESSION
NOR	OR	$J=\overline{(A+B+C+D+E+F+G+H)+(EXP)}$
OR	OR	J=(A+B+C+D+E+F+G+H)+(EXP)
AND	NAND	$J=(ABCDEFGH)\bullet\overline{(EXP)}$
NAND	NAND	$J=\overline{(ABCDEFGH)\bullet\overline{(EXP)}}$
OR/AND	NOR	$J=(A+B+C+D)\bullet(E+F+G+H)\bullet\overline{(EXP)}$
OR/NAND	NOR	$J=(A+B+C+D)\bullet(E+F+G+H)\bullet\overline{(EXP)}$
AND/NOR	AND	$J=\overline{(ABCD)+(EFGH)+(EXP)}$
AND/OR	AND	J=(ABCD)+(EFGH)+(EXP)

NOTES: 1. (EXP) designates the EXPAND function (i.e., X1 + X2 + . . .XN).

2. Refer to FUNCTION TRUTH TABLE for connection of unused inputs.

FUNCTION TRUTH TABLE

OUTPUT FUNCTION	BOOLEAN EXPRESSION	Ka	Kb	Kc	UNUSED INPUT*
NOR	$J=\overline{A+B+C+D+E+F+G+H}$	0	0	0	VSS
OR	J=A+B+C+D+E+F+G+H	0	0	1	VSS
OR/AND	J=(A+B+C+D)•(E+F+G+H)	0	1	0	VSS
OR/NAND	$J=\overline{(A+B+C+D)\bullet(E+F+G+H)}$	0	1	1	VSS
AND	J=ABCDEFGH	1	0	0	VDD
NAND	$J=\overline{ABCDEFGH}$	1	0	1	VDD
AND/NOR	$J=\overline{ABCD+EFGH}$	1	1	0	VDD
AND/OR	J=ABCD+EFGH	1	1	1	VDD
Kd = 1 Normal Inverter Action Kd = 0 High Impedance Output					

EXPAND Input = 0

*See Figures 1, 2, 3, 4 and 5

Typical Performance Characteristics

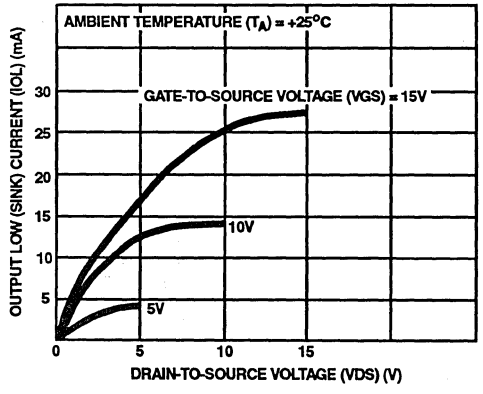


FIGURE 6. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

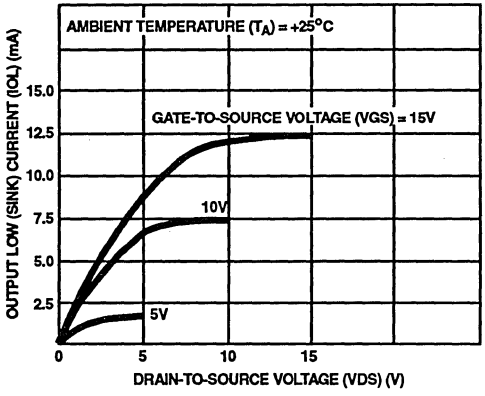


FIGURE 7. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

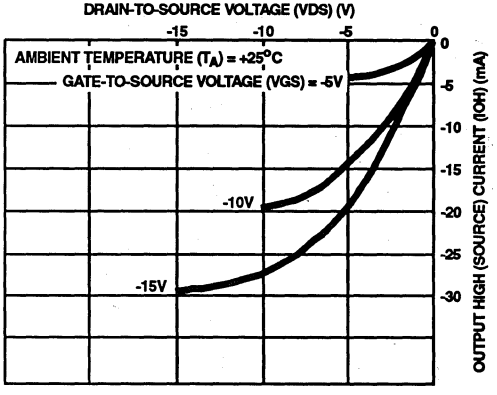


FIGURE 8. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

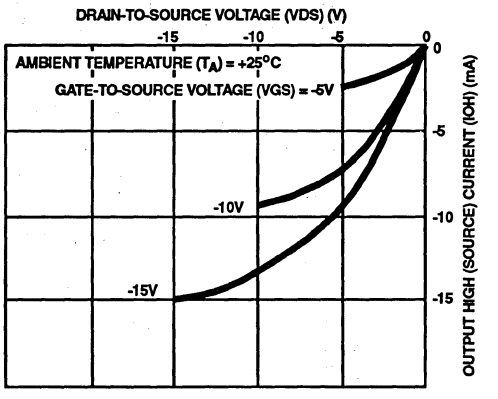


FIGURE 9. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

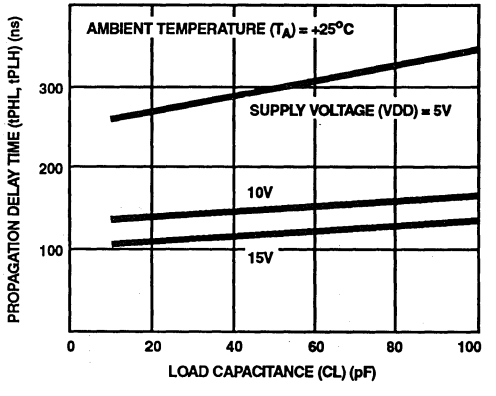


FIGURE 10. TYPICAL PROPAGATION DELAY TIME (LOGIC INPUTS TO OUTPUT) AS A FUNCTION OF LOAD CAPACITANCE

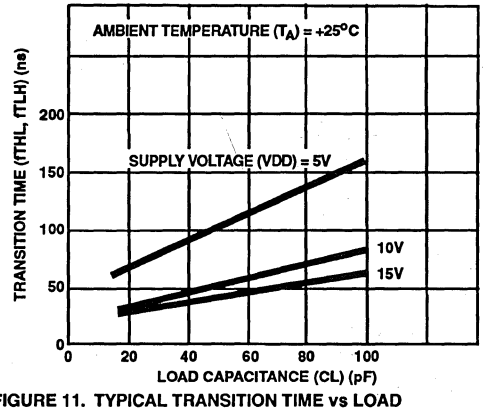


FIGURE 11. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

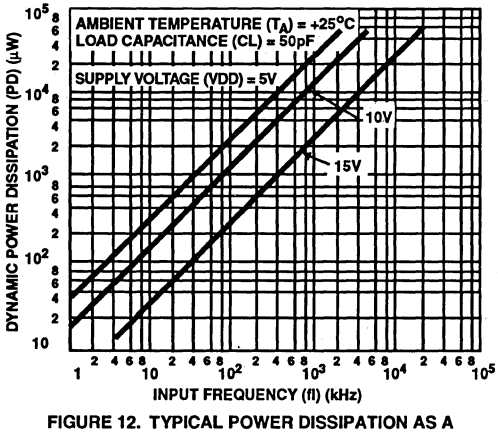


FIGURE 12. TYPICAL POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

Test Circuits and Wave Forms

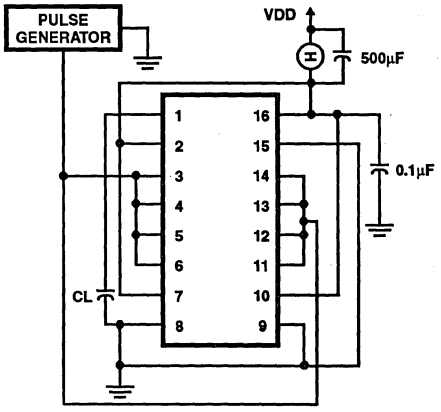


FIGURE 13. DYNAMIC POWER DISSIPATION TEST CIRCUIT

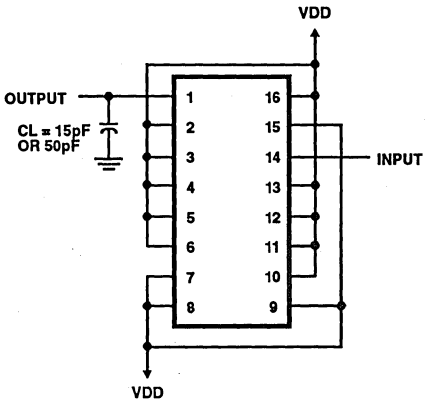


FIGURE 14. TEST CIRCUIT FOR tPHL, tTHL, AND tTHL (AND) MEASUREMENTS

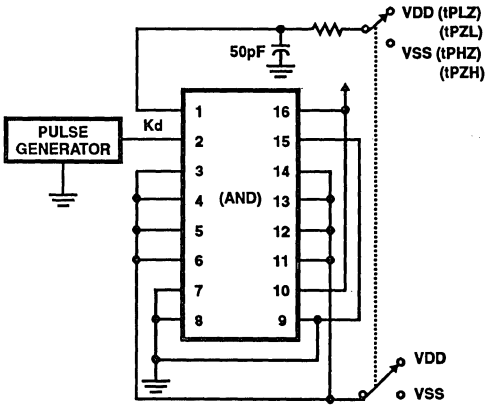


FIGURE 15. TEST CIRCUIT FOR tPZL, tPZH, tPLZ, AND tPHZ (AND)

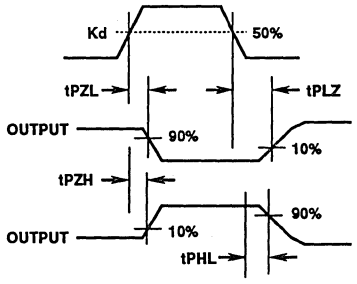


FIGURE 16. WAVEFORMS FOR tPZL, tPZH, tPLZ AND tPHZ (AND)

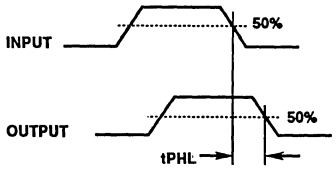


FIGURE 17. WAVEFORMS FOR tPHL AND tPHL (AND)

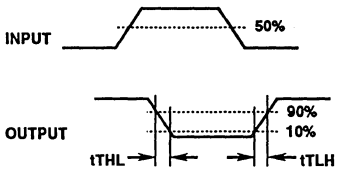
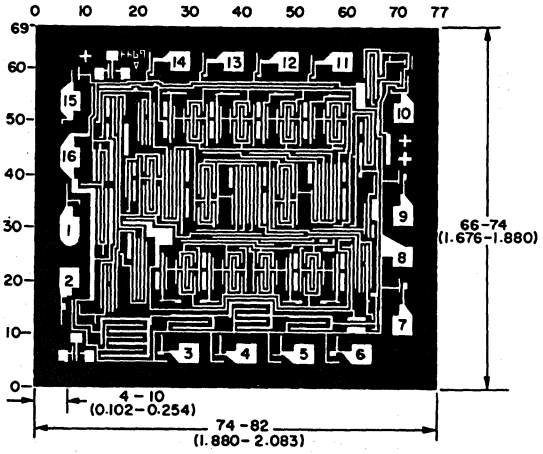


FIGURE 18. WAVEFORMS FOR tTHL AND tTLH (AND)

Chip Dimensions and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4049UBMS

CMOS Hex Buffer/Converter

December 1992

Features

- High Voltage Type (20V Rating)
- Inverting Type
- High Sink Current for Driving 2 TTL Loads
- High-to-Low Level Logic Conversion
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- 5V, 10V and 15V Parametric Ratings

Applications

- CMOS to DTL/TTL Hex Converter
- CMOS Current "Sink" or "Source" Driver
- CMOS High-to-Low Logic Level Converter

Description

The CD4049UBMS is an inverting hex buffer and features logic level conversion using only one supply (voltage (VCC). The input signal high level (VIH) can exceed the VCC supply voltage when this device is used for logic level conversions. This device is intended for use as CMOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (VCC = 5V, VOL ≤ 0.4V, and IOL ≥ 3.3mA.

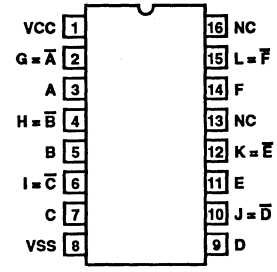
The CD4049UBMS is designated as replacement for CD4009UB. Because the CD4049UBMS requires only one power supply, it is preferred over the CD4009UB and CD4010B and should be used in place of the CD4009UB in all inverter, current driver, or logic level conversion applications. In these applications the CD4049UBMS is pin compatible with the CD4009UB, and can be substituted for this device in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049UBMS, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink current or voltage conversion, the CD4069UB Hex Inverter is recommended.

The CD4049UBMS is supplied in these 16 lead outline packages:

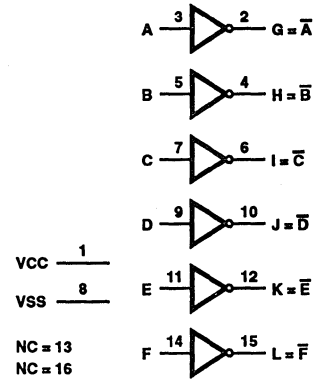
Braze Seal DIP	H4S
Frit Seal DIP	H1E
Ceramic Flatpack	H3X

Pinout

CD4049UBMS
TOP VIEW



Functional Diagram



Schematic

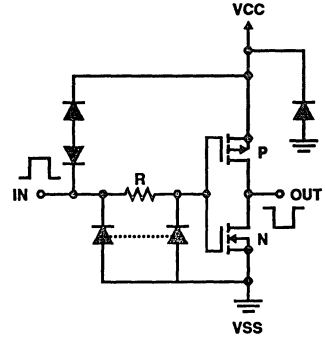


FIGURE 1. SCHEMATIC DIAGRAM, 1 OF 6 IDENTICAL UNITS

7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3315

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL4	VDD = 4.5V, VOUT = 0.4V		1	+25°C	2.6	-	mA
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	3.2	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	8.0	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	24	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.8	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-3.2	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-6.0	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.0	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	4.0	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	2.5	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	12.5	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL	VDD = 5V, VIN = VDD or GND	9	+25°C	-	65	ns
			10, 11	+125°C, -55°C	-	88	ns
Propagation Delay	TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	120	ns
			10, 11	+125°C, -55°C	-	162	ns
Transition Time	TTHL	VDD = 5V, VIN = VDD or GND	9	+25°C	-	60	ns
			10, 11	+125°C, -55°C	-	81	ns
Transition Time	TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	160	ns
			10, 11	+125°C, -55°C	-	216	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL4	VDD = 4.5V, VOUT = 0.4V	1, 2	+125°C	1.8	-	mA
				-55°C	3.3	-	mA
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	2.4	-	mA
				-55°C	4.0	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	5.6	-	mA
				-55°C	10	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	18	-	mA
				-55°C	26	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.48	mA
				-55°C	-	-0.81	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.55	mA
				-55°C	-	-2.6	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-1.18	mA
				-55°C	-	-2.0	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-3.1	mA
				-55°C	-	-5.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	2	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	8	-	V
Propagation Delay	TPHL	VIN = 10V, VDD = 5V	1, 2, 3	+25°C	-	30	ns
		VIN = 10V, VDD = 10V	1, 2, 3	+25°C	-	40	ns
Propagation Delay	TPLH	VIN = 10V, VDD = 5V	1, 2, 3	+25°C	-	90	ns
		VIN = 10V, VDD = 10V	1, 2, 3	+25°C	-	65	ns
Propagation Delay	TPHL	VIN = 15V, VDD = 5V	1, 2, 3	+25°C	-	20	ns
		VIN = 15V, VDD = 15V	1, 2, 3	+25°C	-	30	ns
Propagation Delay	TPLH	VIN = 15V, VDD = 5V	1, 2, 3	+25°C	-	90	ns
		VIN = 15V, VDD = 15V	1, 2, 3	+25°C	-	50	ns
Transition Time	TTHL	VDD = 10V, VIN = VDD OR GND	1, 2, 3	+25°C	-	40	ns
		VDD = 15V, VIN = VDD OR GND	1, 2, 3	+25°C	-	30	ns
Transition Time	TTLH	VDD = 10V, VIN = VDD OR GND	1, 2, 3	+25°C	-	80	ns
		VDD = 15V, VIN = VDD OR GND	1, 2, 3	+25°C	-	60	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	22.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTND	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTPD	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	2, 4, 6, 10, 12, 13, 15	3, 5, 7-9, 11-14	1, 16			
Static Burn-In 2 (Note 1)	2, 4, 6, 10, 12, 13, 15	8	1, 3, 5, 7, 9, 11, 14, 16			
Dynamic Burn-In (Note 3)	13	8	1, 16	2, 4, 6, 10, 12, 15	3, 5, 7, 9, 11, 14	
Irradiation (Note 2)	2, 4, 6, 10, 12, 13, 15, 16	8	1, 3, 5, 7, 9, 11, 14			

NOTE:

1. Each pin except pin 1, pin 16, and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except pin 1, pin 16, and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V
3. Each pin except pin 1, pin 16, and GND will have a series resistor of 4.75K ± 5%, VDD = 18V ± 0.5V

Typical Performance Characteristics

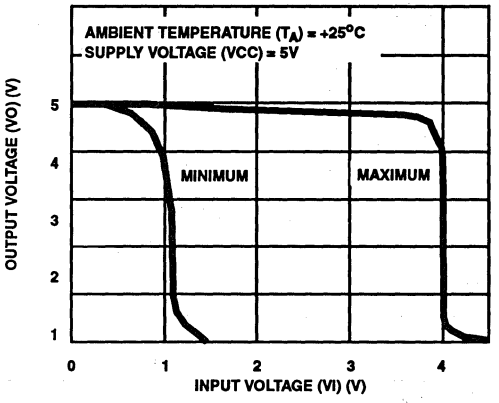


FIGURE 2. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS

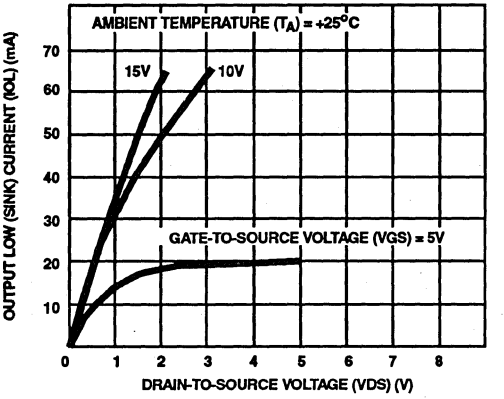


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

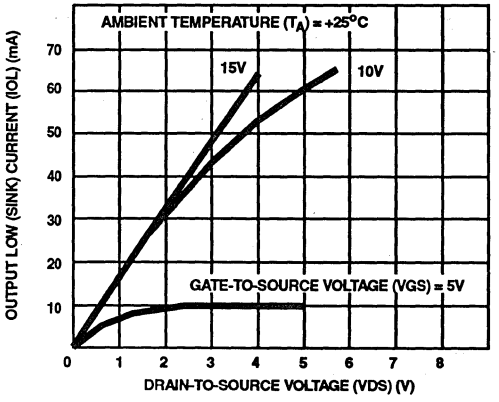


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT DRAIN CHARACTERISTICS

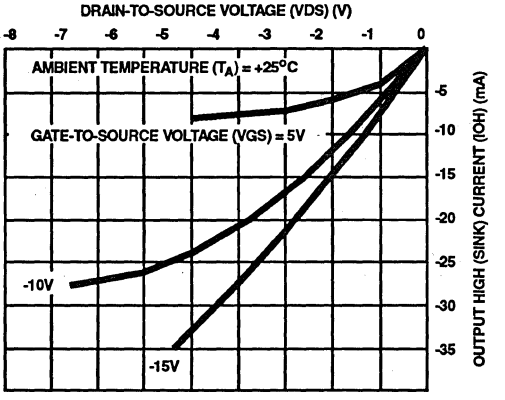


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

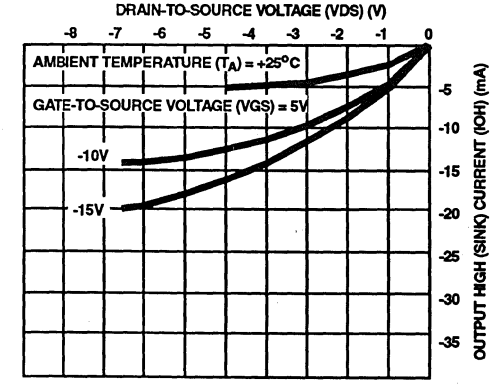


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

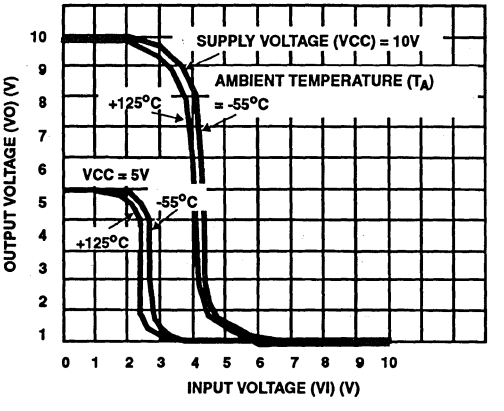


FIGURE 7. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE

Typical Performance Characteristics (Continued)

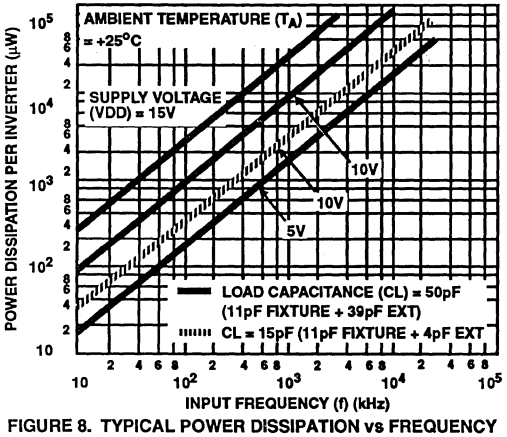


FIGURE 8. TYPICAL POWER DISSIPATION vs FREQUENCY CHARACTERISTICS

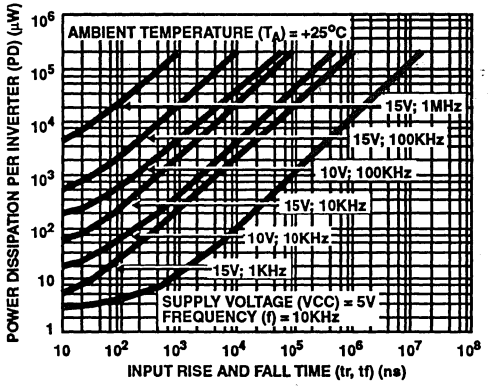
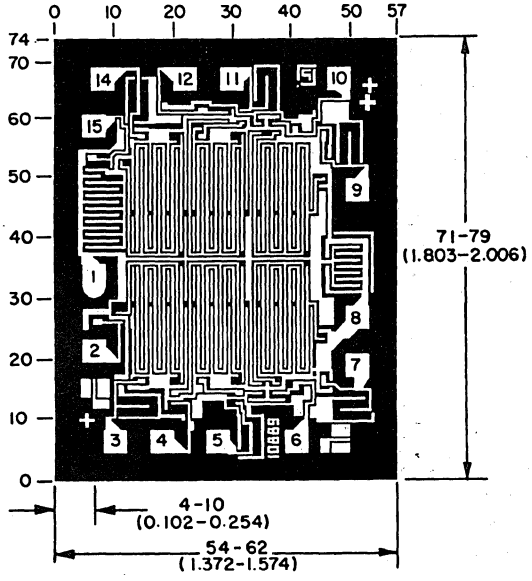


FIGURE 9. TYPICAL POWER DISSIPATION vs INPUT RISE AND FALL TIMES PER INVERTER

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4050BMS

CMOS Hex Buffer/Converter

December 1992

Features

- High Voltage Type (20V Rating)
- Non-Inverting Type
- High Sink Current for Driving 2 TTL Loads
- High-to-Low Level Logic Conversion
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- 5V, 10V and 15V Parametric Ratings

Applications

- CMOS to DTL/TTL Hex Converter
- CMOS Current "Sink" or "Source" Driver
- CMOS High-to-Low Logic Level Converter

Description

The CD4050BMS is an non-inverting hex buffer and features logic level conversion using only one supply voltage (VCC). The input signal high level (VIH) can exceed the VCC supply voltage when this device is used for logic level conversions. This device is intended for use as CMOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (VCC = 5V, VOL ≤ 0.4V, and IOL ≥ 3.3mA.

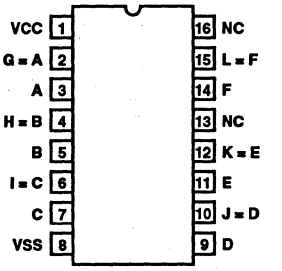
The CD4050BMS is designated as replacement for CD4010B. Because the CD4050BMS requires only one power supply, it is preferred over the CD4010B and should be used in place of the CD4010B in all inverter, current driver, or logic level conversion applications. In these applications the CD4050BMS is pin compatible with the CD4010B, and can be substituted for this device in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4050BMS, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink current or voltage conversion, the CD4069UB Hex Inverter is recommended.

The CD4050BMS is supplied in these 16 lead outline packages:

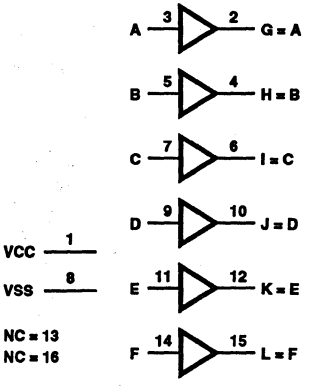
Braze Seal DIP	H4T
Frit Seal DIP	H1E
Ceramic Flatpack	H3X

Pinout

CD4050BMS
TOP VIEW



Functional Diagram



Schematic Diagram

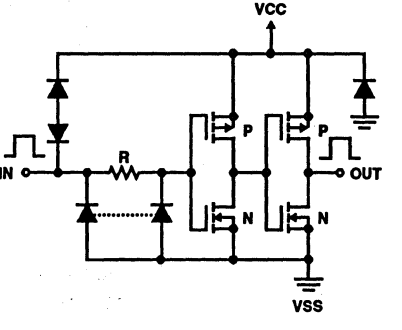


FIGURE 1. SCHEMATIC DIAGRAM, 1 OF 6 IDENTICAL UNITS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3193

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance ..... θ_{ja} θ_{jc}
Ceramic DIP and FRIT Package ..... 80°C/W 20°C/W
Flatpack Package ..... 70°C/W 20°C/W
Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL4	VDD = 4.5V, VOUT = 0.4V		1	+25°C	2.6	-	mA
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	3.2	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	8.0	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	24	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.8	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-3.2	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-6.0	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL	VDD = 5V, VIN = VDD or GND	9	+25°C	-	110	ns
			10, 11	+125°C, -55°C	-	149	ns
Propagation Delay	TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	140	ns
			10, 11	+125°C, -55°C	-	189	ns
Transition Time	TTHL	VDD = 5V, VIN = VDD or GND	9	+25°C	-	60	ns
			10, 11	+125°C, -55°C	-	81	ns
Transition Time	TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	160	ns
			10, 11	+125°C, -55°C	-	216	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL4	VDD = 4.5V, VOUT = 0.4V	1, 2	+125°C	1.8	-	mA
				-55°C	3.3	-	mA
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	2.4	-	mA
				-55°C	4.0	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	5.6	-	mA
				-55°C	10	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	18	-	mA
				-55°C	26	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.48	mA
				-55°C	-	-0.81	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.55	mA
				-55°C	-	-2.6	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-1.18	mA
				-55°C	-	-2.0	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-3.1	mA
				-55°C	-	-5.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay	TPHL	VIN = 10V, VDD = 5V	1, 2, 3	+25°C	-	100	ns
		VIN = 10V, VDD = 10V	1, 2, 3	+25°C	-	55	ns
Propagation Delay	TPLH	VIN = 10V, VDD = 5V	1, 2, 3	+25°C	-	90	ns
		VIN = 10V, VDD = 10V	1, 2, 3	+25°C	-	80	ns
Propagation Delay	TPHL	VIN = 15V, VDD = 5V	1, 2, 3	+25°C	-	100	ns
		VIN = 15V, VDD = 15V	1, 2, 3	+25°C	-	30	ns
Propagation Delay	TPLH	VIN = 15V, VDD = 5V	1, 2, 3	+25°C	-	80	ns
		VIN = 15V, VDD = 15V	1, 2, 3	+25°C	-	60	ns
Transition Time	TTHL	VDD = 10V, VIN = VDD OR GND	1, 2, 3	+25°C	-	40	ns
		VDD = 15V, VIN = VDD OR GND	1, 2, 3	+25°C	-	30	ns
Transition Time	TTLH	VDD = 10V, VIN = VDD OR GND	1, 2, 3	+25°C	-	80	ns
		VDD = 15V, VIN = VDD OR GND	1, 2, 3	+25°C	-	60	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parametric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	2, 4, 6, 10, 12, 13, 15	3, 5, 7-9, 11-14	1, 16			
Static Burn-In 2 (Note 1)	2, 4, 6, 10, 12, 13, 15	8	1, 3, 5, 7, 9, 11, 14, 16			
Dynamic Burn-In (Note 3)	13	8	1, 16	2, 4, 6, 10, 12, 15	3, 5, 7, 9, 11, 14	
Irradiation (Note 2)	2, 4, 6, 10, 12, 13, 15, 16	8	1, 3, 5, 7, 9, 11, 14			

NOTE:

1. Each pin except pin 1, pin 16, and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except pin 1, pin 16, and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V
3. Each pin except pin 1, pin 16, and GND will have a series resistor of 4.75K ± 5%, VDD = 10V ± 0.5V

Typical Performance Characteristics

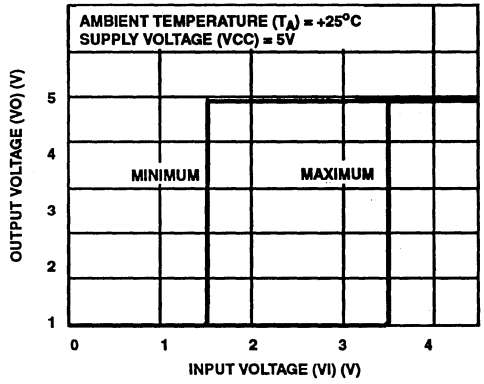


FIGURE 2. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS

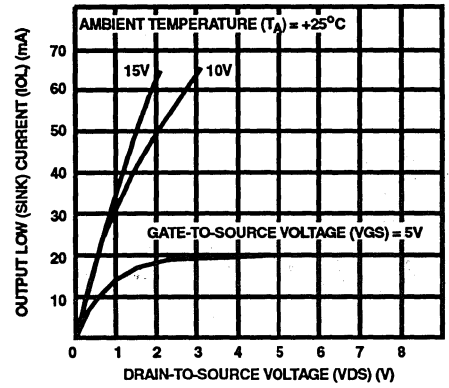


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

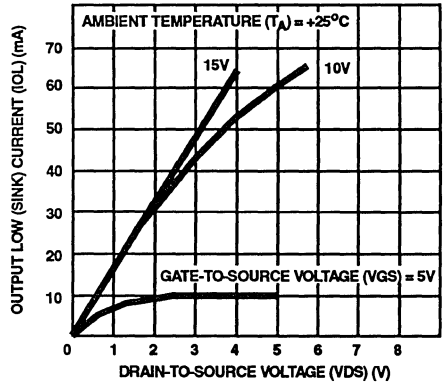


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT DRAIN CHARACTERISTICS

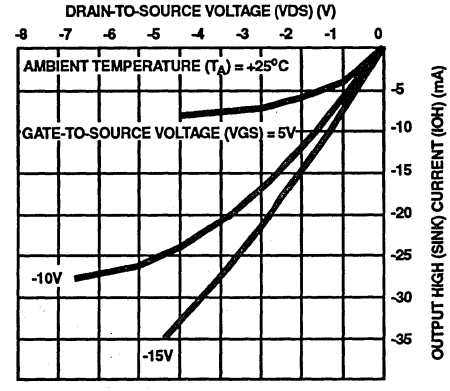


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

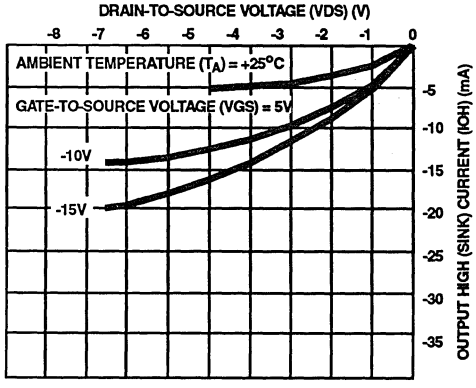


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

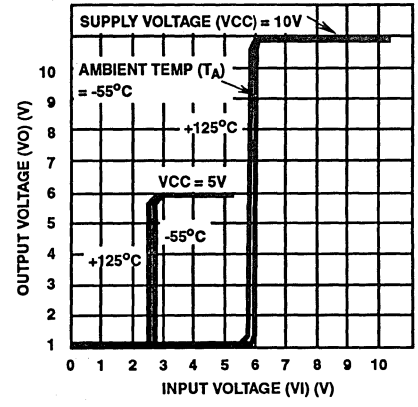


FIGURE 7. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE

Typical Performance Characteristics (Continued)

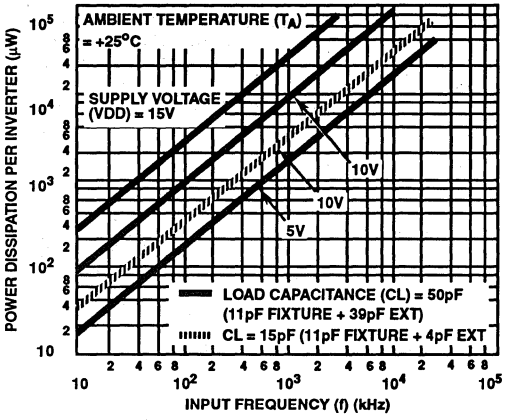


FIGURE 8. TYPICAL POWER DISSIPATION vs FREQUENCY CHARACTERISTICS

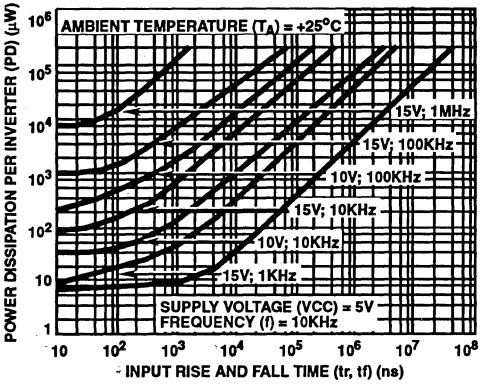
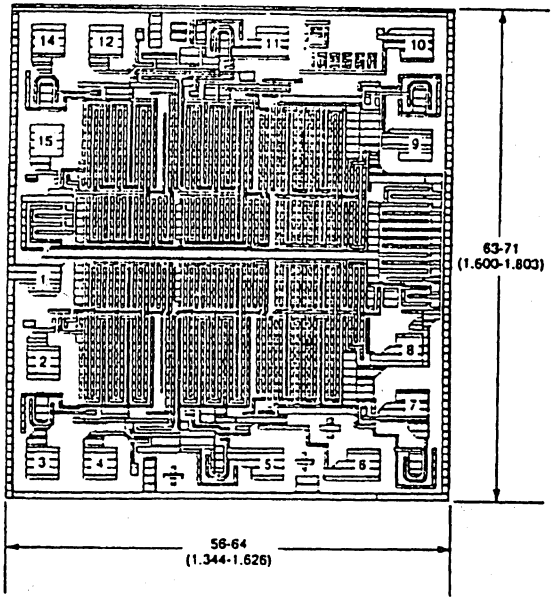


FIGURE 9. TYPICAL POWER DISSIPATION vs INPUT RISE AND FALL TIMES PER INVERTER

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4051BMS, CD4052BMS CD4053BMS

CMOS Analog Multiplexers/Demultiplexers*

December 1992

Features

- Logic Level Conversion
- High-Voltage Types (20V Rating)
- CD4051BMS Signal 8-Channel
- CD4052BMS Differential 4-Channel
- CD4053BMS Triple 2-Channel
- Wide Range of Digital and Analog Signal Levels:
  - Digital 3V to 20V
  - Analog to 20Vp-p
- Low ON Resistance: 125Ω (typ) Over 15Vp-p Signal Input Range for VDD - VEE = 15V
- High OFF Resistance: Channel Leakage of ±100pA (typ) at VDD - VEE = 18V
- Logic Level Conversion:
  - Digital Addressing Signals of 3V to 20V (VDD - VSS = 3V to 20V)
  - Switch Analog Signals to 20Vp-p (VDD - VEE = 20V); See Introductory Text
- Matched Switch Characteristics: RON = 5Ω (typ) for VDD - VEE = 15V
- Very Low Quiescent Power Dissipation Under All Digital Control Input and Supply Conditions: 0.2μW (typ) at VDD - VSS = VDD - VEE = 10V
- Binary Address Decoding on Chip
- 5V, 10V and 15V Parametric Ratings
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Break-Before-Making Switching Eliminates Channel Overlap

Applications

- Analog and Digital Multiplexing and Demultiplexing
- A/D and D/A Conversion
- Signal Gating

* When these devices are used as demultiplexers the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminals are the inputs.

Description

CD4051BMS, CD4052BMS and CD4053BMS analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20V peak-to-peak can be achieved by digital signal amplitudes of 4.5V to 20V (if VDD-VSS = 3V, a VDD-VEE of up to 13V can be controlled; for VDD-VEE level differences above 13V, a VDD-VSS of at least 4.5V is required). For example, if VDD = +4.5V, VSS = 0, and VEE = -13.5V, analog signals from -13.5V to +4.5V can be controlled by digital inputs of 0 to 5V. These multiplexer circuits dissipate extremely low quiescent power over the full VDD-VSS and VDD-VEE supply voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the inhibit input terminal all channels are off.

The CD4051BMS is a single 8 channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052BMS is a differential 4 channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053BMS is a triple 2 channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single pole double-throw configuration.

The CD4051BMS, CD4052BMS and CD4053BMS are supplied in these 16 lead outline packages:

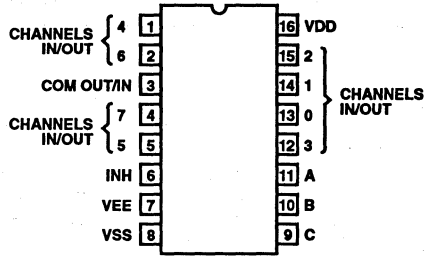
Braze Seal DIP	*H4X	†H4T
Frit Seal DIP	H1E	
Ceramic Flatpack	H6W	

*CD4051B Only †CD4052B, CD4053 Only

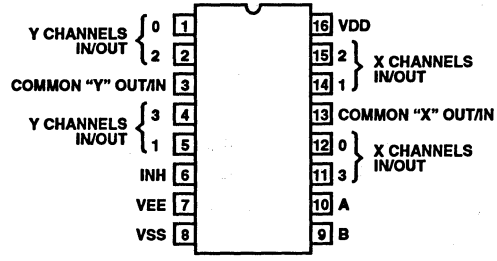
7 LOGIC

Pinouts

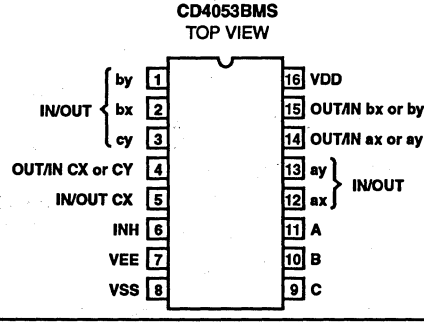
CD4051BM
TOP VIEW



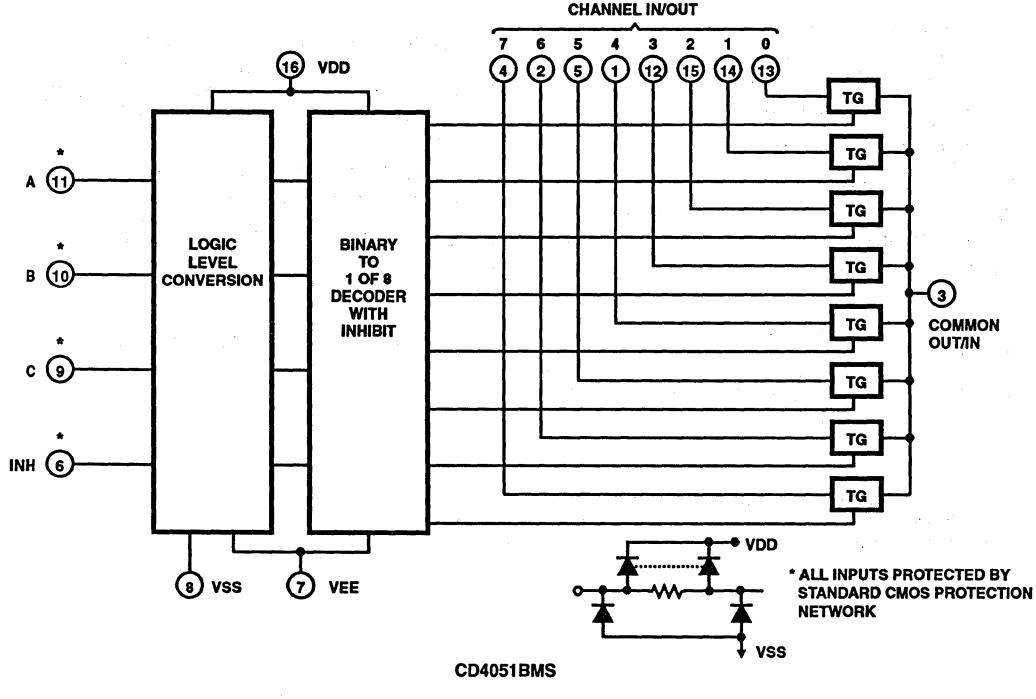
CD4052BMS
TOP VIEW



CD4053BMS
TOP VIEW

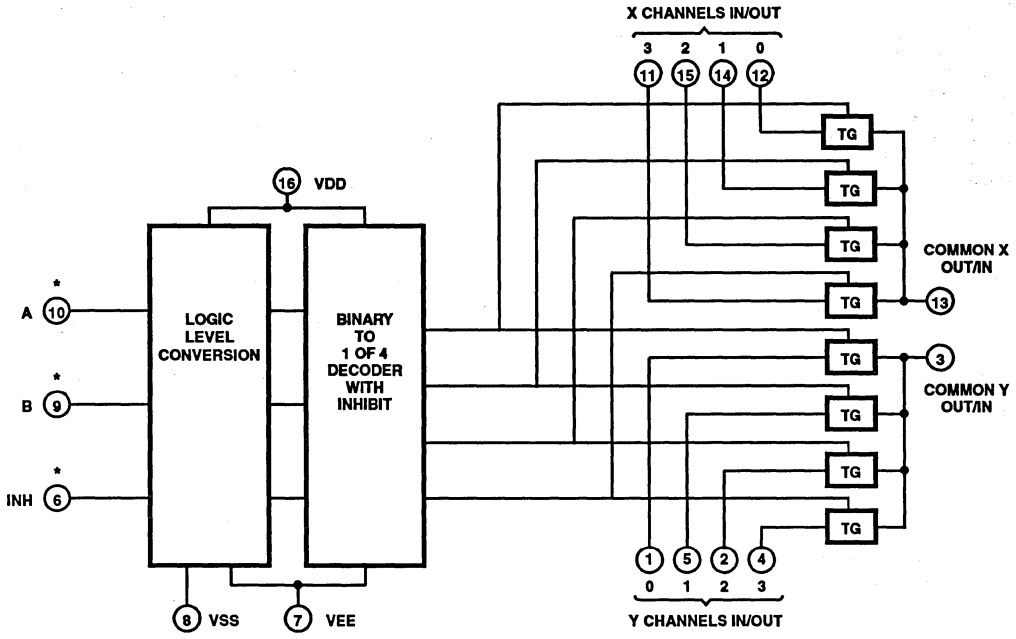


Functional Diagrams

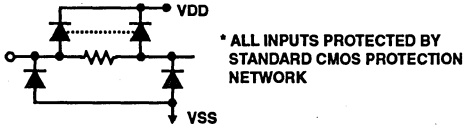


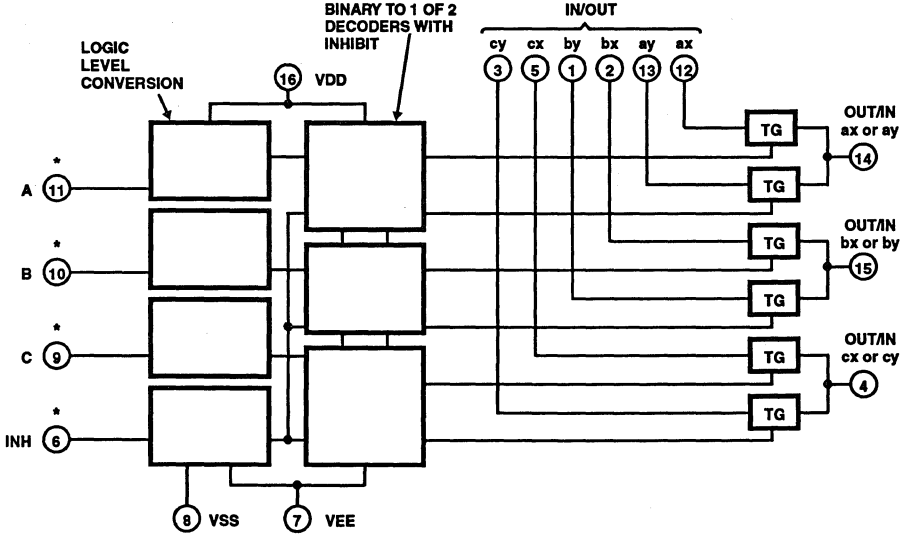
CD4051BMS

Functional Diagrams (Continued)



CD4052BMS





CD4053BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
On-State Resistance RL = 10K Returned to VDD - VSS/2	RON	VDD = 5V VIS = VSS to VDD		1	+25°C	-	1050	Ω
				2	+125°C	-	1300	Ω
				3	-55°C	-	800	Ω
		VDD = 10V VIS = VSS to VDD		1	+25°C	-	400	Ω
				2	+125°C	-	550	Ω
				3	-55°C	-	310	Ω
		VDD = 15V VIS = VSS to VDD		1	+25°C	-	240	Ω
				2	+125°C	-	320	Ω
				3	-55°C	-	220	Ω
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional (Note 4)	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V = VIS thru 1k, VEE = VSS RL = 1k to VSS, IIISI < 2µA OFF Channels		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH			1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V = VIS thru 1K VEE = VSS RL = 1K to VSS, IISSI, <2µA On All OFF Channels		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH			1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Off Channel Leakage Any Channel OFF Or All Channels Off (Common Out/In)	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.1	-	µA
				2	+125°C	-1.0	-	µA
			VDD = 18V	3	-55°C	-0.1	-	µA
	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.1	µA
				2	+125°C	-	1.0	µA
			VDD = 18V	3	-55°C	-	0.1	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.
4. VDD = 2.8V/3.0V, RL = 200k to VDD
VDD = 20V/18V, RL = 10k to VDD

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (Notes 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay (Note 1) Address to Signal Out Channels On or Off	TPHL TPLH	VDD = 5V, VIN = VDD or GND VEE = VSS = 0V	9	+25°C	-	720	ns
			10, 11	+125°C, -55°C	-	972	ns
Propagation Delay (Note 1) Inhibit to Signal Out (Channel Turning On)	TPZH TPZL	VDD = 5V, VIN = VDD or GND VEE = VSS = 0V	9	+25°C	-	720	ns
			10, 11	+125°C, -55°C	-	972	ns
Propagation Delay (Note 1) Inhibit to Signal Out (Channel Turning Off)	TPHZ TPLZ	VDD = 5V, VIN = VDD or GND VEE = VSS = 0V	9	+25°C	-	450	ns
			10, 11	+125°C, -55°C	-	608	ns

NOTES:

1. -55°C and +125°C limits guaranteed, 100% testing being implemented.
2. CL = 50pF, RL = 10KΩ, Input TR, TF < 20ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS		NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND		1, 2	-55°C, +25°C	-	5	µA
					+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND		1, 2	-55°C, +25°C	-	10	µA
					+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND		1, 2	-55°C, +25°C	-	10	µA
					+125°C	-	600	µA
Input Voltage Low	VIL	VDD = VIS = 10V, VEE = VSS RL = 1K to VSS IIISI, 2µA On/Off Channel		1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH			1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Address to Signal Out (Channels On or Off)	TPHL TPLH	VDD = 10V	VEE = VSS = 0V	1, 2, 3	+25°C	-	320	ns
		VDD = 15V		1, 2, 3	+25°C	-	240	ns
		VDD = 5V VEE = -5V		1, 2, 3	+25°C	-	450	ns
Propagation Delay Inhibit to Signal Out (Channel Turning On)	TPZH TPZL	VDD = 10V	VEE = VSS = 0V	1, 2, 3	+25°C	-	320	ns
		VDD = 15V		1, 2, 3	+25°C	-	240	ns
		VDD = 5V VEE = -10V		1, 2, 3	+25°C	-	400	ns
Propagation Delay Inhibit to Signal Out (Channel Turning Off)	TPHZ TPLZ	VDD = 10V	VEE = VSS = 0V	1, 2, 3	+25°C	-	210	ns
		VDD = 15V		1, 2, 3	+25°C	-	160	ns
		VDD = 5V VEE = -15V		1, 2, 3	+25°C	-	300	ns
Input Capacitance	CIN	Any Address or Inhibit Input		1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 10K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
ON Resistance	RONDEL10	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
PART NUMBER CD4051BMS						
Static Burn-In 1 Note 1	3	1, 2, 4 - 6, 7, 8, 9 - 15	16			
Static Burn-In 2 Note 1	3	7, 8	1, 2, 4 - 6, 9 - 16			
Dynamic Burn-In Note 1	-	4 - 6, 7, 8, 9, 12, 14	1, 2, 13, 15, 16	3	11	10
Irradiation Note 2	3	7, 8	1, 2, 4 - 6, 9 - 16			
PART NUMBER CD4052BMS						
Static Burn-In 1 Note 1	3, 13	1, 2, 4 - 6, 7, 8, 9 - 12, 14, 15	16			
Static Burn-In 2 Note 1	3, 13	7, 8	1, 2, 4 - 6, 9 - 12, 14 - 16			
Dynamic Burn-In Note 1	-	4 - 6, 7, 8, 12, 15	1, 2, 11, 14, 16	3, 13	10	9
Irradiation Note 2	3, 13	7, 8	1, 2, 4 - 6, 9 - 12, 14 - 16			
PART NUMBER CD4053BMS						
Static Burn-In 1 Note 1	4, 14, 15	1 - 3, 5 - 8, 9 - 13	16			
Static Burn-In 2 Note 1	4, 14, 15	7, 8	1 - 3, 5, 6, 9 - 13, 16			
Dynamic Burn-In Note 1	-	1, 5 - 8, 12	2, 3, 13, 16	4, 14, 15	9 - 11	
Irradiation Note 2	4, 14, 15	7, 8	1 - 3, 5, 6, 9 - 13, 16			

NOTE:

1. Each pin except pin 7 VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except pin 7 VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Typical Performance Characteristics

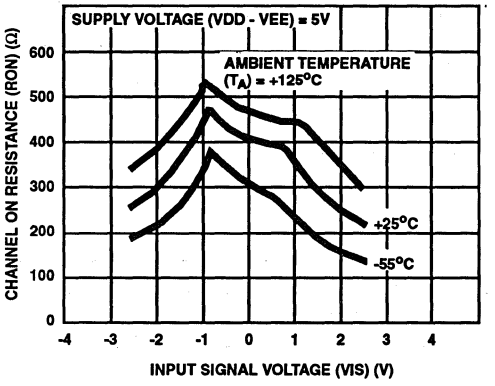


FIGURE 1. TYPICAL CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

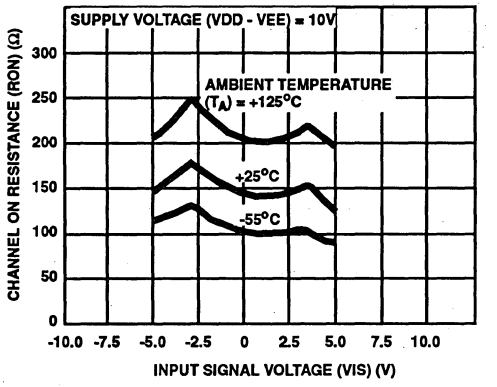


FIGURE 2. TYPICAL CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

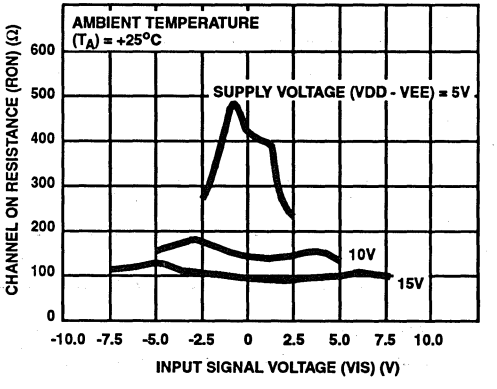


FIGURE 3. TYPICAL CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLATGE (ALL TYPES)

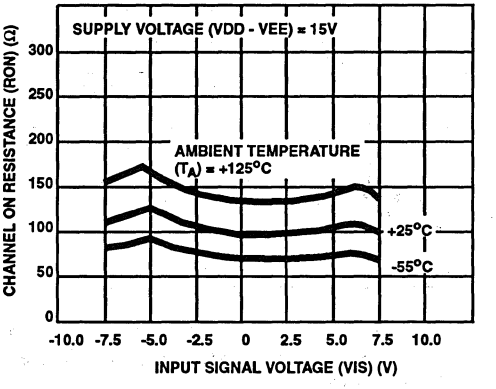


FIGURE 4. TYPICAL CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

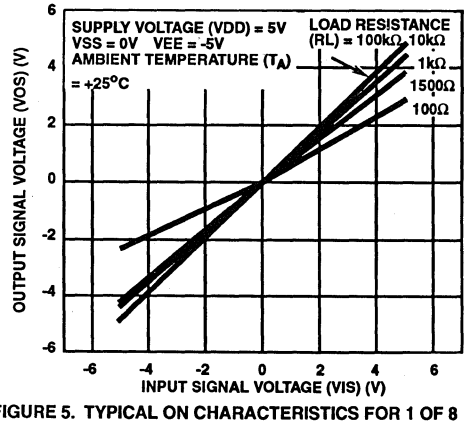


FIGURE 5. TYPICAL ON CHARACTERISTICS FOR 1 OF 8 CHANNELS (CD4051BMS)

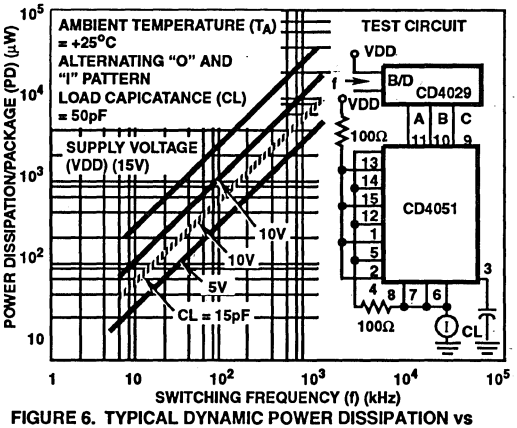


FIGURE 6. TYPICAL DYNAMIC POWER DISSIPATION vs SWITCHING FREQUENCY (CD4051BMS)

Typical Performance Characteristics (Continued)

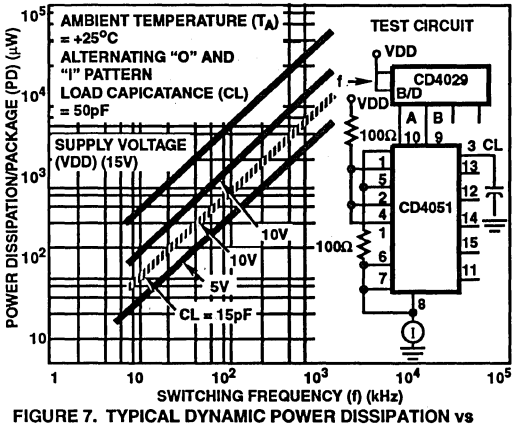


FIGURE 7. TYPICAL DYNAMIC POWER DISSIPATION vs SWITCHING FREQUENCY (CD4052BMS)

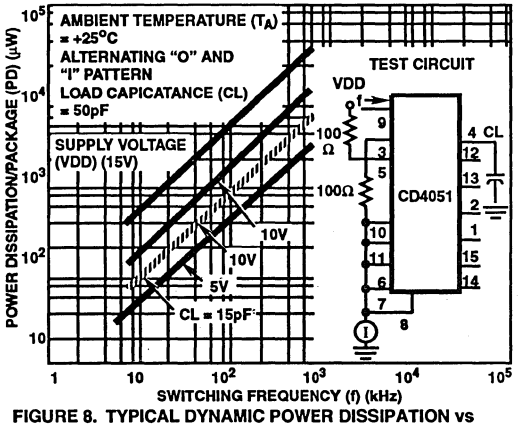
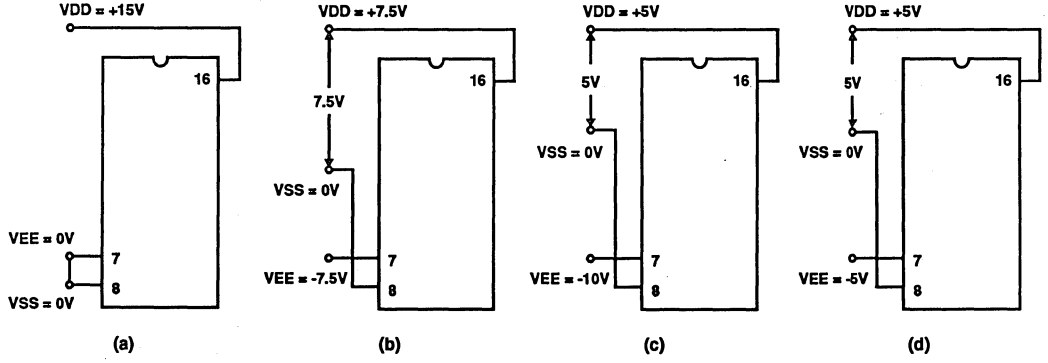


FIGURE 8. TYPICAL DYNAMIC POWER DISSIPATION vs SWITCHING FREQUENCY (CD4053BMS)



The ADDRESS (digital-control inputs) and INHIBIT logic levels are: "0" = VSS and "1" = VDD. The analog signal (through the TG) may swing from VEE to VDD

FIGURE 9. TYPICAL BIAS VOLTAGES

TRUTH TABLE

INPUT STATES				"ON" CHANNEL(S)
CD4051BMS				
INHIBIT	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	NONE
CD4052BMS				
INHIBIT		B	A	
0		0	0	0x, 0y
0		0	1	1x, 1y
0		1	0	2x, 2y
0		1	1	3x, 3y
1		x	x	NONE
CD4053BMS				
INHIBIT		A OR B OR C		
0		0		ax or bx or cx
0		1		ay or by or cy
1		X		NONE

X = Don't Care

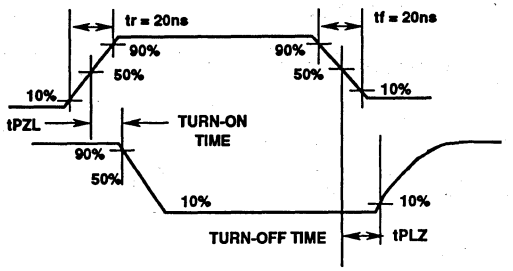


FIGURE 10. WAVEFORM, CHANNEL BEING TURNED ON, OFF (RL = 1kΩ)

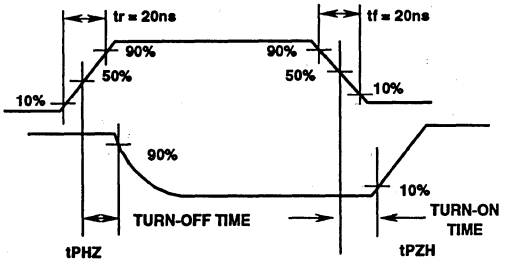


FIGURE 11. WAVEFORM, CHANNEL BEING TURNED OFF, ON (RL = 1kΩ)

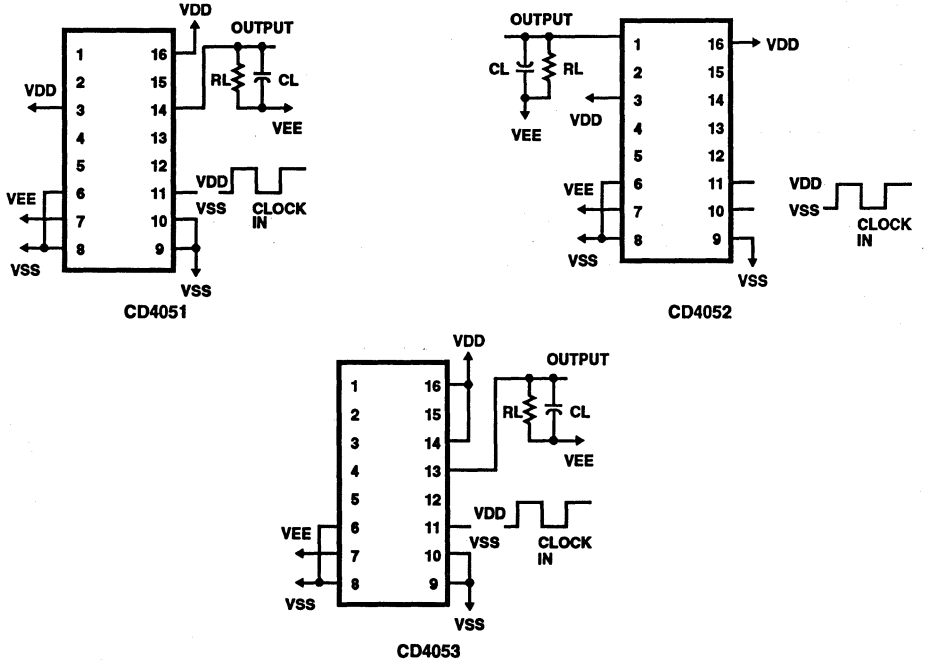


FIGURE 12. PROPAGATION DELAY - ADDRESS INPUT TO SIGNAL OUTPUT

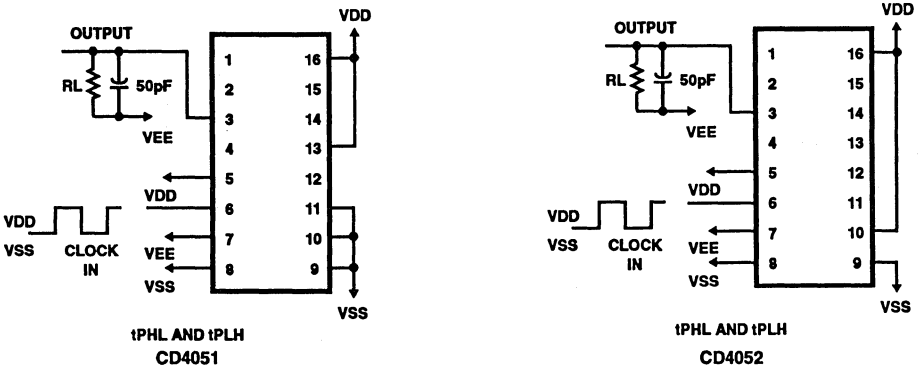


FIGURE 13. PROPAGATION DELAY - INHIBIT INPUT TO SIGNAL OUTPUT

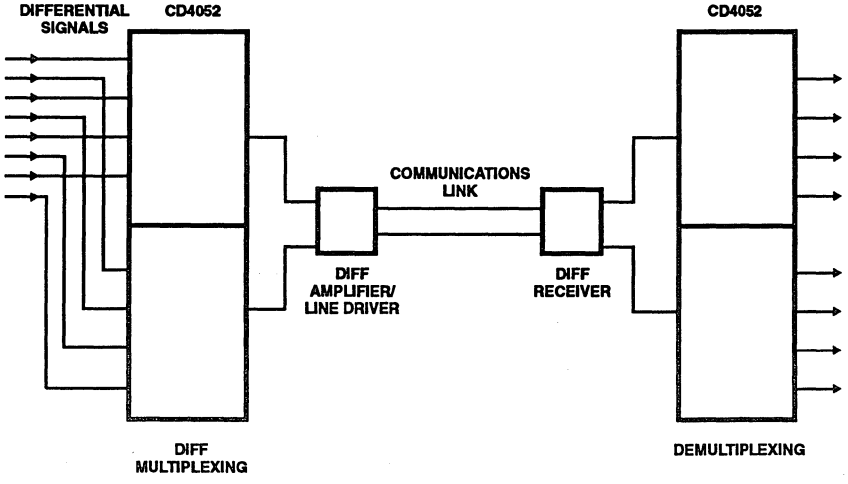
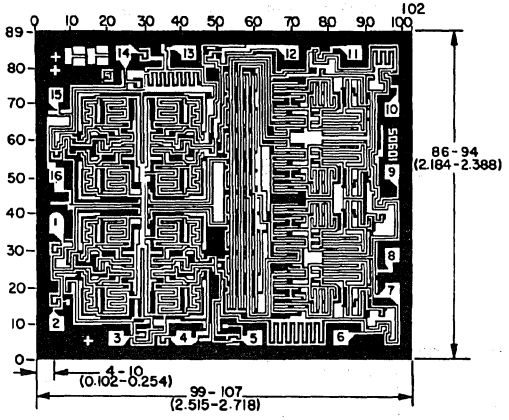
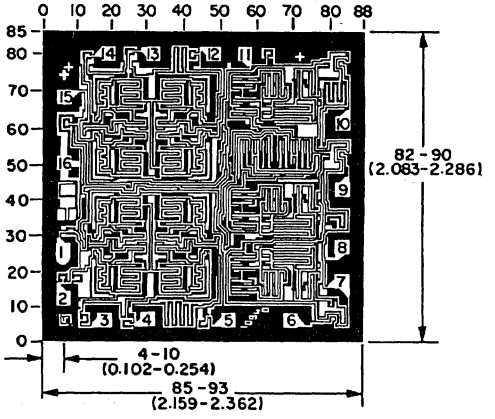


FIGURE 14. TYPICAL TIME-DIVISION APPLICATION OF THE CD4052BMS

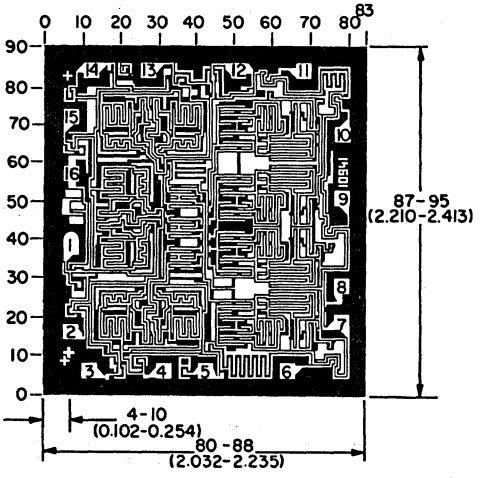
Chip Dimensions and Pad Layouts



CD4051BMSH



CD4052BMSH



CD4053BMSH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4060BMS

CMOS 14 Stage Ripple-Carry Binary Counter/Divider and Oscillator

December 1992

Features

- High Voltage Type (20V Rating)
- Common Reset
- 12MHz Clock Rate at 15V
- Fully Static Operation
- Buffered Inputs and Outputs
- Schmitt Trigger Input Pulse Line
- Standardized, Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Oscillator Features

- All Active Components on Chip
- RC or Crystal Oscillator Configuration
- RC Oscillator Frequency of 690kHz Min. at 15V

Applications

- Control counters
- Timers
- Frequency Dividers
- Time Delay Circuits

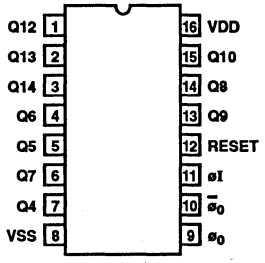
Description

CD4060BMS consists of an oscillator section and 14 ripple carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A RESET input is provided which resets the counter to the all O's state and disables the oscillator. A high level on the RESET line accomplishes the reset function. All counter stages are master slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of øI (and $ø_0$). All inputs and outputs are fully buffered. Schmitt trigger action on the input pulse line permits unlimited input pulse rise and fall times.

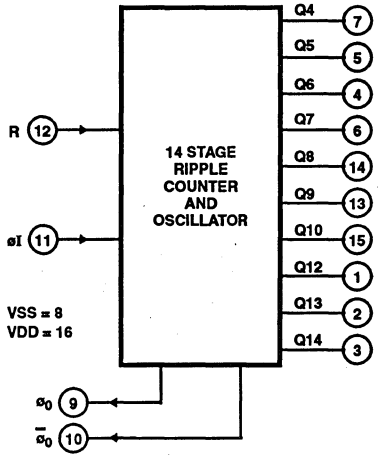
The CD4060BMS is supplied in these 16 lead outline packages:

Braze Seal DIP	H4W
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

Pinout



Functional Diagram



7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3317

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink) (Excluding pins 9 & 10)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source) (Excluding pins 9 & 10)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTES 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Input Pulse Operation øI to Q4	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	740	ns
			10, 11	+125°C, -55°C	-	999	ns
Propagation Delay QN to QN + 1	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Propagation Delay RESET	TPHL3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	360	ns
			10, 11	+125°C, -55°C	-	486	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Input Pulse Frequency	FØI	VDD = 5V VIN = VDD or GND	9	+25°C	3.5	-	MHz
			10, 11	+125°C, -55°C	2.59	-	MHz

NOTES:

1. VDD = 5V, CL = 50pF, RL = 200K
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink) (Excluding pins 9 & 10)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink) (Excluding pins 9 & 10)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink) (Excluding pins 9 & 10)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source) (Excluding pins 9 & 10)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source) (Excluding pins 9 & 10)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source) (Excluding pins 9 & 10)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source) (Excluding pins 9 & 10)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Drive Current at Pin 9 Oscillator Design	IOL	VDD = 5V, VO = .4V	3	+25°C	0.16	-	mA
		VDD = 10V, VO = .5V	3	+25°C	0.42	-	mA
		VDD = 15V, VO = 1.5V	3	+25°C	-1.0	-	mA
Drive Current at Pin 9 Oscillator Design	IOH	VDD = 5V	1, 2, 3	+25°C	-	-.16	mA
		VDD = 10V	1, 2, 3	+25°C	-	-.42	mA
		VDD = 15V	1, 2, 3	+25°C	-	1.0	mA
Propagation Delay Input Pulse øI to Q4	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	300	ns
		VDD = 15V	1, 2, 3	+25°C	-	200	ns
Propagation Delay QN to QN + 1	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Propagation Delay RESET	TPHL3	VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Input Pulse Frequency	FØI	VDD = 10V	1, 2, 3	+25°C	8	-	MHz
		VDD = 15V	1, 2, 3	+25°C	12	-	MHz
Minimum RESET Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	120	ns
		VDD = 10V	1, 2, 3	+25°C	-	60	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Minimum Input Pulse Width F = 100kHz	TW	VDD = 5V	1, 2, 3	+25°C	-	100	ns
		VDD = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V	1, 2, 3	+25°C	-	30	ns
RC Operation RX Max	RX	VDD = 5V, CX = 10µF	2, 3	+25°C	-	20	MΩ
		VDD = 10V, CX = 50µF	2, 3	+25°C	-	20	MΩ
		VDD = 15V, CX = 10µF	2, 3	+25°C	-	10	MΩ
RC Operation CX Max	CX	VDD = 5V, RX = 500kΩ	2, 3	+25°C	-	1000	µF
		VDD = 10V, RX = 300kΩ	2, 3	+25°C	-	50	µF
		VDD = 15V, RX = 300kΩ	2, 3	+25°C	-	50	µF
Maximum Oscillator Frequency (Note 4)	RX = 5kΩ CX = 15pF	VDD = 10V	2, 3	+25°C	530	810	ns
		VDD = 15V	2, 3	+25°C	690	940	ns
RC Operation Variation of Frequency (Unit-to-Unit)	CX = 200pF RS = 560K RX = 50k	VDD = 5V	2, 3	+25°C	18	25	kHz
		VDD = 10V	2, 3	+25°C	20	26	kHz
		VDD = 15V	2, 3	+25°C	21.1	27	kHz
Variation of Frequency with Voltage Change (Same Unit)	CX = 200pF RS = 560K RX = 50k	5V to 10V	2, 3	+25°C	-	2	kHz
		10V to 15V	2, 3	+25°C	-	1	kHz

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. RC Oscillator applications are not recommended at supply voltages below 7V for RX < 50kΩ.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Group D	Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

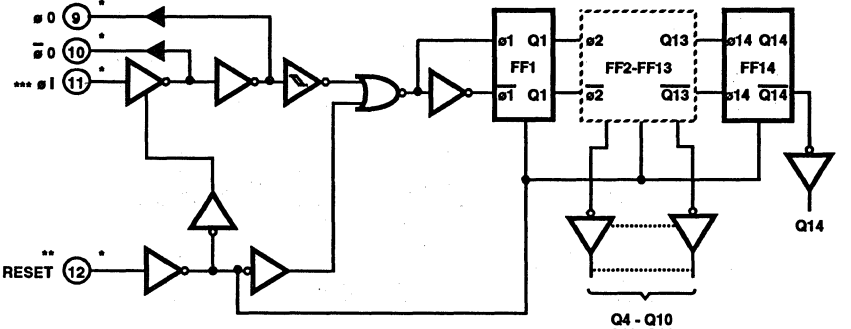
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	1 - 7, 9, 10, 13 - 15	8, 11, 12	16			
Static Burn-In 2 Note 1	1 - 7, 9, 10, 13 - 15	8	11, 12, 16			
Dynamic Burn-In Note 1	-	8, 12	16	1 - 7, 9, 10, 13 - 15	11	-
Irradiation Note 2	1 - 7, 9, 10, 13 - 15	8	11, 12, 16			

NOTES:

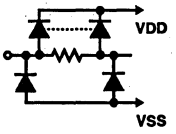
1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram



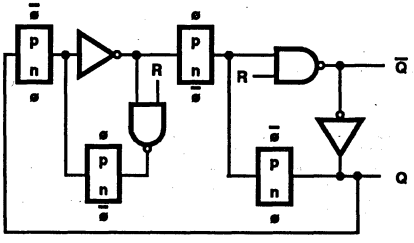
**R = HIGH DOMINATES (RESETS ALL STAGES)

***COUNTER ADVANCES ONE BINARY COUNT ON EACH NEGATIVE - GOING TRANSITION OF øI (AND øO)



*ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

DETAIL OF TYPICAL FLIP-FLOP STAGE



Typical Performance Curves

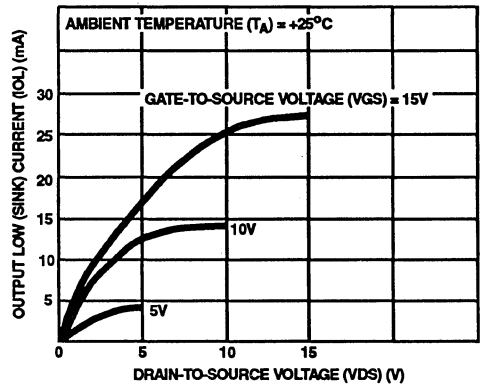


FIGURE 1. TYPICAL N-CHANNEL OUTPUT LOW SINK CURRENT CHARACTERISTICS

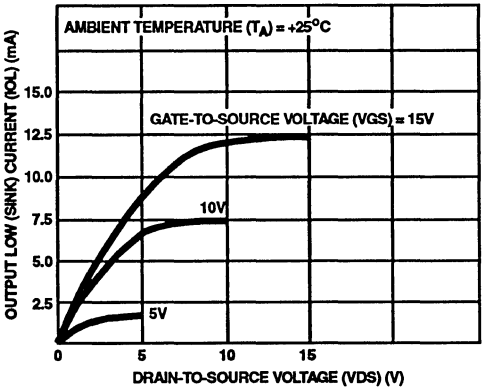


FIGURE 2. MINIMUM N-CHANNEL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

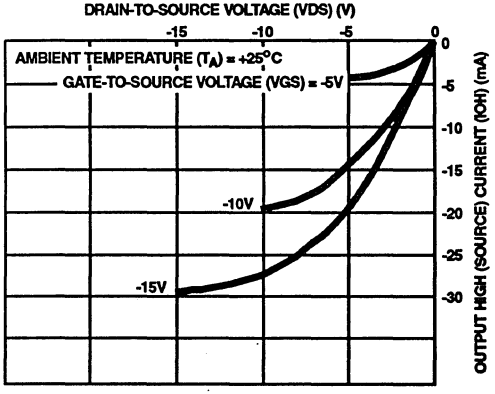


FIGURE 3. TYPICAL P-CHANNEL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

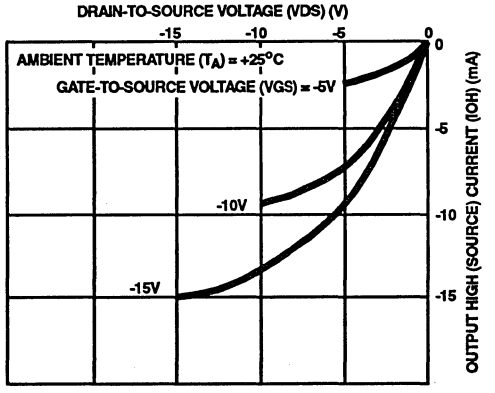


FIGURE 4. MINIMUM P-CHANNEL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

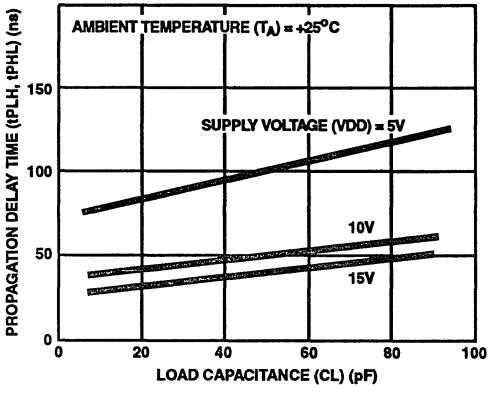


FIGURE 5. TYPICAL PROPAGATION DELAY TIME (QN TO QN+1) AS A FUNCTION OF LOAD CAPACITANCE

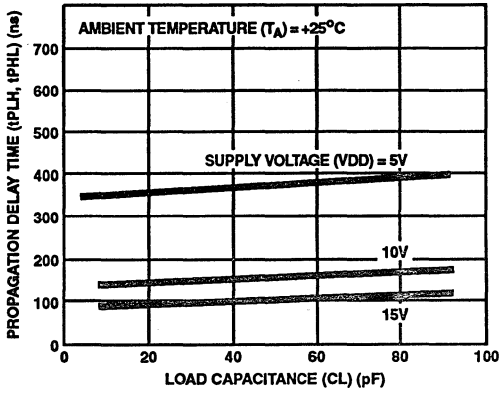


FIGURE 6. TYPICAL PROPAGATION DELAY TIME (Ø1 TO Q4 OUTPUT) AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Curves (Continued)

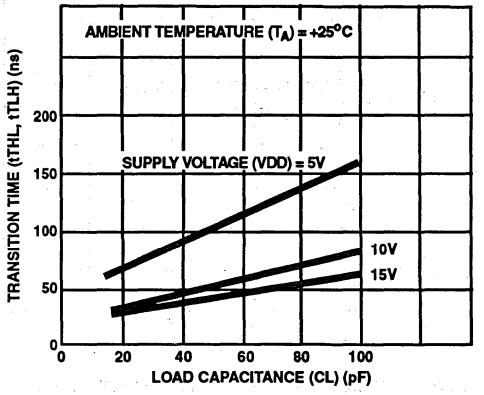


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

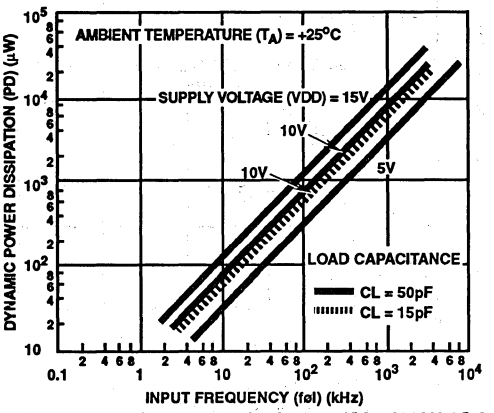


FIGURE 8. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

Test Circuits

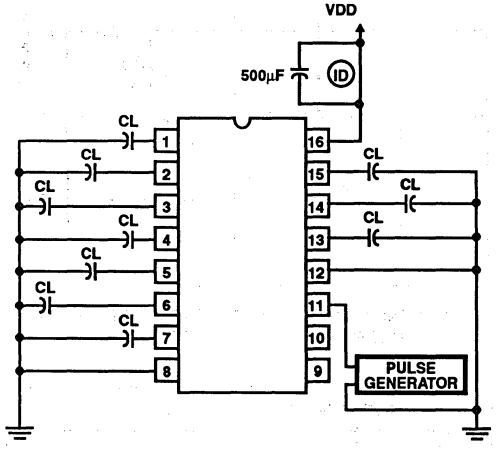


FIGURE 9. DYNAMIC POWER DISSIPATION TEST CIRCUIT

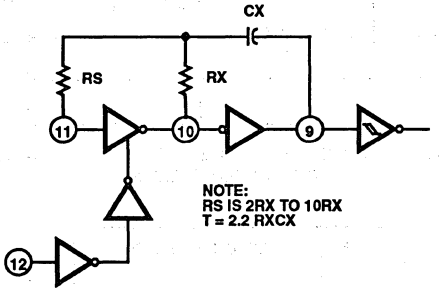
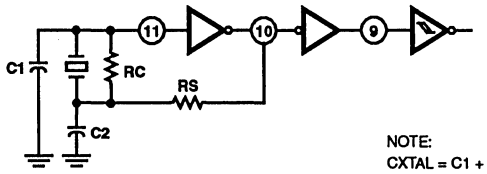


FIGURE 10. TYPICAL RC CIRCUIT

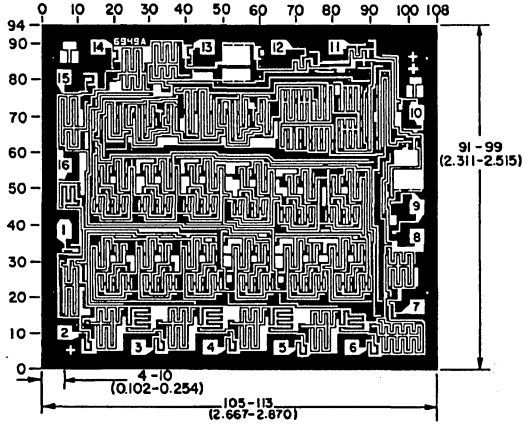
Test Circuits (Continued)



NOTE:
CXTAL = C1 + C2 + CSTRAY
RC = Broader frequency response
RS = Current limiting

FIGURE 11. TYPICAL CRYSTAL CIRCUIT

Chip Dimensions and Pad Layout



Dimension in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4063BMS

December 1992

CMOS 4-Bit Magnitude Comparator

Features

- High Voltage Type (20V Rating)
- Expansion to 8, 12, 16 . . . 4N Bits by Cascading Units
- Medium Speed Operation
  - Compares Two 4-Bit Words in 250ns (Typ.) at 10V
- 100% Tested for Quiescent Current at 20V
- Standardized Symmetrical Output Characteristics
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Full Package Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Servo Motor Controls
- Process Controllers

Description

CD4063BMS is a 4-bit magnitude comparator designed for use in computer and logic applications that require the comparison of two 4-bit words. This logic circuit determines whether one 4-bit word (Binary or BCD) is "less than", "equal to", or "greater than" a second 4-bit word.

The CD4063BMS has eight comparing inputs (A3, B3, through A0, B0), three outputs (A < B, A = B, A > B) and three cascading inputs (A < B, A = B, A > B) that permit systems designers to expand the comparator function to 8, 12, 16 . . . 4N bits. When a single CD4063BMS is used, the cascading inputs are connected as follows: (A < B) = low, (A = B) = high, (A > B) = low.

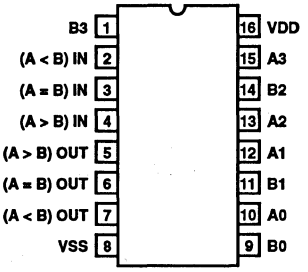
For words longer than 4 bits, CD4063BMS devices may be cascaded by connecting the outputs of the less significant comparator to the corresponding cascading inputs of the more significant comparator. Cascading inputs (A < B, A = B, and A > B) on the least significant comparator are connected to a low, a high, and a low level, respectively.

The CD4063BMS is supplied in these 16 lead outline packages:

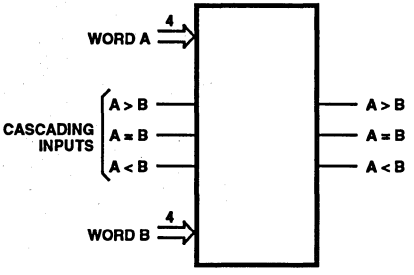
Braze Seal DIP	H4T
Frit Seal DIP	H1E
Ceramic Flatpack	H6W

Pinout

CD4063BMS
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3318

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance ..... θ_{ja} θ_{jc}
Ceramic DIP Package..... 80°C/W 20C/W
Flatpack Package ..... 20°C/W 20°C/W
Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K).....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES:

1. All voltages referenced to device GND. 100% testing being implemented
2. Go/No Go test with limit applied to inputs
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Comparator Input to Output	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	1250	ns
			10, 11	+125°C, -55°C	-	1688	ns
Propagation Delay Cascade Input to Output	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	1000	ns
			10, 11	+125°C, -55°C	-	1350	ns
Transition Time	TTHL	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. VDD = 5V, CL = 50pF, RL = 200K; input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-2.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Comparator Input to Output	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	500	ns
		VDD = 15V	1, 2, 3	+25°C	-	350	ns
Propagation Delay Cascade Input to Output	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	400	ns
		VDD = 15V	1, 2, 3	+25°C	-	280	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN		1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K; input TR, TF < 20ns

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS= -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V (Worst Case)	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES:

1. All voltages referenced to device GND.
2. VDD = 5V, CL = 50pF, RL = 200K; input TR, TF = 20ns
3. See Table 2 for +25°C limit.
4. Read and record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 5% parametric, 3% functional; cumulative for static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

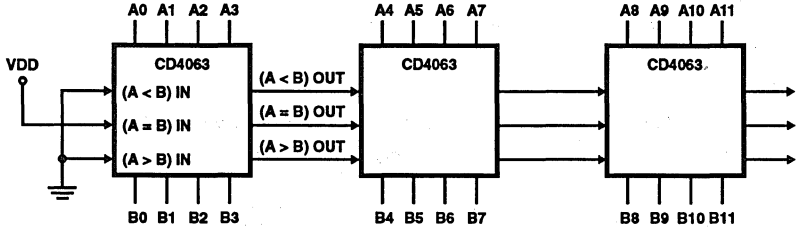
CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9, Deltas	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	5-7	1, 2, 4, 8-15	3, 16			
Static Burn-In 2 Note 1	5-7	3, 8	1, 2, 4, 9-16			
Dynamic Burn-In Note 1	-	1, 2, 4, 8, 10, 11, 13	3, 16	5-7	12, 15	9, 14
Irradiation Note 2	5-7	3, 8	1, 2, 4, 9-16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V



tP TOTAL = tP (COMPARE INPUTS) + 2 x tP (CASCADE INPUTS), AT VDD = 10V
(3 STAGES)
= 250 + (2 x 200) = 650ns (TYP.)

FIGURE 1. TYPICAL SPEED CHARACTERISTICS OF A 12-BIT COMPARATOR

Logic Diagram

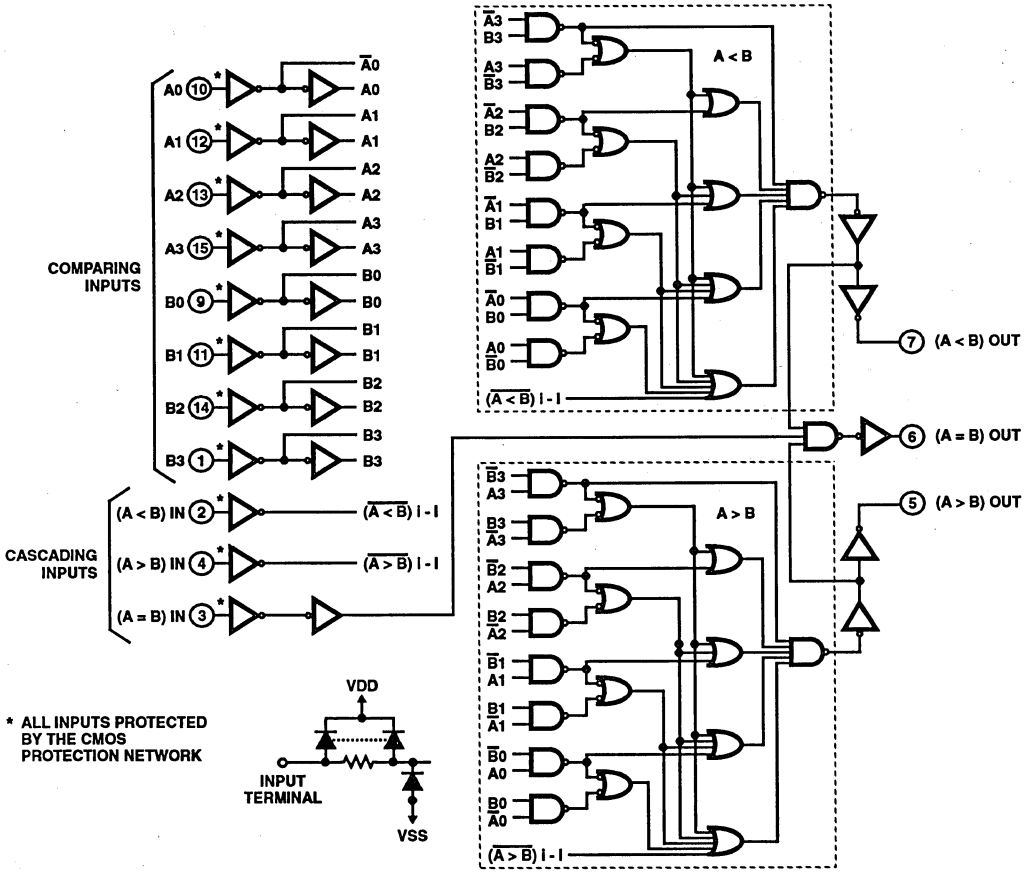


FIGURE 2. LOGIC DIAGRAM

TRUTH TABLE

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3, B3	A2, B2	A1, B1	A0, B0	A <B	A = B	A > B	A < B	A = B	A > B
A3 > B3	X	X	X	X	X	X	0	0	1
A3 = B3	A2 > B2	X	X	X	X	X	0	0	1
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	1	0	0	1	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	0	0	1	0	0
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	1	0	0
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	1	0	0
A3 = B3	A2 < B2	X	X	X	X	X	1	0	0
A3 < B3	X	X	X	X	X	X	1	0	0

X = Don't Care Logic 1 = High Level Logic 0 = Low Level

Typical Performance Characteristics

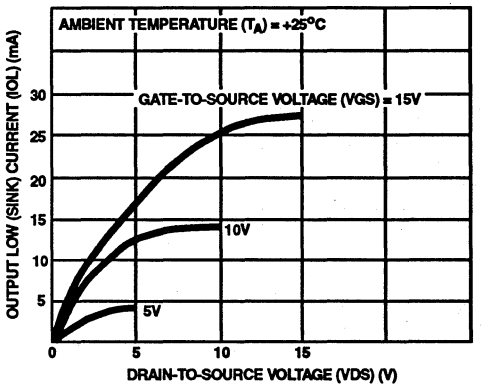


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

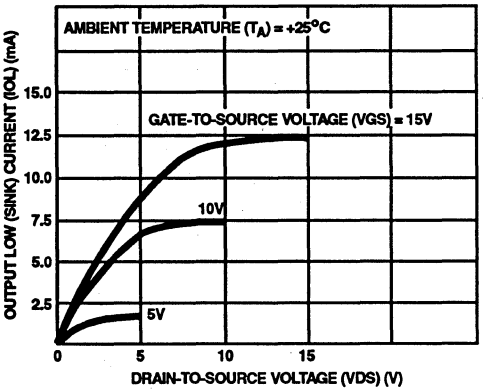


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT DRAIN CHARACTERISTICS

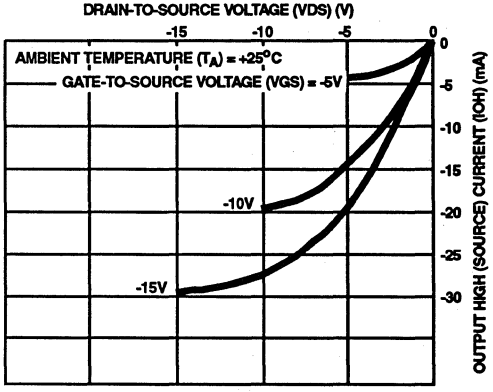


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

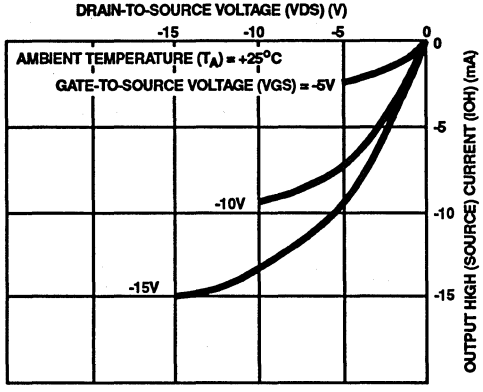


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

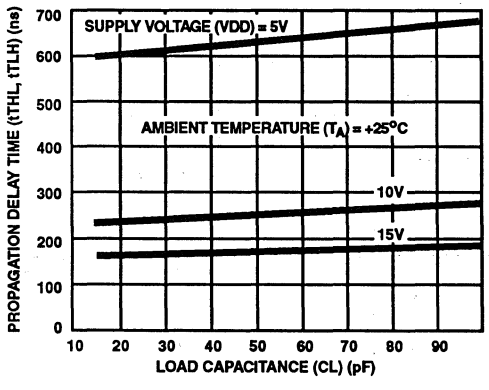


FIGURE 7. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE ("COMPARING INPUTS" TO OUTPUTS)

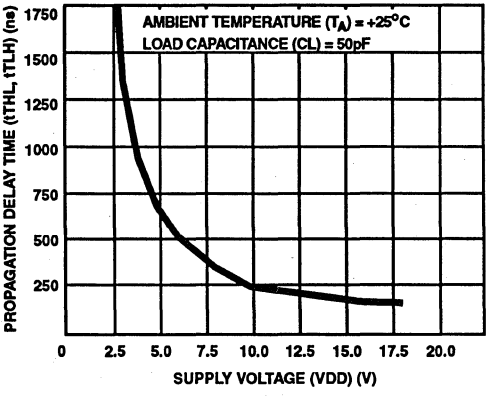


FIGURE 8. TYPICAL PROPAGATION DELAY TIME vs SUPPLY VOLTAGE ("COMPARING INPUTS" TO OUTPUTS)

Typical Performance Characteristics (Continued)

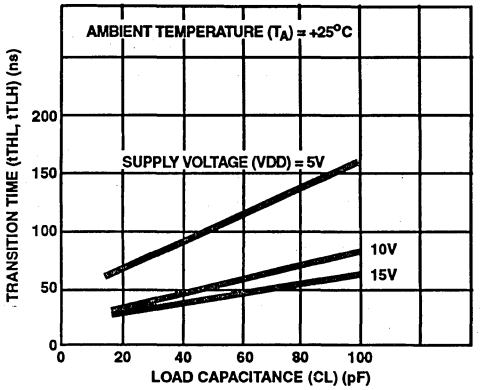


FIGURE 9. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

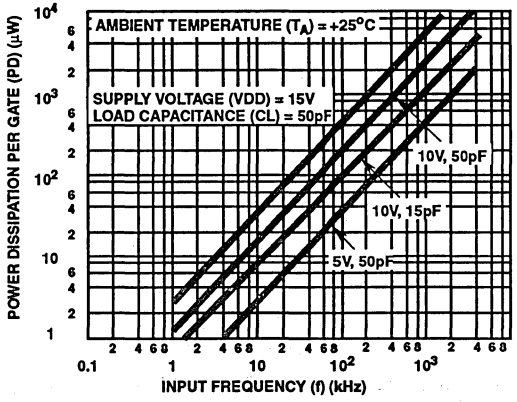
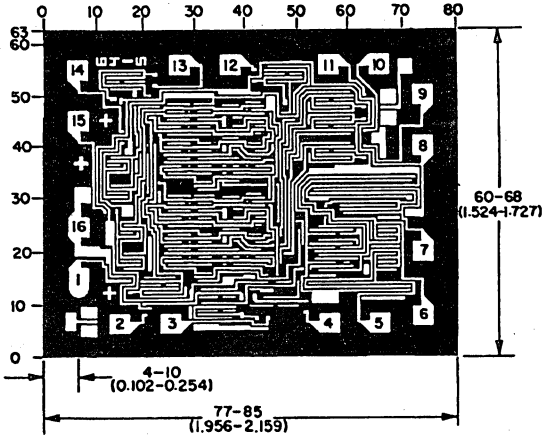


FIGURE 10. TYPICAL POWER DISSIPATION vs FREQUENCY

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4066BMS

December 1992

CMOS Quad Bilateral Switch

Features

- For Transmission or Multiplexing of Analog or Digital Signals
- High Voltage Types (20V Rating)
- 15V Digital or ±7.5V Peak-to-Peak Switching
- 125Ω Typical On-State Resistance for 15V Operation
- Switch On-State Resistance Matched to Within 5Ω Over 15V Signal Input Range
- On-State Resistance Flat Over Full Peak-to-Peak Signal Range
- High On/Off Output Voltage Ratio
  - 80dB Typ. at FIS = 10kHz, RL = 1kΩ
- High Degree of Linearity: <0.5% Distortion Typ. at FIS = 1kHz, VIS = 5Vp-p, VDD - VSS ≥ 10V, RL = 10kΩ
- Extremely Low Off-State Switch Leakage Resulting in Very Low Offset Current and High Effective Off-State Resistance: 10pA Typ. at VDD - VSS = 10V, T_A = +25°C
- Extremely High Control Input Impedance (Control Circuit Isolated from Signal Circuit): $10^{12}\Omega$ Typ.
- Low Crosstalk Between Switches: -50dB Typ. at FIS = 8MHz, RL = 1kΩ
- Matched Control Input to Signal Output Capacitance: Reduces Output Signal Transients
- Frequency Response, Switch on = 40MHz (Typ.)
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of "B" Series CMOS Devices"

Applications

- Analog Signal Switching/Multiplexing
  - Signal Gating
  - Squelch Control
  - Chopper
  - Modulator
  - Demodulator
  - Commutating Switch
- Digital Signal Switching/Multiplexing
- Transmission Gate Logic Implementation
- Analog to Digital & Digital to Analog Conversion
- Digital Control of Frequency, Impedance, Phase, and Analog Signal Gain

Description

CD4066BMS is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin for pin compatible with CD4016B, but exhibits a much lower on state resistance. In addition, the on-state resistance is relatively constant over the full input signal range.

The CD4066BMS consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased on or off simultaneously by the control signal. As shown in Figure 1, the well of the n channel device on each switch is either tied to the input when the switch is on or to VSS when the switch is off. This configuration eliminates the variation of the switch transistor threshold voltage with input signal, and thus keeps the on-state resistance low over the full operating signal range.

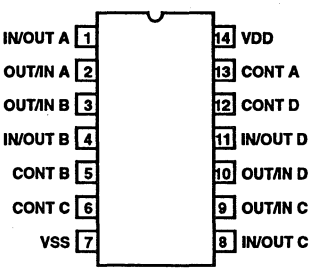
The advantages over single channel switches include peak input signal voltage swings equal to the full supply voltage, and more constant on-state impedance over the input signal range. For sample and hold applications, however, the CD4016B is recommended.

The CD4066BMS is supplied in these 14-lead outline packages:

Braze Seal DIP	H4Q
Frit Seal DIP	H1B
Ceramic Flatpack	H3W

Pinout

CD4066BMS
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3319**

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	0.5	µA
				2	+125°C	-	50	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	0.5	µA
Input Leakage Current	IIL	VC = VDD or GND		1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
				3	-55°C	-100	-	nA
Input Leakage Current	IIH	VC = VDD or GND		1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
				3	-55°C	-	100	nA
Input/Output Leakage Current (Switch OFF)	IOZL	VC = 0V, VIS = 18V, VOS = 0V, VIS = 0V, VOS = 18V	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
	IOZH		VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
On Resistance	RON5	VC = VDD, RL = 10kW returned to VDD - VSS/2 VIS = VSS to VDD	VDD = 5V	1	+25°C	1050	-	Ω
	RON10		VDD = 10V	1	+25°C	400	-	Ω
	RON15		VDD = 15V	1	+25°C	240	-	Ω
On Resistance	RON5	VDD = 5V		1, 2	+125°C	-	1300	Ω
					-55°C	-	800	Ω
On Resistance	RON10	VDD = 10V		1, 2	+125°C	-	550	Ω
					-55°C	-	310	Ω
On Resistance	RON15	VDD = 15V		1, 2	+125°C	-	320	Ω
					-55°C	-	220	Ω
Functional (Note 3)	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Switch Threshold RL = 100k to VDD	SWTHRH5	VDD = 5V, VC = 1.5V, VIS = GND		1, 2, 3	+25°C, +125°C, -55°C	4.1	-	V
	SWTHRH15	VDD = 15V, VC = 2V, VIS = GND		1, 2, 3	+25°C, +125°C, -55°C	14.1	-	V
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Control Input Low Voltage (Note 2) |IIISI < 10µa, VIS = VSS, VOS = VDD and VIS = VDD, VOS = VSS	VILC5	VDD = 5V	1, 2, 3	+25°C, +125°C, -55°C	-	1	V
	VILC15	VDD = 15V	1, 2, 3	+25°C, +125°C, -55°C	-	2	V
Control Input High Voltage (Note 2, Figure 2) VIS = VSS and VIS = VDD	VIHC	VDD = 5V, |IIISI = .51mA, 4.6V < VOS < 0.4V	1	+25°C	3.5	-	V
		VDD = 5V, |IIISI = .36mA, 4.6V < VOS < 0.4V	2	+125°C	3.5	-	V
		VDD = 5V, |IIISI = .64mA, 4.6V < VOS < 0.4V	3	-55°C	3.5	-	V
	VIHC	VDD = 15V, |IIISI = 3.4mA, 13.5V < VOS <1.5V	1	+25°C	11	-	V
		VDD = 15V, |IIISI = 2.4mA, 13.5V < VOS < 1.5V	2	+125°C	11	-	V
		VDD = 15V, |IIISI = 4.2mA, 13.5V < VOS <1.5V	3	-55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. VDD = 2.8V/3.0V, RL = 100K to VDD
VDD = 20V/18V, RL = 10K to VDD

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Signal Input to Signal Output	TPLH TPHL	VC = VDD = 5V, VSS = GND (Notes 2, 3)	9	+25°C	-	40	ns
			10, 11	+125°C, -55°C	-	54	ns
Propagation Delay Turn-On, Turn-Off	TPHZ/ZH TPLZ/ZL	VIS = VDD = 5V (Notes 1, 2)	9	+25°C	-	70	ns
			10, 11	+125°C, -55°C	-	95	ns

NOTES:

1. CL = 50pF, RL = 1K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.25	µA
				+125°C	-	7.5	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	15	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	30	µA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Control Input Low Voltage IIISI < 10µa, VIS = VSS, VOS = VDD and VIS = VDD, VOS = VSS	VILC10	VDD = 10V	1, 2	+25°C, +125°C, -55°C	-	2	V
Control Input High Voltage (See Figure 2)	VIHC10	VDD = 10V, VIS = VDD or GND	2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Signal Input to Signal Output	TPLH TPHL	VDD = 10V	1, 2, 3	+25°C	-	20	ns
		VDD = 15V	1, 2, 3	+25°C	-	15	ns
Propagation Delay Turn-On, Turn-Off	TPHZ/ZH TPLZ/ZL	VDD = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V	1, 2, 3	+25°C	-	30	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - SSI	IDD	±0.1µA
ON Resistance	RONDEL10	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

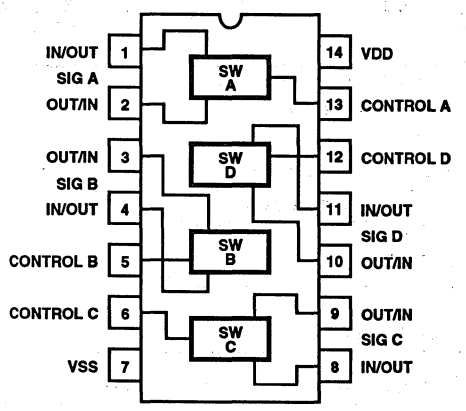
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	2, 3, 9, 10	1, 4-8, 11-13	14			
Static Burn-In 2 (Note 1)	2, 3, 9, 10	7	1, 4-6, 8, 11-14			
Dynamic Burn-In (Note 1)	-	7	14	2, 3, 9, 10	5, 6, 12, 13	1, 4, 8, 11
Irradiation (Note 2)	2, 3, 9, 10	7	1, 4-6, 8, 11-14			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Functional Diagram



TRUTH TABLE EACH SWITCH		
INPUT		OUTPUT
VC	VIS	VOS
1	0	0
1	1	1
0	0	Open
0	1	Open

Positive Logic: Switch ON VC = "1"
Switch OFF VC = "0"

Schematic

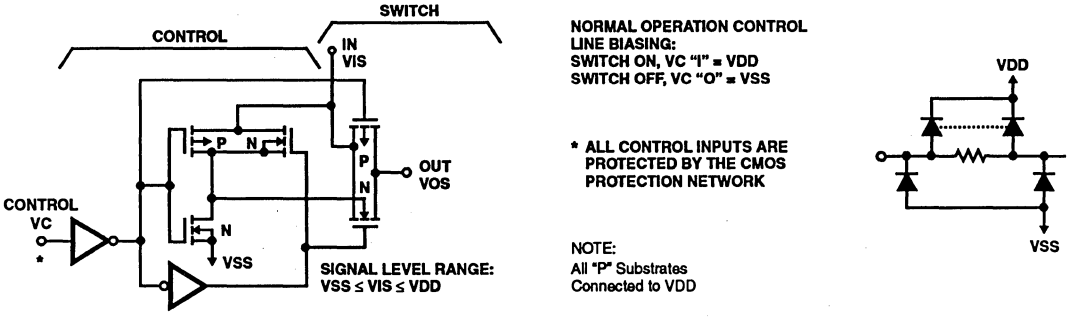


FIGURE 1. SCHEMATIC DIAGRAM OF 1 OF 4 IDENTICAL SWITCHES AND ITS ASSOCIATED CONTROL CIRCUITRY

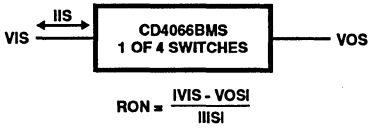


FIGURE 2. DETERMINATION OF RON AS A TEST CONDITION FOR CONTROL INPUT HIGH VOLTAGE (VIHC) SPECIFICATION

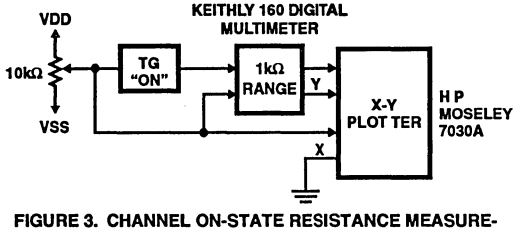


FIGURE 3. CHANNEL ON-STATE RESISTANCE MEASUREMENT CIRCUIT

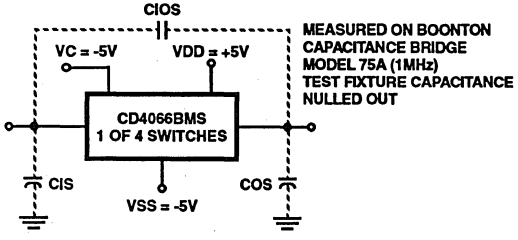


FIGURE 4. CAPACITANCE TEST CIRCUIT

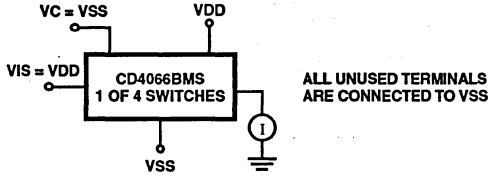


FIGURE 5. OFF SWITCH INPUT OR OUTPUT LEAKAGE

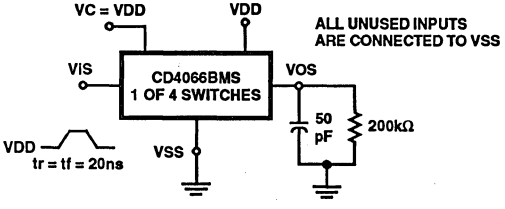


FIGURE 6. PROPAGATION DELAY TIME SIGNAL INPUT (VIS) TO SIGNAL OUTPUT (VOS)

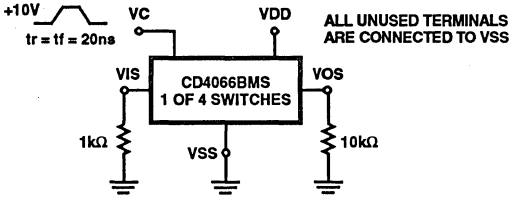


FIGURE 7. CROSSTALK CONTROL INPUT TO SIGNAL OUTPUT

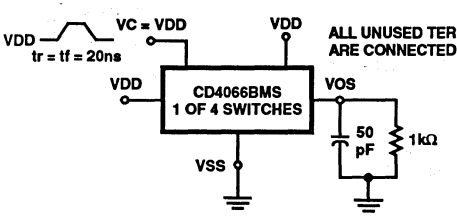


FIGURE 8. PROPAGATION DELAY TPLH, TPHL CONTROL SIGNAL OUTPUT. DELAY IS MEASURED AT VOS LEVEL OF +10% FROM GROUND (TURN ON) OR ON-STATE OUTPUT LEVEL (TURN OFF).

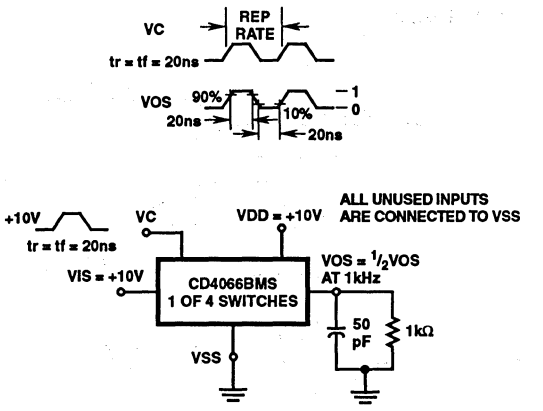


FIGURE 9. MAXIMUM ALLOWABLE CONTROL INPUT REPETITION RATE

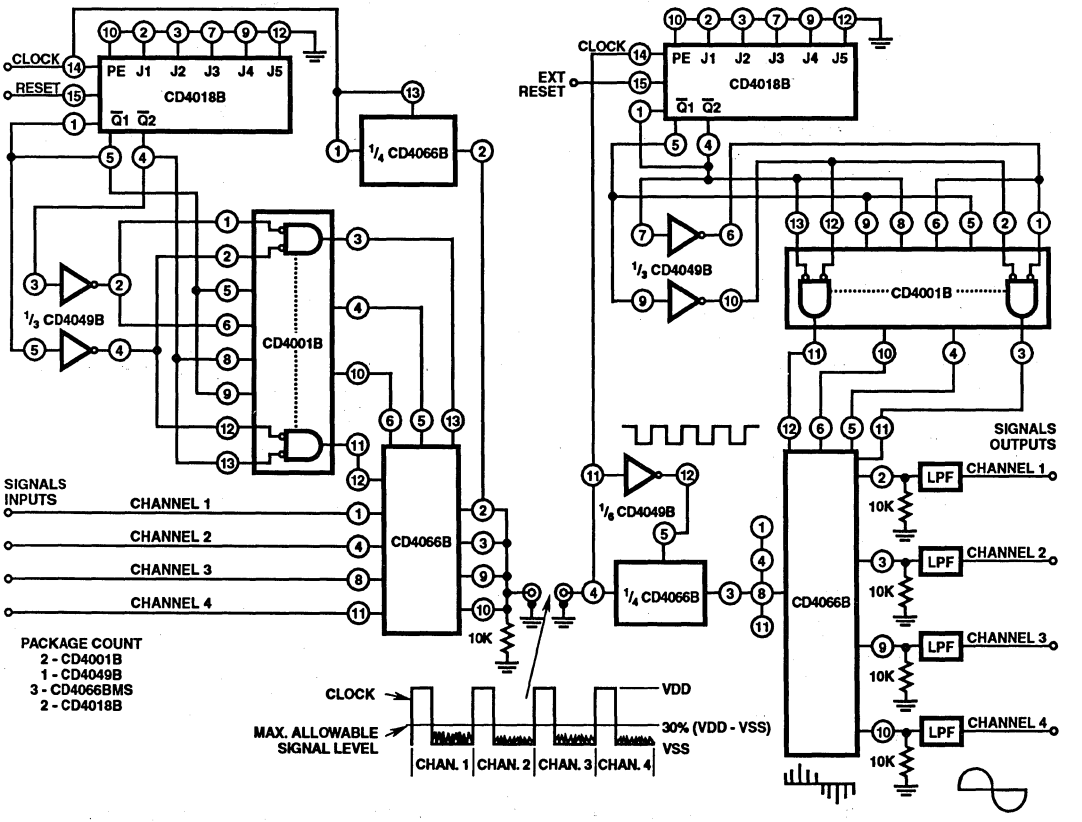


FIGURE 10. 4 CHANNEL PAM MULTIPLEX SYSTEM DIAGRAM

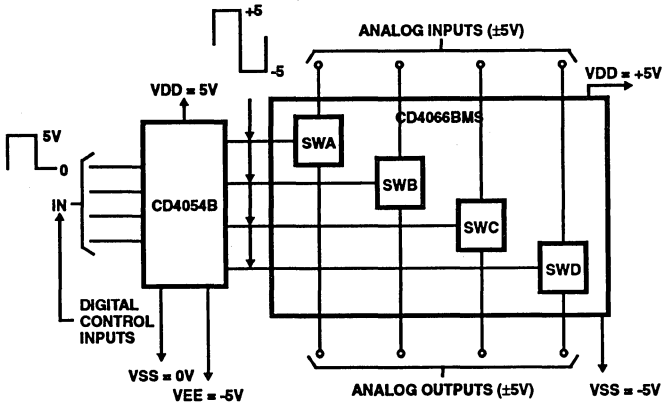


FIGURE 11. BIDIRECTIONAL SIGNAL TRANSMISSION VIA DIGITAL CONTROL LOGIC

Typical Performance Characteristics

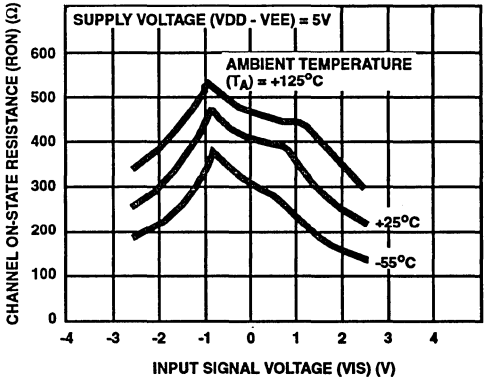


FIGURE 12. TYPICAL ON-STATE RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

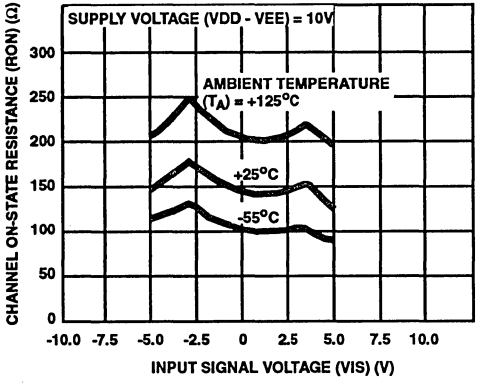


FIGURE 13. TYPICAL ON-STATE vs INPUT SIGNAL VOLTAGE (ALL TYPES).

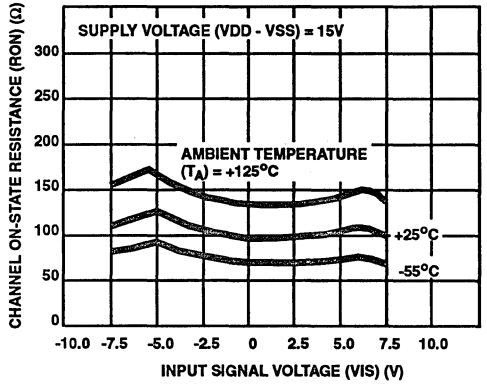


FIGURE 14. TYPICAL ON-STATE RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

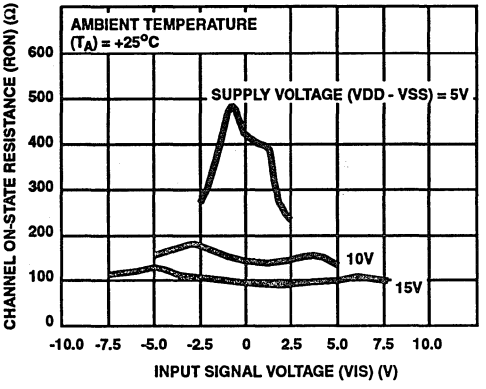


FIGURE 15. ON-STATE RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

Typical Performance Characteristics (Continued)

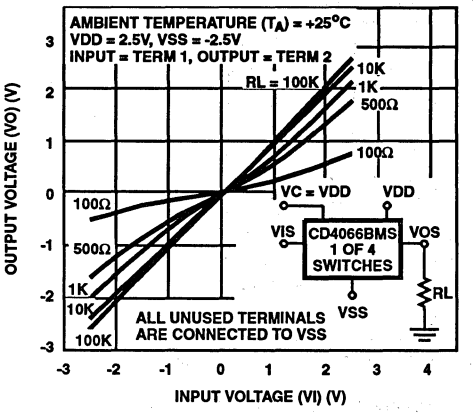


FIGURE 16. TYPICAL ON CHARACTERISTICS FOR 1 OF 4 CHANNELS

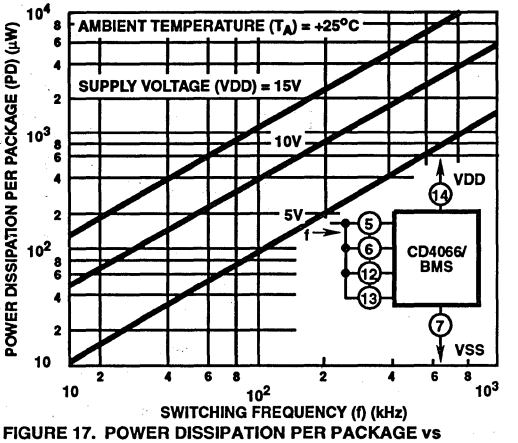
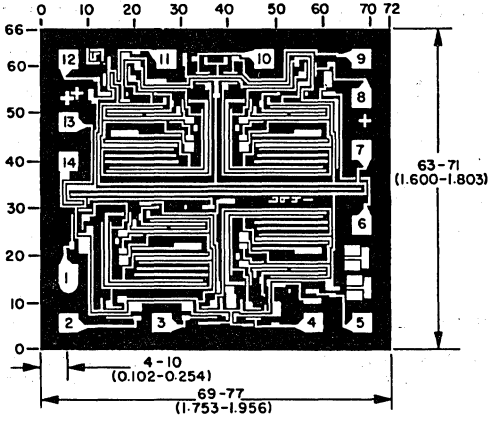


FIGURE 17. POWER DISSIPATION PER PACKAGE vs SWITCHING FREQUENCY

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Special Considerations

In applications that employ separate power sources to drive VDD and the signal inputs, the VDD current capability should exceed VDD/RL (RL = effective external load of the four CD4066B bilateral switches). This provision avoids any permanent current flow or clamp action on the VDD supply when power is applied or removed from the CD4066B.

In certain applications, the external load-resistor current may include both VDD and signal line components. To avoid drawing VDD current when switch current flows into terminals 1, 4, 8 or 11 the voltage drop across the bidirectional switch must not exceed 0.8 volts (calculated from RON values shown).

No VDD current will flow through RL if the switch current flows into terminals 2, 3, 9, or 10.

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4067BMS
CD4097BMS

CMOS Analog Multiplexers/Demultiplexers

December 1992

Features

- High Voltage Types (20V Rating)
- CD4067BMS Single 16 Channel Multiplexer/Demultiplexer
- CD4097BMS Differential 8 Channel Multiplexer/Demultiplexer
- Low ON Resistance: 125Ω (typ) Over 15Vp-p Signal Input Range for VDD - VSS = 15V
- High OFF Resistance: Channel Leakage of ±10pA (typ) at VDD - VSS = 18V
- Matched Switch Characteristics: RON = 5Ω (typ) for VDD - VSS = 15V
- Very Low Quiescent Power Dissipation Under All Digital Control Input and Supply Conditions: 0.2μW (typ) at VDD - VSS = 10V
- Binary Address Decoding on Chip
- 5V, 10V and 15V Parametric Ratings
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Standardized Symmetrical Output Characteristics

Applications

- Analog and Digital Multiplexing and Demultiplexing
- A/D and D/A Conversion
- Signal Gating

* When these devices are used as demultiplexers the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminals are the inputs.

Description

CD4067BMS and CD4097BMS CMOS analog multiplexers/demultiplexers* are digitally controlled analog switches having low ON Impedance, low OFF leakage current, and internal address decoding. In addition, the ON resistance is relatively constant over the full input-signal range.

The CD4067BMS is a 16 channel multiplexer with four binary control inputs, A, B, C, D and an inhibit input, arranged so that any combination of the inputs selects one switch.

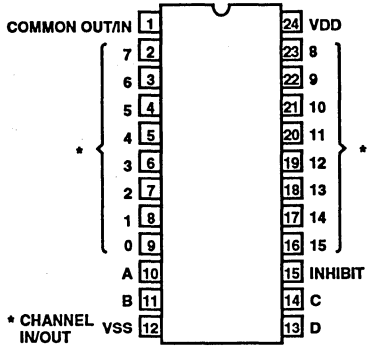
The CD4097BMS is a differential 8 channel multiplexer having three binary control inputs A, B, C and an inhibit input. The inputs permit selection of one of eight pairs of switches. A logic "1" present at the inhibit input turns all channels off.

The CD4067BMS and CD4097BMS are supplied in these 24 lead outline packages:

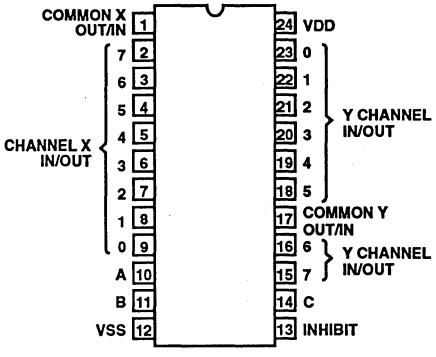
Braze Seal DIP	*H4V	†H6M
Frit Seal DIP	*H1Z	†HFN
Ceramic Flatpack	*H4P	†H4P
*CD4067B Only	†CD4097B	

Pinout

CD4067BMS
TOP VIEW



CD4097BMS
TOP VIEW



7 LOGIC

File Number 3190

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range.....-55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG).....-65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K).....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature .....+175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
ON-State Resistance RL = 10K Returned to VDD - VSS/2	RON	VDD = 5V VIS = VSS to VDD		1	+25°C	-	1050	Ω
				2	+125°C	-	1300	Ω
				3	-55°C	-	800	Ω
		VDD = 10V VIS = VSS to VDD		1	+25°C	-	400	Ω
				2	+125°C	-	500	Ω
				3	-55°C	-	310	Ω
		VDD = 15V VIS = VSS to VDD		1	+25°C	-	240	Ω
				2	+125°C	-	320	Ω
				3	-55°C	-	220	Ω
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional (Note 4)	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH> VDD/2	VOL< VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V = VIS Thru 1K VEE = VSS RL = 1K to VSS IISSI < 2µA on all OFF Channels		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH			1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V = VIS Thru 1K VEE = VSS RL = 1K to VSS IISSI < 2µA on all OFF Channels		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH			1, 2, 3	+25°C, +125°C, -55°C	11	-	V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
OFF Channel Leakage Any Channel OFF or All Channels OFF (Common OUT/IN)	IOZL	VOUT = 0V	VDD = 20V	1	+25°C	-0.1	-	µA
				2	+125°C	-1.0	-	µA
			VDD = 18V	3	-55°C	-0.1	-	µA
	IOZH	VOUT = VDD	VDD = 20V	1	+25°C	-	0.1	µA
				2	+125°C	-	1.0	µA
			VDD = 18V	3	-55°C	-	0.1	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.
4. VDD = 2.8/3.0V, RL = 200K
VDD = 20V/18V, RL = 10K - 25K

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay (Signal In to Output)	TPHL TPLH	VDD = 5V, VIN = VDD or GND (Notes 1, 2)	9	+25°C	-	60	ns
			10, 11	+125°C, -55°C	-	81	ns
Propagation Delay Address or Inhibit to Signal Out. (Channel Turning On)	TPZH TPZL	VDD = 5V, VIN = VDD or GND (Notes 2, 3)	9	+25°C	-	650	ns
			10, 11	+125°C, -55°C	-	878	ns

NOTES:
1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.
3. CL = 50pF, RL = 10K, Input TR, TF < 20ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS		NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND		1, 2	-55°C, +25°C	-	5	µA
					+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND		1, 2	-55°C, +25°C	-	10	µA
					+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND		1, 2	-55°C, +25°C	-	10	µA
					+125°C	-	600	µA
Input Voltage Low	VIL	VDD = VIS = 10V VEE = VSS RL = 1K to VSS IIS < 2µA ON OFF Channel		1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH			1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Address or Inhibit to Signal Out. (Channel Turning On)	TPZH TPZL	VDD = 10V		1, 2, 4	+25°C	-	270	ns
		VDD = 15V		1, 2, 4	+25°C	-	190	ns
Propagation Delay Signal In to Output	TPHL TPLH	VDD = 10V	VIS = VDD or GND	1, 2, 3	+25°C	-	30	ns
		VDD = 15V		1, 2, 3	+25°C	-	20	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Address or Inhibit to Signal Out (Channel Turning Off)	TPHZ TPLZ	VDD = 5V	1, 2, 5	+25°C	-	440	ns
		VDD = 10V	1, 2, 5	+25°C	-	180	ns
		VDD = 15V	1, 2, 5	+25°C	-	130	ns
Input Capacitance	CIN	Any Address or Inhibit	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. CL = 50pF, RL = 10K, Input TR, TF < 20ns.
5. CL = 50pF, RL = 300Ω, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
ON Resistance	RONDEL10	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

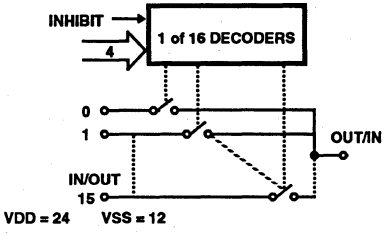
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
PART NUMBER CD4067BMS						
Static Burn-In 1 Note 1	1	2 - 23	24			
Static Burn-In 2 Note 1	1	12	2 - 11, 13 - 24			
Dynamic Burn-In Note 1	-	12, 15	24	1	2 - 9, 16 - 23	10, 11, 13, 14 (Note 3)
Irradiation Note 2	1	12	2 - 11, 13 - 24			
PART NUMBER CD4097BMS						
Static Burn-In 1 Note 1	1, 17	2 - 16, 18 - 23	24			
Static Burn-In 2 Note 1	1, 17	12	2 - 11, 13 - 16, 18 - 24			
Dynamic Burn-In Note 1	-	12, 13	24	1, 17	2 - 9, 15, 16, 18 - 23	10, 11, 14 (Note 4)
Irradiation Note 2	1, 17	12	2 - 11, 13 - 16, 18 - 24			

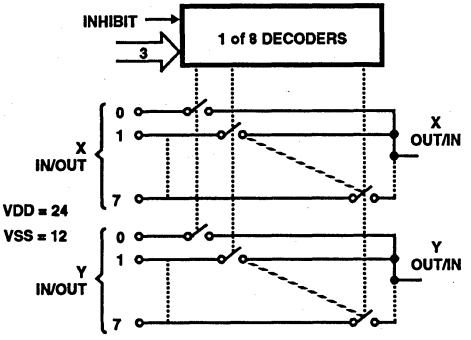
NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V
3. Pin 10 is at 14kHz, Pin 11 is at 7kHz, Pin 13 is at 1.7kHz, Pin 14 is at 3.5kHz
4. Pin 10 is at 14kHz, Pin 11 is at 7kHz, Pin 14 is at 3.5kHZ

Functional Diagram



CD4067



CD4097

CD4067 TRUTH TABLE

A	B	C	D	Inh	SELECTED CHANNEL
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

CD4097 TRUTH TABLE

A	B	C	Inh	SELECTED CHANNEL
X	X	X	1	None
0	0	0	0	0X, 0Y
1	0	0	0	1X, 1Y
0	1	0	0	2X, 2Y
1	1	0	0	3X, 3Y
0	0	1	0	4X, 4Y
1	0	1	0	5X, 5Y
0	1	1	0	6X, 6Y
1	1	1	0	7X, 7Y

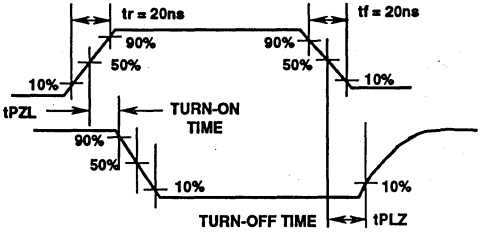


FIGURE 1. WAVEFORM CHANNEL BEING TURNED ON, OFF

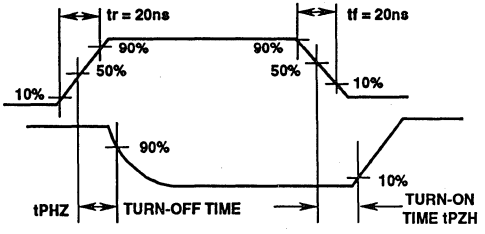


FIGURE 2. PROPAGATION DELAY WAVEFORM, CHANNEL BEING TURNED OFF, ON

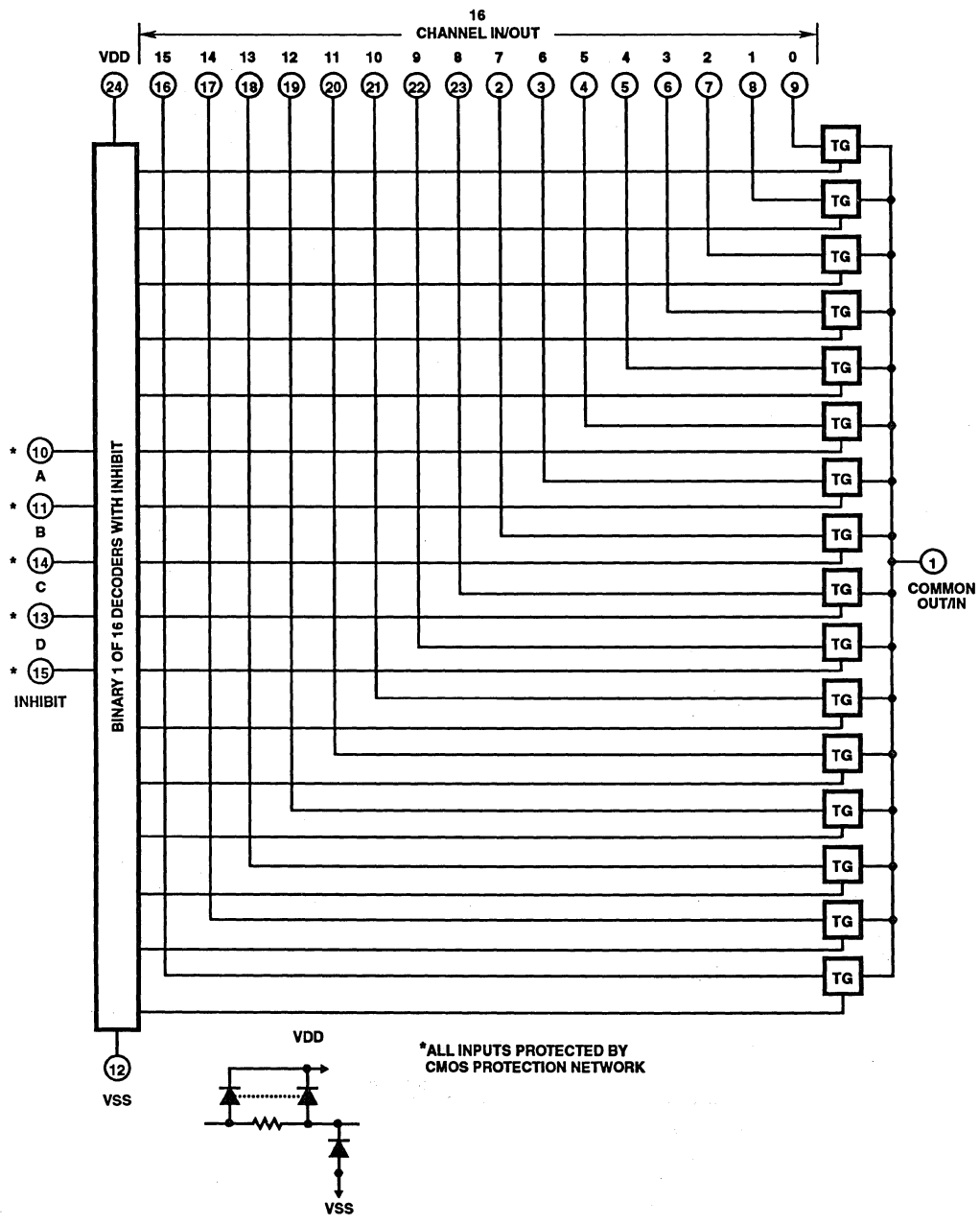


FIGURE 3. CD4067BMS LOGIC DIAGRAM

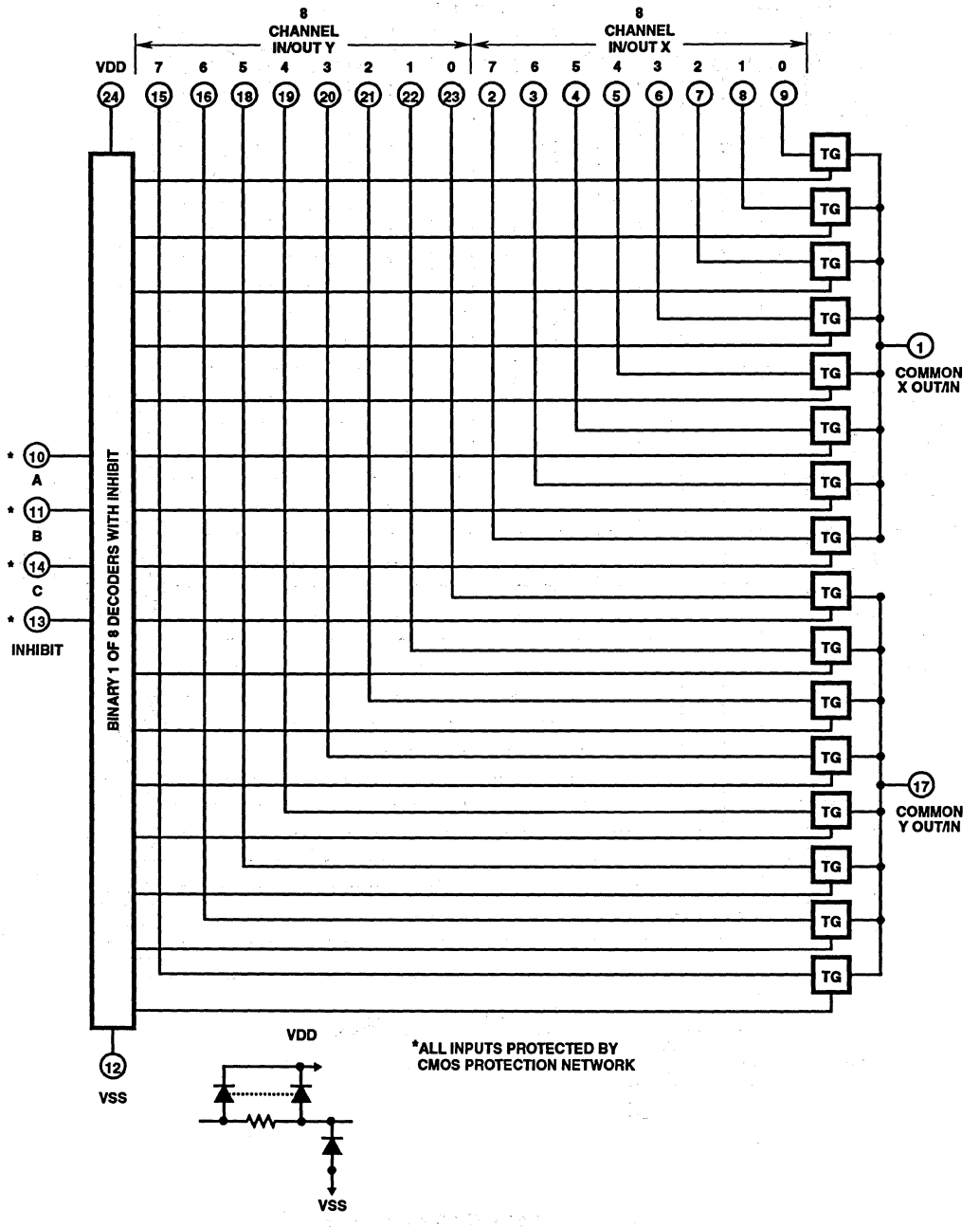


FIGURE 4. CD4097BMS LOGIC DIAGRAM

Typical Performance Characteristics

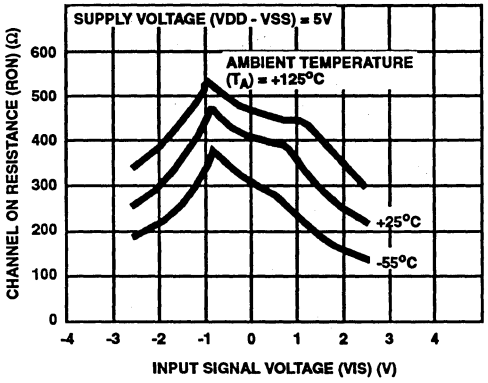


FIGURE 5. TYPICAL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

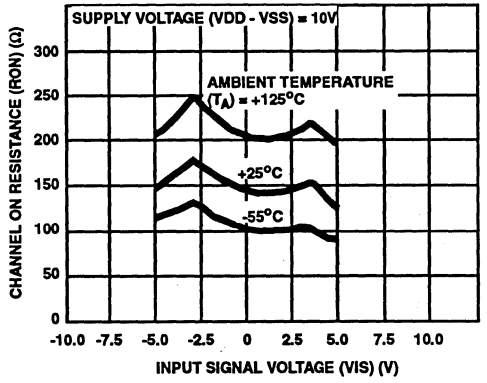


FIGURE 6. TYPICAL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

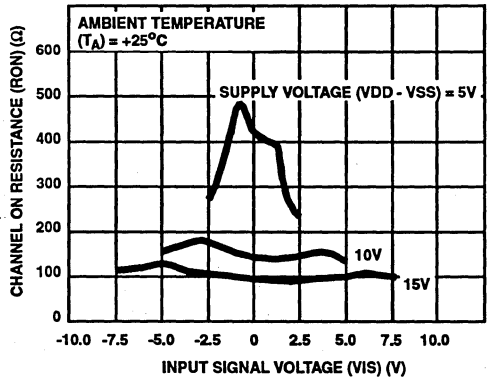


FIGURE 7. TYPICAL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

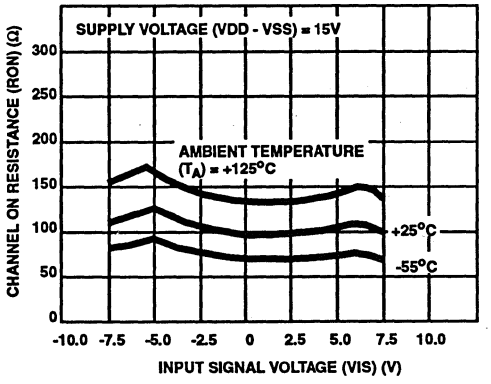
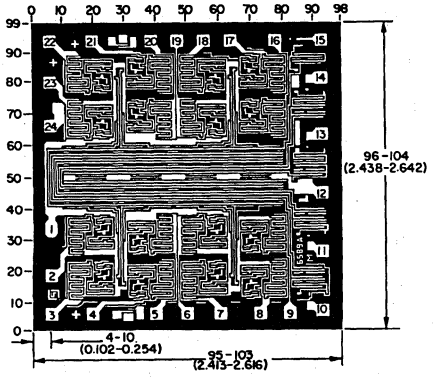
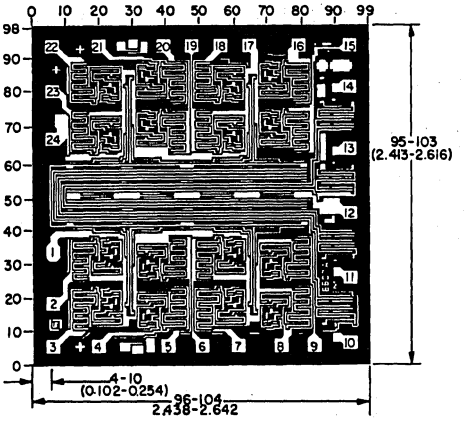


FIGURE 8. TYPICAL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

Chip Dimensions and Pad Layouts



CD4067BMSH



CD4097BMSH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

Special Considerations

In applications where separate power sources are used to drive VDD and the signal inputs, the VDD current capability should exceed VDD/RL (RL = effective external load). This provision avoids permanent current flow or clamp action on the VDD supply when power is applied or removed from the CD4067BMS or CD4097BMS.

When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also when a channel is turned on or off by an address input, there is a momentary conductive path from the channel to VSS, which will dump some charge from any capacitor connected to the input or output of the channel. The inhibit input turning on a channel will similarly dump some charge to VSS.

The amount of charge dumped is mostly a function of the signal level above VSS. Typically, at VDD - VSS = 10V, a 100pF capacitor connected to the input or output of the channel will lose 3 to 4% of its voltage at the moment the channel turns on or off. This loss of voltage is essentially independent of the address or inhibit signal transition time, if the transition time is less than 1 - 2μs. When the inhibit signal turns a channel off, there is no charge dumping to VSS. Rather, there is a slight rise in the channel voltage level (65mV typ.) due to capacitive coupling from inhibit input to channel input or output. Address inputs also couple some voltage steps onto the channel signal levels.

In certain applications, the external load resistor current may include both VDD and signal-line components. To avoid drawing VDD current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from RON values shown in ELECTRICAL CHARACTERISTICS CHART - Table 1). no VDD current will flow through RL if the switch current flows into terminal 1 on the CD4067BMS, terminals 1 and 17 on the CD4097BMS.

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

CD4068BMS

CMOS 8 Input NAND/AND Gate

December 1992

Features

- High Voltage Type (20V Rating)
- Medium Speed Operation
  - TPHL, TPLH = 75ns (Typ.) at VDD = 10V
- Buffered Inputs and Outputs
- 5V, 10V and 15V Parametric Ratings
- Standardized Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Description

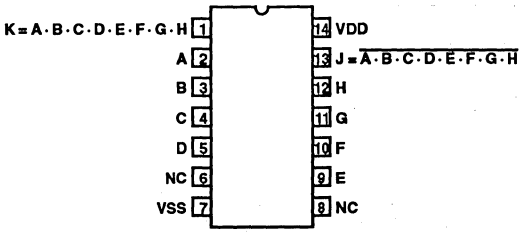
CD4068BMS NAND/AND gate provides the system designer with direct implementation of the positive logic 8 Input NAND and AND functions and supplements the existing family of CMOS gates.

The CD4068BMS is supplied in these 14 lead outline packages:

Braze Seal DIP	H4H
Frit Seal DIP	H1B
Ceramic Flatpack	H3W

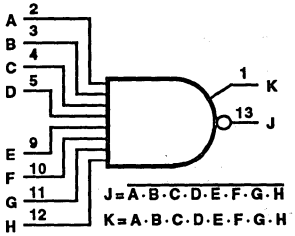
Pinout

CD4068BMS
TOP VIEW



NC = NO CONNECTION

Functional Diagram



VDD = 14
VSS = 7
6, 8 = NO CONNECTION

Logic Diagram

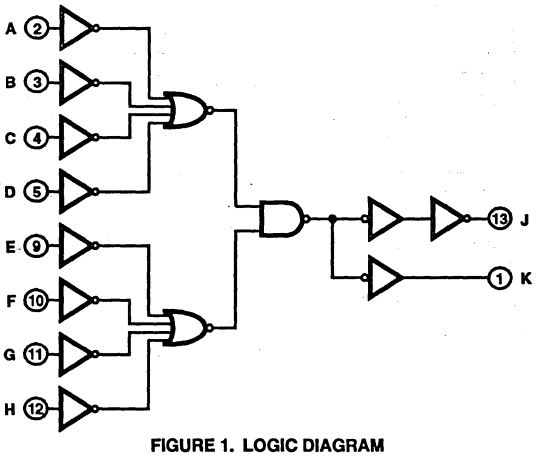


FIGURE 1. LOGIC DIAGRAM

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	0.5	µA
				2	+125°C	-	50	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	0.5	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTES 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	300	ns
			10, 11	+125°C, -55°C	-	405	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.25	µA
				+125°C	-	7.5	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	15	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	30	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-2.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	150	ns
		VDD = 15V	1, 2, 3	+25°C	-	110	ns
Transition Time	TTHL	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	2.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - SSI	IDD	±0.1µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	1, 6, 8, 13	2-5, 7, 9-12	14			
Static Burn-In 2 Note 1	1, 6, 8, 13	7	2-5, 9-12, 14			
Dynamic Burn-In Note 1	6, 8	7	14	1, 13	2-5, 9-12	
Irradiation Note 2	1, 6, 8, 13	7	2-5, 9-12, 14			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Schematic

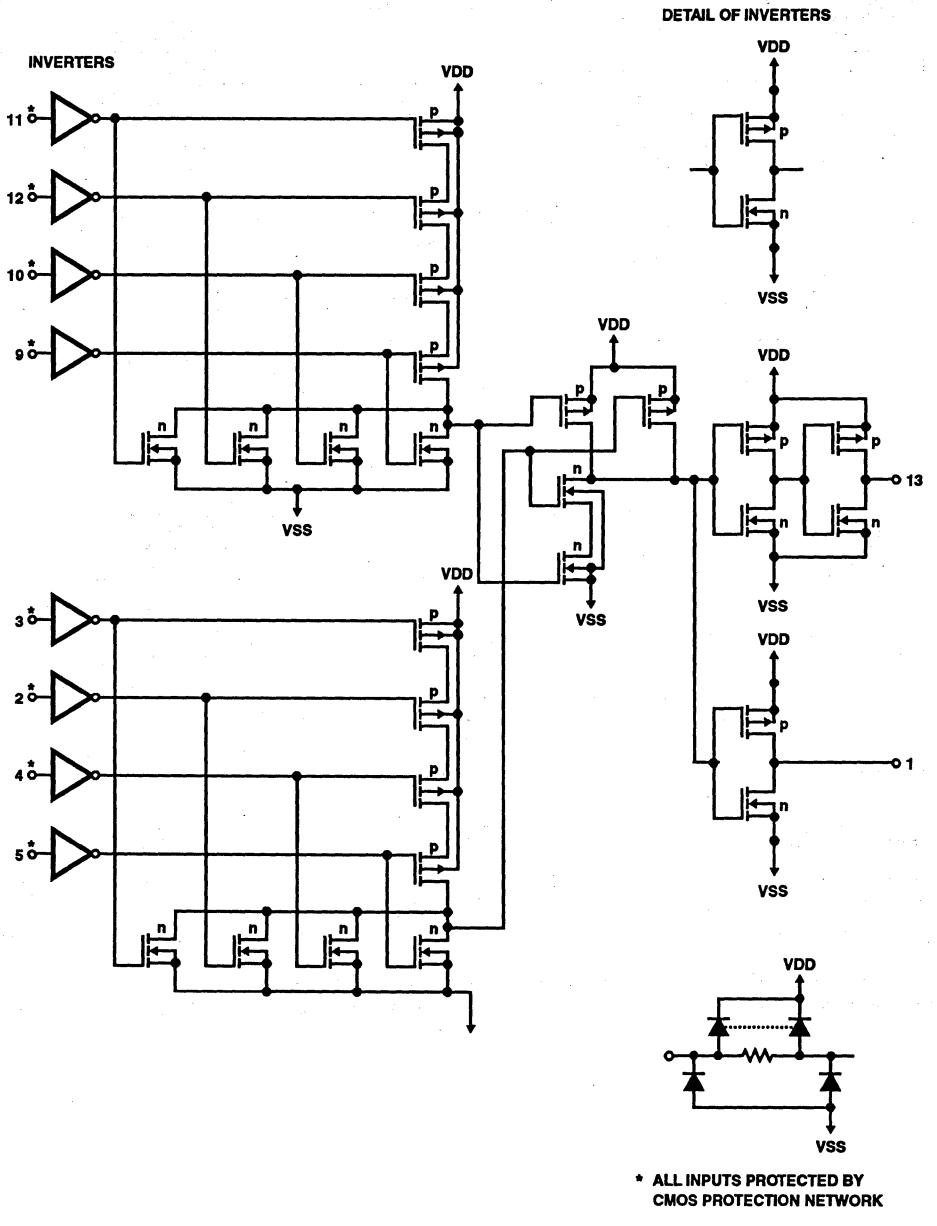


FIGURE 2. SCHEMATIC DIAGRAM

Typical Performance Characteristics

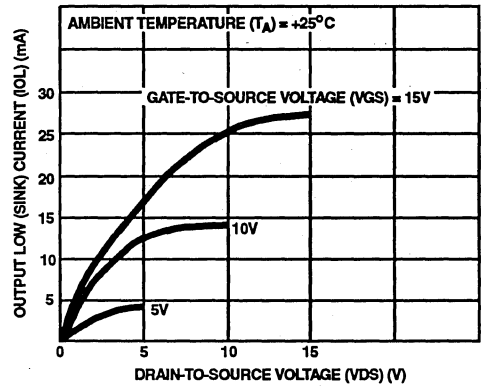


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

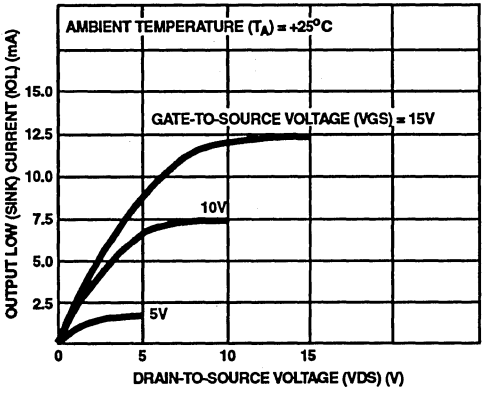


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

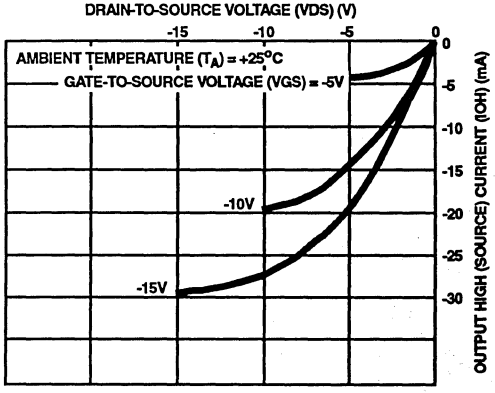


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

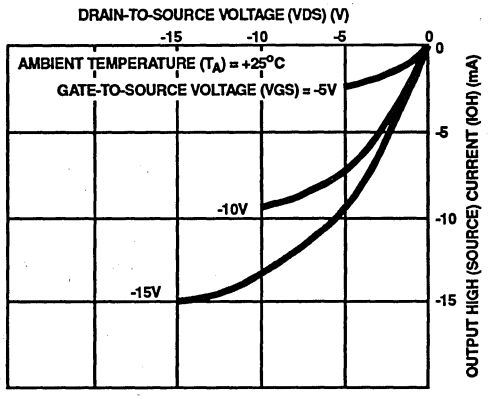


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

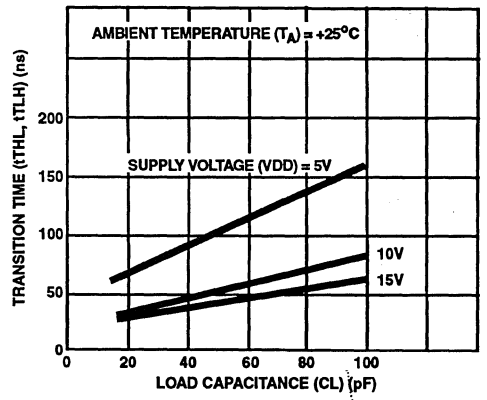


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

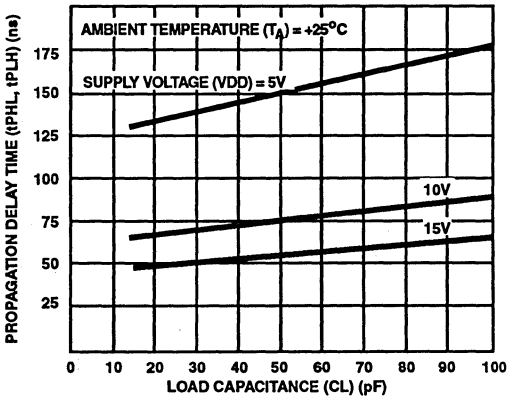


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

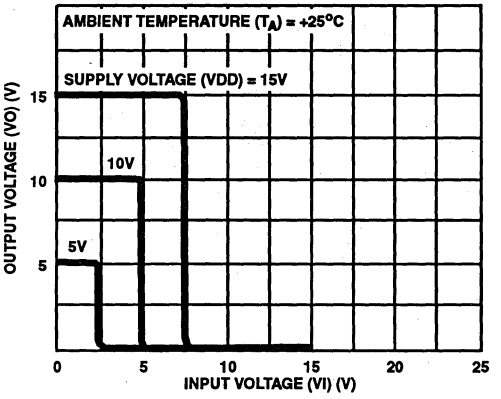


FIGURE 9. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS (NAND OUTPUT)

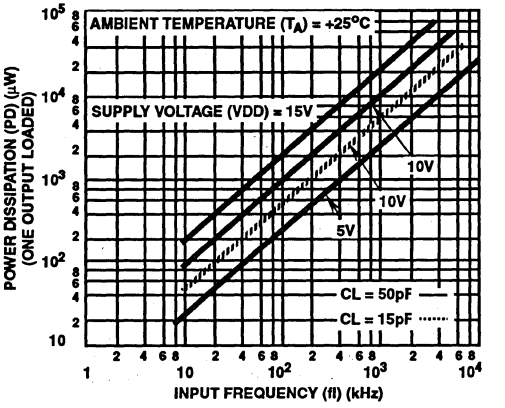
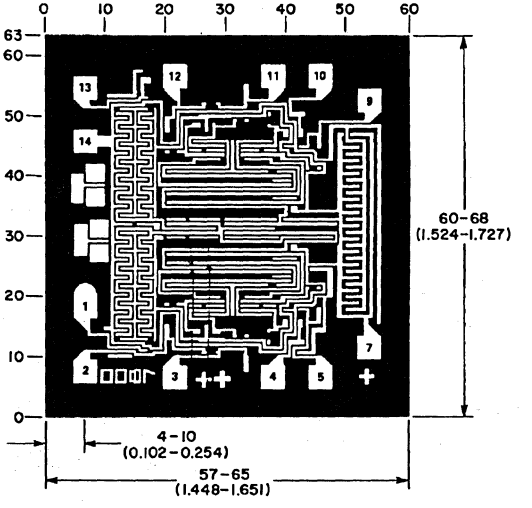


FIGURE 10. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF FREQUENCY

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

CD4069UBMS

CMOS Hex Inverter

December 1992

Features

- High Voltage Types (20V Rating)
- Standardized Symmetrical Output Characteristics
- Medium Speed Operation: tPHL, tPLH = 30ns (typ) at 10V
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Logic Inversion
- Pulse Shaping
- Oscillators
- High-Input-Impedance Amplifiers

Description

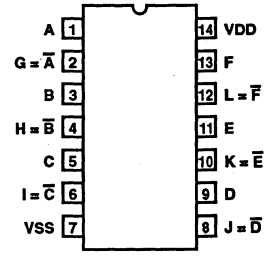
CD4069UBMS types consist of six CMOS inverter circuits. These devices are intended for all general-purpose inverter applications where the medium-power TTL-drive and logic-level conversion capabilities of circuits such as the CD4009 and CD4049 Hex Inverter/Buffers are not required.

The CD4069UBMS is supplied in these 14 lead outline packages:

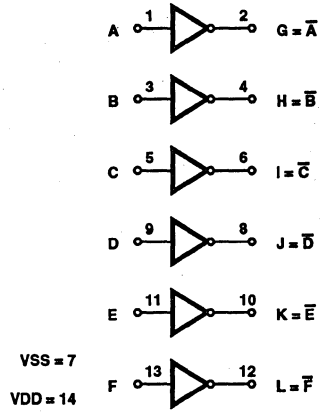
Braze Seal DIP	H4H
Frit Seal DIP	H1B
Ceramic Flatpack	H3W

Pinout

CD4069UBMS
TOP VIEW



Functional Diagram



Schematic Diagram

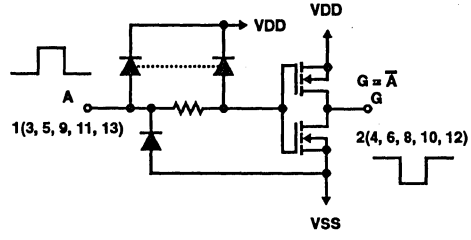


FIGURE 1. SCHEMATIC DIAGRAM OF 1 OF 6 IDENTICAL INVERTERS

7 LOGIC

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	0.5	µA
				2	+125°C	-	50	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	0.5	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.0	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	4.0	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	2.5	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	12.5	-	V

NOTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTES 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	110	ns
			10, 11	+125°C, -55°C	-	149	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.25	µA
				+125°C	-	7.5	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	15	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	30	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-2.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	2	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	8	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	60	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	15	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	2.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - SSI	IDD	±0.1µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Final Test	100% 5004	2, 3, 8A, 8B, 10, 11	

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	2, 4, 6, 8, 10, 12	1, 3, 5, 7, 9, 11, 13	14			
Static Burn-In 2 (Note 1)	2, 4, 6, 8, 10, 12	7	1, 3, 5, 9, 11, 13, 14			
Dynamic Burn-In (Note 1)	-	7	14	2, 4, 6, 8, 10, 12	1, 3, 5, 9, 11, 13	
Irradiation (Note 2)	2, 4, 6, 8, 10, 12	7	1, 3, 5, 9, 11, 13, 14			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Typical Performance Characteristics

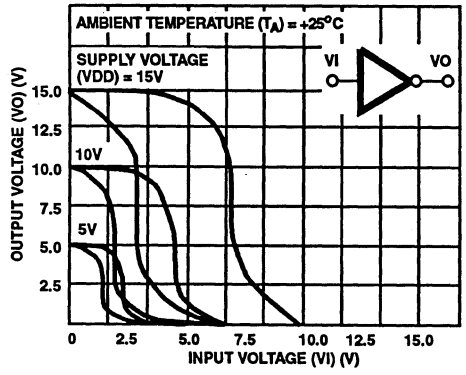


FIGURE 2. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS

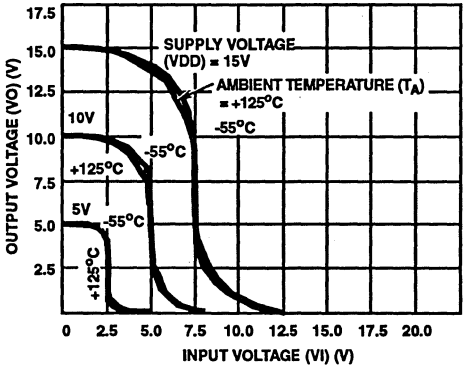


FIGURE 3. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE

Typical Performance Characteristics (Continued)

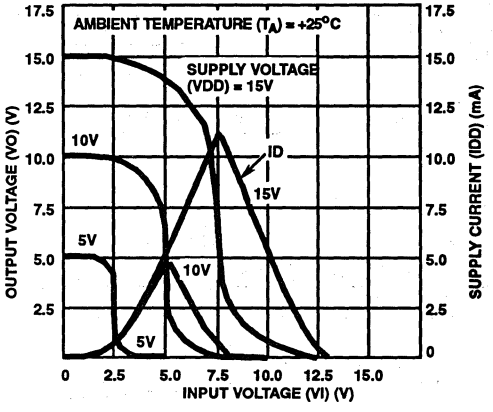


FIGURE 4. TYPICAL CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS)

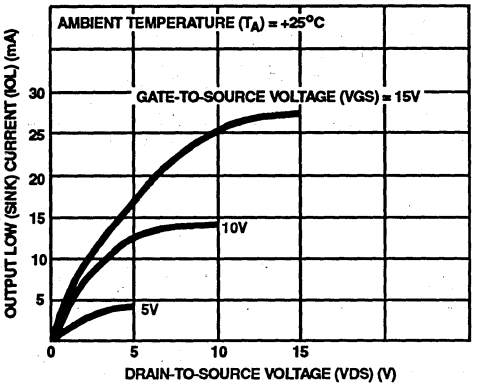


FIGURE 5. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

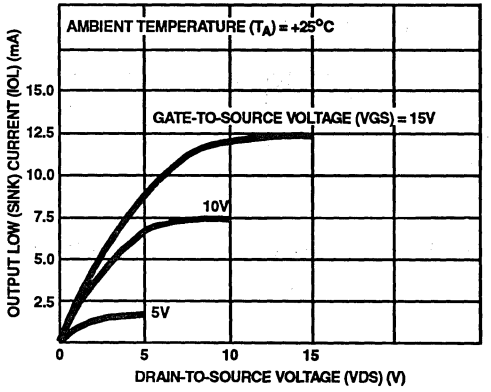


FIGURE 6. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

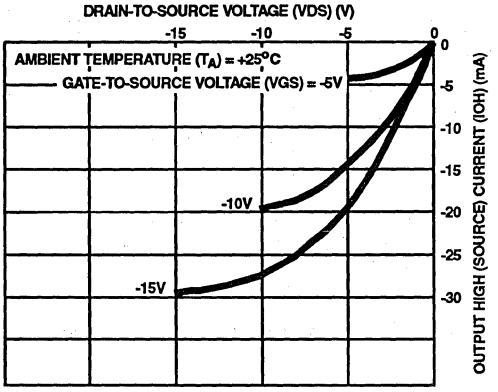


FIGURE 7. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

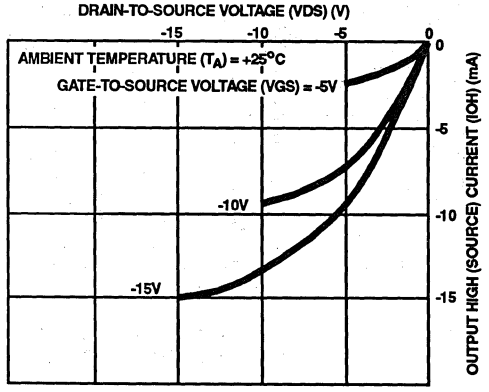


FIGURE 8. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

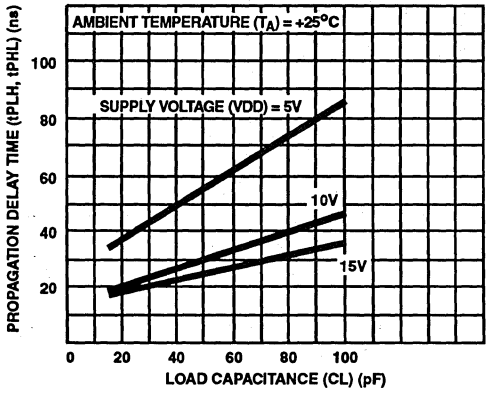


FIGURE 9. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

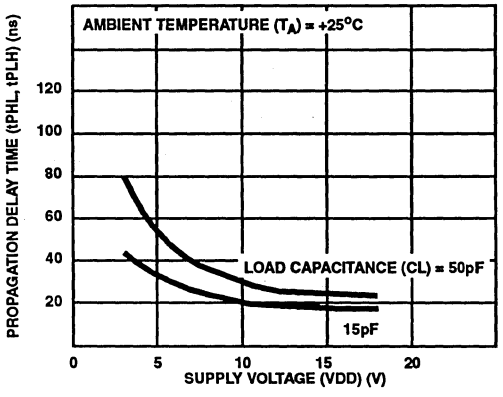


FIGURE 10. TYPICAL PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

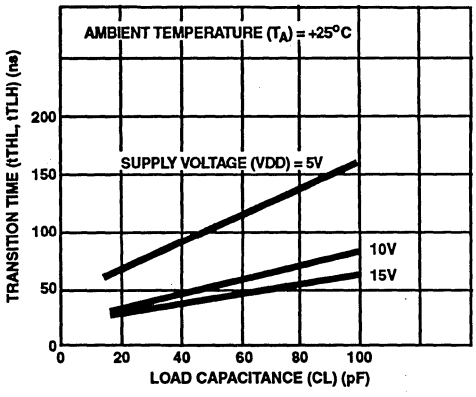


FIGURE 11. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

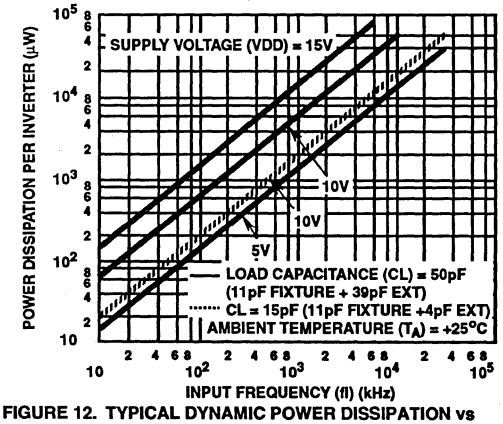


FIGURE 12. TYPICAL DYNAMIC POWER DISSIPATION vs FREQUENCY

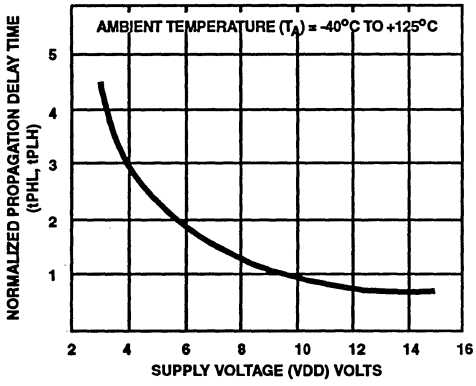
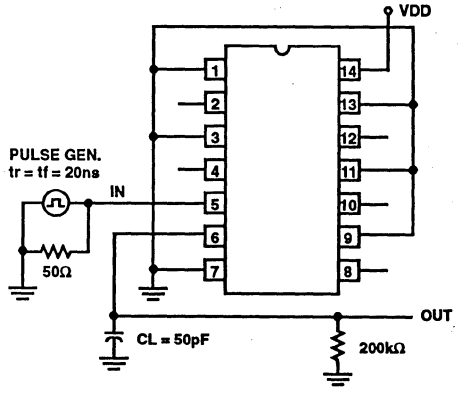


FIGURE 13. VARIATION OF NORMALIZED PROPAGATION DELAY TIME (tPHL AND tPLH) WITH SUPPLY VOLTAGE



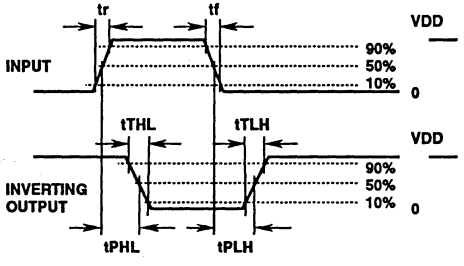


FIGURE 14. DYNAMIC ELECTRICAL CHARACTERISTICS TEST CIRCUIT AND WAVEFORMS

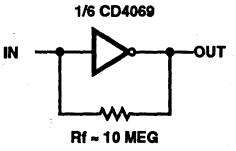
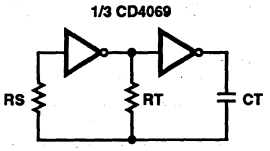
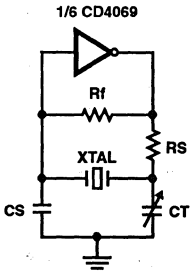


FIGURE 15. HIGH-INPUT IMPEDANCE AMPLIFIER



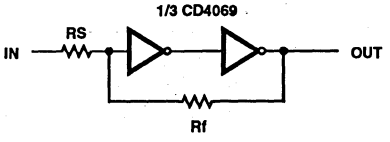
FOR TYPICAL COMPONENT VALUES AND CIRCUIT PERFORMANCE, SEE APPLICATION NOTE AN-6466

FIGURE 16. TYPICAL RC OSCILLATOR CIRCUIT



FOR TYPICAL COMPONENT VALUES AND CIRCUIT PERFORMANCE, SEE APPLICATION NOTES: AN-6086 AND AN-6539

FIGURE 17. TYPICAL CRYSTAL OSCILLATOR CIRCUIT



UPPER SWITCHING POINT

$$VP \approx \frac{RS + Rf}{Rf} \cdot \frac{VDD}{2}$$

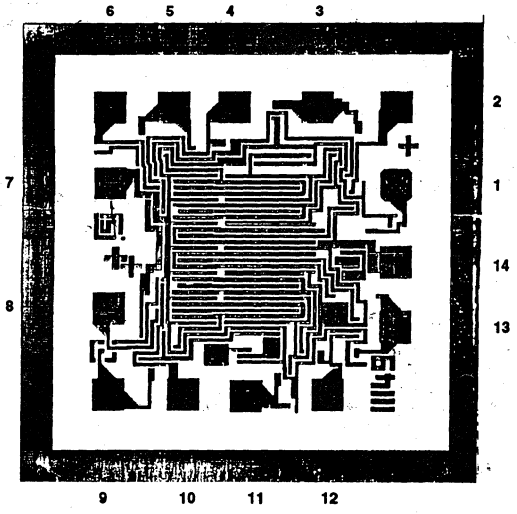
LOWER SWITCHING POINT

$$VN \approx \frac{Rf - RS}{Rf} \cdot \frac{VDD}{2}$$

$Rf > RS$

FIGURE 18. INPUT PULSE SHAPING CIRCUIT (SCHMITT TRIGGER)

Chip Dimensions and Pad Layout



DIE SIZE:
48 X 48 (45 - 53)
(1.143 - 1.346)

Dimension in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4070BMS
CD4077BMS

CMOS Quad Exclusive OR and Exclusive NOR Gates

December 1992

Features

- High Voltage Types (20V Rating)
- CD4070BMS - Quad Exclusive OR Gate
- CD4077BMS - Quad Exclusive NOR Gate
- Medium Speed Operation
  - tPHL, tPLH = 65ns (Typ.) at VDD = 10V, CL = 50pF
- 5V, 10V and 15V Parametric Ratings
- Standardized, Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Logical Comparators
- Parity Generators and Checkers
- Adders/Subtractors

Description

CD4070BMS contains four independent Exclusive OR gates. The CD4077BMS contains four independent Exclusive NOR gates.

The CD4070BMS and CD4077BMS provide the system designer with a means for direct implementation of the Exclusive OR and Exclusive NOR functions, respectively.

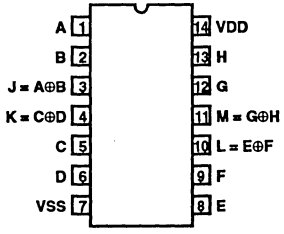
The CD4070BMS and CD4077BMS are supplied in these 14 lead outline packages:

Braze Seal DIP	H4Q	
Frit Seal DIP	H1B	
Ceramic Flatpack	*H4F	†H3W

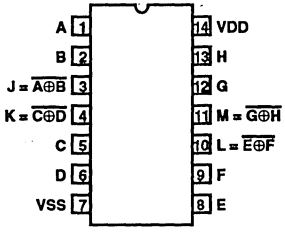
*CD4070B Only †CD4077B Only

Pinouts

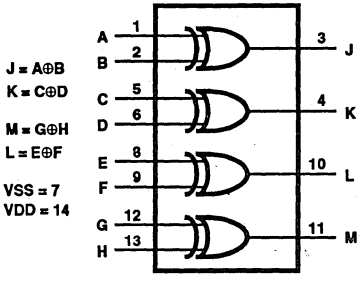
CD4070BMS
TOP VIEW



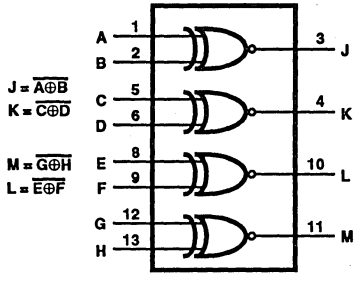
CD4077BMS
TOP VIEW



Functional Diagram



CD4070BMS



CD4077BMS

7 LOGIC

File Number 3322

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K)..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTES 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	280	ns
			10, 11	+125°C, -55°C	-	378	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-2.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	130	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

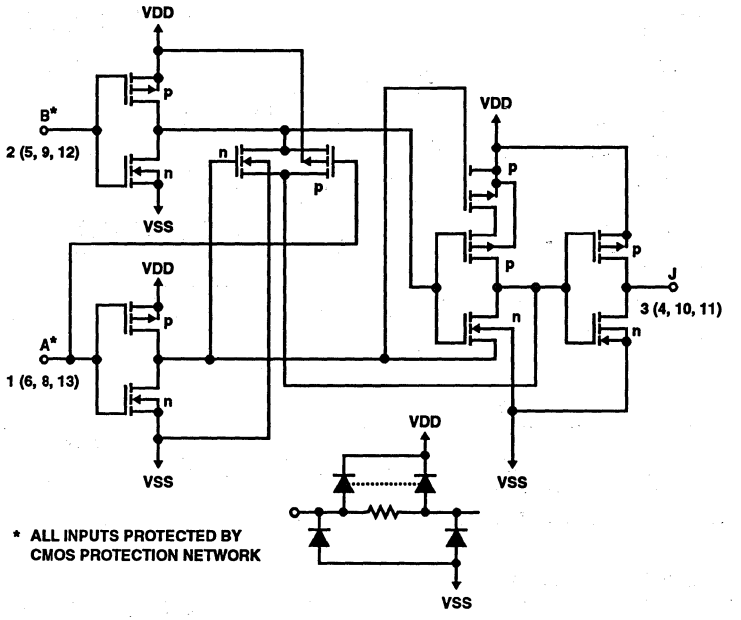
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	3, 4, 10, 11	1, 2, 5-9, 12, 13	14			
Static Burn-In 2 Note 1	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12-14			
Dynamic Burn-In Note 1	-	7	14	3, 4, 10, 11	1, 5, 8, 12	2, 6, 9, 13
Irradiation Note 2	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12-14			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Schematics

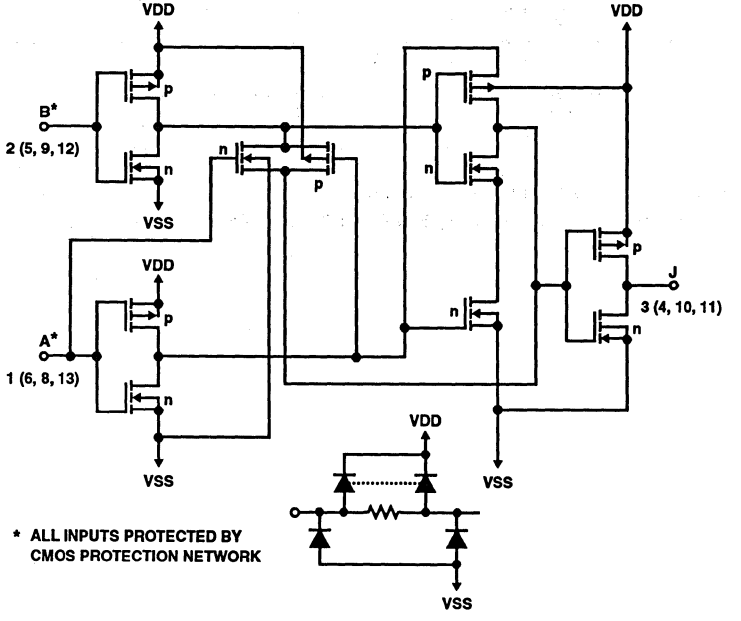


TRUTH TABLE CD4070BMS
1 OF 4 GATES

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

1 = High Level
0 = Low Level
J = A⊕B

FIGURE 1. SCHEMATIC DIAGRAM FOR CD4070BMS (1 OF 4 IDENTICAL GATES)



TRUTH TABLE CD4077BMS
1 OF 4 GATES

A	B	J
0	0	1
1	0	0
0	1	0
1	1	1

1 = High Level
0 = Low Level
J = $\overline{A \oplus B}$

FIGURE 2. SCHEMATIC DIAGRAM FOR CD4077BMS (1 OF 4 IDENTICAL GATES)

Typical Performance Characteristics

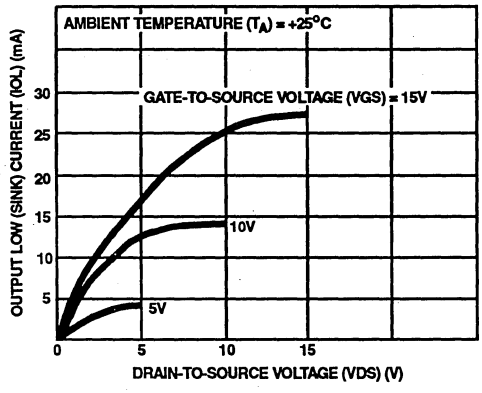


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

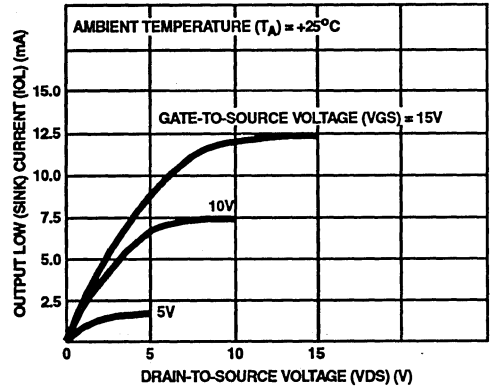


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

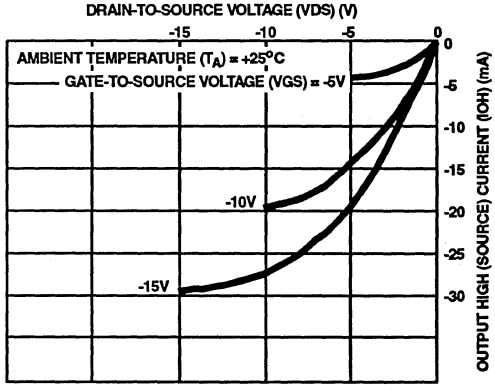


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

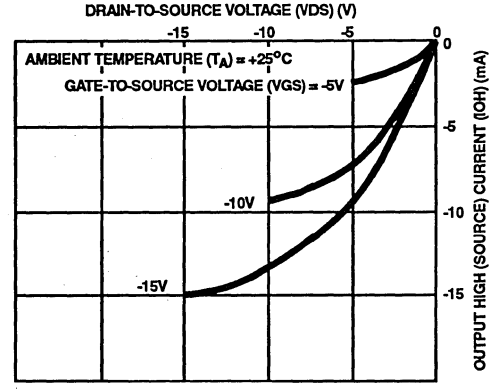


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

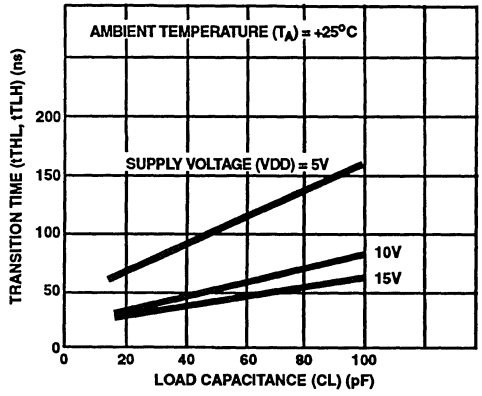


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

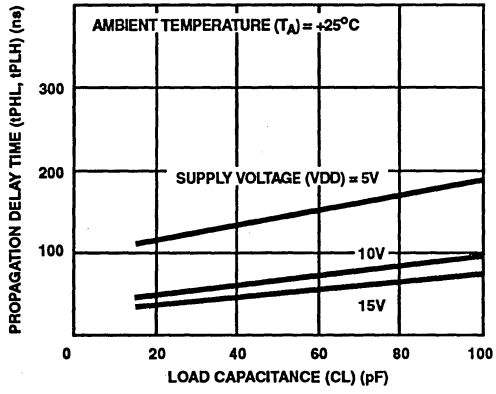


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

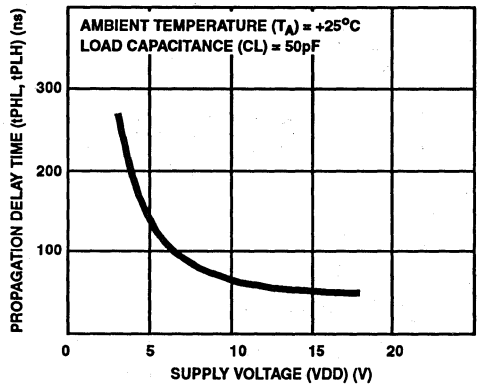


FIGURE 9. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF SUPPLY VOLTAGE

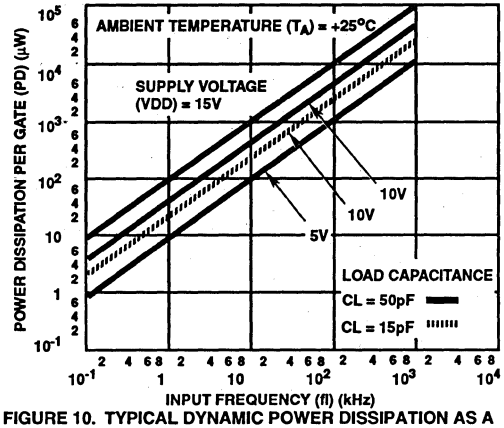
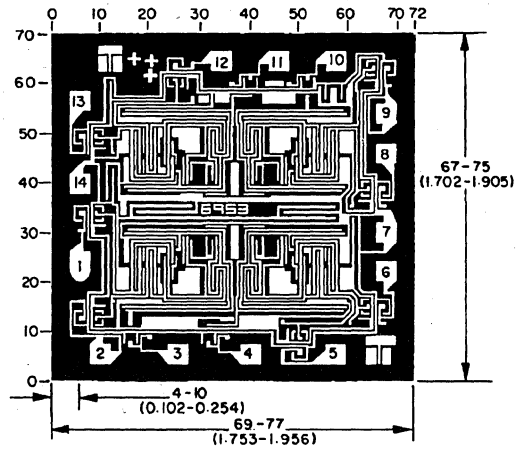


FIGURE 10. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

Chip Dimensions and Pad Layout



CD4077BMSH

Dimensions and pad layout for CD4070BMSH are identical

Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4071BMS, CD4072BMS CD4075BMS

December 1992

CMOS OR Gate

Features

- High-Voltage Types (20V Rating)
- CD4071BMS Quad 2-Input OR Gate
- CD4072BMS Dual 4-Input OR Gate
- CD4075BMS Triple 3-Input OR Gate
- Medium Speed Operation:
  - tPHL, tPLH = 60ns (typ) at 10V
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Standardized Symmetrical Output Characteristics
- Noise Margin (Over Full Package Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Description

CD4071BMS, CD4072BMS and CD4075BMS OR gates provide the system designer with direct implementation of the positive-logic OR function and supplement the existing family of CMOS gates.

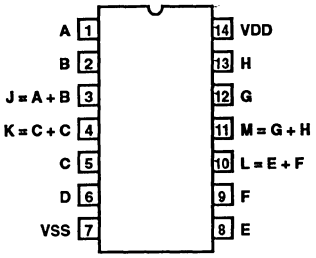
The CD4071BMS, CD4072BMS and CD4075BMS are supplied in these 14 lead outline packages:

Braze Seal DIP	*H4H	†H4Q
Frit Seal DIP	H1B	
Ceramic Flatpack	H3W	

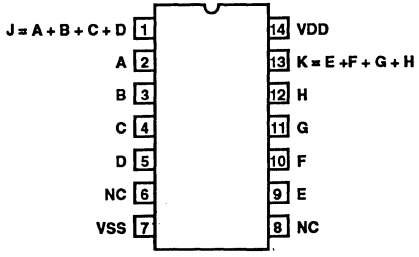
*CD4071, CD4072 †CD4075 Only

Pinout

CD4071BMS
TOP VIEW

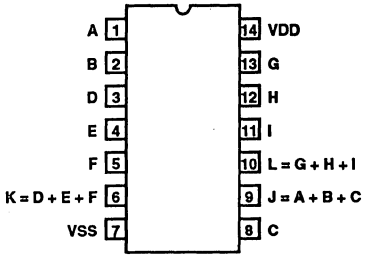


CD4072BMS
TOP VIEW



NC = NO CONNECTION

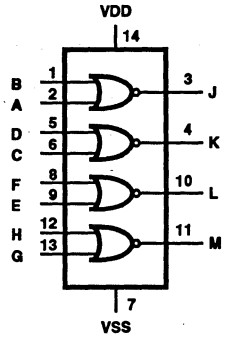
CD4075BMS
TOP VIEW



7 LOGIC

File Number 3323

Functional Diagram



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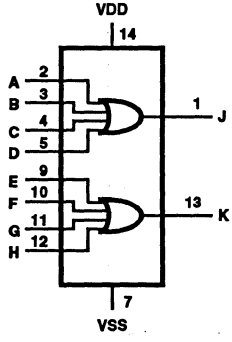

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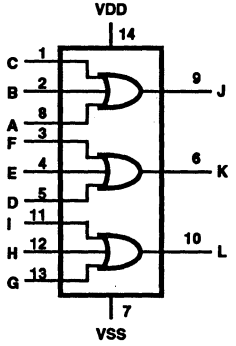


CD4075BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	0.5	µA
				2	+125°C	-	50	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	0.5	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTES 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	250	ns
			10, 11	+125°C, -55°C	-	338	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.25	µA
				+125°C	-	7.5	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	15	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	30	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-2.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	120	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	2.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - SSI	IDD	±0.1µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
PART NUMBER CD4071BMS						
Static Burn-In 1 Note 1	3, 4, 10, 11	1, 2, 5 - 9, 12 - 13	14			
Static Burn-In 2 Note 1	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12 - 14			
Dynamic Burn-In Note 1	-	7	14	3, 4, 10, 11	1, 2, 5, 6, 8, 9, 12, 13	
Irradiation Note 2	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12 - 14			
PART NUMBER CD4072BMS						
Static Burn-In 1 Note 1	1, 6, 8, 13	2 - 5, 7, 9 - 12	14			
Static Burn-In 2 Note 1	1, 6, 8, 13	7	2 - 5, 9 - 12, 14			
Dynamic Burn-In Note 1	6, 8	7	14	1, 13	2 - 5, 9 - 12	
Irradiation Note 2	1, 6, 8, 13	7	2 - 5, 9 - 12, 14			
PART NUMBER CD4075BMS						
Static Burn-In 1 Note 1	6, 9, 10	1 - 5, 7, 8, 11 - 13	14			
Static Burn-In 2 Note 1	6, 9, 10	7	1 - 5, 8, 11 - 14			
Dynamic Burn-In Note 1	-	7	14	6, 9, 10	1 - 5, 8, 11 - 13	
Irradiation Note 2	6, 9, 10	7	1 - 5, 8, 11 - 14			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

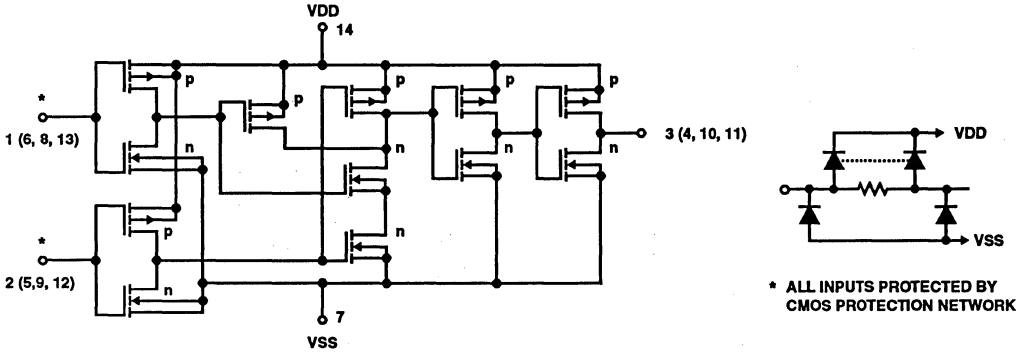


FIGURE 1. SCHEMATIC DIAGRAM FOR CD4071BMS (1 OF 4 IDENTICAL GATES)

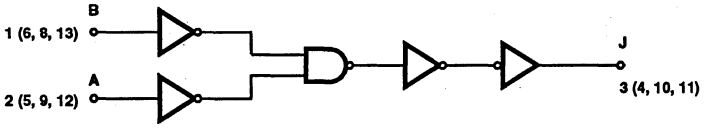


FIGURE 2. LOGIC DIAGRAM FOR CD4071BMS (1 OF 4 IDENTICAL GATES)

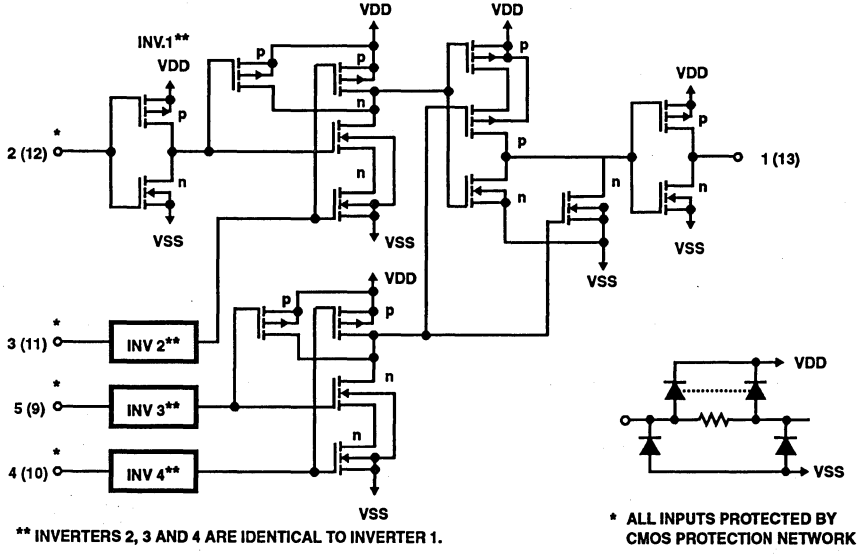


FIGURE 3. SCHEMATIC DIAGRAM FOR CD4072BMS (1 OF 2 IDENTICAL GATES)

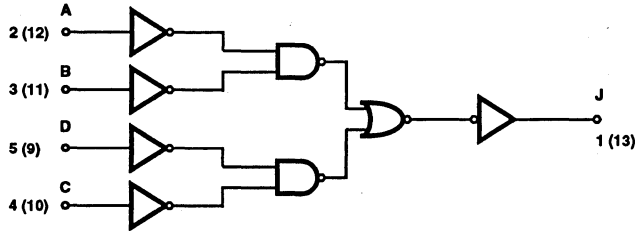


FIGURE 4. LOGIC DIAGRAM FOR CD4072BMS (1 OF 2 IDENTICAL GATES)

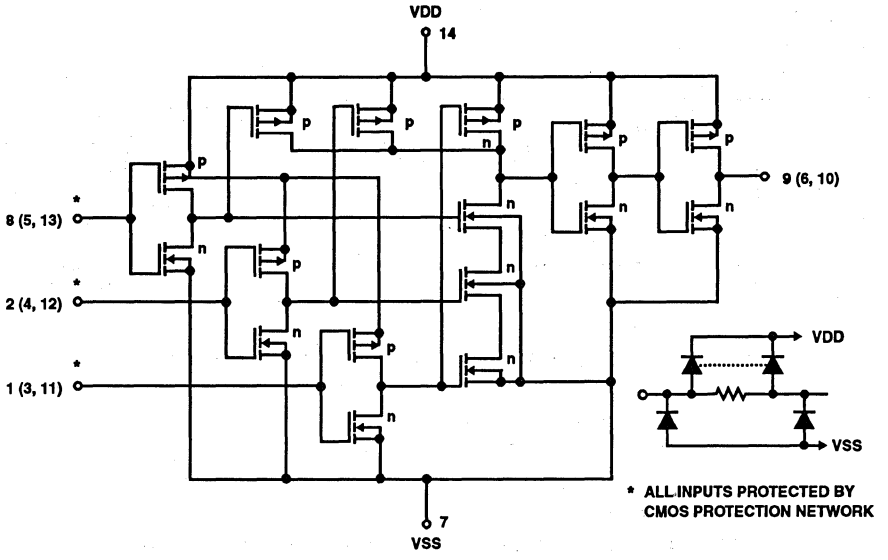


FIGURE 5. SCHEMATIC DIAGRAM FOR CD4075BMS (1 OF 3 IDENTICAL GATES)

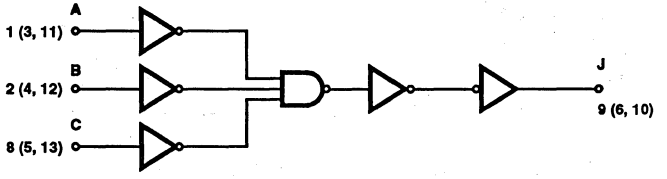


FIGURE 6. LOGIC DIAGRAM FOR CD4075BMS (1 OF 3 IDENTICAL GATES)

Typical Performance Characteristics

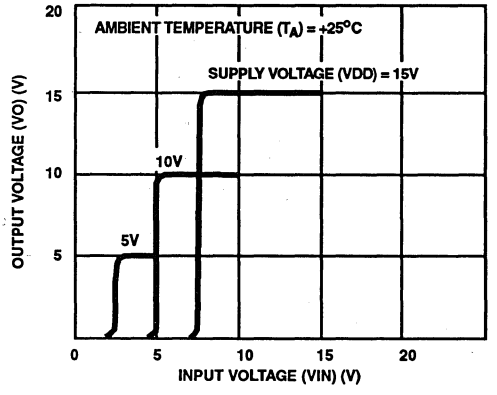


FIGURE 7. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS

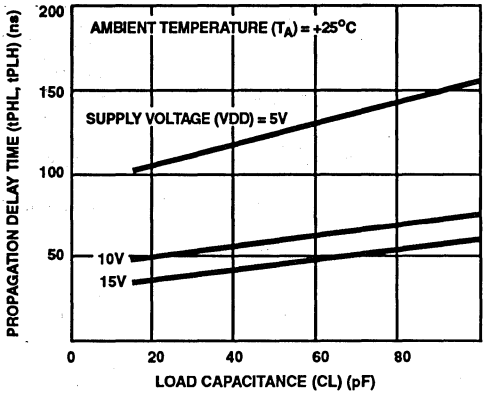


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

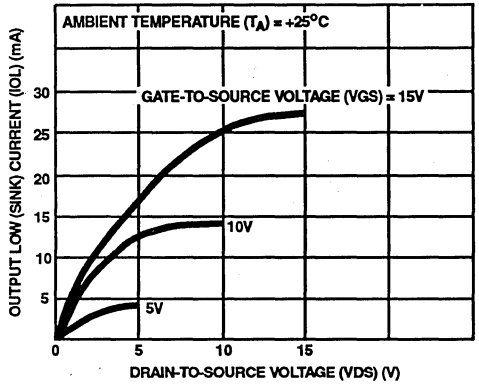


FIGURE 9. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

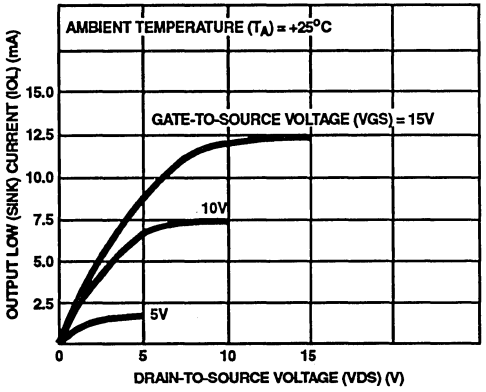


FIGURE 10. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

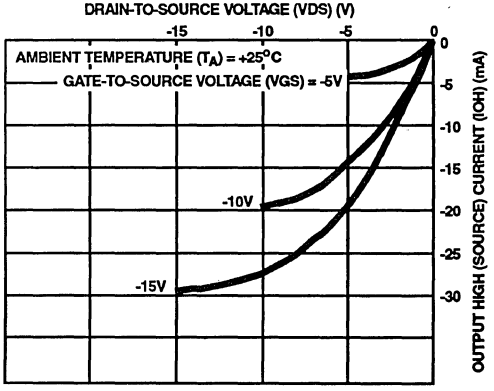


FIGURE 11. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

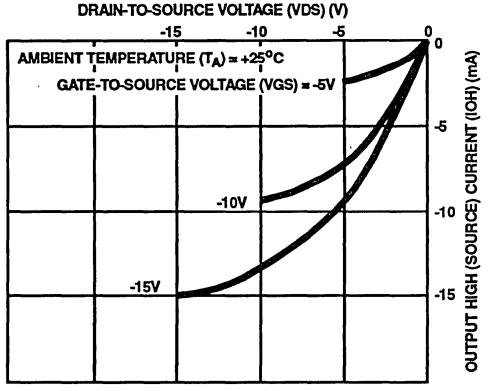


FIGURE 12. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

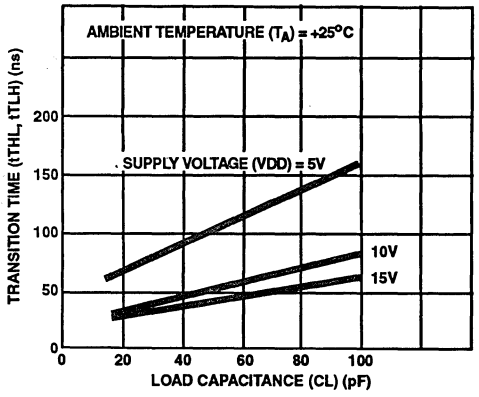


FIGURE 13. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

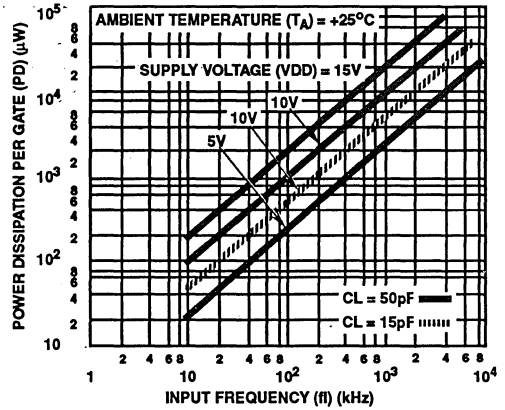
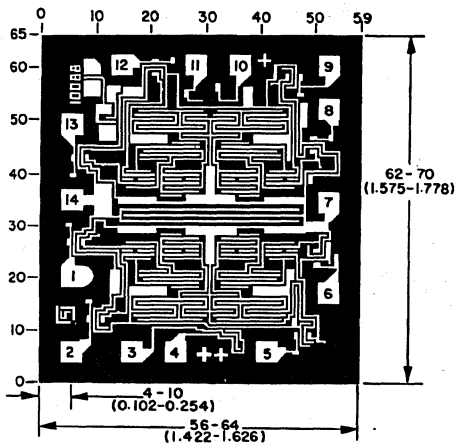


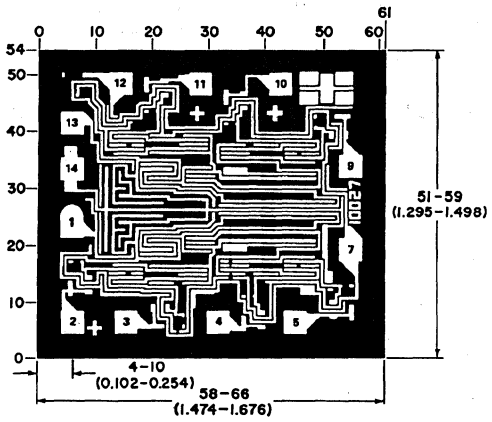
FIGURE 14. TYPICAL DYNAMIC POWER DISSIPATIONAS A FUNCTION OF FREQUENCY

7 LOGIC

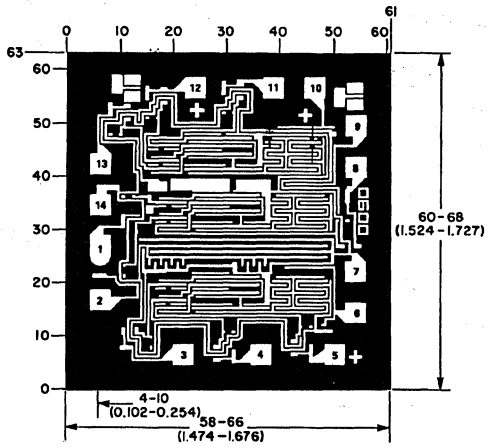
Chip Dimensions and Pad Layouts



CD4071BMS



CD4072BMS



CD4075BMS

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4073BMS, CD4081BMS CD4082BMS

December 1992

CMOS AND Gate

Features

- High-Voltage Types (20V Rating)
- CD4073BMS Triple 3-Input AND Gate
- CD4081BMS Quad 2-Input AND Gate
- CD4082BMS Dual 4-Input AND Gate
- Medium Speed Operation:
  - tPLH, tPHL = 60ns (typ) at VDD = 10V
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Standardized Symmetrical Output Characteristics
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Description

CD4073BMS, CD4081BMS and CD4082BMS AND gates provide the system designer with direct implementation of the AND function and supplement the existing family of CMOS gates.

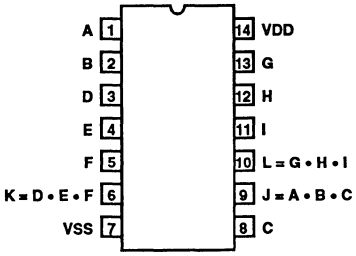
The CD4073BMS, CD4081BMS and CD4082BMS are supplied in these 14 lead outline packages:

Braze Seal DIP	*H4Q	†H4H
Frit Seal DIP	*H1B	
Ceramic Flatpack	*H3W	

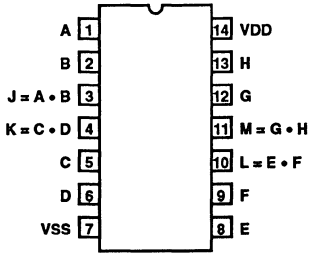
*CD4073B, CD4081B †CD4082B

Pinout

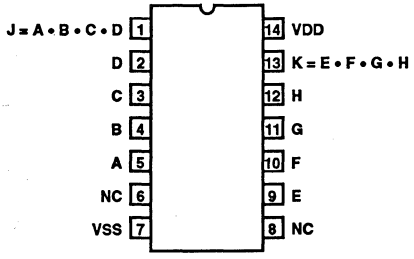
CD4073BMS
TOP VIEW



CD4081BMS
TOP VIEW



CD4082BMS
TOP VIEW



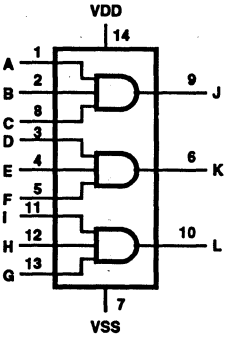
NC = NO CONNECTION

7 LOGIC

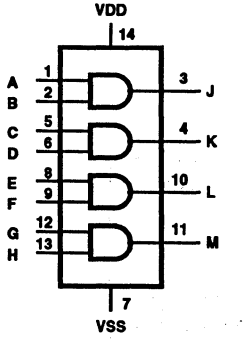
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3324

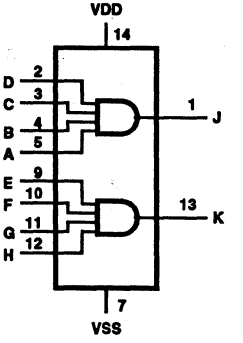
Functional Diagram



CD4073BMS



CD4081BMS



CD4082BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . . -0.5V to VDD +0.5V
DC Input Current, Any One Input. . . . . ±10mA
Operating Temperature Range. . . . . -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . . +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

	θ_{ja}	θ_{jc}
Thermal Resistance		
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) . . . . . Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . . +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	.5	µA
				2	+125°C	-	50	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	.5	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH> VDD/2	VOL< VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTES 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	250	ns
			10, 11	+125°C, -55°C	-	338	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	.25	µA
				+125°C	-	7.5	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	.5	µA
				+125°C	-	15	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	.5	µA
				+125°C	-	30	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-2.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	120	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	2.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - SSI	IDD	±0.1µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
PART NUMBER CD4073BMS						
Static Burn-In 1 Note 1	6, 9, 10	1 - 5, 7, 8, 11 - 13	14			
Static Burn-In 2 Note 1	6, 9, 10	7	1 - 5, 8, 11 - 14			
Dynamic Burn-In Note 1	-	7	14	6, 9, 10	1, 5, 8, 11 - 13	
Irradiation Note 2	6, 9, 10	7	1 - 5, 8, 11 - 14			
PART NUMBER CD4081BMS						
Static Burn-In 1 Note 1	3, 4, 10, 11	1, 2, 5 - 9, 12, 13	14			
Static Burn-In 2 Note 1	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12 - 14			
Dynamic Burn-In Note 1	-	7	14	3, 4, 10, 11	1, 2, 5, 6, 8, 9, 12, 13	
Irradiation Note 2	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12 - 14			
PART NUMBER CD4082BMS						
Static Burn-In 1 Note 1	1, 6, 8, 13	2 - 5, 7, 9 - 12	14			
Static Burn-In 2 Note 1	1, 6, 8, 13	7	2 - 5, 9 - 12, 14			
Dynamic Burn-In Note 1	6, 8	7	14	1, 3	2 - 5, 9 - 12	
Irradiation Note 2	1, 6, 8, 13	7	2 - 5, 9 - 12, 14			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

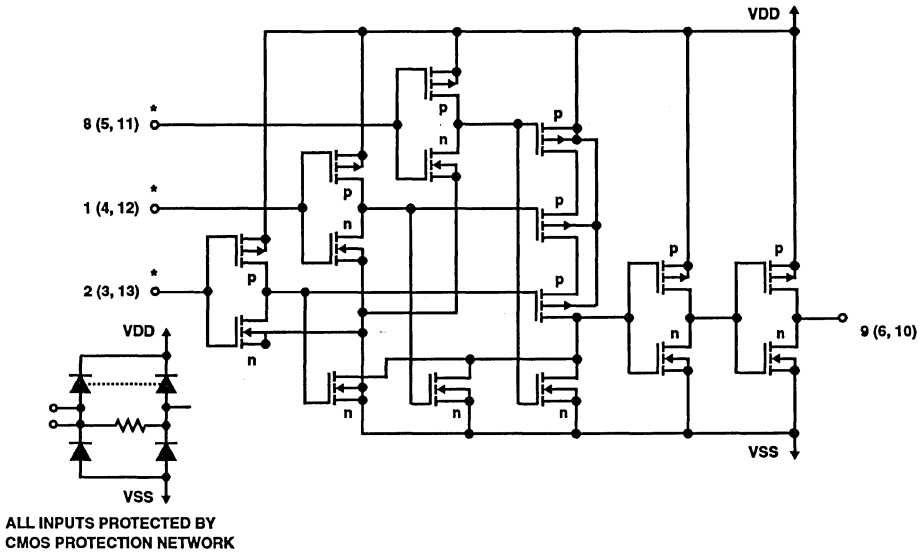


FIGURE 1. SCHEMATIC DIAGRAM FOR CD4073BMS (1 OF 3 IDENTICAL GATES)

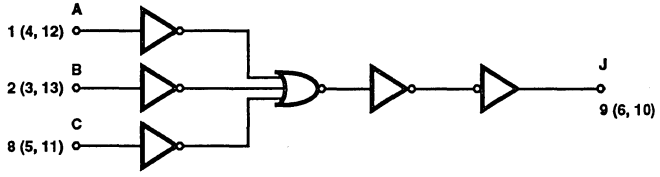


FIGURE 2. LOGIC DIAGRAM FOR CD4073BMS (1 OF 3 IDENTICAL GATES)

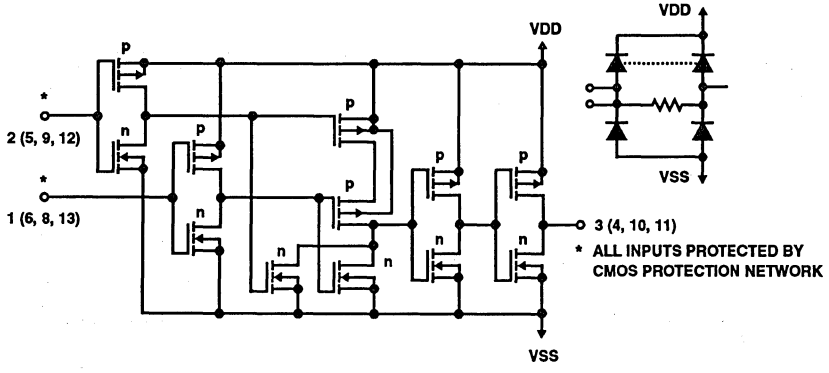


FIGURE 3. SCHEMATIC DIAGRAM FOR CD4081BMS (1 OF 4 IDENTICAL GATES)

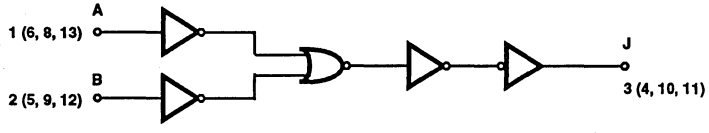


FIGURE 4. LOGIC DIAGRAM FOR CD4081BMS (1 OF 4 IDENTICAL GATES)

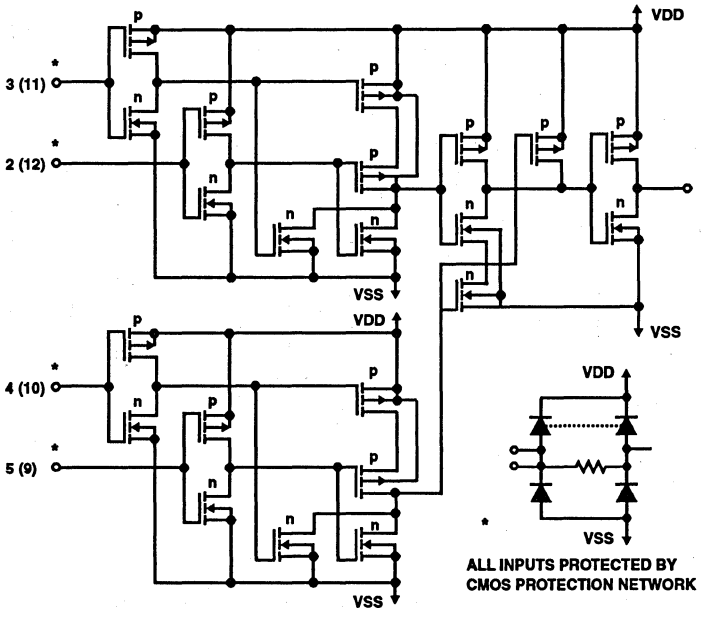


FIGURE 5. SCHEMATIC DIAGRAM FOR CD4082BMS (1 OF 2 IDENTICAL GATES)

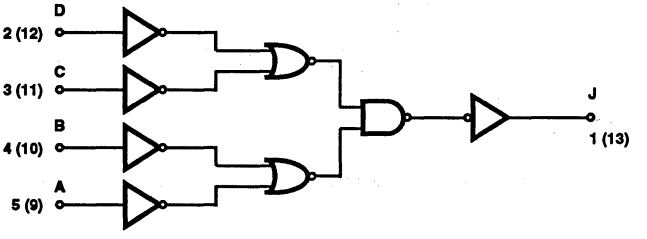


FIGURE 6. LOGIC DIAGRAM FOR CD4082BMS (1 OF 2 IDENTICAL GATES)

Typical Performance Characteristics

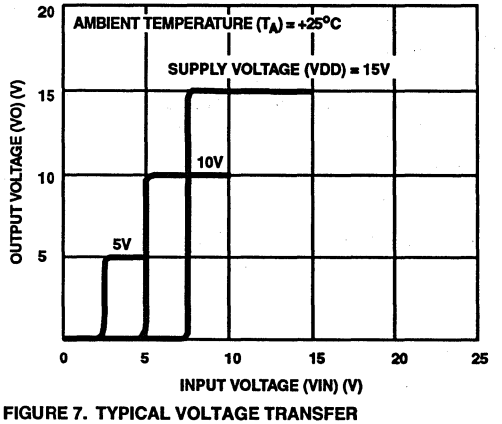


FIGURE 7. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS

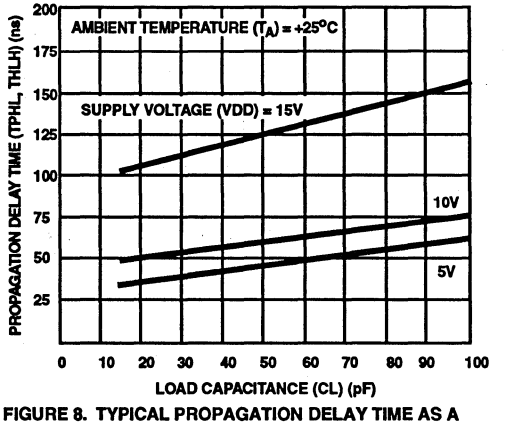


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

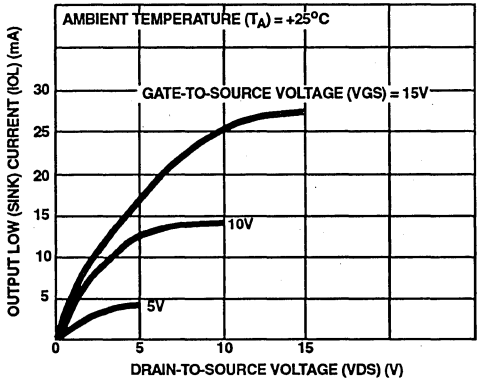


FIGURE 9. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

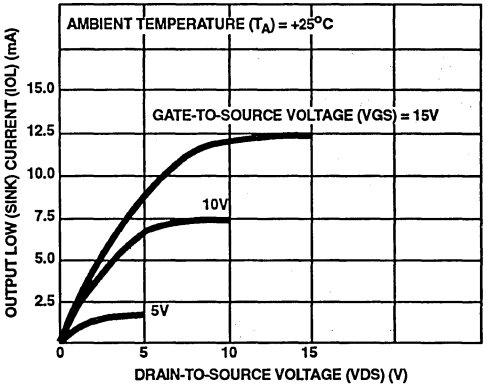


FIGURE 10. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

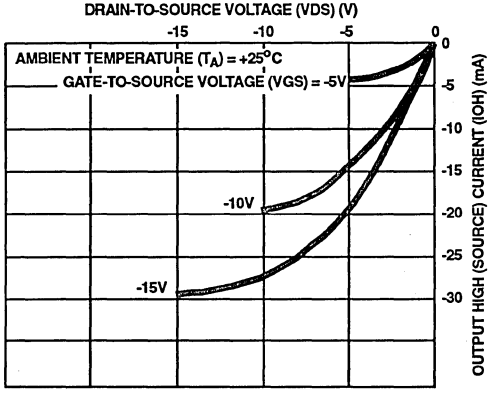


FIGURE 11. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

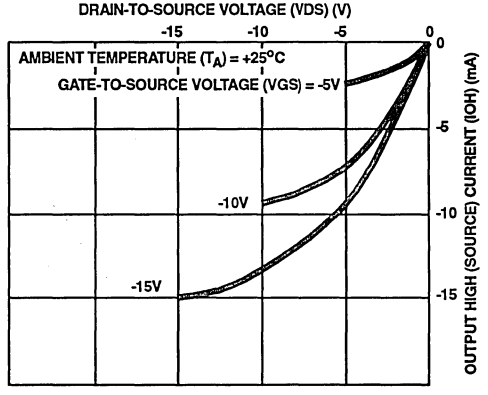


FIGURE 12. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

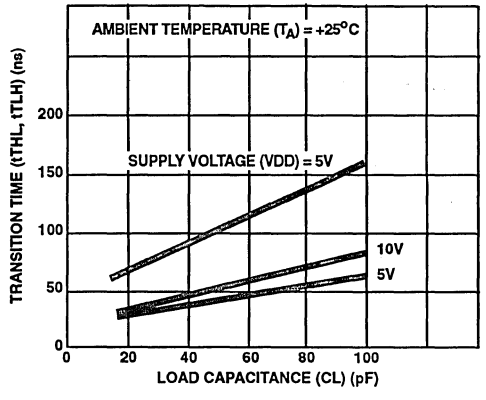


FIGURE 13. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

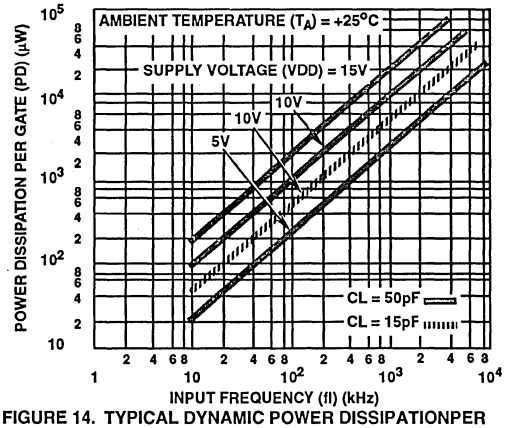
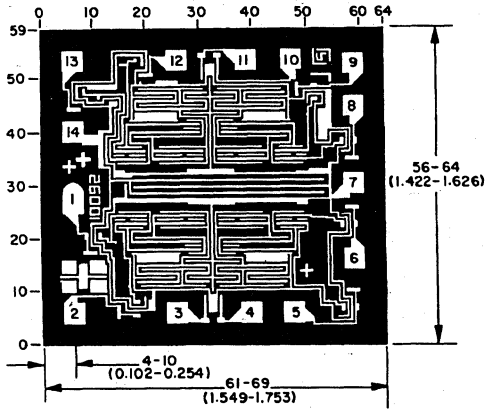
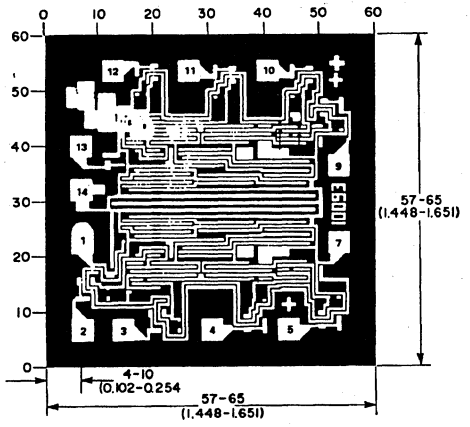


FIGURE 14. TYPICAL DYNAMIC POWER DISSIPATIONPER GATE AS A FUNCTION OF FREQUENCY

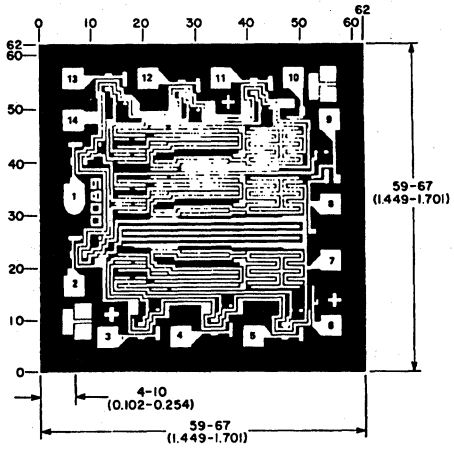
Chip Dimensions and Pad Layouts



CD4081BMS



CD4082BMS



CD4073BMS

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

CD4076BMS

CMOS 4 -Bit D-Type Registers

December 1992

Features

- High Voltage Type (20V Rating)
- Three State Outputs
- Input Disabled Without Gating the Clock
- Gated Output Control Lines for Enabling or Disabling the Outputs
- Standardized Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Description

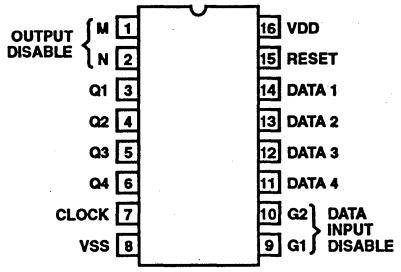
CD4076BMS types are four-bit registers consisting of D-type flip-flops that feature three-state outputs. Data Disable inputs are provided to control the entry of data into the flip-flops. When both Data Disable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Output Disable inputs are also provided. When the Output Disable inputs are both low, the normal logic states of the four outputs are available to the load. The outputs are disabled independently of the clock by a high logic level at either Output Disable input, and present a high impedance.

The CD4076BMS is supplied in these 16 lead outline packages:

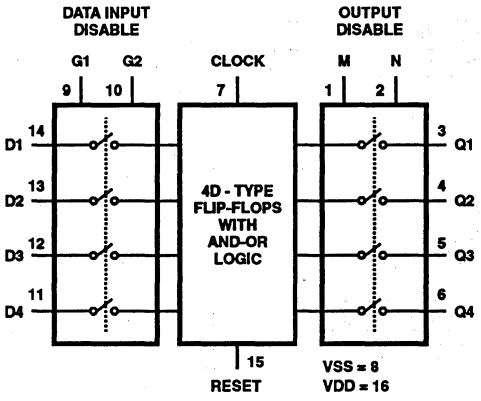
Braze Seal DIP	H4T
Frit Seal DIP	H1E
Ceramic Flatpack	H6W

Pinout

CD4076BMS
TOP VIEW



Functional Diagram



7 LOGIC

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs ..... -0.5V to VDD +0.5V
DC Input Current, Any One Input ..... ±10mA
Operating Temperature Range ..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH> VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.4	-	µA
				2	+125°C	-12	-	µA
			VDD = 18V	3	-55°C	-0.4	-	µA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.4	µA
				2	+125°C	-	12	µA
			VDD = 18V	3	-55°C	-	0.4	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (Notes 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Q Output	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-2.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Clock to Q Output	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	250	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns
Propagation Delay Reset	TPHL2	VDD = 5V	1, 2, 3	+25°C	-	460	ns
		VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	150	ns
Propagation Delay 3 - State	TPHZ TPLZ	VDD = 5V	1, 2, 4	+25°C	-	300	ns
		VDD = 10V	1, 2, 4	+25°C	-	150	ns
		VDD = 15V	1, 2, 4	+25°C	-	120	ns
Propagation Delay 3 - State	TPZH TPZL	VDD = 5V	1, 2, 4	+25°C	-	300	ns
		VDD = 10V	1, 2, 4	+25°C	-	150	ns
		VDD = 15V	1, 2, 4	+25°C	-	120	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Transition Time	TTLH	VDD = 10V	1, 2, 3	+25°C	-	-	ns
		VDD = 15V	1, 2, 3	+25°C	-	-	ns
Maximum Clock Input Frequency	FCL	VDD = 5V	1, 2, 3	+25°C	3	-	MHz
		VDD = 10V	1, 2, 3	+25°C	6	-	MHz
		VDD = 15V	1, 2, 3	+25°C	8	-	MHz
Minimum Data Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Minimum Data Hold Time Reset Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	120	ns
		VDD = 10V	1, 2, 3	+25°C	-	50	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Minimum Data Input Set-Up Time	TS	VDD = 5V	1, 2, 3	+25°C	-	180	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	70	ns
Maximum Clock Input Rise and Fall Time	TRCL TFCL	VDD = 5V	1, 2, 3, 5	+25°C	-	15	µs
		VDD = 10V	1, 2, 3, 5	+25°C	-	5	µs
		VDD = 15V	1, 2, 3, 5	+25°C	-	5	µs

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. CL = 50pF, RL = 1K, Input TR, TF < 20ns.
5. If more than one unit is cascaded, TRCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Group D	Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	3 - 6	1, 2, 7 - 15	16			
Static Burn-In 2 Note 1	3 - 6	8	1, 2, 7, 9 -16			
Dynamic Burn-In Note 1	-	1, 2, 8 - 10, 15	16	3 - 6	7	11 - 14
Irradiation (Note 2)	3 - 6	8	1, 2, 7, 9 - 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

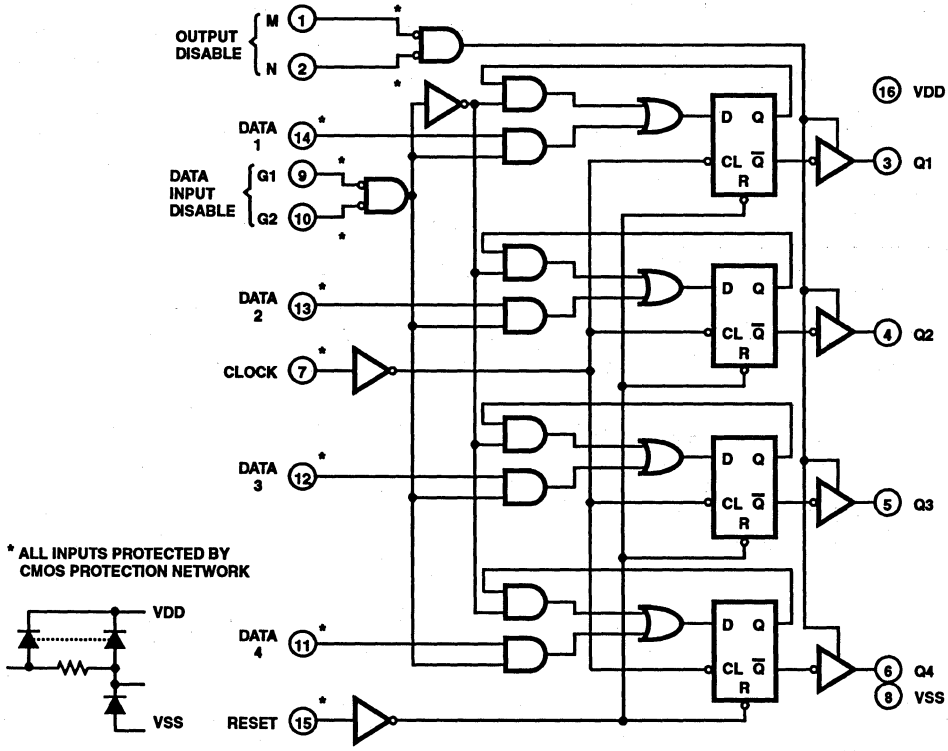


FIGURE 1. CD4076BMS LOGIC DIAGRAM

TRUTH TABLE

RESET	CLOCK	DATA INPUT DISABLE G1	DATA INPUT DISABLE G2	DATA D	NEXT STATE OUTPUT Q	
1	X	X	X	X	0	
0	0	X	X	X	Q	NC
0	↑	1	X	X	Q	NC
0	↑	X	1	X	Q	NC
0	↑	0	0	1	1	
0	↑	0	0	0	0	
0	1	X	X	X	Q	NC
0	↓	X	X	X	Q	NC

When either Output Disable M or N is high, the outputs are disabled (high impedance state), however sequential operation of the flip-flops is not affected

1 = High Level
X = Don't Care
0 = Low Level
NC = No Change

Typical Performance Characteristics

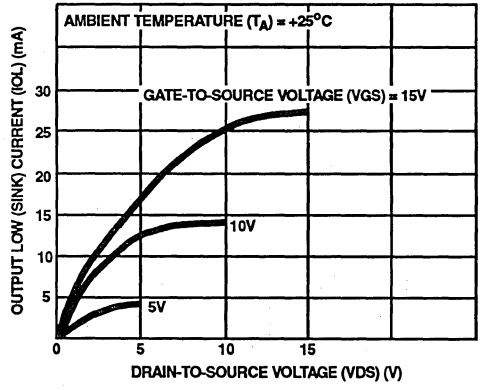


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

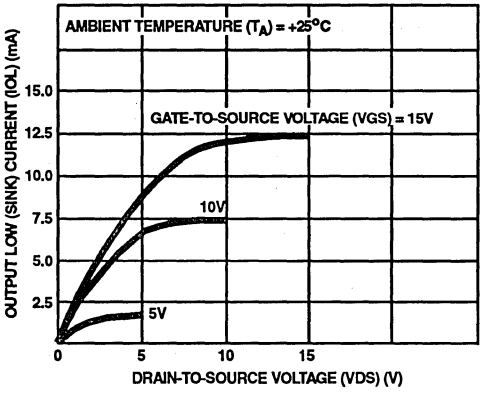


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

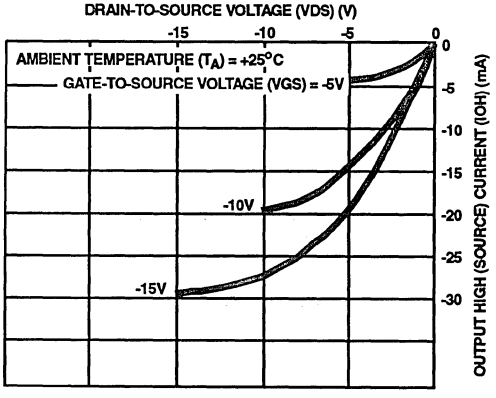


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

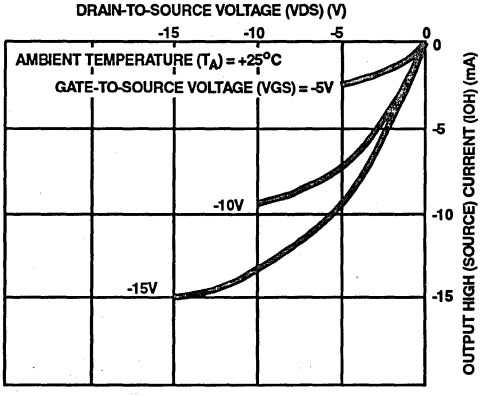


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

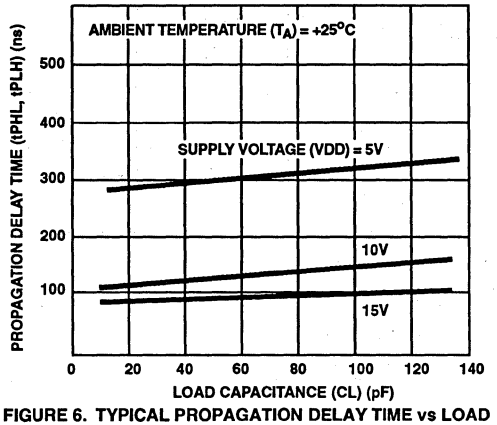


FIGURE 6. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE (CLOCK TO Q)

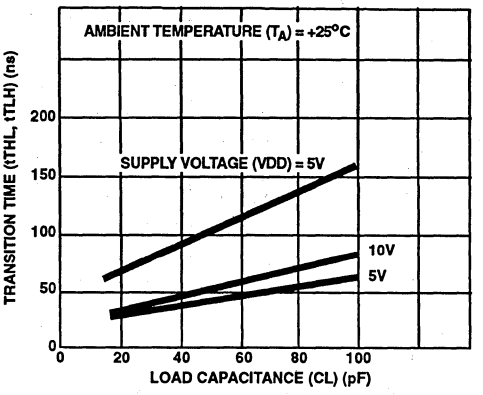


FIGURE 7. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

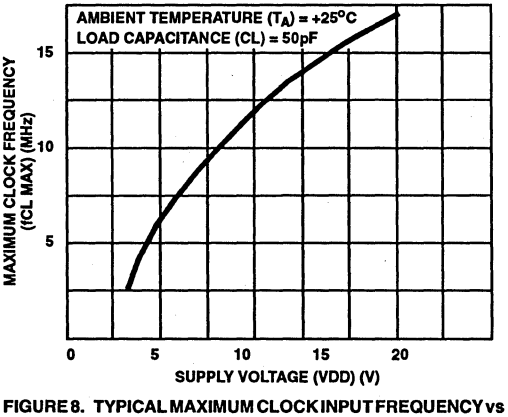


FIGURE 8. TYPICAL MAXIMUM CLOCK INPUT FREQUENCY vs SUPPLY VOLTAGE

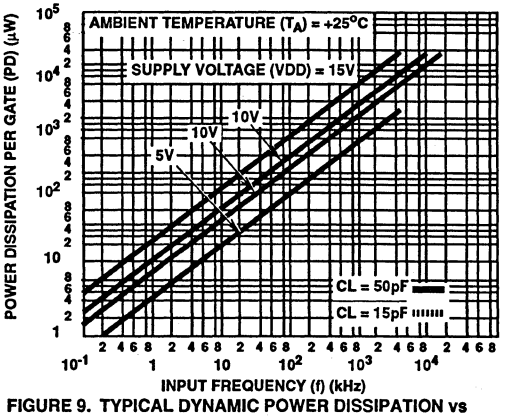


FIGURE 9. TYPICAL DYNAMIC POWER DISSIPATION vs FREQUENCY

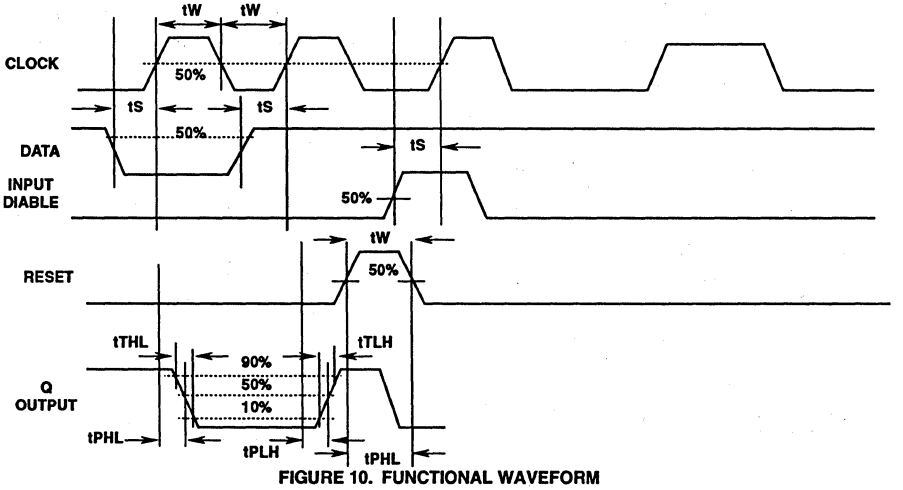


FIGURE 10. FUNCTIONAL WAVEFORM

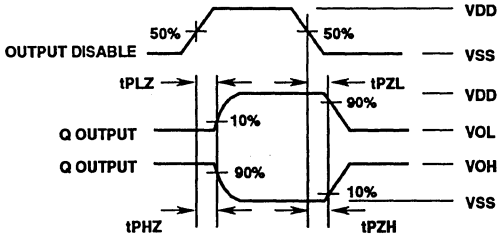
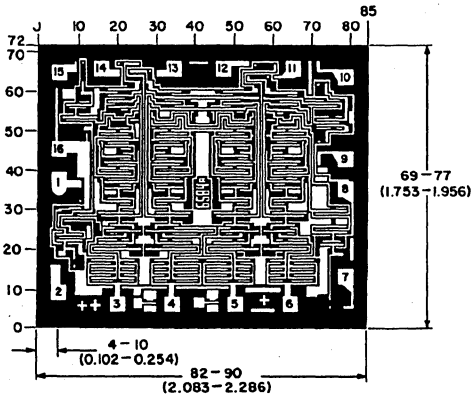


FIGURE 11. FUNCTIONAL WAVEFORM

CHARACTER	TEST VOLTAGE AT D	TEST VOLTAGE AT Q
tPHZ	VDD	VSS
tPLZ	VSS	VDD
tPZL	VSS	VDD
tPZH	VDD	VSS

Chip Dimensions and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4078BMS

December 1992

CMOS 8 Input NOR/OR Gate

Features

- High Voltage Type (20V Rating)
- Medium Speed Operation
  - tPHL, tPLH = 75ns (Typ.) at VDD = 10V
- Buffered Inputs and Output
- 5V, 10V and 15V Parametric Ratings
- Standardized, Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Description

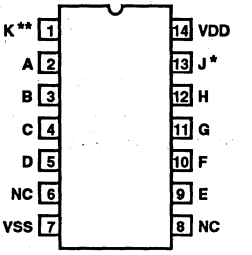
CD4078BMS NOR/OR Gate provides the system designer with direct implementation of the positive logic 8 input NOR and OR functions and supplements the existing family of CMOS gates.

The CD4078BMS is supplied in these 14 lead outline packages:

Braze Seal DIP	H4Q
Frit Seal DIP	H1B
Ceramic Flatpack	H3W

Pinout

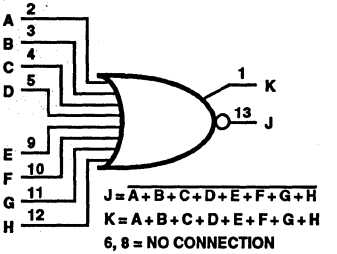
CD4078BMS
TOP VIEW



* $J = \overline{A+B+C+D+E+F+G+H}$ ** $K = A+B+C+D+E+F+G+H$

NC = NO CONNECTION

Functional Diagram



$J = \overline{A+B+C+D+E+F+G+H}$

$K = A+B+C+D+E+F+G+H$

6, 8 = NO CONNECTION

VDD = 14

VSS = 7

Logic Diagram

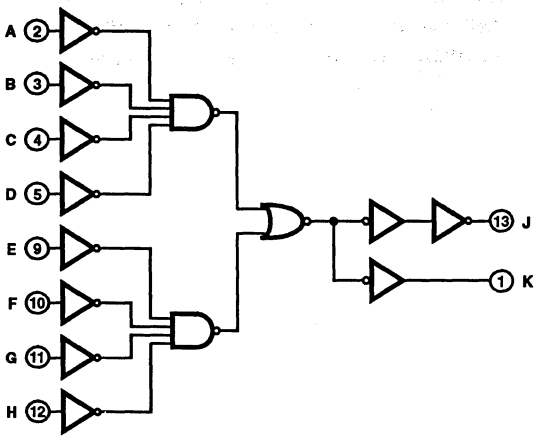


FIGURE 1. LOGIC DIAGRAM

File Number 3326

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . . -0.5V to VDD +0.5V
DC Input Current, Any One Input. . . . . ±10mA
Operating Temperature Range. . . . . -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . . +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) . . . . . Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . . +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	0.5	µA
				2	+125°C	-	50	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	0.5	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTES 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	300	ns
			10, 11	+125°C, -55°C	-	405	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	3	-	MHz
			10, 11	+125°C, -55°C	2.22	-	MHz

NOTES:

1. VDD = 5V, CL = 50pF, RL = 200K
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.25	µA
				+125°C	-	7.5	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	15	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	30	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	150	ns
		VDD = 15V	1, 2, 3	+25°C	-	110	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	6	-	MHz
		VDD = 15V	1, 2, 3	+25°C	8.5	-	MHz
Input Capacitance	CIN	ut	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	2.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - SSI	IDD	± 0.1µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	1, 6, 8, 13	2-5, 7, 9-12	14			
Static Burn-In 2 Note 1	1, 6, 8, 13	7	2-5, 9-12, 14			
Dynamic Burn-In Note 1	6, 8	7	14	1, 13	2-5, 9-12	
Irradiation Note 2	1, 6, 8, 13	7	2-5, 9-12, 14			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Schematic

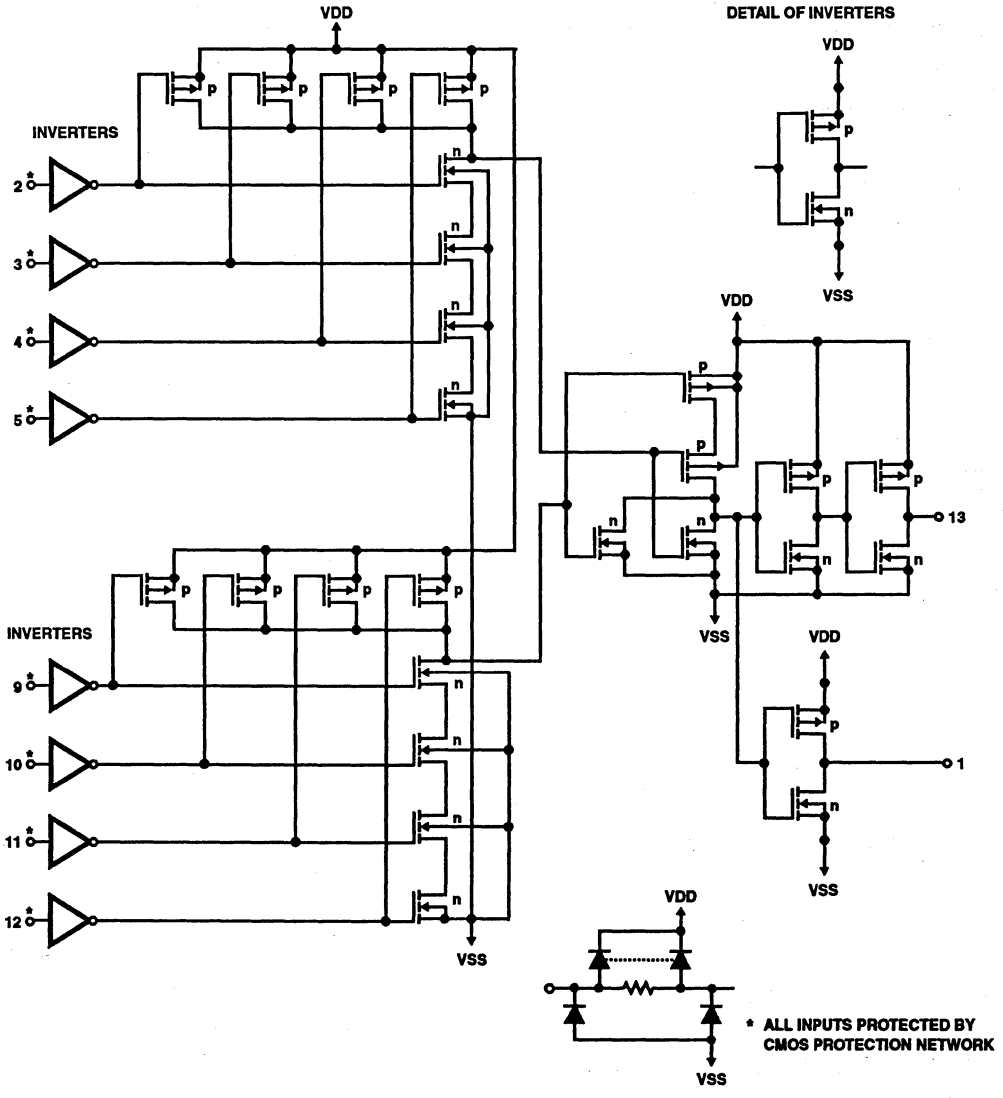


FIGURE 2. SCHEMATIC DIAGRAM

Typical Performance Characteristics

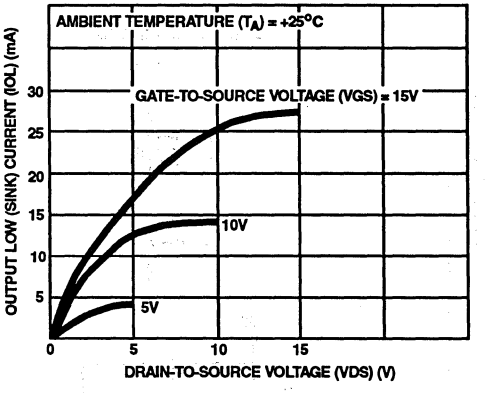


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

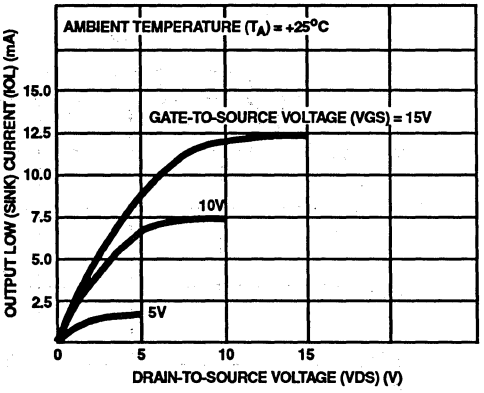


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

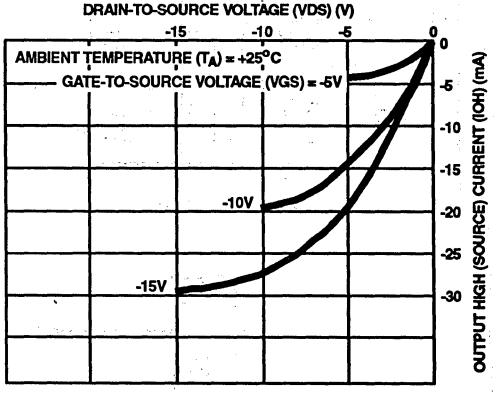


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

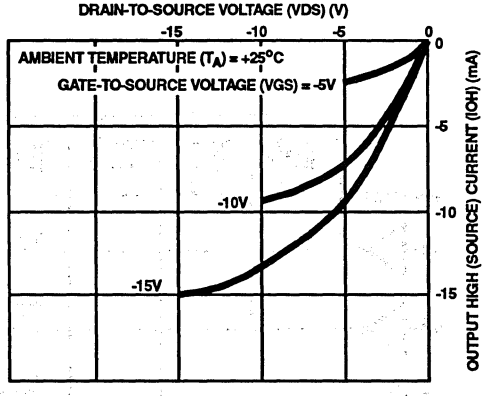


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

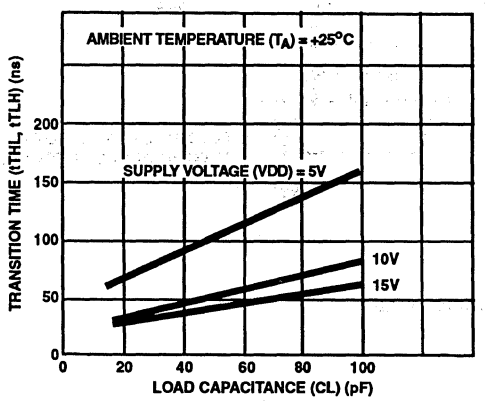


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

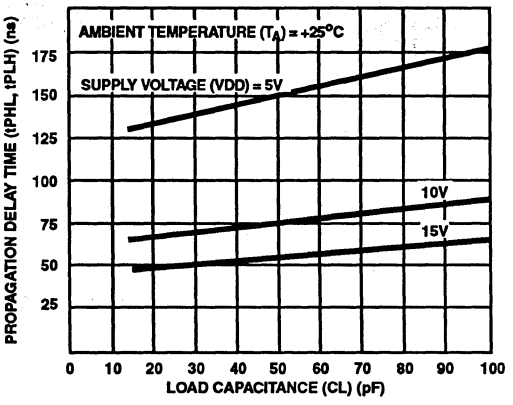


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

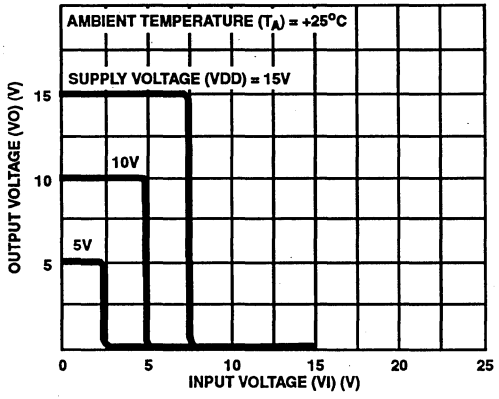


FIGURE 9. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF SUPPLY VOLTAGE

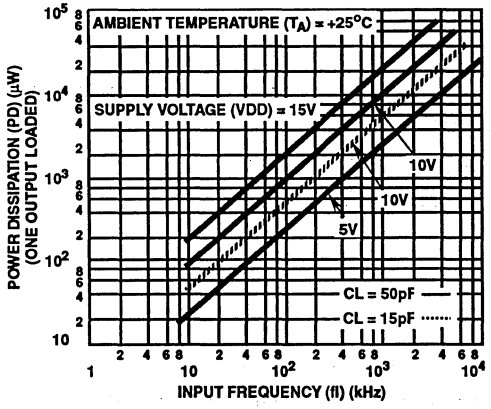
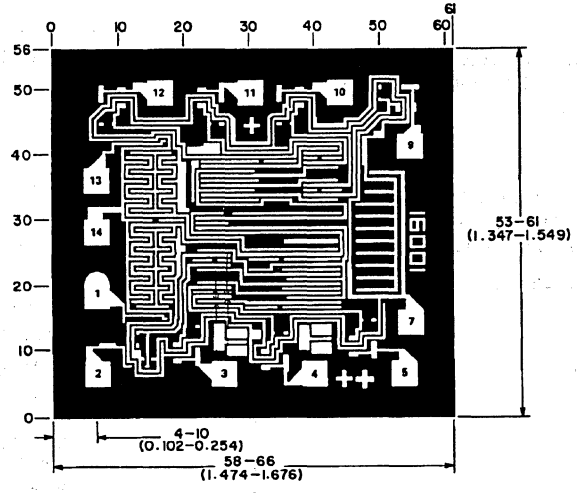


FIGURE 10. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4085BMS

CMOS Dual 2 Wide 2 Input AND-OR-INVERT Gate

December 1992

Features

- High Voltage Type (20V Rating)
- Medium Speed Operation
  - tPHL = 90ns
  - tPLH = 125ns (Typ.) at 10V
- Individual Inhibit Controls
- 5V, 10V and 15V Parametric Ratings
- Standardized Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Description

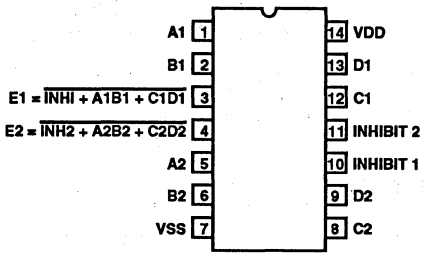
CD4085BMS contains a pair of AND-OR-INVERT gates, each consisting of two 2 input AND gates driving a 3 input NOR gate. Individual inhibit controls are provided for both A-O-I gates..

The CD4085BMS is supplied in these 14 lead outline packages:

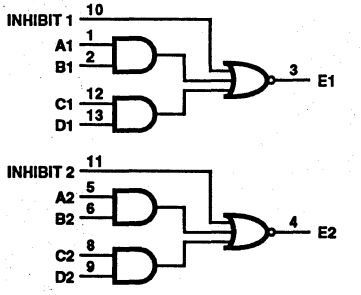
Braze Seal DIP	H4H
Frit Seal DIP	H1B
Ceramic Flatpack	H5W

Pinout

CD4085BMS
TOP VIEW



Functional Diagram



$E = \overline{INHIBIT + AB + CD}$
LOGIC 1 = HIGH
LOGIC 0 = LOW

VDD = 14
VSS = 7

File Number 3327

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTES 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Data	TPHL1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	450	ns
			10, 11	+125°C, -55°C	-	608	ns
Propagation Delay Data	TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	620	ns
			10, 11	+125°C, -55°C	-	837	ns
Propagation Delay Inhibit	TPHL2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	300	ns
			10, 11	+125°C, -55°C	-	405	ns
Propagation Delay Inhibit	TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-2.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Data	TPHL1	VDD = 10V	1, 2, 3	+25°C	-	180	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Propagation Delay Data	TPLH1	VDD = 10V	1, 2, 3	+25°C	-	250	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns
Propagation Delay Inhibit	TPHL2	VDD = 10V	1, 2, 3	+25°C	-	120	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Propagation Delay Inhibit	TPLH2	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	140	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	3, 4	1, 2, 5-13	14			
Static Burn-In 2 Note 1	3, 4	7	1, 2, 5, 6, 8-14			
Dynamic Burn-In Note 1	-	7	14	3, 4	1, 2, 5, 6, 8, 9, 12, 13	10, 11
Irradiation Note 2	3, 4	7	1, 2, 5, 6, 8-14			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Schematic

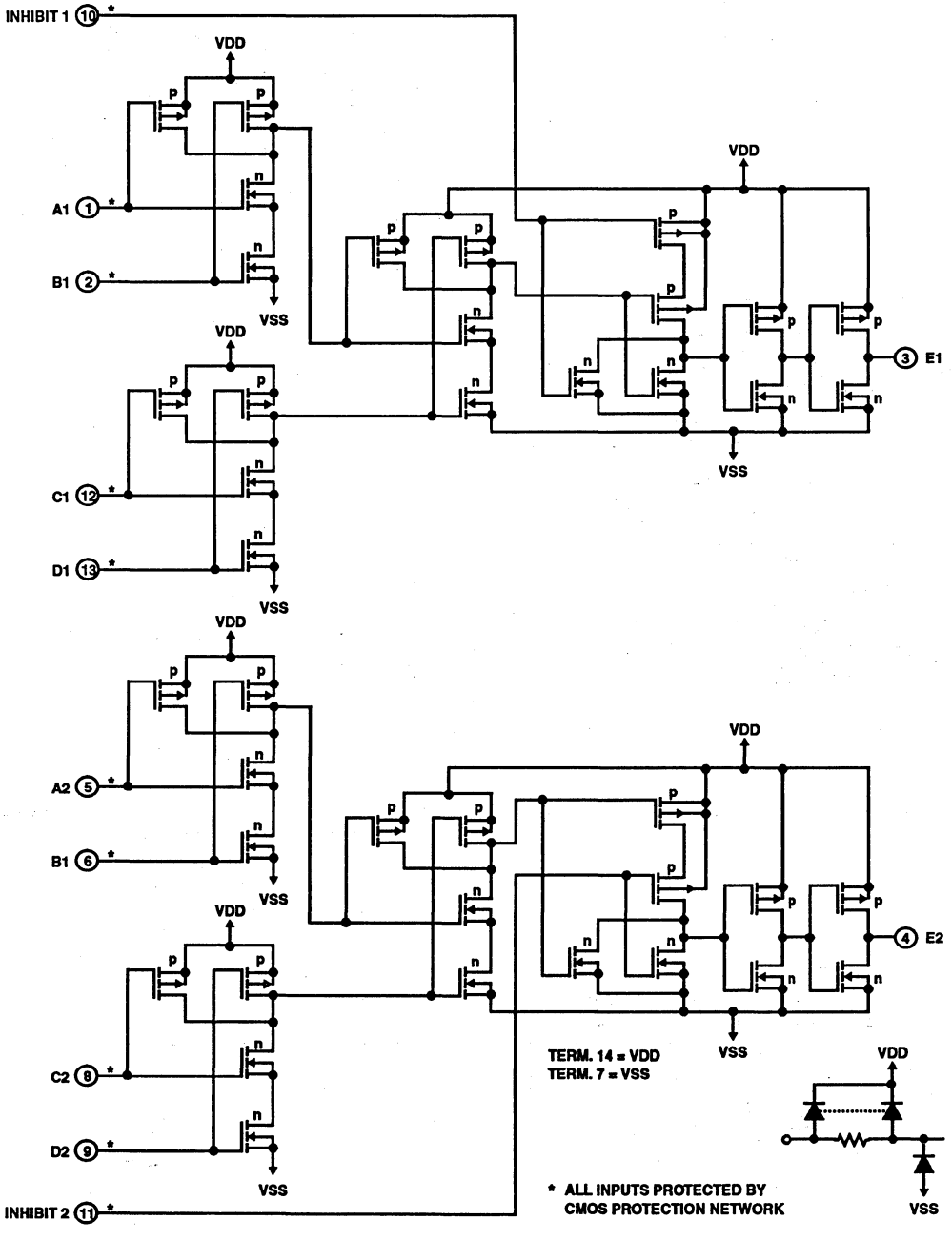


FIGURE 1. CD408B SCHEMATIC DIAGRAM

Typical Performance Characteristics

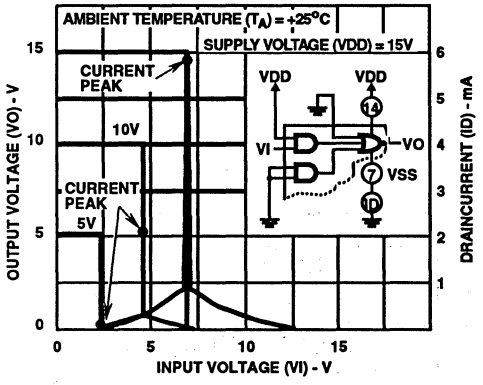


FIGURE 2. TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

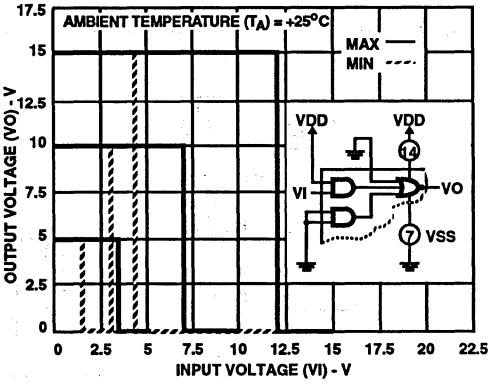


FIGURE 3. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS

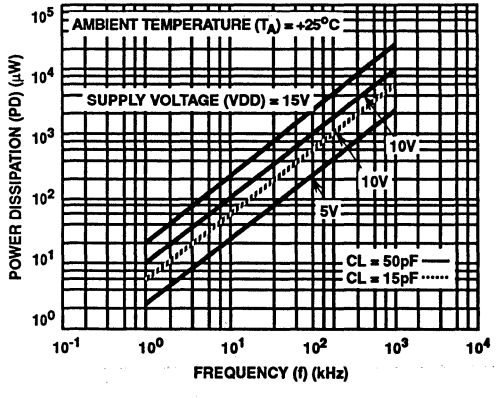


FIGURE 4. TYPICAL POWER DISSIPATION vs FREQUENCY

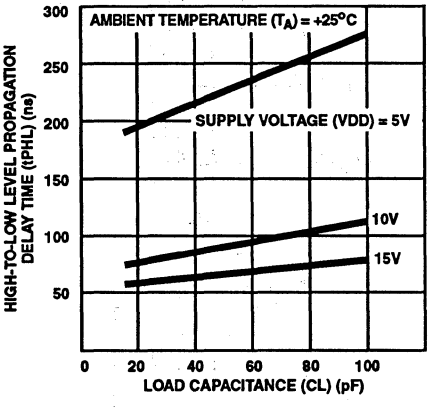


FIGURE 5. TYPICAL DATA HIGH-TO-LOW LEVEL PROPAGATION DELAY TIME vs LOAD CAPACITANCE

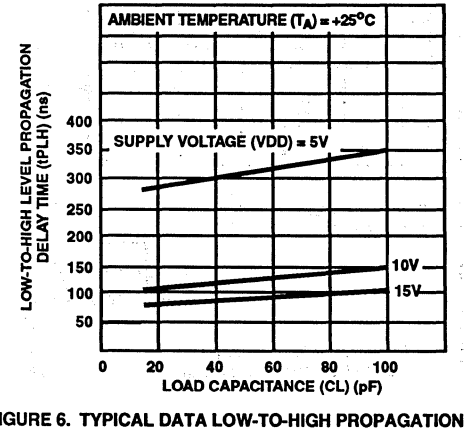


FIGURE 6. TYPICAL DATA LOW-TO-HIGH PROPAGATION DELAY TIME vs LOAD CAPACITANCE

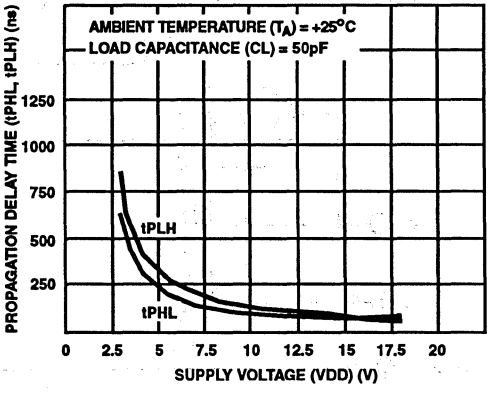


FIGURE 7. TYPICAL DATA PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

Typical Performance Characteristics (Continued)

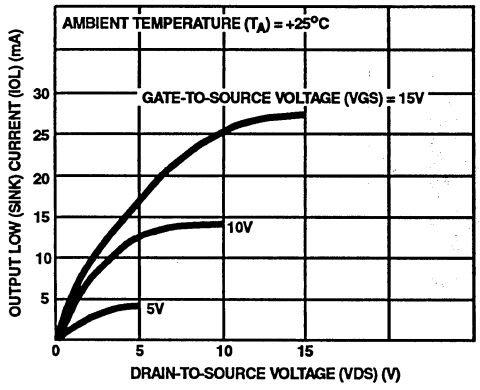


FIGURE 8. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

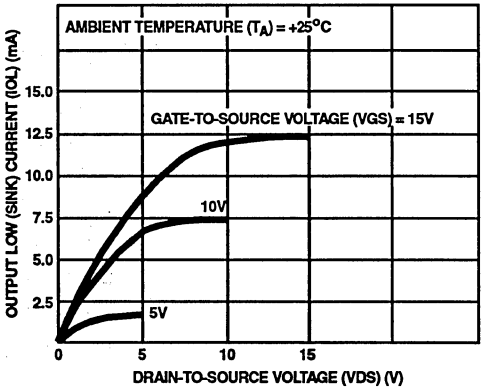


FIGURE 9. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

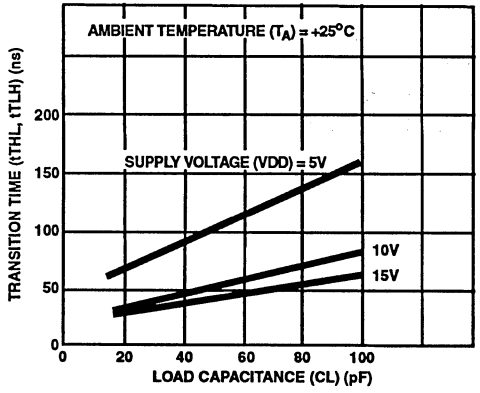


FIGURE 10. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

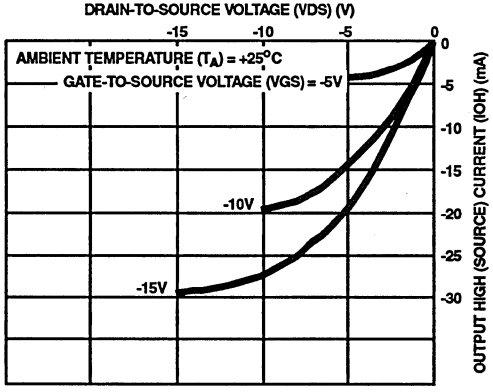


FIGURE 11. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

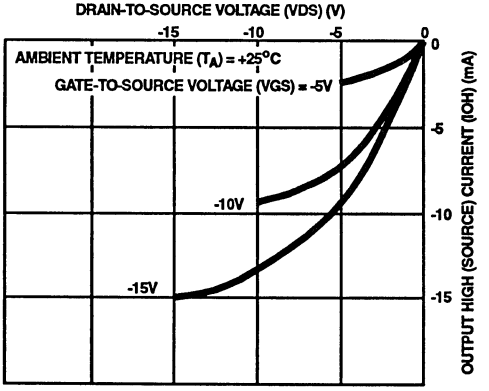
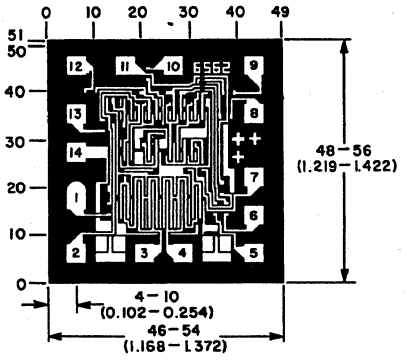


FIGURE 12. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4086BMS

CMOS Expandable 4-Wide 2-Input AND-OR-INVERT Gate

December 1992

Features

- Medium Speed Operation - tPHL = 90ns; tPLH = 140ns (Typ.) at 10V
- High Voltage Type (20V Rating)
- INHIBIT and ENABLE Inputs
- Buffered Outputs
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Standardized Symmetrical Output Characteristics
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Description

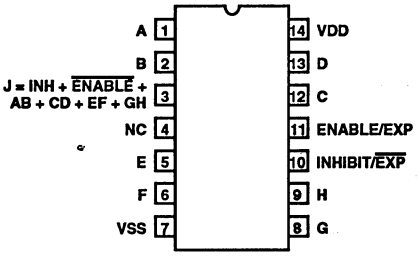
CD4086BMS contains one 4-wide 2-input AND-OR-INVERT gate with an INHIBIT/$\overline{EXP}$ input and an ENABLE/EXP input. For a 4-wide A-O-I function INHIBIT/EXP is tied to VSS and ENABLE/$\overline{EXP}$ to VDD. See Figure 2 and its associated explanation for applications where a capability greater than 4-wide is required.

The CD4076B is supplied in these 14 lead outline packages:

Braze Seal DIP	H4H
Frit Seal DIP	H1B
Ceramic Flatpack	H4F

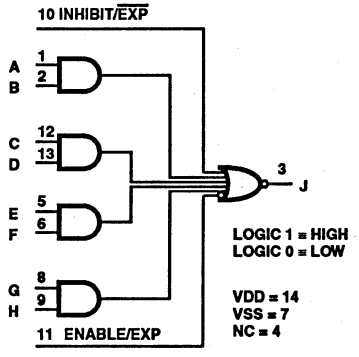
Pinout

CD4086BMS
TOP VIEW



NC = NO CONNECTION

Functional Diagram



$J = INH + \overline{ENABLE} + AB + CD + EF + GH$

7 LOGIC

File Number 3328

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN_s= VDD or GND		3	-55°C	-	2	µA
Input Leakage	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTES 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay DATA	TPHL1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	450	ns
			10, 11	+125°C, -55°C	-	608	ns
Propagation Delay DATA	TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	620	ns
			10, 11	+125°C, -55°C	-	837	ns
Propagation Delay INHIBIT	TPHL2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	300	ns
			10, 11	+125°C, -55°C	-	405	ns
Propagation Delay INHIBIT	TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-2.6	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay DATA	TPHL1	VDD = 10V	1, 2, 3	+25°C	-	180	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Propagation Delay DATA	TPLH1	VDD = 10V	1, 2, 3	+25°C	-	250	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns
Propagation Delay INHIBIT	TPHL2	VDD = 10V	1, 2, 3	+25°C	-	120	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Propagation Delay INHIBIT	TPLH2	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	140	ns
Transition Time	TTHL1 TTLH1	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	3, 4	1, 2, 5 - 13	14			
Static Burn-In 2 Note 1	3, 4	7	1, 2, 5, 6, 8 - 14			
Dynamic Burn-In Note 1	4	7	14	3	1, 2, 5, 6, 8, 9, 12, 13	10, 11
Irradiation Note 2	3, 4	7	1, 2, 5, 6, 8 - 14			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

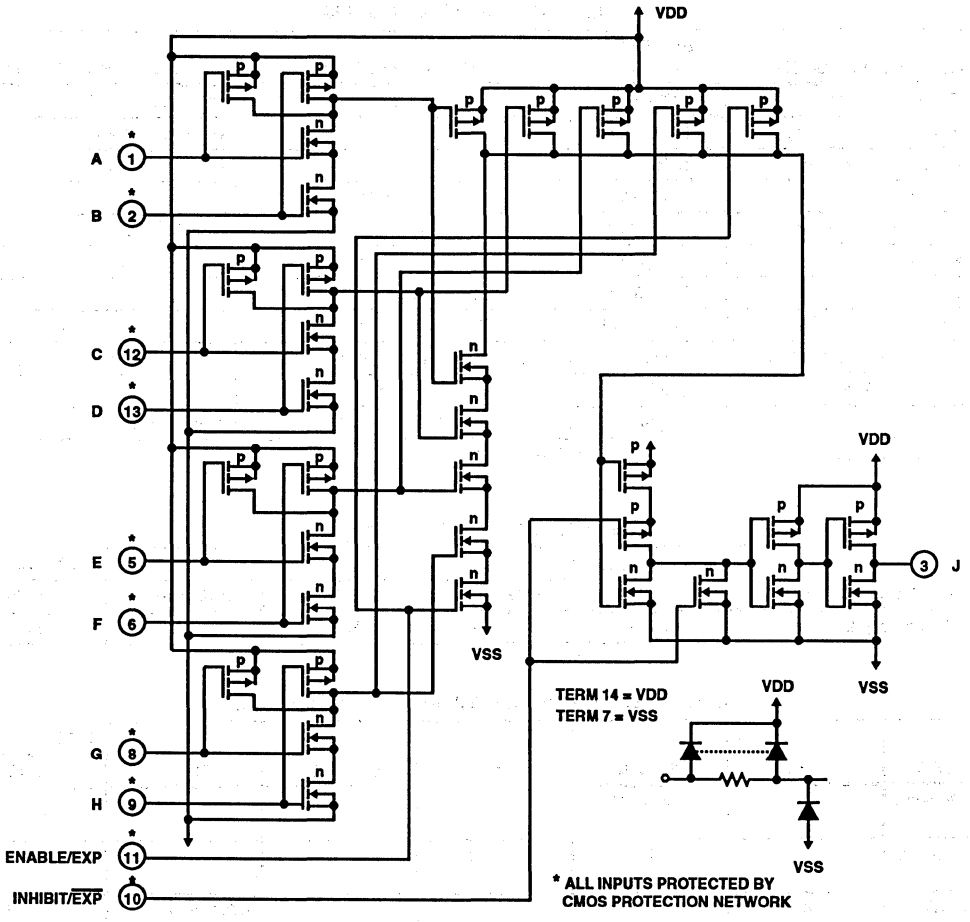


FIGURE 1. SCHEMATIC DIAGRAM

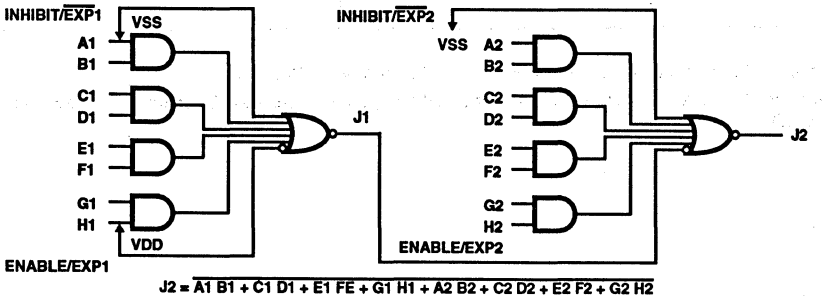


FIGURE 2. TWO CD4086BMS'S CONNECTED AS AN 8-WIDE 2-INPUT A-O-I GATE

Figure 2 above shows two CD4086's utilized to obtain 8-wide 2-input A-O-I function. The output (J1) of one CD4086 is fed directly to the ENABLE/EXP2 line of the second CD4086. In a similar fashion, any NAND gate output can be fed directly into the ENABLE/EXP input to obtain a 5-wide A-O-I function. In addition, and AND gate output can be fed directly into the INHIBIT/$\overline{\text{EXP}}$ input with the same result.

Typical Performance Characteristics

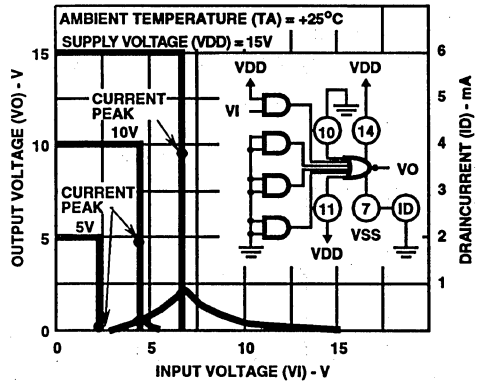


FIGURE 3. TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

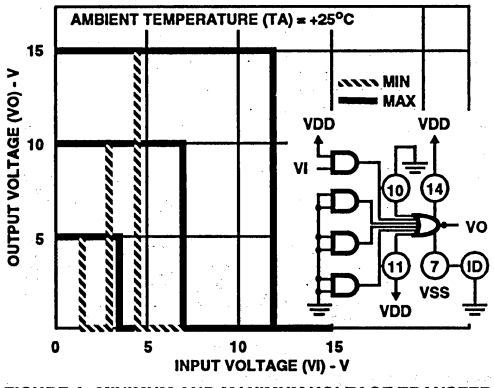


FIGURE 4. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS

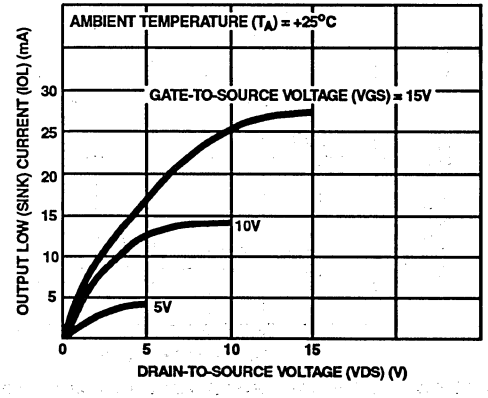


FIGURE 5. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

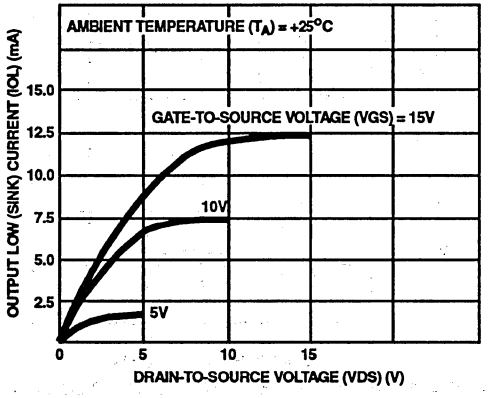


FIGURE 6. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

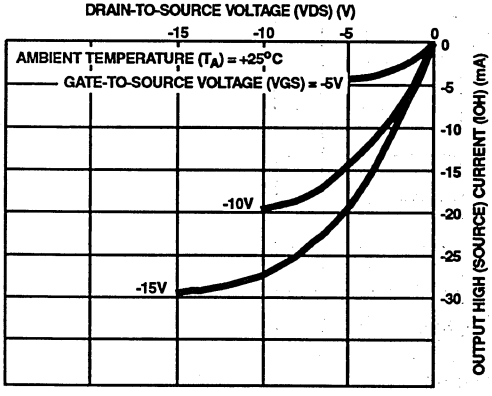


FIGURE 7. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

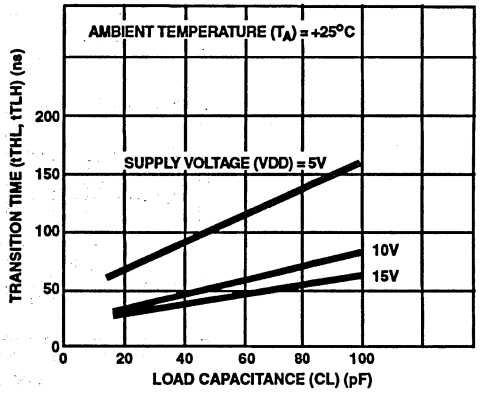


FIGURE 8. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

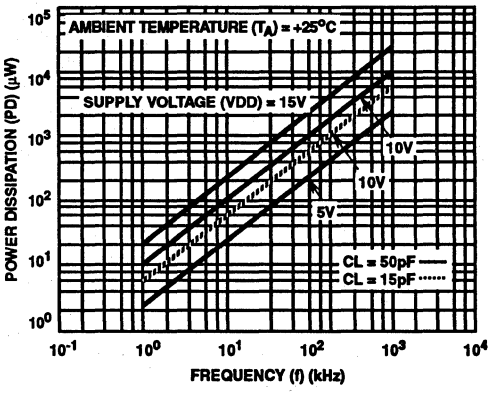


FIGURE 9. TYPICAL POWER DISSIPATION vs FREQUENCY

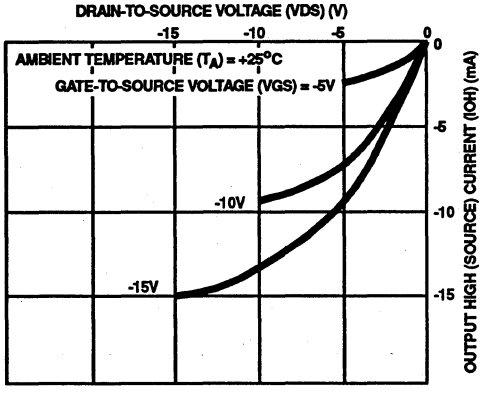


FIGURE 10. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

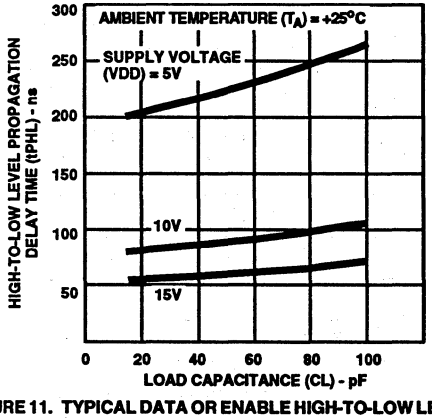


FIGURE 11. TYPICAL DATA OR ENABLE HIGH-TO-LOW LEVEL PROPAGATION DELAY TIME vs LOAD CAPACITANCE

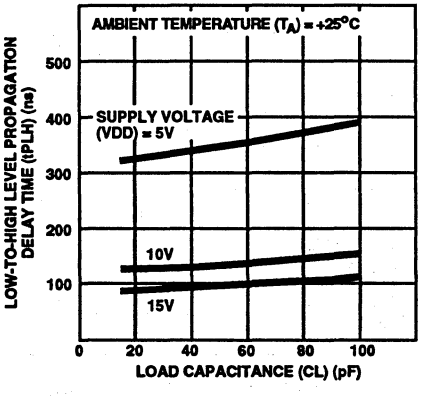


FIGURE 12. TYPICAL DATA OR ENABLE LOW-TO-HIGH LEVEL PROPAGATION DELAY TIME vs LOAD CAPACITANCE

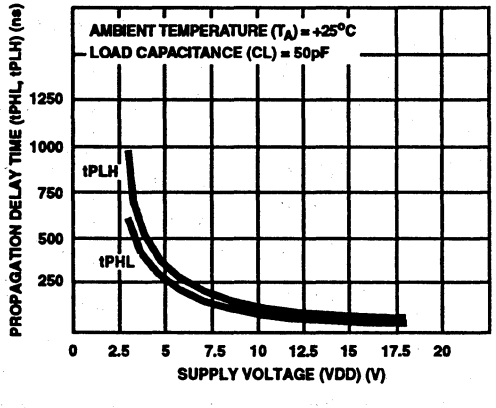
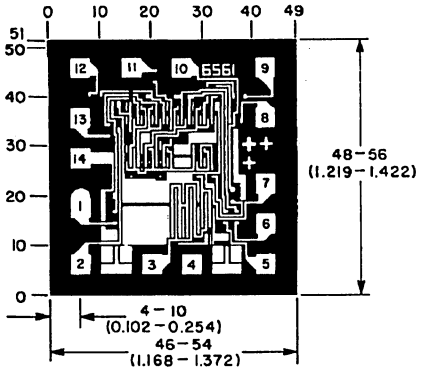


FIGURE 13. TYPICAL DATA OR ENABLE PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4089BMS

CMOS Binary Rate Multiplier

December 1992

Features

- High Voltage Type (20V Rating)
- Cascadable in Multiples of 4 Bits
- Set to "15" Input and "15" Detect Output
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Standardized Symmetrical Output Characteristics
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Numerical Control
- Instrumentation
- Digital Filtering
- Frequency Synthesis

Description

CD4089BMS is a low power 4 bit digital rate multiplier that provides an output pulse rate that is the clock-input-pulse rate multiplied by $^1/_{16}$ times the binary input. For example, when the binary input number is 13, there will be 13 output pulses for every 16 input pulses. This device may be used in conjunction with an up/down counter and control logic used to perform arithmetic operations (adds, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigometric functions, A/D and D/A conversions, and frequency division.

For words of more than 4 bits, CD4089BMS devices may be cascaded in two different modes: an Add mode and a Multiply mode (see Figures 3 and 4). In the Add mode some of the gaps left by the more significant unit at the count of 15 are filled in by the less significant units. For example, when two units are cascaded in the Add mode and programmed to 11 and 13, respectively, the more significant unit will have 11 output pulses for every 16 input pulses and the other unit will have 13 output pulses for every 256 input pulses for a total of

$$\frac{11}{16} + \frac{13}{256} = \frac{189}{256}$$

In the Multiply mode the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second multiplier. Thus the output rate will be

$$\frac{11}{16} \times \frac{13}{16} = \frac{143}{256}$$

The CD4089BMS has an internal synchronous 4 bit counter which, together with one of the four binary input bits, produces pulse trains as shown in Figure 6.

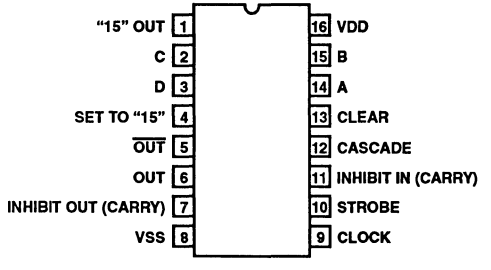
If more than one binary input bit is high, the resulting pulse train is a combination of the separate pulse trains as shown in Figure 6.

The CD4089BMS is supplied in these 16-lead outline packages:

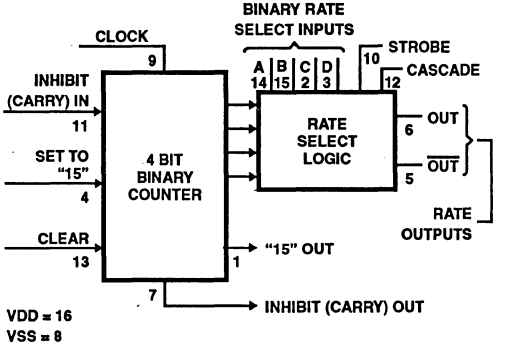
Braze Seal DIP	H4W
Frit Seal DIP	H2R
Ceramic Flatpack	H6P

Pinout

CD4089BMS
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3329

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTES 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Output	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	300	ns
			10, 11	+125°C, -55°C	-	405	ns
Propagation Delay Clear to Out	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	760	ns
			10, 11	+125°C, -55°C	-	1026	ns
Propagation Delay Cascade to Out	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	180	ns
			10, 11	+125°C, -55°C	-	243	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	1.2	-	MHz
			10, 11	+125°C, -55°C	.89	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL5	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL10	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH5	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH10	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Clock to $\overline{\text{Out}}$	TPHL4 TPLH4	VDD = 5V	1, 2, 3	+25°C	-	220	ns
		VDD = 10V	1, 2, 3	+25°C	-	110	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns
Propagation Delay Clock to Out	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	150	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Propagation Delay Clock to Inhibit Out	TPHL5	VDD = 5V	1, 2, 3	+25°C	-	720	ns
		VDD = 10V	1, 2, 3	+25°C	-	320	ns
		VDD = 15V	1, 2, 3	+25°C	-	220	ns
Propagation Delay Clock to Inhibit Out	TPLH5	VDD = 5V	1, 2, 3	+25°C	-	500	ns
		VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	150	ns
Propagation Delay Clear to Out	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	350	ns
		VDD = 15V	1, 2, 3	+25°C	-	260	ns
Propagation Delay Cascade to Out	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25°C	-	90	ns
		VDD = 15V	1, 2, 3	+25°C	-	70	ns
Propagation Delay Clock to "9" or "15" Out	TPHL6 TPLH6	VDD = 5V	1, 2, 3	+25°C	-	600	ns
		VDD = 10V	1, 2, 3	+25°C	-	250	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns
Propagation Delay Inhibit In to Inhibit Out	TPHL7 TPLH7	VDD = 5V	1, 2, 3	+25°C	-	320	ns
		VDD = 10V	1, 2, 3	+25°C	-	150	ns
		VDD = 15V	1, 2, 3	+25°C	-	110	ns
Propagation Delay Set to Out	TPHL8 TPLH8	VDD = 5V	1, 2, 3	+25°C	-	660	ns
		VDD = 10V	1, 2, 3	+25°C	-	300	ns
		VDD = 15V	1, 2, 3	+25°C	-	220	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	2.5	-	MHz
		VDD = 15V	1, 2, 3	+25°C	3.5	-	MHz
Minimum Inhibit-In Setup Time	TSU	VDD = 5V	1, 2, 3	+25°C	-	100	ns
		VDD = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V	1, 2, 3	+25°C	-	20	ns
Minimum Inhibit-In Removal Time	TREM	VDD = 5V	1, 2, 3	+25°C	-	240	ns
		VDD = 10V	1, 2, 3	+25°C	-	130	ns
		VDD = 15V	1, 2, 3	+25°C	-	110	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	330	ns
		VDD = 10V	1, 2, 3	+25°C	-	170	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Maximum Clock Rise and Fall Time	TRCL TFCL	VDD = 5V	1, 2, 3, 4	+25°C	-	15	µs
		VDD = 10V	1, 2, 3, 4	+25°C	-	15	µs
		VDD = 15V	1, 2, 3, 4	+25°C	-	15	µs
Minimum Set Removal Time	TREM	VDD = 5V	1, 2, 3	+25°C	-	150	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Clear Removal Time	TREM	VDD = 5V	1, 2, 3	+25°C	-	60	ns
		VDD = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V	1, 2, 3	+25°C	-	30	ns
Minimum Set or Clear Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	160	ns
		VDD = 10V	1, 2, 3	+25°C	-	90	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. If more than one unit is cascaded, TRCL should be made less than or equal to the sumof the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	1, 5-7	2-4, 8-15	16			
Static Burn-In 2 (Note 1)	1, 5-7	8	2-4, 9-16			
Dynamic Burn-In (Note 1)	-	2, 4, 8, 10, 12-15	3, 16	1, 5-7	9	11
Irradiation (Note 2)	1, 5-7	8	2-4, 9-16			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram

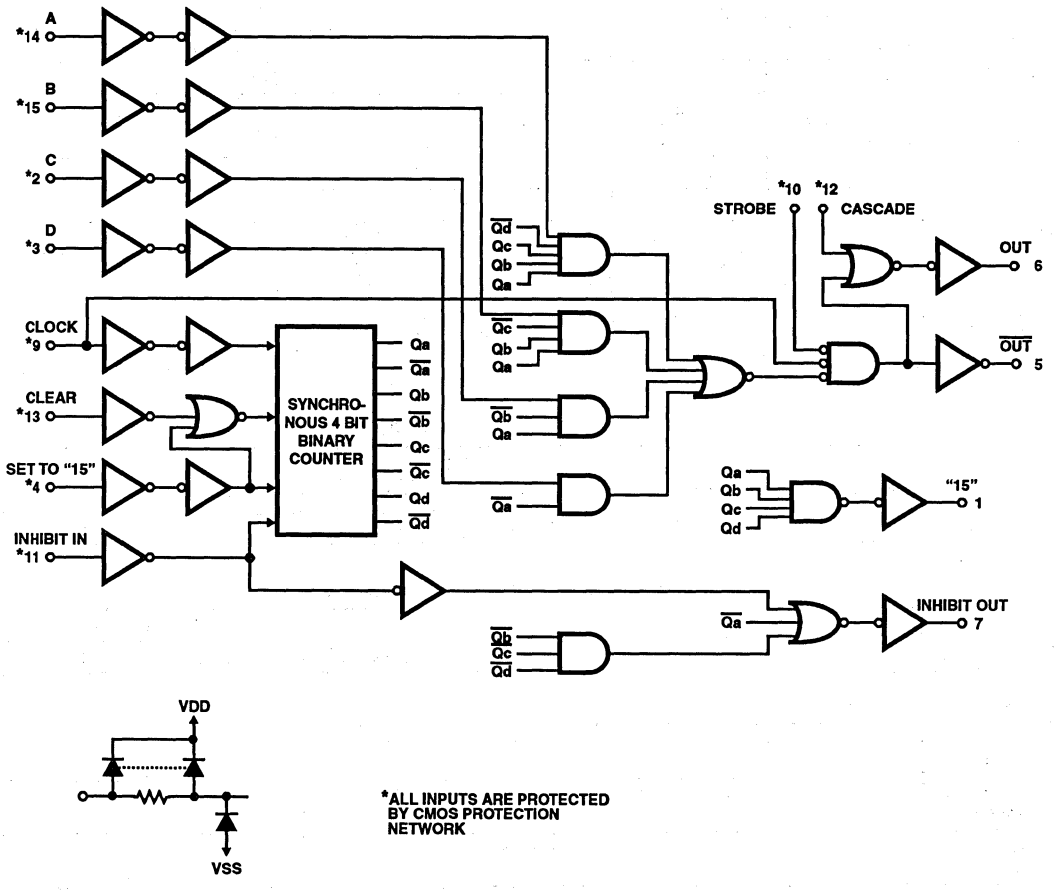


FIGURE 1. LOGIC DIAGRAM

TRUTH TABLE

INPUTS										OUTPUTS			
NUMBER OF PULSES OR INPUT LOGIC LEVEL (0 = Low; 1 = High; X = Don't Care)										NUMBER OF PULSES OR OUTPUT LOGIC LEVEL (L = Low; H = High)			
D	C	B	A	CLK	INH IN	STR	CAS	CLR	SET	OUT	$\overline{OUT}$	INH OUT	"15" OUT
0	0	0	0	16	0	0	0	0	0	L	H	1	1
0	0	0	1	16	0	0	0	0	0	1	1	1	1
0	0	1	0	16	0	0	0	0	0	2	2	1	1
0	0	1	1	16	0	0	0	0	0	3	3	1	1
0	1	0	0	16	0	0	0	0	0	4	4	1	1
0	1	0	1	16	0	0	0	0	0	5	5	1	1
0	1	1	0	16	0	0	0	0	0	6	6	1	1
0	1	1	1	16	0	0	0	0	0	7	7	1	1
1	0	0	0	16	0	0	0	0	0	8	8	1	1
1	0	0	1	16	0	0	0	0	0	9	9	1	1
1	0	1	0	16	0	0	0	0	0	10	10	1	1
1	0	1	1	16	0	0	0	0	0	11	11	1	1
1	1	0	0	16	0	0	0	0	0	12	12	1	1
1	1	0	1	16	0	0	0	0	0	13	13	1	1
1	1	1	0	16	0	0	0	0	0	14	14	1	1
1	1	1	1	16	0	0	0	0	0	15	15	1	1
X	X	X	X	16	1	0	0	0	0	**	**	H	**
X	X	X	X	16	0	1	0	0	0	L	H	1	1
X	X	X	X	16	0	0	1	0	0	H	*	1	1
1	X	X	X	16	0	0	0	1	0	16	16	H	L
0	X	X	X	16	0	0	0	1	0	L	H	H	L
X	X	X	X	16	0	0	0	X	1	L	H	L	H

* Output same as the first 16 lines of this truth table (depending on values A, B, C, D)

** Depends on internal state of counter

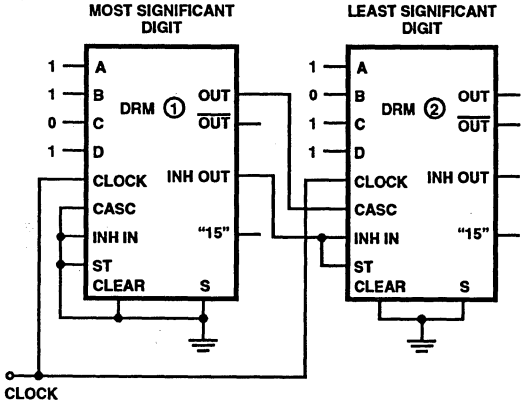


FIGURE 2. TWO CD4089BMS's CASCADED IN THE "ADD" MODE WITH A PRESET NUMBER OF 189 $\left(\frac{11}{16} + \frac{13}{256} = \frac{189}{256}\right)$

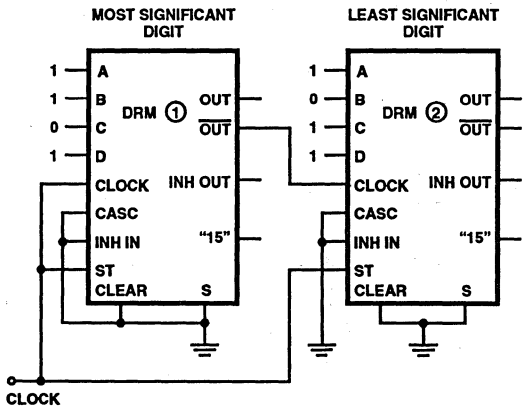


FIGURE 3. TWO CD4089BMS's CASCADED IN THE "MULTIPLY" MODE WITH A PRESET NUMBER OF 143 $\left(\frac{11}{16} + \frac{13}{16} = \frac{143}{256}\right)$

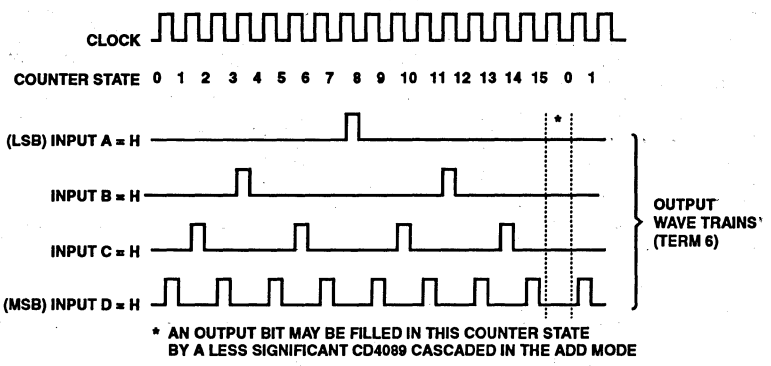


FIGURE 4. TIMING DIAGRAM

Typical Performance Characteristics

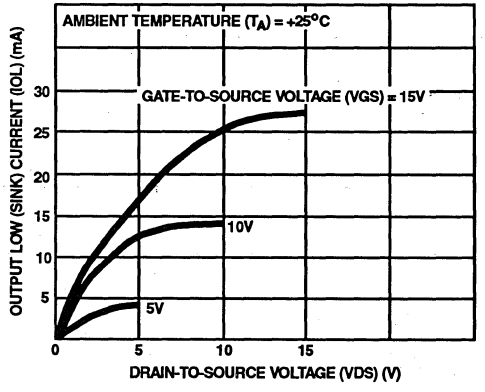


FIGURE 5. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

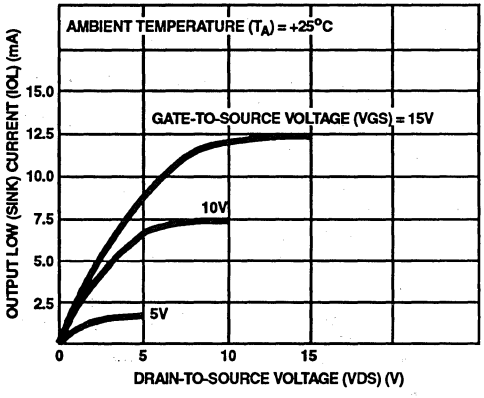


FIGURE 6. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

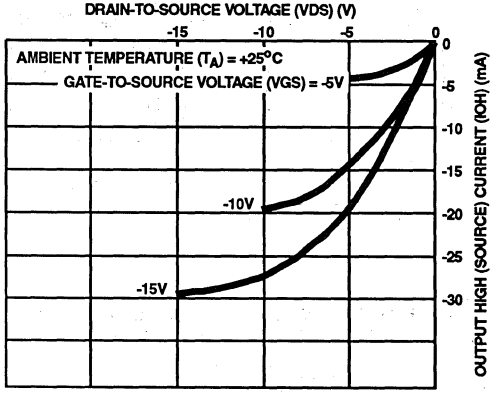


FIGURE 7. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

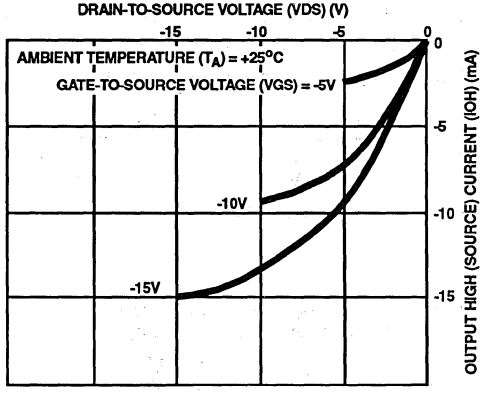


FIGURE 8. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

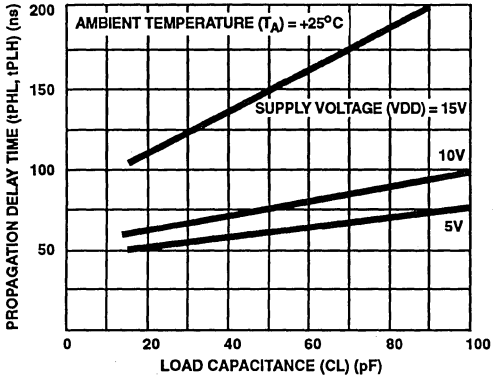


FIGURE 9. TYP. PROPAGATION DELAY TIMES AS FUNCTION OF LOAD CAPACITANCE (CLOCK OR STROBE TO OUT)

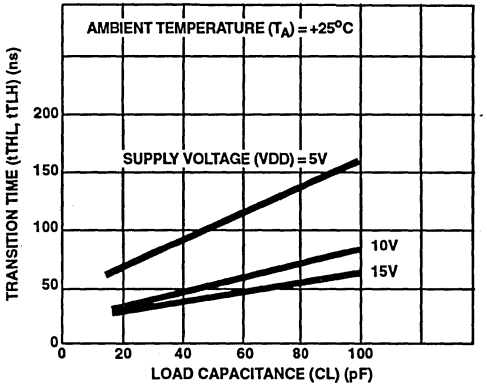


FIGURE 10. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

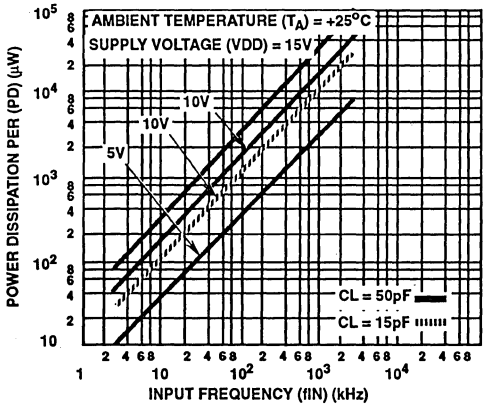
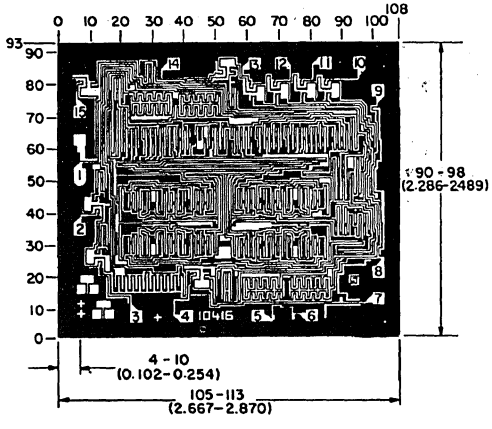


FIGURE 11. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4093BMS

CMOS Quad 2-Input NAND Schmitt Triggers

December 1992

Features

- High Voltage Types (20V Rating)
- Schmitt Trigger Action on Each Input With No External Components
- Hysteresis Voltage Typically 0.9V at VDD = 5V and 2.3V at VDD = 10V
- Noise Immunity Greater than 50%
- No Limit on Input Rise and Fall Times
- Standardized, Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range, 100nA at 18V and +25°C
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Wave and Pulse Shapers
- High Noise Environment Systems
- Monostable Multivibrators
- Astable Multivibrators
- NAND Logic

Description

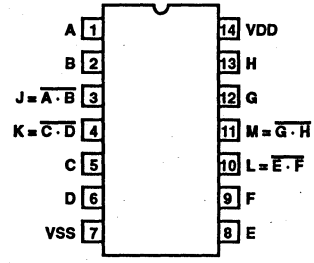
CD4093BMS consists of four Schmitt trigger circuits. Each circuit functions as a two input NAND gate with Schmitt trigger action on both inputs. The gate switches at different points for positive and negative going signals. The difference between the positive voltage (VP) and the negative voltage (VN) is defined as hysteresis voltage (VH) (see Figure 1).

The CD4093BMS is supplied in these 14 lead outline packages:

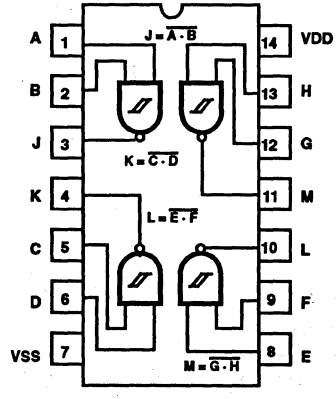
Braze Seal DIP	H4H
Frit Seal DIP	H1B
Ceramic Flatpack	H3W

Pinout

CD4093BMSMS
TOP VIEW



Functional Diagram



Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 5)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Positive Trigger Threshold Voltage	VP5V	VDD = 5V (Note 2)		1, 2, 3	+25°C, +125°C, -55°C	2.2	3.6	V
	VP15V	VDD = 15V (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	6.8	10.8	V
Positive Trigger Threshold Voltage	VP5V	VDD = 5V (Note 4)		1, 2, 3	+25°C, +125°C, -55°C	2.6	4.0	V
Negative Trigger Threshold Voltage	VN5V	VDD = 5V (Note 2)		1, 2, 3	+25°C, +125°C, -55°C	0.9	2.8	V
	VN15V	VDD = 15V (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	4.0	7.4	V
Negative Trigger Threshold Voltage	VN5V	VDD = 5V (Note 4)		1, 2, 3	+25°C, +125°C, -55°C	1.4	3.2	V
Hysteresis Voltage	VH5V	VDD = 5V (Note 2)		1, 2, 3	+25°C, +125°C, -55°C	0.3	1.6	V
	VH15V	VDD = 15V (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	1.6	5.0	V
Hysteresis Voltage	VH5V	VDD = 5V (Note 4)		1, 2, 3	+25°C, +125°C, -55°C	0.3	1.6	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Inputs on terminals 1, 5, 8, 12
3. Input on Terminal 1
4. Input on terminals 1 and 2, 5 and 6, 8 and 9, or 12 and 13
5. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTES 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	380	ns
			10, 11	+125°C, -55°C	-	513	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Propagation Delay	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	180	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Positive Trigger Threshold Voltage	VP10V	VDD = 10V	1, 2, 4	+25°C, +125°C, -55°C	4.6	7.1	V
	VP10V	VDD = 10V	1, 2, 5	+25°C, +125°C, -55°C	5.6	8.2	V
	VP15V	VDD = 15V	1, 2, 5	+25°C, +125°C, -55°C	6.3	12.7	V
Negative Trigger Threshold Voltage	VN10V	VDD = 10V	1, 2, 4	+25°C, +125°C, -55°C	2.5	5.2	V
	VN10V	VDD = 10V	1, 2, 5	+25°C, +125°C, -55°C	3.4	6.6	V
	VN15V	VDD = 15V	1, 2, 5	+25°C, +125°C, -55°C	4.8	9.6	V
Hysteresis Voltage	VH10V	VDD = 10V	1, 2, 4	+25°C, +125°C, -55°C	1.2	3.4	V
	VH10V	VDD = 10V	1, 2, 5	+25°C, +125°C, -55°C	1.2	3.4	V
	VH15V	VDD = 15V	1, 2, 5	+25°C, +125°C, -55°C	1.6	5.0	V
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. Input on terminals 1, 5, 8, 12
5. Input on terminals 1 and 2, 5 and 6, 8 and 9, or 12 and 13

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

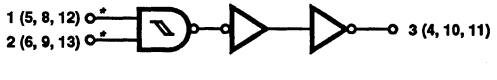
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	3, 4, 10, 11	1, 2, 5-9, 12, 13	14			
Static Burn-In 2 Note 1	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12-14			
Dynamic Burn-In Note 1	-	7	14	3, 4, 10, 11	1, 2, 5, 6, 8, 9, 12, 13	-
Irradiation Note 2	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12-14			

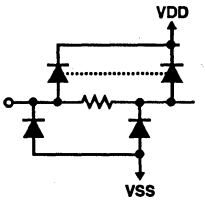
NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

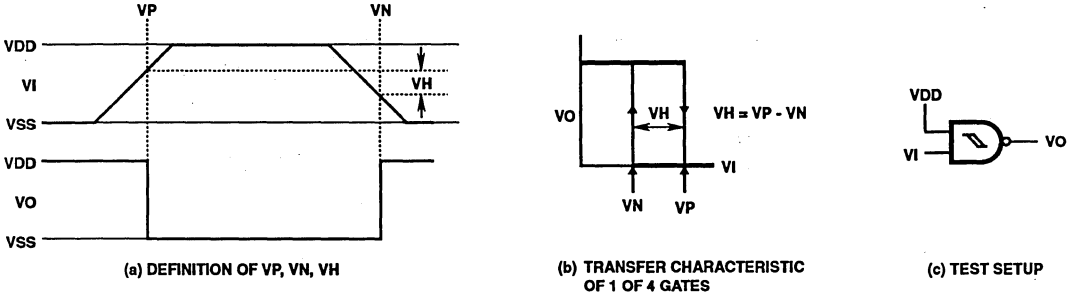
Logic Diagram



* All inputs protected by CMOS protection network



1 OF 4 SCHMITT TRIGGERS



(a) DEFINITION OF VP, VN, VH

(b) TRANSFER CHARACTERISTIC OF 1 OF 4 GATES

(c) TEST SETUP

FIGURE 1. HYSTERESIS DEFINITION, CHARACTERISTIC, AND TEST SETUP

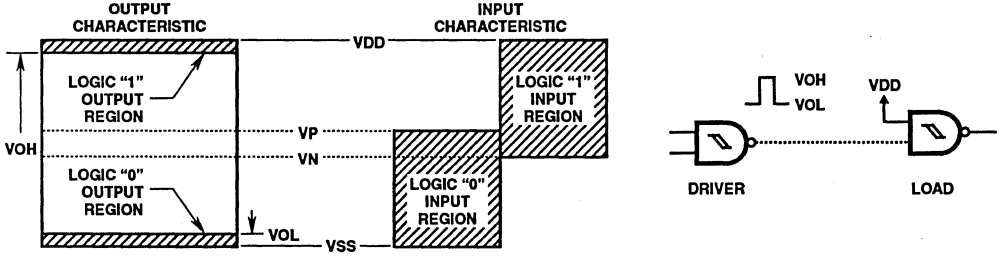


FIGURE 2. INPUT AND OUTPUT CHARACTERISTICS

Typical Performance Curves

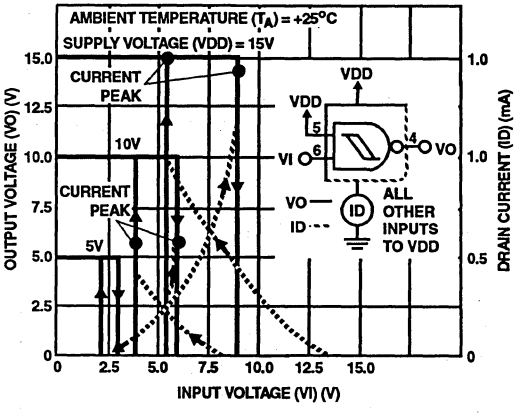


FIGURE 3. TYPICAL CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS

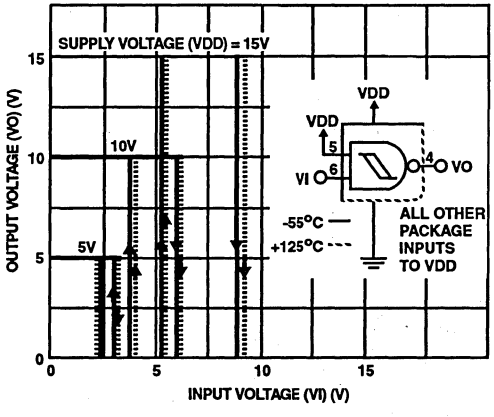


FIGURE 4. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE

Typical Performance Curves (Continued)

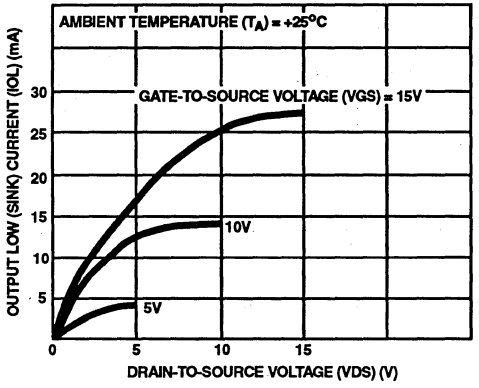


FIGURE 5. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

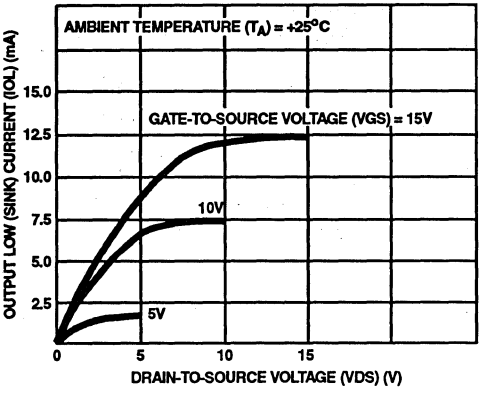


FIGURE 6. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

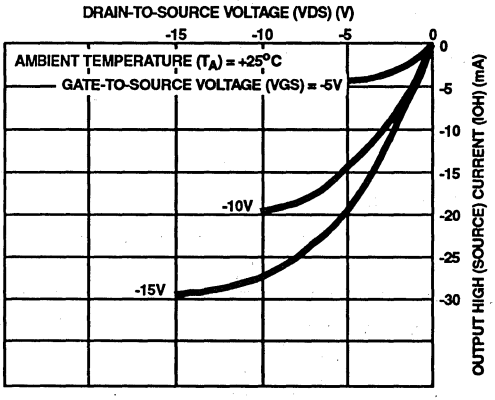


FIGURE 7. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

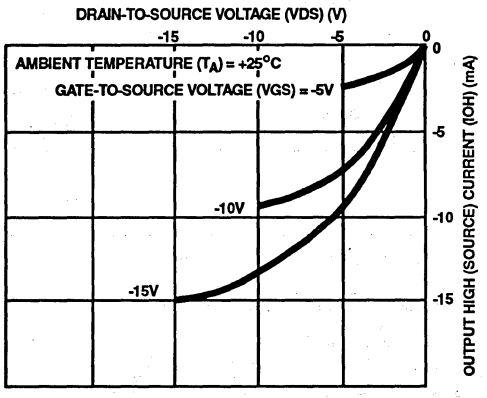


FIGURE 8. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

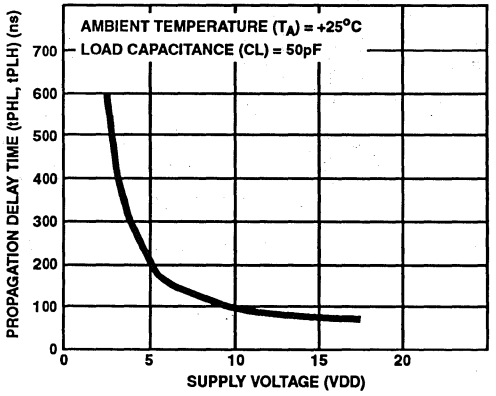


FIGURE 9. TYPICAL PROPAGATION DELAY TIME vs. SUPPLY VOLTAGE

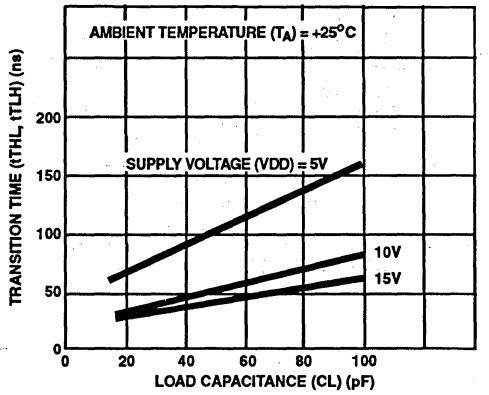


FIGURE 10. TYPICAL TRANSITION TIME vs. LOAD CAPACITANCE

Typical Performance Curves (Continued)

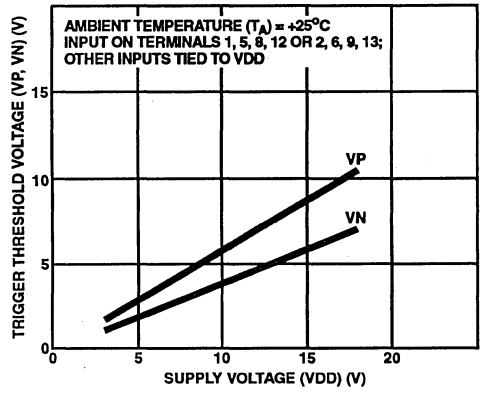


FIGURE 11. TYPICAL TRIGGER THRESHOLD VOLTAGE vs. VDD

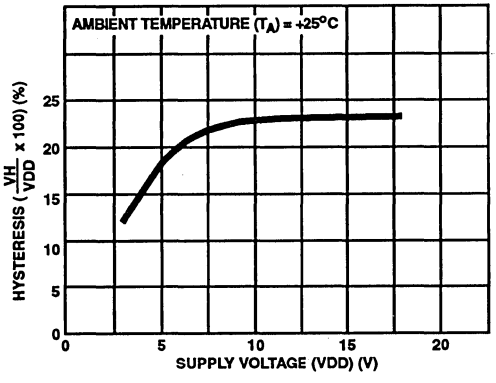


FIGURE 12. TYPICAL PERCENT HYSTERESIS vs. SUPPLY VOLTAGE

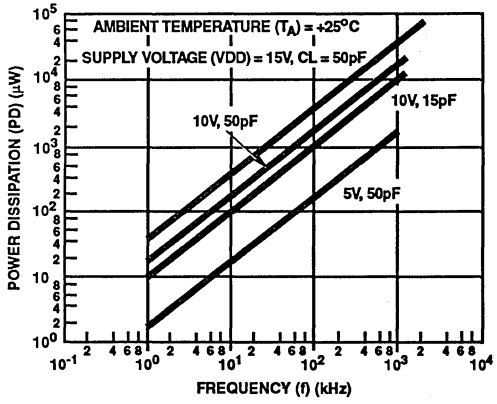


FIGURE 13. TYPICAL POWER DISSIPATION vs. FREQUENCY CHARACTERISTICS

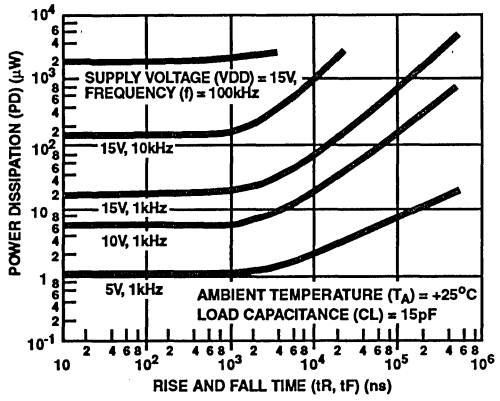
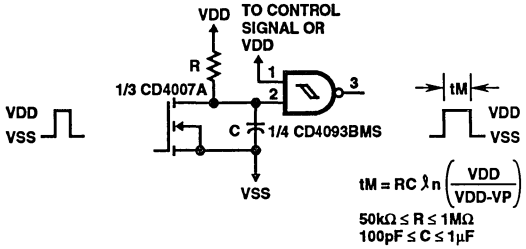


FIGURE 14. TYPICAL POWER DISSIPATION vs. RISE AND FALL TIMES

Applications

FREQUENCY RANGE OF WAVE SHAPE IS FROM DC TO 1MHz

FIGURE 15. WAVE SHAPER



FOR THE RANGE OF R AND C GIVEN 5µs < tM < 1s

FIGURE 16. MONOSTABLE MULTIVIBRATOR

Applications (Continued)

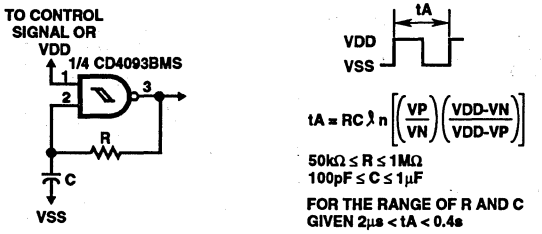
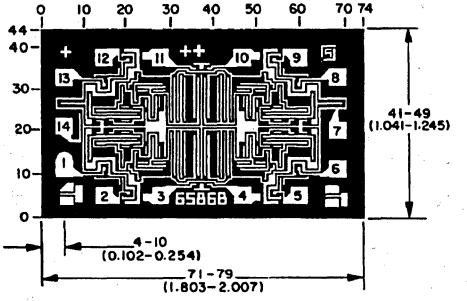


FIGURE 17. ASTABLE MULTIVIBRATOR

Chip Dimensions and Pad Layout



Dimension in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4094BMS

CMOS 8-Stage Shift-and-Store Bus Register

December 1992

Features

- High Voltage Type (20V Rating)
- 3-State Parallel Outputs for Connection to Common Bus
- Separate Serial Outputs Synchronous to Both Positive and Negative Clock Edges for Cascading
- Medium Speed Operation - 5MHz at 10V (typ)
- Standardized Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Serial-to-Parallel Data Conversion
- Remote Control Holding Register
- Dual-Rank Shift, Hold, and Bus Applications

Description

CD4094BMS is a 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the STROBE input is high. Data in the storage register appears at the outputs whenever the OUTPUT-ENABLE signal is high.

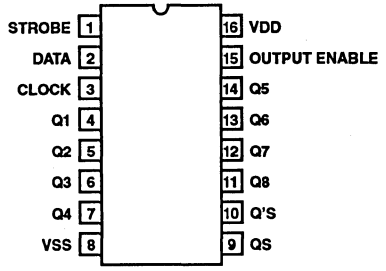
Two serial outputs are available for cascading a number of CD4094BMS devices. Data is available at the QS serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the Q'S terminal on the next negative clock edge, provides a means for cascading CD4094BMS devices when the clock rise time is slow.

The CD4094BMS is supplied in these 16 lead outline packages:

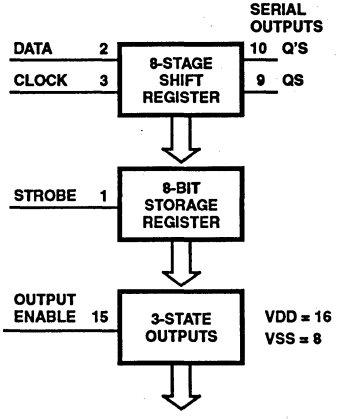
Braze Seal DIP	H4X
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

Pinout

CD4094BMS
TOP VIEW



Functional Diagram



PARALLEL OUTPUTS Q1 - Q8

(TERMINALS 4, 5, 6, 7, 14, 13, 12, 11, RESPECTIVELY)

7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3194

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.4	-	µA
				2	+125°C	-12	-	µA
			VDD = 18V	3	-55°C	-0.4	-	µA
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.4	µA
				2	+125°C	-	12	µA
			VDD = 18V	3	-55°C	-	0.4	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Serial Output QS	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Propagation Delay Clock to Serial Output Q'S	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	460	ns
			10, 11	+125°C, -55°C	-	621	ns
Propagation Delay Clock to Parallel Output	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	840	ns
			10, 11	+125°C, -55°C	-	1134	ns
Propagation Delay Strobe to Parallel Output	TPHL4 TPLH4	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	580	ns
			10, 11	+125°C, -55°C	-	783	ns
Propagation Delay Output Enable to Parallel Output	TPHZ TPZH	VDD = 5V, VIN = VDD or GND (Note 2, 3)	9	+25°C	-	280	ns
			10, 11	+125°C, -55°C	-	378	ns
Propagation Delay Output Enable to Parallel Output	TPLZ TPZL	VDD = 5V, VIN = VDD or GND (Note 2, 3)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	1.25	-	MHz
			10, 11	+125°C, -55°C	.93	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.
3. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.1	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-2.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Clock to Serial Output Qs	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	250	ns
		VDD = 15V	1, 2, 3	+25°C	-	190	ns
Propagation Delay Clock to Serial Output Q's	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	220	ns
		VDD = 15V	1, 2, 3	+25°C	-	150	ns
Propagation Delay Clock to Parallel Output	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25°C	-	390	ns
		VDD = 15V	1, 2, 3	+25°C	-	270	ns
Propagation Delay Strobe to Parallel Output	TPHL4 TPLH4	VDD = 10V	1, 2, 3	+25°C	-	290	ns
		VDD = 15V	1, 2, 3	+25°C	-	200	ns
Propagation Delay Output Enable to Parallel Output	TPHZ TPZH	VDD = 10V	1, 2, 4	+25°C	-	120	ns
		VDD = 15V	1, 2, 4	+25°C	-	90	ns
Propagation Delay Output Enable to Parallel Output	TPLZ TPZL	VDD = 10V	1, 2, 4	+25°C	-	100	ns
		VDD = 15V	1, 2, 4	+25°C	-	80	ns
Transition Time	TTLH TTHL	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	2.5	-	MHz
		VDD = 15V	1, 2, 3	+25°C	3	-	MHz
Minimum Data Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	125	ns
		VDD = 10V	1, 2, 3	+25°C	-	55	ns
		VDD = 15V	1, 2, 3	+25°C	-	35	ns
Maximum Clock Input Rise and Fall Time	TRCL TFCL	VDD = 5V	1, 2, 3, 5	+25°C	-	15	µs
		VDD = 10V	1, 2, 3, 5	+25°C	-	5	µs
		VDD = 15V	1, 2, 3, 5	+25°C	-	5	µs
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	83	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Minimum Strobe Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	70	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. CL = 50pF, RL = 1K, Input TR, TF < 20ns.
5. If more than one unit is cascaded, TRCL should be made less than or equal to the sumof the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	4 - 7, 9 - 14	1 - 3, 8, 15	16			
Static Burn-In 2 (Note 1)	4 - 7, 9 - 14	8	1 - 3, 15, 16			
Dynamic Burn-In (Note 1)	-	8	1, 15, 16	4 - 7, 9 - 14	3	2
Irradiation (Note 2)	4 - 7, 9 - 14	8	1 - 3, 15, 16			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

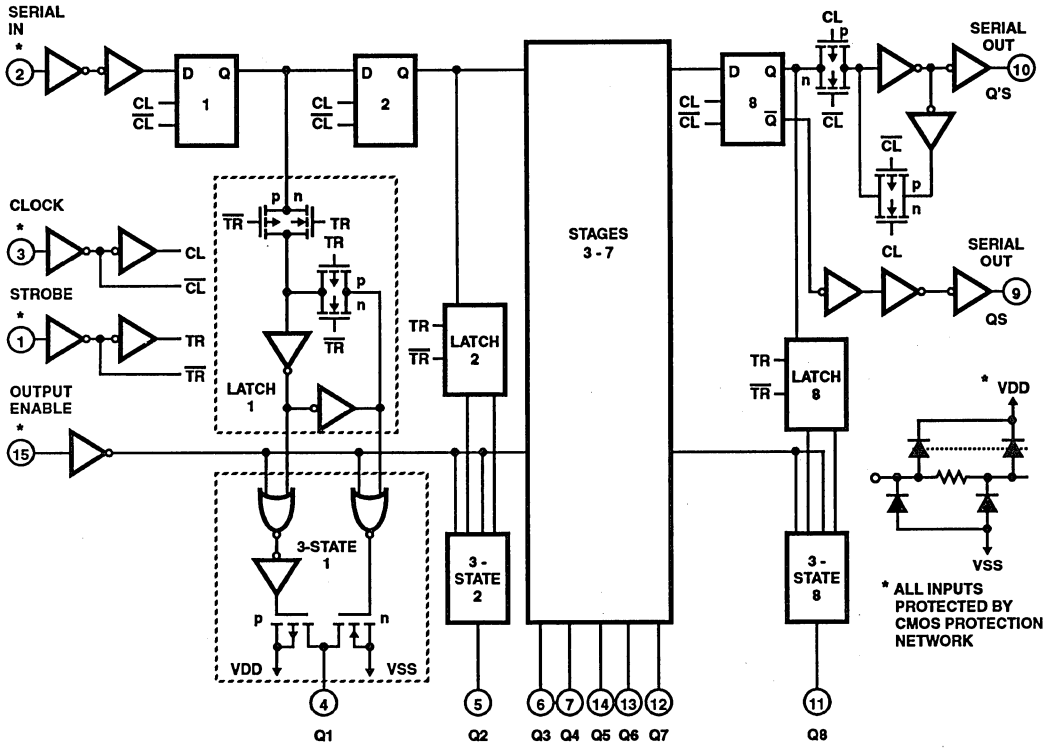


FIGURE 1. LOGIC DIAGRAM

TRUTH TABLE

CLΔ	OUTPUT ENABLE	STROBE	DATA	PARALLEL OUTPUTS		SERIAL OUTPUTS	
				Q1	QN	QS*	Q'S
↗	0	X	X	OC	OC	Q7	NC
↘	0	X	X	OC	OC	NC	Q7
↗	1	0	X	NC	NC	Q7	NC
↗	1	1	0	0	QN-1	Q7	NC
↗	1	1	1	1	QN-1	Q7	NC
↘	1	1	1	NC	NC	NC	Q7

Δ = Level Change
X = Don't Care
NC = No Change
OC = Open Circuit
Logic 1 = High
Logic 0 = Low

* At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the QS output

Typical Performance Characteristics

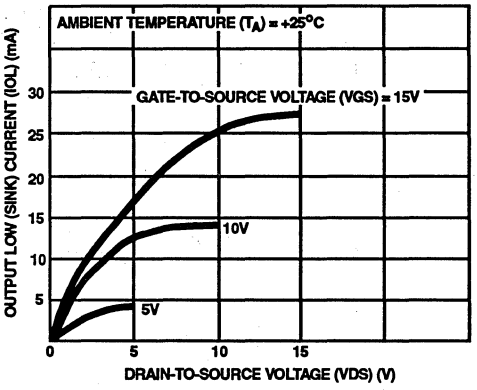


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT TRANSFER CHARACTERISTICS

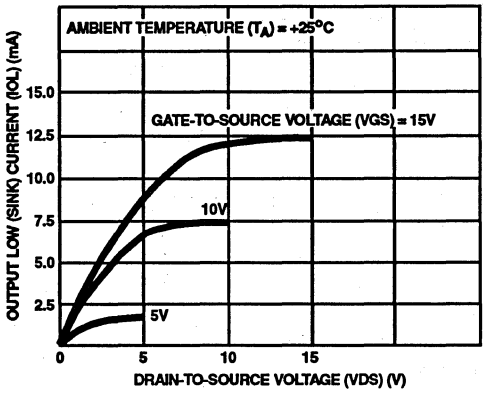


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

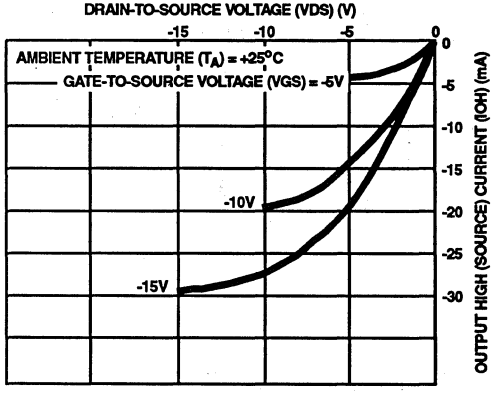


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

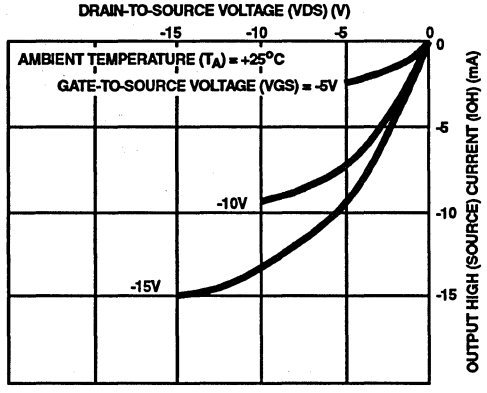


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

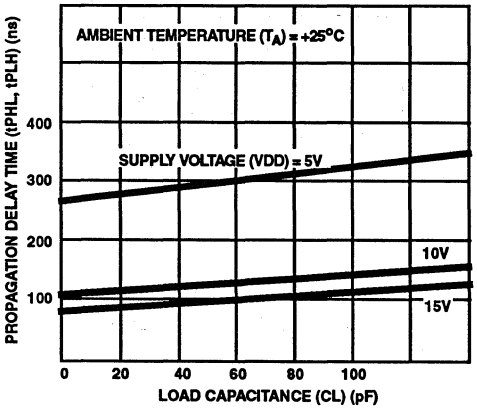


FIGURE 6. CLOCK-TO-SERIAL OUTPUT QS PROPAGATION DELAY vs CL

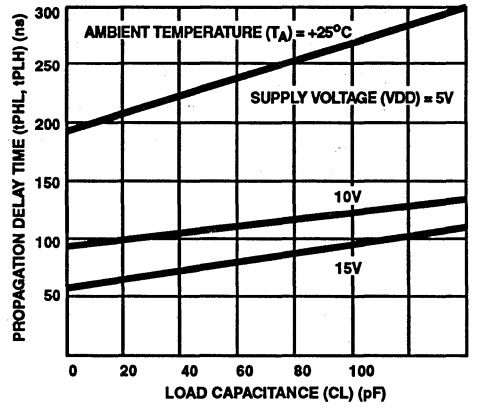


FIGURE 7. CLOCK-TO-SERIAL OUTPUT Q'S PROPAGATION DELAY vs CL

Typical Performance Characteristics (Continued)

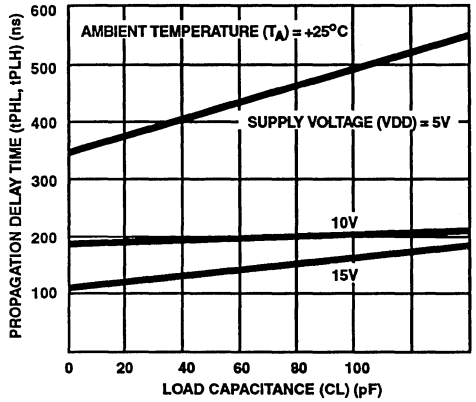


FIGURE 8. CLOCK-TO-PARALLEL OUTPUT PROPAGATION DELAY vs CL

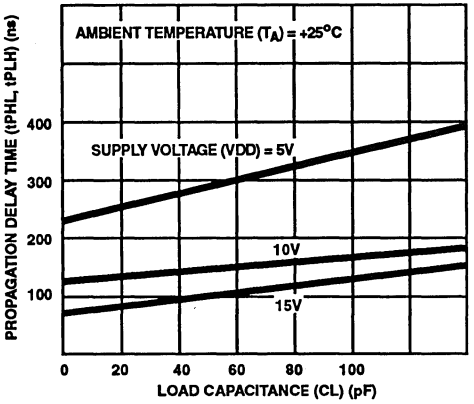


FIGURE 9. STROBE-TO-PARALLEL OUTPUT PROPAGATION DELAY vs CL

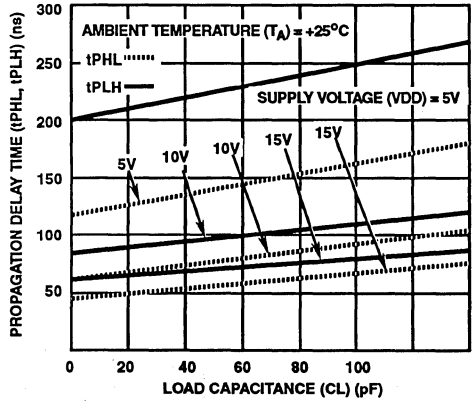


FIGURE 10. OUTPUT ENABLE-TO-PARALLEL OUTPUT PROPAGATION DELAY vs CL

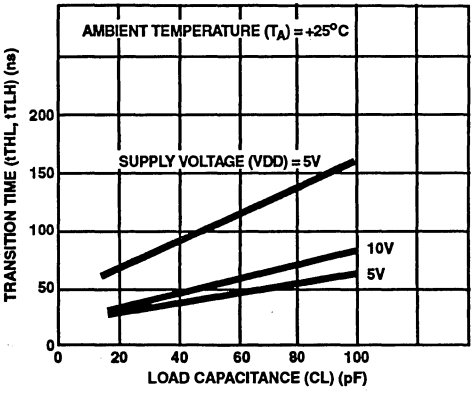


FIGURE 11. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

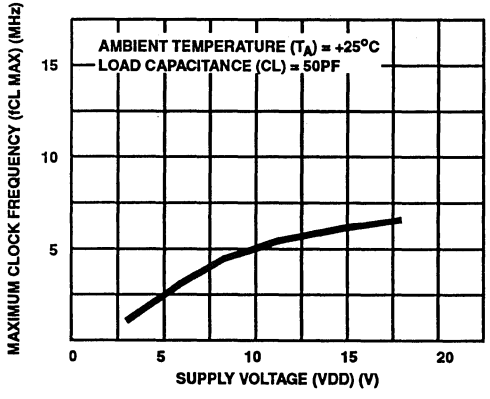


FIGURE 12. TYPICAL MAXIMUM-CLOCK-FREQUENCY vs SUPPLY VOLTAGE

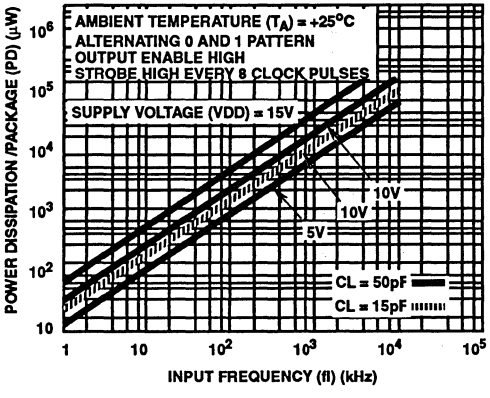


FIGURE 13. DYNAMIC POWER DISSIPATION vs INPUT CLOCK FREQUENCY

7 LOGIC

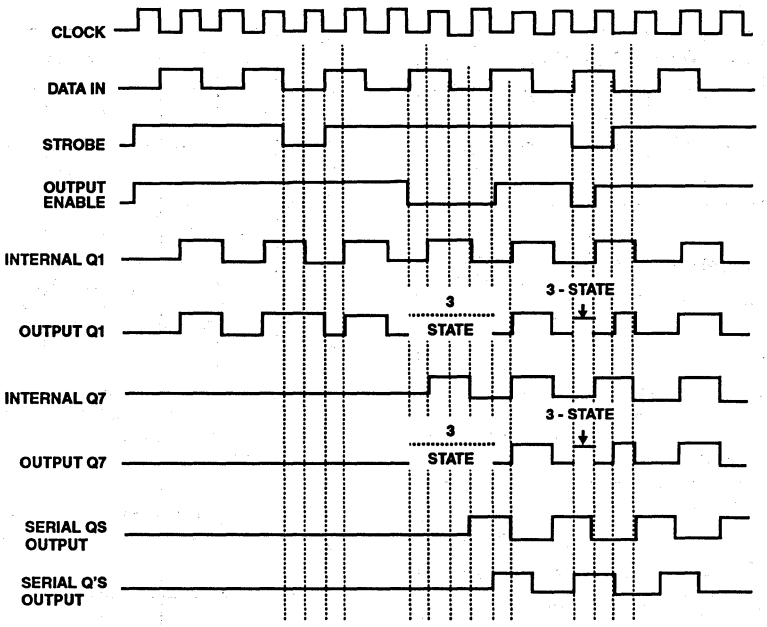


FIGURE 14. TIMING DIAGRAM

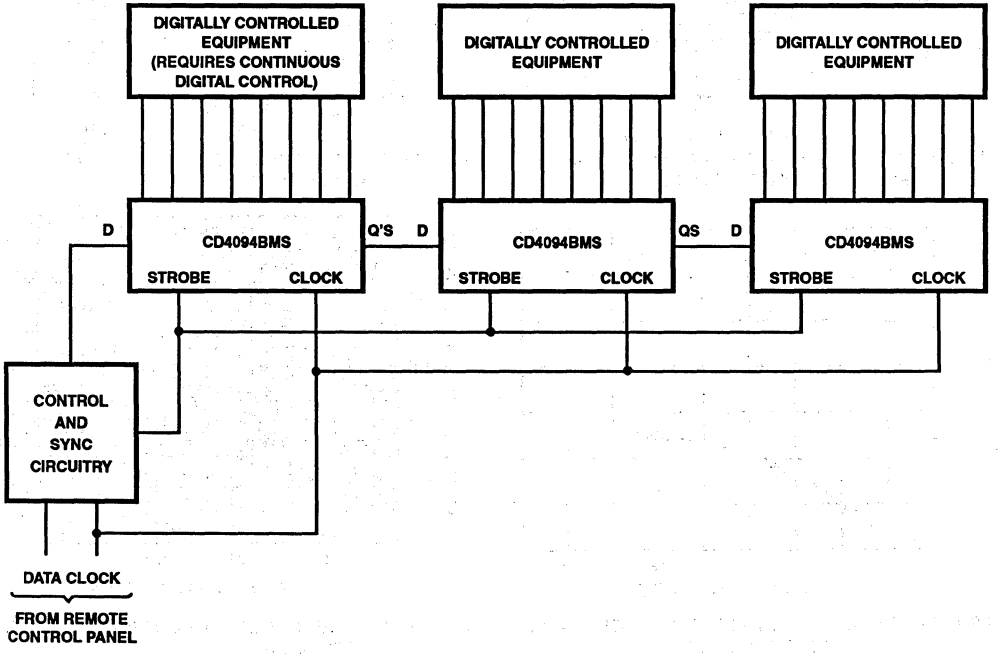
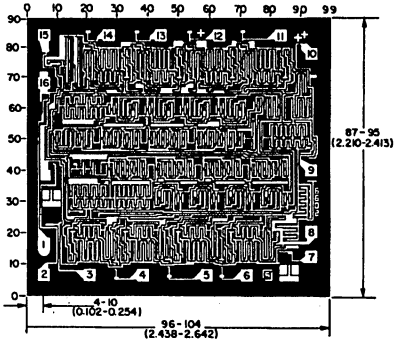


FIGURE 15. REMOTE CONTROL HOLDING REGISTER

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4095BMS
CD4096BMS

CMOS Gated J-K Master-Slave Flip-Flops

December 1992

Features

- Set-Reset Capability
- High Voltage Types (20V Rating)
- CD4095BMS Non-Inverting J and K Inputs
- CD4096BMS Inverting and Non-Inverting J and K Inputs
- 16MHz Toggle Rate (Typ.) at VDD - VSS = 10V
- Gated Inputs
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Standardized Symmetrical Output Characteristics
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Registers
- Counters
- Control Circuits

Description

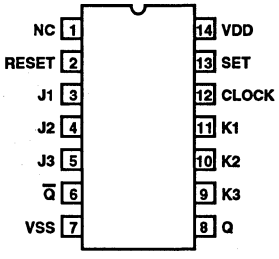
CD4095BMS and CD4096BMS are J-K Master-Slave Flip-Flops featuring separate AND gating of multiple J and K inputs. The gated J-K inputs control transfer of information into the master section during clocked operation. Information on the J-K inputs is transferred to the Q and $\overline{Q}$ outputs on the positive edge of the clock pulse. SET and RESET inputs (active high) are provided for asynchronous operation.

The CD4095BMS and CD4096BMS are supplied in these 14 lead outline packages:

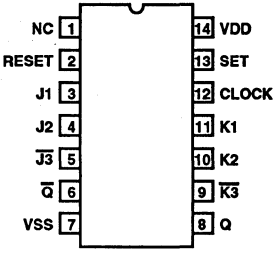
Braze Seal DIP	H4Q
Frit Seal DIP	H1A

Pinouts

CD4095BMS
TOP VIEW



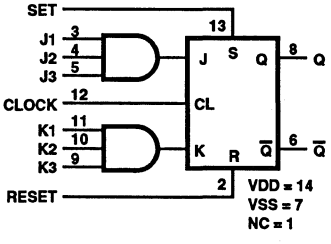
CD4096BMS
TOP VIEW



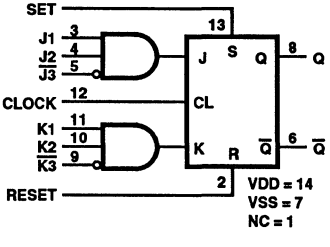
NC = NO CONNECTION

Functional Diagrams

CD4095BMS



CD4096BMS



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3331

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Output	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Propagation Delay Set or Reset to Output	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	300	ns
			10, 11	+125°C, -55°C	-	405	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	3.5	-	MHz
			10, 11	+125°C, -55°C	2.59	-	MHz

NOTES:

1. VDD = 5V, CL = 50pF, RL = 200K
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Clock to Output	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	150	ns
Propagation Delay Set or Reset to Output	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	150	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	8	-	MHz
		VDD = 15V	1, 2, 3	+25°C	12	-	MHz
Minimum Set or Reset Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Data Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	400	ns
		VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	140	ns
		VDD = 10V	1, 2, 3	+25°C	-	60	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Maximum Clock Input Rise or Fall Time	TRCL TFCL	VDD = 5V	1, 2, 3	+25°C	-	15	µs
		VDD = 10V	1, 2, 3	+25°C	-	5	µs
		VDD = 15V	1, 2, 3	+25°C	-	5	µs
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
CD4095BMS						
Static Burn-In 1 Note 1	1, 6, 8	2-5, 7, 9-13	14			
Static Burn-In 2 Note 1	1, 6, 8	7	2-5, 9-14			
Dynamic Burn-In Note 1	1	2, 7, 13	3-5, 9-11, 14	6, 8	-	12
Irradiation Note 2	1, 6, 8	7	2-5, 9-14			
CD4096BMS						
Static Burn-In 1 Note 1	1, 6, 8	2-5, 7, 9-13	14			
Static Burn-In 2 Note 1	1, 6, 8	7	2-5, 9-14			
Dynamic Burn-In Note 1	1	2, 5, 7, 9, 13	3, 4, 10, 11, 14	6, 8	12	
Irradiation Note 2	1, 6, 8	7	2-5, 9-14			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram

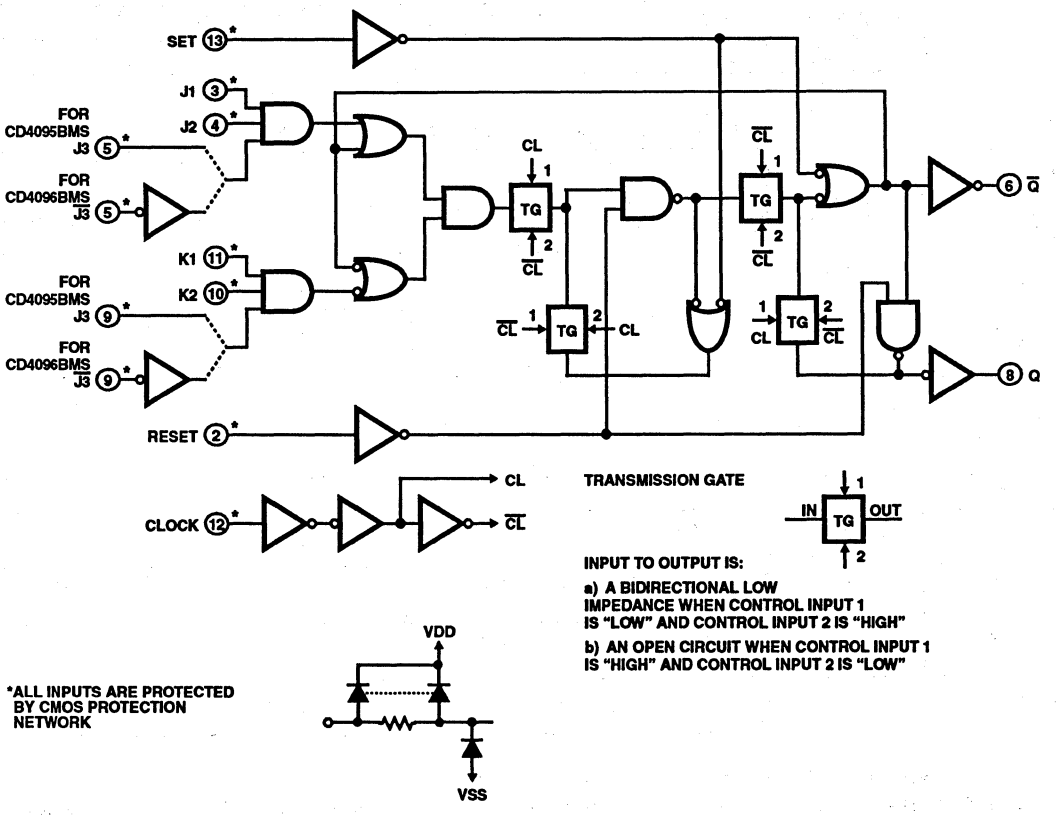


FIGURE 1. CD4095BMS AND CD4096BMS LOGIC DIAGRAM

TRUTH TABLES

SYNCHRONOUS OPERATION (S = 0, R = 0)				ASYNCHRONOUS OPERATION (J AND K = Don't Care)			
INPUTS BEFORE POSITIVE CLOCK TRANSITION		OUTPUTS AFTER POSITIVE CLOCK TRANSITION		INPUTS BEFORE POSITIVE CLOCK TRANSITION		OUTPUTS AFTER POSITIVE CLOCK TRANSITION	
J*	K*	Q	$\overline{Q}$	S	R	Q	$\overline{Q}$
0	0	No Change	No Change	0	0	No Change	No Change
0	1	0	1	0	1	0	1
1	0	1	0	1	0	1	0
1	1	Toggles	Toggles	1	1	0	0

* For CD4095BMS
J = J1 • J2 • J3
K = K1 • K2 • K3

For CD4096BMS
J = J1 • J2 • $\overline{J3}$
K = K1 • K2 • $\overline{K3}$

0 = VSS, 1 = VDD

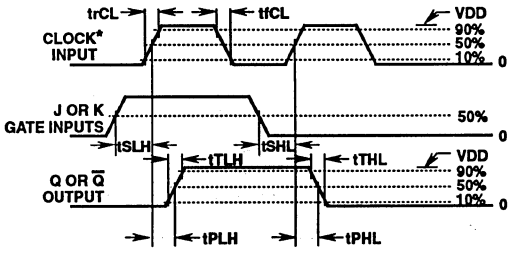


FIGURE 2. PROPAGATION DELAY, TRANSITION, AND SETUP TIME WAVEFORMS

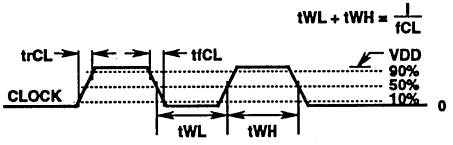


FIGURE 3. CLOCK PULSE RISE AND FALL TIME WAVEFORMS

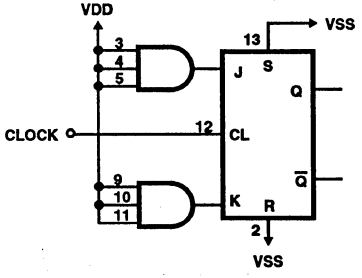


FIGURE 4. CD4095BMS CONNECTED IN TOGGLE MODE

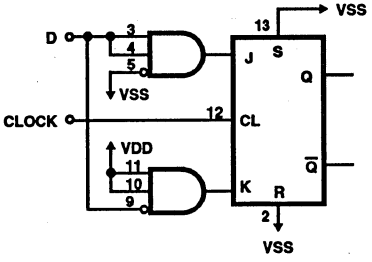
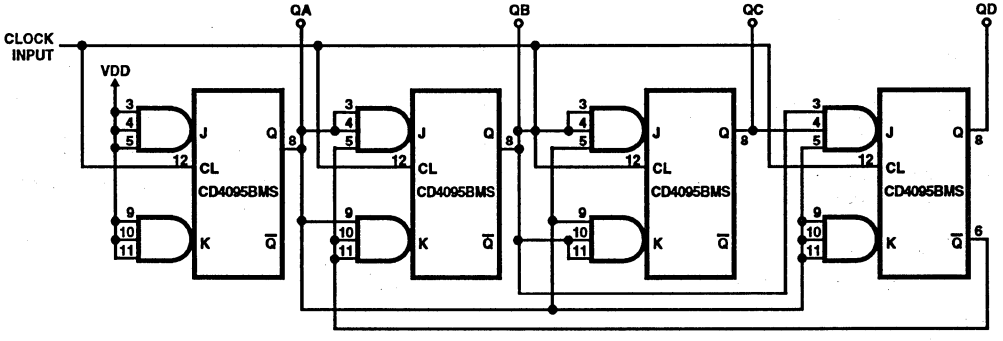
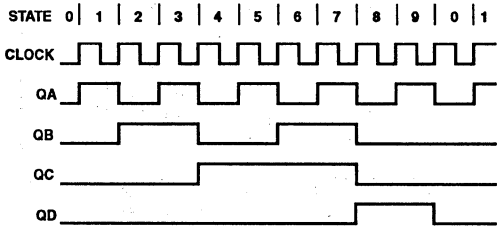


FIGURE 5. CD4096BMS CONNECTED AS A "D" TYPE FLIP-FLOP





STATE	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

NOTE:
PINS 2 & 13 RESET & SET, GO TO VSS ON ALL UNITS

FIGURE 6. SYNCHRONOUS BINARY DIVIDE-BY-TEN COUNTER

Typical Performance Characteristics

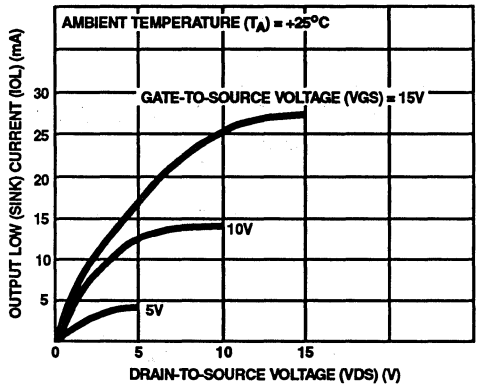


FIGURE 7. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

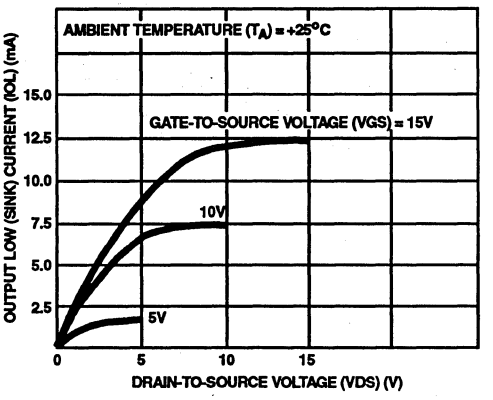


FIGURE 8. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

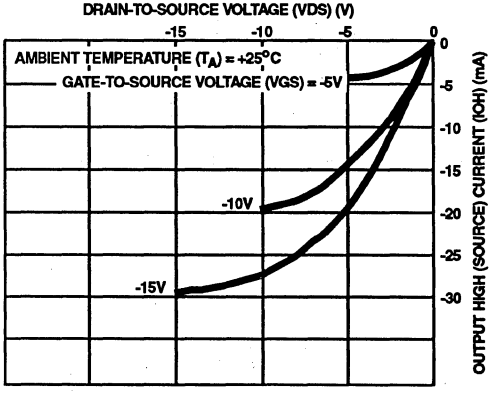


FIGURE 9. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

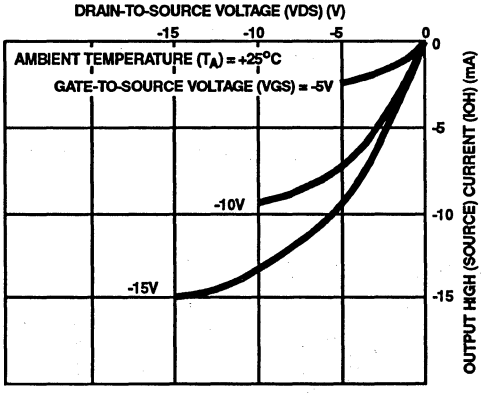


FIGURE 10. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

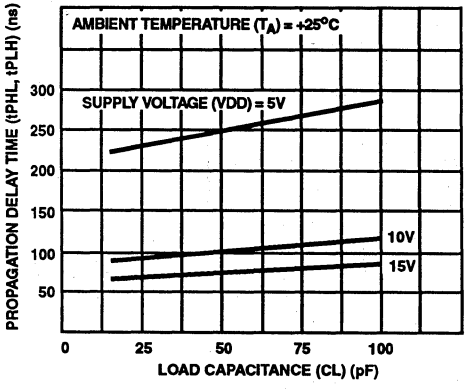


FIGURE 11. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE

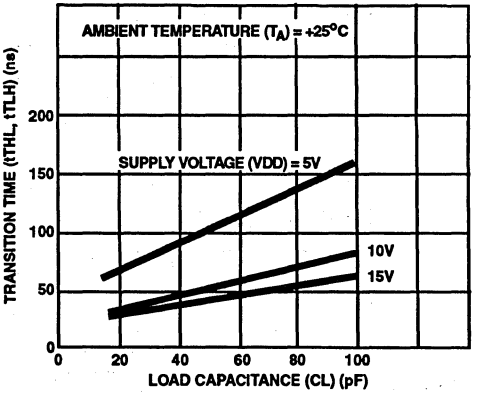


FIGURE 12. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

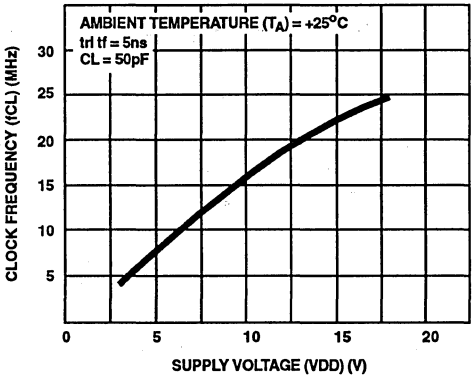


FIGURE 13. TYPICAL CLOCK FREQUENCY vs SUPPLY VOLTAGE (TOGGLE MODE - SEE FIGURE 4)

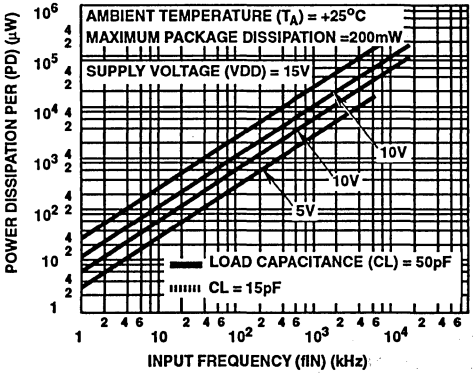
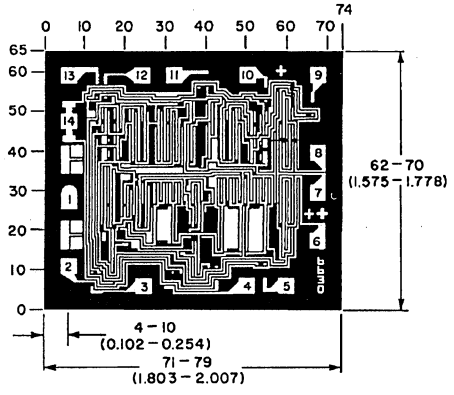
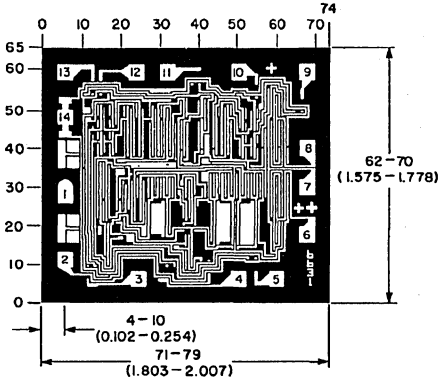


FIGURE 14. TYPICAL POWER DISSIPATION vs INPUT CLOCK FREQUENCY

Chip Dimensions and Pad Layouts



CD4095BHMS



CD4096BHMS

Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4098BMS

CMOS Dual Monostable Multivibrator

December 1992

Features

- High Voltage Type (20V Rating)
- Retriggerable/Resettable Capability
- Trigger and Reset Propagation Delays Independent of RX, CX
- Triggering from Leading or Trailing Edge
- Q and $\overline{Q}$ Buffered Outputs Available
- Separate Resets
- Wide Range of Output Pulse Widths
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Standardized Symmetrical Output Characteristics
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

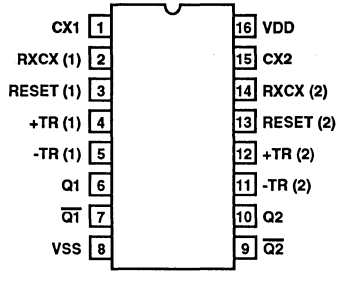
Applications

- Pulse Delay and Timing
- Pulse Shaping

Astable Multivibrator

Pinout

CD4098BMS
TOP VIEW



TERMINALS 1, 8, 15 ARE ELECTRICALLY CONNECTED INTERNALLY

Description

CD4098BMS dual monostable multivibrator provides stable retriggerable/resettable one shot operation for any fixed voltage timing application.

An external resistor (RX) and an external capacitor (CX) control the timing for the circuit. Adjustment of RX and CX provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of RX and CX.

Leading edge triggering (+TR) and trailing edge triggering (-TR) inputs are provided for triggering from either edge of an input pulse. An unused +TR input should be tied to VSS. An unused -TR input should be tied to VDD. A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to VDD. However, if an entire section of the CD4098BMS is not used, its RESET should be tied to VSS. See Table 9.

In normal operation the circuit triggers (extends the output pulse one period) on the application of each new trigger pulse. For operation in the non-retriggerable mode, $\overline{Q}$ is connected to -TR when leading edge triggering (+TR) is used or Q is connected to +TR when trailing edge triggering (-TR) is used.

The time period (T) for this multivibrator can be approximated by: TX = $^1/_2$RXCX for CX 3 0.01μF. Time periods as a function of RX for values of CX and VDD are given in Figure 8. Values of T vary from unit to unit and as a function of voltage, temperature, and RXCX.

The minimum value of external resistance, RX, is 5kΩ. The maximum value of external capacitance, CX, is 100μF. Figure 9 shows time periods as a function of CX for values of RX and VDD.

The output pulse width has variations of ±2.5% typically, over the temperature range of -55°C to +125°C for CX = 1000pF and RX = 100kΩ.

For power supply variations of ±5%, the output pulse width has variations of ±0.5% typically, for VDD = 10V and 15V and ±1% typically, for VDD = 5V at CX = 1000pF and RX = 5kΩ.

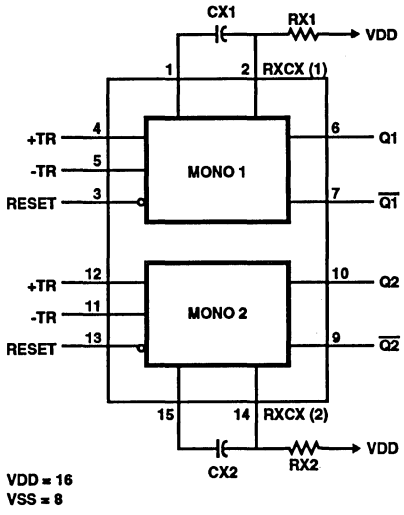
The CD4098BMS is supplied in these 16-lead outline packages:

Braze Seal DIP	H4T
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3332

Functional Diagram



Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20V	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20V	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay +TR, -TR to Q, $\overline{Q}$	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND RX = 5K to 10KΩ, CX ≥ 15pF	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Transition Time	TTHL1	VDD = 5V, VIN = VDD or GND RX = 5K to 10KΩ, CX = 15pF to 10,000pF	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Transition Time (Note 2)	TTLH1	VDD = 5V, VIN = VDD or GND RX = 5K to 10KΩ, CX ≥ 15pF	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay +TR, -TR to Q, $\overline{Q}$ CX ≥ 15pF	TPHL1 TPLH1	VDD = 10V	1, 2, 3, 4	+25°C	-	250	ns
		VDD = 15V	1, 2, 3, 4	+25°C	-	200	ns
Propagation Delay Reset CX ≥ 15pF	TPHL2 TPLH2	VDD = 5V	1, 2, 3	+25°C	-	450	ns
		VDD = 10V	1, 2, 3, 4	+25°C	-	250	ns
		VDD = 15V	1, 2, 3,4	+25°C	-	150	ns
Transition Time CX = 15pF to 10,000pF	TTHL1	VDD = 10V	1, 2, 3, 4	+25°C	-	100	ns
		VDD = 15V	1, 2, 3, 4	+25°C	-	80	ns
Transition Time CX = 0.01µF to 0.1µF	TTLH2 TTHL2	VDD = 5V	1, 2, 3	+25°C	-	300	ns
		VDD = 10V	1, 2, 3, 5	+25°C	-	150	ns
		VDD = 15V	1, 2, 3, 5	+25°C	-	130	ns
Transition Time CX = 0.1µF to 1µF	TTHL3	VDD = 5V	1, 2, 3	+25°C	-	500	ns
		VDD = 10V	1, 2, 3, 4	+25°C	-	300	ns
		VDD = 15V	1, 2, 3, 4	+25°C	-	160	ns
Transition Time CX ≥ 15pF	TTLH1	VDD = 10V	1, 2, 3, 4	+25°C	-	100	ns
		VDD = 15V	1, 2, 3, 4	+25°C	-	80	ns
Minimum Reset Pulse Width, CX = 15pF	TW	VDD = 5V	1, 2, 3, 5	+25°C	-	200	ns
		VDD = 10V	1, 2, 3, 5	+25°C	-	80	ns
		VDD = 15V	1, 2, 3, 5	+25°C	-	60	ns
Minimum Reset Pulse Width, CX = 1000pF	TW	VDD = 5V	1, 2, 3, 5	+25°C	-	1200	ns
		VDD = 10V	1, 2, 3, 5	+25°C	-	600	ns
		VDD = 15V	1, 2, 3,5	+25°C	-	500	ns
Minimum Reset Pulse Width, CX = 0.1µF	TW	VDD = 5V	1, 2, 3, 5	+25°C	-	50	µs
		VDD = 10V	1, 2, 3, 5	+25°C	-	30	µs
		VDD = 15V	1, 2, 3, 5	+25°C	-	20	µs
Pulse Width Match Between Circuits in Same Package	TW	VDD = 5V	1, 2, 3, 6	+25°C	-	10	%
		VDD = 10V	1, 2, 3, 6	+25°C	-	15	%
		VDD = 15V	1, 2, 3, 6	+25°C	-	15	%
Trigger Rise or Fall Time	TRTR TFTR	VDD = 5V to 15V	1, 2	+25°C	-	100	µs
Input Capacitance	CIN	Any Inputs	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, inputs tR, tF < 20ns.
4. RX = 5K to 10MΩ.
5. RX = 100kΩ
6. RX = 10kΩ

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST PRE-IRRAD	TEST POST-IRRAD	READ AND RECORD PRE-IRRAD	READ AND RECORD POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	6, 7, 9, 10	1-5, 8, 11-15	16			
Static Burn-In 2 Note 1	6, 7, 9, 10	1, 8, 15	2-5, 11-14, 16			
Dynamic Burn-In Note 1	-	1, 4, 8, 12, 15	2, 14, 16	6, 7, 9, 10	5, 11	3, 13
Irradiation Note 2	2, 6, 7, 9, 10, 14	1, 8, 15	3-5, 11-13, 16			

NOTE:

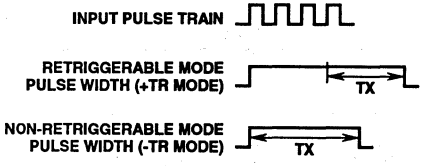
1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

TABLE 9. FUNCTIONAL TERMINAL CONNECTIONS

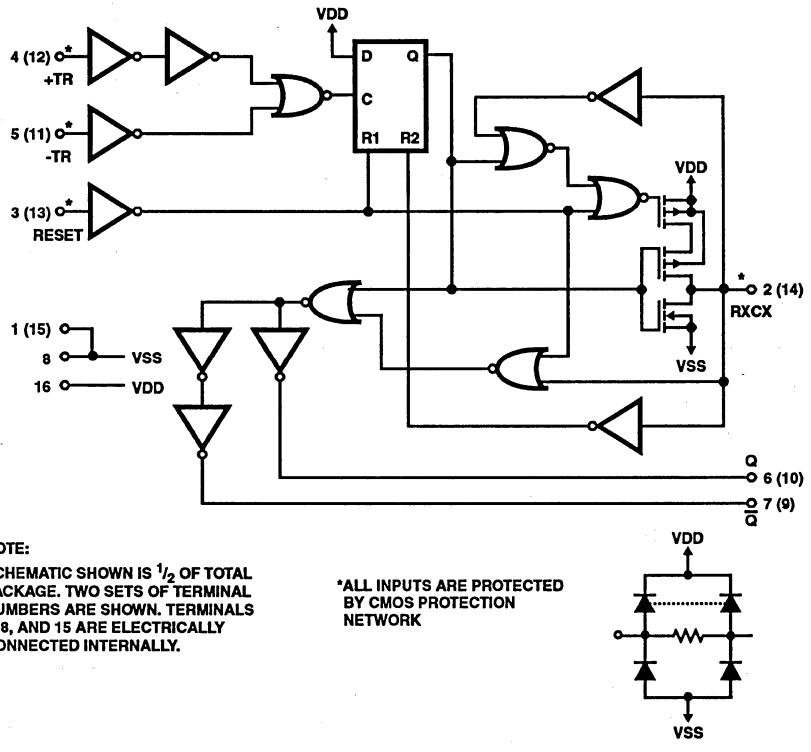
FUNCTION	VDD TO TERM. NO.		VSS TO TERM. NO.		INPUT PULSE TO TERM. NO.		OTHER CONNECTIONS	
	MONO 1	MONO 2	MONO 1	MONO 2	MONO 1	MONO 2	MONO 1	MONO 2
Leading Edge Trigger/ Retriggerable	3, 5	11, 13			4	12		
Leading Edge Trigger/ Non-Retriggerable	3	13			4	12	5-7	11-9
Trailing Edge Trigger/ Retriggerable	3	13	4	12	5	11		
Trailing Edge Trigger/ Non-Retriggerable	3	13			5	11	4-6	12-10
Unused Section	5	11	3, 4	12, 13				

NOTES:

1. A retriggerable one-shot multivibrator has an output pulse width which is extended one full time period (TX) after application of the last trigger pulse. The minimum time between retriggering edges (or trigger and retrigger edges) is 40% of (TX).
2. A non-retriggerable one-shot multivibrator has a time period TX referenced from the application of the first trigger pulse.



Logic Diagram



NOTE:

SCHEMATIC SHOWN IS $^1/_2$ OF TOTAL PACKAGE. TWO SETS OF TERMINAL NUMBERS ARE SHOWN. TERMINALS 1, 8, AND 15 ARE ELECTRICALLY CONNECTED INTERNALLY.

*ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

FIGURE 1. LOGIC DIAGRAM

Typical Performance Characteristics

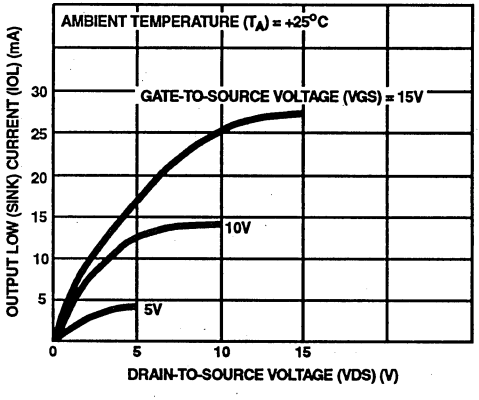


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

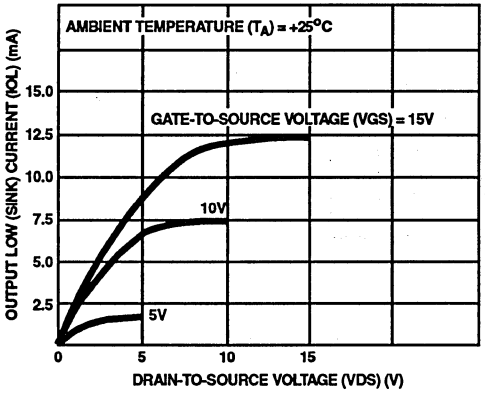


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

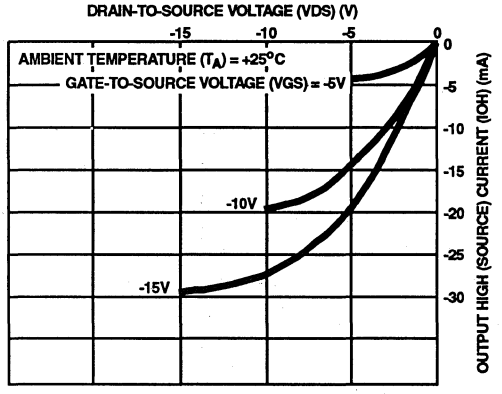


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

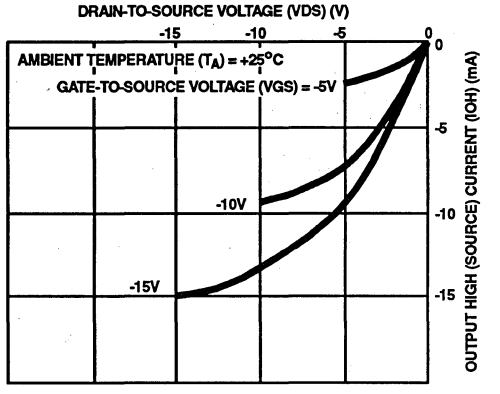


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

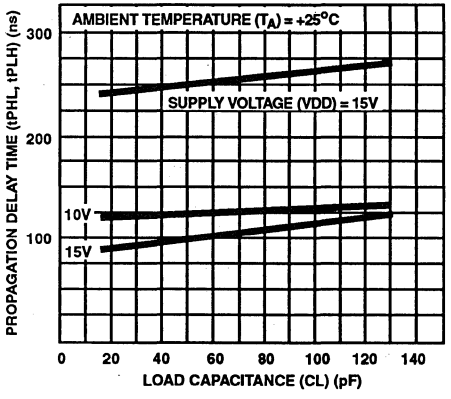


FIGURE 6. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE, TRIGGER INTO Q OUT (ALL VALUES OF CX AND RX).

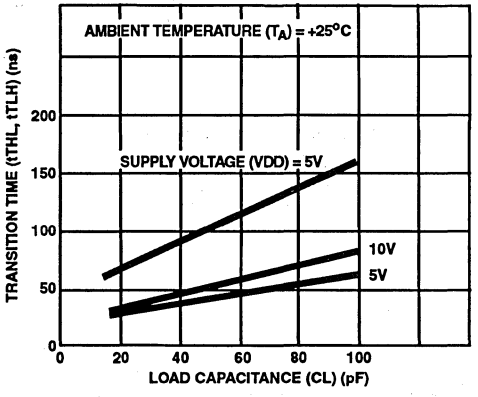


FIGURE 7. TRANSITION TIME vs LOAD CAPACITANCE FOR RX = 5kΩ-10000kΩ AND CX = 15pF-10000pF

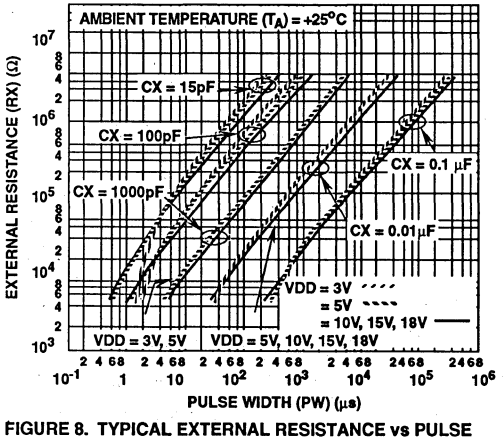


FIGURE 8. TYPICAL EXTERNAL RESISTANCE vs PULSE WIDTH

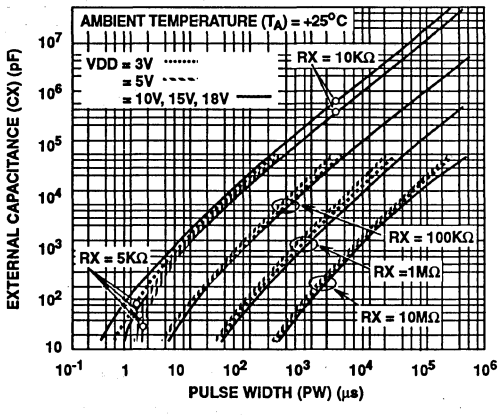


FIGURE 9. TYPICAL EXTERNAL CAPACITANCE vs PULSE WIDTH

Typical Performance Characteristics (Continued)

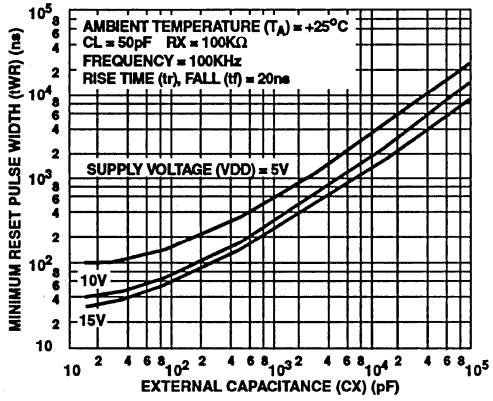
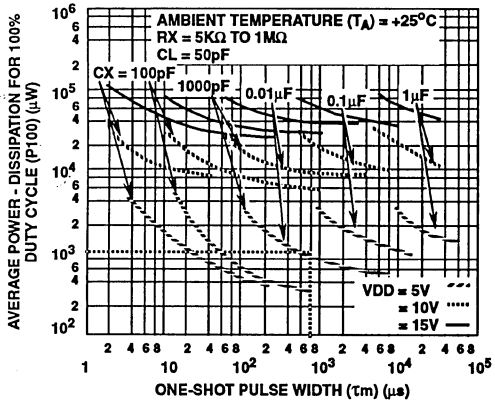


FIGURE 10. TYPICAL MINIMUM RESET PULSE WIDTH vs EXTERNAL CAPACITANCE



To calculate average power dissipation(P) for less than 100% duty cycle:

P100 = average power for 100% duty cycle:

$P = \left(\frac{tm}{\tau T}\right) P100$ where τm = one shot pulse width

τT = trigger pulse period

e.g. For τm = 600μs, tT = 1000μs. CX = 0.01mF

VDD = 5V

$P1 = \left(\frac{600}{1000}\right) 10^3\ \mu W = 600\mu W$ (see dotted line on graph)

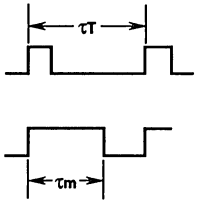


FIGURE 11. AVERAGE POWER DISSIPATION vs ONE-SHOT PULSE WIDTH

Applications

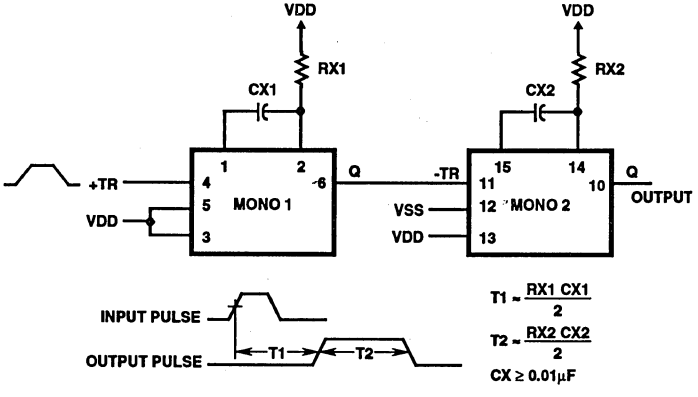
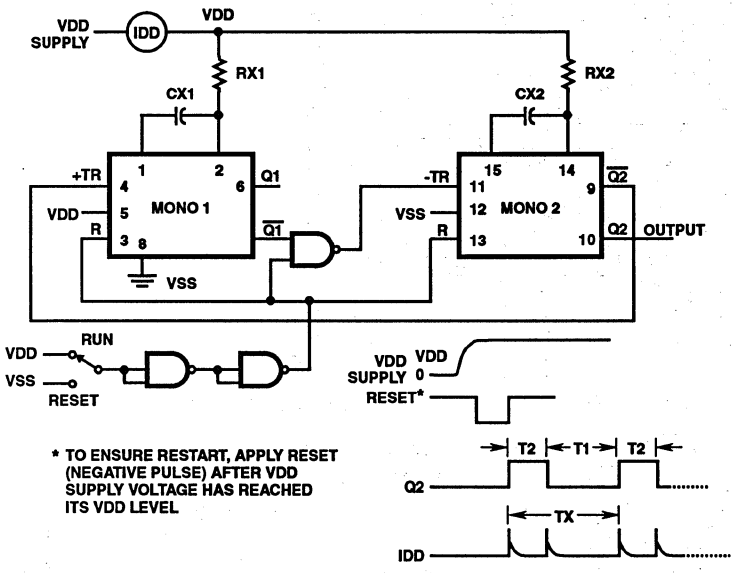


FIGURE 12. PULSE DELAY

Applications (Continued)



* TO ENSURE RESTART, APPLY RESET (NEGATIVE PULSE) AFTER VDD SUPPLY VOLTAGE HAS REACHED ITS VDD LEVEL

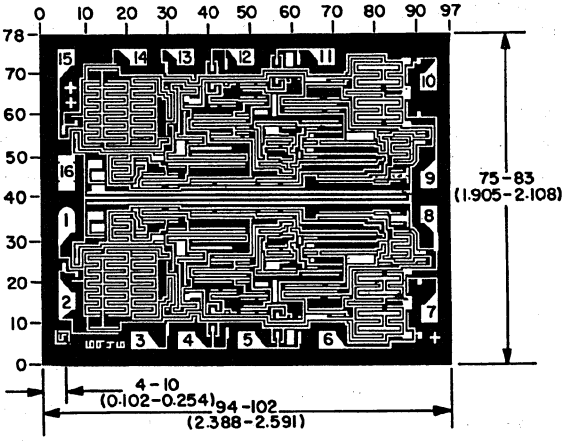
IDD, TX vs RX

RX	IDD (AVG.)	TX (T1 + T2)	VDD
10kΩ ↓ 10MΩ	1mA ↓ 0.05mA	3.8µs ↓ 0.5s	5V
	2.5mA ↓ 0.5mA	3.2µs ↓ 0.5s	10V
	5mA ↓ 1mA	3µs ↓ 0.5s	10V

NOTES:
1. All values are typical.
2. CX range: 0.0001µF to 0.1µF

FIGURE 13. ASTABLE MULTIVIBRATOR WITH RESTART AFTER RESET CAPABILITY

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4099BMS

December 1992

CMOS 8-Bit Addressable Latch

Features

- High Voltage Type (20V Rating)
- Serial Data Input
- Active Parallel Output
- Storage Register Capability
- Master Clear
- Can Function as Demultiplexer
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Standardized Symmetrical Output Characteristics
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Multi-Line Decoders
- A/D Converters

Description

CD4099BMS 8-bit addressable latch is a serial input, parallel output storage register that can perform a variety of functions.

Data are inputted to a particular bit in the latch when that bit is addressed (by means of inputs A0, A1, A2) and when WRITE DISABLE is at a low level. When WRITE DISABLE is high, data entry is inhibited; however, all 8 outputs can be continuously read independent of WRITE DISABLE and address inputs.

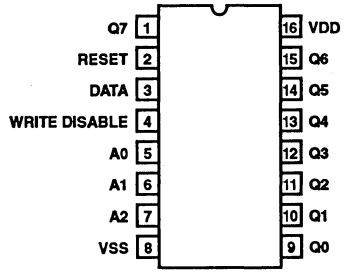
A master RESET input is available, which resets all bits to a logic "0" level when RESET and WRITE DISABLE are at a high level. When RESET is at a high level, and WRITE DISABLE is at a low level, the latch acts as a 1 of 8 demultiplexer; the bit that is addressed has an active output which follows the data input, while all unaddressed bits are held to a logic "0" level.

The CD4099BMS is supplied in these 16-lead outline packages:

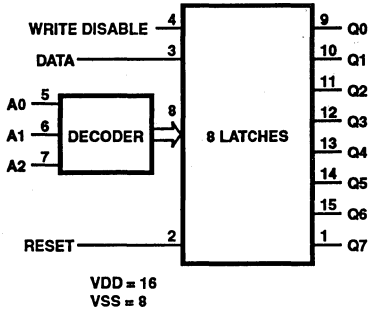
Braze Seal DIP	H4X
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

Pinout

CD4099BMS
TOP VIEW



Functional Diagram



7 LOGIC

File Number 3333

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance ..... θ_{ja} θ_{jc}
Ceramic DIP and FRIT Package ..... 80°C/W 20°C/W
Flatpack Package ..... 70°C/W 20°C/W
Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Data to Output	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay Write Disable to Output	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay Reset to Output	TPHL3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	350	ns
			10, 11	+125°C, -55°C	-	473	ns
Propagation Delay Address to Output	TPHL4 TPLH4	VDD = 5V, VIN = VDD or GND	9	+25°C	-	450	ns
			10, 11	+125°C, -55°C	-	608	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Data to Output	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	150	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Propagation Delay Write Disable to Output	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Propagation Delay Reset to Output	TPHL3	VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Propagation Delay Address to Output	TPHL4 TPLH4	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	150	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Minimum Hold time Data to Write Disable	TH	VDD = 5V	1, 2, 3	+25°C	-	150	MHz
		VDD = 10V	1, 2, 3	+25°C	-	75	MHz
		VDD = 15V	1, 2, 3	+25°C	-	50	MHz
Minimum Data Setup Time Data to Write Disable	TS	VDD = 5V	1, 2, 3	+25°C	-	100	ns
		VDD = 10V	1, 2, 3	+25°C	-	50	ns
		VDD = 15V	1, 2, 3	+25°C	-	35	ns
Minimum Pulse Width Data	TW	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Minimum Pulse Width Address	TW	VDD = 5V	1, 2, 3	+25°C	-	400	ns
		VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	125	ns
Minimum Pulse Width Reset	TW	VDD = 5V	1, 2, 3	+25°C	-	150	ns
		VDD = 10V	1, 2, 3	+25°C	-	75	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Input Capacitance	CIN	Any inputs	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	1, 9-15	2-8	16			
Static Burn-In 2 Note 1	1, 9-15	8	2-7, 16			
Dynamic Burn-In Note 1	-	5-8	16	1, 9-15	2, 4	3
Irradiation Note 2	1, 9-15	8	2-7, 16			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram

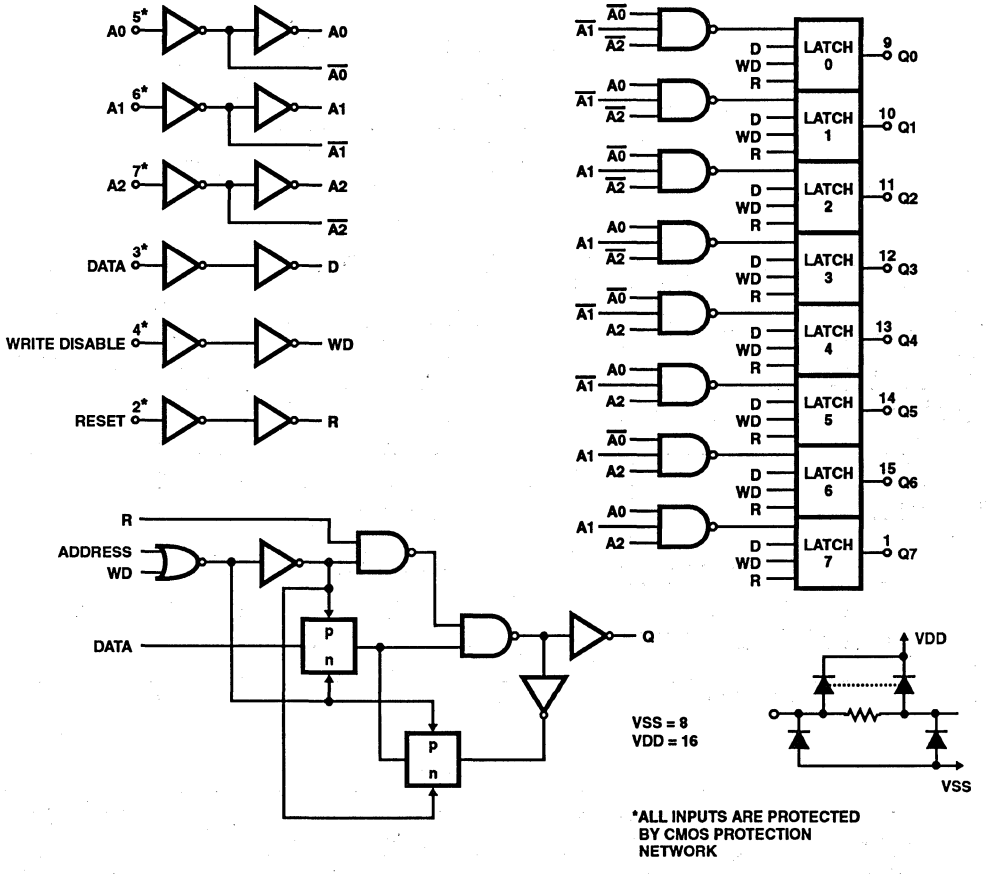
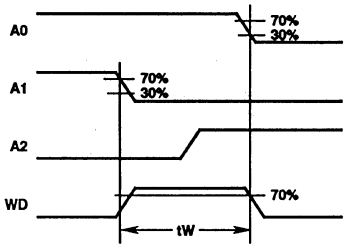


FIGURE 1. LOGIC DIAGRAM OF CD4099BMS AND DETAIL OF 1 OF 8 LATCHES



MODE SELECTION			
WD	R	ADDRESSED LATCH	UNADDRESSED LATCH
0	0	Follows Data	Holds Previous State
0	1	Follows Data (Active High 8-Channel Demultiplexer)	Reset to "0"
1	0	Holds Previous State	
1	1	Reset to "0"	Reset to "0"

WD = Write Disable R = Reset

FIGURE 2. DEFINITION OF WRITE DISABLE ON TIME

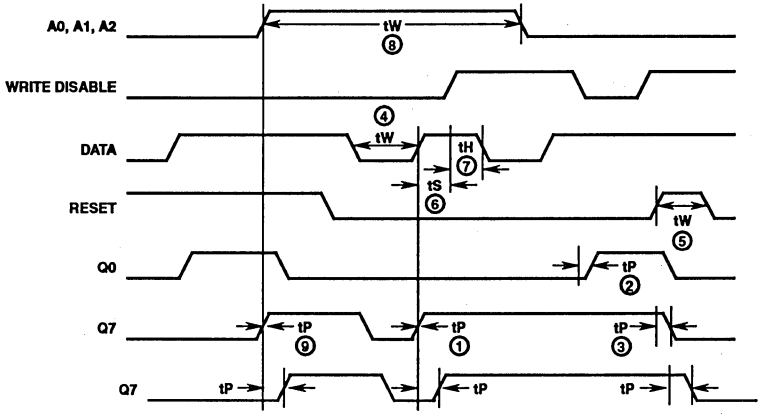


FIGURE 3. MASTER TIMING DIAGRAM

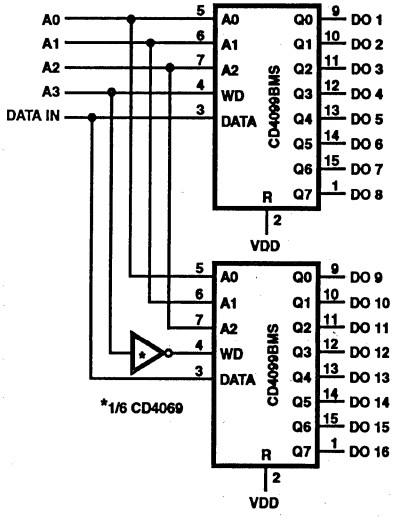


FIGURE 4. 1 OF 16 DECODER/DEMULTIPLEXER

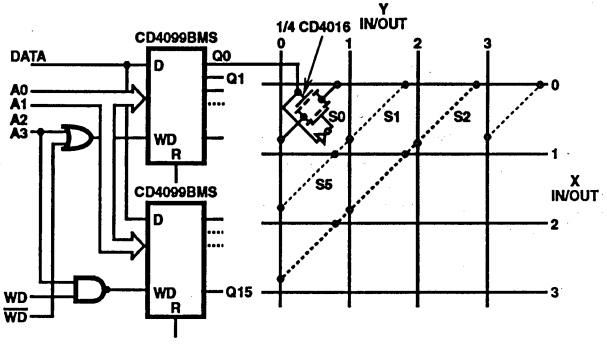


FIGURE 5. MULTIPLE SELECTION DECODING - 4 x 4 CROSSPOINT SWITCH

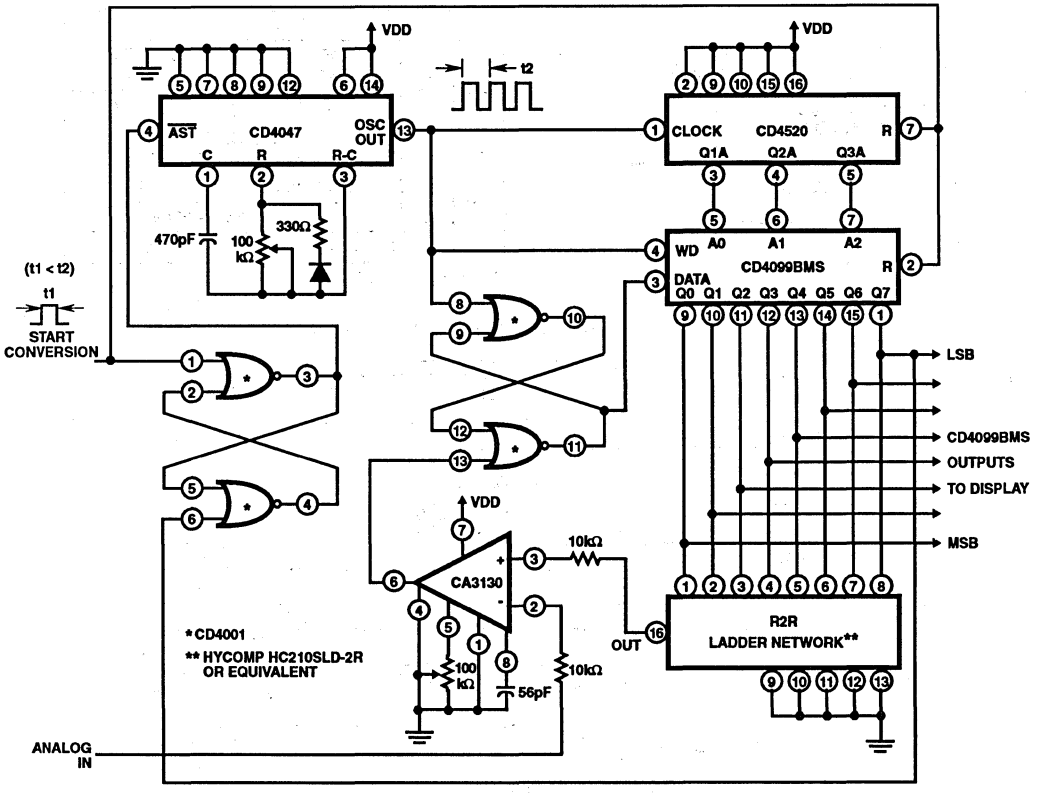


FIGURE 6. A/D CONVERTER

Typical Performance Characteristics

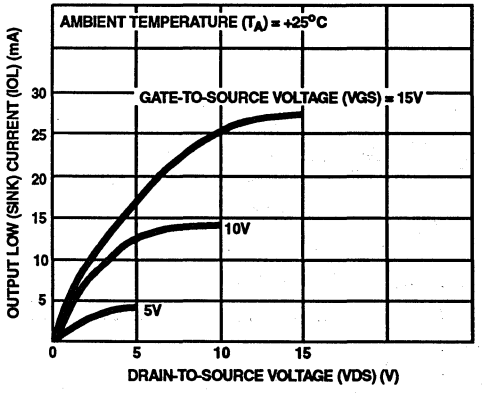


FIGURE 7. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

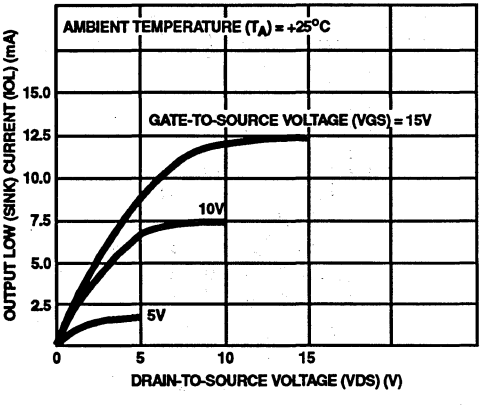


FIGURE 8. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

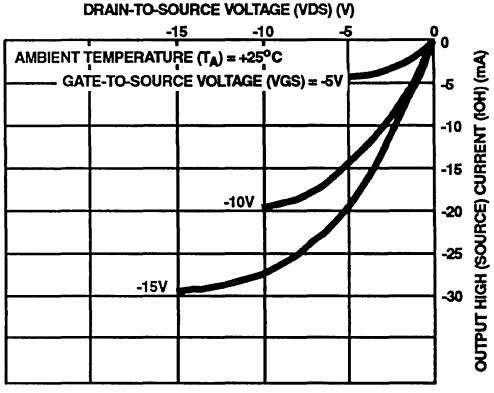


FIGURE 9. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

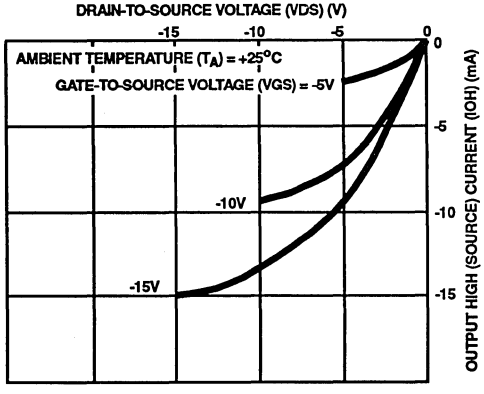


FIGURE 10. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

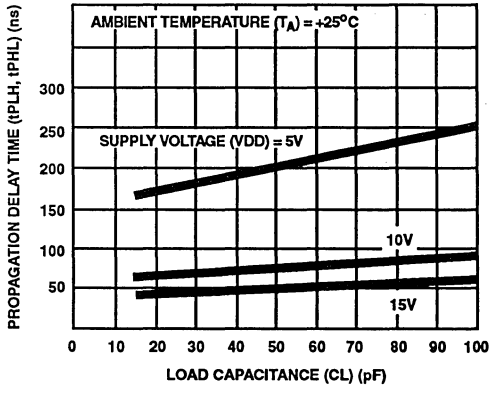


FIGURE 11. TYPICAL PROPAGATION DELAY TIME (DATA TO Qn) vs LOAD CAPACITANCE

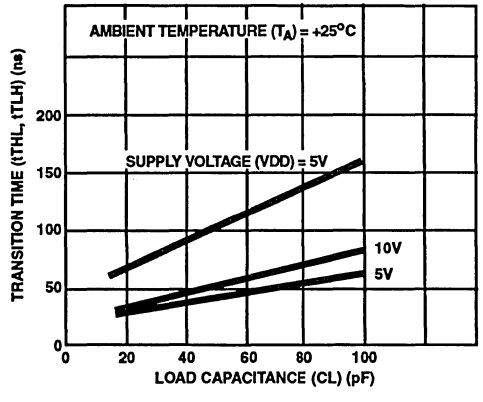


FIGURE 12. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

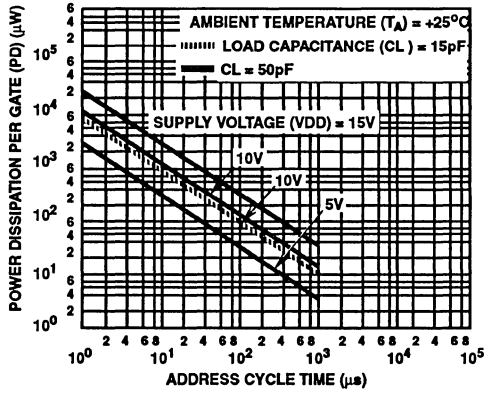
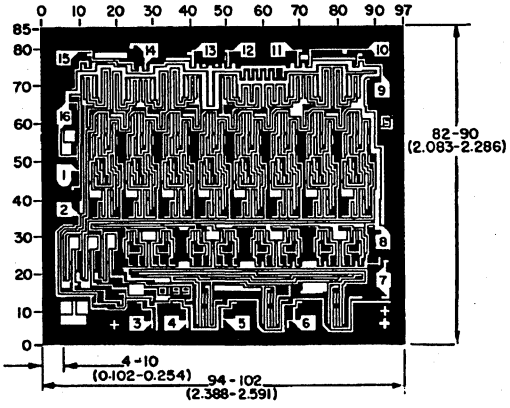


FIGURE 13. TYPICAL DYNAMIC POWER DISSIPATION vs ADDRESS CYCLE TIME

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4502BMS

December 1992

CMOS Strobed Hex Inverter/Buffer

Features

- High Voltage Type (20V Rating)
- 2 TTL Load Output Drive Capability
- 3 State Outputs
- Common Output Disable Control
- Inhibit Control
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- 3 State Hex Inverter for Interfacing ICs with Data Buses
- COS/MOS to TTL Hex Buffer

Description

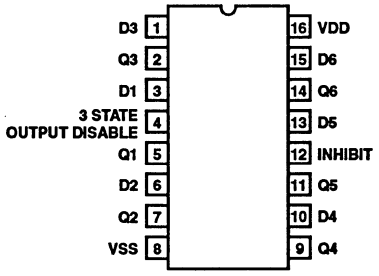
CD4502BMS consists of six inverter/buffers with 3 state outputs. A logic "1" on the OUTPUT DISABLE input produces a high impedance state in all six outputs. This feature permits common busing of the outputs, thus simplifying system design. A Logic "1" on the INHIBIT input switches all six outputs to logic "0" if the OUTPUT DISABLE input is a logic "0". This device is capable of driving two standard TTL loads, which is equivalent to six times the JEDEC "B" series IOL standard.

The CD4502BMS is supplied in these 16-lead outline packages:

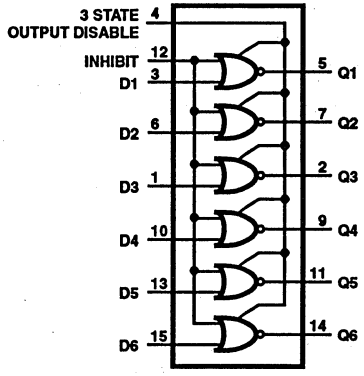
Braze Seal DIP	H4T
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

Pinout

CD4502BMS
TOP VIEW



Functional Diagram



VDD = 16
VSS = 8

7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3334

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	3.06	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	7.8	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	20.4	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL5	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH5	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL15	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH15	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.4	-	µA
				2	+125°C	-12	-	µA
			VDD = 18V	3	-55°C	-0.4	-	µA
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.4	µA
				2	+125°C	-	12	µA
			VDD = 18V	3	-55°C	-	0.4	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Data or Inhibit to Output	TPHL1	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	270	ns
			10, 11	+125°C, -55°C	-	365	ns
Propagation Delay Data or Inhibit to Output	TPLH1	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	380	ns
			10, 11	+125°C, -55°C	-	513	ns
Propagation Delay Inhibit to Output	TPHL2	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	270	ns
			10, 11	+125°C, -55°C	-	365	ns
Propagation Delay Inhibit to Output	TPLH2	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	380	ns
			10, 11	+125°C, -55°C	-	513	ns
Propagation Delay Disable to Output	TPHZ	VDD = 5V, VIN = VDD or GND (Note 2, 3)	9	+25°C	-	120	ns
			10, 11	+125°C, -55°C	-	162	ns
Propagation Delay Disable to Output	TPZH	VDD = 5V, VIN = VDD or GND (Note 2, 3)	9	+25°C	-	220	ns
			10, 11	+125°C, -55°C	-	297	ns
Propagation Delay Disable to Output	TPLZ	VDD = 5V, VIN = VDD or GND (Note 2, 3)	9	+25°C	-	250	ns
			10, 11	+125°C, -55°C	-	338	ns
Propagation Delay Disable to Output	TPZL	VDD = 5V, VIN = VDD or GND (Note 2, 3)	9	+25°C	-	250	ns
			10, 11	+125°C, -55°C	-	338	ns
Transition Time	TTHL	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	120	ns
			10, 11	+125°C, -55°C	-	162	ns
Transition Time	TTLH	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.
3. VDD = 5V, CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	2.16	-	mA
				-55°C	3.84	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2, 4	+125°C	5.4	-	mA
				-55°C	9.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2, 4	+125°C	14.4	-	mA
				-55°C	25.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Data to Output	TPHL1	VDD = 10V	1, 2, 3	+25°C	-	120	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Propagation Delay Data to Output	TPLH1	VDD = 10V	1, 2, 3	+25°C	-	180	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Propagation Delay Inhibit to Output	TPHL2	VDD = 10V	1, 2, 3	+25°C	-	120	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Propagation Delay Inhibit to Output	TPLH2	VDD = 10V	1, 2, 3	+25°C	-	180	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Propagation Delay Disable to Output	TPHZ	VDD = 10V	1, 2, 4	+25°C	-	80	ns
		VDD = 15V	1, 2, 4	+25°C	-	60	ns
Propagation Delay Disable to Output	TPZH	VDD = 10V	1, 2, 4	+25°C	-	100	ns
		VDD = 15V	1, 2, 4	+25°C	-	80	ns
Propagation Delay Disable to Output	TPLZ	VDD = 10V	1, 2, 4	+25°C	-	130	ns
		VDD = 15V	1, 2, 4	+25°C	-	110	ns
Propagation Delay Disable to Output	TPZL	VDD = 10V	1, 2, 4	+25°C	-	110	ns
		VDD = 15V	1, 2, 4	+25°C	-	80	ns
Transition Time	TTHL	VDD = 10V	1, 2, 3	+25°C	-	60	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Transition Time	TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	Any Inputs	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

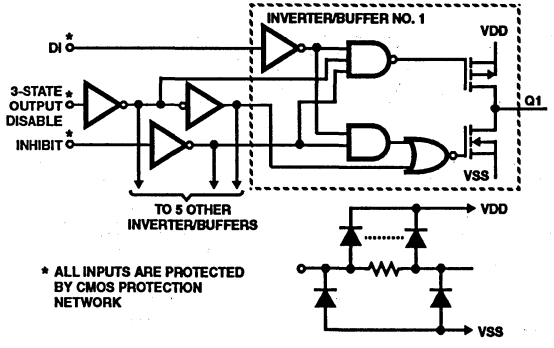
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	2, 5, 7, 9, 11, 14	1, 3, 4, 6, 8, 10, 12, 13, 15	16			
Static Burn-In 2 Note 1	2, 5, 7, 9, 11, 14	8	1, 3, 4, 6, 10, 12, 13, 15, 16			
Dynamic Burn-In Note 1	-	8	16	2, 5, 7, 9, 11, 14	4	1, 3, 6, 10, 12, 13, 15
Irradiation Note 2	2, 5, 7, 9, 11, 14	8	1, 3, 4, 6, 10, 12, 13, 15, 16			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram



TRUTH TABLE

DISABLE	INHIBIT	Dn	Qn
0	0	0	1
0	0	1	0
0	1	X	0
1	X	X	Z

Logic 0 = Low

Logic 1 = High

Z = High Impedance

X = Don't Care

FIGURE 1. LOGIC DIAGRAM OF 1 OF 6 IDENTICAL INVERTER/BUFFERS

Typical Performance Characteristics

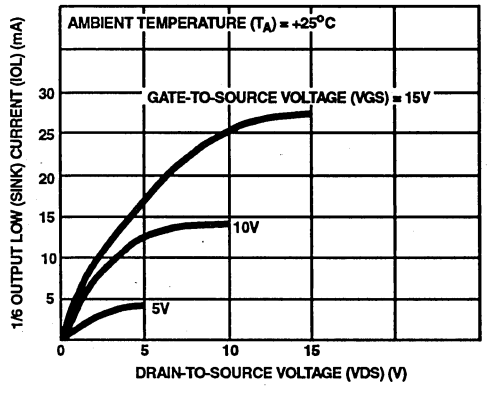


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

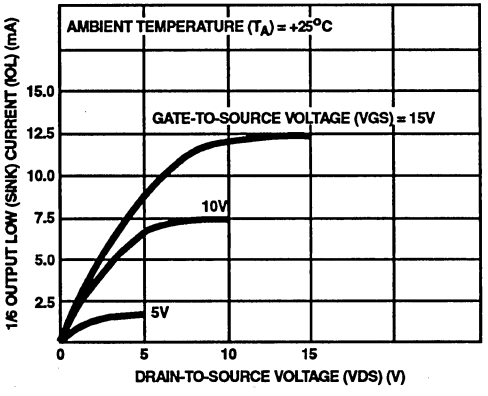


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

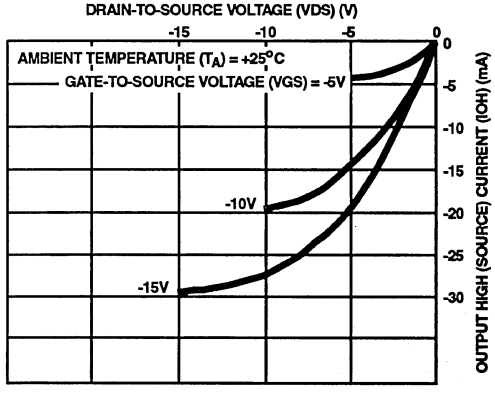


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

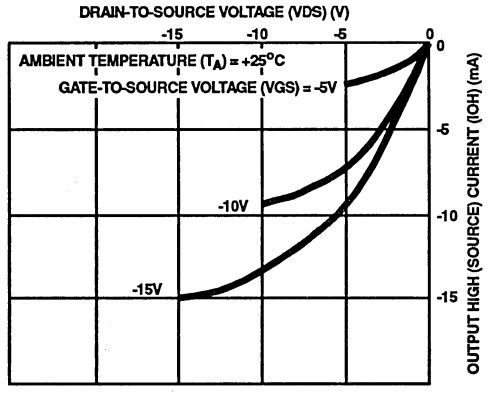


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

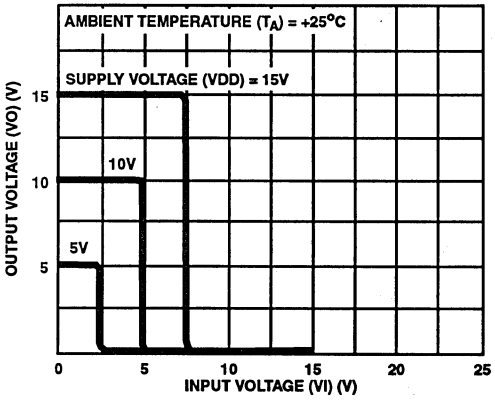


FIGURE 7. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS

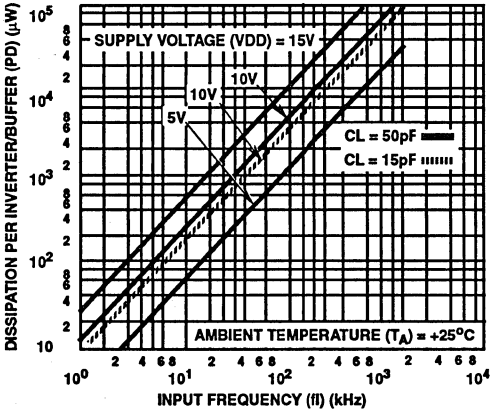


FIGURE 8. TYPICAL POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

Typical Performance Characteristics (Continued)

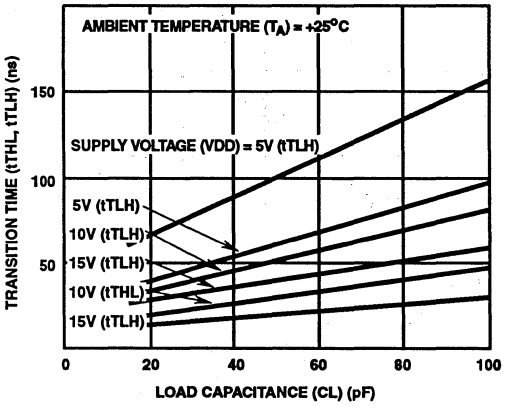


FIGURE 9. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

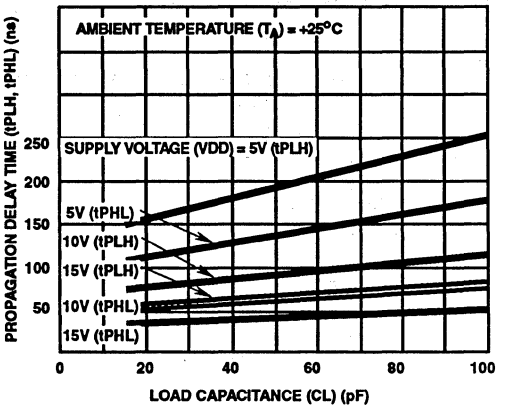
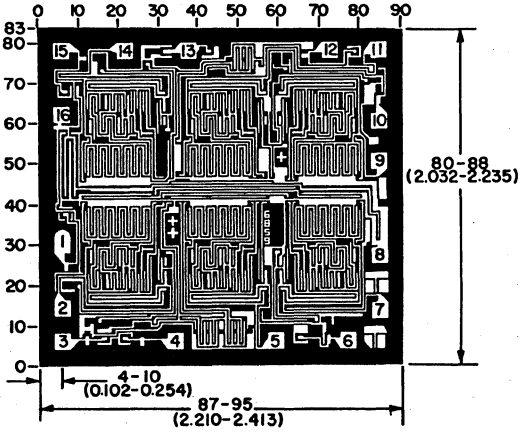


FIGURE 10. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4503BMS

CMOS Hex Buffer

December 1992

Features

- High Voltage Type (20V Rating)
- 3 State Non-Inverting Type
- 1 TTL Load Output Drive Capability
- 2 Output Disable Controls
- 3 State Outputs
- Pin Compatible with Industry Types MM80C97, MC14503, and 340097
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- 3 State Hex Buffer for Interfacing ICs with Data Buses
- COS/MOS to TTL Hex Buffer

Description

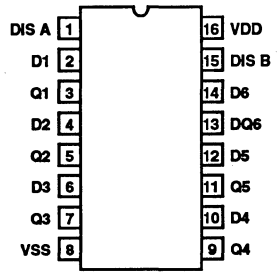
CD4503BMS is a hex noninverting buffer with 3 state outputs having high sink and source current capability. Two disable controls are provided, one of which controls four buffers and the other controls the remaining two buffers.

The CD4503BMS is supplied in these 16-lead outline packages:

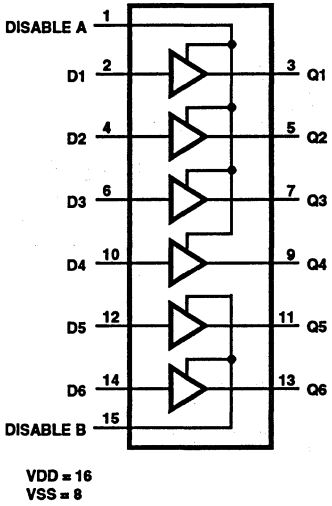
Braze Seal DIP	H4T
Frit Seal DIP	H1E
Ceramic Flatpack	H6W

Pinout

CD4503BMS
TOP VIEW



Functional Diagram



7 LOGIC

File Number 3335

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K)..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	2.1	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	5.5	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	16.1	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-1.02	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-4.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-2.6	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-6.8	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH> VDD/2	VOL< VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.4	-	µA
				2	+125°C	-12	-	µA
			VDD = 18V	3	-55°C	-0.4	-	µA
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.4	µA
				2	+125°C	-	12	µA
			VDD = 18V	3	-55°C	-	0.4	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	110	ns
			10, 11	+125°C, -55°C	-	149	ns
Propagation Delay	TPLH	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	150	ns
			10, 11	+125°C, -55°C	-	203	ns
Propagation Delay3 State	TPHZ TPZH	VDD = 5V, VIN = VDD or GND (Note 2, 3)	9	+25°C	-	140	ns
			10, 11	+125°C, -55°C	-	189	ns
Propagation Delay3 State	TPZL TPLZ	VDD = 5V, VIN = VDD or GND (Note 2, 3)	9	+25°C	-	180	ns
			10, 11	+125°C, -55°C	-	243	ns
Transition Time	TTHL	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	70	ns
			10, 11	+125°C, -55°C	-	95	ns
Transition Time	TTLH	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	90	ns
			10, 11	+125°C, -55°C	-	122	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.
3. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	1.3	-	mA
				-55°C	2.6	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	3.8	-	mA
				-55°C	6.5	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	11.2	-	mA
				-55°C	19.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.7	mA
				-55°C	-	-1.2	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-3.0	mA
				-55°C	-	-5.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-1.8	mA
				-55°C	-	-3.1	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-4.8	mA
				-55°C	-	-8.2	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay	TPHL	VDD = 10V	1, 2, 3	+25°C	-	50	ns
		VDD = 15V	1, 2, 3	+25°C	-	35	ns
Propagation Delay	TPLH	VDD = 10V	1, 2, 3	+25°C	-	70	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Propagation Delay	TPHZ TPZH	VDD = 10V	1, 2, 4	+25°C	-	60	ns
		VDD = 15V	1, 2, 4	+25°C	-	50	ns
Propagation Delay	TPZL TPLZ	VDD = 10V	1, 2, 4	+25°C	-	80	ns
		VDD = 15V	1, 2, 4	+25°C	-	70	ns
Transition Time	TTHL	VDD = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V	1, 2, 3	+25°C	-	25	ns
Transition Time	TTLH	VDD = 10V	1, 2, 3	+25°C	-	45	ns
		VDD = 15V	1, 2, 3	+25°C	-	35	ns
Input Capacitance	CIN	Any Inputs	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

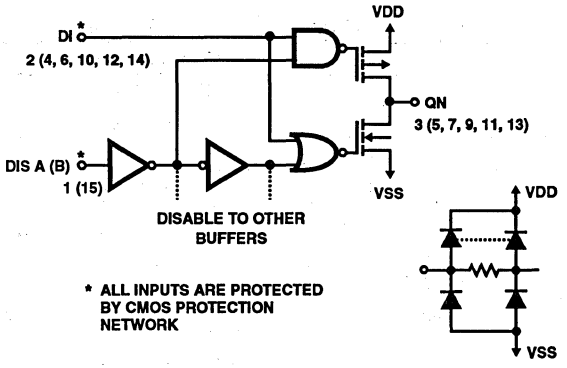
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	3, 5, 7, 9, 11, 13	1, 2, 4, 6, 8,10, 12, 14, 15	16			
Static Burn-In 2 (Note 1)	3, 5, 7, 9, 11, 13	8	1, 2, 4, 6, 10, 12, 14-16			
Dynamic Burn-In (Note 1)	-	1, 8, 15	16	3, 5, 7, 9, 11, 13	2, 4, 6, 10, 12, 14	
Irradiation (Note 2)	3, 5, 7, 9, 11, 13	8	1, 2, 4, 6, 10, 12, 14-16			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram



TRUTH TABLE

DN	DIS A (B)	Qn
0	0	0
1	0	1
X	1	High Z

X = Don't Care

FIGURE 1. LOGIC DIAGRAM OF 1 TO 6 IDENTICAL BUFFERS

Typical Performance Characteristics

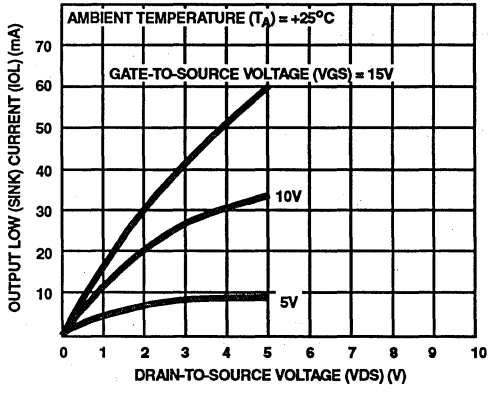


FIGURE 2. TYPICAL N-CHANNEL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

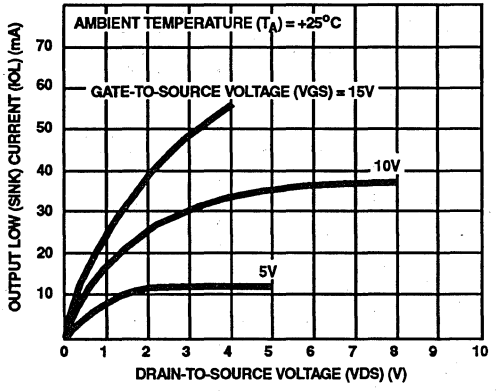


FIGURE 3. MINIMUM N-CHANNEL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

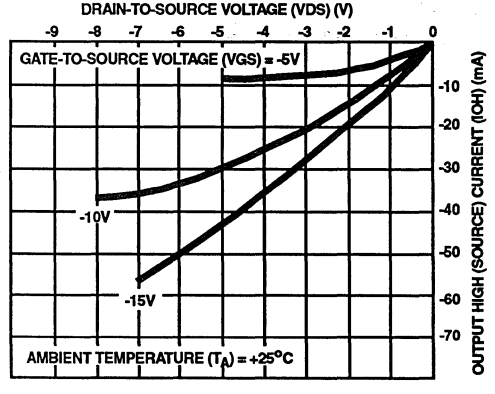


FIGURE 4. TYPICAL P-CHANNEL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

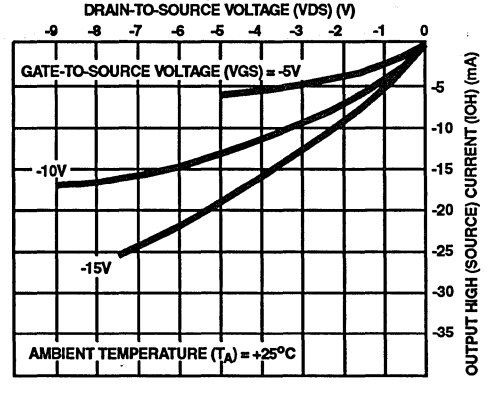


FIGURE 5. MINIMUM P-CHANNEL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

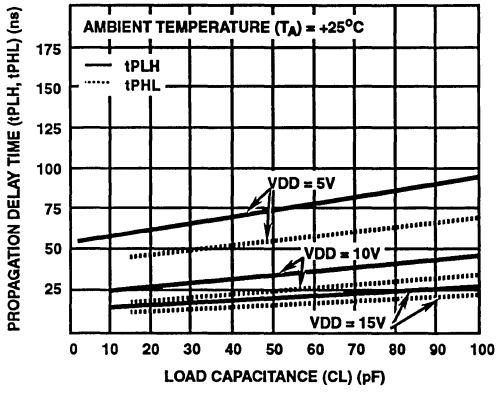


FIGURE 6. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

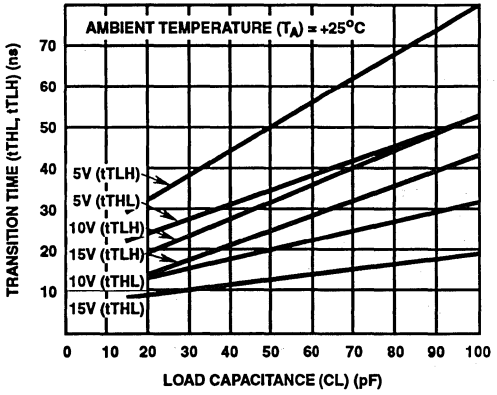


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

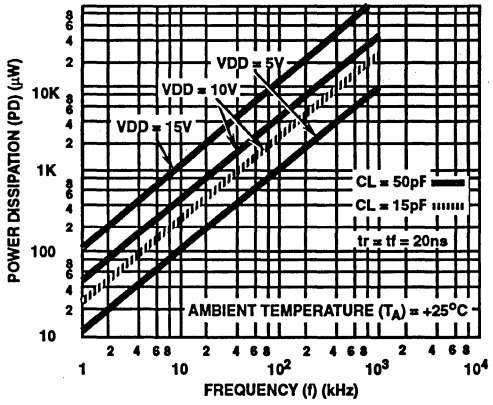
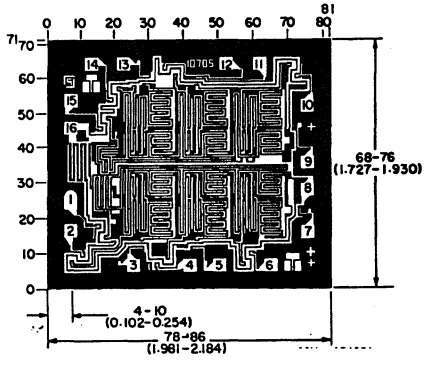


FIGURE 8. TYPICAL POWER DISSIPATION AS A FUNCTION OF FREQUENCY

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

7 LOGIC

HARRIS SEMICONDUCTOR

CD4504BMS

CMOS Hex Voltage Level Shifter for TTL-to-CMOS or CMOS-to-CMOS Operation

December 1992

Features

- High Voltage Type (20V Rating)
- Independence of Power Supply Sequence Considerations
  - VCC can Exceed VDD
  - Input Signals can Exceed Both VCC and VDD
- Up and Down Level Shifting Capability
- Shiftable Input Threshold for Either CMOS or TTL Compatibility
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Standardized Symmetrical Output Characteristics
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Description

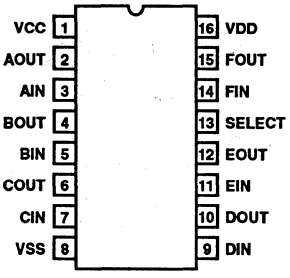
CD4504BMS hex voltage level shifter consists of six circuits which shift input signals from the VCC logic level to the VDD logic level. To shift TTL signals to CMOS logic levels, the SELECT input is at the VCC HIGH logic state. When the SELECT input is at a LOW logic state, each circuit translates signals from one CMOS level to another.

The CD4504BMS is supplied in these 16-lead outline packages:

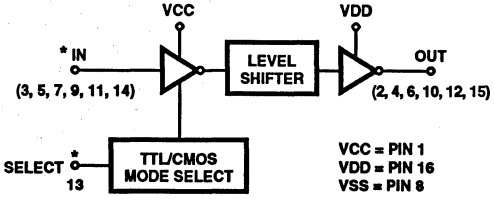
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

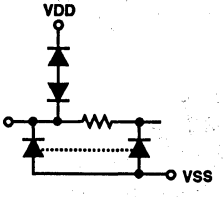
Pinout

CD4504BMS
TOP VIEW



Functional Diagram





* ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3336

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range.....-55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG).....-65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K).....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature .....+175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 4.5V, VCC = 2.8, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 4.5V, VCC = 3.0, VIN = VDD or GND		8B	-55°C			
		VDD = 18V, VCC = 18V, VIN = GND or VCC		8A	+125°C			
		VDD = 18V, VCC = 4.5V, VIN = VCC or GND		8A	+125°C			
		VDD = 4.5V, VCC = 18V, VIN = VCC or GND		8A	+125°C			
		VDD = 20V, VCC = 20V, VIN = GND or VCC		7	+25°C			
		VDD = 20V, VCC = 4.5V, VIN = VCC or GND		7	+25°C			
		VDD = 4.5V, VCC = 20V, VIN = VCC or GND		7	+25°C			

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage Low (Note 2) TTL-CMOS	VIL	VDD = 15V, VOH > 13.5V, VOL < 1V VCC = 5V	1, 2, 3	+25°C, +125°C, -55°C	-	0.8	V
Input Voltage High (Note 2) TTL-CMOS	VIH	VDD = 15V, VOH > 13.5V, VOL < 1V VCC = 5V	1, 2, 3	+25°C, +125°C, -55°C	2	-	V
Input Voltage Low (Note 2) CMOS-CMOS	VIL	VDD = 10V, VOH > 9V, VOL < 1V VCC = 5V	1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)CMOS-CMOS	VIH	VDD = 10V, VOH > 9V, VOL < 1V VCC = 5V	1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2) CMOS-CMOS	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V, VCC = 10V	1, 2, 3	+25°C, +125°C, -55°C	-	3	V
Input Voltage High (Note 2) CMOS-CMOS	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V, VCC = 10V	1, 2, 3	+25°C, +125°C, -55°C	7	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay TTL to CMOS VDD > VCC	TPHL1	VDD = 10V, VIN = VCC or GND VCC = 5V	9	+25°C	-	280	ns
			10, 11	+125°C, -55°C	-	378	ns
Propagation Delay CMOS to CMOS VDD > VCC	TPHL2	VDD = 10V, VIN = VCC or GND VCC = 5V	9	+25°C	-	240	ns
			10, 11	+125°C, -55°C	-	324	ns
Propagation Delay CMOS to CMOS VCC > VDD	TPHL3	VDD = 5V, VIN = VCC or GND VCC = 10V	9	+25°C	-	550	ns
			10, 11	+125°C, -55°C	-	743	ns
Propagation Delay TTL to CMOS VDD > VCC	TPLH1	VDD = 10V, VIN = VCC or GND VCC = 5V	9	+25°C	-	280	ns
			10, 11	+125°C, -55°C	-	378	ns
Propagation Delay CMOS to CMOS VDD > VCC	TPLH2	VDD = 10V, VIN = VCC or GND VCC = 5V	9	+25°C	-	240	ns
			10, 11	+125°C, -55°C	-	324	ns
Propagation Delay CMOS to CMOS VCC > VDD	TPLH3	VDD = 5V, VIN = VCC or GND VCC = 10V	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Transition Time	TTHL TTLH	All Modes	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low TTL - CMOS	VIL	VDD = 10V, VOH > 9V, VOL < 1V, VCC = 5V	1, 2	+25°C, +125°C, -55°C	-	0.8	V
Input Voltage High TTL - CMOS	VIH	VDD = 10V, VOH > 9V, VOL < 1V, VCC = 5V	1, 2	+25°C, +125°C, -55°C	2	-	V
Input Voltage Low CMOS - CMOS	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V, VCC = 5V	1, 2	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High CMOS - CMOS	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V, VCC = 5V	1, 2	+25°C, +125°C, -55°C	3.5	-	V
Propagation Delay TTL - CMOS, VDD > VCC	TPHL1	VDD = 15V, VCC = 5V	1, 2, 3	+25°C	-	280	ns
Propagation Delay CMOS - CMOS, VDD > VCC	TPHL2	VDD = 15V, VCC = 5V	1, 2, 3	+25°C	-	240	ns
		VDD = 15V, VCC = 10V	1, 2, 3	+25°C	-	140	ns
Propagation Delay CMOS - CMOS, VCC > VDD	TPHL3	VDD = 5V, VCC = 15V	1, 2, 3	+25°C	-	550	ns
		VDD = 10V, VCC = 15V	1, 2, 3	+25°C	-	140	ns
Propagation Delay TTL - CMOS, VDD > VCC	TPLH1	VDD = 15V, VCC = 5V	1, 2, 3	+25°C	-	280	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay CMOS - CMOS, VDD > VCC	TPLH2	VDD = 15V, VCC = 5V	1, 2, 3	+25°C	-	240	ns
		VDD = 15V, VCC = 10V	1, 2, 3	+25°C	-	140	ns
Propagation Delay CMOS - CMOS VCC > VDD	TPLH3	VDD = 5V, VCC = 15V	1, 2, 3	+25°C	-	400	ns
		VDD = 10V, VCC = 15V	1, 2, 3	+25°C	-	120	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	2, 4, 6, 10, 12, 15	3, 5, 7-9, 11, 14	16	1, 13		
Static Burn-In 2 (Note 1)	2, 4, 6, 10, 12, 15	8	16	1, 3, 5, 7, 9, 11, 13, 14		
Dynamic Burn-In (Note 1, 3)	-	8	16	1, 2, 4, 6, 10, 12, 15	3, 5, 7, 9, 11, 14	
Irradiation (Note 2)	2, 4, 6, 10, 12, 15	8	1, 3, 5, 7, 9, 11, 13, 14, 16			

NOTES:

1. Each pin except VCC, VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VCC, VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V
3. Oscillator output to be VDD/2.

Typical Performance Characteristics

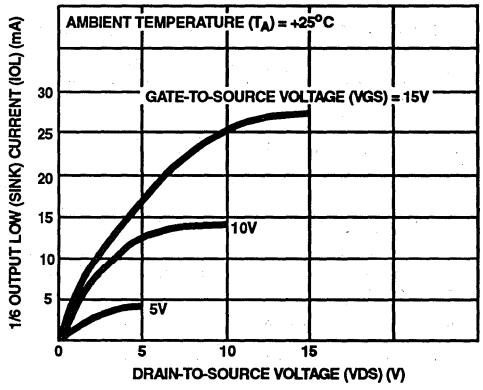


FIGURE 1. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

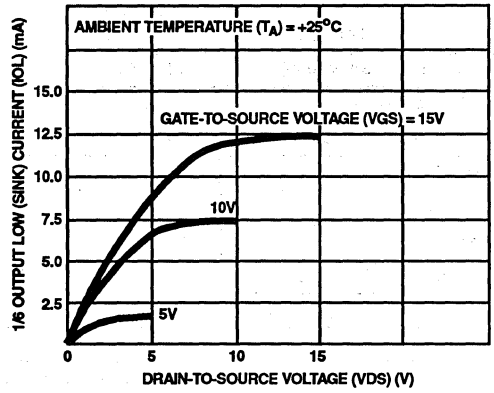


FIGURE 2. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

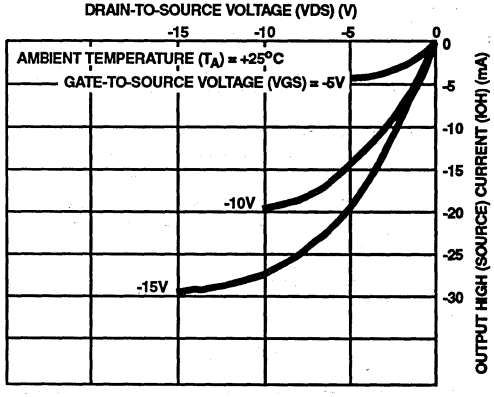


FIGURE 3. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

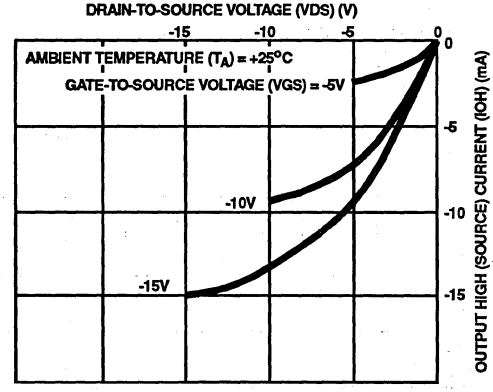


FIGURE 4. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

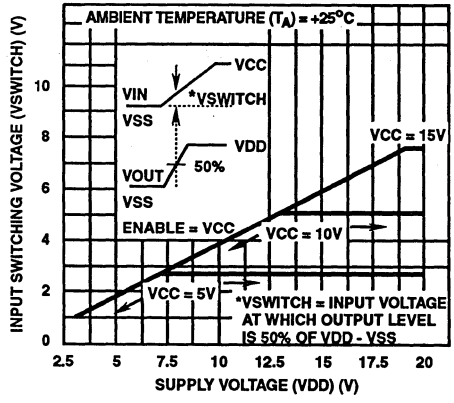


FIGURE 5. TYPICAL INPUT SWITCHING AS A FUNCTION OF HIGH LEVEL SUPPLY VOLTAGE (SELECT AT VCC-CMOS MODE)

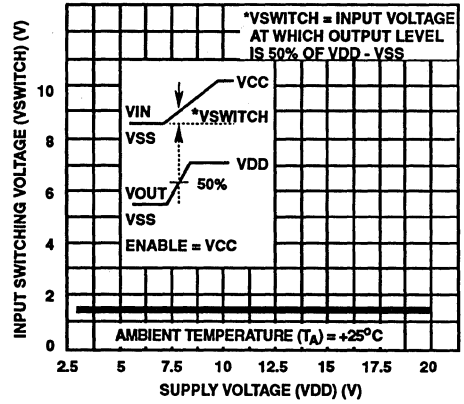


FIGURE 6. TYPICAL INPUT SWITCHING AS A FUNCTION OF HIGH LEVEL SUPPLY VOLTAGE (SELECT AT VSS-TTL MODE)

Typical Performance Characteristics (Continued)

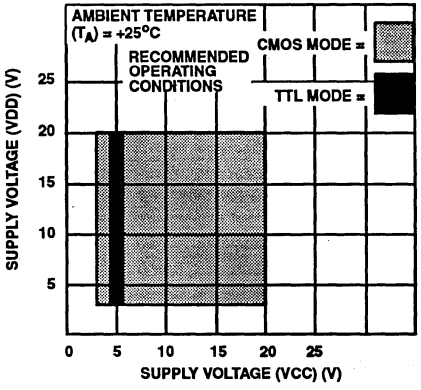
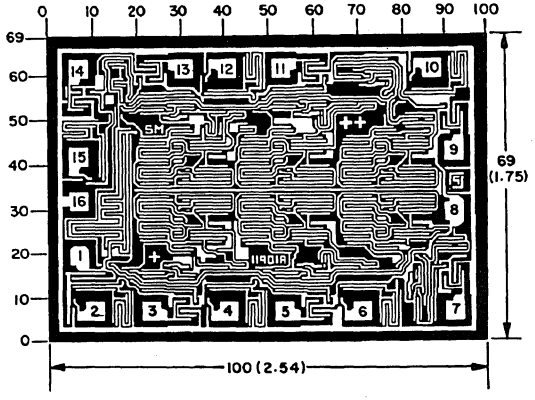


FIGURE 7. HIGH LEVEL SUPPLY VOLTAGE vs LOW LEVEL SUPPLY VOLTAGE

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4508BMS

December 1992

CMOS Dual 4-Bit Latch

Features

- High-Voltage Types (20-Volt Rating)
- Two Independent 4-Bit Latches
- Individual Master Reset for Each 4-Bit Latch
- 3-State Outputs with High-Impedance State for Bus Line Applications
- Medium-Speed Operation: tPHL = tPLH = 70nS (Typ.) at VDD = 10V and CL = 50pF
- 100% Tested for Quiescent Current at 20V
- 5V, 10V, and 15V Parametric Ratings
- Standardized, Symmetrical Output Characteristics
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and 25°C
- Noise Margin (Full Package-Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets all Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Buffer Storage
- Holding Registers
- Data Storage and Multiplexing

Description

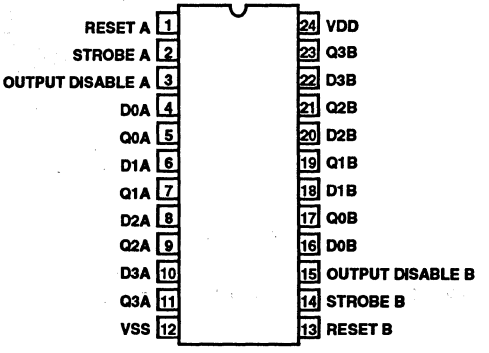
CD4508BMS dual 4-bit latch contains two identical 4-bit latches with separate STROBE, RESET, and OUTPUT DISABLE controls. With the STROBE line in the high state, the data on the "D" inputs appear at the corresponding "Q" outputs provided the DISABLE line is in the low state. Changing the STROBE line to the low state locks the data into the latch. A high on the reset line forces the outputs to a low level regardless of the state of the STROBE input. The outputs are forced to the high-impedance state for bus line applications by a high level on the DISABLE input.

The CD4508BMS is supplied in these 24 lead outline packages:

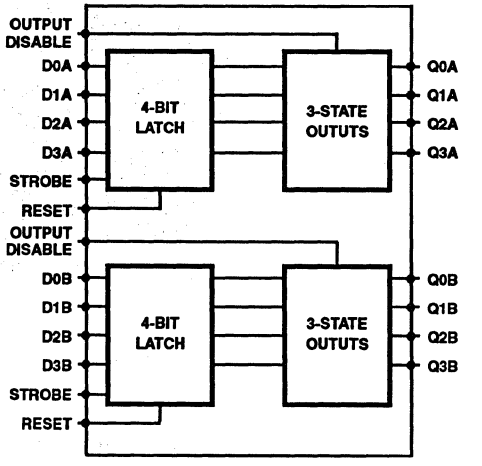
Braze Seal DIP	H4V
Frit Seal DIP	H1Z
Ceramic Flatpack	H4P

Pinout

CD4508BMS
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3337

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K).....500mW
For T_A = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature .....+175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.4	-	µA
				2	+125°C	-12	-	µA
			VDD = 18V	3	-55°C	-0.4	-	µA
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.4	µA
				2	+125°C	-	12	µA
			VDD = 18V	3	-55°C	-	0.4	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Strobe In to Data Out	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	260	ns
			10, 11	+125°C, -55°C	-	351	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Strobe In to Data Out	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	140	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Data In to Data Out	TPHL2 TPLH2	VDD = 5V	1, 2, 3	+25°C	-	210	ns
		VDD = 10V	1, 2, 3	+25°C	-	120	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns
Propagation Delay Reset to Data Out	TPHL3 TPLH3	VDD = 5V	1, 2, 3	+25°C	-	180	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Propagation Delay 3-State	TPHZ TPZH	VDD = 5V	1, 2, 4	+25°C	-	180	ns
		VDD = 10V	1, 2, 4	+25°C	-	100	ns
		VDD = 15V	1, 2, 4	+25°C	-	70	ns
Transition Time 3-State	TPLZ TPZL	VDD = 5V	1, 2, 4	+25°C	-	180	ns
		VDD = 10V	1, 2, 4	+25°C	-	100	ns
		VDD = 15V	1, 2, 4	+25°C	-	70	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Minimum Strobe Pulse Width	TWS	VDD = 5V	1, 2, 3	+25°C	-	140	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	70	ns
Minimum Data Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	50	ns
		VDD = 10V	1, 2, 3	+25°C	-	30	ns
		VDD = 15V	1, 2, 3	+25°C	-	20	ns
Minimum Data Hold Time	TH	VDD = 5V	1, 2, 3	+25°C	-	0	ns
		VDD = 10V	1, 2, 3	+25°C	-	0	ns
		VDD = 15V	1, 2, 3	+25°C	-	0	ns
Minimum Reset Pulse Width	TWR	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	140	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10μA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0μA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

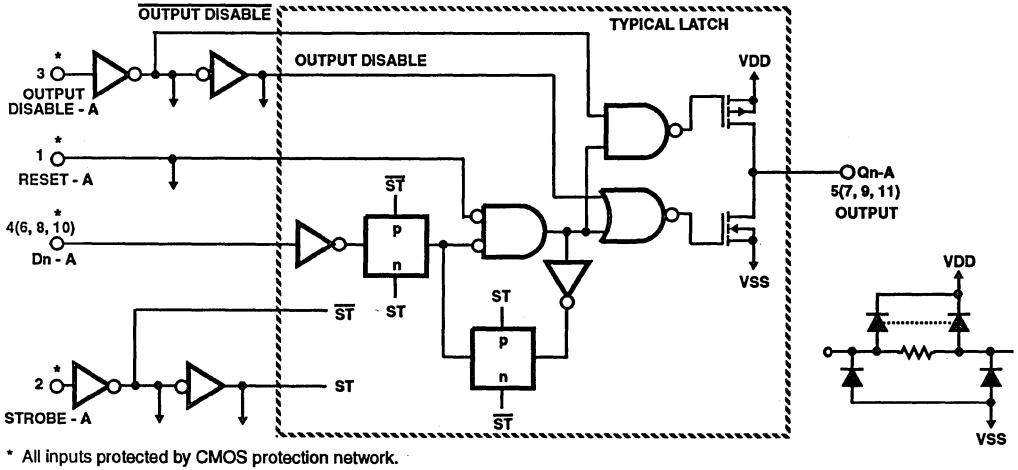
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	5, 7, 9, 11, 17, 19, 21, 23	1-4, 6, 8, 10, 12-16, 18, 20, 22	24			
Static Burn-In 2 Note 1	5, 7, 9, 11, 17, 19, 21, 23	12	1-4, 6, 8, 10, 13-16, 18, 20, 22, 24			
Dynamic Burn-In Note 1	-	1, 3, 12, 13, 15	2, 14, 24	5, 7, 9, 11, 17, 19, 21, 23	4, 6, 8, 10, 16, 18, 20, 22	-
Irradiation Note 2	5, 7, 9, 11, 17, 19, 21, 23	12	1-4, 6, 8, 10, 13-16, 18, 20, 22, 24			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram



* All inputs protected by CMOS protection network.

FIGURE 1. LOGIC DIAGRAM (A-SECTION), 1 OF 4 IDENTICAL LATCHES WITH COMMON OUTPUT DISABLE, RESET AND STROBE

TRUTH TABLE

RESET	DISABLE	STROBE	D INPUT	Q OUTPUT
0	0	1	1	1
0	0	1	0	0
0	0	0	X	LATCHED
1	0	X	X	0
X	1	X	X	Z

1 = HIGH LEVEL
0 = LOW LEVEL
X = DON'T CARE
Z = HIGH IMPEDANCE

Typical Performance Characteristics

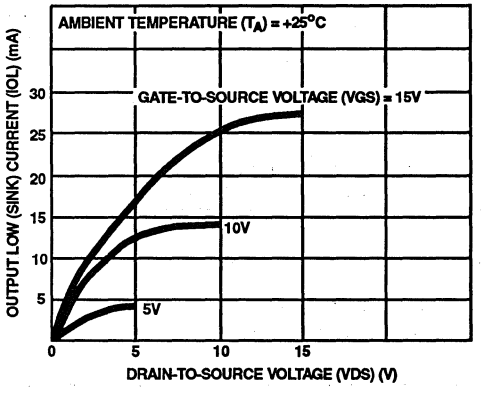


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

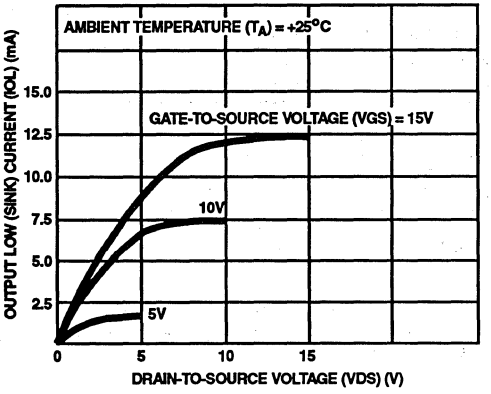


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

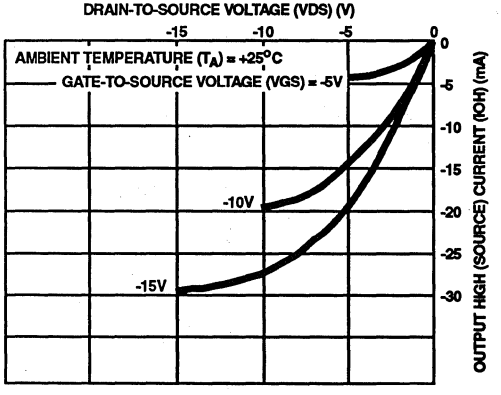


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

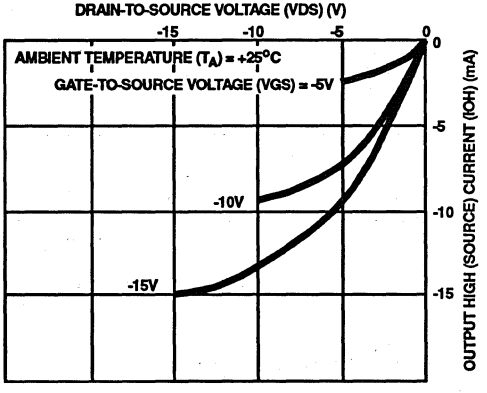


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

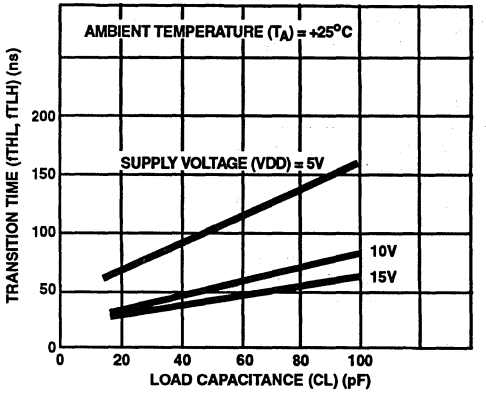


FIGURE 6. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

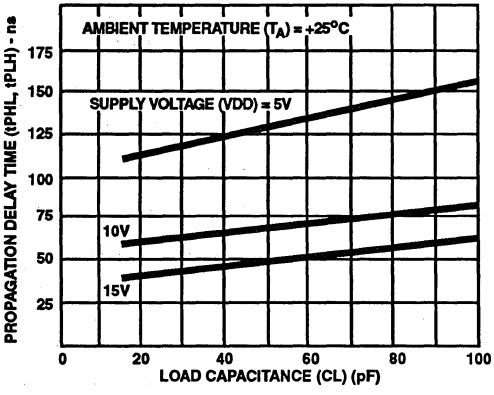


FIGURE 7. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (STROBE TO DATA OUT)

Typical Performance Characteristics (Continued)

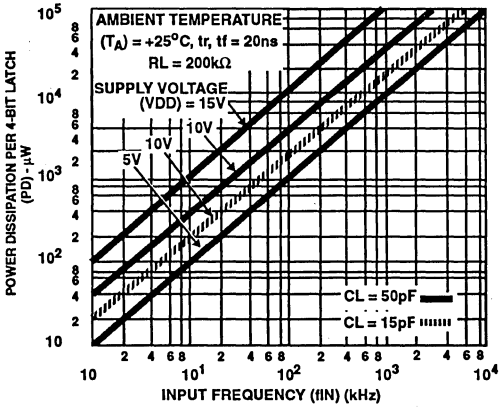
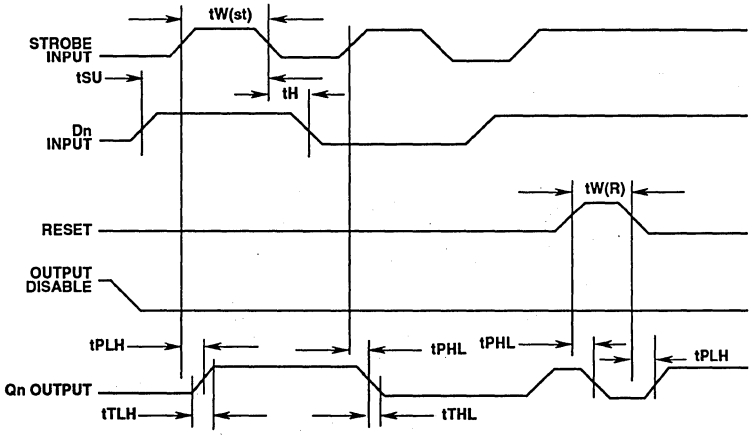
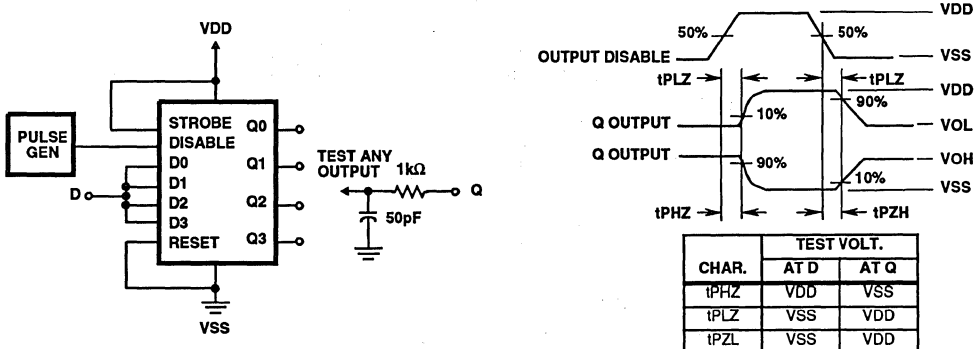


FIGURE 8. TYPICAL POWER DISSIPATION AS A FUNCTION OF FREQUENCY

Waveforms and Test Circuits



FIIGURE 9. TEST WAVEFORMS



CHAR.	TEST VOLT. AT D	AT Q
tPHZ	VDD	VSS
tPLZ	VSS	VDD
tPZL	VSS	VDD
tPZH	VDD	VSS

FIGURE 10. OUTPUT DISABLE TEST CIRCUIT AND WAVEFORMS

Bus Registers

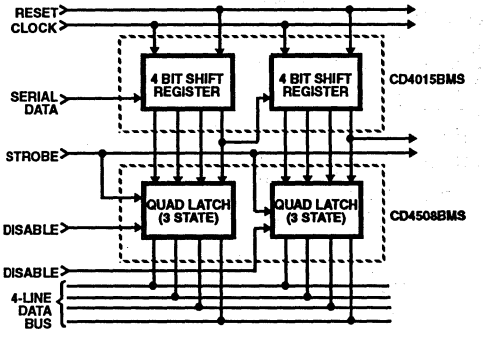
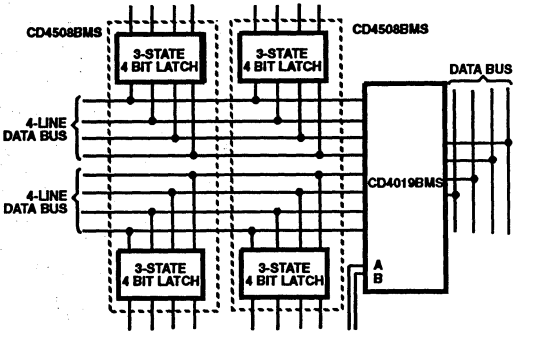


FIGURE 11. BUS REGISTER

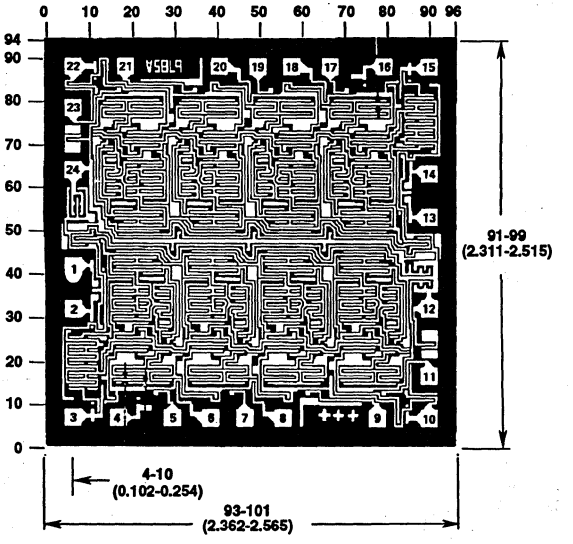


FUNCTON SELECT

A	B	FUNCTION
0	0	Inhibit (All 0)
1	0	Select A Bus
0	1	Select B Bus
1	1	AI + BI

FIGURE 12. DUAL MULTIPLEXED BUS REGISTER WITH FUNCTION SELECT

Chip Dimensions and Pad Layouts



Dimensions in parentheses are in milimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch.)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4510BMS
CD4516BMS

December 1992

CMOS Presettable Up/Down Counters

Features

- High Voltage Types (20V Rating)
- CD4510BMS - BCD Type
- CD4516BMS - Binary Type
- Medium Speed Operation
  - fCL = 8MHz Typ. at 10V
- Synchronous Internal Carry Propagation
- Reset and Preset Capability
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Standardized Symmetrical Output Characteristics
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Up/Down Difference Counting
- Multistage Synchronous Counting
- Multistage Ripple Counting
- Synchronous Frequency Dividers

Description

CD4510BMS Presettable BCD Up/Down Counter and the CD4516BMS Presettable Binary Up/Down counter consist of four synchronously clocked D-type flip-flops (with a gating structure to provide T-type flip-flop capability) connected as counters. These counters can be cleared by a high level on the RESET line, and can be preset to any binary number present on the jam inputs by a high level on the PRESET ENABLE line. The CD4510BMS will count out of non-BCD counter states in a maximum of two clock pulses in the up mode, and a maximum of four clock pulses in the down mode.

If the CARRY IN input is held low, the counter advances up or down on each positive-going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the CARRY OUT of a less significant stage to the CARRY IN of a more significant stage.

The CD4510BMS and CD4516BMS can be cascaded in the ripple mode by connecting the CARRY OUT to the clock of the next stage. If the UP/DOWN input changes during a terminal count, the CARRY OUT must be gated with the clock, and the UP/DOWN input must change while the clock is high. This method provides a clean clock signal to the subsequent counting stage. (See Figures 13, 14.)

These devices are similar to types MC14510 and MC14516.

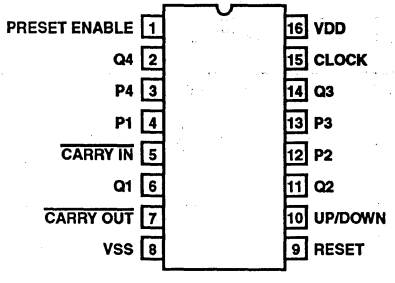
The CD4510BMS and CD4516BMS are supplied in these 16-lead outline packages:

Braze Seal DIP	*H4W	†H45
Frit Seal DIP	*FBF	†H1F
Ceramic Flatpack	H6W	

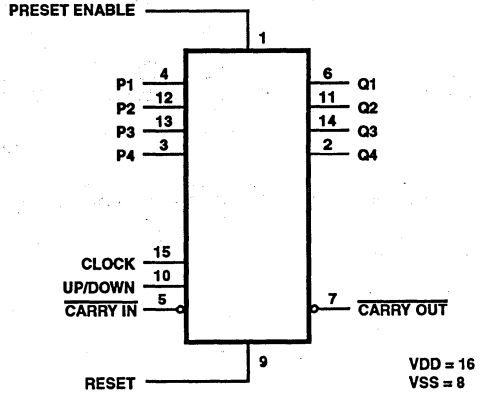
*CD4510B Only †CD4516B Only

Pinout

CD4510BMS, CD4516BMS
TOP VIEW



Functional Diagram



7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3338

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature .....+175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Q Output	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay Preset or Reset to Q	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	420	ns
			10, 11	+125°C, -55°C	-	567	ns
Propagation Delay Clock to Carry Out	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	480	ns
			10, 11	+125°C, -55°C	-	648	ns
Propagation Delay Carry In to Carry Out	TPHL4 TPLH4	VDD = 5V, VIN = VDD or GND	9	+25°C	-	250	ns
			10, 11	+125°C, -55°C	-	338	ns
Propagation Delay Preset or Reset to Carry Out	TPHL5 TPLH5	VDD = 5V, VIN = VDD or GND (Note 3)	9	+25°C	-	640	ns
			10, 11	+125°C, -55°C	-	864	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	2	-	MHz
			10, 11	+125°C, -55°C	1.48	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.
3. Reset to Carry Out (TPLH) only.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Clock to Q Output	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	150	ns
Propagation Delay Preset or Reset to Q	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	210	ns
		VDD = 15V	1, 2, 3	+25°C	-	160	ns
Propagation Delay Clock to Carry Out	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25°C	-	240	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns
Propagation Delay Carry In to Carry Out	TPHL4 TPLH4	VDD = 10V	1, 2, 3	+25°C	-	120	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Propagation Delay Preset or Reset to Carry Out	TPHL5 TPLH5	VDD = 10V	1, 2, 3, 4	+25°C	-	320	ns
		VDD = 15V	1, 2, 3, 4	+25°C	-	250	ns
Transition Time	TTLH TTHL	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2	+25°C	4	-	MHz
		VDD = 15V	1, 2	+25°C	5.5	-	MHz
Minimum Hold Time Preset Enable to JN	TH	VDD = 5V	1, 2, 3	+25°C	-	70	ns
		VDD = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Minimum Data Setup Time Preset Enable to JN	TS	VDD = 5V	1, 2, 3	+25°C	-	25	ns
		VDD = 10V	1, 2, 3	+25°C	-	10	ns
		VDD = 15V	1, 2, 3	+25°C	-	10	ns
Minimum Data Hold Time Clock to Carry In	TH	VDD = 5V	1, 2, 3	+25°C	-	60	ns
		VDD = 10V	1, 2, 3	+25°C	-	30	ns
		VDD = 15V	1, 2, 3	+25°C	-	30	ns
Minimum Clock Hold Time Clock to Up/Down	TH	VDD = 5V	1, 2, 3	+25°C	-	30	ns
		VDD = 10V	1, 2, 3	+25°C	-	30	ns
		VDD = 15V	1, 2, 3	+25°C	-	30	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. Reset to Carry Out (TPLH) only.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST PRE-IRRAD	TEST POST-IRRAD	READ AND RECORD PRE-IRRAD	READ AND RECORD POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
CD4510BMS						
Static Burn-In 1 (Note 1)	2, 6, 7, 11, 14	1, 3-5, 8-10, 12, 13, 15	16			
Static Burn-In 2 (Note 1)	2, 6, 7, 11, 14	8	1, 3-5, 9, 10, 12, 13, 15, 16			
Dynamic Burn-In (Note 1)	-	1, 3, 4, 8, 9, 12, 13	10, 16	2, 6, 7, 11, 14	15	5
Irradiation (Note 2)	2, 6, 7, 11, 14	8	1, 3-5, 9, 10, 12, 13, 15, 16			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagrams

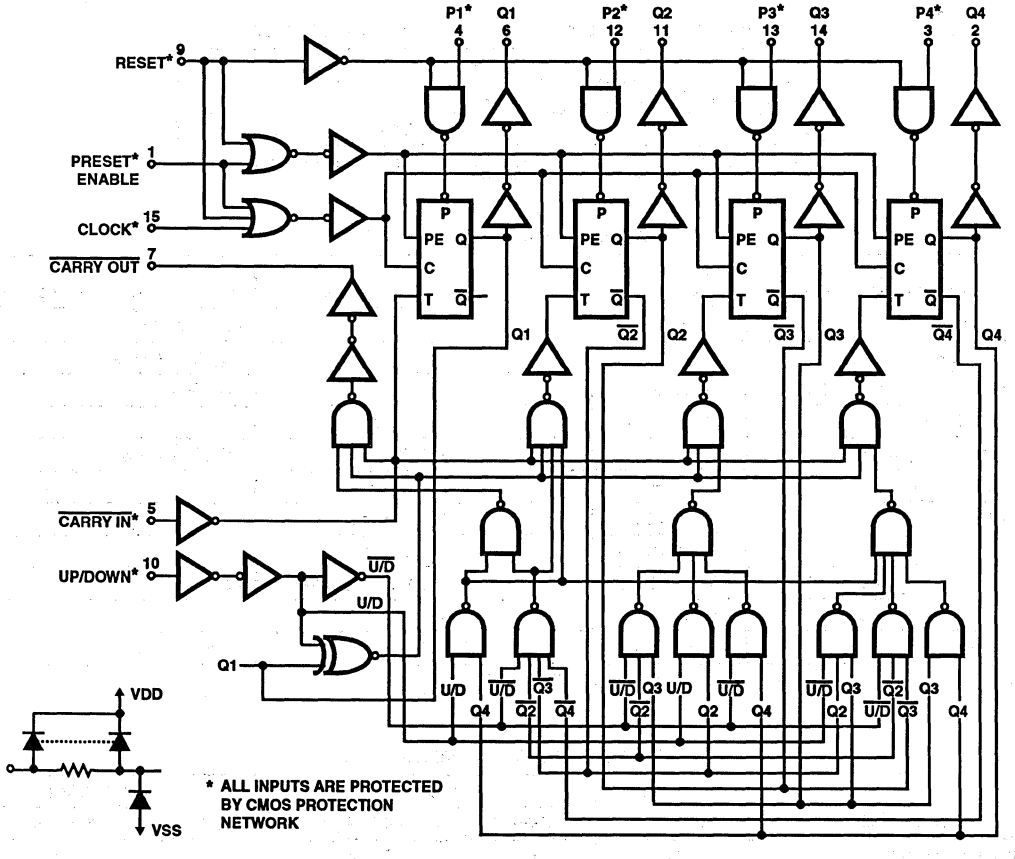


FIGURE 1. CD4510BMS

Logic Diagrams (Continued)

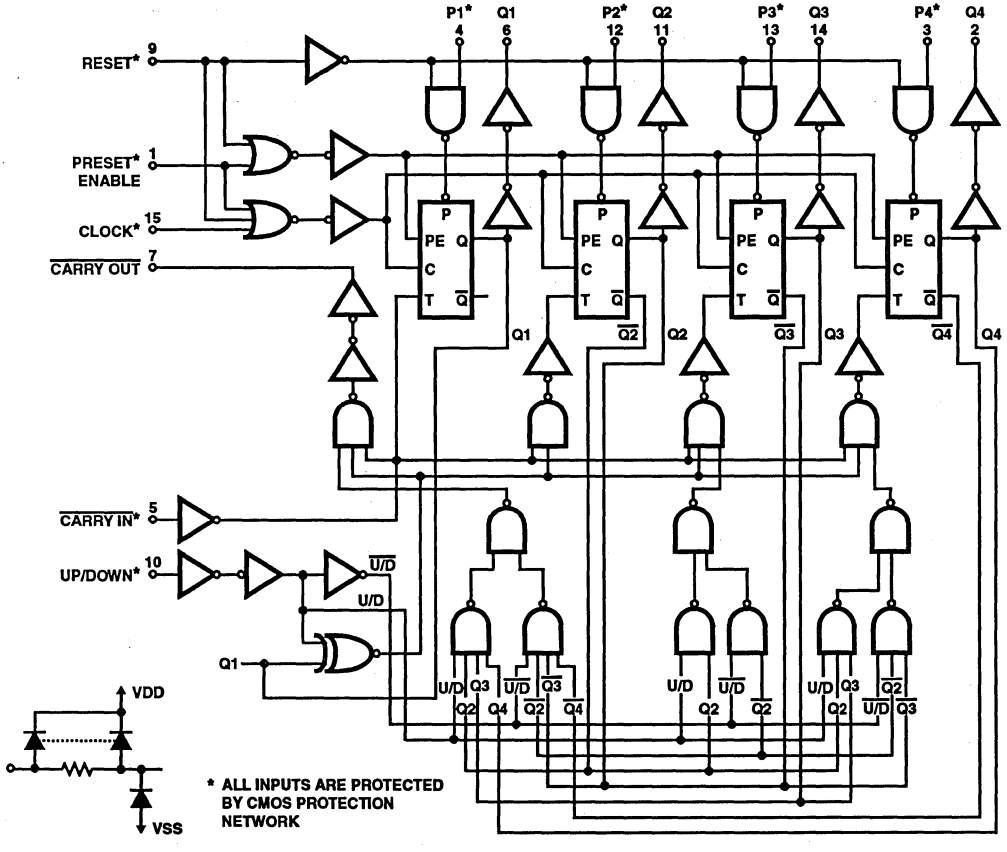


FIGURE 2. CD4516BMS

TRUTH TABLE

CL	CI	U/D	PE	R	ACTION
X	1	X	0	0	NO COUNT
⎍	0	1	0	0	COUNT UP
⎍	0	0	0	0	COUNT DOWN
X	X	X	1	0	PRESET
X	X	X	X	1	RESET

X = DON'T CARE

7 LOGIC

Typical Performance Characteristics

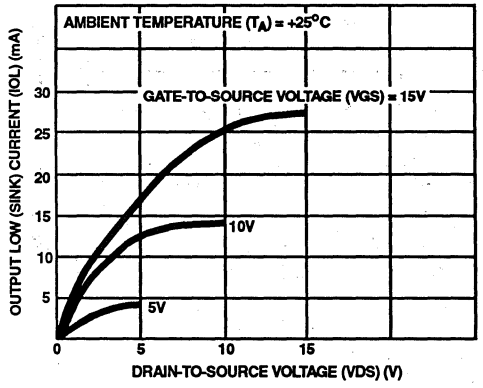


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

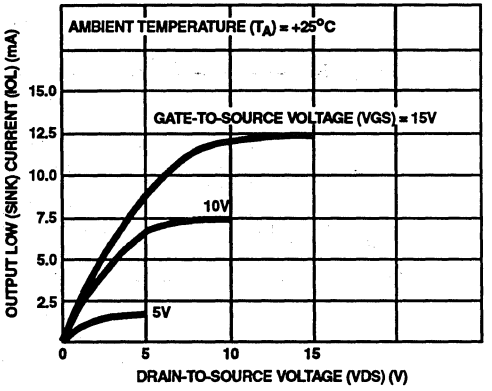


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

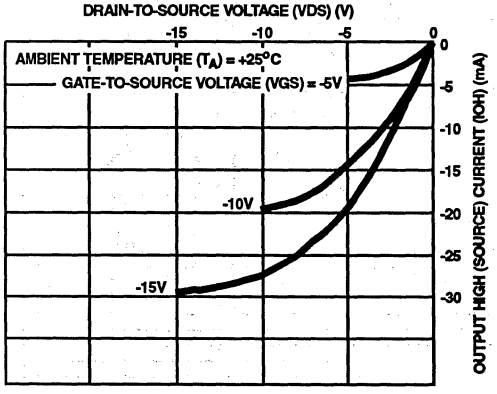


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

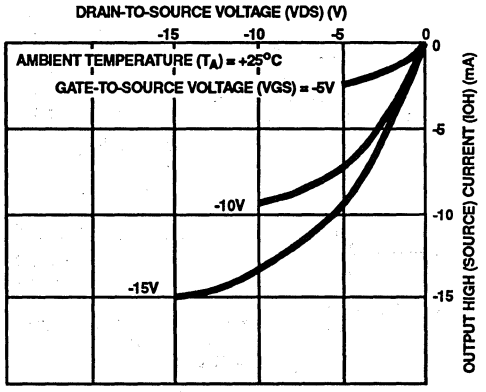


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

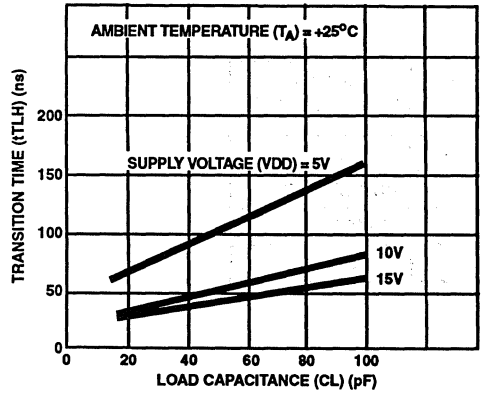


FIGURE 7. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

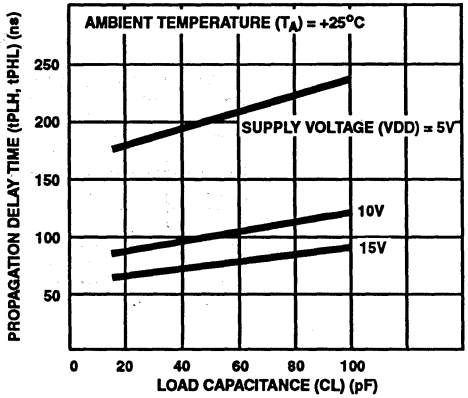


FIGURE 8. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE FOR CLOCK-TO-Q OUTPUTS

Typical Performance Characteristics (Continued)

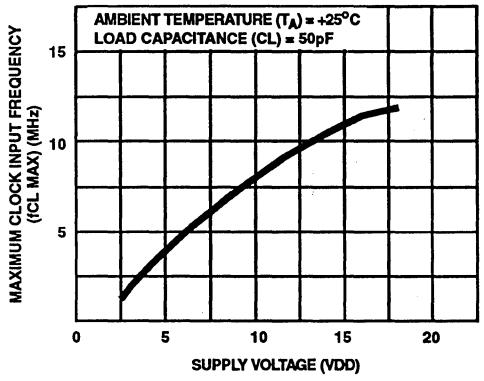


FIGURE 9. TYPICAL MAXIMUM CLOCK INPUT FREQUENCY vs SUPPLY VOLTAGE

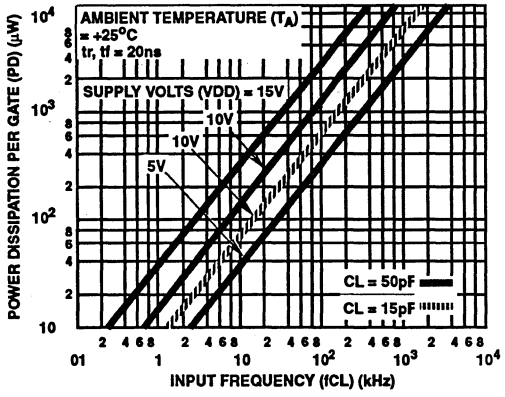
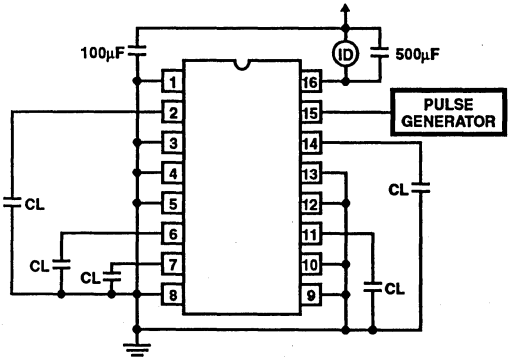


FIGURE 10. TYPICAL DYNAMIC POWER DISSIPATION vs FREQUENCY

Test Circuit and Waveform



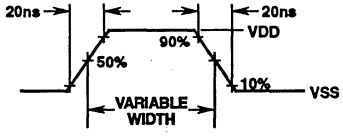
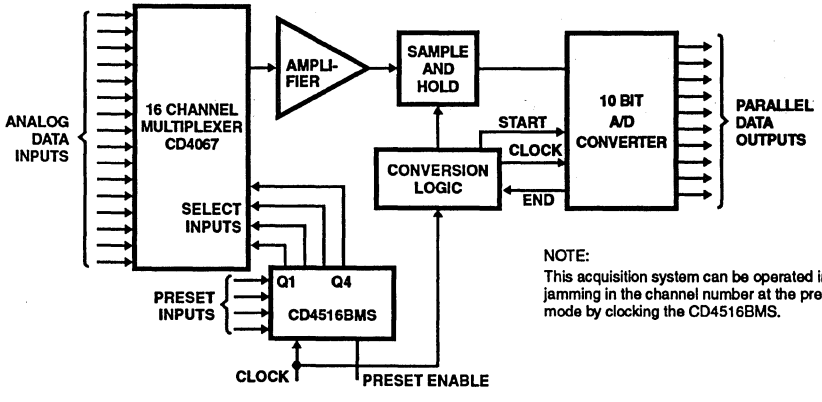


FIGURE 11. POWER DISSIPATION TEST CIRCUIT AND INPUT WAVEFORM

Acquisition System



NOTE:
This acquisition system can be operated in the random access mode by jamming in the channel number at the present inputs, or in the sequential mode by clocking the CD4516BMS.

FIGURE 12. TYPICAL 16 CHANNEL, 10 BIT DATA ACQUISITION SYSTEM

7 LOGIC

Timing Diagrams

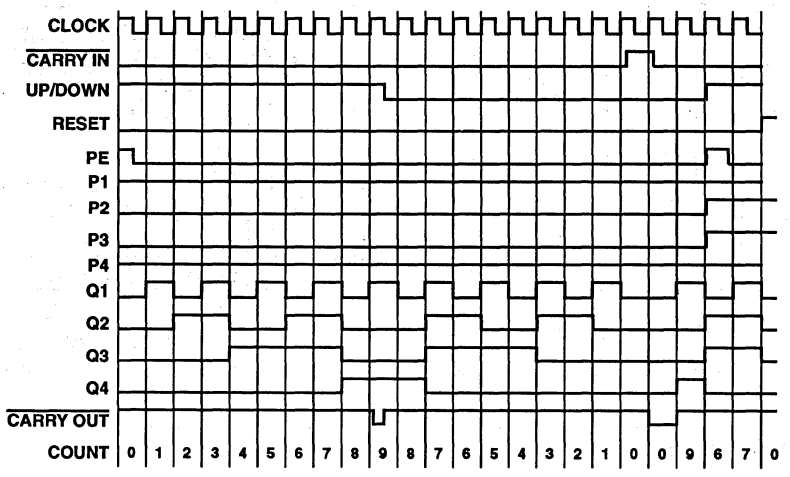


FIGURE 13. CD4510BMS

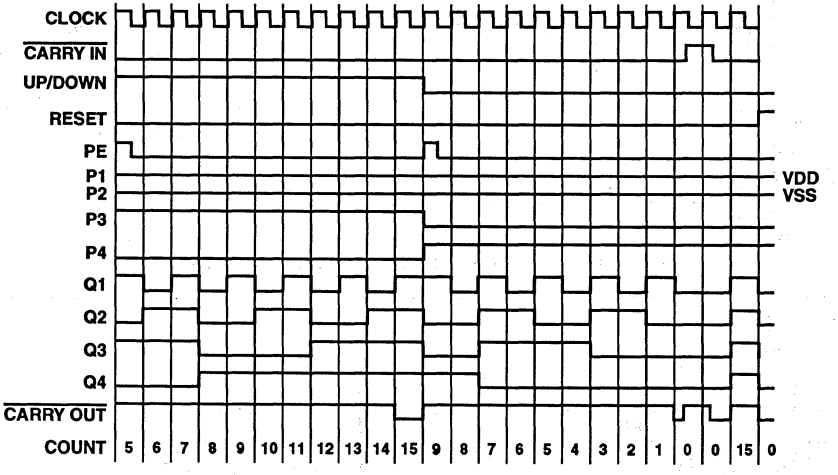
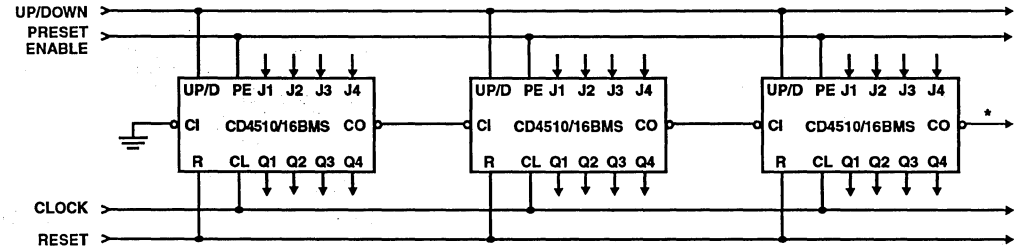


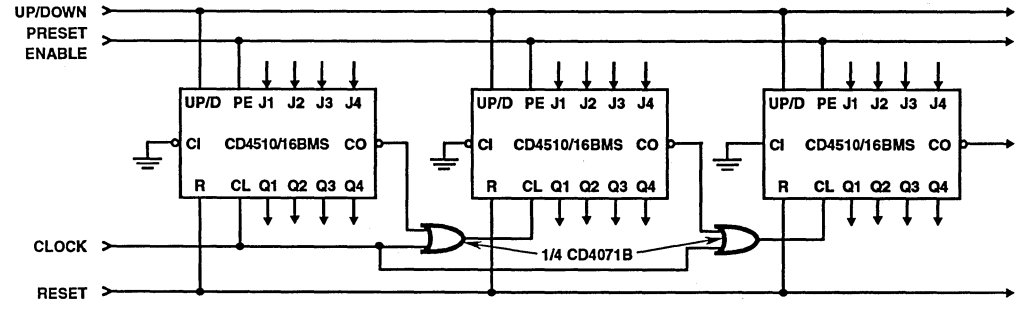
FIGURE 14. CD4516BMS

PARALLEL CLOCKING



* CARRY OUT lines at the 2nd, 3rd, etc., stages may have a negative-going glitch pulse resulting from differential delays of different CD4010/16BMS IC'S. These negative going glitches do not affect proper CD4029BMS operation. However, if the CARRY OUT signals are used to trigger other edge-sensitive logic devices, such as FF'S or counters, the CARRY OUT signals should be gated with the clock signal using a 2-input OR gate such as CD4071BMS.

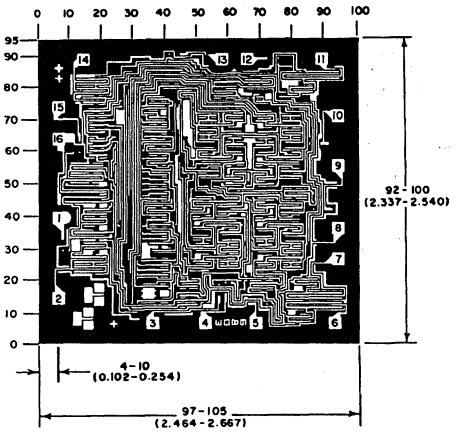
RIPPLE CLOCKING



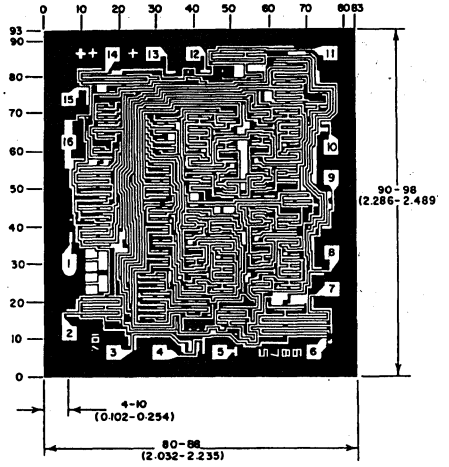
Ripple Clocking Mode: The up/down control can be changed at any count. The only restriction on changing the up/down control is that the clock input to the first counting stage must be high. For cascading counters operating in a fixed up-count or down-count mode, the OR gates are not required between stages, and CO is connected directly to the CL input of the next stage with CI grounded.

FIGURE 15. CASCADING COUNTER PACKAGES

Chip Dimensions and Pad Layouts



CD4510BMS



CD4510BMS

Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4511BMS

CMOS BCD-to-7-Segment Latch Decoder Drivers

December 1992

Features

- High Voltage Type (20V Rating)
- High Output Sourcing Capability up to 25mA
- Input Latches for BCD Code Storage
- Lamp Test and Blanking Capability
- 7 Segment Outputs Blanked for BCD Input Codes > 1001
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C

Applications

- Driving Common Cathode LED Displays
- Multiplexing with Common Cathode LED Displays
- Driving Incandescent Displays
- Driving Low Voltage Fluorescent Displays

Description

CD4511BMS is a BCD-to-7-Segment latch decoder drivers constructed with CMOS logic and n-p-n bipolar transistor output devices on a single monolithic structure. These devices combine the low quiescent power dissipation and high noise immunity features of Harris CMOS with n-p-n bipolar output transistors capable of sourcing up to 25mA. This capability allows the CD4511BMS types to drive LED's and other displays directly.

Lamp Test ($\overline{LT}$), Blanking ($\overline{BL}$), and Latch Enable or Strobe inputs are provided to test the display, shut off or intensity modulate it, and store or strobe a BCD code, respectively. Several different signals may be multiplexed and displayed when external multiplexing circuitry is used.

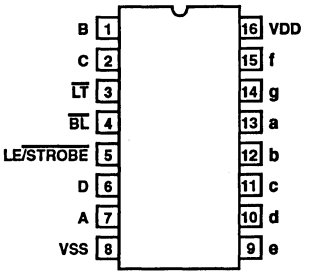
These devices are similar to the type MC14511.

The CD4511BMS is supplied in these 16-lead outline packages:

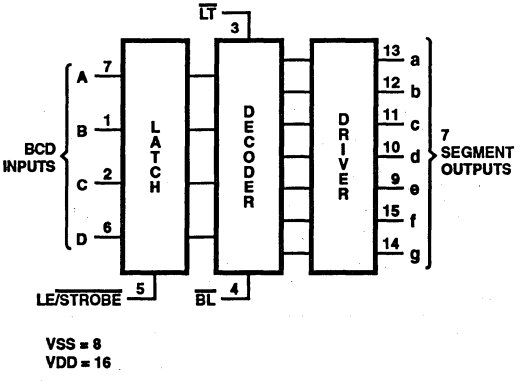
Braze Seal DIP	H4W
Frit Seal DIP	H2R
Ceramic Flatpack	H6W

Pinout

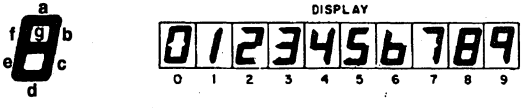
CD4511BMS
TOP VIEW



Functional Diagram



7-Segment Display



7 LOGIC

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range.....-55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG).....-65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K).....500mW
For T_A = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature .....+175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1	+25°C	14.1	-	V
				2	+125°C	14.2		V
				3	-55°C	14.0		V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	1	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	2.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	6.8	-	mA
Output Drive Voltage	LVOH5	VDD = 5V, IOH = -20mA		1	+25°C	3.4	-	V
Output Drive Voltage	LVOH10	VDD = 10V, IOH = -20mA		1	+25°C	8.6	-	V
Output Drive Voltage	LVOH15	VDD = 15V, IOH = -20mA		1	+25°C	13.7	-	V
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 3.6V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 3.6V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 12.6V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 12.6V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Data to Output	TPHL	VDD = 5V, VIN = VDD or GND	9	+25°C	-	1040	ns
			10, 11	+125°C, -55°C	-	1404	ns
Propagation Delay Data to Output	TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	1320	ns
			10, 11	+125°C, -55°C	-	1782	ns
Transition Time	TTHL	VDD = 5V, VIN = VDD or GND	9	+25°C	-	310	ns
			10, 11	+125°C, -55°C	-	419	ns
Transition Time	TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	80	ns
			10, 11	+125°C, -55°C	-	108	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C	4.1	-	V
			1, 2	+125°C	4.2	-	V
			1, 2	-55°C	4.0	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C	9.1	-	V
			1, 2	+125°C	9.2	-	V
			1, 2	-55°C	9.0	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS(Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Data to Output	TPHL	VDD = 10V	1, 2, 3	+25°C	-	420	ns
		VDD = 15V	1, 2, 3	+25°C	-	300	ns
Propagation Delay Data to Output	TPLH	VDD = 10V	1, 2, 3	+25°C	-	520	ns
		VDD = 15V	1, 2, 3	+25°C	-	360	ns
Propagation Delay ($\overline{BT}$)	TPHL	VDD = 5V	1, 2, 3	+25°C	-	700	ns
		VDD = 10V	1, 2, 3	+25°C	-	350	ns
		VDD = 15V	1, 2, 3	+25°C	-	250	ns
Propagation Delay ($\overline{BT}$)	TPLH	VDD = 5V	1, 2, 3	+25°C	-	800	ns
		VDD = 10V	1, 2, 3	+25°C	-	350	ns
		VDD = 15V	1, 2, 3	+25°C	-	300	ns
Propagation Delay ($\overline{LT}$)	TPHL	VDD = 5V	1, 2, 3	+25°C	-	500	ns
		VDD = 10V	1, 2, 3	+25°C	-	250	ns
		VDD = 15V	1, 2, 3	+25°C	-	170	ns
Propagation Delay ($\overline{LT}$)	TPLH	VDD = 5V	1, 2, 3	+25°C	-	300	ns
		VDD = 10V	1, 2, 3	+25°C	-	150	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Transition Time	TTHL	VDD = 10V	1, 2, 3	+25°C	-	185	ns
		VDD = 15V	1, 2, 3	+25°C	-	160	ns
Transition Time	TTLH	VDD = 10V	1, 2, 3	+25°C	-	60	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Data Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	150	ns
		VDD = 10V	1, 2, 3	+25°C	-	70	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Minimum Data Hold Time	TH	VDD = 5V	1, 2, 3	+25°C	-	0	ns
		VDD = 10V	1, 2, 3	+25°C	-	0	ns
		VDD = 15V	1, 2, 3	+25°C	-	0	ns
Minimum Strobe Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	400	ns
		VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Output Drive Voltage	LVOH5	VDD = 5V, IOH = -10mA	1, 2	+25°C	3.9	-	V
			1, 2	+125°C	3.9	-	V
			1, 2	-55°C	3.8	-	V
		VDD = 5V, IOH = -20mA	1, 2	-55°C	3.55	-	V
		VDD = 5V, IOH = -25mA	1, 2	+25°C	3.1	-	V
			1, 2	-55°C	3.4	-	V
Output Drive Voltage	LVOH10	VDD = 10V, IOH = -10mA	1, 2	+25°C	9.0	-	V
			1, 2	+125°C	9.0	-	V
			1, 2	-55°C	8.85	-	V
		VDD = 10V, IOH = -20mA	1, 2	+125°C	8.4	-	V
			1, 2	-55°C	8.7	-	V
		VDD = 10V, IOH = -25mA	1, 2	+25°C	8.3	-	V
			1, 2	-55°C	8.6	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS(Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Drive Voltage	LVOH15	VDD = 15V, IOH = -10mA	1, 2	+25°C	14.0	-	V
			1, 2	+125°C	14.0	-	V
			1, 2	-55°C	13.9	-	V
		VDD = 15V, IOH = -20mA	1, 2	+125°C	13.5	-	V
			1, 2	-55°C	13.75	-	V
		VDD = 15V, IOH = -25mA	1, 2	+25°C	13.5	-	V
			1, 2	-55°C	13.65	-	V
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	9-15	1-8	16			
Static Burn-In 2 (Note 1)	9-15	8	1-7, 16			
Dynamic Burn-In (Note 1)	9-15	5, 8	3, 4, 16	-	1, 2, 7	6
Irradiation (Note 2)	9-15	8	1-7, 16			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram

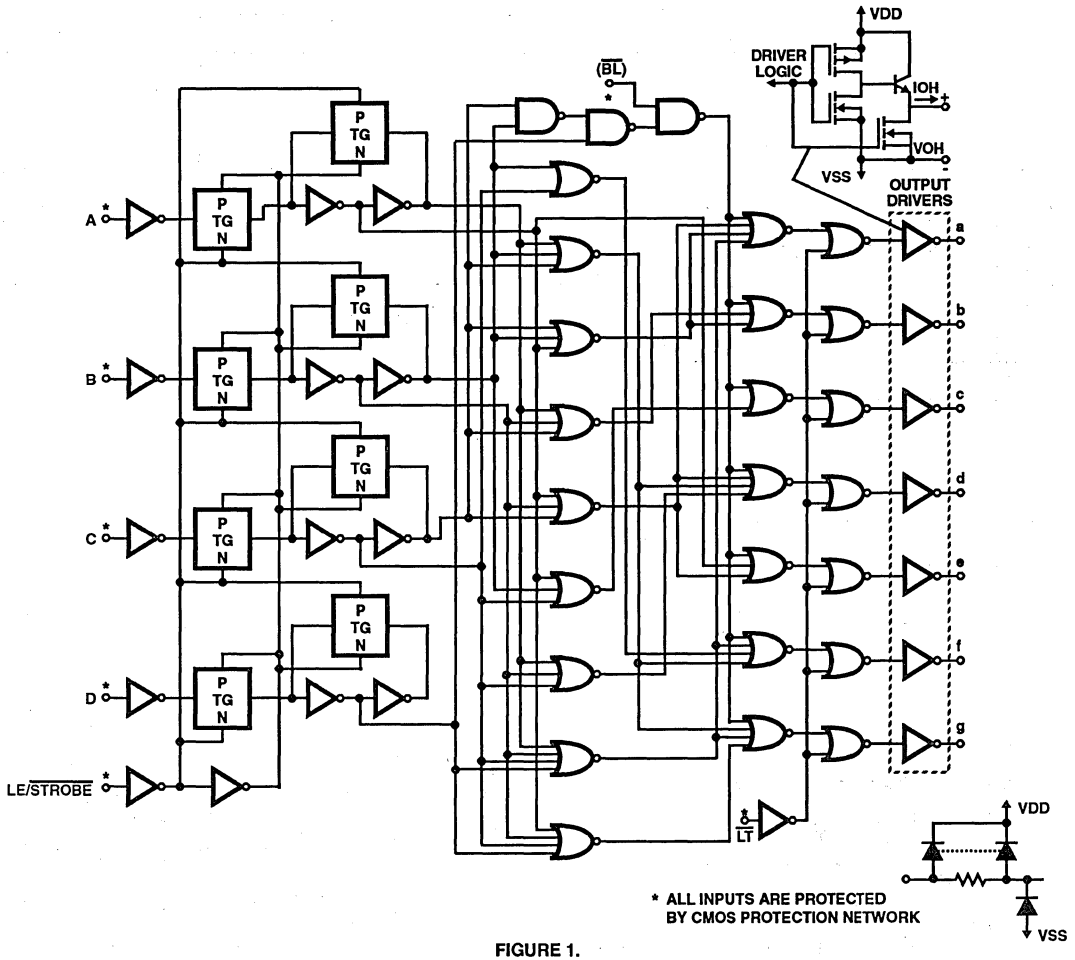


FIGURE 1.

TRUTH TABLE

LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5

TRUTH TABLE (Continued)

LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X	*							*

X = Don't Care

* Depends on BCD code previously applied when LE = 0

NOTE: Display is blank for all illegal input codes (BCD > 1001).

Typical Performance Characteristics

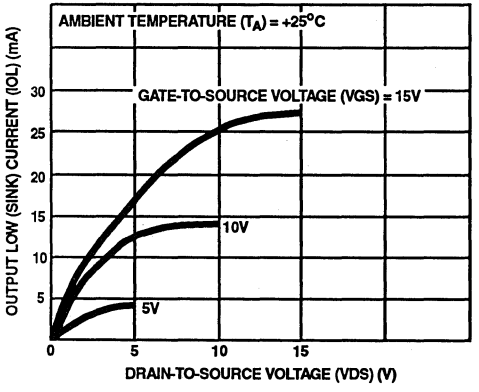


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

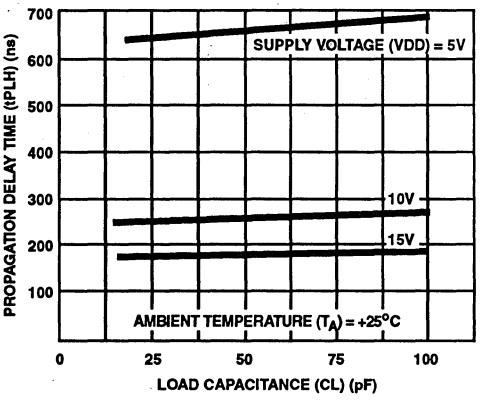


FIGURE 3. TYPICAL DATA-TO-OUTPUT, LOW-TO-HIGH-LEVEL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics

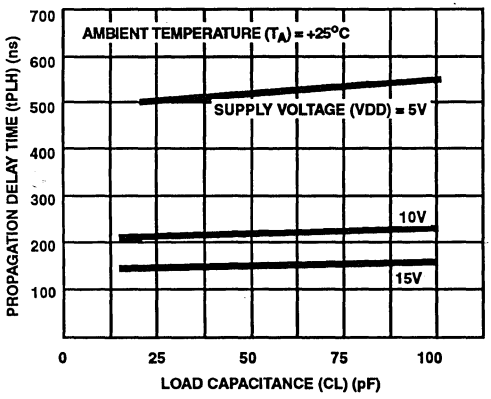


FIGURE 4. TYPICAL DATA-TO-OUTPUT, HIGH-TO-LOW-LEVEL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

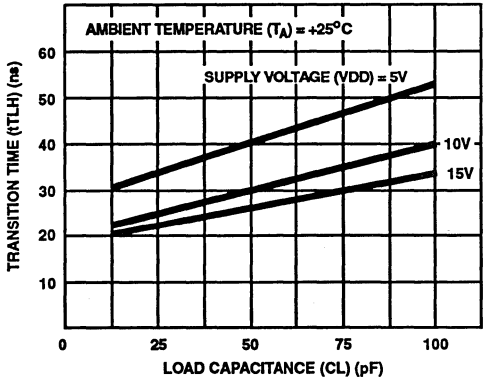


FIGURE 5. TYPICAL LOW-TO-HIGH-LEVEL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

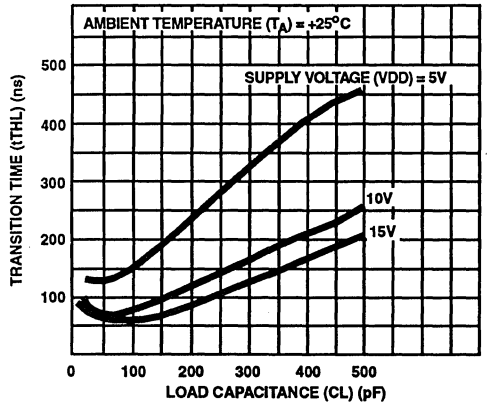


FIGURE 6. TYPICAL HIGH-TO-LOW TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

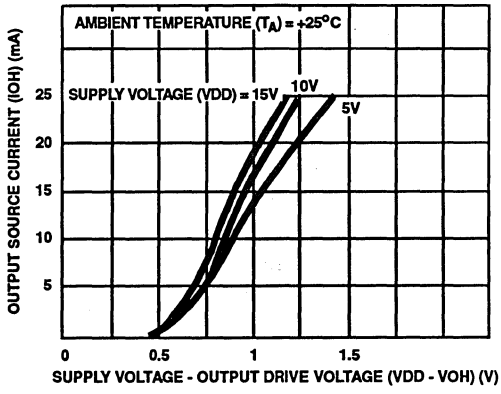


FIGURE 7. TYPICAL VOLTAGE DROP (VDD TO OUTPUT) vs OUTPUT SOURCE CURRENT AS A FUNCTION OF SUPPLY

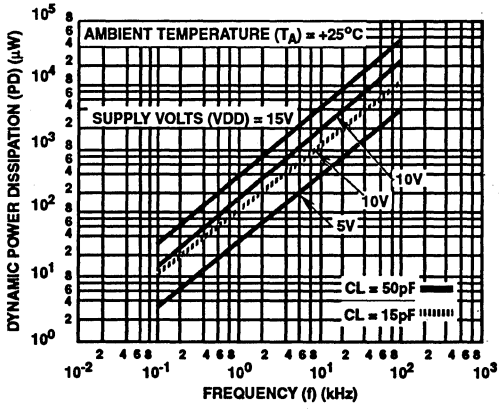
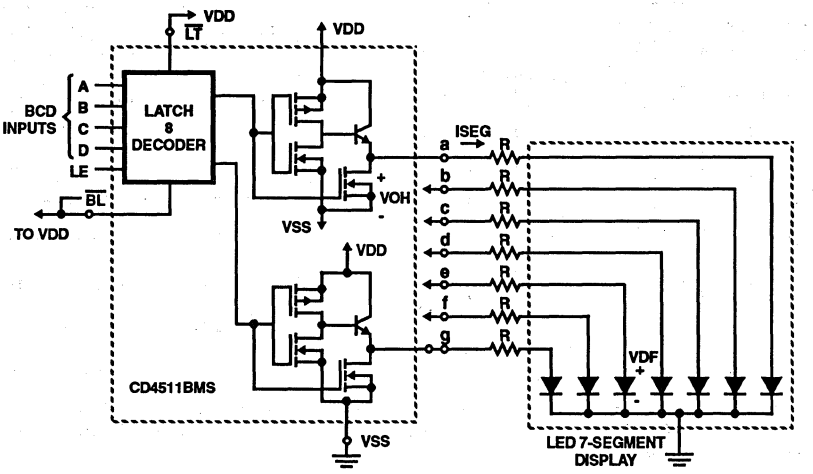


FIGURE 8. TYPICAL DYNAMIC POWER DISSIPATION CHARACTERISTICS

Applications Interfacing with Various Displays

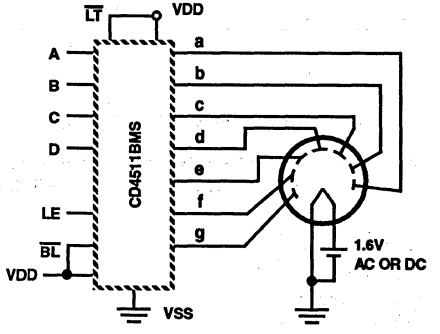


DUTY CYCLE = 100%

ISEG = IDIODEAVG. = 20mA AT LUMINOUS INTENSITY/SEGMENT = 250μcd

$$R = \frac{VOH - VDF}{ISEG}$$

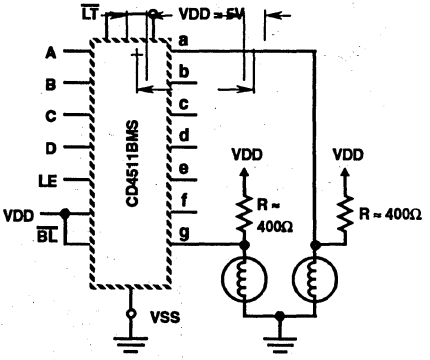
FIGURE 9. DRIVING COMMON CATHODE 7-SEGMENT LED DISPLAYS (EXAMPLE HEWLET-PACKARD 5082-7740)



A MEDIUM BRIGHTNESS INTENSITY DISPLAY CAN BE OBTAINED WITH LOW VOLTAGE FLUORESCENT DISPLAYS SUCH AS THE TUNG-SOL DIGIVAC S/G* SERIES

* Trademark Tung-Sol Division Wagner Electric Co.

FIGURE 10. DRIVING LOW VOLTAGE FLOURESCENT DISPLAYS



2 OF 7 SEGMENTS SHOWN CONNECTED

RESISTORS R FROM VDD TO EACH 7-SEGMENT DRIVER OUTPUT ARE CHOSEN TO KEEP ALL NUMITRON SEGMENTS SLIGHTLY ON AND WARM

FIGURE 11. DRIVING INCANDESCENT DISPLAYS (RCA NUMITRON DR2000 SERIES DISPLAYS)

Applications Interfacing with Various Displays (Continued)

MULTIPLEXING SCHEME SHOWING 2 OF 7 SEGMENTS CONNECTED

TRANSISTORS T1 - T4 (2N3053 OR 2N2102) HAVE IC MAX. RATING > 7 x ISEG

DUTY CYCLE = 25%

ISEG = (IDIODEAVG) x 4

$$R = \frac{(VOH - VDF - VCE)}{ISEG}$$

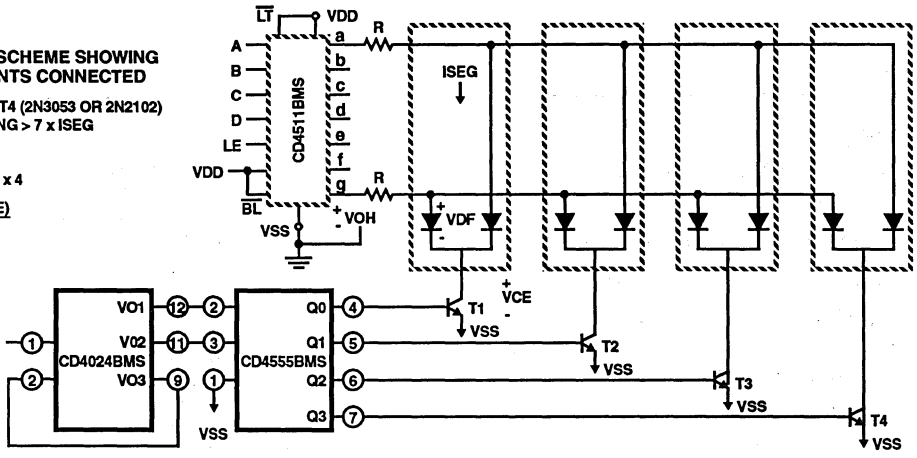


FIGURE 12. MULTIPLEXING WITH COMMON CATHODE 7-SEGMENT LED DISPLAYS (EXAMPLE HEWLET-PACKARD 5082-7404 4 CHARACTER DISPLAY OR 4 DISCRETE MONOSANTO MAN 3 DISPLAYS)

Waveforms

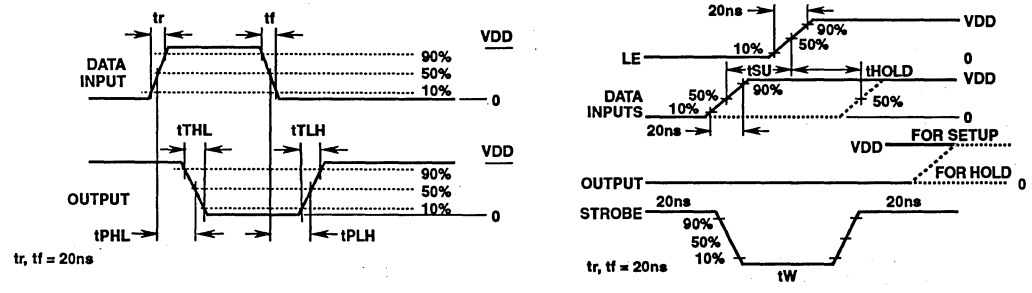
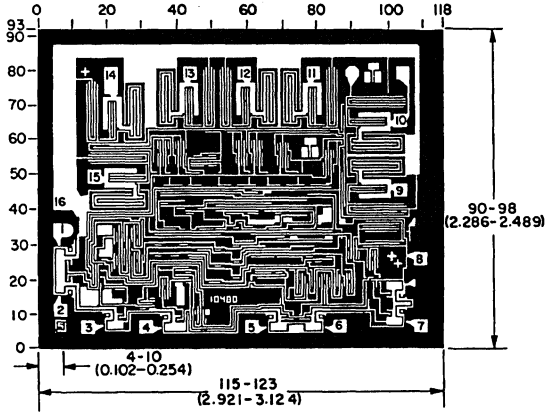


FIGURE 13. DYNAMIC WAVEFORMS

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4512BMS

December 1992

CMOS Dual 4-Bit Latch

Features

- High-Voltage Types (20-Volt Rating)
- 3-State Outputs
- Standardized, Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- 5V, 10V, and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and 25°C
- Noise Margin (Full Package-Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets all Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Digital Multiplexing
- Number-sequence Generation
- Signal Gating

Description

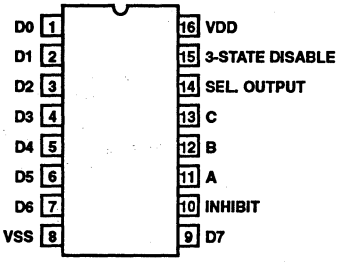
CD4512BMS is an 8-channel data selector featuring a three-state output that can interface directly with, and drive, data lines of bus-oriented systems.

The CD4512BMS is supplied in these 16 lead outline packages:

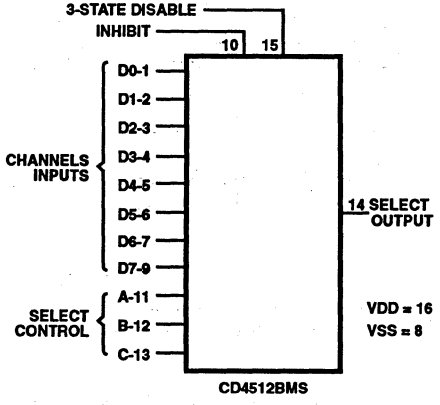
Braze Seal DIP	H4S
Frit Seal DIP	H1E
Ceramic Flatpack	H3X

Pinout

CD4512BMS
TOP VIEW



Functional Diagram



File Number 3340

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.4	-	µA
				2	+125°C	-12	-	µA
			VDD = 18V	3	-55°C	-0.4	-	µA
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.4	µA
				2	+125°C	-	12	µA
			VDD = 18V	3	-55°C	-	0.4	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

7 LOGIC

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Inhibit to Output	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	280	ns
			10, 11	+125°C, -55°C	-	378	ns
Propagation Delay "A" Select to Output	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay Data to Output	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	360	ns
			10, 11	+125°C, -55°C	-	486	ns
Propagation Delay 3-State Disable	TPHZ TPZH	VDD = 5V, VIN = VDD or GND (Note 2, 3)	9	+25°C	-	120	ns
			10, 11	+125°C, -55°C	-	162	ns
Propagation Delay 3-State Disable	TPLZ TPZL	VDD = 5V, VIN = VDD or GND (Note 2, 3)	9	+25°C	-	120	ns
			10, 11	+125°C, -55°C	-	162	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND (Note 2, 3)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Inhibit to Output	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	140	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Propagation Delay "A" Select ot Output	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	170	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Propagation Delay Data to Output	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25°C	-	150	ns
		VDD = 15V	1, 2, 3	+25°C	-	110	ns
Propagation Delay 3-State Enable	TPHZ TPZH	VDD = 10V	1, 2, 4	+25°C	-	60	ns
		VDD = 15V	1, 2, 4	+25°C	-	40	ns
Propagation Delay 3-State Enable	TPLZ TPZL	VDD = 10V	1, 2, 4	+25°C	-	60	ns
		VDD = 15V	1, 2, 4	+25°C	-	40	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0μA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

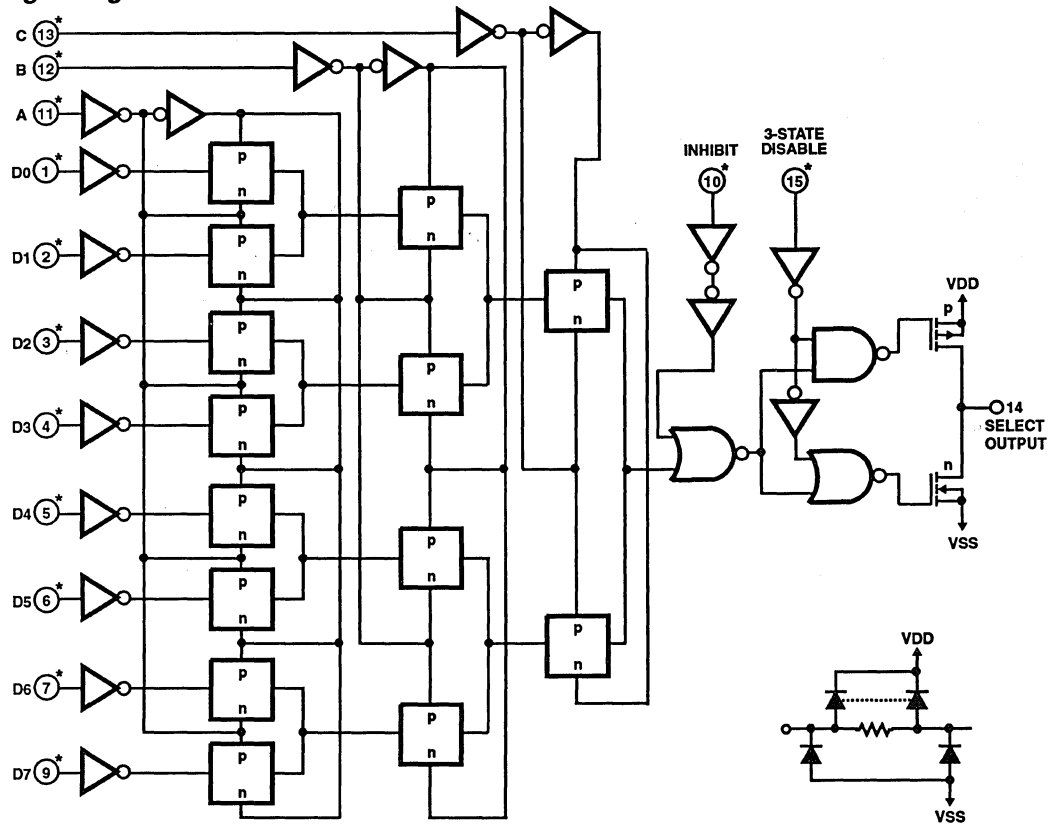
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	14	1-13, 15	16			
Static Burn-In 2 Note 1	14	8	1-7, 9-13, 15, 16			
Dynamic Burn-In Note 1	-	8, 10, 15	16	14	1-7, 9, 11, 12	13
Irradiation Note 2						

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram



* All inputs protected by CMOS protection network.

FIGURE 1. LOGIC DIAGRAM

TRUTH TABLE

SELECT CONT.			INH	3-STATE DISABLE	SELECT OUTPUT
A	B	C			
0	0	0	0	0	D0
1	0	0	0	0	D1
0	1	0	0	0	D2
1	1	0	0	0	D3
0	0	1	0	0	D4
1	0	1	0	0	D5
0	1	1	0	0	D6
1	1	1	0	0	D7
X	X	X	1	0	0
X	X	X	X	1	High Z

1 = HIGH LEVEL
0 = LOW LEVEL

X = DON'T CARE

Typical Performance Characteristics

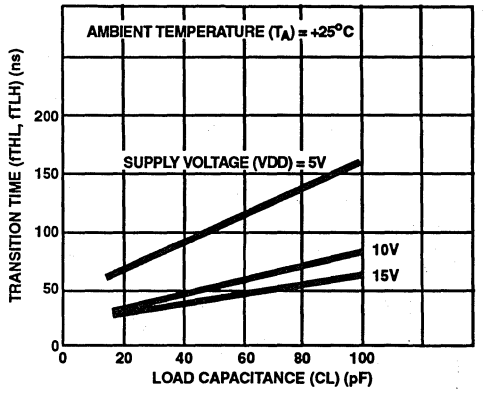


FIGURE 2. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

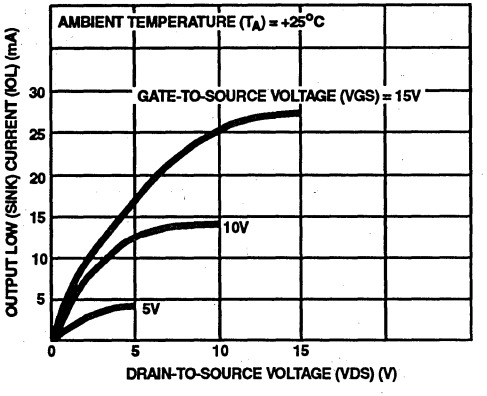


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

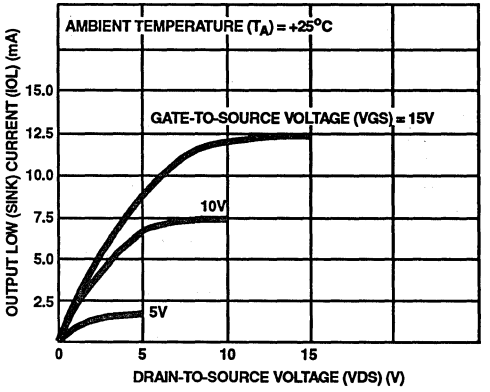


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

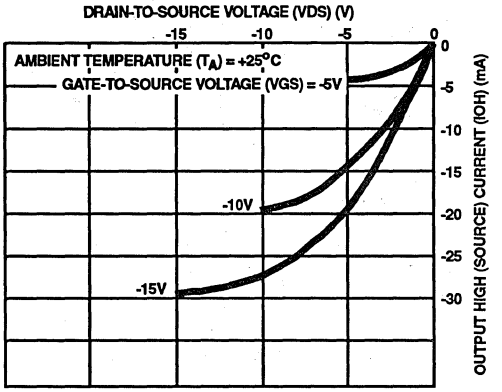


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

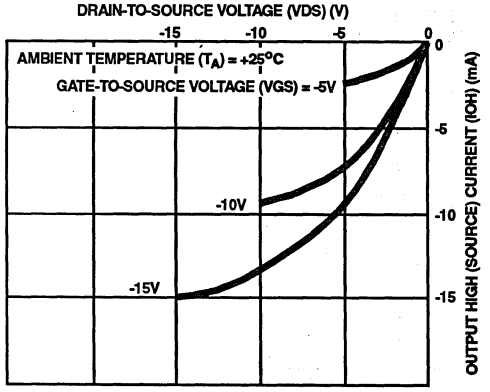


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

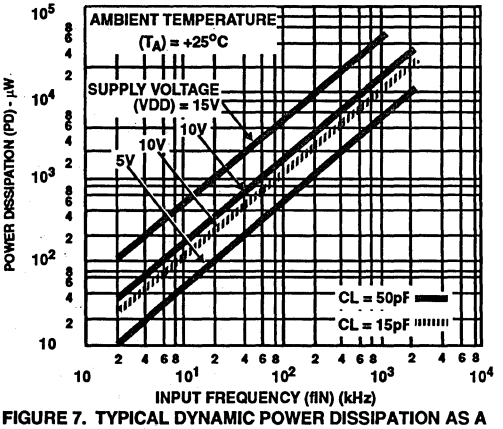


FIGURE 7. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF FREQUENCY

Typical Performance Characteristics (Continued)

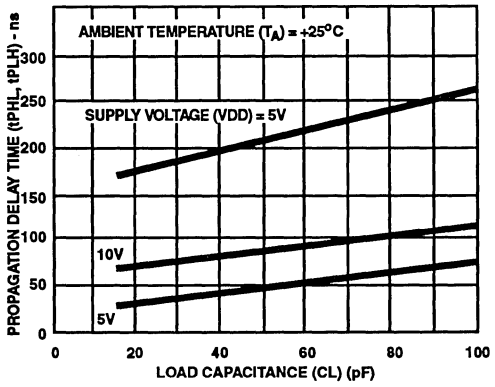
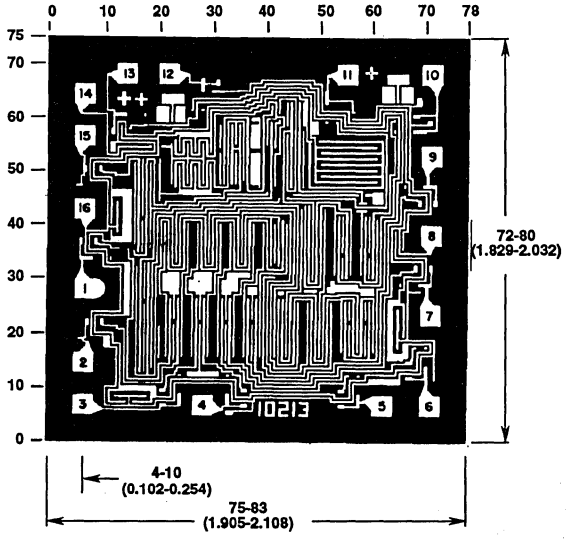


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE ("A" SELECT TO OUTPUT)

Chip Dimensions and Pad Layouts



Dimensions in parentheses are in milimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch.)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4514BMS
CD4515BMS

CMOS 4-Bit Latch/4-to-16 Line Decoders

December 1992

Features

- High-Voltage Types (20-Volt Rating)
- CD4514BMS Output "High" on Select
- CD4515BMS Output "Low" on Select
- Strobed Input Latch
- Inhibit Control
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and 25°C
- Noise Margin (Full Package-Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- 5V, 10V, and 15V Parametric Ratings
- Standardized, Symmetrical Output Characteristics
- Meets all Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Digital Multiplexing
- Address Decoding
- Hexadecimal/BCD Decoding
- Program-counter Decoding
- Control Decoder

Description

CD4514BMS and CD4515BMS consist of a 4-bit strobed latch and a 4-to-16-line decoder. The latches hold the last input data presented prior to the strobe transition from 1 to 0. Inhibit control allows all outputs to be placed at 0(CD4514BMS) or 1(CD4515BMS) regardless of the state of the data or strobe inputs.

The decode truth table indicates all combinations of data inputs and appropriate selected outputs.

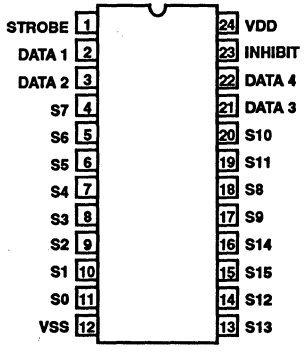
These devices are similar to industry types MC14514 and MC14515.

The CD4514BMS and CD4515BMS are supplied in these 24 lead outline packages:

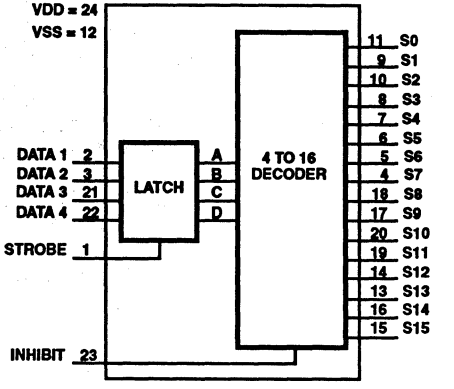
Braze Seal DIP	H4V
Frit Seal DIP	H1Z
Ceramic Flatpack	H4P

Pinout

CD4514BMS, CD4515BMS
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3195

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

7 LOGIC

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Strobe or Data	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	970	ns
			10, 11	+125°C, -55°C	-	1310	ns
Propagation Delay Inhibit	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Strobe or Datat	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	370	ns
		VDD = 15V	1, 2, 3	+25°C	-	270	ns
Propagation Delay Inhibit	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	220	ns
		VDD = 15V	1, 2, 3	+25°C	-	170	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Minimum Data Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	150	ns
		VDD = 10V	1, 2, 3	+25°C	-	70	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Minimum Strobe Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	250	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	75	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

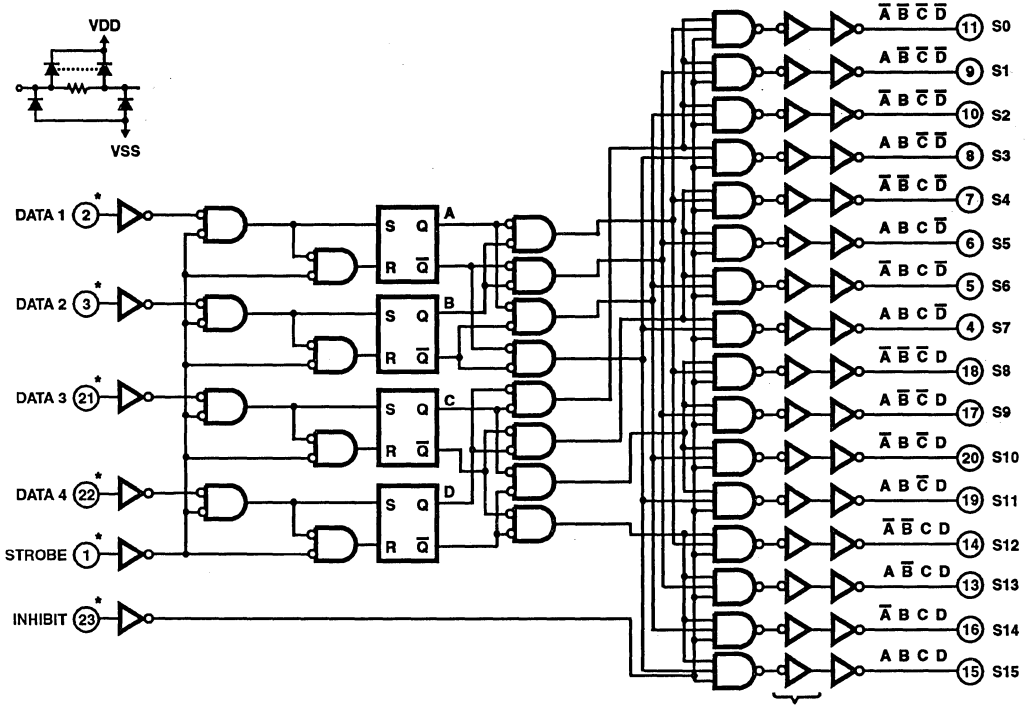
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	4-11, 13-20	1-3, 12, 21-23	24			
Static Burn-In 2 (Note 1)	4-11, 13-20	12	1-3, 21-24			
Dynamic Burn-In (Note 1)	-	2, 3, 12	21, 22, 24	4-11, 13-20	1	23
Irradiation (Note 2)						

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram



* All inputs protected by CMOS protection network.

FIGURE 1. LOGIC DIAGRAM

TRUTH TABLE

INHIBIT	DECODER INPUTS D	C	B	A	SELECTED OUTPUT CD4514BMS = LOGIC 1 (HIGH) CD4515BMS = LOGIC 0 (LOW)
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, CD4514BMS All Outputs = 1, CD4515BMS

1 = HIGH LEVEL 0 = LOW LEVEL X = DON'T CARE

Typical Performance Characteristics

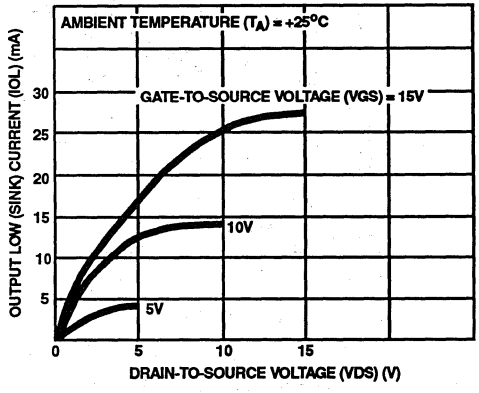


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

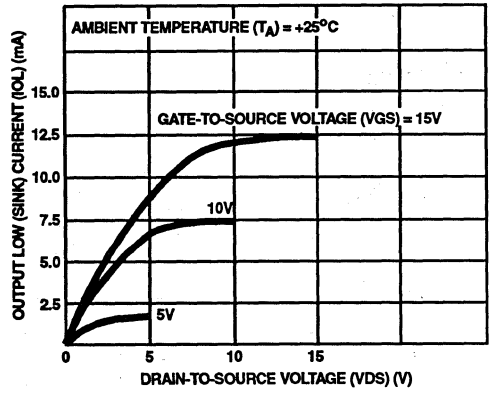


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

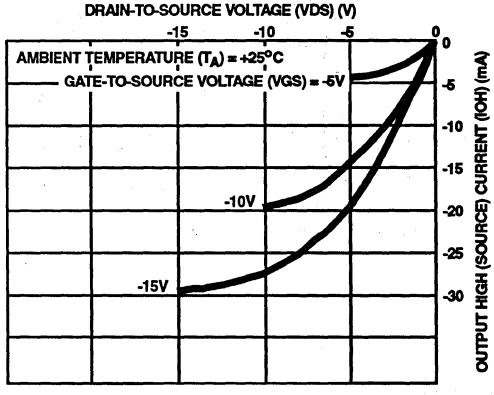


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

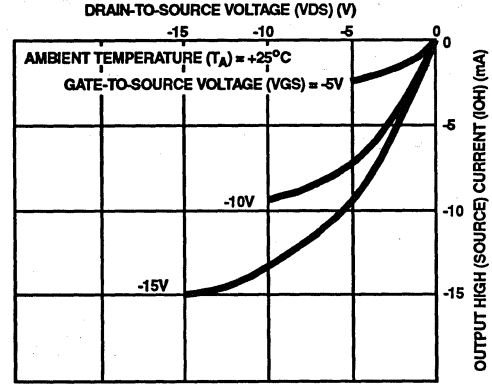


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

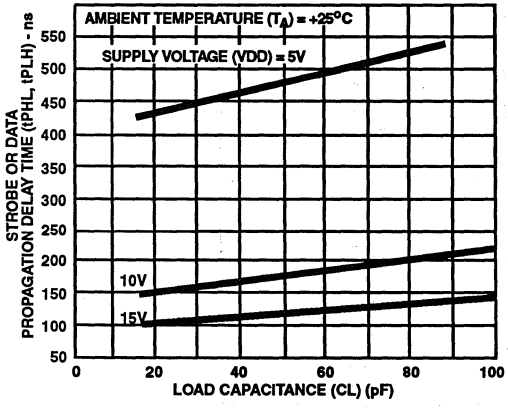


FIGURE 6. TYPICAL STROBE OR DATA PROPAGATION DELAY TIME vs LOAD CAPACITANCE

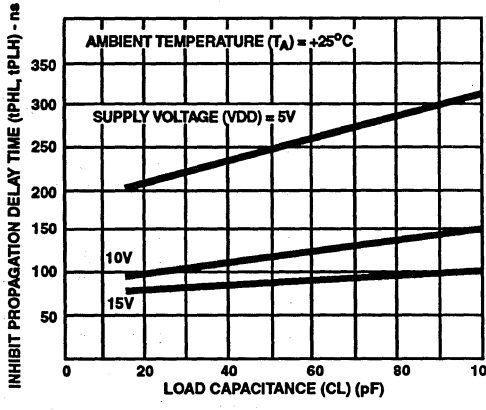


FIGURE 7. TYPICAL INHIBIT PROPAGATION DELAY TIME vs LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

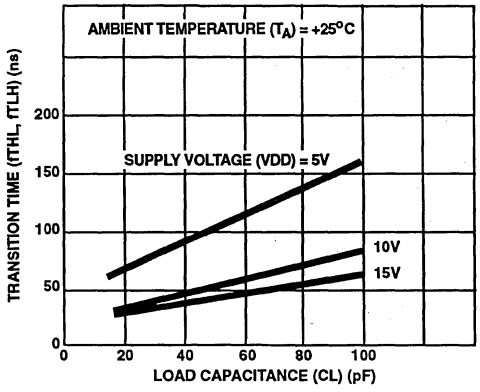


FIGURE 8. TYPICAL LOW-TO-HIGH TRANSITION TIME vs LOAD CAPACITANCE

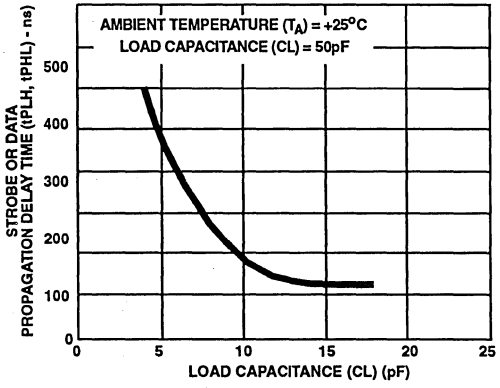
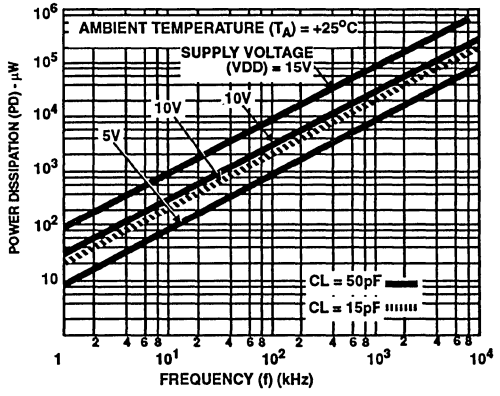


FIGURE 9. TYPICAL STROBE OR DATA PROPAGATION DELAY TIME vs SUPPLY VOLTAGE



10. TYPICAL POWER DISSIPATION vs FREQUENCY

Waveforms

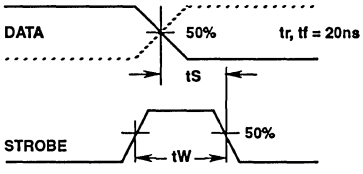
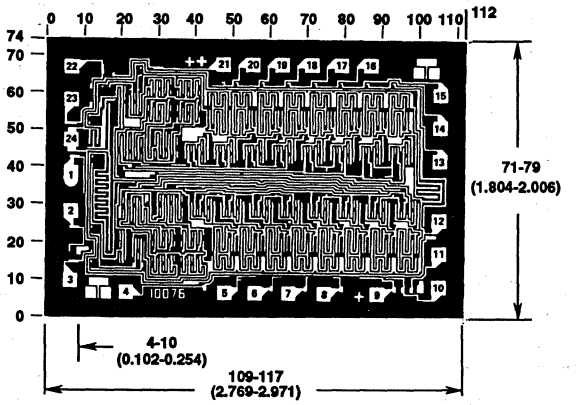


FIGURE 11. WAVEFORMS FOR SETUP TIME AND STROBE PULSE WIDTH

7 LOGIC

Chip Dimensions and Pad Layouts



Dimensions in parentheses are in milimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch.)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4517BMS

CMOS Dual 64-Stage Static Shift Register

December 1992

Features

- High-Voltage Types (20-Volt Rating)
- Low Quiescent Current - 10nA/pkg (Typ.) at VDD = 5V
- Clock Frequency 12MHz (Typ.) at VDD = 10V
- Schmitt Trigger Clock Inputs Allow Operation with Very Slow Clock Rise and Fall Times
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load, or Two HTL Loads
- 3-State Outputs
- 100% Tested for Quiescent Current at 20V
- Standardized, Symmetrical Output Characteristics
- 5V, 10V, and 15V Parametric Ratings
- Meets all Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Time-delay Circuits
- Scratch-pad Memories
- General-purpose Serial Shift-register Applications

Description

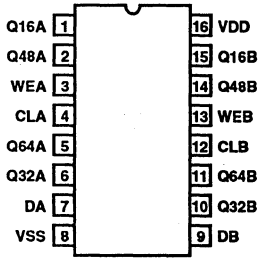
CD4517BMS dual 64-stage static shift register consists of two independent registers each having a clock, data, and write enable input and outputs accessible at taps following the 16th, 32rd, 48th, and 64th stages. These taps also serve as input points allowing data to be inputted at the 17th, 33rd, and 49th stages when the write enable input is a logic 1 and the clock goes through a low-to-high transition. The truth table indicates how the clock and write enable inputs control the opeation of the CD4517BMS. Inputs at the intermediate taps allow entry of 64 bits into the register with 16 clock pulses. The 3-state outputs permit connection of this device to an external bus.

The CD4517BMS is supplied in these 16 lead outline packages:

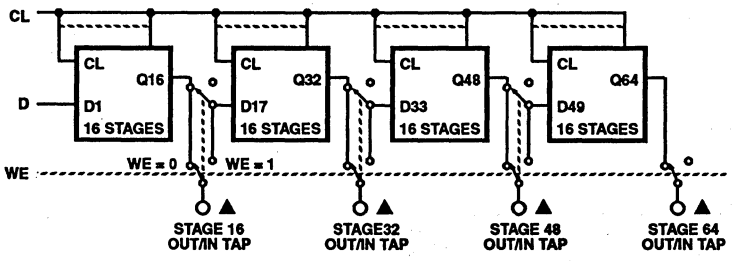
Braze Seal DIP	H4X
Frit Seal DIP	H1F
Ceramic Flatpack	H6P

Pinout

CD4517BMS
TOP VIEW



Functional Diagram



7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3341

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.4	-	µA
				2	+125°C	-12	-	µA
			VDD = 18V	3	-55°C	-0.4	-	µA
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.4	µA
				2	+125°C	-	12	µA
			VDD = 18V	3	-55°C	-	0.4	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (Note 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to 16	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	3	-	MHz
			10, 11	+125°C, -55°C	2.22	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Q16	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	220	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns
Propagation Delay 3-State WE to Q16	TPHZ, ZH TPLZ, ZL	VDD = 5V	1, 2, 5	+25°C	-	150	ns
		VDD = 10V	1, 2, 4	+25°C	-	80	ns
		VDD = 15V	1, 2, 4	+25°C	-	60	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2	+25°C	6	-	MHz
		VDD = 15V	1, 2	+25°C	8	-	MHz
Minimum Data to Clock Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	20	ns
		VDD = 10V	1, 2, 3	+25°C	-	10	ns
		VDD = 15V	1, 2, 3	+25°C	-	10	ns
Minimum Data to Clock Hold Time	TH	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	180	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Write Enable - to-Clock Release Time	TR	VDD = 5V	1, 2, 3	+25°C	-	100	ns
		VDD = 10V	1, 2, 3	+25°C	-	50	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Write Enable-to-Clock Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	0	-	ns
		VDD = 10V	1, 2, 3	+25°C	0	-	ns
		VDD = 15V	1, 2, 3	+25°C	0	-	ns
Maximum Clock Input Rise and Fall Time	TRCL TFCL	VDD = 5V	1, 2, 3, 5	+25°C	-	15	µs
		VDD = 10V	1, 2, 3, 5	+25°C	-	5	µs
		VDD = 15V	1, 2, 3, 5	+25°C	-	5	µs
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. Measured at the point of 10% change in output with an output load 50pF, RL = 1KΩ to VDD for TPZL and TPLZ and RL = 1KΩ to VSS for TPZH and TPHZ
5. If more than one unit is cascaded, TRCL should be made less than or equal to the sumof the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0μA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	1, 2, 5, 6, 10, 11, 14, 15	3, 4, 7-9, 12, 13	16			
Static Burn-In 2 (Note 1)	1, 2, 5, 6, 10, 11, 14, 15	8	3, 4, 7, 9, 12, 13, 16			
Dynamic Burn-In (Note 1)	-	3, 8, 13	16	1, 2, 5, 6, 10, 11, 14, 15	4, 12	7, 9

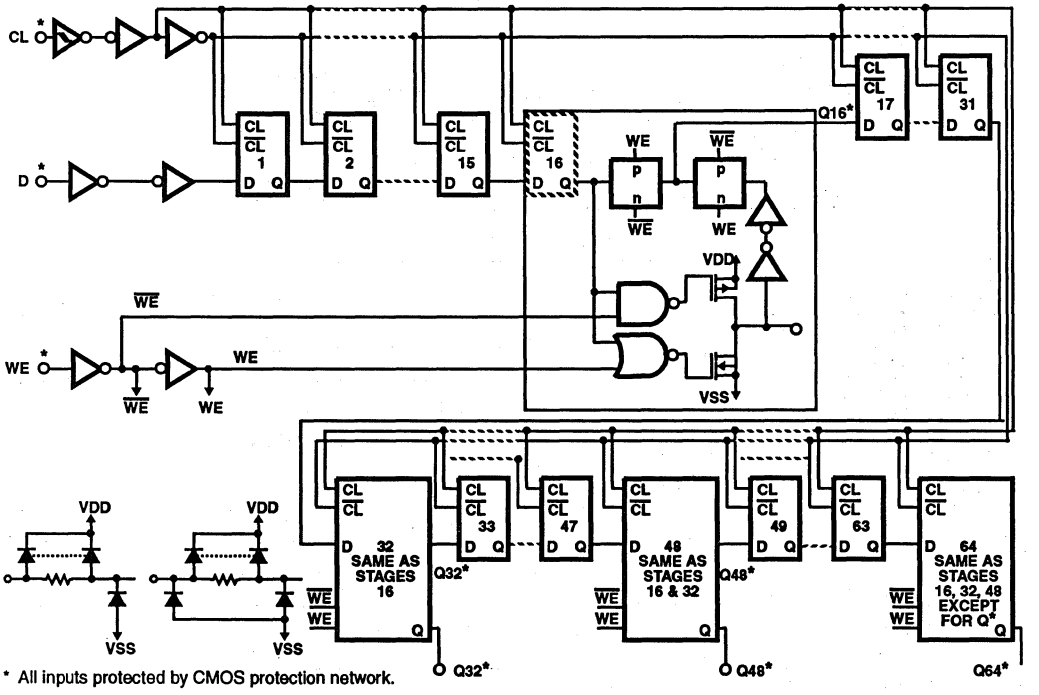
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS (Continued)

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Irradiation (Note 2)	1, 2, 5, 6, 10, 11, 14, 15	8	3, 4, 7, 9, 12, 13, 16			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram



* All inputs protected by CMOS protection network.

FIGURE 1. LOGIC BLOCK DIAGRAM

TRUTH TABLE

CLOCK	WRITE ENABLE	DATA	STAGE 16 TAP	STAGE 32 TAP	STAGE 48 TAP	STAGE 64 TAP
0	0	X	Q16	Q32	Q48	Q64
0	1	X	Z	Z	Z	Z
1	0	X	Q16	Q32	Q48	Q64
1	1	X	Z	Z	Z	Z
⎍	0	DI In	Q16	Q32	Q48	Q64
⎍	1	DI In	D17 In	D33 In	D49 In	Z
⎎	0	X	Q16	Q32	Q48	Q64
⎎	1	X	Z	Z	Z	Z

1 = HIGH LEVEL
0 = LOW LEVEL
X = DON'T CARE
Z = HIGH IMPEDANCE

Typical Performance Characteristics

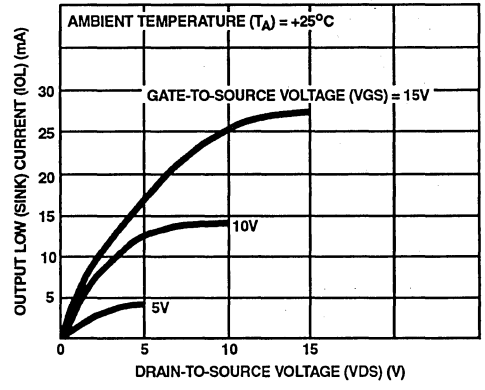


FIGURE 2. TYPICAL N-CHANNEL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

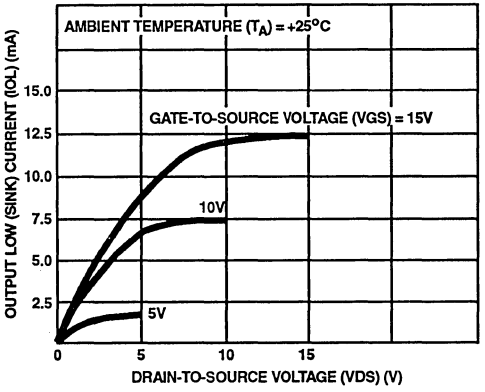


FIGURE 3. MINIMUM N-CHANNEL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

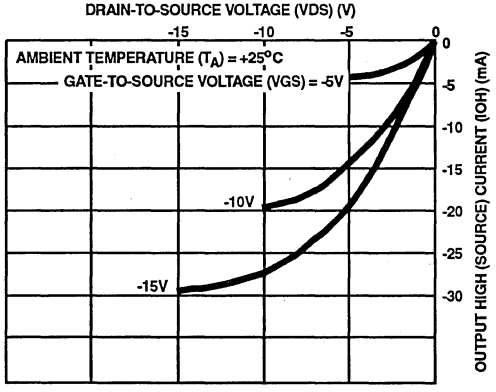


FIGURE 4. TYPICAL P-CHANNEL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

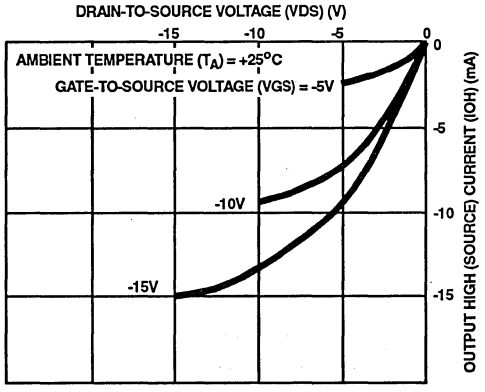


FIGURE 5. MINIMUM P-CHANNEL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

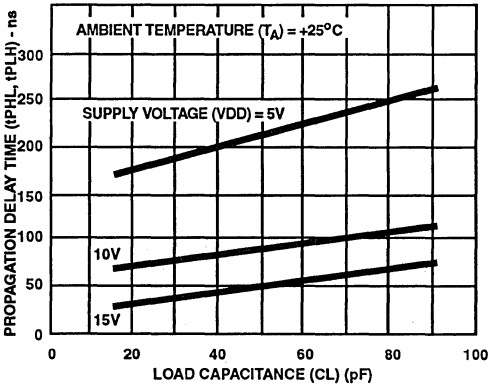


FIGURE 6. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

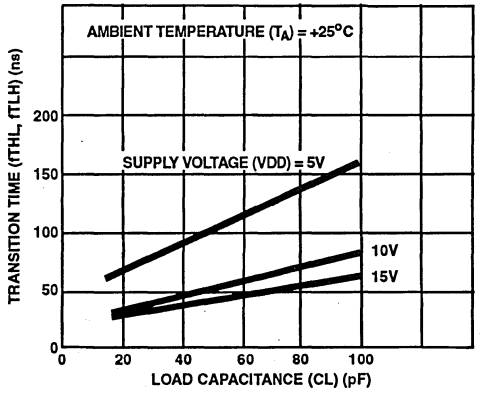


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

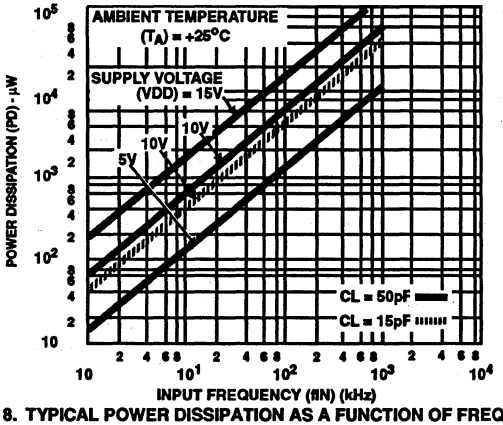
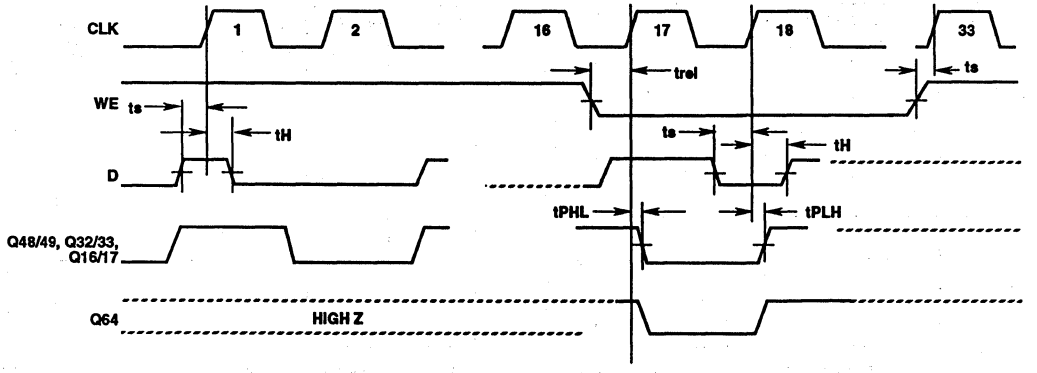


FIGURE 8. TYPICAL POWER DISSIPATION AS A FUNCTION OF FREQUENCY

Waveforms and Test Circuits



FIIGURE 9. DYNAMIC TEST WAVEFORMS

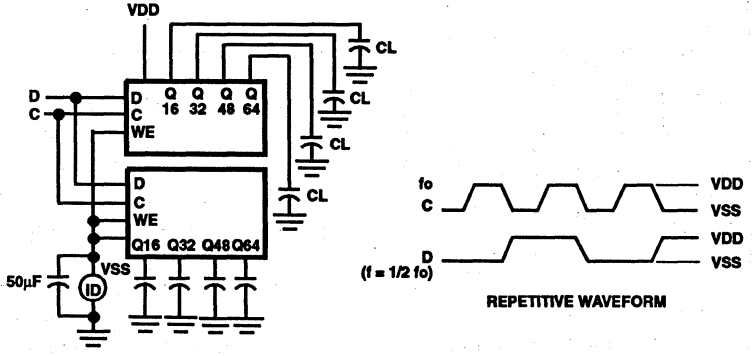
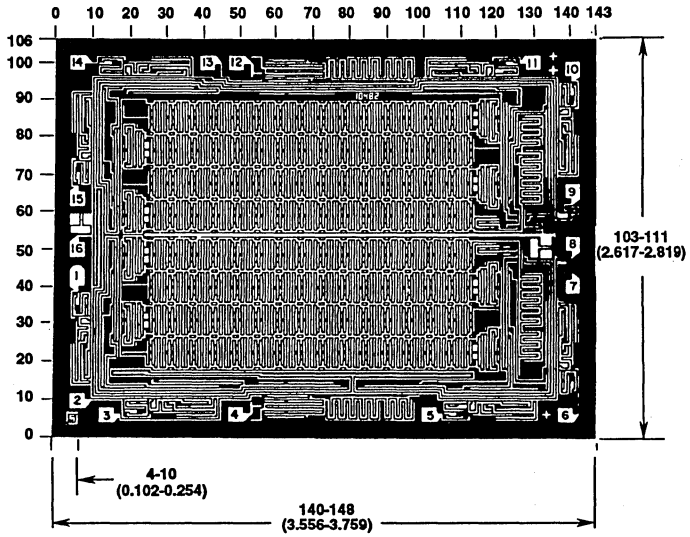


FIGURE 10. DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

Chip Dimensions and Pad Layouts



Dimensions in parentheses are in milimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch.)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4518BMS
CD4520BMS

December 1992

CMOS Dual Up Counters

Features

- High Voltage Types (20V Rating)
- CD4518BMS Dual BCD Up Counter
- CD4520BMS Dual Binary Up Counter
- Medium Speed Operation
  - 6MHz Typical Clock Frequency at 10V
- Positive or Negative Edge Triggering
- Synchronous Internal Carry Propagation
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Standardized Symmetrical Output Characteristics
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Multistage Synchronous Counting
- Multistage Ripple Counting
- Frequency Dividers

Description

CD4518BMS Dual BCD Up Counter and CD4520BMS Dual Binary Up Counter each consist of two identical, internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable CLOCK and ENABLE lines for incrementing on either the positive-going or negative-going transition. For single unit operation the ENABLE input is maintained high and the counter advances on each positive-going transition of the CLOCK. The counters are cleared by high levels on their RESET lines.

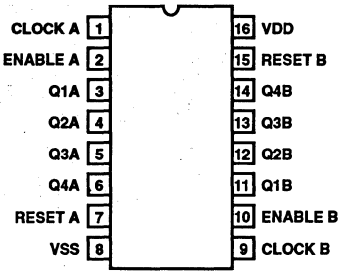
The counter can be cascaded in the ripple mode by connecting Q4 to the enable input of the subsequent counter while the CLOCK input of the latter is held low.

The CD4518BMS and CD4520BMS are supplied in these 16-lead outline packages:

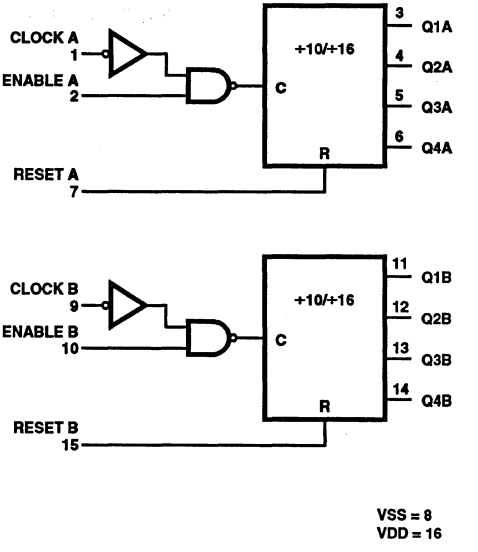
Braze Seal DIP	H4S
Frit Seal DIP	H1F
Ceramic Flatpack	*H6P †H6W
*CD4518B Only	†CD4520B Only

Pinout

CD4518BMS, CD4520BMS
TOP VIEW



Functional Diagram



File Number 3342

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Output	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	560	ns
			10, 11	+125°C, -55°C	-	756	ns
Propagation Delay Reset to Ouput	TPHL2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	650	ns
			10, 11	+125°C, -55°C	-	878	ns
Transition Time (Note 2)	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	1.5	-	MHz
			10, 11	+125°C, -55°C	1.11	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Output	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	230	ns
		VDD = 15V	1, 2, 3	+25°C	-	160	ns
Propagation Delay Reset to Output	TPHL2	VDD = 10V	1, 2, 3	+25°C	-	225	ns
		VDD = 15V	1, 2, 3	+25°C	-	170	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	3	-	MHz
		VDD = 15V	1, 2, 3	+25°C	4	-	MHz
Maximum Clock Rise and Fall Time	TRCL TFCL	VDD = 5V	1, 2, 3, 4	+25°C	-	15	µs
		VDD = 10V	1, 2, 3, 4	+25°C	-	5	µs
		VDD = 15V	1, 2, 3, 4	+25°C	-	5	µs
Minimum Enable Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	400	ns
		VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	140	ns
Minimum Reset Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	250	ns
		VDD = 10V	1, 2, 3	+25°C	-	110	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	70	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. If more than one unit is cascaded, TRCL should be made less than or equal to the sumof the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	3-6, 11-14	1, 2, 7-10, 15	16			
Static Burn-In 2 Note 1	3-6, 11-14	8	1, 2, 7, 9, 10, 15, 16			
Dynamic Burn-In Note 1	-	7, 8, 15	2, 10, 16	3-6, 11-14	1, 9	
Irradiation Note 2	3-6, 11-14	8	1, 2, 7, 9, 10, 15, 16			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagrams

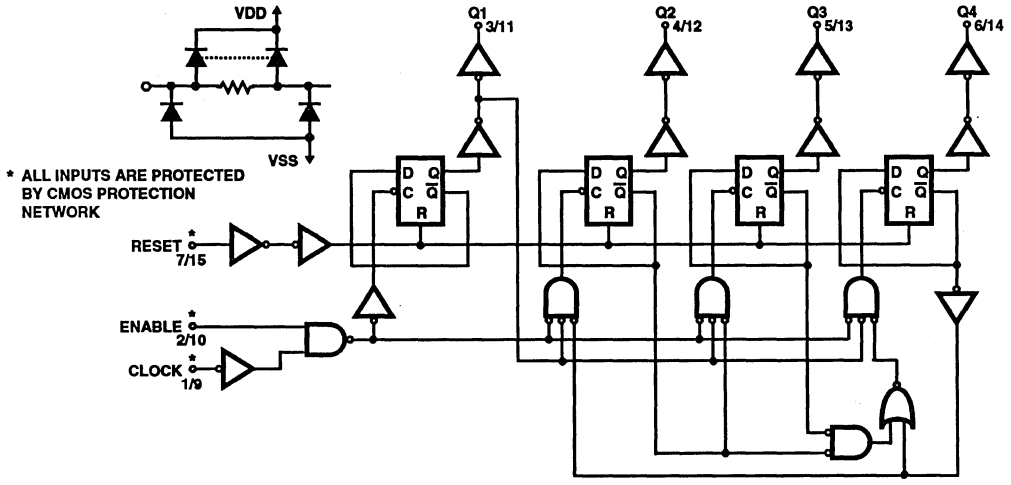


FIGURE 1. DECADE COUNTER (CD4518BMS) LOGIC DIAGRAM FOR ONE OF TWO IDENTICAL COUNTERS

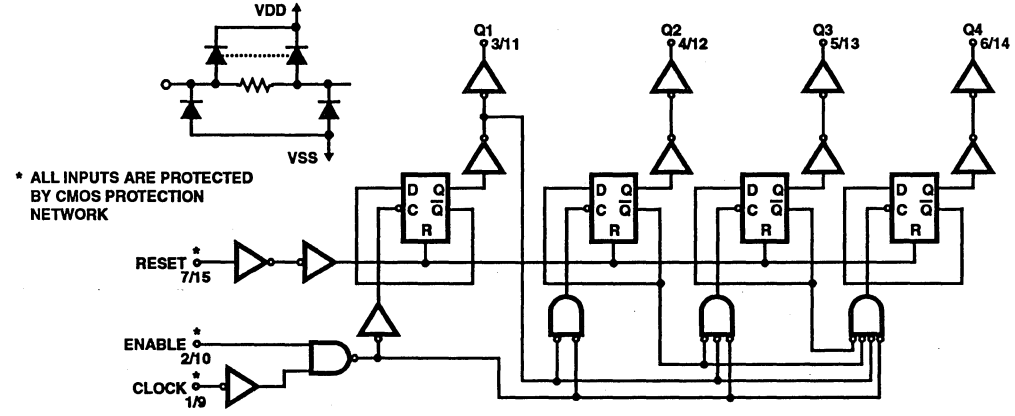


FIGURE 2. BINARY COUNTER (CD4520BMS) LOGIC DIAGRAM FOR ONE OF TWO IDENTICAL COUNTERS

TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
⌐	1	0	Increment Counter
0	¬	0	Increment Counter
¬	X	0	No Change
X	⌐	0	No Change
⌐	0	0	No Change
1	¬	0	No Change
X	X	1	Q1 thru Q4 = 0

X = Don't Care 1 ≡ High State 0 ≡ Low State

Typical Performance Curves

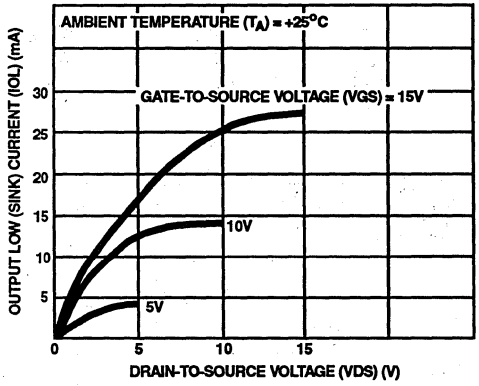


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

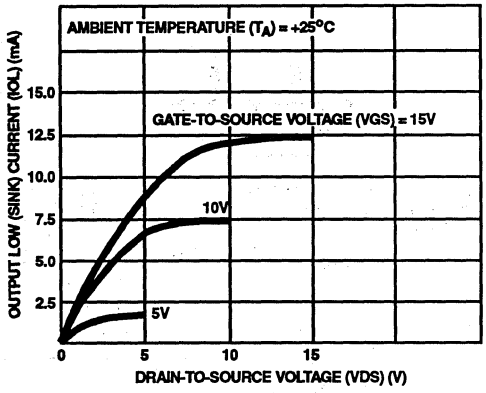


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

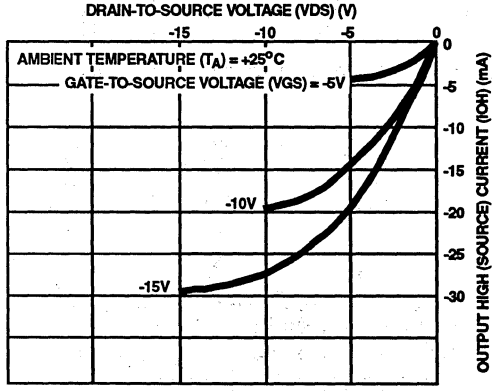


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

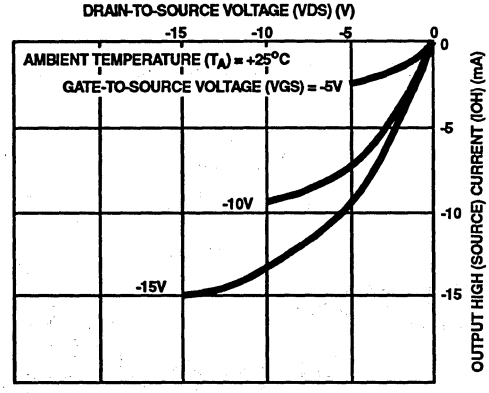


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

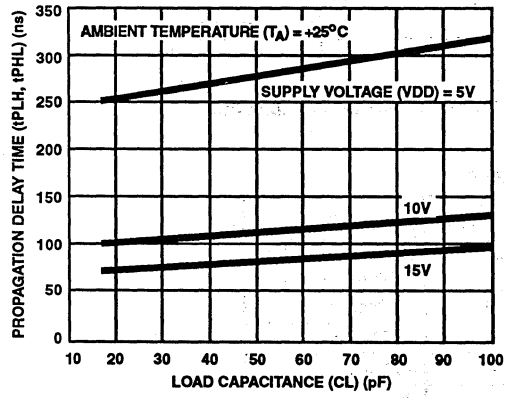


FIGURE 7. TYPICAL PROPAGATION DELAY vs LOAD CAPACITANCE, CLOCK OR ENABLE TO OUTPUT

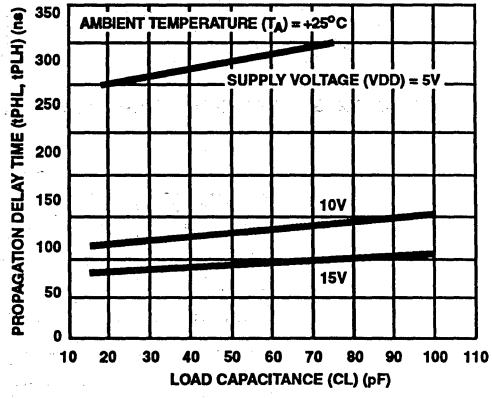


FIGURE 8. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE, RESET TO OUTPUT

Typical Performance Curves

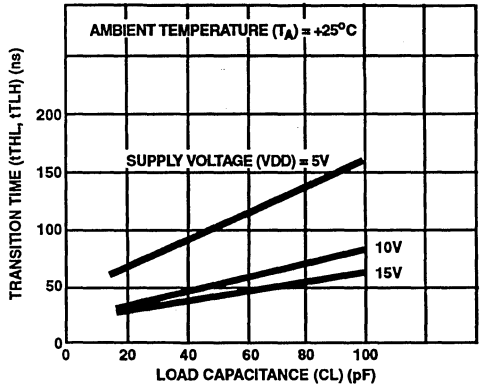


FIGURE 9. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

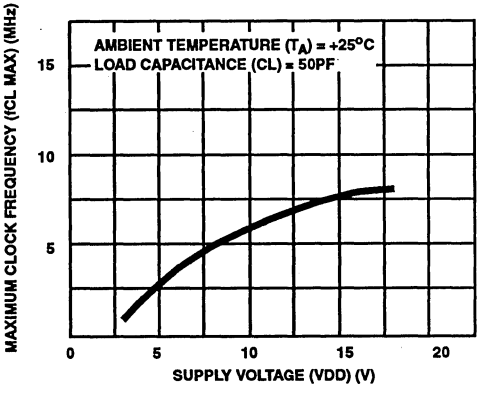


FIGURE 10. TYPICAL MAXIMUM CLOCK FREQUENCY vs SUPPLY VOLTAGE

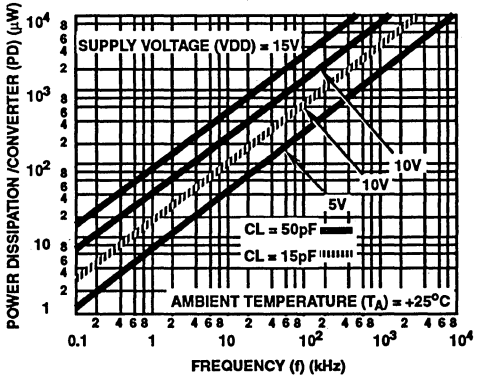


FIGURE 11. TYPICAL POWER DISSIPATION CHARACTERISTICS

Timing Diagrams

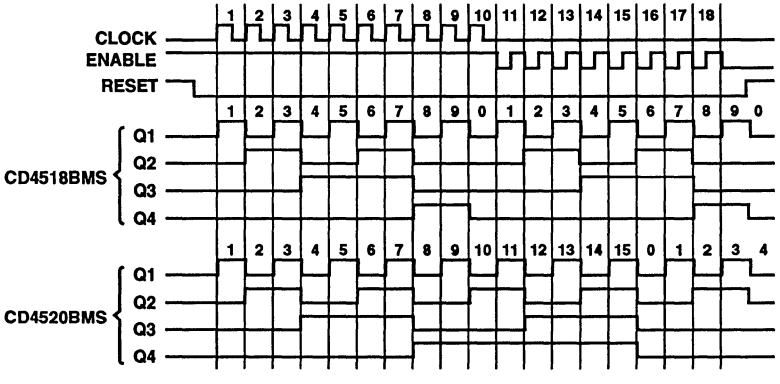


FIGURE 12. TIMING DIAGRAMS FOR CD4518BMS AND CD4520BMS

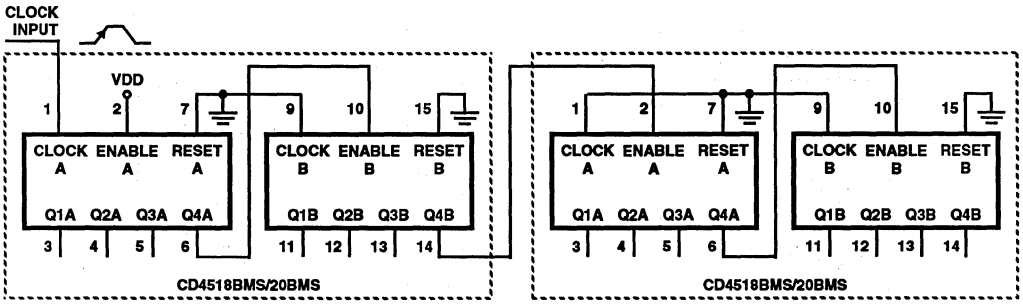
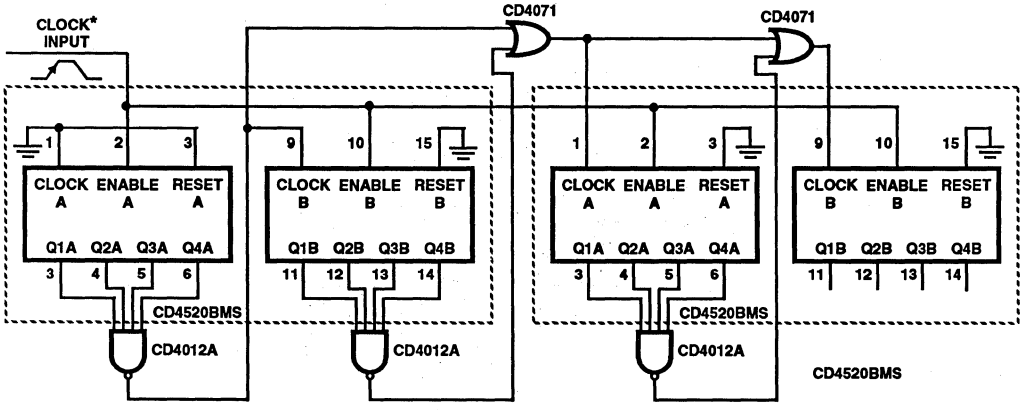


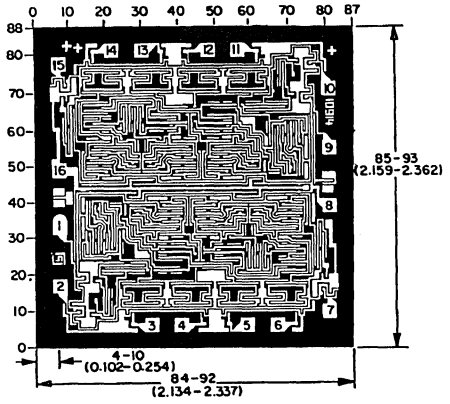
FIGURE 13. RIPPLE CASCADING OF FOUR COUNTERS WITH POSITIVE EDGE TRIGGERING



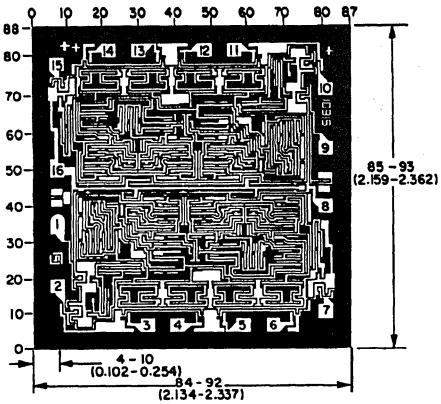
* For synchronous cascading, the clock transition time should be made less than or equal to the sum of the fixed propagation delay at 15pF and the transition time of the output driver stage for the estimated capacitive load.

FIGURE 14. SYNCHRONOUS CASCADING OF FOUR BINARY COUNTERS WITH NEGATIVE EDGE TRIGGERING

Chip Dimensions and Pad Layouts



CD4518BMS



CD4520BMS

Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10-3 inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4527BMS

CMOS BCD Rate Multiplier

December 1992

Features

- High Voltage Type (20V Rating)
- Cascadable in Multiples of 4-Bits
- Set to "9" Input and "9" Detect Output
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Standardized Symmetrical Output Characteristics
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Numerical Control
- Instrumentation
- Digital Filtering
- Frequency Synthesis

Description

CD4527BMS is a low power 4-bit digital rate multiplier that provides an output pulse rate which is the clock input pulse rate multiplied by 1/10 times the BCD input. For example, when the BCD input is 8, there will be 8 output pulses for every 10 input pulses. This device may be used to perform arithmetic operations (add, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigonometric functions, A/D and D/A conversion, and frequency division.

For fractional multipliers with more than one digit, CD4527BMS devices may be cascaded in two different modes: the Add mode and the Multiply mode (see Figures 9 and 11). In the Add mode,

Output Rate =
(Clock Rate) [0.1BCD1 + 0.01BCD2 + 0.001BCD3 + . . .]

In the Multiply mode, the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second one,

$$\text{e.g. } \frac{9}{10} \times \frac{4}{10} = \frac{36}{100} \text{ or 36 output}$$

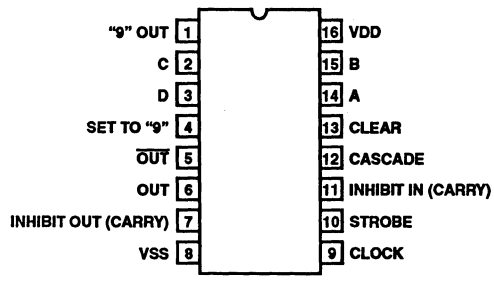
pulses for every 100 clock input pulses.

The CD4527BMS is supplied in these 16-lead outline packages:

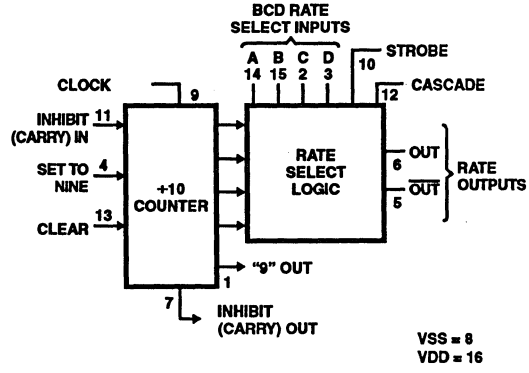
Braze Seal DIP	H4X
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

Pinout

CD4527BMS
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3343

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range.....-55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG).....-65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K).....500mW
For T_A = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature .....+175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Output	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	300	ns
			10, 11	+125°C, -55°C	-	405	ns
Propagation Delay Clear to Output	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	760	ns
			10, 11	+125°C, -55°C	-	1026	ns
Propagation Delay Cascade to Output	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	180	ns
			10, 11	+125°C, -55°C	-	243	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	1.2	-	MHz
			10, 11	+125°C, -55°C	.89	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Clock to Output	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	150	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Propagation Delay Clear to Output	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	350	ns
		VDD = 15V	1, 2, 3	+25°C	-	260	ns
Propagation Delay Cascade to Output	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25°C	-	90	ns
		VDD = 15V	1, 2, 3	+25°C	-	70	ns
Propagation Delay Clock to $\overline{Out}$	TPHL TPLH	VDD = 5V	1, 2, 3	+25°C	-	220	ns
		VDD = 10V	1, 2, 3	+25°C	-	110	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns
Propagation Delay Clock to INHIBIT Out	TPHL	VDD = 5V	1, 2, 3	+25°C	-	640	ns
		VDD = 10V	1, 2, 3	+25°C	-	290	ns
		VDD = 15V	1, 2, 3	+25°C	-	200	ns
Propagation Delay Clock to INHIBIT Out	TPLH	VDD = 5V	1, 2, 3	+25°C	-	500	ns
		VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	150	ns
Propagation Delay INHIBIT IN to INHIBIT Out	TPHL TPLH	VDD = 5V	1, 2, 3	+25°C	-	260	ns
		VDD = 10V	1, 2, 3	+25°C	-	120	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns
Propagation Delay Clock to "9" or "15" Out	TPHL TPLH	VDD = 5V	1, 2, 3	+25°C	-	600	ns
		VDD = 10V	1, 2, 3	+25°C	-	250	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns
Propagation Delay Set to Out	TPHL TPLH	VDD = 5V	1, 2, 3	+25°C	-	660	ns
		VDD = 10V	1, 2, 3	+25°C	-	300	ns
		VDD = 15V	1, 2, 3	+25°C	-	220	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2	+25°C	2.5	-	MHz
		VDD = 15V	1, 2	+25°C	3.5	-	MHz
Minimum Data Setup Time - Inhibit	TS	VDD = 5V	1, 2, 3	+25°C	-	100	ns
		VDD = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V	1, 2, 3	+25°C	-	20	ns
Minimum Inhibit Removal Time	TREM	VDD = 5V	1, 2, 3	+25°C	-	240	ns
		VDD = 10V	1, 2, 3	+25°C	-	130	ns
		VDD = 15V	1, 2, 3	+25°C	-	110	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	330	ns
		VDD = 10V	1, 2, 3	+25°C	-	170	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Maximum Clock Rise and Fall Time	TRCL TFCL	VDD = 5V	1, 2, 3, 4	+25°C	-	15	µs
		VDD = 10V	1, 2, 3, 4	+25°C	-	15	µs
		VDD = 15V	1, 2, 3, 4	+25°C	-	15	µs

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Minimum Clear Removal Time	TREM	VDD = 5V	1, 2, 3	+25°C	-	60	ns
		VDD = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V	1, 2, 3	+25°C	-	30	ns
Minimum Set Removal Time	TREM	VDD = 5V	1, 2, 3	+25°C	-	150	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Set or Clear Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	160	ns
		VDD = 10V	1, 2, 3	+25°C	-	90	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. If more than one unit is cascaded, TRCL should be made less than or equal to the sumof the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	1, 5-7	2-4, 8-15	16			
Static Burn-In 2 Note 1	1, 5-7	8	2-4, 9-16			
Dynamic Burn-In Note 1	-	2, 4, 8, 10, 12-15	3, 16	1, 5-7	9	11
Irradiation Note 2	1, 5-7	8	2-4, 9-16			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram

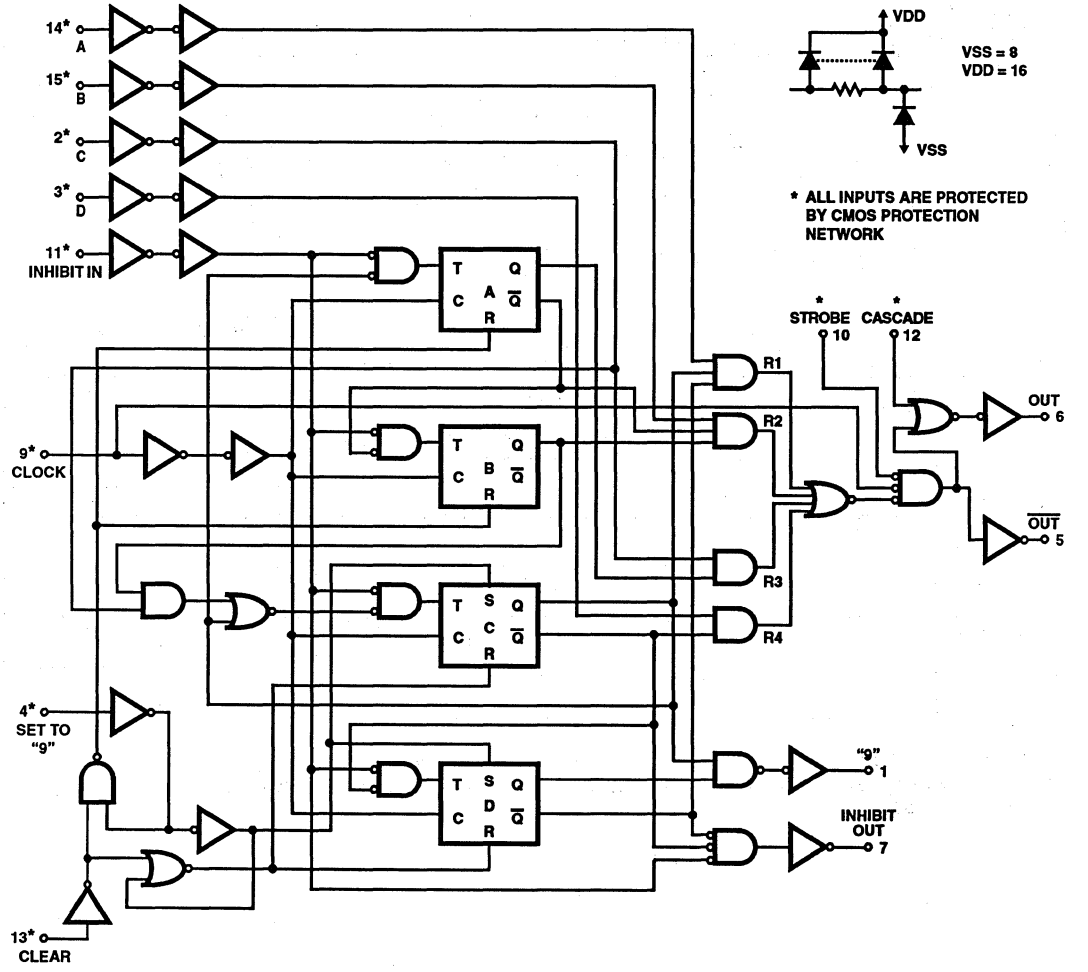


FIGURE 1.

TRUTH TABLE

INPUTS										OUTPUTS			
NUMBER OF PULSES OR INPUT LOGIC LEVEL (0 = Low; 1 = High; X = Don't Care)										NUMBER OF PULSES OR OUTPUT LOGIC LEVEL (L = Low; H = High)			
D	C	B	A	CLK	INH IN	STR	CAS	CLR *	SET *	OUT	$\overline{OUT}$	INH OUT	"9" OUT
0	0	0	0	10	0	0	0	0	0	L	H	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	**	**	H	**
X	X	X	X	10	0	1	0	0	0	L	H	1	1
X	X	X	X	10	0	0	1	0	0	H	***	1	1
1	X	X	X	10	0	0	0	1	0	10	10	H	L
0	X	X	X	10	0	0	0	1	0	L	H	H	L
X	X	X	X	10	0	0	0	0	1	L	H	L	H

* Clear and Set Inputs should not be high at the same time; device draws increased quiescent current when in this non-valid state.

** Depends on internal state of counter.

*** Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).

Typical Performance Characteristics

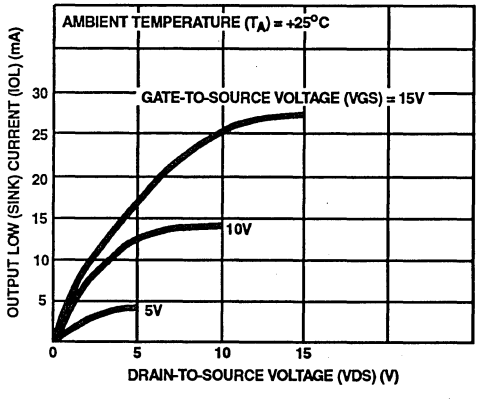


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

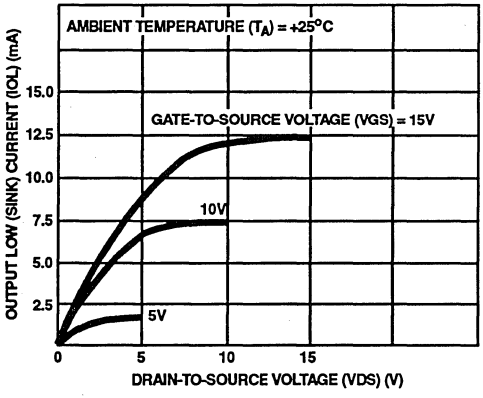


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

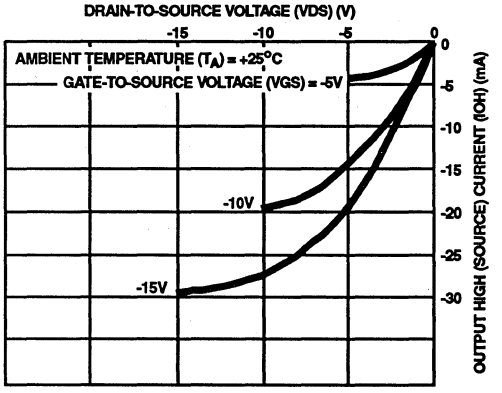


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

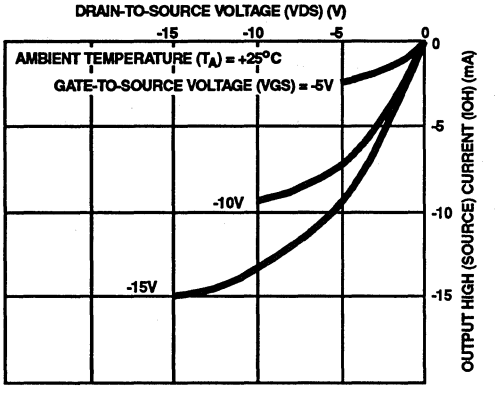


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

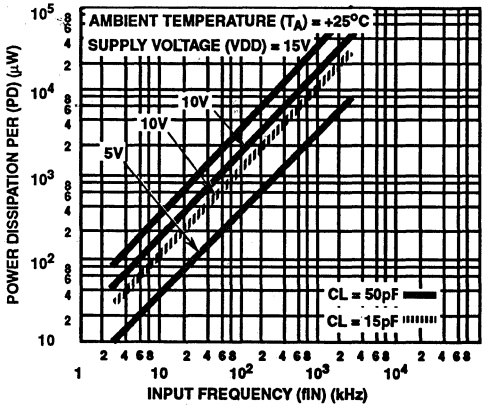


FIGURE 6. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

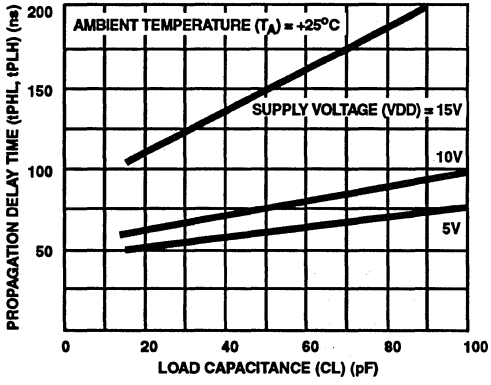


FIGURE 7. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (CLOCK OR STROBE TO OUT)

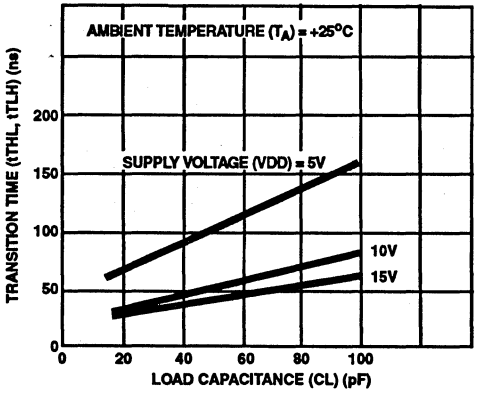


FIGURE 8. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

Applications

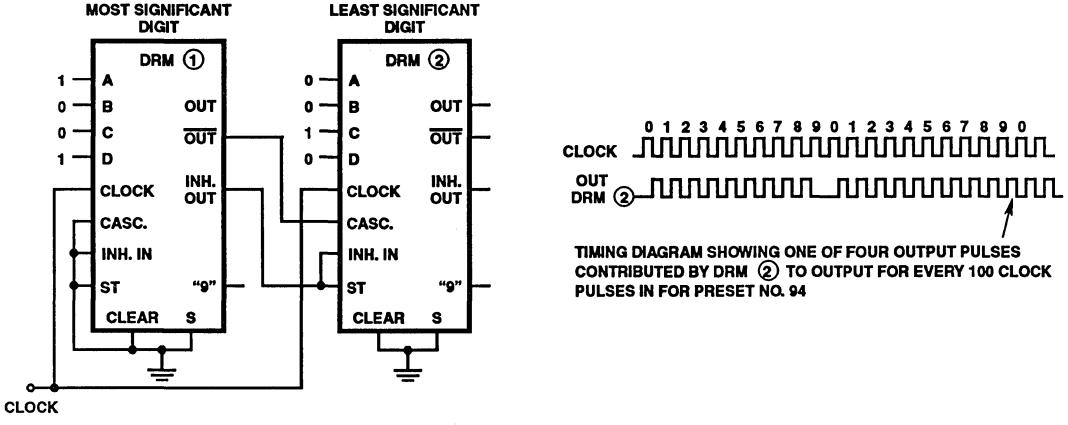


FIGURE 9. TWO CD4527BMS's CASCADED IN THE "ADD" MODE WITH A PRESET NUMBER

$$\text{OF 94}\left(\frac{9}{10}+\frac{4}{100}=\frac{94}{100}\right)$$

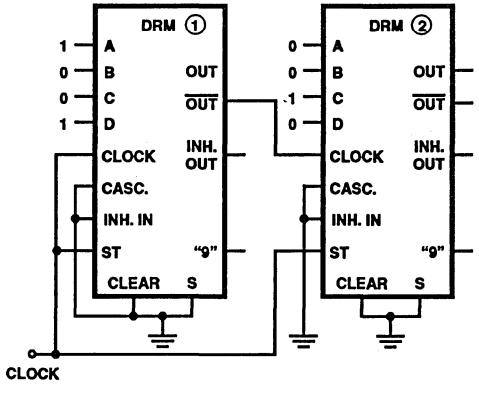


FIGURE 10. TWO CD4527BMS's CASCADED IN THE "MULTIPLY" MODE WITH A PRESET NUMBER

$$\text{OF 36}\left(\frac{9}{10}\times\frac{4}{100}=\frac{36}{100}\right)$$

Timing Diagram

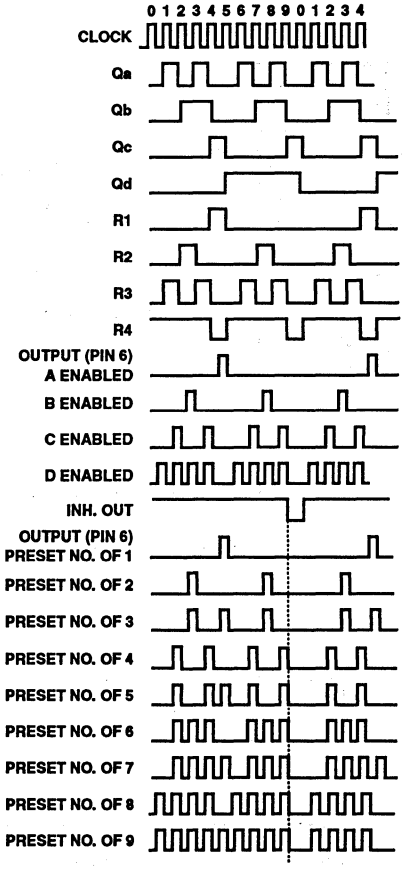
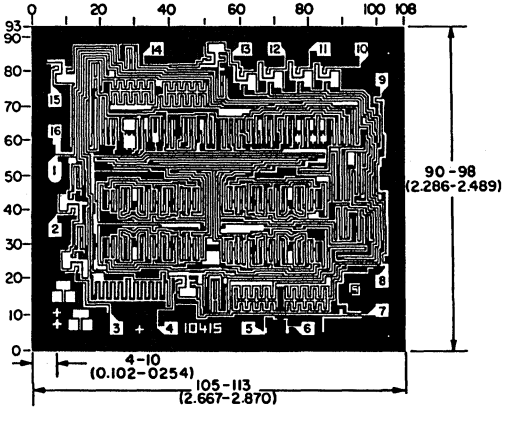


FIGURE 11. (SEE LOGIC DIAGRAM)

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

CD4532BMS

CMOS 8-Bit Priority Encoder

December 1992

Features

- High Voltage Type (20V Rating)
- Converts From 1 of 8 to Binary
- Provides Cascading Feature to Handle Any Number of Inputs
- Group Select Indicates One or More Priority Inputs
- Standardized Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 0.5V at VDD = 5V
  - 1.5V at VDD = 10V
  - 1.5V at VDD = 15V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Priority Encoder
- Binary or BCD Encoder (Keyboard Encoding)
- Floating Point Arithmetic

Description

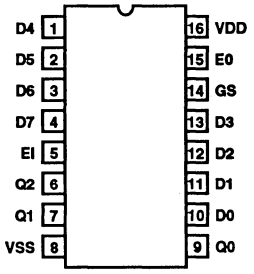
CD4532BMS consists of combinational logic that encodes the highest priority input (D7 - D0) to a 3-bit binary code. The eight inputs, D7 through D0, each have an assigned priority; D7 is the highest priority and D0 is the lowest. The priority encoder is inhibited when the chip-enable input E1 is low. When E1 is high, the binary representation of the highest-priority input appears on output lines Q2 - Q0, and the group select line GS is high to indicate that priority inputs are present. The enable-out (EO) is high when no priority inputs are present. If any one input is high, EO is low and all cascaded lower-order stages are disabled.

The CD4532BMS is supplied in these 16-lead outline packages:

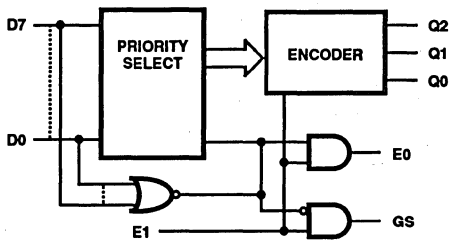
Braze Seal DIP	H4T
Frit Seal DIP	H1E
Ceramic Flatpack	H6W

Pinout

CD4532BMS
TOP VIEW



Functional Diagram



7 LOGIC

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range.....-55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG).....-65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K).....500mW
For T_A = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature .....+175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH> VDD/2	VOL< VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay E1 to E0 E1 to GS	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	220	ns
			10, 11	+125°C, -55°C	-	297	ns
Propagation Delay E1 to QM DN to GS	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	340	ns
			10, 11	+125°C, -55°C	-	459	ns
Propagation Delay DN to QM	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	440	ns
			10, 11	+125°C, -55°C	-	594	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay E1 to E0 E1 to GS	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	110	ns
		VDD = 15V	1, 2, 3	+25°C	-	85	ns
Propagation Delay E1 to QM DN to GS	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	170	ns
		VDD = 15V	1, 2, 3	+25°C	-	125	ns
Propagation Delay DN to QM	TPLH3 TPHL3	VDD = 10V	1, 2, 3	+25°C	-	220	ns
		VDD = 15V	1, 2, 3	+25°C	-	160	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	6, 7, 9, 14, 15	1 - 5, 8, 10 - 13	16			
Static Burn-In 2 (Note 1)	6, 7, 9, 14, 15	8	1 - 5, 10 - 13, 16			
Dynamic Burn-In (Note 1)	-	8	5, 16	6, 7, 9, 14, 15	1 - 4, 10 - 13	
Irradiation (Note 2)	6, 7, 9, 14, 15	8	1 - 5, 10 - 13, 16			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram

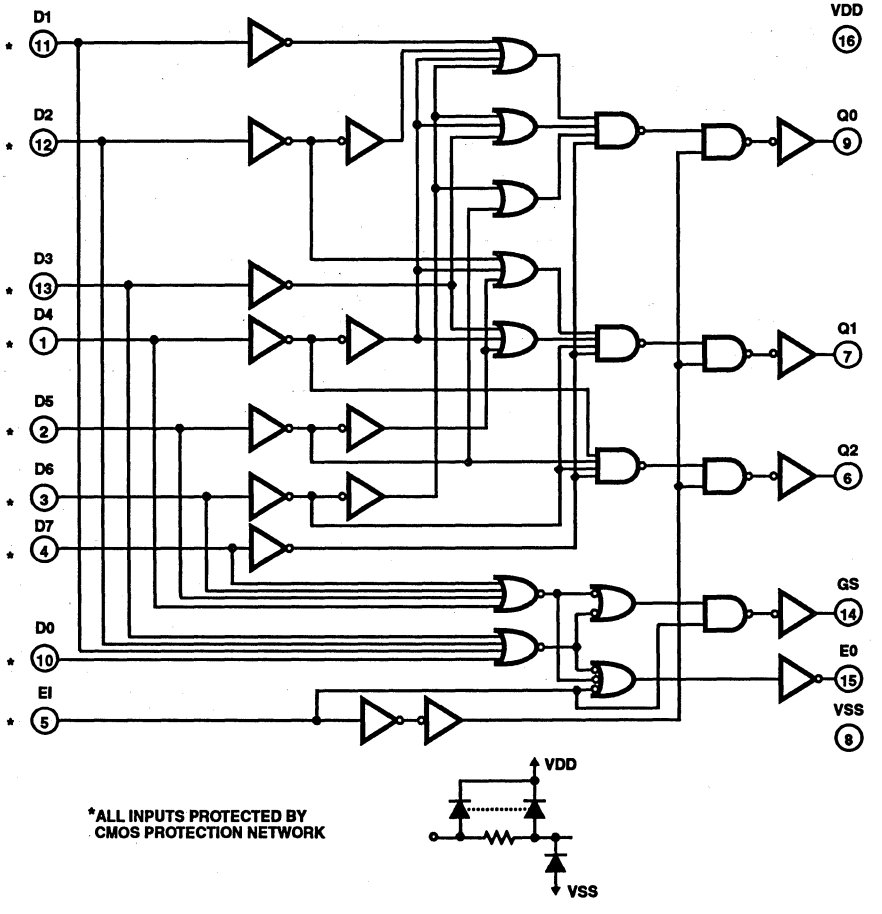


FIGURE 1. CD4532BMS LOGIC DIAGRAM

TRUTH TABLE

INPUT									OUTPUT				
E1	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E0
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care Logic 1 ≡ High Logic 0 ≡ Low

Typical Performance Characteristics

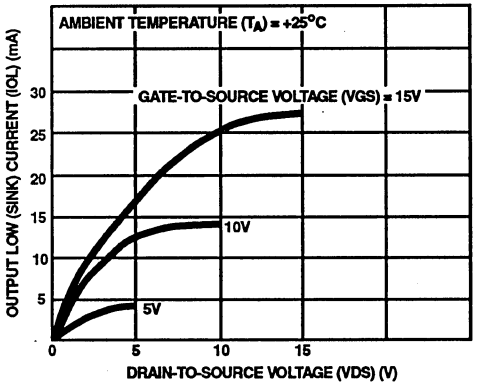


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

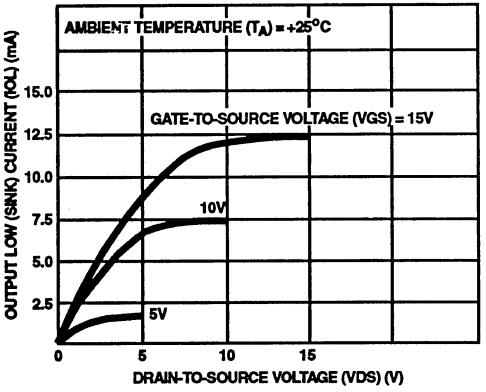


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

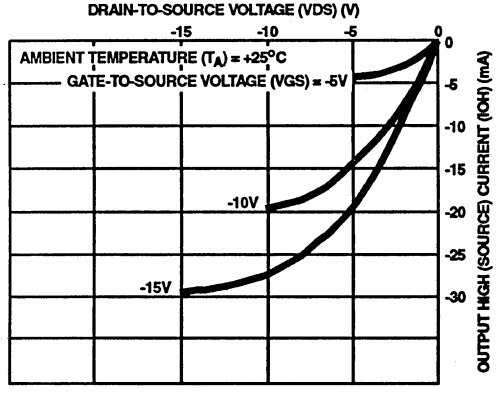


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

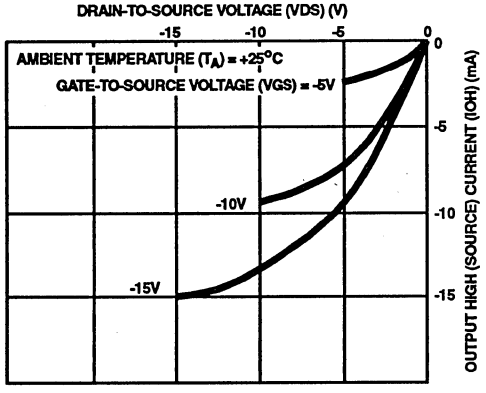


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

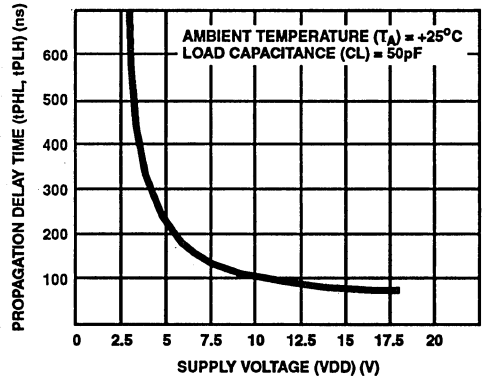


FIGURE 6. TYPICAL PROPAGATION DELAY (DN TO QM) vs SUPPLY VOLTAGE

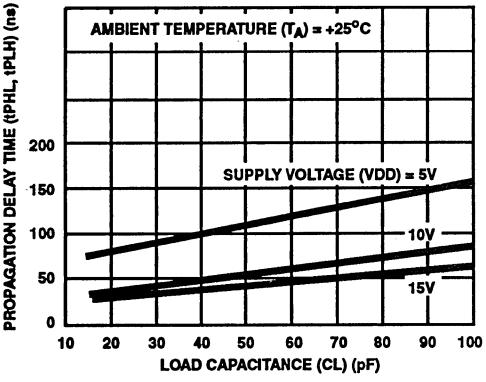


FIGURE 7. TYPICAL PROPAGATION DELAY (E1 TO GS, E1 TO EQ) vs LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

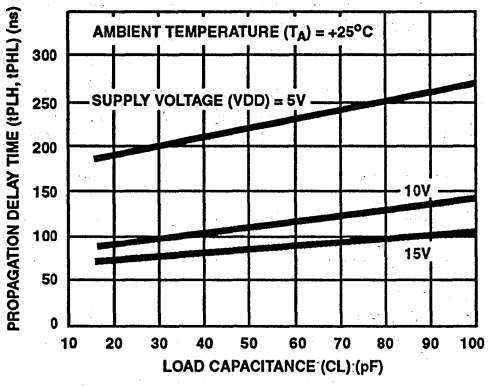


FIGURE 8. TYPICAL PROPAGATION DELAY (DN TO QM) vs LOAD CAPACITANCE

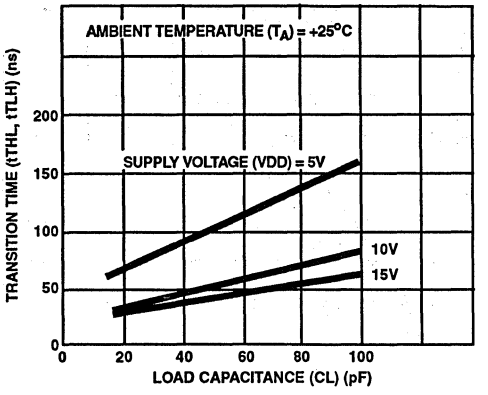


FIGURE 9. TYPICAL TRANSITION TIME vs LOAD CPACITANCE

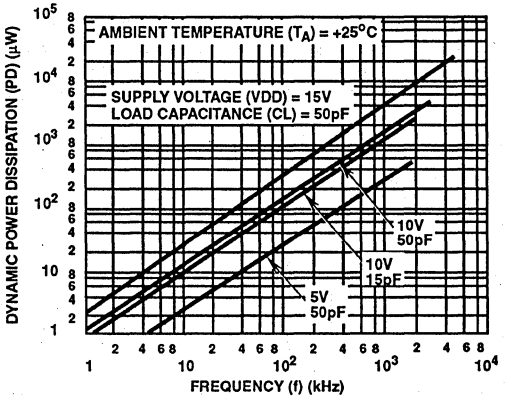


FIGURE 10. TYPICAL DYNAMIC POWER DISSIPATION vs FREQUENCY

Applications

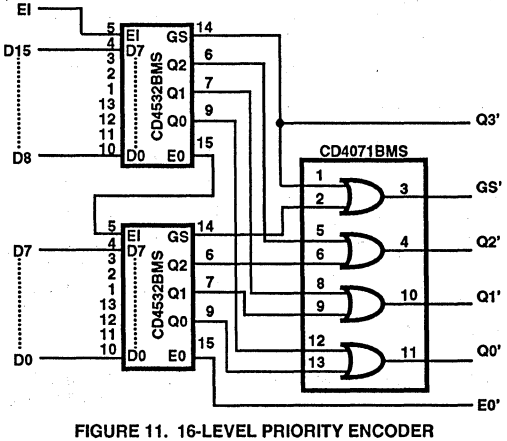


FIGURE 11. 16-LEVEL PRIORITY ENCODER

Applications (Continued)

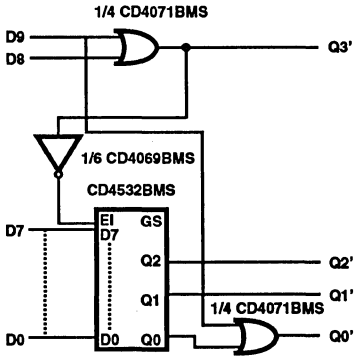


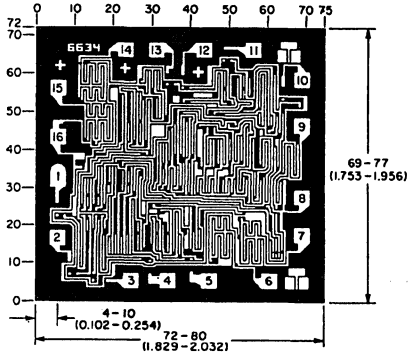
FIGURE 12. 0-TO-9 KEYBOARD ENCODER

TRUTH TABLE

INPUT										OUTPUT				
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q3'	Q2'	Q1'	Q0'
1	X	X	X	X	X	X	X	X	X	0	1	0	0	1
0	1	X	X	X	X	X	X	X	X	0	1	0	0	0
0	0	1	X	X	X	X	X	X	X	1	0	1	1	1
0	0	0	1	X	X	X	X	X	X	1	0	1	1	0
0	0	0	0	1	X	X	X	X	X	1	0	1	0	1
0	0	0	0	0	1	X	X	X	X	1	0	1	0	0
0	0	0	0	0	0	1	X	X	X	1	0	0	1	1
0	0	0	0	0	0	0	1	X	X	1	0	0	1	0
0	0	0	0	0	0	0	0	1	X	1	0	0	0	1
0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care Logic 1 ≡ High Logic 0 ≡ Low

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4536BMS

CMOS Programmable Timer

December 1992

Features

- High Voltage Type (20V Rating)
- 24 Flip-Flop Stage - Counts from 2^0 to 2^{24}
- Last 16 Stages Selectable by BCD Select Code
- Bypass Input Allows Bypassing First 8 Stages
- On-Chip RC Oscillator Provision
- Clock Inhibit Input
- Schmitt Trigger in clock Line Permits Operation with Very Long Rise and Fall Times
- On-Chip Monostable Output Provision
- Typical fCL = 3MHz at VDD = 10V
- Test Mode Allows Fast Test Sequence
- Set and Reset Inputs
- Capable of Driving Two Low Power TTL Loads, One Lower Power Schottky Load, or Two HTL Loads Over the Rated Temperature Range
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Standardized, Symmetrical Output Characteristics
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Description

CD4536BMS is a programmable timer consisting of 24 ripple binary counter stages. The salient feature of this device is its flexibility. The device can count from 1 to 2^{24} or the first 8 stages can be bypassed to allow an output, selectable by a 4-bit code, from any one of the remaining 16 stages. It can be driven by an external clock or an RC oscillator that can be constructed using on-chip components. Input IN1 serves as either the external clock input or the input to the on-chip RC oscillator. OUT1 and OUT2 are connection terminals for the external RC components. In addition, an on-chip monostable circuit is provided to allow a variable pulse width output. Various timing functions can be achieved using combinations of these capabilities.

A logic 1 on the 8-BYPASS input enables a bypass of the first 8 stages and makes stage 9 the first counter stage of the last 16 stages. Selection of 1 of 16 outputs is accomplished by the decoder and the BCD inputs A, B, C and D. MONO IN is the timing input for the on-chip monostable oscillator. Grounding of the MONO IN terminal through a resistor of 10kΩ or higher, disables the one-shot circuit and connects the decoder directly to the DECODE OUT terminal. A resistor to VDD and a capacitor to ground from the MONO IN terminal enables the one-shot circuit and controls its pulse width.

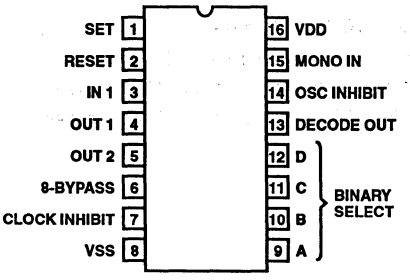
A fast test mode is enabled by a logic 1 on 8-BYPASS, SET, and RESET. This mode divides the 24-stage counter into three 8-stage sections to facilitate a fast test sequence.

The CD4536BMS is supplied in these 16-lead outline packages:

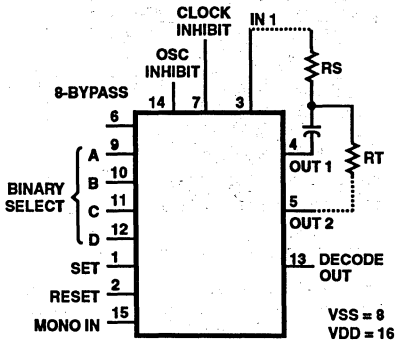
Braze Seal DIP	H4X
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

Pinout

CD4536BMS
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3345

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Q1 8-Bypass High	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	2000	ns
			10, 11	+125°C, -55°C	-	2700	ns
Propagation Delay Clock to Q1 8-Bypass Low	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	5000	ns
			10, 11	+125°C, -55°C	-	6750	ns
Propagation Delay Clock to Q16	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	8000	ns
			10, 11	+125°C, -55°C	-	10800	ns
Propagation Delay Reset to QN	TPHL4	VDD = 5V, VIN = VDD or GND	9	+25°C	-	6000	ns
			10, 11	+125°C, -55°C	-	8100	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	.5	-	MHz
			10, 11	+125°C, -55°C	.37	-	MHz

NOTES:

1. VDD = 5V, CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Clock to Q1 8-Bypass High	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	1000	ns
		VDD = 15V	1, 2, 3	+25°C	-	700	ns
Propagation Delay Clock to Q1 8-Bypass Low	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	1600	ns
		VDD = 15V	1, 2, 3	+25°C	-	1200	ns
Propagation Delay Clock to Q16	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25°C	-	3000	ns
		VDD = 15V	1, 2, 3	+25°C	-	2000	ns
Propagation Delay Qn to Qn+1	TPHL TPLH	VDD = 5V	1, 2, 3	+25°C	-	300	
		VDD = 10V	1, 2, 3	+25°C	-	150	
		VDD = 15V	1, 2, 3	+25°C	-	100	
Propagation Delay Set to Qn	TPLH	VDD = 5V	1, 2, 3	+25°C	-	600	
		VDD = 10V	1, 2, 3	+25°C	-	250	
		VDD = 15V	1, 2, 3	+25°C	-	160	
Propagation Delay Reset to Qn	TPHL4	VDD = 10V	1, 2, 3	+25°C	-	2000	ns
		VDD = 15V	1, 2, 3	+25°C	-	1500	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency. Unlimited Input Rise or Fall Time	FCL	VDD = 10V	1, 2, 3	+25°C	1.5	-	MHz
		VDD = 15V	1, 2, 3	+25°C	2.5	-	MHz
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	400	ns
		VDD = 10V	1, 2, 3	+25°C	-	150	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Minimum Set Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	400	ns
		VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Minimum Reset Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	6	µs
		VDD = 10V	1, 2, 3	+25°C	-	2	µs
		VDD = 15V	1, 2, 3	+25°C	-	1.5	µs
Minimum Set Recovery Time	TREM	VDD = 5V	1, 2, 3	+25°C	-	5	µs
		VDD = 10V	1, 2, 3	+25°C	-	2	µs
		VDD = 15V	1, 2, 3	+25°C	-	1.6	µs
Minimum Reset Recovery Time	TREM	VDD = 5V	1, 2, 3	+25°C	-	7	µs
		VDD = 10V	1, 2, 3	+25°C	-	3	µs
		VDD = 15V	1, 2, 3	+25°C	-	2	µs
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	4, 5, 13	1-3, 6-12, 14, 15	16			
Static Burn-In 2 Note 1	4, 5, 13	8	1-3, 6, 7, 9-12, 14-16			
Dynamic Burn-In Note 1	-	1, 2, 6-8, 14, 15	9-12, 16	4, 5, 13	3	
Irradiation Note 2	4, 5, 13	8	1-3, 6, 7, 9-12, 14-16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram

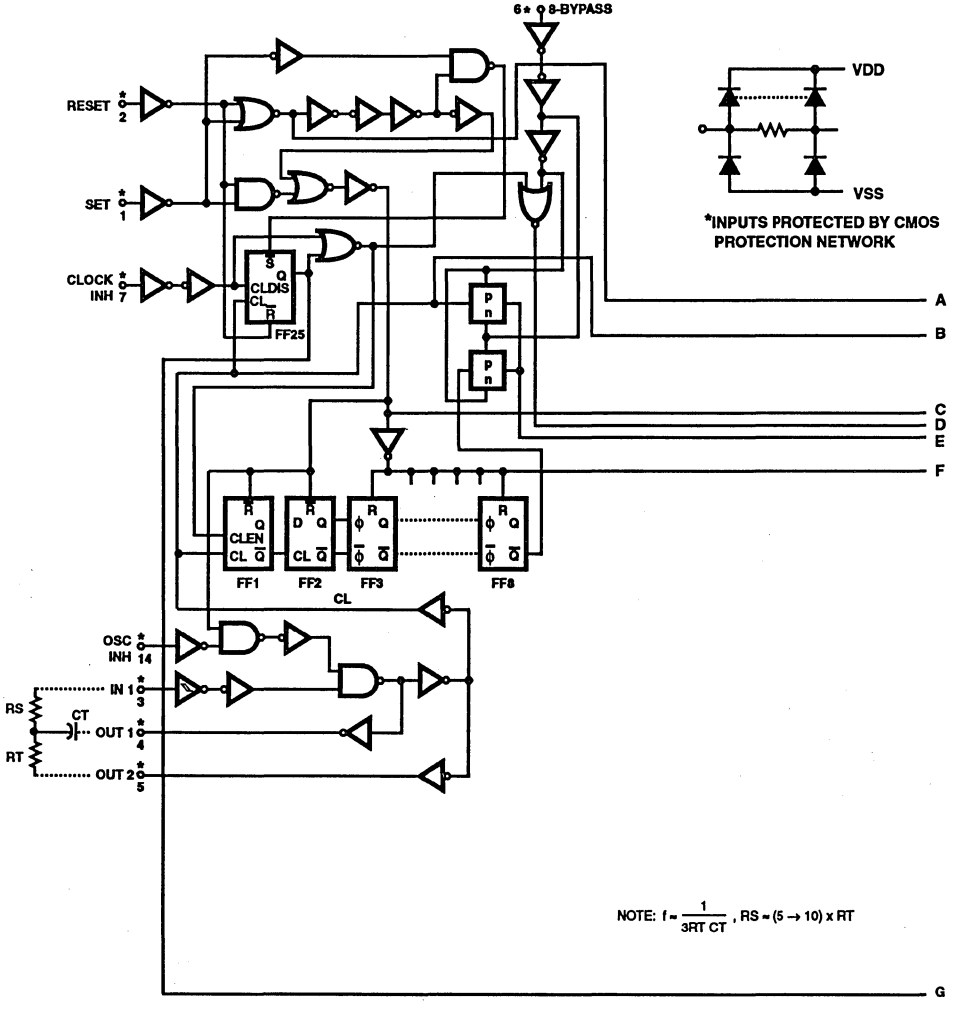
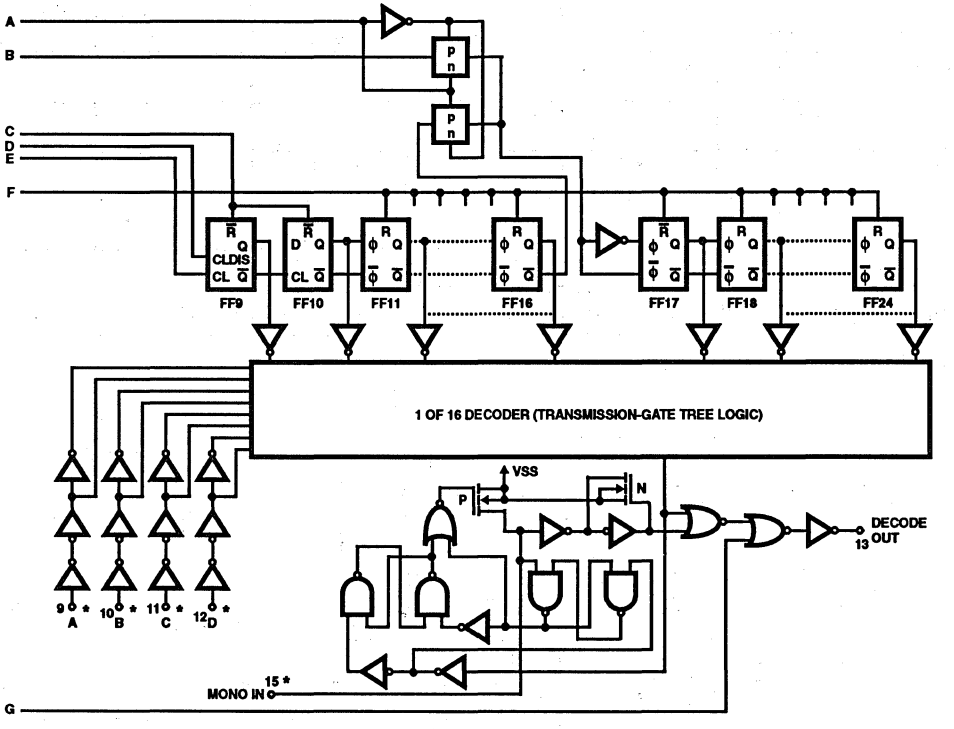
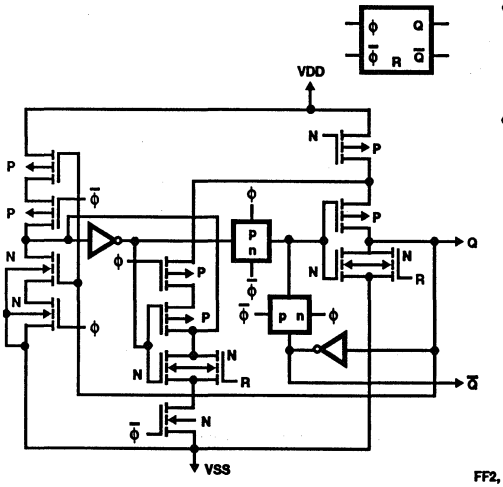


FIGURE 1.

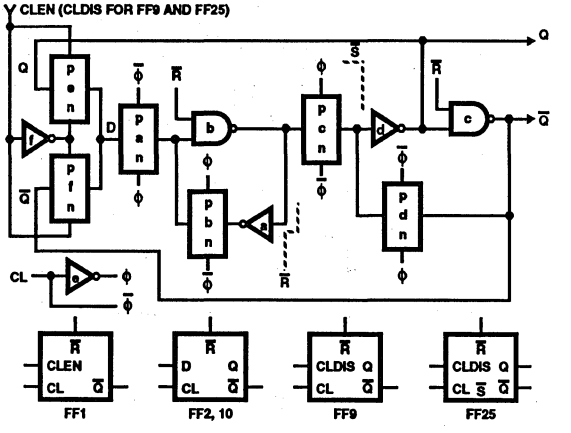
Logic Diagram (Continued)



DETAIL FOR
FF3-8, 11-16, 17-24



DETAIL FOR
FF1, FF2, FF10, FF9, FF25



FF1: AS SHOWN EXCEPT Q NOT BROUGHT OUT

FF9: SAME AS FF1 EXCEPT Q IS BROUGHT OUT AND Q, $\overline{Q}$ GO TO TGf AND TGe RESP.

FF2, FF10: DELETE TGe, TGf, AND INVf; FEED $\overline{Q}$ TO D; DELETE CLEN, CLDIS

FF25: INVa AND INVd BECOME 2-INPUT NAND GATES, WITH ADDED INPUTS $\overline{S}$; FEED Q TO TGf VSS TO TGe PREVIOUS Q INPUT; DELETE $\overline{Q}$ OUTPUT

FIGURE 1. (Continued)

TRUTH TABLE

IN	SET	RESET	CLOCK INH	OSC INH	OUT1	OUT2	DECODE OUT
⎍	0	0	0	0	⎍	⎎	No Change
⎎	0	0	0	0	⎎	⎍	Advance to Next State
X	1	0	0	0	0	1	1
X	0	1	0	0	0	1	0
X	0	0	1	0			No Change
0	0	0	0	X	0	1	No Change
1	0	0	0	⎍	⎎	⎍	Advance to Next State

0 = Low Level 1 = High Level X = Don't Care

Typical Performance Characteristics

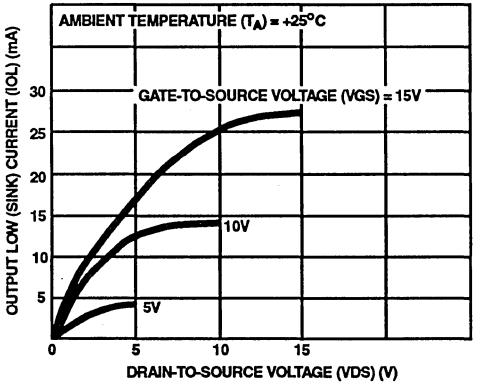


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

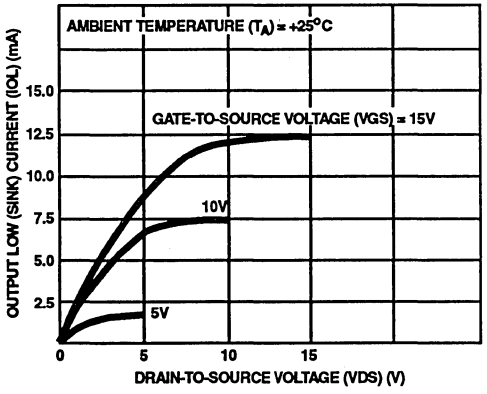


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

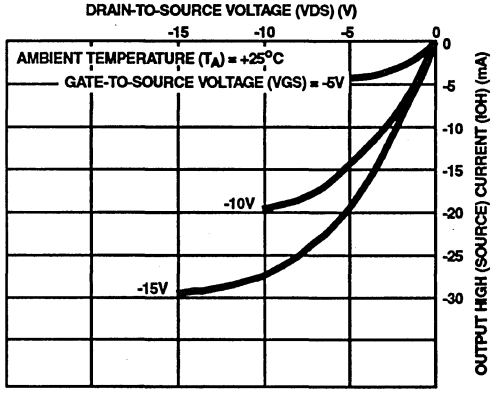


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

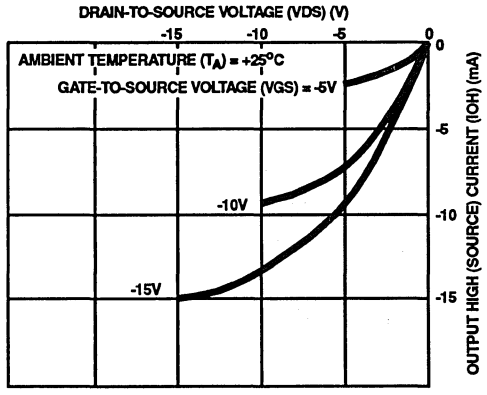


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

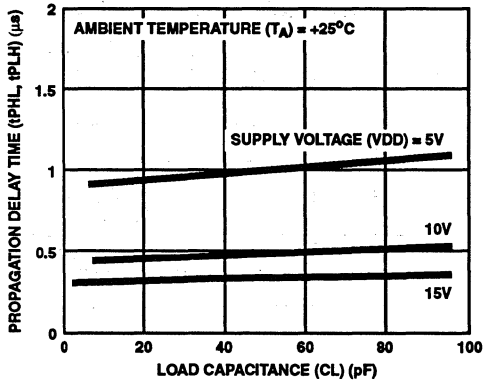


FIGURE 6. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (CLOCK TO Q1, 8-BYPASS HIGH)

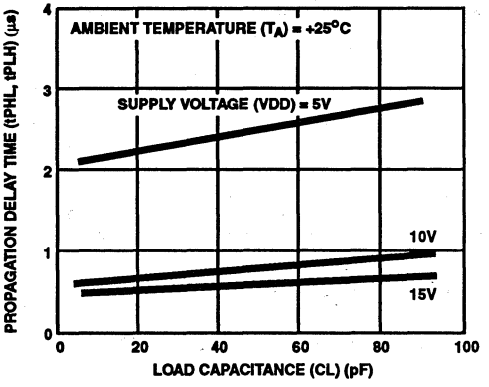


FIGURE 7. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (CLOCK TO Q1, 8-BYPASS LOW)

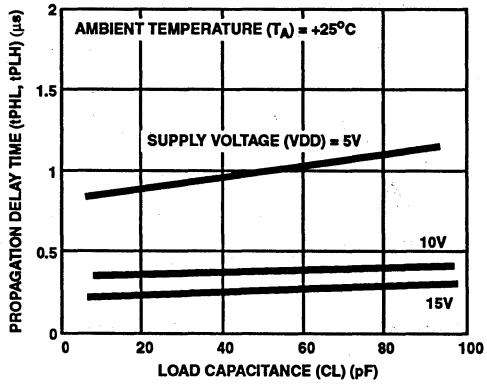


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (CLOCK TO Q16, 8-BYPASS HIGH)

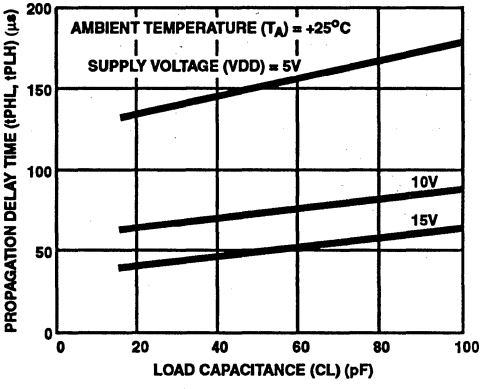


FIGURE 9. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (QN TO QN + 1)

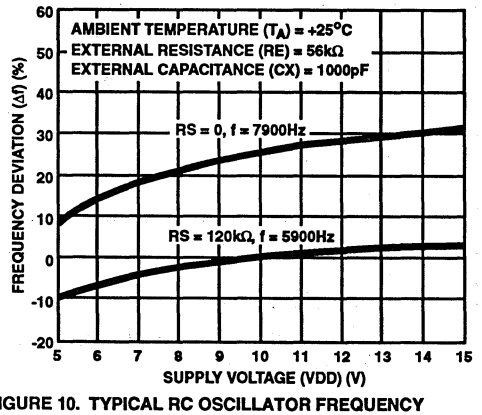


FIGURE 10. TYPICAL RC OSCILLATOR FREQUENCY DEVIATION AS A FUNCTION OF SUPPLY VOLTAGE

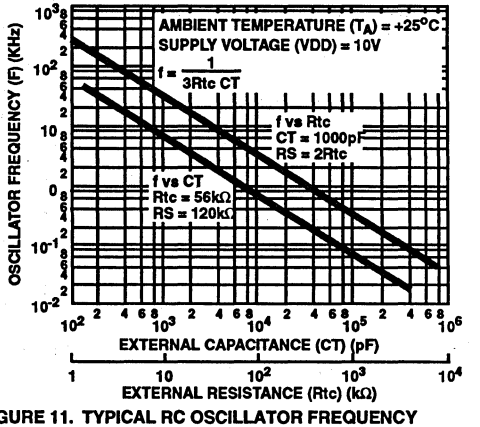


FIGURE 11. TYPICAL RC OSCILLATOR FREQUENCY DEVIATION AS A FUNCTION OF TIME CONSTANT RESISTANCE AND CAPACITANCE

Typical Performance Characteristics (Continued)

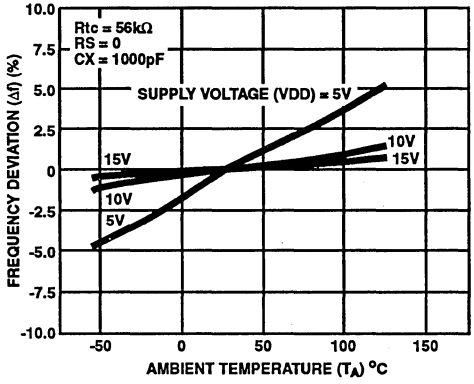


FIGURE 12. TYPICAL RC OSCILLATOR FREQUENCY DEVIATION AS A FUNCTION OF AMBIENT TEMPERATURE (RS = 0)

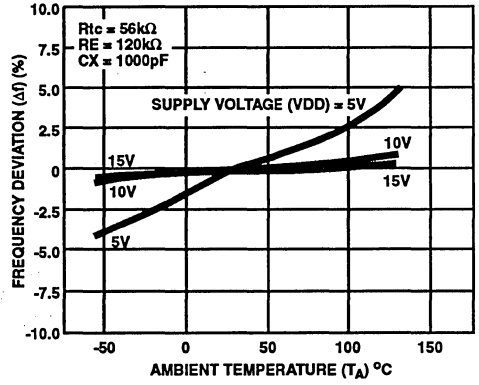


FIGURE 13. TYPICAL RC OSCILLATOR FREQUENCY DEVIATION AS A FUNCTION OF AMBIENT TEMPERATURE (RS = 120kΩ)

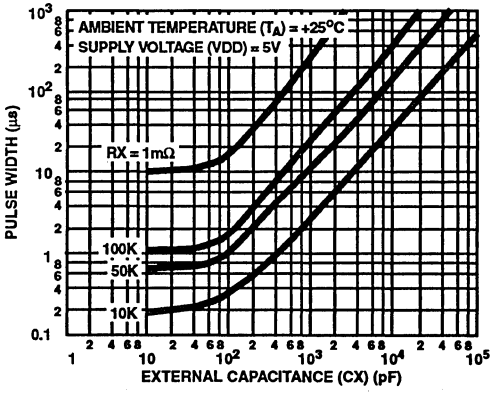


FIGURE 14. TYPICAL PULSE WIDTH AS A FUNCTION OF EXTERNAL CAPACITANCE (VDD = 5V)

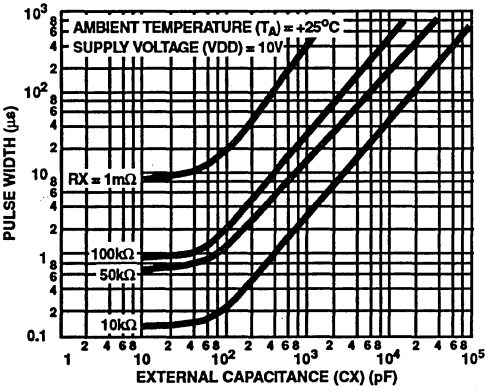


FIGURE 15. TYPICAL PULSE WIDTH AS A FUNCTION OF EXTERNAL CAPACITANCE (VDD = 10V)

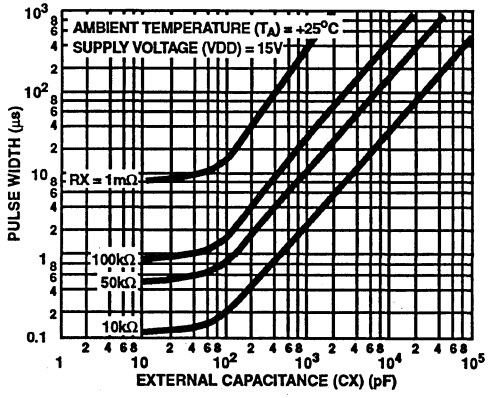


FIGURE 16. TYPICAL PULSE WIDTH AS A FUNCTION OF EXTERNAL CAPACITANCE (VDD = 15V)

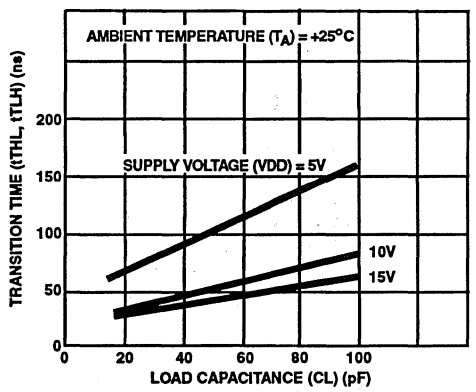


FIGURE 17. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

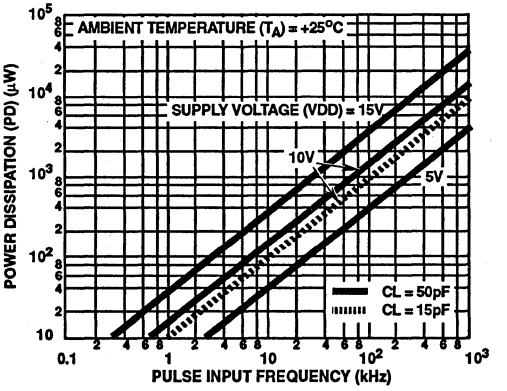


FIGURE 18. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT PULSE FREQUENCY

Applications

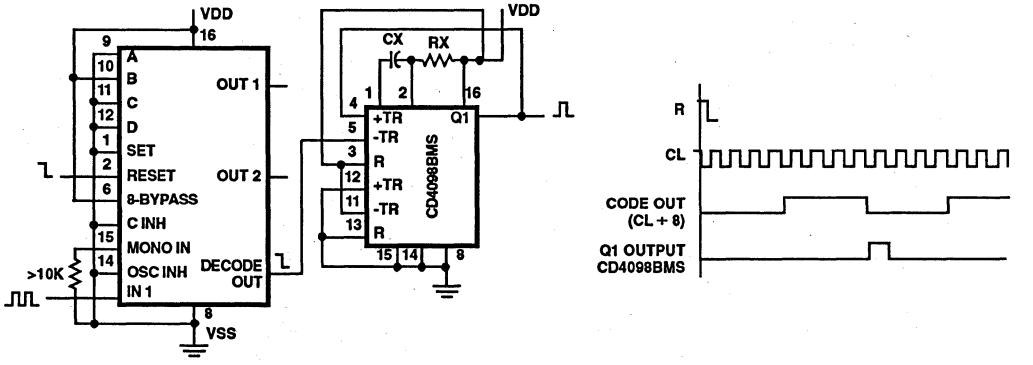


FIGURE 19. APPLICATION SHOWING USE OF CD4098BMS AND CD4536BMS TO GET DECODE PULSE 8 CLOCK PULSES AFTER RESET PULSE

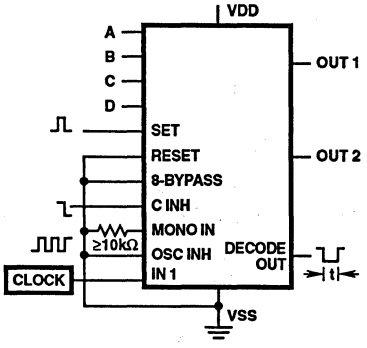


FIGURE 20. TIME INTERVAL CONFIGURATION USING EXTERNAL CLOCK; SET AND CLOCK INHIBIT FUNCTIONS

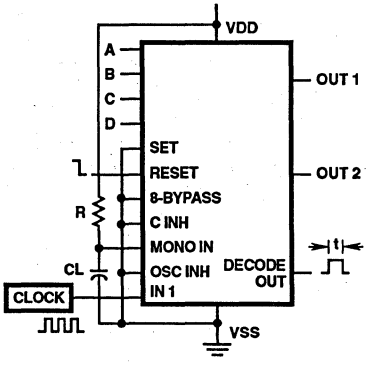


FIGURE 21. TIME INTERVAL CONFIGURATION USING EXTERNAL CLOCK; RESET AND OUTPUT MONOSTABLE TO ACHIEVE A PULSE OUTPUT

Applications (Continued)

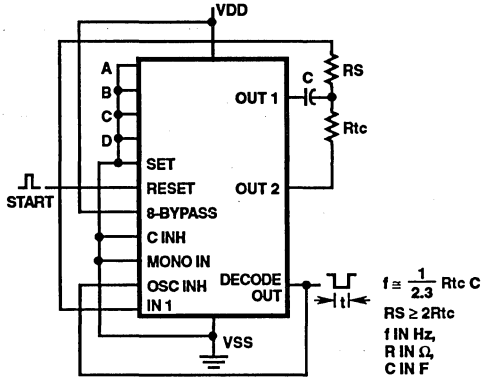
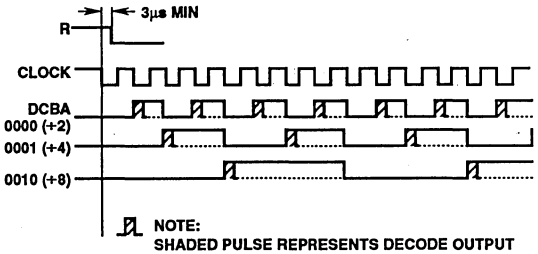


FIGURE 22. TIME INTERVAL CONFIGURATION USING ON-CHIP RC OSCILLATOR AND RESET INPUT TO INITIATE TIME INTERVAL



NOTE:
SHADED PULSE REPRESENTS DECODE OUTPUT IN MONOSTABLE MODE. IF AN OUTPUT PULSE IS REQUIRED 1 FULL COUNTDOWN AFTER REMOVAL OF RESET PULSE, SEE FIGURE 19 FOR USE OF CD4098BMS.

FIGURE 23. TIMING DIAGRAM

DECODE OUT SELECTION TABLE

				NUMBER OF STAGES IN DIVIDER CHAIN	
D	C	B	A	8-BYPASS = 0	8-BYPASS = 1
0	0	0	0	9	1
0	0	0	1	10	2
0	0	1	0	11	3
0	0	1	1	12	4
0	1	0	0	13	5
0	1	0	1	14	6
0	1	1	0	15	7
0	1	1	1	16	8
1	0	0	0	17	9
1	0	0	1	18	10
1	0	1	0	19	11
1	0	1	1	20	12
1	1	0	0	21	13
1	1	0	1	22	14
1	1	1	0	23	15
1	1	1	1	24	16

0 = Low Level 1 = High Level

Functional Block Diagram

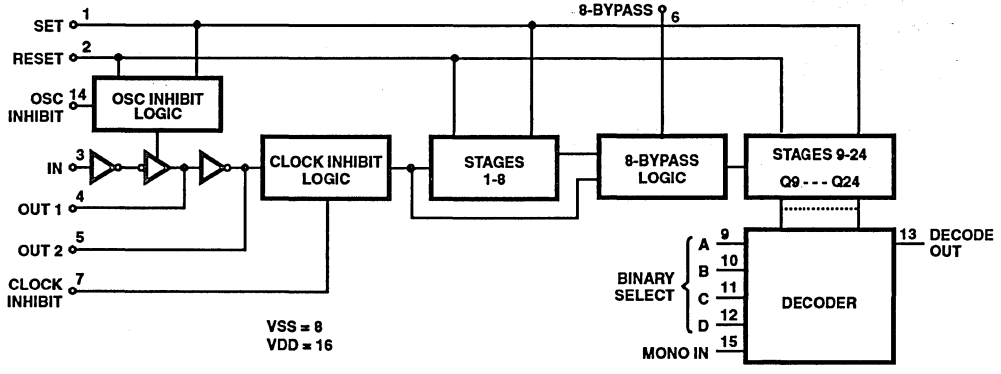


FIGURE 24.

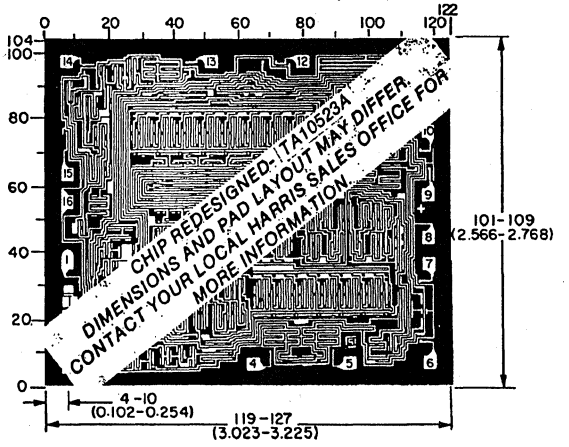
FUNCTIONAL TEST SEQUENCE

INPUTS				OUTPUTS	COMMENTS
IN 1	SET	RESET	8-BYPASS	DECODE OUT Q1 THRU 24	
1	0	1	1	0	ALL 24 STEPS ARE IN RESET MODE
1	1	1	1	0	Counter is in three 8-stage section in parallel mode
0	1	1	1	0	First "1" to "0" transition of clock
1 0 - - -	1	1	1		255 "1" to "0" transitions are clocked in the counter
0	1	1	1	1	The 255 "1" to "0" transition
0	0	0	0	1	Counter converted back to 24 stages in series mode. Set and Reset must be connected together and simultaneously go from "1" to "0"
1	0	0	0	1	In1 Switches to a "1"
0	0	0	0	0	Counter Ripples from an all "1" state to an all "0" state

Functional Test Sequence

Test Function has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a "1". The counter is now returned to the normal 24 steps in series configuration. One more pulse is entered into In1 which will cause the counter to ripple from an all "1" state to an all "0" state.

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4555BMS
CD4556BMS

CMOS Dual Binary to 1 of 4 Decoder/Demultiplexers

December 1992

Features

- High Voltage Type (20V Rating)
- CD4555BMS: Outputs High on Select
- CD4556BMS: Outputs Low on Select
- Expandable with Multiple Packages
- 100% Tested for Quiescent Current at 20V
- Standardized, Symmetrical Output Characteristics
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Decoding
- Code Conversion
- Demultiplexing (Using Enable Input as a Data Input
- Memory Chip-Enable Selection
- Function Selection

Description

CD4555BMS and CD4556BMS are dual one-of-four decoders/demultiplexers. Each decoder has two select inputs (A and B), an Enable input ($\overline{E}$), and four mutually exclusive outputs. On the CD4555BMS the outputs are high on select; on the CD4556BMS the outputs are low on select.

When the Enable input is high, the outputs of the CD4555BMS remain low and the outputs of the CD4556BMS remain high regardless of the state of the select inputs A and B. The CD4555BMS and CD4556BMS are similar to types MC14555 and MC14556, respectively.

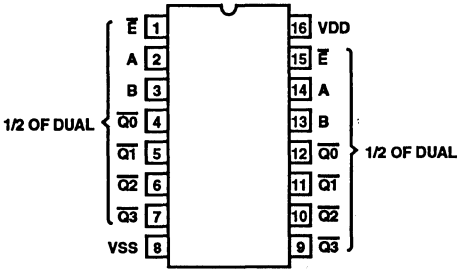
The CD4555BMS and CD4556BMS are supplied in these 16-lead outline packages:

Braze Seal DIP	*H46	†H4T
Frit Seal DIP	H1E	
Ceramic Flatpack	H6W	

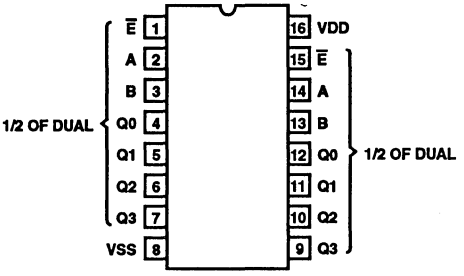
*CD4555B Only †CD4556B Only

Pinouts

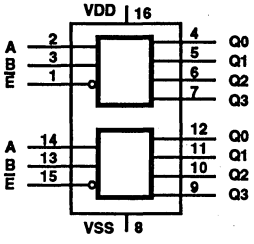
CD4556BMS
TOP VIEW



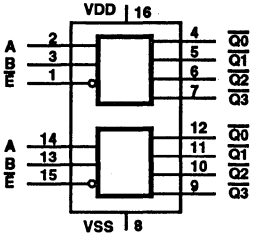
CD4555BMS
TOP VIEW



Functional Diagrams



CD4555BMS



CD4556BMS

7 LOGIC

File Number 3346

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay A or B Input to any Output	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	440	ns
			10, 11	+125°C, -55°C	-	594	ns
Propagation Delay $\overline{E}$ to any Output	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay A or B Input to any Output	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	190	ns
		VDD = 15V	1, 2, 3	+25°C	-	140	ns
Propagation Delay $\overline{E}$ to any Output	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	170	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
PART NUMBER	CD4555BMS & CD4556BMS					
Static Burn-In 1 Note 1	4 - 7, 9 - 12	1 - 3, 8, 13 - 15	16			
Static Burn-In 2 Note 1	4 - 7, 9 - 12	8	1 - 3, 13 - 16			
Dynamic Burn-In Note 1	-	1, 8, 15	16	4 - 7, 9 - 12	2, 14	3, 13
Irradiation Note 2						

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagrams

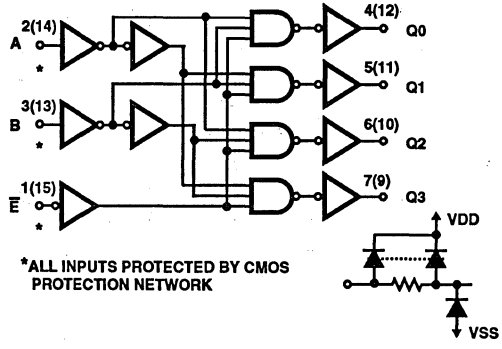


FIGURE 1. CD455RBMS LOGIC DIAGRAM (1 OF 2 IDENTICAL CIRCUITS)

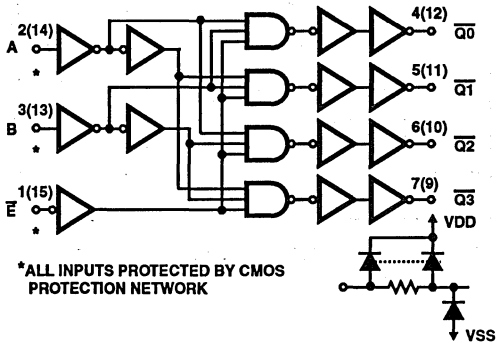


FIGURE 2. CD4556BMS LOGIC DIAGRAM (1 OF 2 IDENTICAL CIRCUITS)

TRUTH TABLE

INPUTS ENABLE SELECT			OUTPUTS CD4555BMS				OUTPUTS CD4556BMS			
E	B	A	Q3	Q2	Q1	Q0	Q3	Q2	Q1	Q0
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = Don't Care

Logic 1 ≡ High
Logic 0 ≡ Low

Typical Performance Characteristics

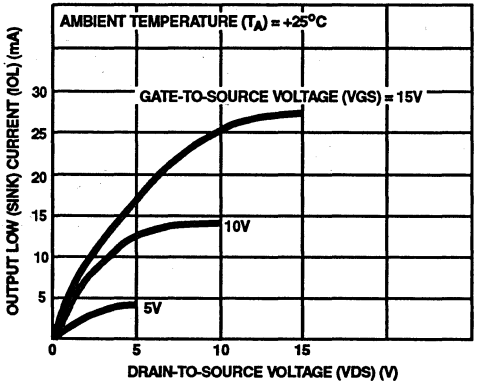


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

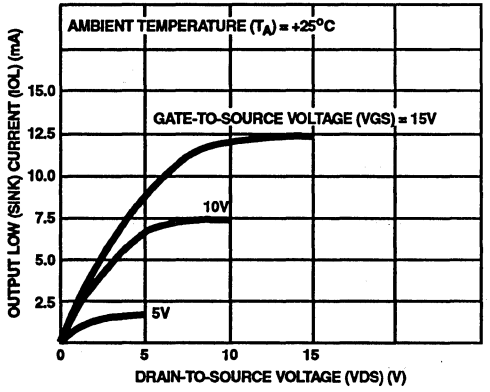


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

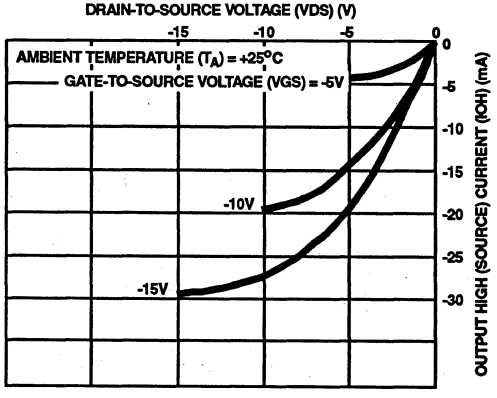


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

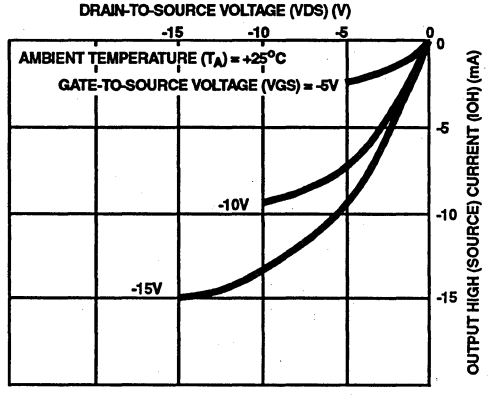


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

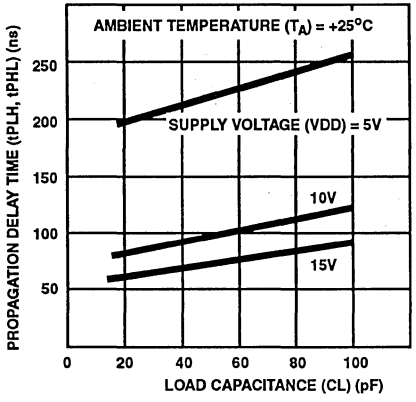


FIGURE 7. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE (A OR B INPUT TO ANY OUTPUT)

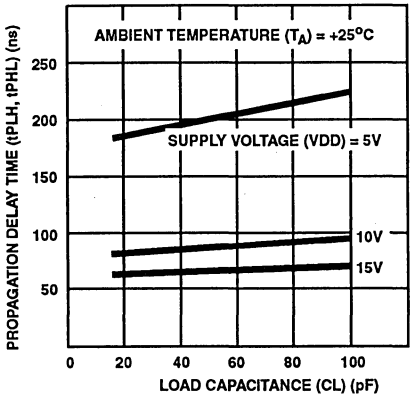


FIGURE 8. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE ($\overline{E}$ INPUTS TO ANY OUTPUT)

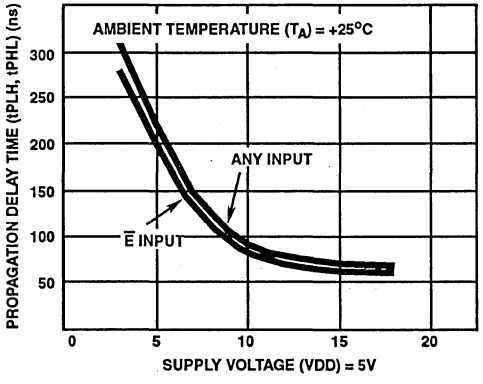


FIGURE 9. TYPICAL PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

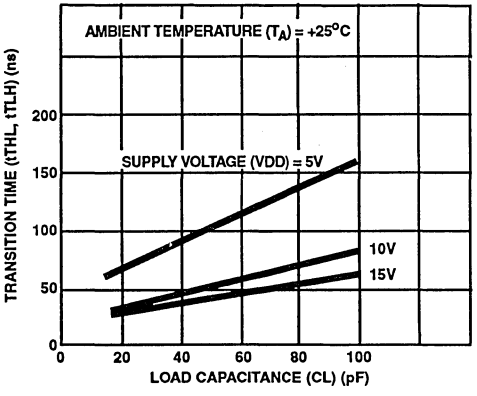


FIGURE 10. TYPICAL TRANSITION TIME vs LOAD CPACITANCE

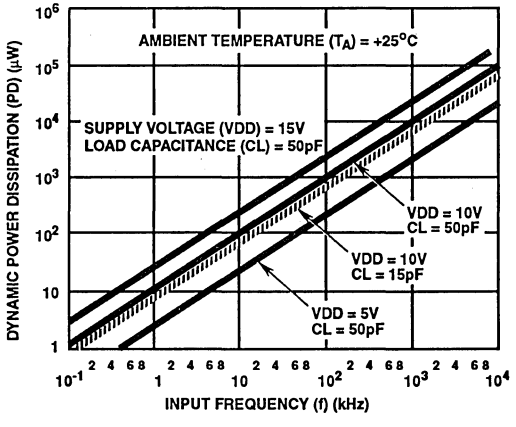
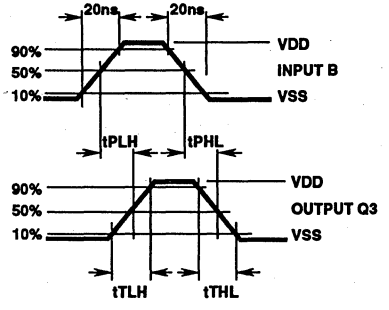


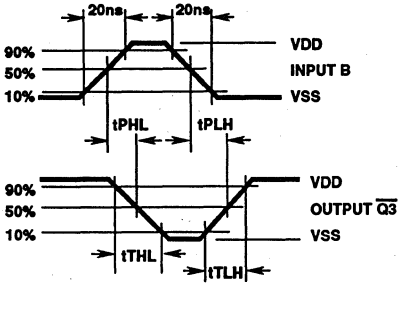
FIGURE 11. TYPICAL DYNAMIC POWER DISSIPATION vs FREQUENCY

7 LOGIC



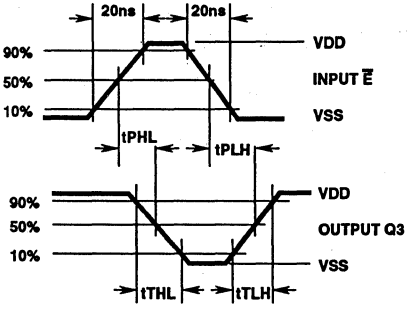
fl = 1MHz, 50% DUTY CYCLE

FIGURE 12. CD4555BMS B INPUT TO Q3 OUTPUT DYNAMIC SIGNAL WAVEFORMS



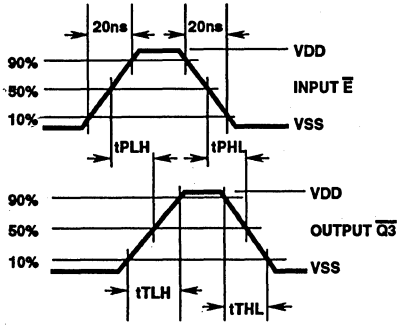
fl = 1MHz, 50% DUTY CYCLE

FIGURE 13. CD4556BMS B INPUT TO $\overline{Q3}$ OUTPUT DYNAMIC SIGNAL WAVEFORMS



fl = 1MHz, 50% DUTY CYCLE

FIGURE 14. CD4555BMS $\overline{E}$ INPUT TO Q3 OUTPUT DYNAMIC SIGNAL WAVEFORMS



fl = 1MHz, 50% DUTY CYCLE

FIGURE 15. CD4556BMS $\overline{E}$ INPUT TO $\overline{Q3}$ OUTPUT DYNAMIC SIGNAL WAVEFORMS

Applications

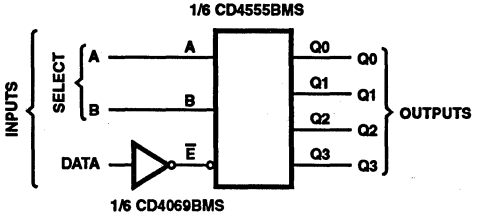
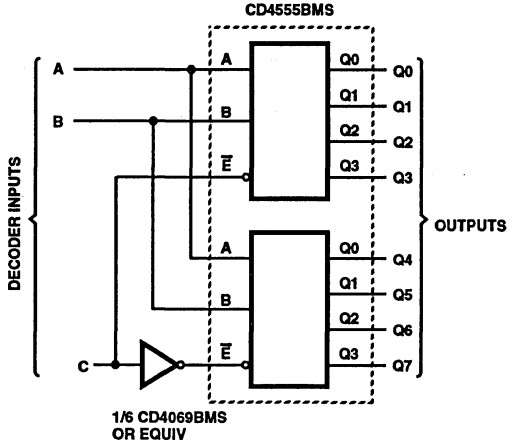


FIGURE 16. 1 OF 4 LINE DATA DEMULTIPLEXER USING CD4555BMS

TRUTH TABLE

SELECT INPUTS		OUTPUTS			
B	A	Q0	Q1	Q2	Q3
0	0	DATA	0	0	0
0	1	0	DATA	0	0
1	0	0	0	DATA	0
1	1	0	0	0	DATA

Applications (Continued)



TRUTH TABLE

INPUTS			Q OUTPUTS							
C	B	A	0	1	2	3	4	5	6	7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

FIGURE 17. 1 OF 8 DECODER USING CD4555BMS

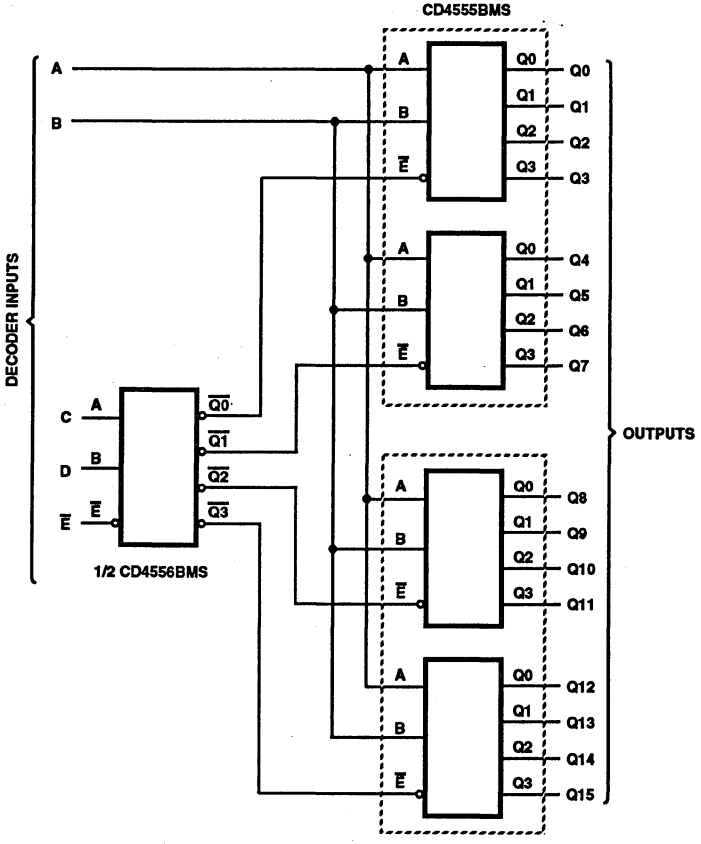


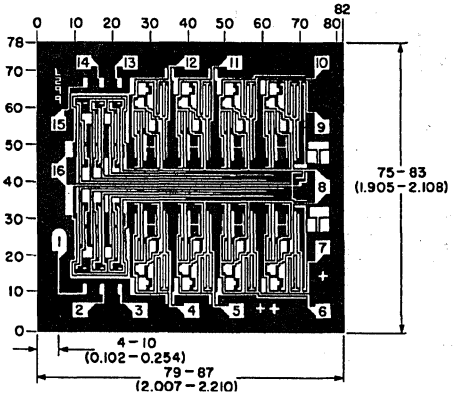
FIGURE 18. 1 OF 16 DECODER USING CD4555BMS AND CD4556BMS

TRUTH TABLE

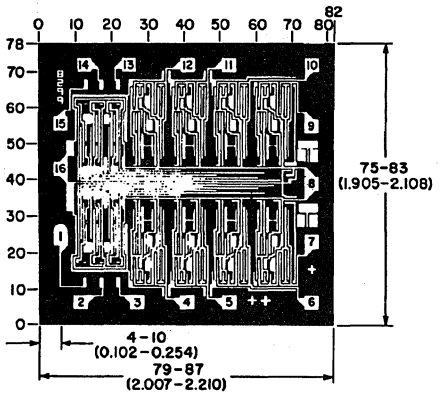
INPUTS					Q OUTPUTS														
E	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

X = Don't Care

Chip Dimensions and Pad Layouts



CD4555BMSH



CD4556BMSH

Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10-3 inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

CD4585BMS

CMOS 4-Bit Magnitude Comparator

December 1992

Features

- High Voltage Type (20V Rating)
- Expansion to 8, 12, 16 . . .4N Bits by Cascading Units
- Medium Speed Operation
  - Compares Two 4-Bit Words in 180ns (Typ.) at 10V
- 100% Tested for Quiescent Current at 20V
- Standardized Symmetrical Output Characteristics
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Servo Motor Controls
- Process Controllers

Description

CD4585BMS is a 4-bit magnitude comparator designed for use in computer and logic applications that require the comparison of two 4-bit words. This logic circuit determines whether one 4-bit word (Binary or BCD) is "less than", "equal to" or "greater than" a second 4-bit word.

The CD4585BMS has eight comparing inputs (A3, B3, through A0, B0), three outputs (A < B, = B, A > B) and three cascading inputs (A < B, A = B, A > B) that permit system designers to expand the comparator function to 8, 12, 16 . . .4N bits. When a single CD4585BMS is used, the cascading inputs are connected as follows: (A < B) = low, (A = B) = high, (A > B) = high.

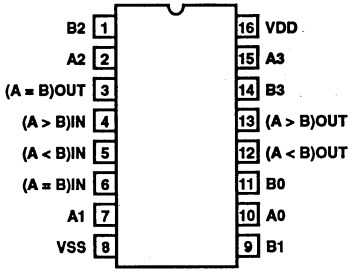
Cascading thses units for comparision of more than 4 bits is accomplished as shown in Figure 9.

The CD4585BMS is supplied in these 16-lead outline packages:

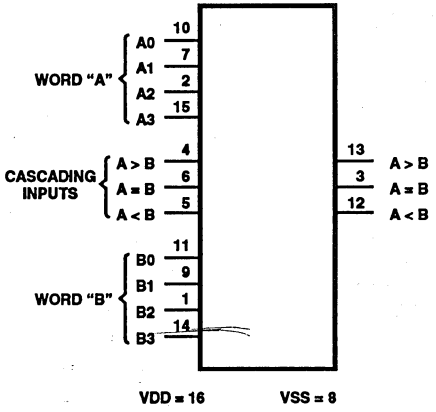
Braze Seal DIP	H4T
Frit Seal DIP	H1E
Ceramic Flatpack	H6W

Pinout

CD4585BMS
TOP VIEW



Functional Diagram



7 LOGIC

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range.....-55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG).....-65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K).....500mW
For T_A = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature .....+175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

						LIMITS		
PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	MIN	MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
* Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Comparing Inputs to Outputs	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Propagation Delay Cascading Inputs to Outputs	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Comparing Inputs to Outputs	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	250	ns
		VDD = 15V	1, 2, 3	+25°C	-	160	ns
Propagation Delay Cascading Inputs to Outputs	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Inputs	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	3, 12, 13	1, 2, 4 - 11, 14, 15	16			
Static Burn-In 2 Note 1	3, 12, 13	8	1, 2, 4 - 7, 9 - 11, 14 - 16			
Dynamic Burn-In Note 1	-	5 - 9, 11, 14, 15	1, 4, 16	3, 12, 13	2	10
Irradiation Note 2	3, 12, 13	8	1, 2, 4 - 7, 9 - 11, 14 - 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram

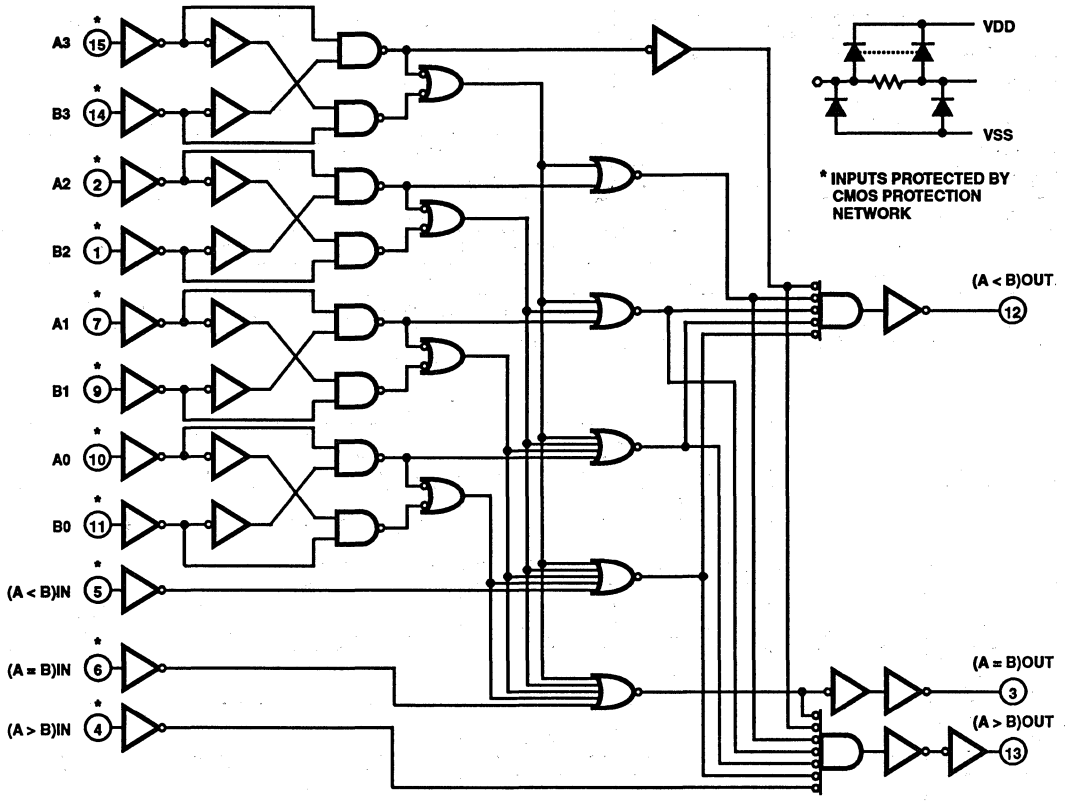


FIGURE 1. LOGIC DIAGRAM

TRUTH TABLE

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3, B3	A2, B2	A1, B1	A0, B0	A < B	A = B	A > B	A < B	A = B	A > B
A3 > B3	X	X	X	X	X	1	0	0	1
A3 = B3	A2 > B2	X	X	X	X	1	0	0	1
A3 = B3	A2 = B2	A1 > B1	X	X	X	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	1	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	1	X	0	1	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	0	X	1	0	0
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	1	0	0
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	1	0	0
A3 = B3	A2 < B2	X	X	X	X	X	1	0	0
A3 < B3	X	X	X	X	X	X	1	0	0

X = Don't Care Logic 1 = High Level Logic 0 = Low Level

Typical Performance Characteristics

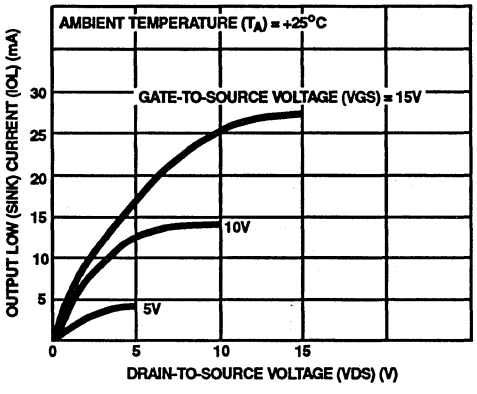


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

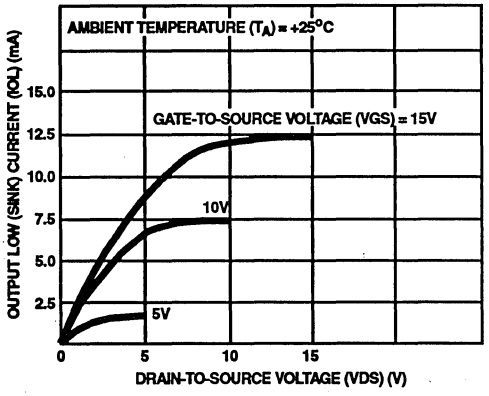


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

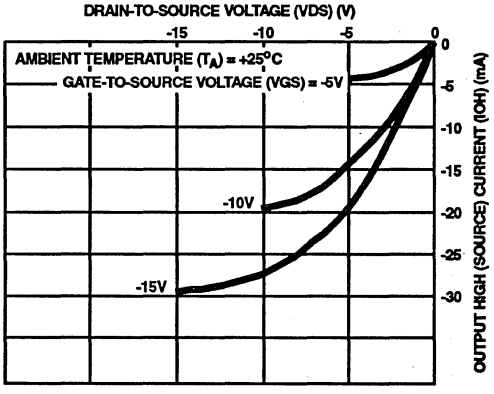


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

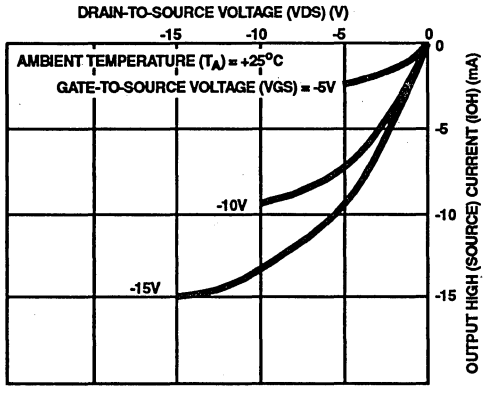


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

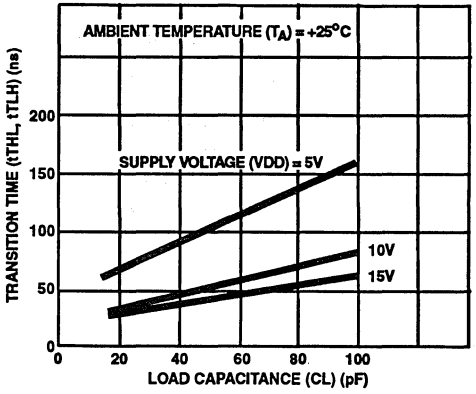


FIGURE 6. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

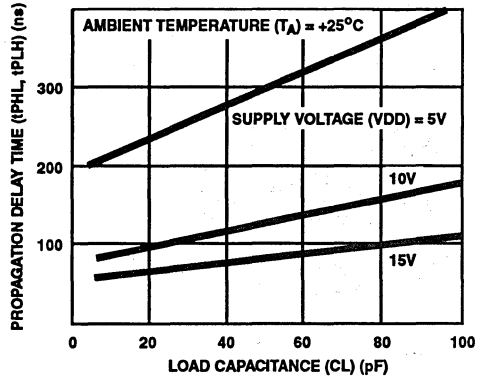


FIGURE 7. TYPICAL PROPAGATION DELAY TIME ("COMPARING INPUTS" TO OUTPUTS) AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

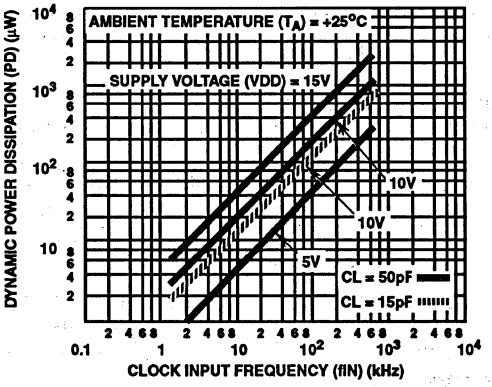
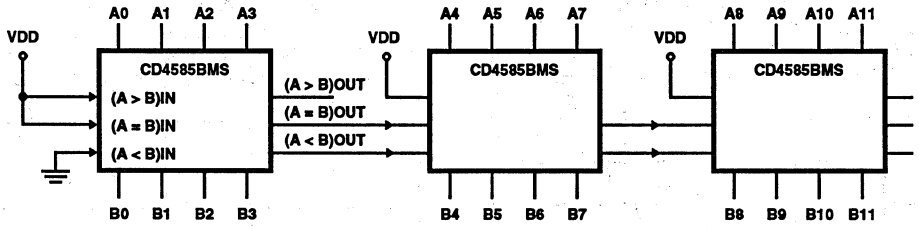


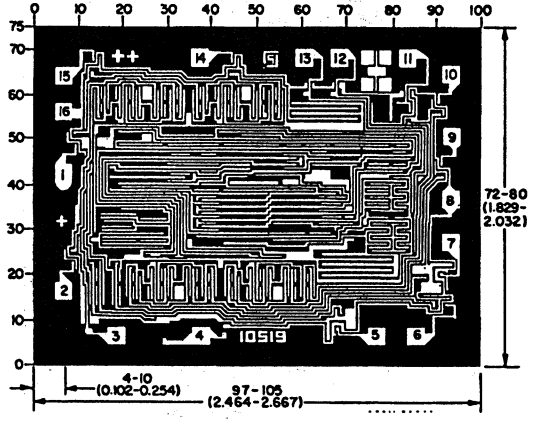
FIGURE 8. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF CLOCK INPUT FREQUENCY



tp TOTAL = tp (COMPARE) + 2 x tp (CASCADE), AT VDD = 10V
INPUTS INPUTS

FIGURE 9. TYPICAL SPEED CHARACTERISTICS OF A 12-BIT COMPARATOR

Chip Dimensions and Pad Layout



Dimensions in parenthese are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD4724BMS

December 1992

CMOS 8-Bit Addressable Latch

Features

- High Voltage Type (20V Rating)
- Serial Data Input
- Active Parallel Output
- Storage Register Capability
- Master Clear
- Can Function as Demultiplexer
- Standardized Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Multi-line Decoders
- A/D Converters

Description

CD4724BMS 8-bit addressable latch is a serial-input, parallel-output storage register that can perform a variety of functions.

Data are inputted to a particular bit in the latch when that bit is addressed (by means of inputs A0, A1, A2) and when WRITE DISABLE is at a low level. When WRITE DISABLE is high, data entry is inhibited; however, all 8 outputs can be continuously read independent of WRITE DISABLE and address inputs.

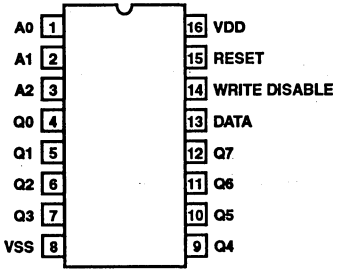
A master RESET input is available, which resets all bits to a logic "0" level when RESET and WRITE DISABLE are at a high level. When RESET is at a high level, and WRITE DISABLE is at a low level, the latch acts as a 1-of-8 demultiplexer; the bit that is addressed has an active output which follows that data input, while all unaddressed bits are held to a logic "0" level.

The CD4724BMS is supplied in these 16-lead outline packages:

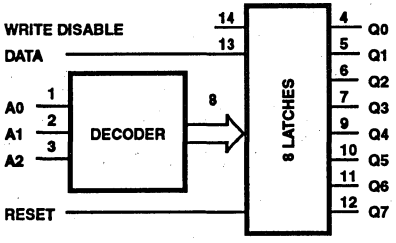
Braze Seal DIP	H4W
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

Pinout

CD4724BMS
TOP VIEW



Functional Diagram



VDD = 16
VSS = 8

7 LOGIC

File Number 3348

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Data to Output	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay Write Disable to Output	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay Reset to Output	TPHL3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	350	ns
			10, 11	+125°C, -55°C	-	473	ns
Propagation Delay Address to Output	TPHL4 TPLH4	VDD = 5V, VIN = VDD or GND	9	+25°C	-	450	ns
			10, 11	+125°C, -55°C	-	608	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Data to Output	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	150	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Propagation Delay Write Disable to Output	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Propagation Delay Reset to Output	TPHL3	VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Propagation Delay Address to Output	TPHL4 TPLH4	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	150	ns
Transition Time	TTLH TTHL	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Minimum Address Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	400	MHz
		VDD = 10V	1, 2, 3	+25°C	-	200	MHz
		VDD = 15V	1, 2, 3	+25°C	-	125	MHz
Minimum Reset Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	150	ns
		VDD = 10V	1, 2, 3	+25°C	-	75	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Data Setup Time Data to Write Disable	TS	VDD = 5V	1, 2, 3	+25°C	-	100	ns
		VDD = 10V	1, 2, 3	+25°C	-	50	ns
		VDD = 15V	1, 2, 3	+25°C	-	35	ns
Minimum Data Hold Time Data to Write Disable	TH	VDD = 5V	1, 2, 3	+25°C	-	150	ns
		VDD = 10V	1, 2, 3	+25°C	-	75	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Data Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	4 - 7, 9 - 12	1 - 3, 8, 13 - 15	16			
Static Burn-In 2 Note 1	4 - 7, 9 - 12	8	1 - 3, 13 - 16			
Dynamic Burn-In Note 1	-	1 - 3, 8	16	4 - 7, 9 - 12	14, 15	13
Irradiation Note 2	4 - 7, 9 - 12	8	1 - 3, 13 - 16			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram

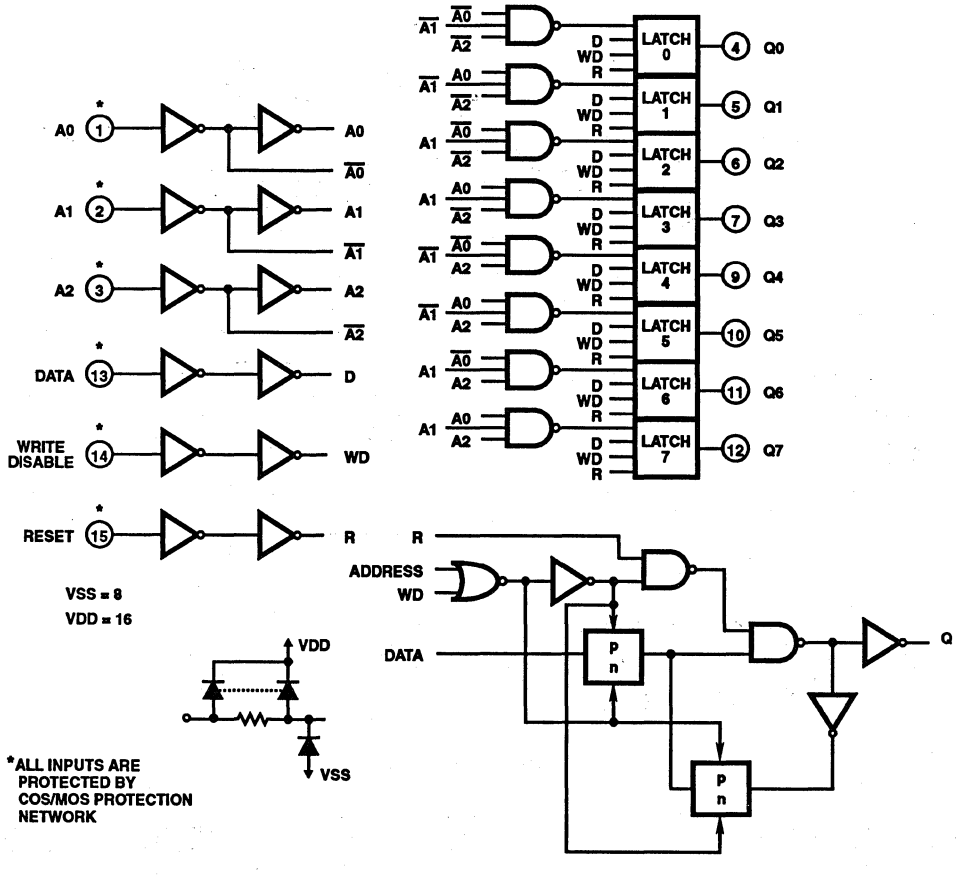


FIGURE 1. LOGIC DIAGRAM OF CD4724BMS AND DETAIL OF 1 OF 8 LATCHES

Typical Performance Characteristics

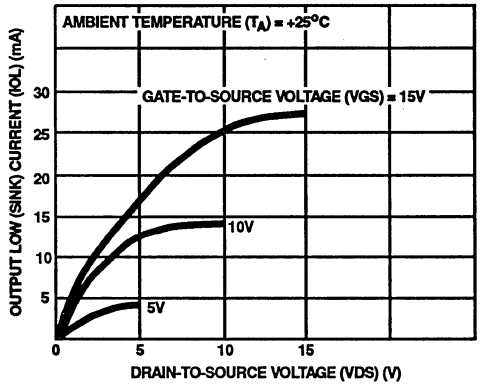


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

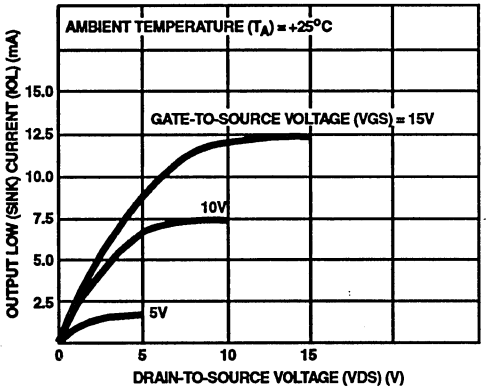


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

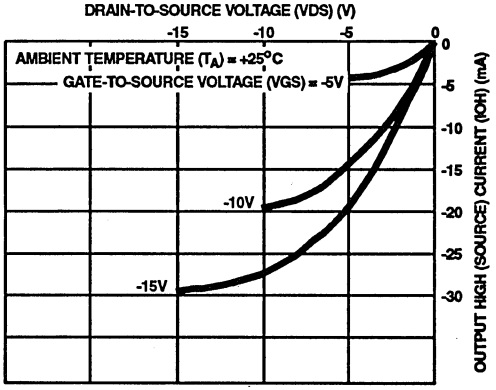


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

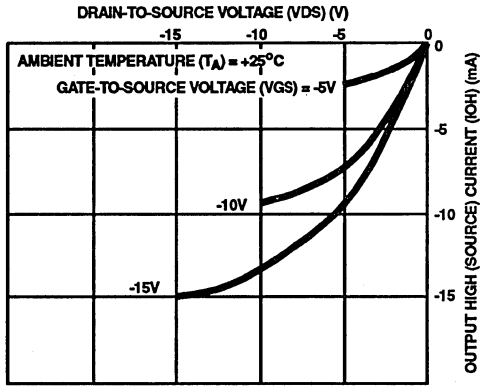


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

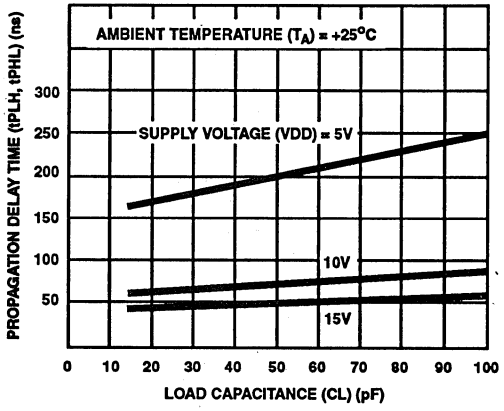


FIGURE 6. TYPICAL PROPAGATION DELAY TIME (DATA TO QN) vs LOAD CAPACITANCE

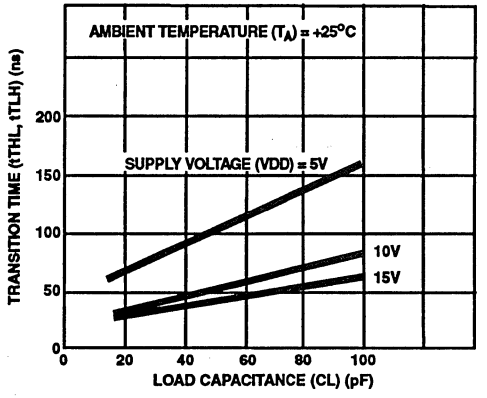


FIGURE 7. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

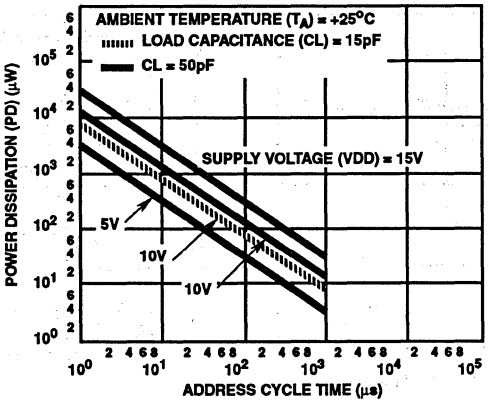


FIGURE 8. TYPICAL DYNAMIC POWER DISSIPATION vs ADDRESS CYCLE TIME

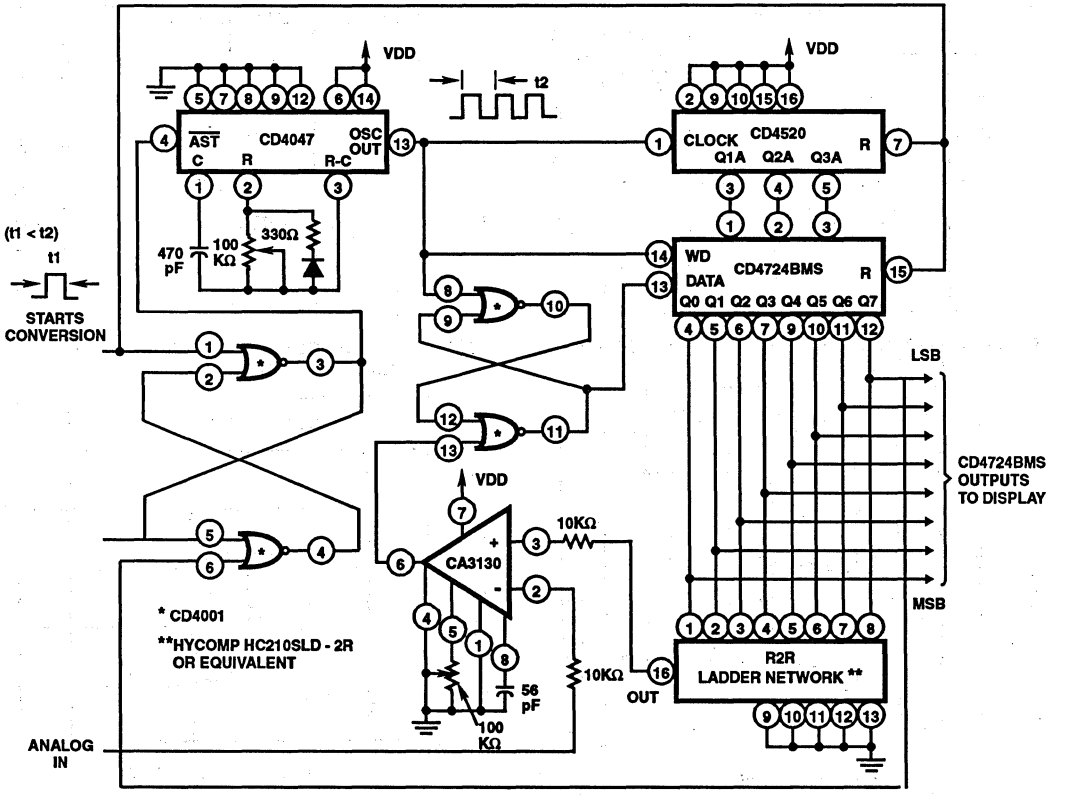


FIGURE 9. A/D CONVERTER

MODE SELECTION			
WD	R	ADDRESSED LATCH	UNADDRESSED LATCH
0	0	Follows Data	Holds Previous State
0	1	Follows Data (Active High 8-Channel Demultiplexer)	Reset to "0"
1	0	Holds Previous State	
1	1	Reset to "0"	Reset to "0"

WD = Write Disable R = Reset

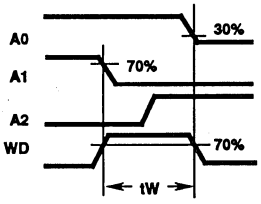


FIGURE 10. DEFINITION OF WRITE DISABLE ON TIME

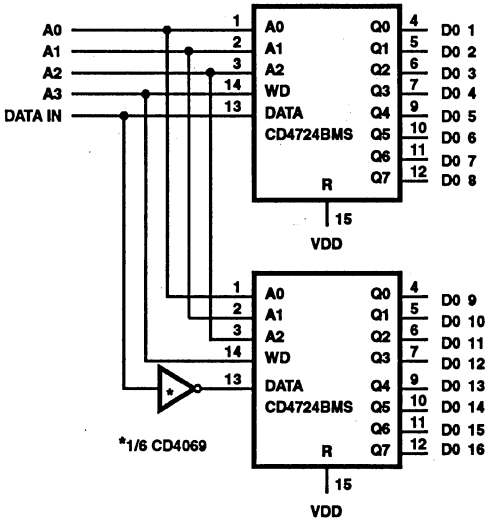


FIGURE 11. 1 OF 16 DECODER/DEMULTIPLEXER

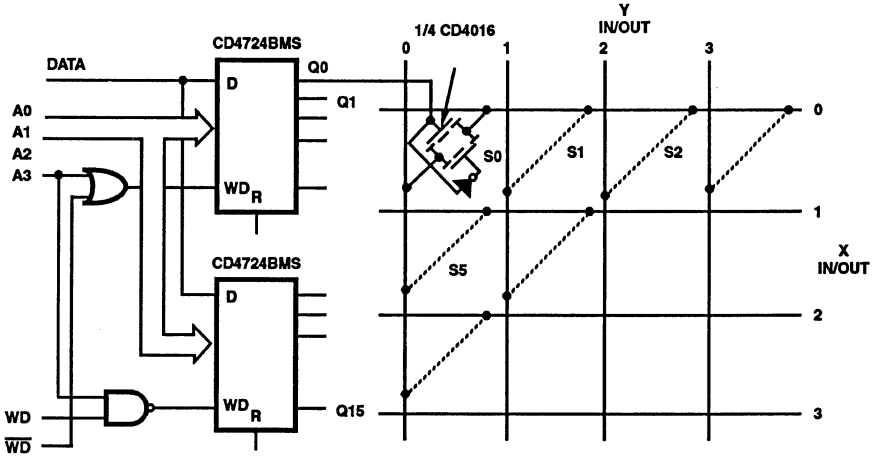
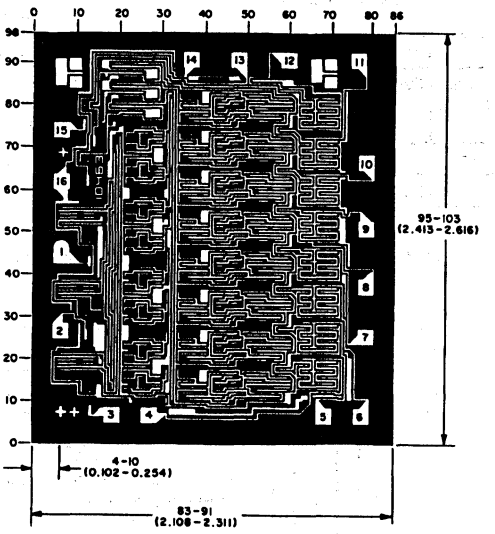


FIGURE 12. MULTIPLE SELECTION DECODING - 4 X 4 CROSSPOINT SWITCH

Chip Dimensions and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD40100BMS

CMOS 32-Stage Static Left/Right Shift Register

December 1992

Features

- High Voltage Type (20V Rating)
- Fully Static Operation
- Shift Left/Shift Right Capability
- Multiple Package Cascading
- Recirculate Capability
- LIFO of FIFO Capability
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Standardized, Symmetrical Output Characteristics
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Serial Shift Registers
- Time Delay Circuits
- Expandable N-Bit Data Storage Stack (LIFO Operation)

Description

CD40100BMS is a 32-Stage shift register containing 32 D-type master-slave flip-flops.

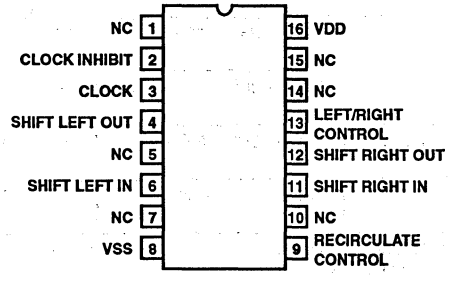
The data present at the SHIFT RIGHT INPUT is transferred into the first register stage synchronously with the positive CLOCK edge, provided the LEFT/RIGHT CONTROL is at a low level, the RECIRCULATE CONTROL is at a high level, and the CLOCK INHIBIT is low. If the LEFT/RIGHT CONTROL is at a high level and the RECIRCULATE CONTROL is also high, data at the SHIFT LEFT INPUT is transferred into the 32nd register stage synchronously with the positive CLOCK transition, provided the CLOCK INHIBIT is low. The state of the LEFT/RIGHT CONTROL, RECIRCULATE CONTROL, and CLOCK INHIBIT should not be changed when the CLOCK is high.

Data is shifted one stage left or one stage right depending on the state of the LEFT/RIGHT CONTROL, synchronously with the positive CLOCK edge. Data clocked into the first or 32nd register states is available at the SHIFT LEFT or SHIFT RIGHT OUTPUT respectively, on the next negative CLOCK transition (see Data Transfer Table). No shifting occurs on the positive CLOCK edge if the CLOCK INHIBIT line is at a high level. With the RECIRCULATE CONTROL low, data in the 32nd stage is shifted into the first stage when the LEFT/RIGHT CONTROL is low and from the first stage to the 32nd stage when the LEFT/RIGHT CONTROL is low, and from the first state to the 32nd stage when the LEFT/RIGHT control is high. The CD40100BMS is supplied in these 16-lead outline packages:

Braze Seal DIP	H4T
Frit Seal DIP	H2R
Ceramic Flatpack	H6W

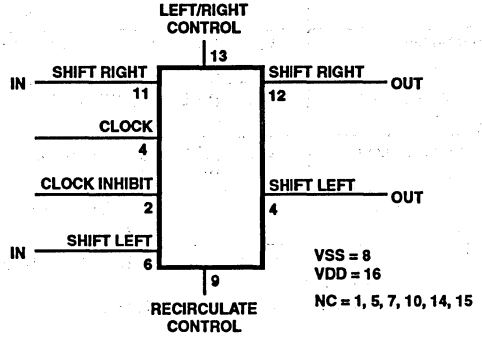
Pinout

CD40100BMS
TOP VIEW



NC = NO CONNECTION

Functional Diagram



7 LOGIC

File Number 3349

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Shift Left/Right Output	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	720	ns
			10, 11	+125°C, -55°C	-	972	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	1	-	MHz
			10, 11	+125°C, -55°C	.74	-	MHz

NOTES:

1. VDD = 5V, CL = 50pF, RL = 200K
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Clock to Shift Left/Right Output	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	330	ns
		VDD = 15V	1, 2, 3	+25°C	-	230	ns
Transition Time	TTHL	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	2.5	-	MHz
		VDD = 15V	1, 2, 3	+25°C	3	-	MHz
Minimum Data Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	100	ns
		VDD = 10V	1, 2, 3	+25°C	-	20	ns
		VDD = 15V	1, 2, 3	+25°C	-	10	ns
Minimum Data Hold Time	TH	VDD = 5V	1, 2, 3	+25°C	-	275	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	75	ns
Minimum Clock Pulse Width Low Level	TWL	VDD = 5V	1, 2, 3	+25°C	-	450	ns
		VDD = 10V	1, 2, 3	+25°C	-	230	ns
		VDD = 15V	1, 2, 3	+25°C	-	190	ns
Minimum Clock Pulse Width High Level	TWH	VDD = 5V	1, 2, 3	+25°C	-	280	ns
		VDD = 10V	1, 2, 3	+25°C	-	150	ns
		VDD = 15V	1, 2, 3	+25°C	-	140	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading
ON Resistance	RONDEL10	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	1, 4, 5, 7, 10, 12, 14, 15	2, 3, 6, 8, 9, 11, 13	16			
Static Burn-In 2 Note 1	1, 4, 5, 7, 10, 12, 14, 15	8	2, 3, 6, 9, 11, 13, 16			
Dynamic Burn-In Note 1	1, 5, 7, 10, 14, 15	2, 8, 13	9, 16	4, 12	3	6, 11

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS (Continued)

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Irradiation Note 2	1, 4, 5, 7, 10, 12, 14, 15	8	2, 3, 6, 9, 11, 13, 16			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

TABLE 9. DATA TRANSFER TABLE*

INITIAL STATE			CLOCK	RESULTING STATE	
DATA INPUT	CLOCK INHIBIT	INTERNAL STAGE	LEVEL CHANGE	INTERNAL STAGE Q	OUTPUT
0	0	X	⌐‾	0	NC
X	0	0	‾⌐	NC	0
1	0	X	⌐‾	1	NC
X	0	1	‾⌐	NC	1
X	1	1	X	NC	NC

0 = Low Level 1 = High Level X = Don't Care NC = No Change

* For Shift-Right Mode
Data Input = SHIFT RIGHT INPUT (Term. 11)
Internal Stage = Stage 1 (Q1)
Output = SHIFT LEFT OUTPUT (Term. 4)

For Shift Left Mode
Data Input = SHIFT LEFT INPUT (Term. 6)
Internal Stage = Stage 32 (Q32)
Output = SHIFT RIGHT OUTPUT (Term. 12)

TABLE 10. CONTROL TRUTH TABLE

LEFT/RIGHT CONTROL	CLOCK INHIBIT	RECIRCULATE CONTROL	ACTION	INPUT BIT ORIGIN
1	0	1	Shift Left	Shift Left Input
1	0	0	Shift Left	Stage 1
0	0	1	Shift Right	Shift Right Input
0	0	0	Shift Right	Stage 32
X	1	X	No Shift	-

Logic Diagram

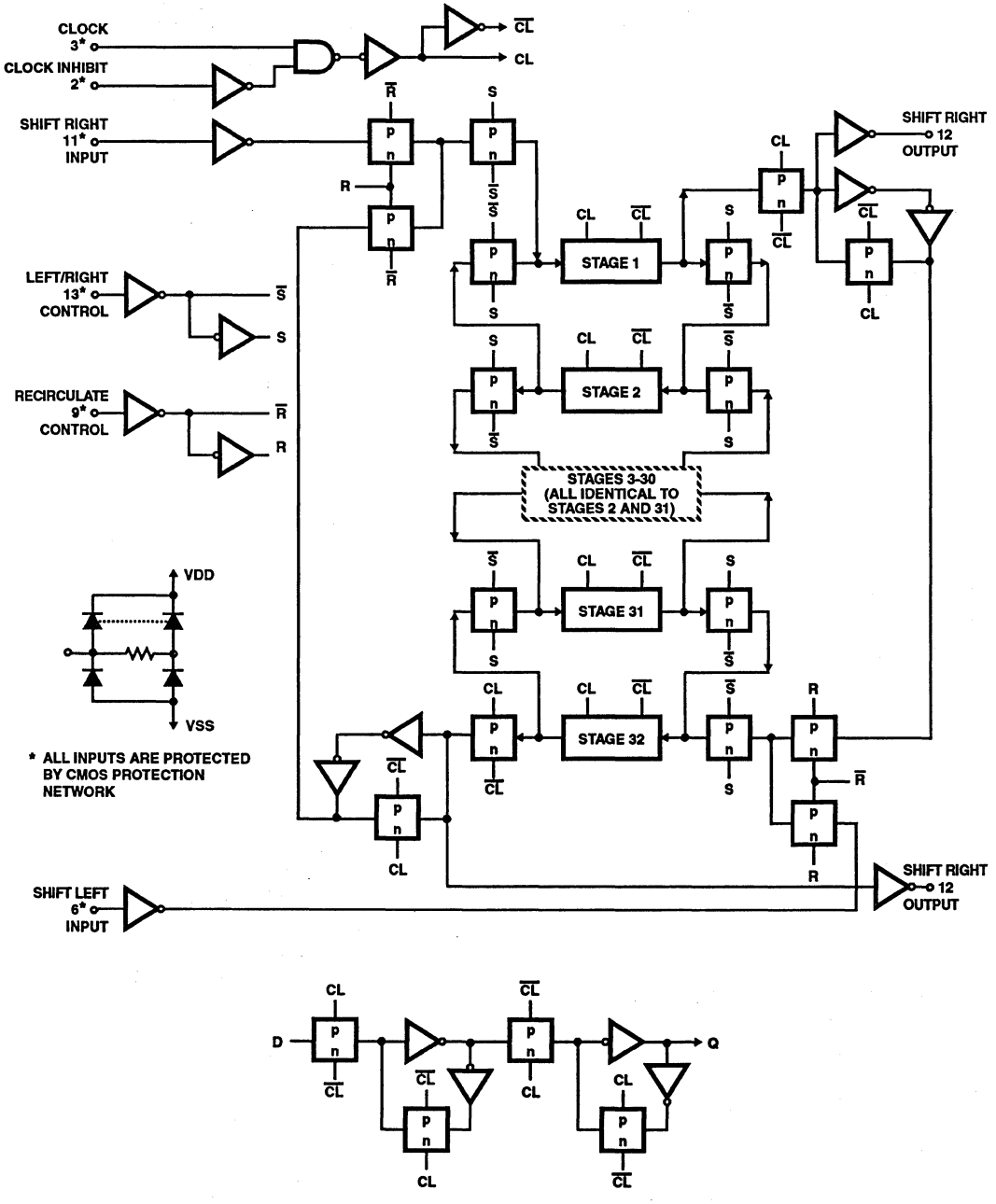


FIGURE 1.

Typical Performance Characteristics

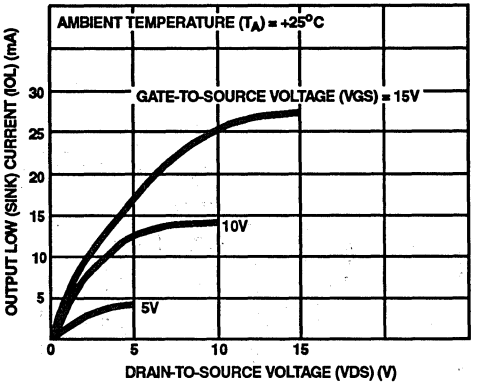


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

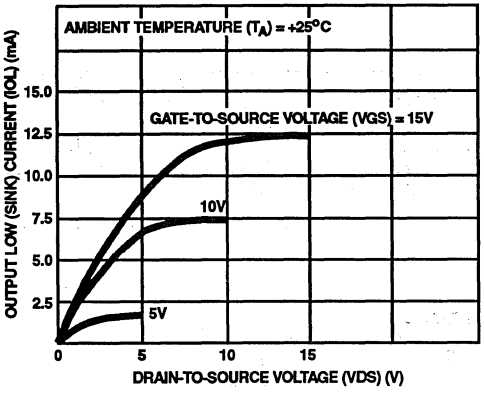


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

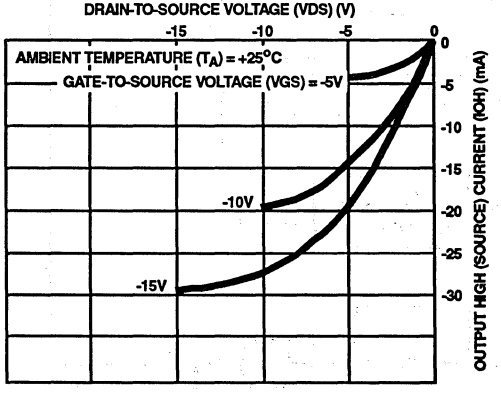


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

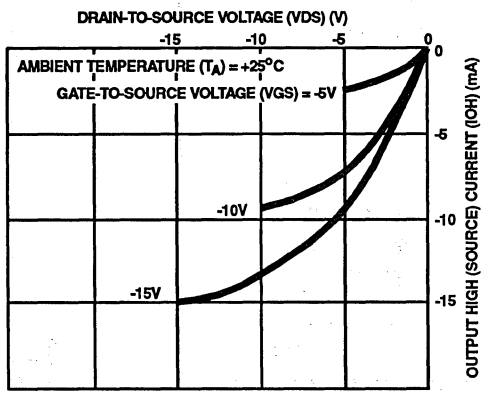


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

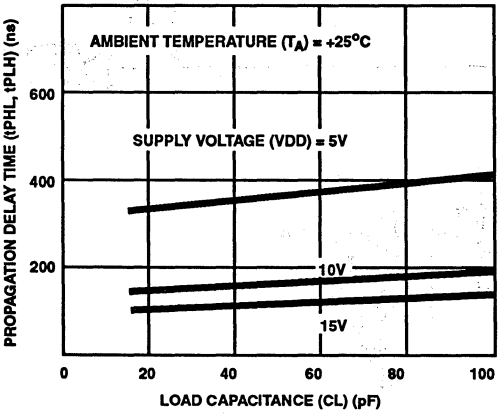


FIGURE 6. TYPICAL PROPAGATION DELAY TIME (CLOCK TO SHIFT LEFT/RIGHT) AS A FUNCTION OF LOAD CAPACITANCE

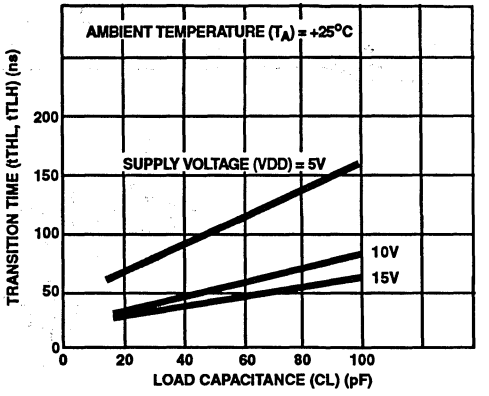


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

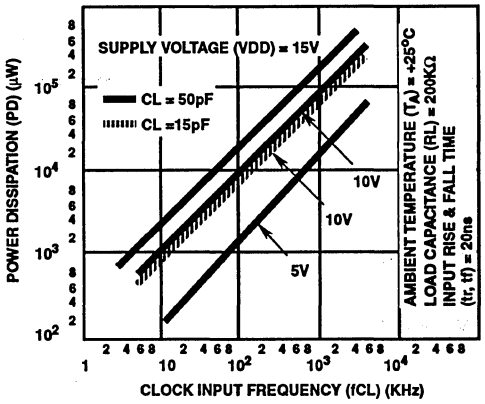


FIGURE 8. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF CLOCK FREQUENCY

Timing Diagram

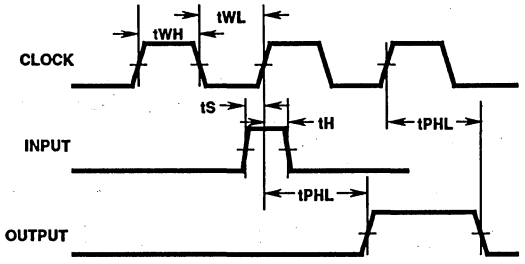
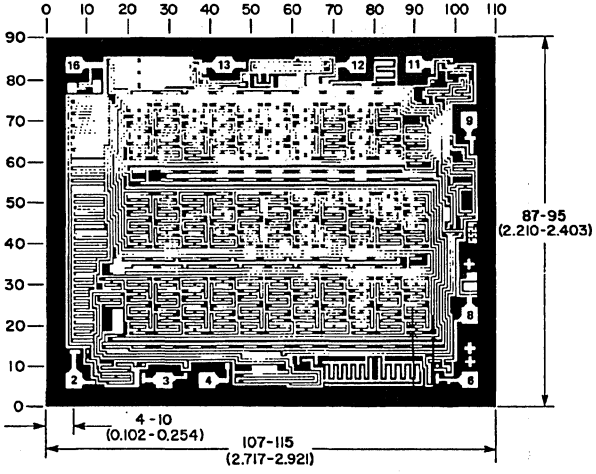


FIGURE 9. TIMING DIAGRAM DEFINING SETUP, HOLD, AND PROPAGATION DELAY TIMES

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD40101BMS

December 1992

CMOS 9-Bit Parity Generator/Checker

Features

- High Voltage Type (20V Rating)
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Standardized Symmetrical Output Characteristics
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Description

The CD40101BMS is a 9-bit (8 data bits plus 1 parity bit) parity generator/checker. It may be used to detect errors in data transmission or data retrieval. Odd and even outputs facilitate odd or even parity generation and checking.

When used as a parity generator, a parity bit is supplied along with the data to generate an even or odd parity output.

When used as a parity checker, the received data bits and parity bits are compared for correct parity. The even or odd outputs are used to indicate an error in the received data.

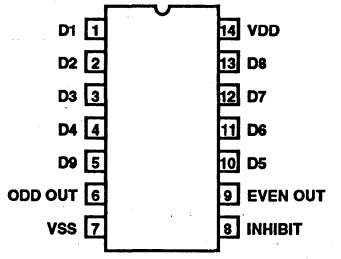
Word length capability is expandable by cascading. The CD40101BMS is also provided with an inhibit control. If the inhibit control is set at logical "1", the even and odd outputs go to a logical "0".

The CD40101BMS is supplied in these 14 lead outline packages:

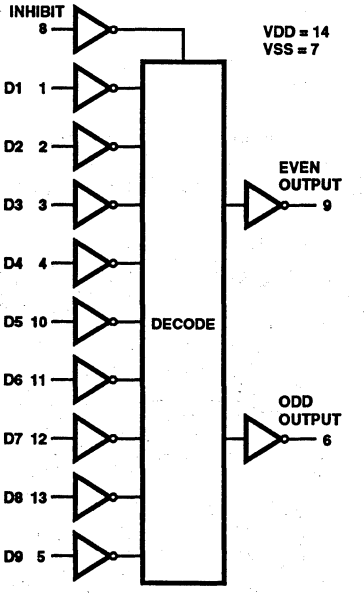
Braze Seal DIP	H4H
Frit Seal DIP	H1B
Ceramic Flatpack	H3W

Pinout

CD40101BMS
TOP VIEW



Functional Diagram



Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering)..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Data-In To Output	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	700	ns
			10, 11	+125°C, -55°C	-	945	ns
Propagation Delay Inhibit-In to Output	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	280	ns
			10, 11	+125°C, -55°C	-	378	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Data to Output	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	300	ns
		VDD = 15V	1, 2, 3	+25°C	-	200	ns
Propagation Delay Inhibit to Output	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	140	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Transition Time	TTLH TTHL	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

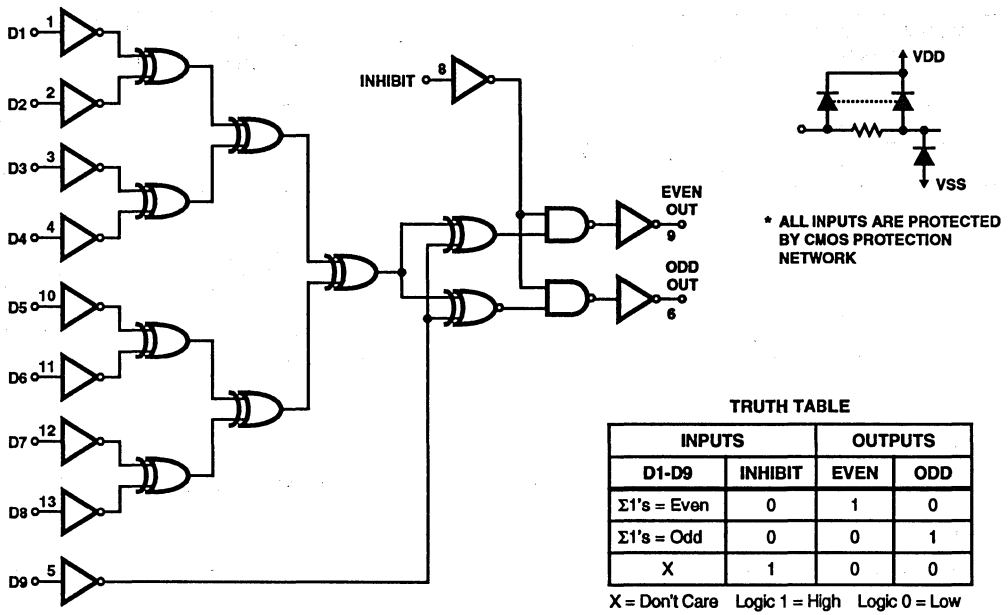
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	6, 9	1-5, 7, 8, 10-13	14			
Static Burn-In 2 Note 1	6, 9	7	1-5, 8, 10-14			
Dynamic Burn-In Note 1	-	4, 7	12, 14	6, 9	2, 3, 5, 8, 10	1, 11, 13
Irradiation Note 2	6, 9	7	1-5, 8, 10-14			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram



TRUTH TABLE

INPUTS		OUTPUTS	
D1-D9	INHIBIT	EVEN	ODD
Σ1's = Even	0	1	0
Σ1's = Odd	0	0	1
X	1	0	0

X = Don't Care Logic 1 = High Logic 0 = Low

FIGURE 1.

Typical Performance Characteristics

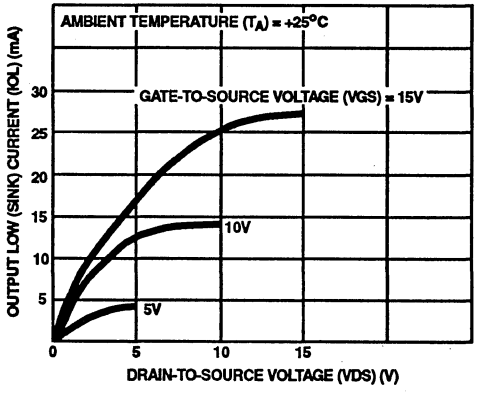


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

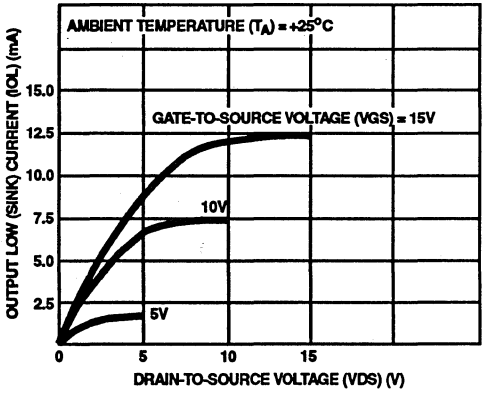


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

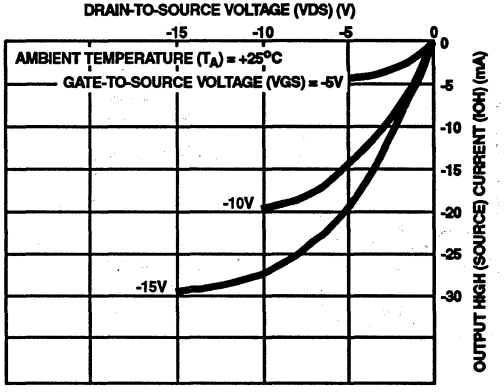


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

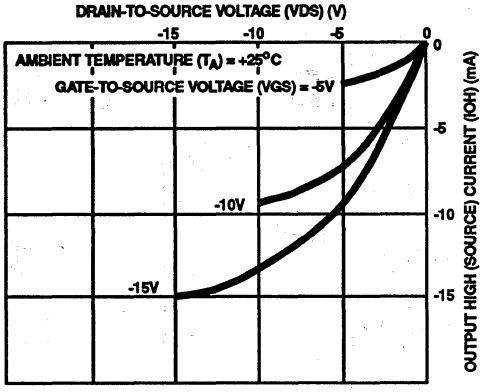


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

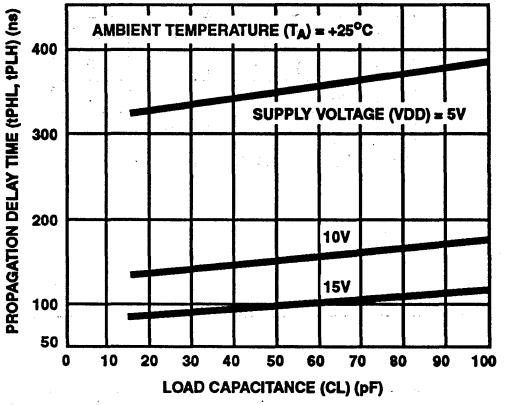


FIGURE 6. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

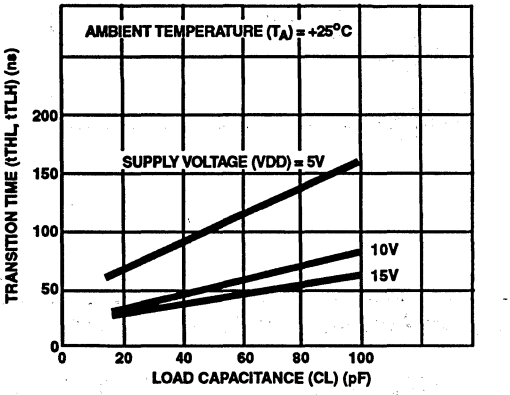


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

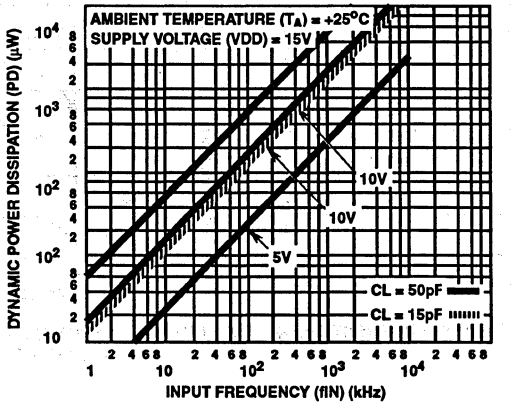
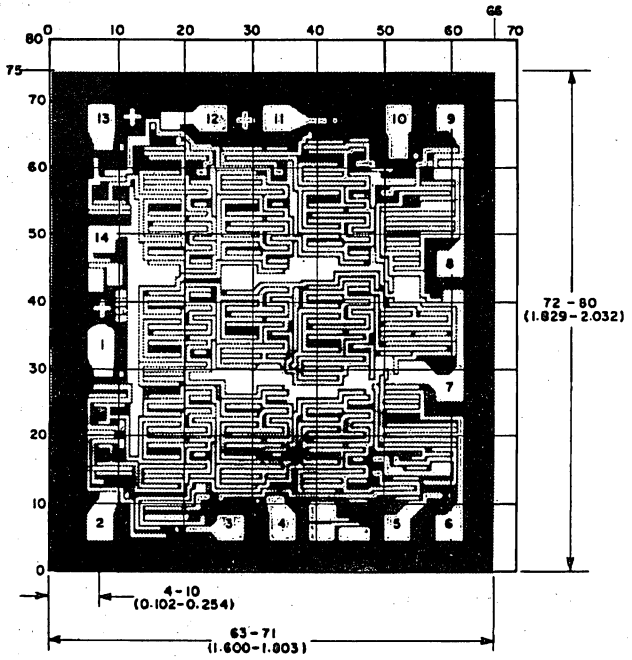


FIGURE 8. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD40102BMS CD40103BMS

CMOS 8-Stage Presettable Synchronous Down Counters

December 1992

Features

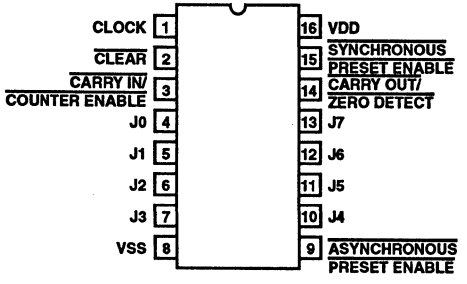
- High Voltage Type (20V Rating)
- CD40102BMS: 2-Decade BCD Type
- CD40103BMS: 8-Bit Binary Type
- Synchronous or Asynchronous Preset
- Medium Speed Operation
  - fCL = 3.6MHz (Typ) at 10V
- Cascadable
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Standardized Symmetrical Output Characteristics
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Divide-By- "N" Counters
- Programmable Times
- Interrupt Timers
- Cycle/Program Counter

Pinout

CD40102BMS, CD40130BMS
TOP VIEW



Description

CD40102BMS and CD40103BMS consist of an 8-stage synchronous down counter with a single output which is active when the internal count is zero. The CD40102BMS is configured as two cascaded 4-bit BCD counters, and the CD40103BMS contains a single 8-bit binary counter. Each type has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the CARRY-OUT/ZERO-DETECT output are active-low logic.

In normal operation, the counter is decremented by one count on each positive transition of the CLOCK. Counting is inhibited when the CARRY-IN/COUNTER ENABLE ($\overline{CI/CE}$) inputs is high. The CARRY-OUT/ZERO-DETECT ($\overline{CO/ZD}$) output goes low when the count reaches zero if the $\overline{CI/CE}$ input is low, and remains low for one full clock period.

When the SYNCHRONOUS PRESET-ENABLE ($\overline{SPE}$) input is low, data at the JAM input is clocked into the counter on the next positive clock transition regardless of the state of the $\overline{CI/CE}$ input. When the ASYNCHRONOUS PRESET-ENABLE ($\overline{APE}$) input is low, data at the JAM inputs is asynchronously forced into the counter regardless of the state of the $\overline{SPE}$, $\overline{CI/CE}$, or CLOCK inputs. JAM inputs J0-J7 represent two 4-bit BCD words for the CD40102BMS and a single 8-bit binary word for the CD40103BMS.

When the CLEAR ($\overline{CLR}$) input is low, the counter is asynchronously cleared to its maximum count (99_{10} for the CD40102BMS and 255_{10} for the CD40103BMS) regardless of the state of any other input. The precedence relationship between control inputs is indicated in the truth table.

If all control inputs except $\overline{CI/CE}$ are high at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 100 or 256 clock pulses long.

This causes the $\overline{CO/ZD}$ output to go low to enable the clock on each succeeding clock pulse.

The CD40102BMS and CD40103BMS may be cascaded using the $\overline{CI/CE}$ input and the $\overline{CO/ZD}$ output, in either a synchronous or ripple mode as shown in Figures 16 and 17.

The CD40102MS and CD40103BMS are supplied in these 16-lead outline packages:

Braze Seal DIP	*H4W	†H4X
Frit Seal DIP	*H1L	†H1F
Ceramic Flatpack	H6W	

*CD40102B Only †CD40130B Only

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3351

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range.....-55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG).....-65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K).....500mW
For T_A = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature .....+175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20V	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20V	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Output	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Propagation Delay Carry In/Counter Enable to Output	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay Asynchronous Preset Enable to Output	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	1300	ns
			10, 11	+125°C, -55°C	-	1755	ns
Propagation Delay $\overline{\text{Clear}}$ to Output	TPLH4	VDD = 5V, VIN = VDD or GND	9	+25°C	-	750	ns
			10, 11	+125°C, -55°C	-	1012	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	.7	-	MHz
			10, 11	+125°C, -55°C	.52	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Clock to Output	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	260	ns
		VDD = 15V	1, 2, 3	+25°C	-	190	ns
Propagation Delay Carry In/Counter Enable to Output	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	180	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Propagation Delay Asynchronous Preset Enable to Output	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25°C	-	600	ns
		VDD = 15V	1, 2, 3	+25°C	-	400	ns
Propagation Delay $\overline{\text{Clear}}$ to Output	TPLH4	VDD = 10V	1, 2, 3	+25°C	-	360	ns
		VDD = 15V	1, 2, 3	+25°C	-	200	ns
Transition Time	TTHL1 TTLH1	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2	+25°C	1.8	-	MHz
		VDD = 15V	1, 2	+25°C	2.4	-	MHz
Minimum $\overline{\text{SPE}}$ Setup Time	TSU	VDD = 5V	1, 2, 3	+25°C	-	280	ns
		VDD = 10V	1, 2, 3	+25°C	-	140	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Minimum $\overline{\text{CI/CE}}$ Setup Time	TSU	VDD = 5V	1, 2, 3	+25°C	-	500	ns
		VDD = 10V	1, 2, 3	+25°C	-	250	ns
		VDD = 15V	1, 2, 3	+25°C	-	150	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	300	ns
		VDD = 10V	1, 2, 3	+25°C	-	180	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Minimum $\overline{\text{APE}}$ Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	360	ns
		VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Minimum JAM Setup Time (Synchronous Presetting)	TSU	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Minimum $\overline{\text{APE}}$ Removal Time	TREM	VDD = 5V	1, 2, 3	+25°C	-	220	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	70	ns
Minimum $\overline{\text{CLR}}$ Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	320	ns
		VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Final Test	100% 5004	2, 3, 8A, 8B, 10, 11	
Group A	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

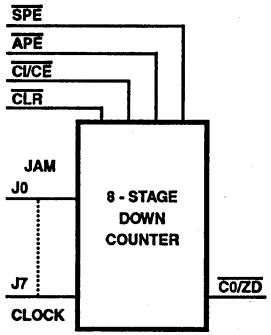
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
PART NUMBER CD40102BMS, CD40103BMS						
Static Burn-In 1 Note 1	14	1 - 13, 15	16			
Static Burn-In 2 Note 1	14	8	1 - 7, 9 - 13, 15, 16			
Dynamic Burn-In Note 1	-	3, 8, 15	2, 16	14	1, 4, 6, 11, 13	5, 7, 9, 10, 12
Irradiation Note 2	-					

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Functional Diagram



CD40102BMS, CD40103BMS

Logic Diagrams

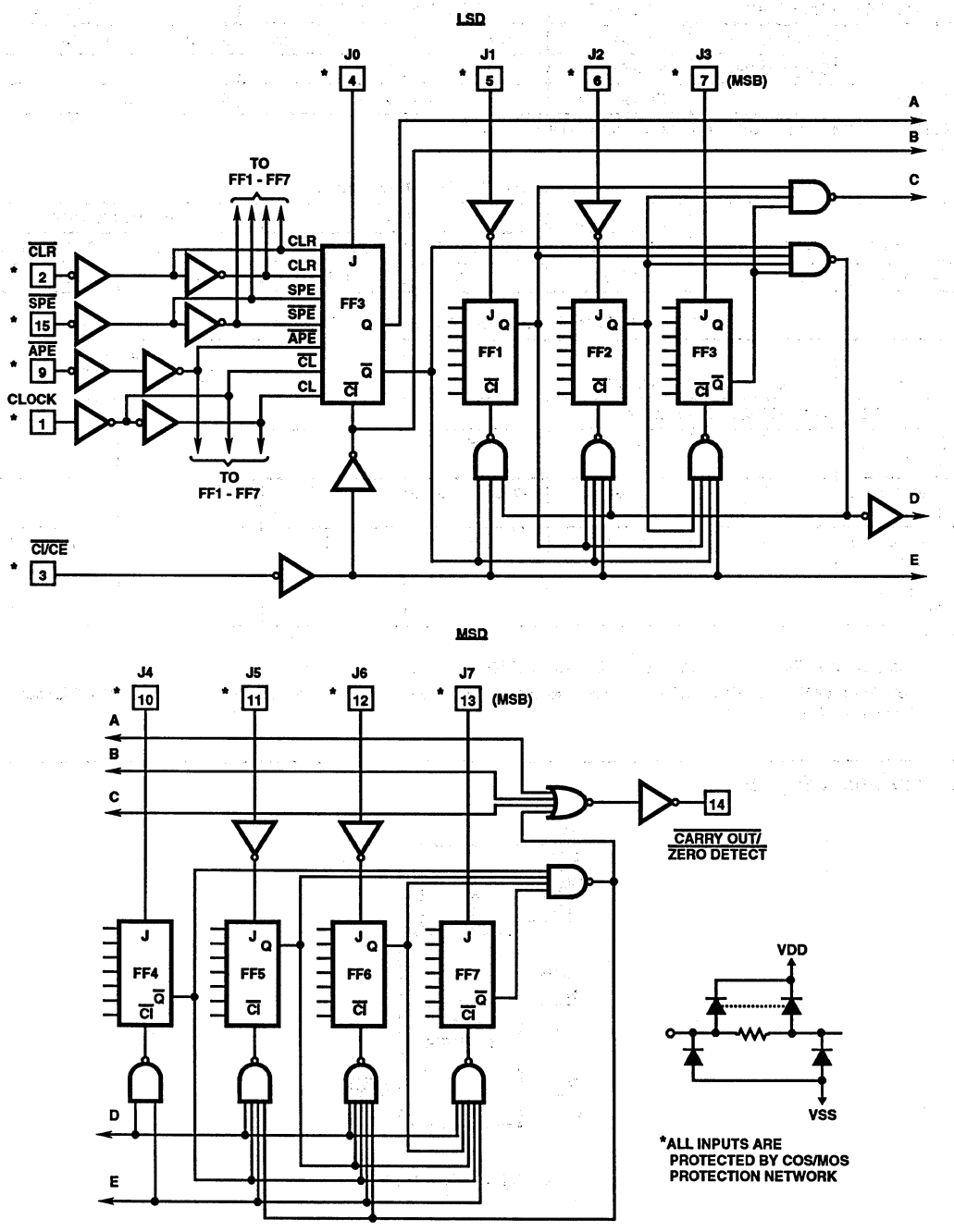


FIGURE 1. LOGIC DIAGRAM FOR CD40102BMS

Logic Diagrams (Continued)

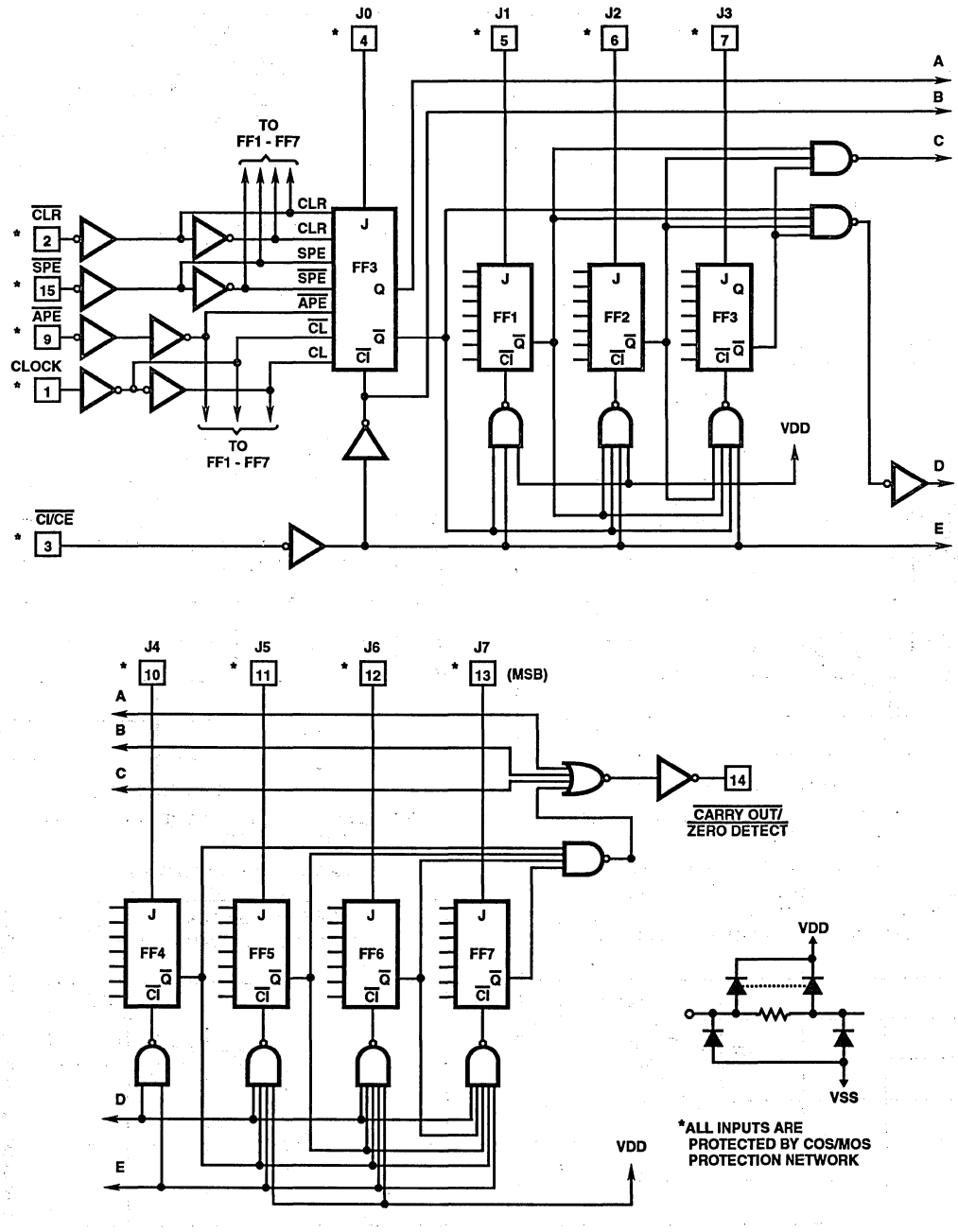


FIGURE 2. LOGIC DIAGRAM FOR CD40103BMS

TRUTH TABLE

CONTROL INPUTS					
$\overline{CLR}$	$\overline{APE}$	$\overline{SPE}$	$\overline{CI/CE}$	PRESET MODE	ACTION
1	1	1	1	Synchronous	Inhibit Counter
1	1	1	0		Count Down*
1	1	0	X		Preset on next positive clock transition
1	0	X	X	Asynchronous	Preset Asynchronously
0	X	X	X		Clear to maximum count

NOTES:

1. 0 = Low Level
   1 = High Level
   X = Don't Care
2. Clock connected to clock input
3. Synchronous operation: changes occur on negative-to-positive clock transitions
4. JAM inputs: CD40102BMS;
   MSD = J7, J6, J5, J4, (J7 is MSB)
   LSD = J3, J2, J1, J0 (J3 is MSB)
   CD40103BMS Binary;
   MBS = J7, LSB = J0

*At zero count, the counters will jump to the maximum count on the next clock transition to "High"

Typical Performance Characteristics

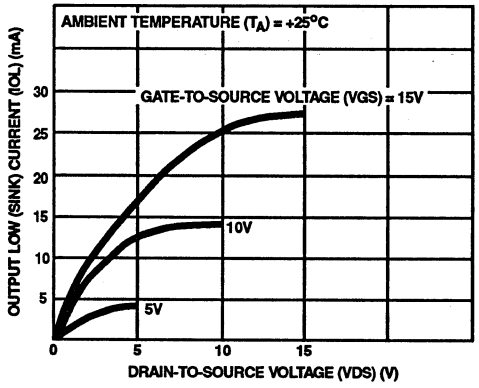


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

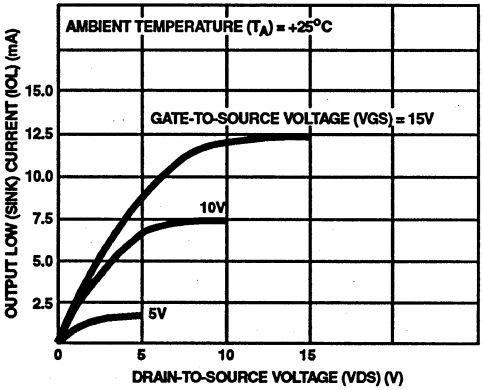


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

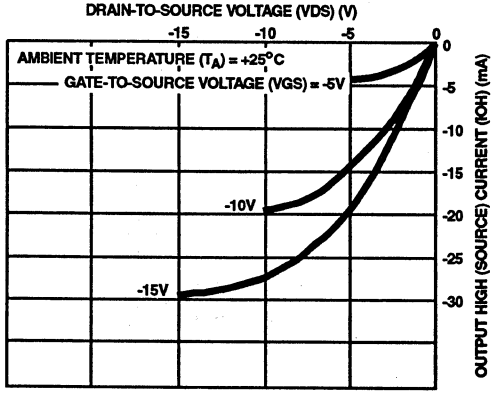


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

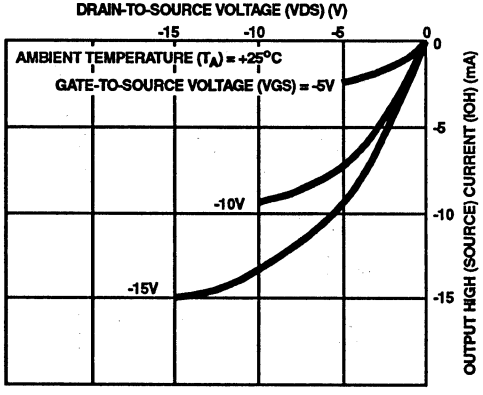


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

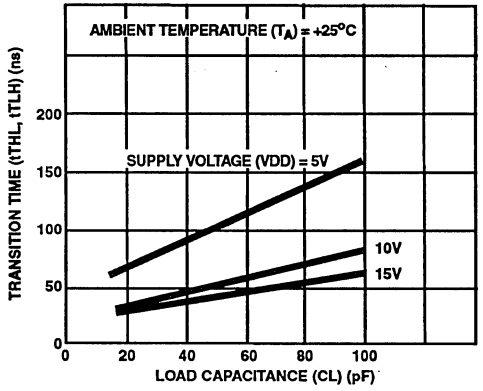


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

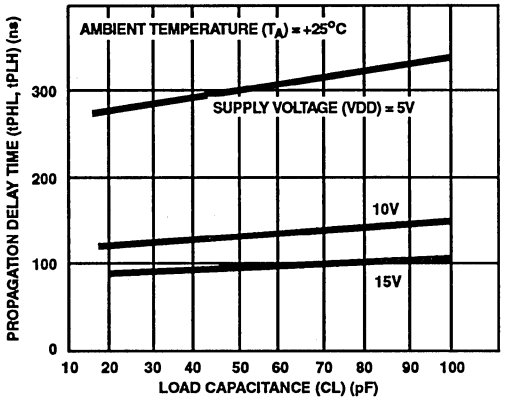


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (CLOCK TO $\overline{CO/ZD}$)

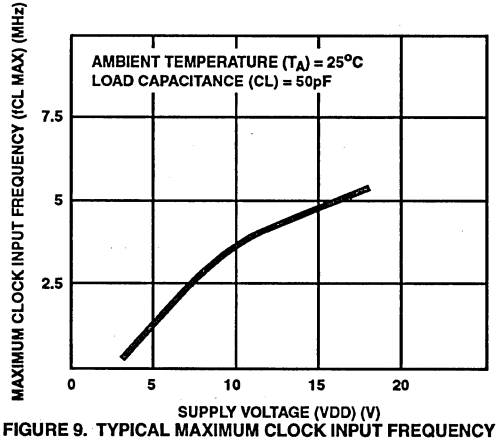


FIGURE 9. TYPICAL MAXIMUM CLOCK INPUT FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

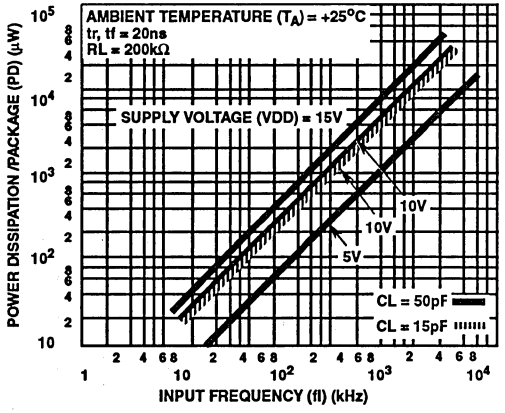


FIGURE 10. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF FREQUENCY

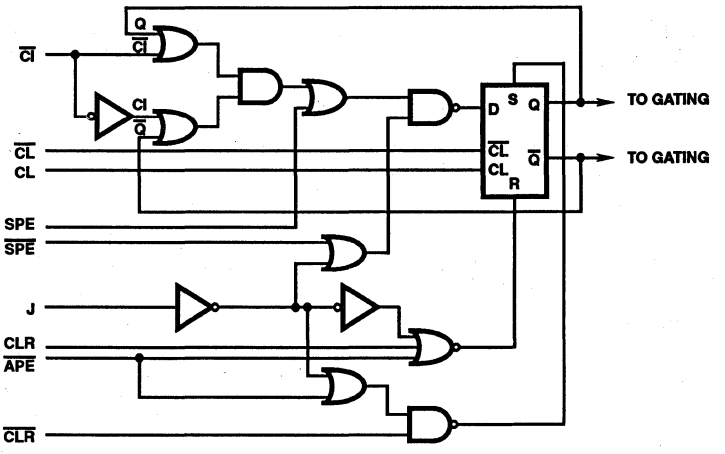


FIGURE 11. DETAIL LOGIC DIAGRAM FOR FLIP-FLOPS, FF0 - FF7, USED IN LOGIC DIAGRAMS FOR CD40102BMS AND CD40103BMS

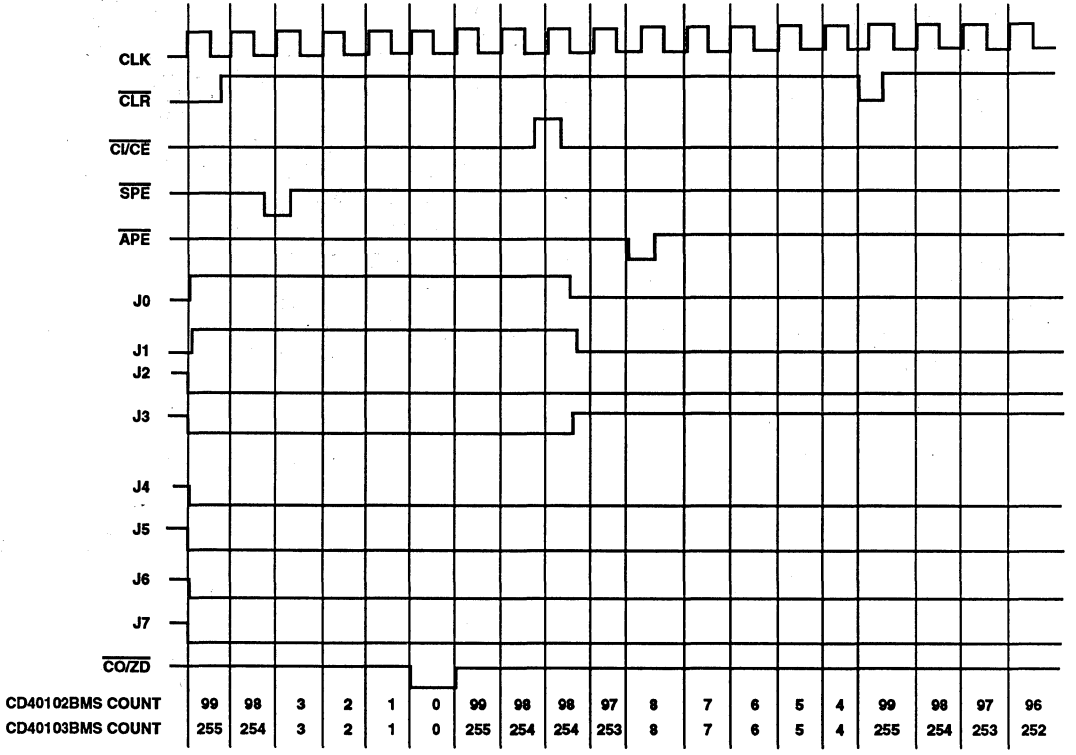


FIGURE 12. TIMING DIAGRAM FOR CD40102BMS AND CD40103BMS

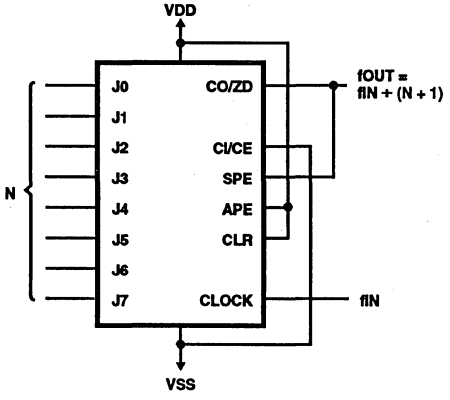


FIGURE 13. DIVIDE-BY- "N" COUNTER

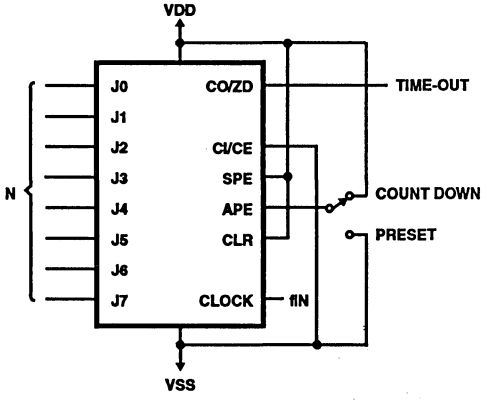


FIGURE 14. PROGRAMMABLE TIMER

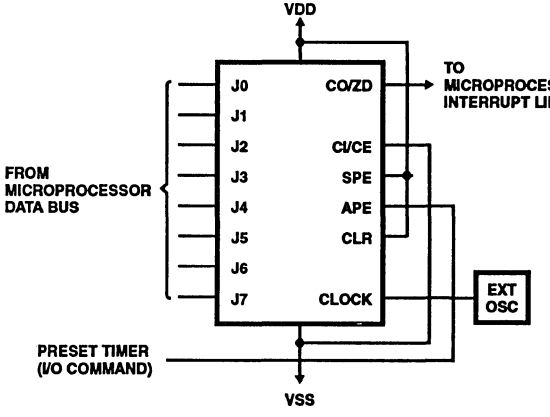
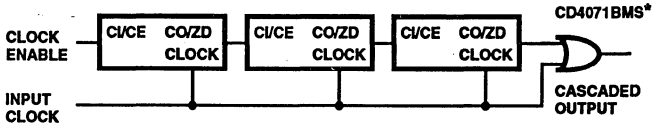


FIGURE 15. MICROPROCESSOR INTERRUPT TIMER



*An output spike (160ns at VDD = 5V) occurs whenever two or more devices are cascaded in the parallel-clocked mode because the clock-to-carry out delay is greater than the carry-in-to-carry out delay. This spike is eliminated by gating the output of the last device with the clock as shown.

FIGURE 16. SYNCHRONOUS CASCADING

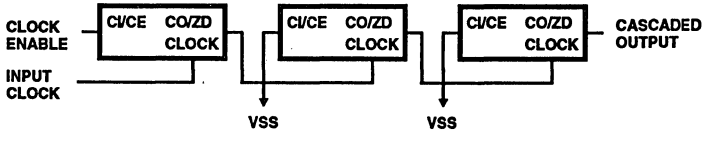
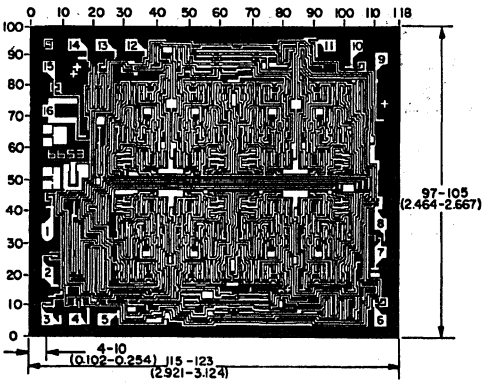
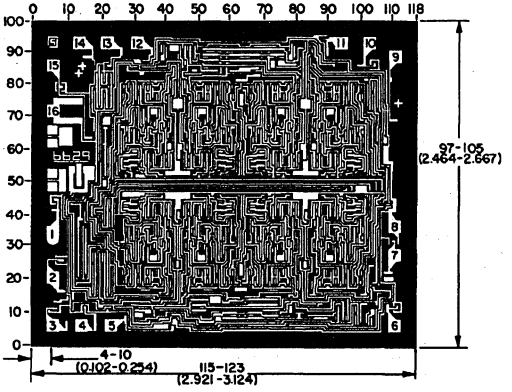


FIGURE 17. RIPPLE CASCADING

Chip Dimensions and Pad Layouts



CD40102BMS



CD40103BMS

Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10-3 inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD40104BMS
CD40194BMS

CMOS 4-Bit Bidirectional Universal Shift Register

December 1992

Features

- High Voltage Type (20V Rating)
- Medium Speed fCL = 12MHz (typ.) at VDD = 10V
- Fully Static Operation
- Synchronous Parallel or Serial Operation
- Three State Outputs (CD40104BMS)
- Asynchronous Master Reset (CD40194BMS)
- 5V, 10V and 15V Parametric Ratings
- Standardized Symmetrical Output Characteristics
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Arithmetic Unit Bus Registers
- Serial/Parallel Conversions
- General Purpose Register for Bus Organized Systems
- General Purpose Registers

Description

The CD40104BMS is a universal shift register featuring parallel inputs, parallel outputs, SHIFT RIGHT and SHIFT LEFT serial inputs, and a high impedance third output state allowing the device to be used in bus organized systems.

In the parallel load mode (S0 and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift right and shift left are accomplished synchronously on the positive clock edge with serial data entered at the SHIFT RIGHT and SHIFT LEFT serial inputs, respectively. Clearing the register is accomplished by setting both mode controls low and clocking the register. When the output enable input is low, all outputs assume the high impedance state.

The CD40194BMS is a universal shift register featuring parallel inputs, parallel outputs SHIFT RIGHT and SHIFT LEFT serial inputs, and a direct overriding clear input. In the parallel load mode (S0 and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift right and shift left are accomplished synchronously on the positive clock edge with data entered at the SHIFT RIGHT and SHIFT LEFT serial inputs, respectively. Clocking of the register is inhibited when both mode control inputs are low. When low, the $\overline{\text{RESET}}$ input resets all stages and forces all outputs low. The CD40194BMS is similar to industry types 340194 and MC40194.

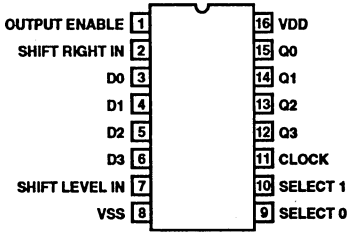
The CD40104BMS and CD40194BMS series types are supplied in these 16 lead outline packages

Braze Seal DIP	*HNX,	†H4W
Frit Seal DIP	*H1L,	†HIF
Ceramic Flatpack	H6W	

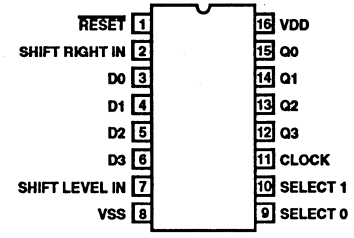
* CD40104B Only †CD40194B Only

Pinouts

CD40104BMS
TOP VIEW

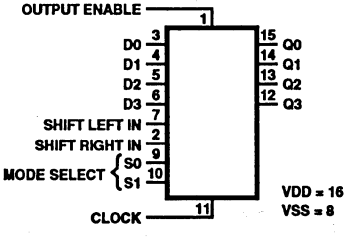


CD40194BMS
TOP VIEW

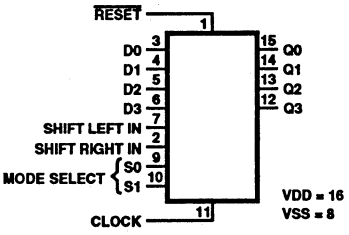


Functional Diagrams

CD40104BMS



CD40194BMS



7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3352

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

	θ_{ja}	θ_{jc}
Thermal Resistance		
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20V	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20V	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.4	-	µA
				2	+125°C	-12	-	µA
			VDD = 18V	3	-55°C	-0.4	-	µA
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.4	µA
				2	+125°C	-	12	µA
			VDD = 18V	3	-55°C	-	0.4	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Q	TPHL TPLH	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	440	ns
			10, 11	+125°C, -55°C	-	594	ns
Propagation Delay CD40194BMS Reset to Q	TPHL	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	460	ns
			10, 11	+125°C, -55°C	-	621	ns
Propagation Delay CD40104BMS 3-State	TPZH TPZL TPLZ	VDD = 5V, VIN = VDD or GND (Note 2, 3)	9	+25°C	-	160	ns
			10, 11	+125°C, -55°C	-	216	ns
Propagation Delay CD40104BMS 3-State	TPHZ	VDD = 5V, VIN = VDD or GND (Note 2, 3)	9	+25°C	-	90	ns
			10, 11	+125°C, -55°C	-	122	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	3	-	MHz
			10, 11	+125°C, -55°C	2.22	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.
3. VDD = 5V, CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Clock to Q	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	140	ns
Propagation Delay CD40194B Reset to Q	TPLH TPHL	VDD = 10V	1, 2, 3	+25°C	-	180	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Propagation Delay CD40104BMS 3-State	TPZH TPZL TPLZ	VDD = 10V	1, 2, 3, 4	+25°C	-	70	ns
		VDD = 15V	1, 2, 3, 4	+25°C	-	50	ns
Propagation Delay CD40104BMS 3-State	TPHZ	VDD = 10V	1, 2, 4	+25°C	-	50	ns
		VDD = 15V	1, 2, 4	+25°C	-	40	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Minimum Data Setup Time, D0, D3, SRIN, SLIN to Clock	TS	VDD = 5V	1, 2, 3	+25°C	-	100	ns
		VDD = 10V	1, 2, 3	+25°C	-	70	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Data Hold Time D0, D3, SRIN, SLIN to Clock	TH	VDD = 5V	1, 2, 3	+25°C	-	0	ns
		VDD = 10V	1, 2, 3	+25°C	-	0	ns
		VDD = 15V	1, 2, 3	+25°C	-	0	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	180	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Maximum Clock Rise and Fall Time	TRCL TFCL	VDD = 5V	1, 2, 3, 5	+25°C	3	-	µs
		VDD = 10V	1, 2, 3, 5	+25°C	6	-	µs
		VDD = 15V	1, 2, 3, 5	+25°C	8	-	µs
Minimum Data Setup Time Select 1, Select 0 to Clock	TS	VDD = 5V	1, 2, 3	+25°C	-	400	ns
		VDD = 10V	1, 2, 3	+25°C	-	220	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Minimum Data Hold Time Select 1, Select 0 to Clock	TH	VDD = 5V	1, 2, 3	+25°C	-	0	ns
		VDD = 10V	1, 2, 3	+25°C	-	0	ns
		VDD = 15V	1, 2, 3	+25°C	-	0	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Minimum Reset Pulse Width CD40194BMS	TW	VDD = 5V	1, 2, 3	+25°C	-	300	ns
		VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	140	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. CL = 50pF, RL = 1K, Input TR, TF < 20ns.
5. If more than one unit is cascaded, TRCL should be made less than or equal to the sumof the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

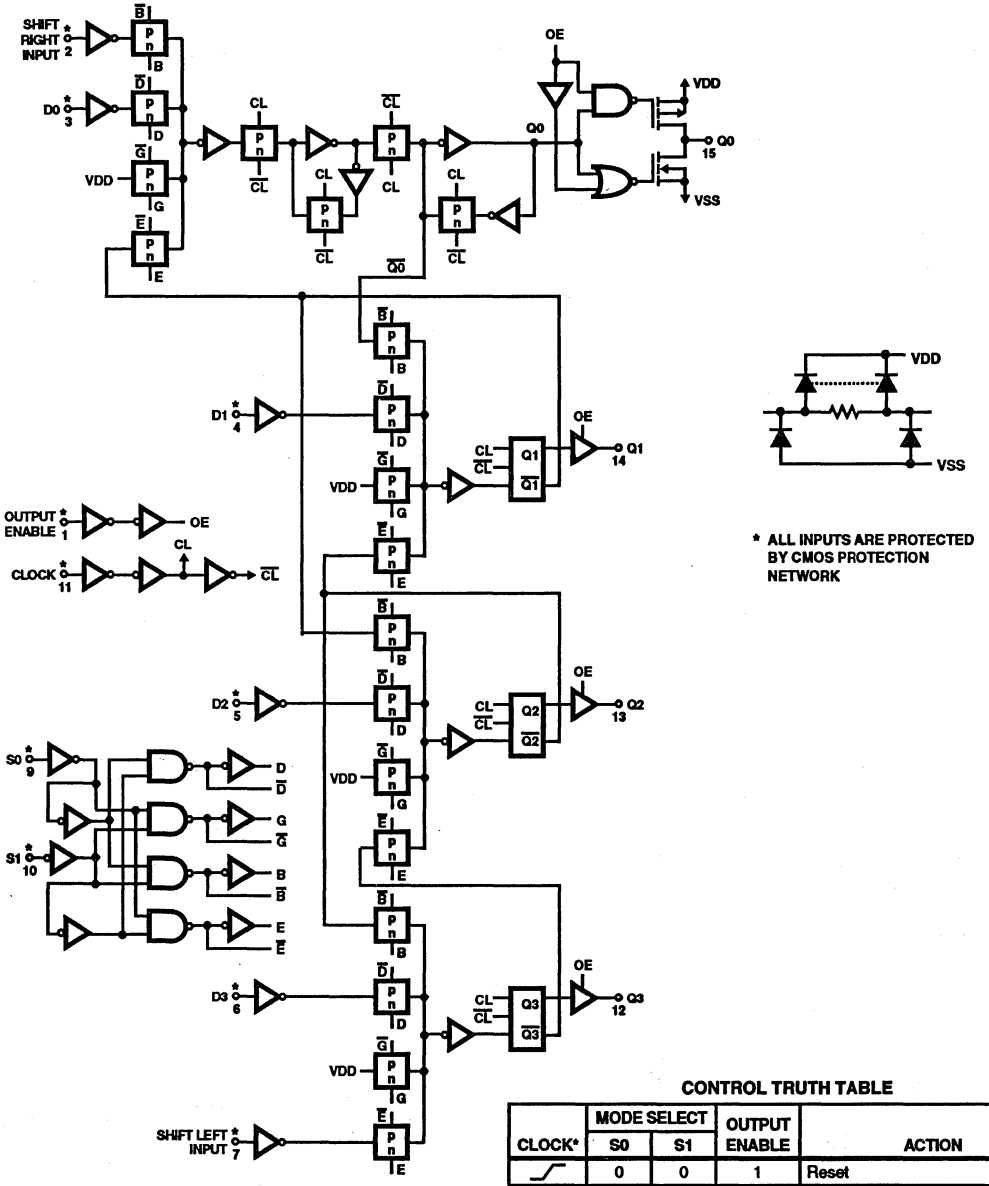
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
CD40104BMS, CD40194BMS						
Static Burn-In 1 Note 1	12-15	1-11	16			
Static Burn-In 2 Note 1	12-15	8	1-7, 9-11, 16			
Dynamic Burn-In Note 1	-	7, 8, 10	1, 3-6, 9, 16	12-15	11	2
Irradiation Note 2	12-15	8	1-7, 9-11, 16			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagrams



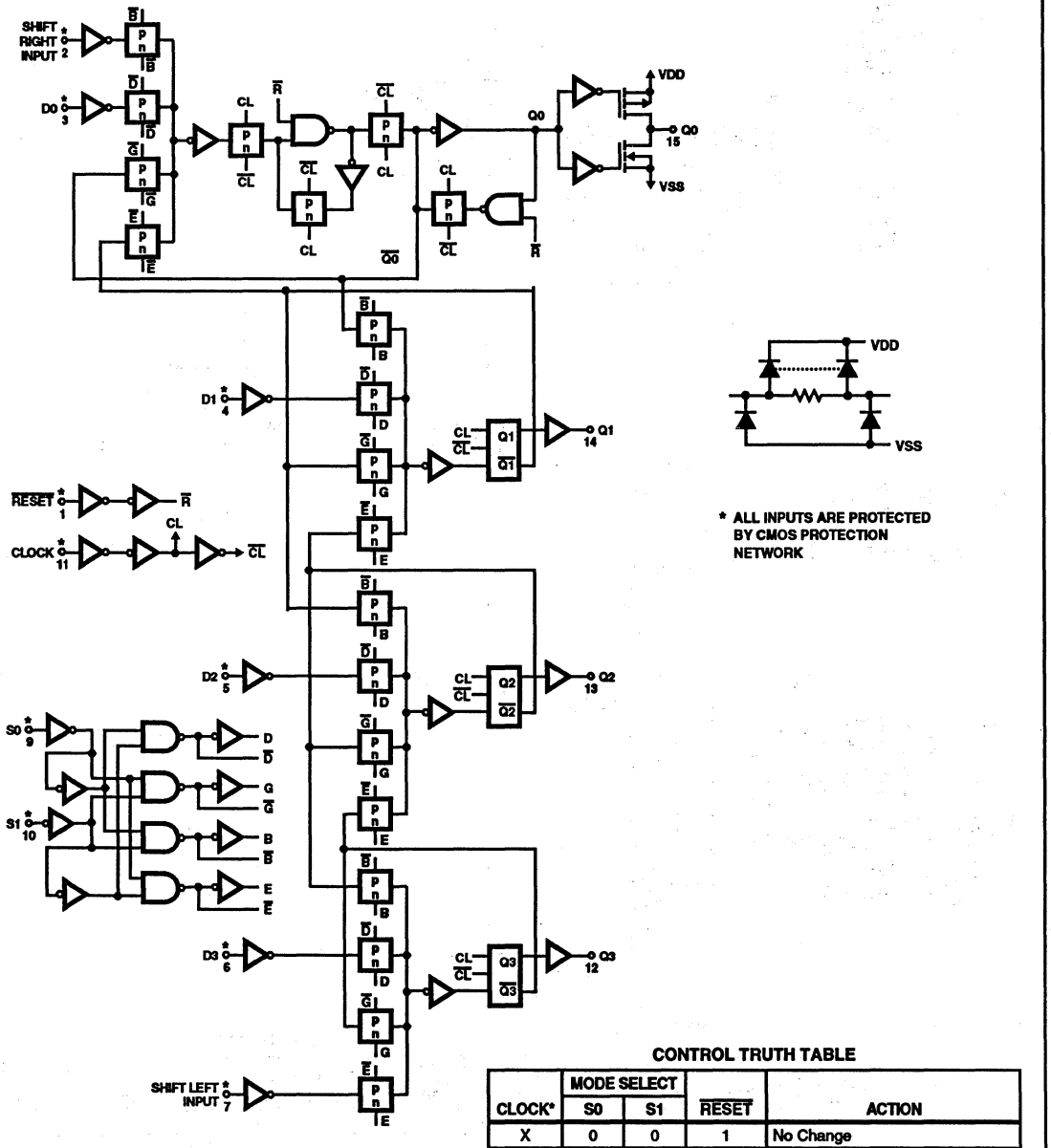
CONTROL TRUTH TABLE

CLOCK*	MODE SELECT S0	MODE SELECT S1	OUTPUT ENABLE	ACTION
↑	0	0	1	Reset
↑	1	0	1	Shift Right (Q0 toward Q3)
↑	0	1	1	Shift Left (Q3 toward Q0)
↑	1	1	1	Parallel Load
X	X	X	0	Operations occur as shown above, but outputs assume high impedance

X = Don't Care 1 = High level 0 = Low level * Level change

FIGURE 1. CD40104BMS

Logic Diagrams (Continued)



CONTROL TRUTH TABLE

CLOCK*	MODE SELECT S0	MODE SELECT S1	$\overline{\text{RESET}}$	ACTION
X	0	0	1	No Change
⎍	1	0	1	Shift Right (Q0 toward Q3)
⎍	0	1	1	Shift Left (Q3 toward Q0)
⎍	1	1	1	Parallel Load
X	X	X	0	Reset

X = Don't Care 1 = High level 0 = Low level * Level change

FIGURE 2. CD40194BMS

Typical Performance Characteristics

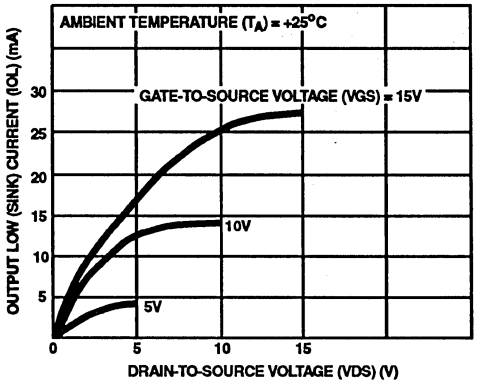


FIGURE 3. TYPICAL N-CHANNEL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

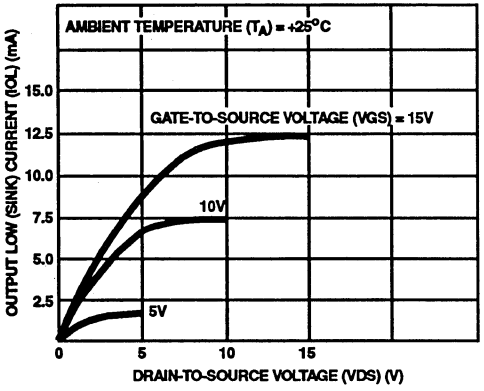


FIGURE 4. MINIMUM N-CHANNEL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

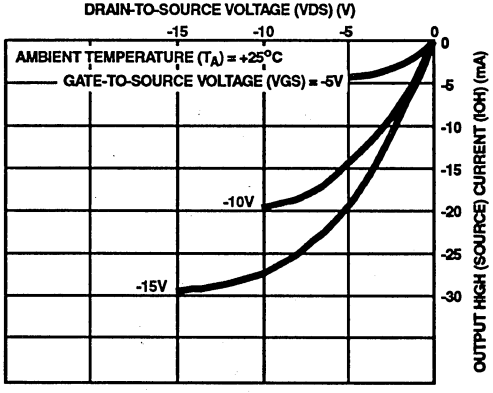


FIGURE 5. TYPICAL P-CHANNEL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

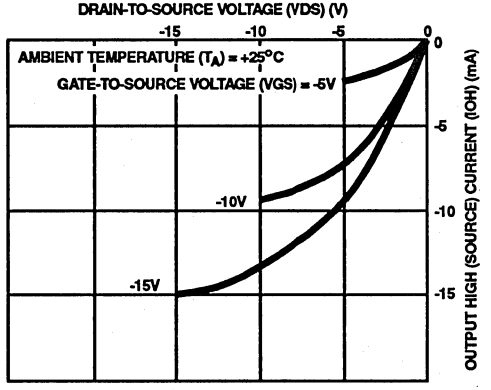


FIGURE 6. MINIMUM P-CHANNEL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

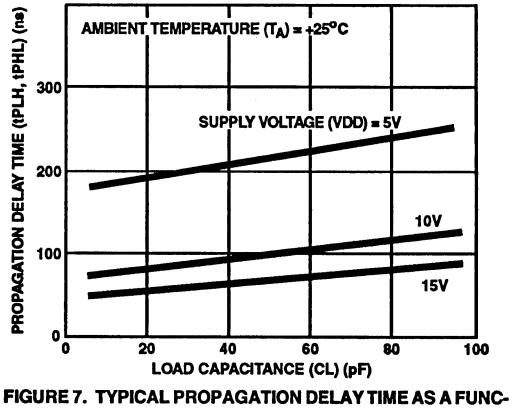


FIGURE 7. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE, (CLOCK TO Q)

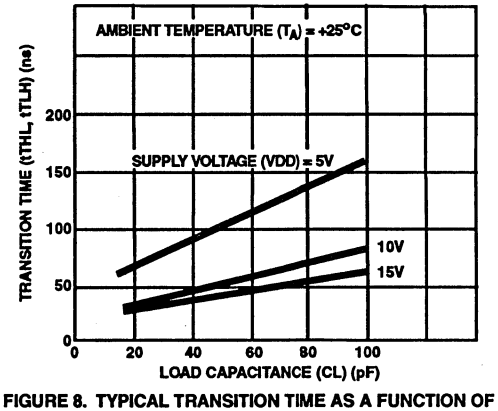


FIGURE 8. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

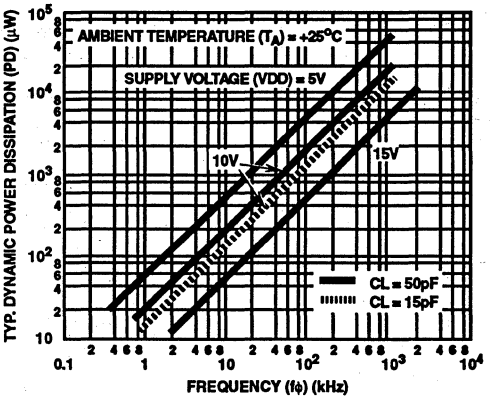
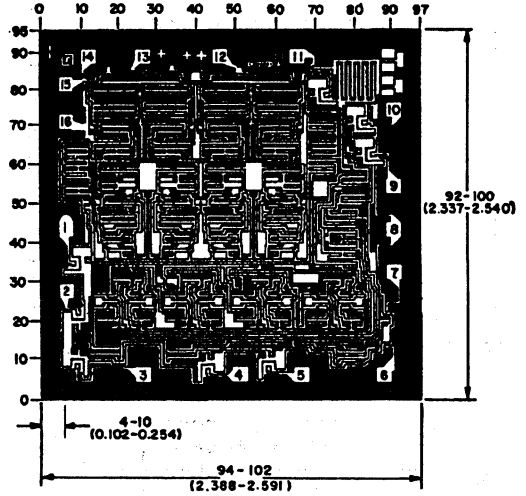
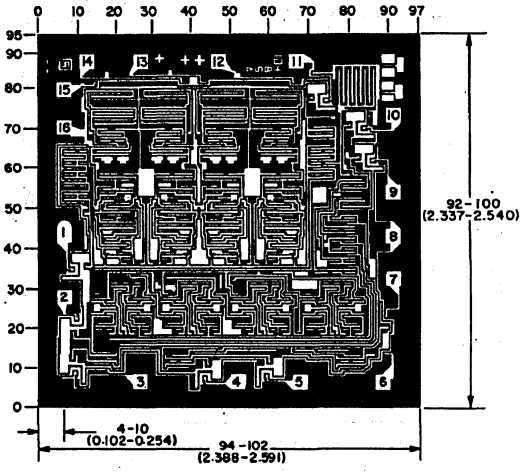


FIGURE 9. TYPICAL POWER DISSIPATION AS A FUNCTION OF FREQUENCY

Chip Dimensions and Pad Layouts



CD40104BMS



CD40194BMS

Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD40105BMS

December 1992

CMOS FIFO Register

Features

- 4 Bits x 16 Words
- High Voltage Type (20V Rating)
- Independent Asynchronous Inputs and Outputs
- 3-State Outputs
- Expandable in Either Direction
- Status Indicators on Input and Output
- Reset Capability
- Standardized Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Bit Rate Smoothing
- CPU/Terminal Buffering
- Data Communications
- Peripheral Buffering
- Line Printer Input Buffers
- Auto Dialers
- CRT Buffer Memories
- Radar Data Acquisition

Description

CD40105BMS is a low-power first-in-first-out (FIFO) "elastic" storage register that can store 16 4-bit words. It is capable of handling input and output data at different shifting rates. This feature makes it particularly useful as a buffer between asynchronous systems.

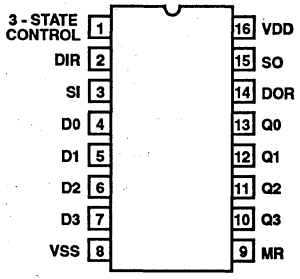
Each word position in the register is clocked by a control flip-flop, which stores a marker bit. A "1" signifies that the position's data is filled and a "0" denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding flip-flop. When a control flip-flop is in the "0" state and sees a "1" in the preceding flip-flop, it generates a clock pulse that transfers data from the preceding four data latches into its own four data latches and resets the preceding flip-flop to "0". The first and last control flip-flops have buffered outputs. Since all empty locations "bubble" automatically to the input end, and all valid data ripple through to the output end, the status of the first control flip-flop (DATA-IN READY) indicates if the FIFO is full, and the status of the last flip-flop (DATA-OUT READY) indicates if the FIFO contains data. As the earliest data are removed from the bottom of the data stack (the output end), all data entered later will automatically propagate (ripple) toward the output.

Loading Data - Data can be entered whenever the DATA-IN READY (DIR) flag is high, by a low to high transition on the SHIFT-IN (SI) input. This input must go low momentarily before the next word is accepted by the FIFO. The DIR flag will go low momentarily, until that data have been transferred to the second location. The flag will remain low when all 16-word locations are filled with valid data, and further pulses on the SI input will be ignored until DIR goes high.

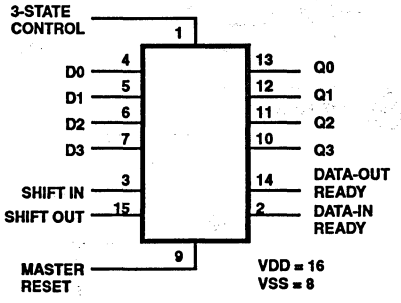
Continued on next page

Pinout

CD40105BMS
TOP VIEW



Functional Diagram



Unloading Data - As soon as the first word has rippled to the output, DATA-OUT READY (DOR) goes high, and data can be removed by a falling edge on the SO input. This falling edge causes the DOR signal to go low while the word on the output is dumped and the next word moves to the output. As long as valid data are available in the FIFO, the DOR signal will go high again signifying that the next word is ready at the output. When the FIFO is empty, DOR will remain low, and any further commands will be ignored until a "1" marker ripples down to the last control register, when DOR goes high. Unloading of data is inhibited while the 3-state control input is high. The 3-state control signal should not be shifted from high to low (data outputs turned on) while the SHIFT-OUT is at logic 0. This level change would cause the first word to be shifted out (unloaded) immediately and the data to be lost.

Cascading - The CD40105BMS can be cascaded to form longer registers simply by connecting the DIR to SO and DOR to SI. In the cascaded mode, a MASTER RESET pulse must be applied after the supply voltage is turned on. For words wider than 4 bits, the DIR and the DOR outputs must be gated together with AND gates. Their outputs drive the SI and SO inputs in parallel, if expanding is done in both directions (see Figures 9 and 11).

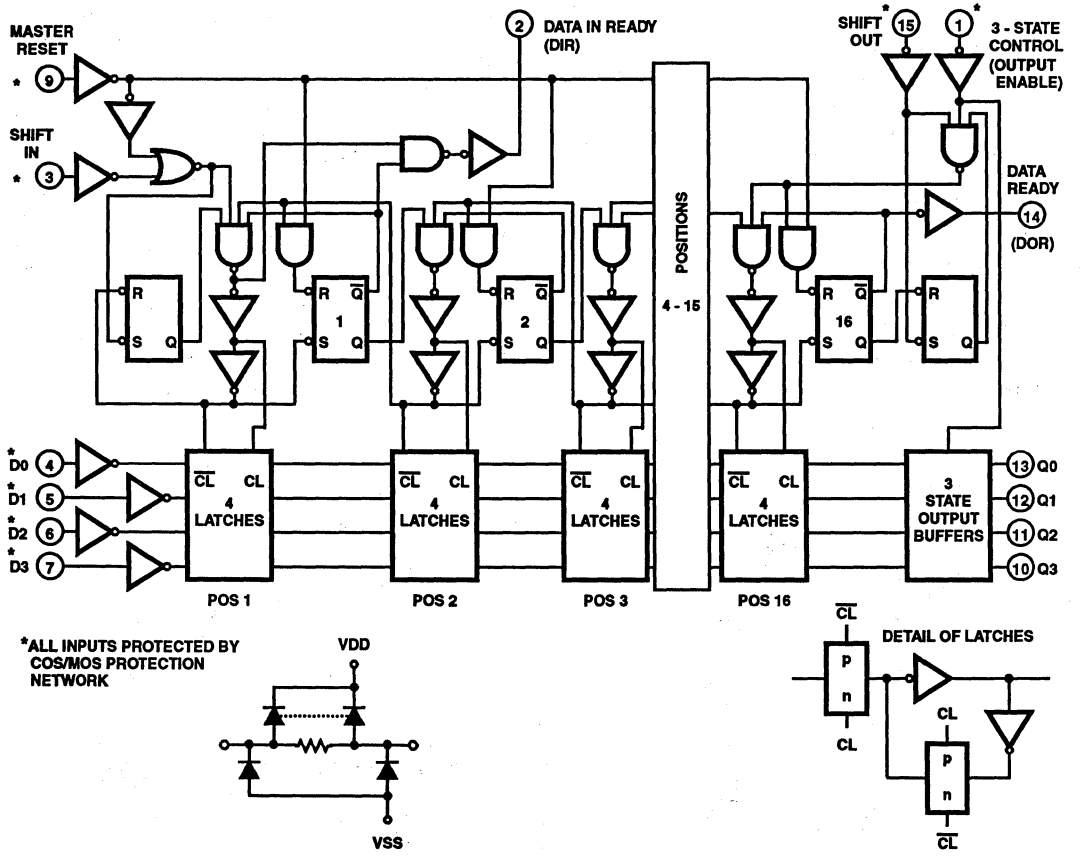
3-State Outputs - In order to facilitate data busing, 3-state outputs are provided on the data output lines, while the load condition of the register can be detected by the state of the DOR output.

Master Reset - A high on the MASTER RESET (MR) sets all the control logic marker bits to "0". DOR goes low and DIR goes high. The contents of the data register are not changed, only declared invalid, and will be superseded when the first word is loaded. The shift-in must be low during Master Reset.

The CD40105BMS is supplied in these 16-lead outline packages:

Braze Seal DIP	H4X
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

Logic Diagram



Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional (Note 4)	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.4	-	µA
				2	+125°C	-12	-	µA
			VDD = 18V	3	-55°C	-0.4	-	µA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.4	µA
				2	+125°C	-	12	µA
			VDD = 18V	3	-55°C	-	0.4	µA

NOTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.
4. VDD = 2.8V/3.0V, RL = 100K to VDD
   VDD = 20V/18V, RL = 10K to VDD

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Shift Out or Reset to Data-Out Ready	TPHL1	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	370	ns
			10, 11	+125°C, -55°C	-	500	ns
Propagation Delay Shift In to Data-In Ready	TPHL2	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	320	ns
			10, 11	+125°C, -55°C	-	432	ns
Propagation Delay Ripple through Delay Input to Output	TPLH3	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	4	µs
			10, 11	+125°C, -55°C	-	5.4	µs
Propagation Delay 3-State Control to Data Out	TPZH	VDD = 5V, VIN = VDD or GND (Note 2, 3)	9	+25°C	-	280	ns
			10, 11	+125°C, -55°C	-	378	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Shift-In or Shift-Out Rate	FCL	VDD = 5V (Note 1, 2), VIN = VDD or GND	9	+25°C	1.5	-	MHz
			10, 11	+125°C, -55°C	1.11	-	MHz

NOTES:
1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.
3. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Shift or Reset to Data Out Ready	TPHL1	VDD = 10V	1, 2, 3	+25°C	-	180	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Propagation Delay Ripple through Delay Input to Output	TPLH3	VDD = 10V	1, 2, 3	+25°C	-	2	µs
		VDD = 15V	1, 2, 3	+25°C	-	1.4	µs
Propagation Delay Shift-In to Data-In Ready	TPHL2	VDD = 10V	1, 2, 3	+25°C	-	130	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns
Propagation Delay Shift Out to QN Out	TPHL4 TPLH4	VDD = 5V	1, 2, 3	+25°C	-	420	ns
		VDD = 10V	1, 2, 3	+25°C	-	380	ns
		VDD = 15V	1, 2, 3	+25°C	-	250	ns
Propagation Delay 3-State Control to Data Out	TPZH TPZL	VDD = 10V	1, 2, 4	+25°C	-	120	ns
		VDD = 15V	1, 2, 4	+25°C	-	80	ns
Propagation Delay 3-State Control to Data Out	TTHZ TPLZ	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Shift-In or Shift-Out Rate	FCL	VDD = 10V	1, 2	+25°C	3	-	MHz
		VDD = 15V	1, 2	+25°C	4	-	MHz
Maximum Shift-In or Shift-Out Rise Time	TR	VDD = 5V	3	+25°C	-	15	µs
		VDD = 10V	3	+25°C	-	15	µs
		VDD = 15V	3	+25°C	-	15	µs
Maximum Shift-In Fall Time	TF	VDD = 5V	3	+25°C	-	15	µs
		VDD = 10V	3	+25°C	-	15	µs
		VDD = 15V	3	+25°C	-	15	µs

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Maximum Shift-Out Fall Time	TF	VDD = 5V	3	+25°C	-	15	µs
		VDD = 10V	3	+25°C	-	5	µs
		VDD = 15V	3	+25°C	-	5	µs
Minimum Master Reset Pulse Width	TWH	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	90	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Data-In Ready Pulse Width	TWL	VDD = 5V	1, 2, 3	+25°C	-	520	ns
		VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	140	ns
Data-Out Ready Pulse Width	TWL	VDD = 5V	1, 2, 3	+25°C	-	440	ns
		VDD = 10V	1, 2, 3	+25°C	-	180	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Minimum Shift Out Pulse Width	TWL	VDD = 5V	1, 2, 3	+25°C	-	180	ns
		VDD = 10V	1, 2, 3	+25°C	-	75	ns
		VDD = 15V	1, 2, 3	+25°C	-	55	ns
Minimum Data Setup Time	TSU	VDD = 5V	1, 2, 3	+25°C	-	0	ns
		VDD = 10V	1, 2, 3	+25°C	-	0	ns
		VDD = 15V	1, 2, 3	+25°C	-	0	ns
Minimum Data Hold Time	TH	VDD = 5V	1, 2, 3	+25°C	-	350	ns
		VDD = 10V	1, 2, 3	+25°C	-	150	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Minimum Shift In Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	2, 10 - 14	1, 3 - 9, 15	16			
Static Burn-In 2 Note 1	2, 10 - 14	8	1, 3 - 7, 9, 15, 16			
Dynamic Burn-In Note 1	-	1, 8, 9	16	2, 10 - 14	3, 15	4 - 7
Irradiation Note 2	2, 10 - 14	8	1, 3 - 7, 9, 15, 16			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Typical Performance Characteristics

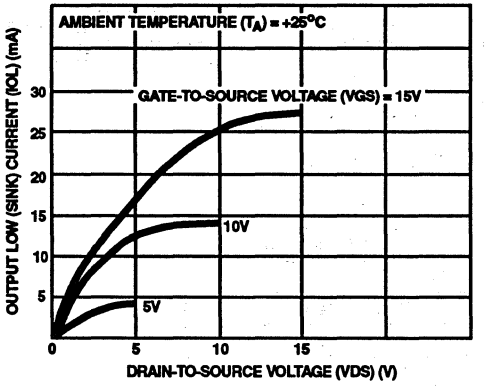


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

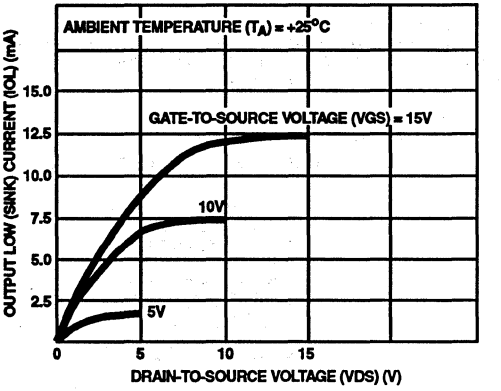


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

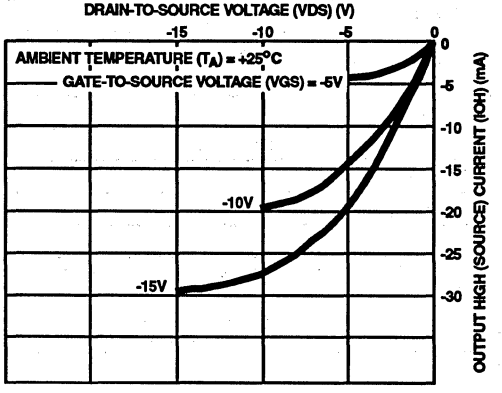


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

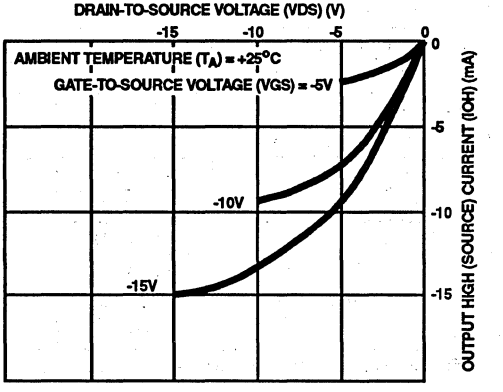


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

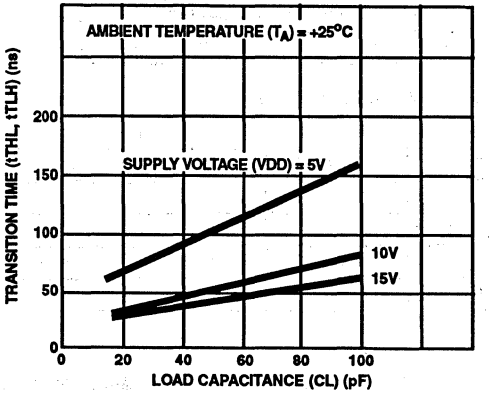


FIGURE 6. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

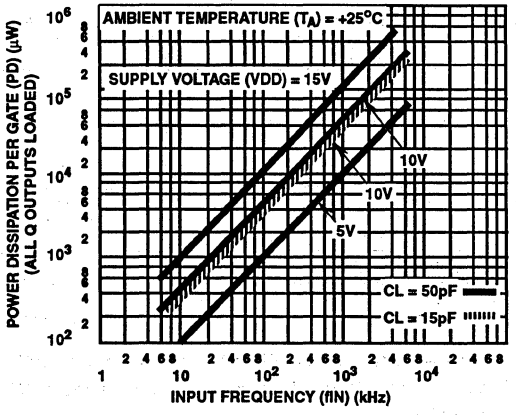


FIGURE 7. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF FREQUENCY

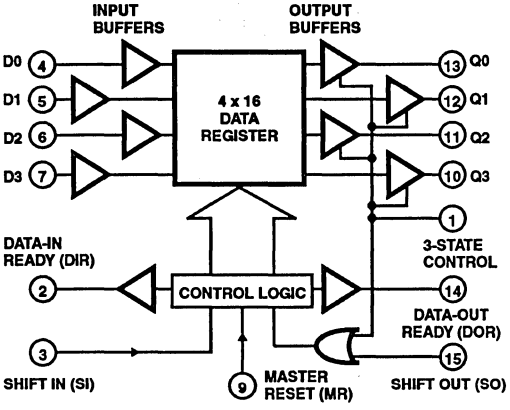


FIGURE 8. CD40105BMS FUNCTIONAL BLOCK DIAGRAM

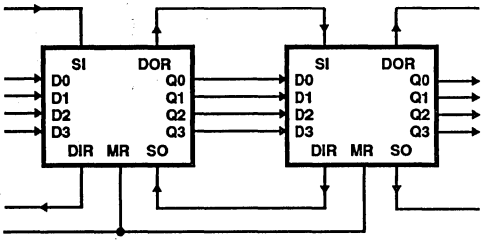
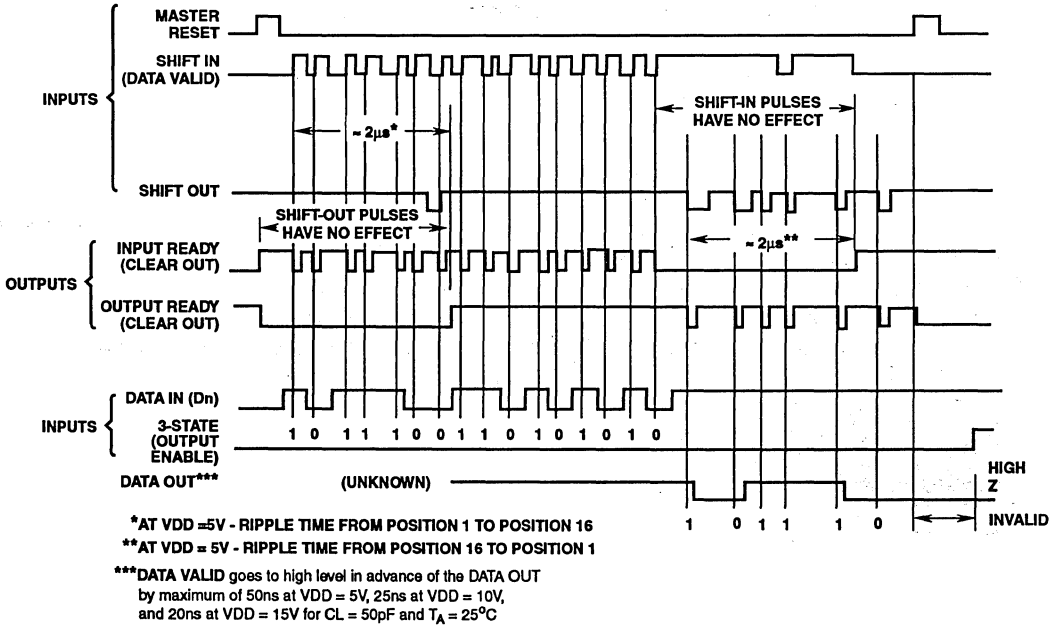


FIGURE 9. EXPANSION, 4-BITS WIDE-BY-16 N-BITS LONG



*AT VDD =5V - RIPPLE TIME FROM POSITION 1 TO POSITION 16
**AT VDD = 5V - RIPPLE TIME FROM POSITION 16 TO POSITION 1
***DATA VALID goes to high level in advance of the DATA OUT by maximum of 50ns at VDD = 5V, 25ns at VDD = 10V, and 20ns at VDD = 15V for CL = 50pF and $T_A = 25^oC$

FIGURE 10. TIMING DIAGRAM FOR THE CD40105BMS

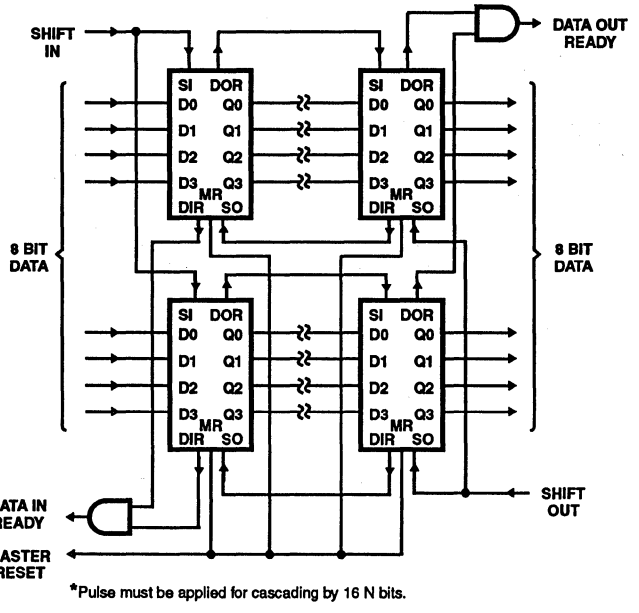
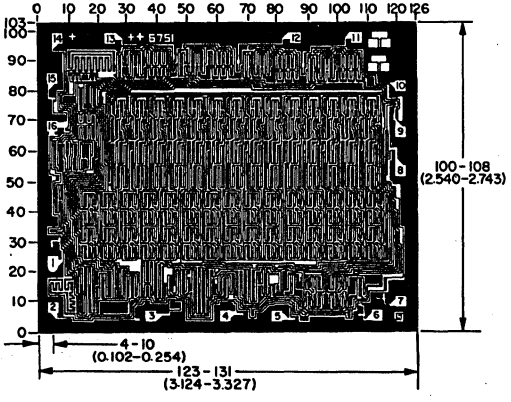


FIGURE 11. EXPANSION, 8-BITS-WIDE-BY-16 N-BITS LONG USING CD40105BMS

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10-3 inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD40106BMS

CMOS Hex Schmitt Triggers

December 1992

Features

- High Voltage Type (20V Rating)
- Schmitt Trigger Action with No External Components
- Hysteresis Voltage (Typ.)
  - 0.9V at VDD = 5V
  - 2.3V at VDD = 10V
  - 3.5V at VDD = 15V
- Noise Immunity Greater than 50%
- No Limit on Input Rise and Fall Times
- Low VDD to VSS Current During Slow Input Ramp
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Standardized Symmetrical Output Characteristics
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Wave and Pulse Shapers
- High Noise Environment Systems
- Monostable Multivibrators
- Astable Multivibrators

Description

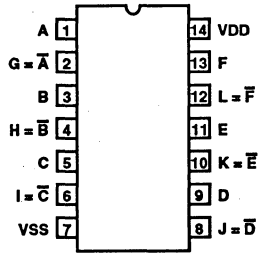
CD40106BMS consists of six Schmitt trigger circuits. Each circuit functions as an inverter with Schmitt trigger action on the input. The trigger switches at different points for positive and negative going signals. The difference between the positive going voltage (VP) and the negative going voltage (VN) is defined as hysteresis voltage (VH) (see Figure 17).

The CD40106BMS is supplied in these 14 lead outline packages:

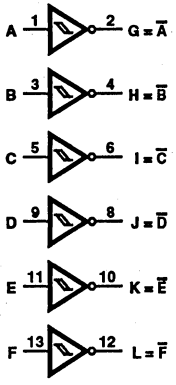
Braze Seal DIP	H4Q
Frit Seal DIP	H1B
Ceramic Flatpack	H3W

Pinout

CD40106BMS
TOP VIEW



Functional Diagram



Logic Diagram

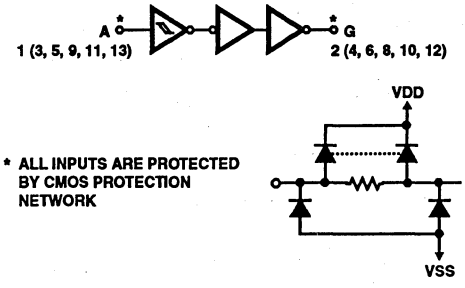


FIGURE 1. 1 OF 6 SCHMITT TRIGGERS

7 LOGIC

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 2)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Positive Trigger Threshold Voltage (See Figure 17)	VP5	VDD = 5V		1, 2, 3	+25°C, +125°C, -55°C	2.2	3.6	V
	VP10	VDD = 10V		1, 2, 3	+25°C, +125°C, -55°C	4.6	7.1	V
	VP15	VDD = 15V		1, 2, 3	+25°C, +125°C, -55°C	6.8	10.8	V
Negative Trigger Threshold Voltage (See Figure 17)	VN5	VDD = 5V		1, 2, 3	+25°C, +125°C, -55°C	0.9	2.8	V
	VN10	VDD = 10V		1, 2, 3	+25°C, +125°C, -55°C	2.5	5.2	V
	VN15	VDD = 15V		1, 2, 3	+25°C, +125°C, -55°C	4	7.4	V
Hysteresis Voltage (See Figure 17)	VH5	VDD = 5V		1, 2, 3	+25°C, +125°C, -55°C	0.3	1.6	V
	VH10	VDD = 10V		1, 2, 3	+25°C, +125°C, -55°C	1.2	3.4	V
	VH15	VDD = 15V		1, 2, 3	+25°C, +125°C, -55°C	1.6	5.0	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	280	ns
			10, 11	+125°C, -55°C	-	378	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Propagation Delay	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	140	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K., Input TR, TF < 20ns

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	2, 4, 6, 8, 10, 12	1, 3, 5, 7, 9, 11, 13	14			
Static Burn-In 2 Note 1	2, 4, 6, 8, 10, 12	7	1, 3, 5, 9, 11, 13, 14			
Dynamic Burn-In Note 1	-	7	14	2, 4, 6, 8, 10, 12	1, 3, 5, 9, 11, 13	
Irradiation Note 2	2, 4, 6, 8, 10, 12	7	1, 3, 5, 9, 11, 13, 14			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Typical Performance Characteristics

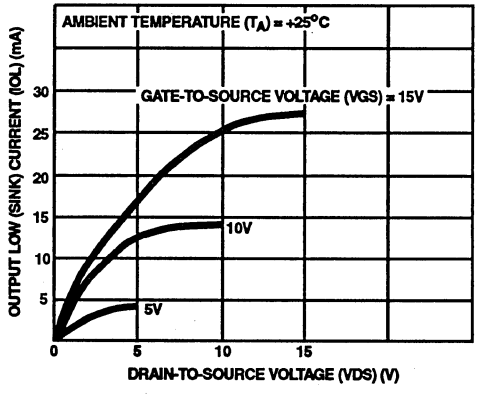


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

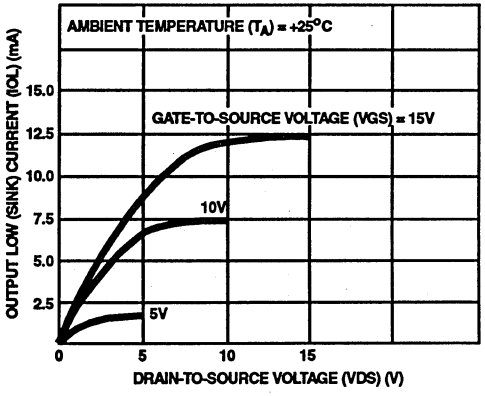


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

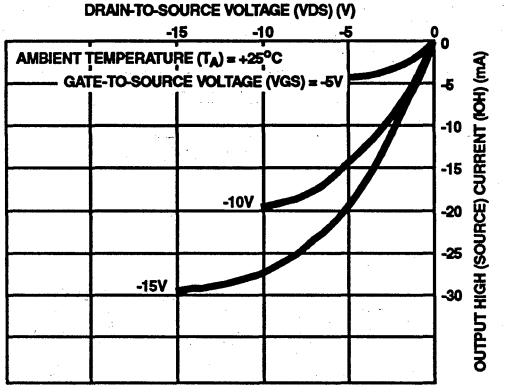


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

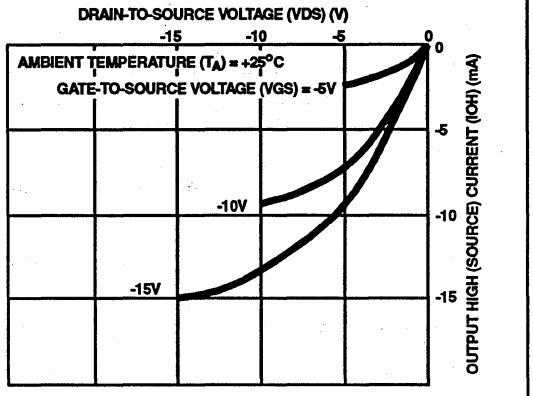


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

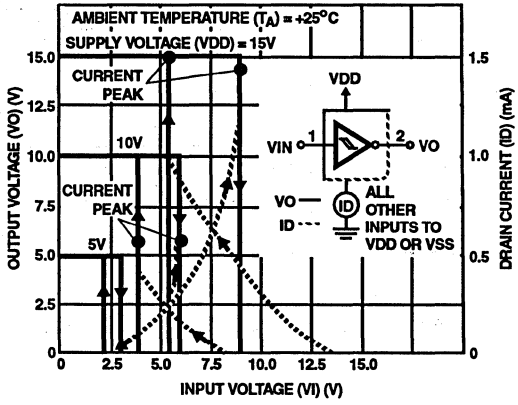


FIGURE 6. TYPICAL CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS

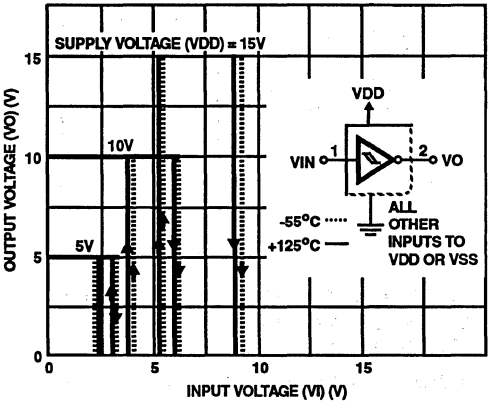


FIGURE 7. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE

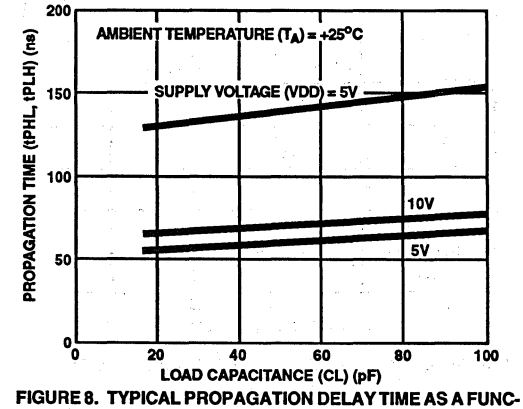


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

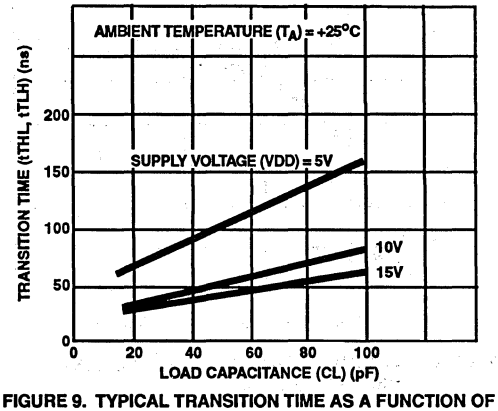


FIGURE 9. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

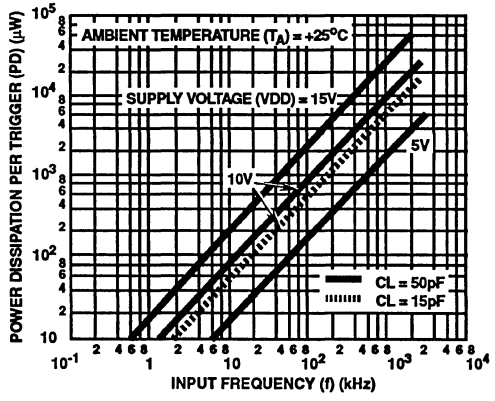


FIGURE 10. TYPICAL POWER DISSIPATION PER TRIGGER AS A FUNCTION OF INPUT FREQUENCY

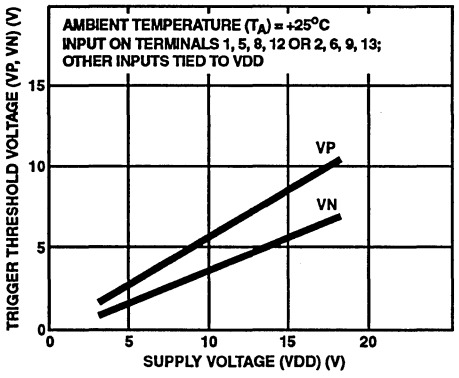


FIGURE 11. TYPICAL TRIGGER THRESHOLD VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE

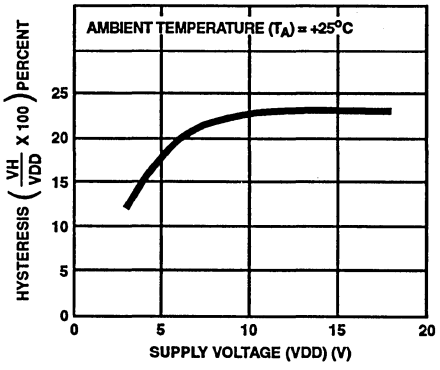


FIGURE 12. TYPICAL PERCENT HYSTERESIS AS A FUNCTION OF SUPPLY VOLTAGE

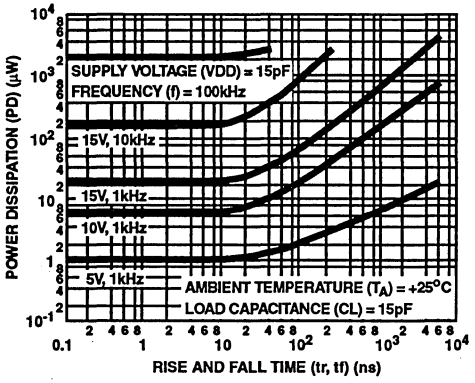


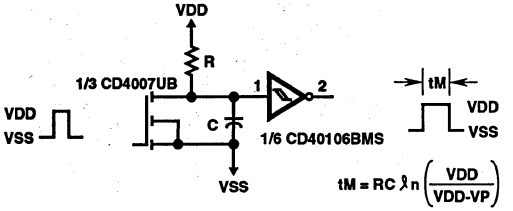
FIGURE 13. TYPICAL POWER DISSIPATION AS A FUNCTION OF RISE AND FALL TIMES

7 LOGIC

Applications

FREQUENCY RANGE OF WAVE SHAPE
IS FROM DC TO 1MHz

FIGURE 14. WAVE SHAPER

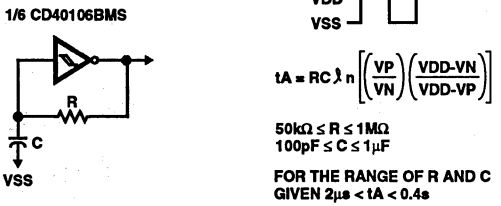


$$tM = RC \ln\left(\frac{VDD}{VDD-VP}\right)$$

$50k\Omega \leq R \leq 1M\Omega$
$100pF \leq C \leq 1\mu F$

FOR THE RANGE OF R AND C
GIVEN $5\mu s < tM < 1s$

FIGURE 15. MONOSTABLE MULTIVIBRATOR

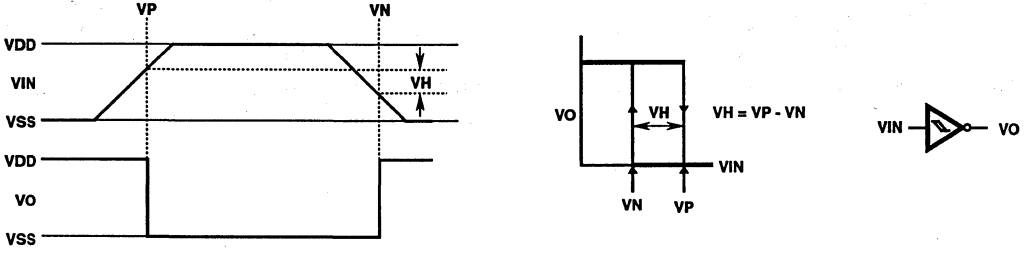


$$tA = RC \ln\left[\left(\frac{VP}{VN}\right)\left(\frac{VDD-VN}{VDD-VP}\right)\right]$$

$50k\Omega \leq R \leq 1M\Omega$
$100pF \leq C \leq 1\mu F$

FOR THE RANGE OF R AND C
GIVEN $2\mu s < tA < 0.4s$

FIGURE 16. ASTABLE MULTIVIBRATOR



(a) DEFINITION OF VP, VN, VH

(b) TRANSFER CHARACTERISTIC OF 1 OF 6 GATES

FIGURE 17. HYSTERESIS DEFINITION, CHARACTERISTICS, AND TEST SETUP

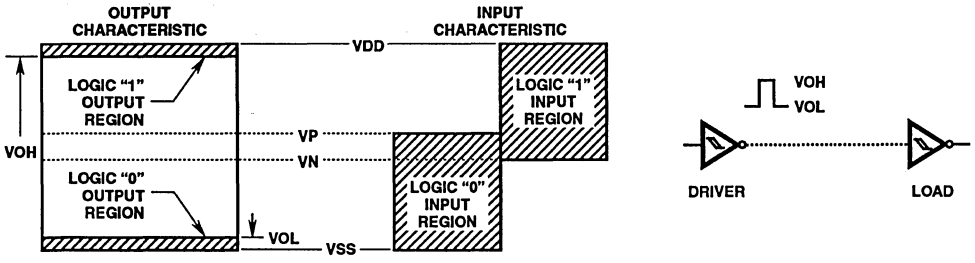
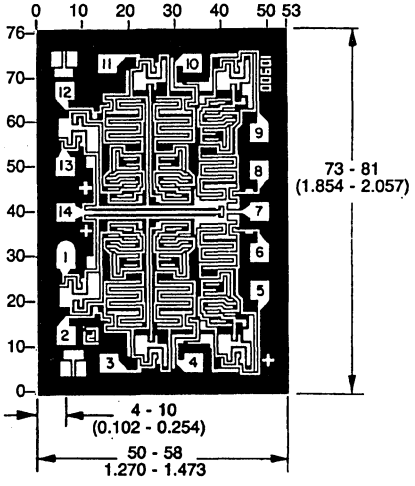


FIGURE 18. INPUT AND OUTPUT CHARACTERISTICS

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD40107BMS

December 1992

CMOS Dual 2 Input NAND Buffer /Driver

Features

- High Voltage Type (20V Rating)
- 32 Times Standard B Series Output Current Drive Sinking Capability
  - 136mA Typ. at VDD = 10V
  - VDS = 1V
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range) RL to VDD = 10kΩ
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Driving Relays, Lamps, LEDs
- Line Driver
- Level Shifter (Up or Down)

Description

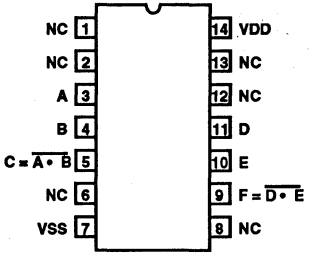
CD40107BMS is a dual 2 input NAND buffer/driver containing two independent 2 input NAND buffers with open drain single n-channel transistor outputs. This device features a wired OR capability and high output sink current capability (136mA typ. at VDD = 10V, VDS = 1V).

The CD40107BMS is supplied in these 14 lead outline packages:

Braze Seal DIP	H4H
Frit Seal DIP	H1B
Ceramic Flatpack	H3W

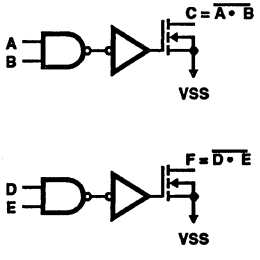
Pinouts

CD40107BF
TOP VIEW



NC = NO CONNECTION

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3355

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Drive Voltage	VOL5A	VDD = 5V, IOL = 16mA		1	+25°C	-	0.4	V
Output Drive Voltage	VOL5B	VDD = 5V, IOL = 34mA		1	+25°C	-	1.0	V
	VOL10A	VDD = 10V, IOL = 37mA		1	+25°C	-	0.5	V
Output Drive Voltage	VOL10B	VDD = 10V, IOL = 68mA		1	+25°C	-	1.0	V
	VOL15	VDD = 15V, IOL = 50mA		1	+25°C	-	0.5	V
Output Current (Source)	IOH5A	No Internal Pull-Up Device						
Output Current (Source)	IOH5B							
Output Current (Source)	IOH10							
Output Current (Source)	IOH15							
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional (Note 3)	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2, 3)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2, 3)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2, 3)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2, 3)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Tri-State Output Leakage High	IOZ	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	2	µA
				2	+125°C	-	20	µA
			VDD = 18V	3	-55°C	-	2	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	100	ns
			10, 11	+125°C, -55°C	-	135	ns

NOTES:

1. CL = 50pF, RL = 120Ω, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage (Note 5)	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage (Note 5)	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5A	VDD = 5.0V, VOUT = 0.4V	1, 2	+125°C	12	-	mA
				-55°C	21	-	mA
Output Current (Sink)	IOL5B	VDD = 5V, VOUT = 1.0V	1, 2, 4	+125°C	25	-	mA
				-55°C	44	-	mA
Output Current (Sink)	IOL10A	VDD = 10V, VOUT = 0.5V	1, 2, 4	+125°C	28	-	mA
				-55°C	49	-	mA
Output Current (Sink)	IOL10B	VDD = 10V, VOUT = 1V	1, 2, 4	+125°C	51	-	mA
				-55°C	89	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 0.5V	1, 2	+125°C	38	-	mA
				-55°C	66	-	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2, 4	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2, 4	+25°C, +125°C, -55°C	+7	-	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL	VDD = 10V	1, 2, 3	+25°C	-	90	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Propagation Delay	TPLH	VDD = 10V	1, 2, 3	+25°C	-	120	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Transition Time	TTHL	VDD = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V	1, 2, 3	+25°C	-	20	ns
Transition Time	TTLH	VDD = 10V	1, 2, 3	+25°C	-	70	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 120Ω, pull up resistor to VDD, Input TR, TF < 20ns.
4. Measured with external pull-up resistor RL = 10K to VDD

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1, 5	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES:

1. All voltages referenced to device GND.
2. CL = 50pF, RL = 120Ω, pull up resistor to VDD, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record
5. Measured with external pull-up resistor RL = 10K to VDD

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

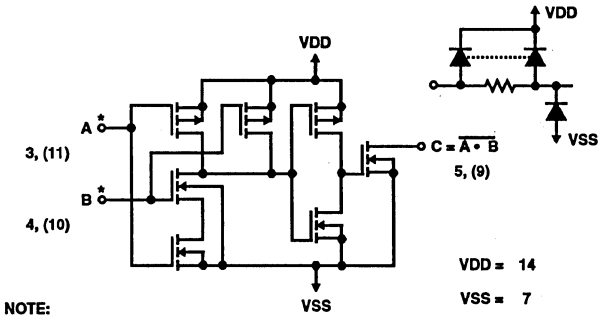
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	1, 2, 5, 6, 8, 9, 12, 13	3, 4, 7, 10, 11	14			
Static Burn-In 2 (Note 1)	1, 2, 5, 6, 8, 9, 12, 13	7	3, 4, 10, 11, 14			
Dynamic Burn-In (Note 3)	1, 2, 6, 8, 12, 13	7	14	5, 9	-	3, 4, 10, 11
Irradiation (Note 2)	1, 2, 5, 6, 8, 9, 12, 13	7	3, 4, 10, 11, 14			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V
3. Each pin except VDD and GND will have a series resistor of 4.75K ±5%, VDD = 18V ±.5.

Schematic



* ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

NOTE:
1 OF 2 GATES (NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR SECOND GATE)

TRUTH TABLE

A	B	C	
0	0	1*	Z**
1	0	1*	Z**
0	1	1*	Z**
1	1	0	

* Requires external pull-up resistor (RL) to VDD.

** Without pull-up resistor (3-state).

FIGURE 1. 1 OF 2 GATES

Typical Performance Characteristics

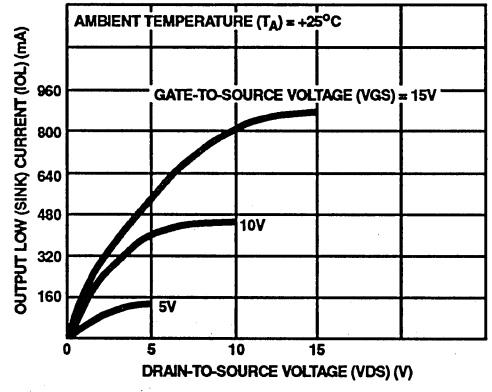


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

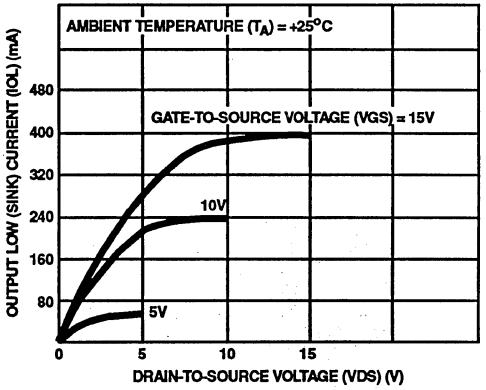


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

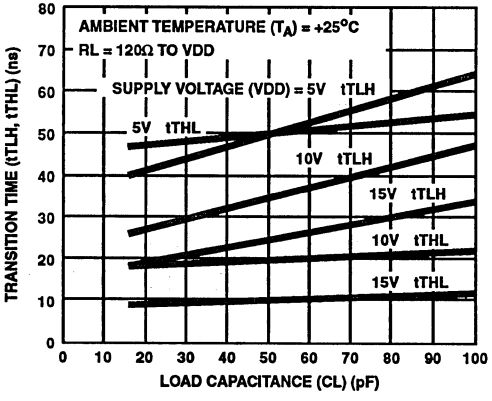


FIGURE 4. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

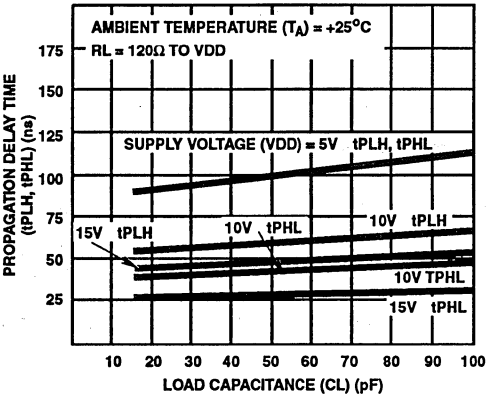


FIGURE 5. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

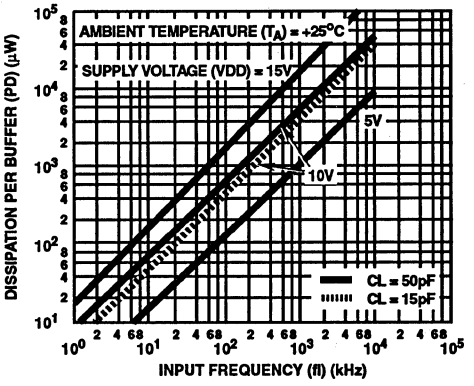
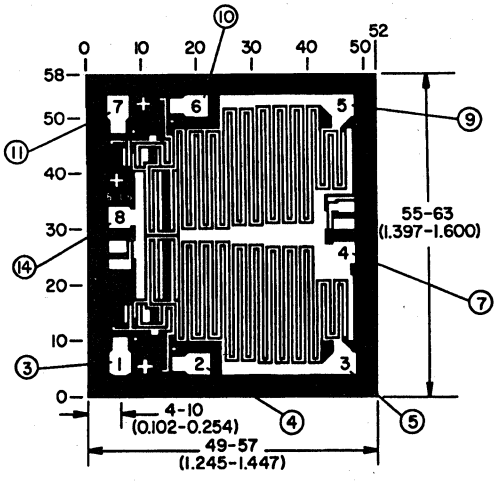


FIGURE 6. TYPICAL POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

Chip Dimensions and Pad Layout



NOTE:
Numbers inside pads for CD40107BE not offered as standard part.
Numbers outside chip are for CD40107BF

Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

Special Considerations

Limiting Capacitive Currents for CL > 500pF, VDD > 15V

For VDD > 15V, and load capacitance (CL) from output to ground > 500pF, an external 25Ω series limiting resistor should be inserted between the output terminal and CL. No external resistor is necessary if CL < 500pF or VDD < 15V.

Driving Inductive Loads

When using the CD40107BMS to drive inductive loads, the load should be shunted with a diode to prevent high voltages from developing across the CD40107BMS output.

HARRIS SEMICONDUCTOR

CD40108BMS

December 1992

CMOS 4 x 4 Multiport Register

Features

- High Voltage Type (20V Rating)
- Four 4-Bit Registers
- One Input and Two Output Buses
- Unlimited Expansion in Bit and Word Directions
- Data Lines have latched Inputs
- 3-State Outputs
- Separate Control of Each Bus, Allowing Simultaneous Independent Reading of Any of Four Registers on Bus A and Bus B and Independent Writing into Any of the Four Registers
- CD40108BMS is Pin-Compatible with Industry Type MC14580
- Standardized Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Description

The CD40108BMS is a 4 x 4 multiport register containing four 4-bit registers, write address decoder, two separate read address decoders, and two 3-state output buses.

When the ENABLE input is low, the corresponding output bus is switched, independently of the clock, to a high-impedance state. The high-impedance third state provides the outputs with the capability of being connected to the bus lines in a bus-organized system without the need for interface or pull-up components.

When the WRITE ENABLE input is high, all data input lines are latched on the positive transition of the CLOCK and the data is entered into the word selected by the write address lines. When WRITE ENABLE is low, the CLOCK is inhibited and no new data is entered. In either case, the contents of any word may be accessed via the read address lines independent of the state of the CLOCK input.

The CD40108BMS is supplied in these 24-lead outline packages:

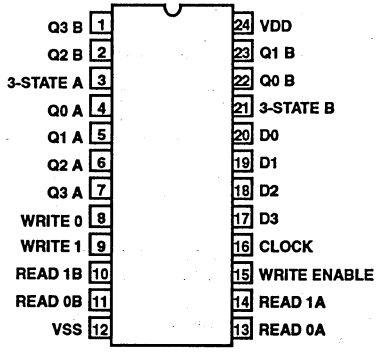
Braze Seal DIP	H4V
Ceramic Flatpack	H4P

Applications

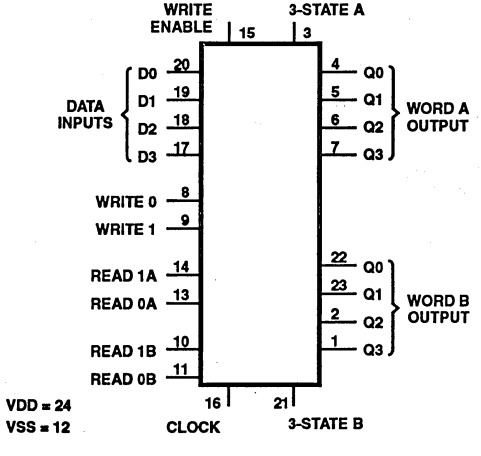
- Scratch-Pad Memories
- Arithmetic Units
- Data Storage

Pinout

CD40108BMS
TOP VIEW



Functional Diagram



7 LOGIC

File Number 3356

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.4	-	µA
				2	+125°C	-12	-	µA
			VDD = 18V	3	-55°C	-0.4	-	µA
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.4	µA
				2	+125°C	-	12	µA
			VDD = 18V	3	-55°C	-	0.4	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock or Write Enable to Q	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	720	ns
			10, 11	+125°C, -55°C	-	972	ns
Propagation Delay Read or Write Address to Q	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Propagation Delay 3-State Disable Delay Time	TPZH TPHZ	VDD = 5V, VIN = VDD or GND (Note 2, 3)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Propagation Delay 3-State Disable Delay Time	TPZL TPLZ	VDD = 5V, VIN = VDD or GND (Note 2, 3)	9	+25°C	-	260	ns
			10, 11	+125°C, -55°C	-	351	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	1.5	-	MHz
			10, 11	+125°C, -55°C	1.11	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Clock or Write Enable to Q	TPLH1 TPHL1	VDD = 10V	1, 2, 3	+25°C	-	280	ns
		VDD = 15V	1, 2, 3	+25°C	-	200	ns
Propagation Delay Read or Write Address to Q	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	240	ns
		VDD = 15V	1, 2, 3	+25°C	-	170	ns
Propagation Delay 3-State Disable Delay Time	TPZH TPHZ	VDD = 10V	1, 2, 4	+25°C	-	100	ns
		VDD = 15V	1, 2, 4	+25°C	-	80	ns
Propagation Delay 3-State Disable Delay Time	TPZL TPLZ	VDD = 10V	1, 2, 4	+25°C	-	120	ns
		VDD = 15V	1, 2, 4	+25°C	-	100	ns
Transition Time	TTLH TTHL	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	3.5	-	MHz
		VDD = 15V	1, 2, 3	+25°C	4.5	-	MHz
Minimum Data Setup Time Data to Clock	TS	VDD = 5V	1, 2, 3	+25°C	0		ns
		VDD = 10V	1, 2, 3	+25°C	0		ns
		VDD = 15V	1, 2, 3	+25°C	0		ns
Minimum Data Setup Time Write Enable to $\overline{\text{Clock}}$	TS	VDD = 5V	1, 2, 3	+25°C	250		ns
		VDD = 10V	1, 2, 3	+25°C	100		ns
		VDD = 15V	1, 2, 3	+25°C	70		ns
Minimum Data Setup Time Write Address to $\overline{\text{Clock}}$	TS	VDD = 5V	1, 2, 3	+25°C	250		ns
		VDD = 10V	1, 2, 3	+25°C	100		ns
		VDD = 15V	1, 2, 3	+25°C	70		ns
Clock Rise and Fall Time	TRCL TFCL	VDD = 5V	1, 2, 3, 5	+25°C	-	15	ns
		VDD = 10V	1, 2, 3, 5	+25°C	-	5	ns
		VDD = 15V	1, 2, 3, 5	+25°C	-	5	ns
Minimum Hold Time Data to Clock	TH	VDD = 5V	2, 3	+25°C	220		ns
		VDD = 10V	2, 3	+25°C	100		ns
		VDD = 15V	2, 3	+25°C	80		ns
Hold Time Write Enable to Clock	TH	VDD = 5V	2, 3	+25°C	-	270	ns
		VDD = 10V	2, 3	+25°C	-	130	ns
		VDD = 15V	2, 3	+25°C	-	80	ns
Write Address to Clock	TH	VDD = 5V	2, 3	+25°C	-	330	ns
		VDD = 10V	2, 3	+25°C	-	140	ns
		VDD = 15V	2, 3	+25°C	-	90	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Minimum Clock Pulse Width Clock or Write Enable	TW	VDD = 5V	3	+25°C	-	350	ns
		VDD = 10V	3	+25°C	-	130	ns
		VDD = 15V	3	+25°C	-	90	ns
Minimum Clock Pulse Width Write Address	TW	VDD = 5V	3	+25°C	-	300	ns
		VDD = 10V	3	+25°C	-	150	ns
		VDD = 15V	3	+25°C	-	90	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. CL = 50pF, RL = 1K, Input TR, TF < 20ns.
5. If more than one unit is cascaded, TRCL should be made less than or equal to the sumof the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	1	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	1, 2, 4 - 7, 22, 23	3, 8 - 12	24			
Static Burn-In 2 (Note 1)	1, 2, 4 - 7, 22, 23	2	3, 8 - 11, 13 - 21, 24			
Dynamic Burn-In (Note 1)	-	2	3, 15, 16, 21, 24	1, 2, 4 - 7, 22, 23	8, 11, 14, 19, 20	9, 10, 13, 17, 18
Irradiation (Note 2)	1, 2, 4 - 7, 22, 23	2	3, 8 - 11, 13 - 21, 24			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Block Diagram

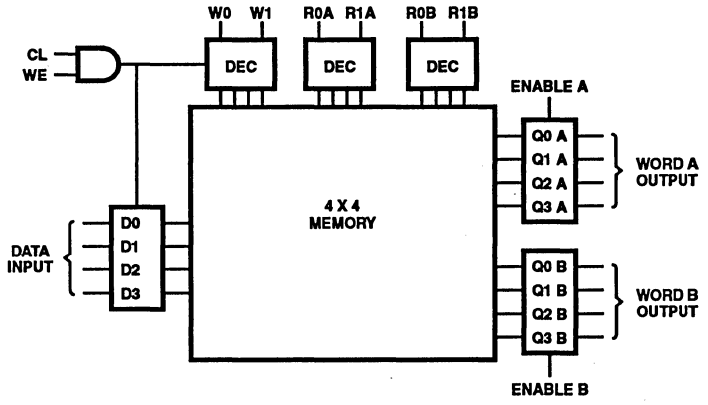


FIGURE 1.

TRUTH TABLE

CLOCK	WRITE ENABLE	WRITE 1	WRITE 0	READ 1A	READ 0A	READ 1B	READ 0B	ENABLE A	ENABLE B	DN	QnA	QnB
⎍	1	S1	S2	S1	S2	S1	S2	1	1	1	1	1
⎍	1	S1	S2	S1	S2	S1	S2	1	1	0	0	0
X	X	X	X	X	X	X	X	0	0	X	Z	Z
⎍	1	0	0	0	1	1	0	1	1	Dn to word 0	Word 1 out	Word 2 out
⎍	0	0	0	0	1	1	0	1	1	Word 0 not altered	Word 1 out	Word 2 out
X	X	X	X	1	0	0	1	1	1	X	Word 2 out	Word 1 out
⎎	X	X	X	X	X	X	X	1	1	X	NC	NC

1 = High Level 0 = Low Level X = Don't Care Z = High Impedance

S! and S2 refer to input states of either 1 or 0

Typical Performance Characteristics

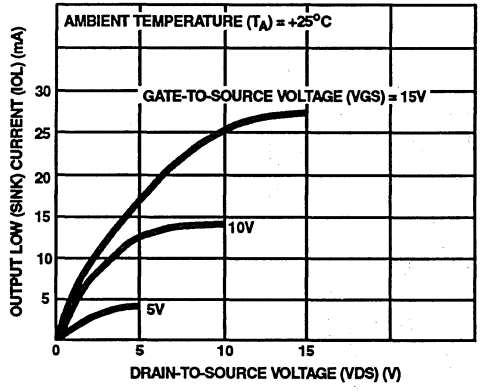


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

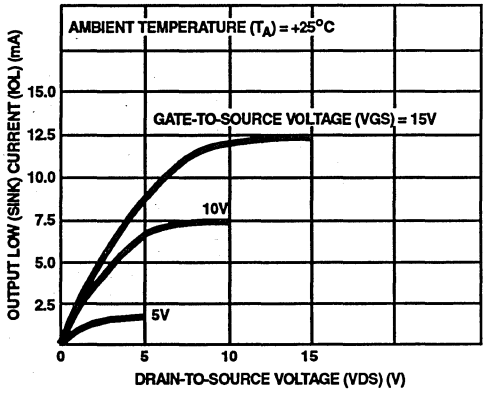


FIGURE 3. MIMIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

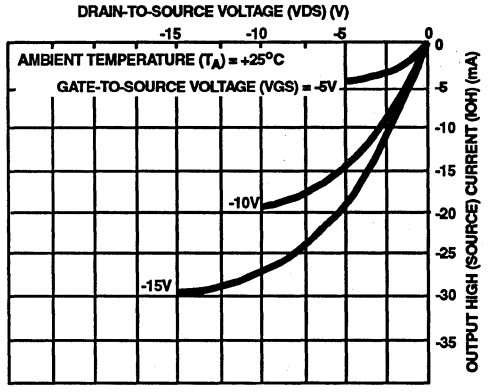


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

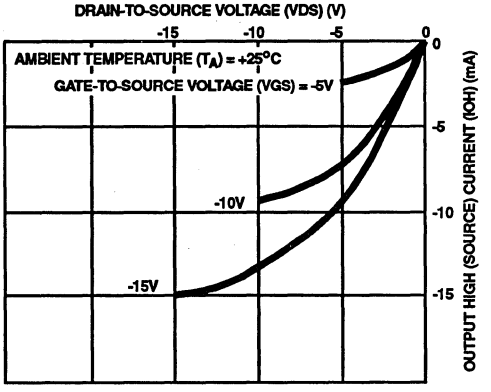


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

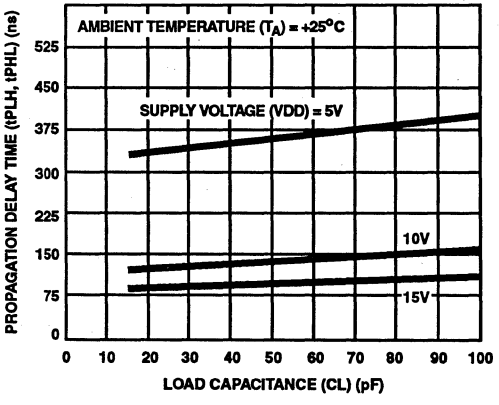


FIGURE 6. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (CL OR WE TO Q)

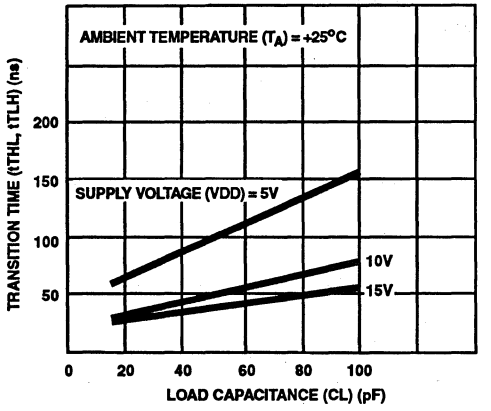


FIGURE 7. TYPICAL TRANSISTION TIME AS A FUNCTION OF LOAD CAPACITANCE

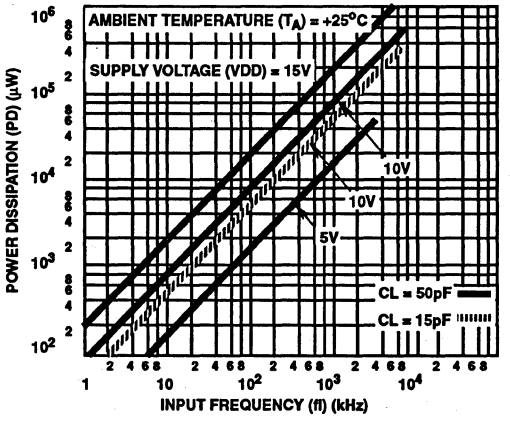


FIGURE 8. TYPICAL POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

Schematic Diagram

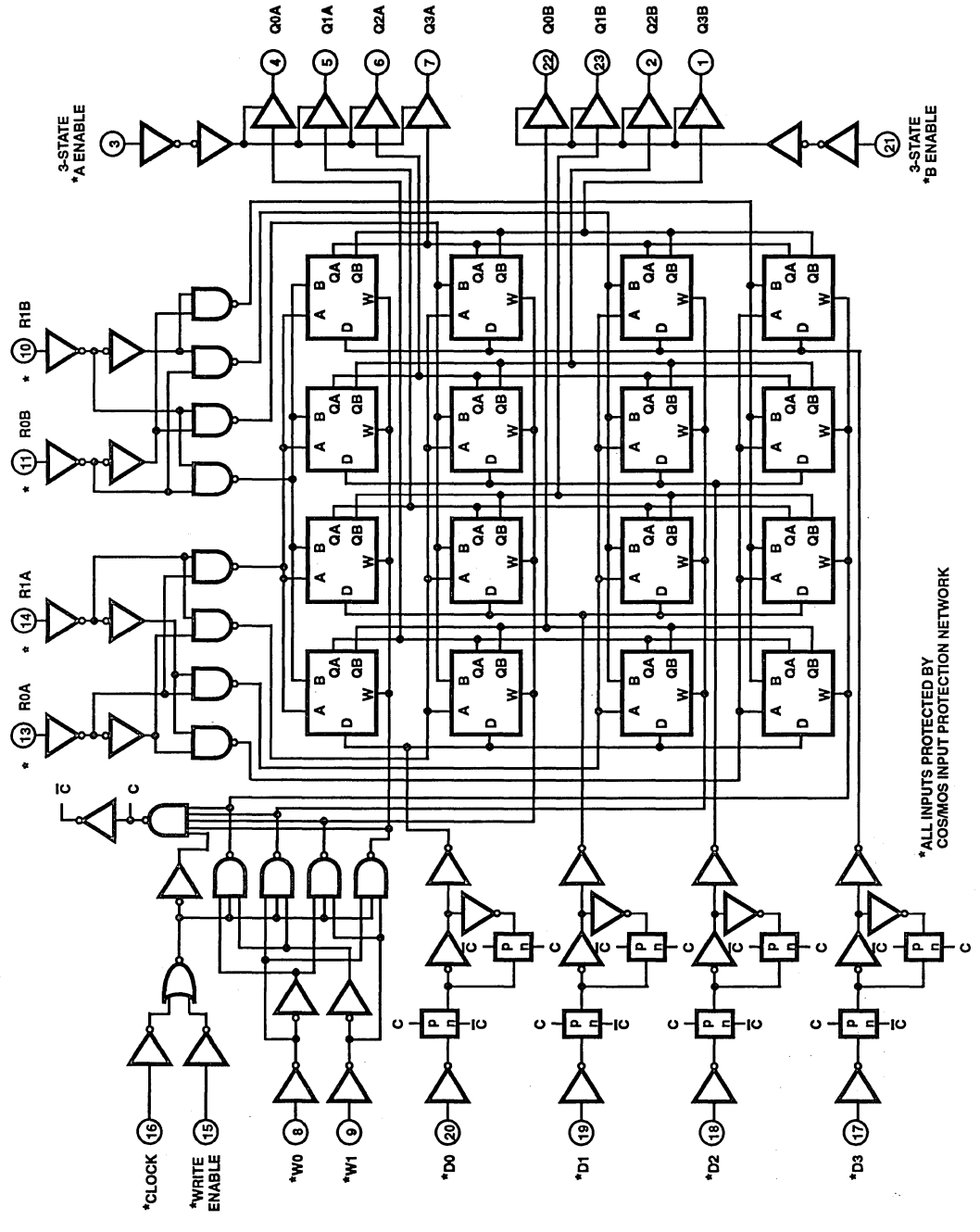


FIGURE 9.

Schematic Diagram (Continued)

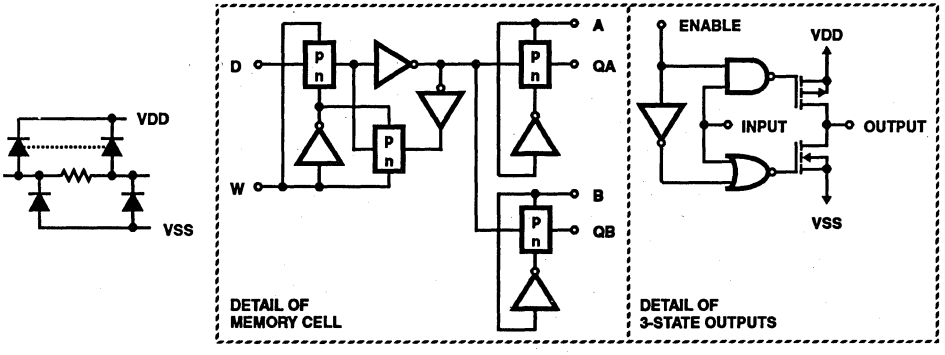


FIGURE 9. (Continued)

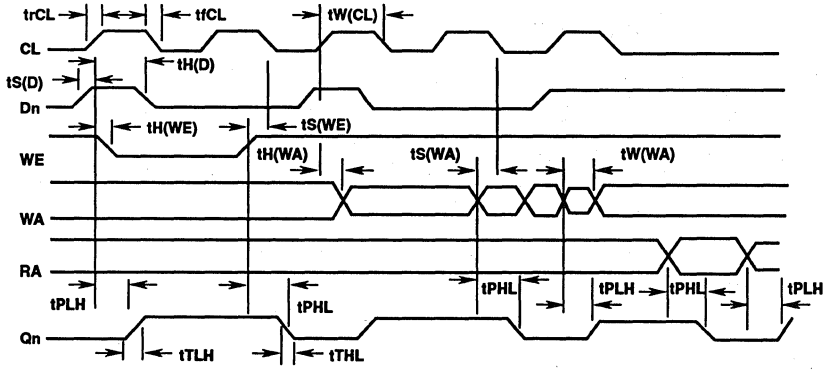


FIGURE 10. TIMING DIAGRAM

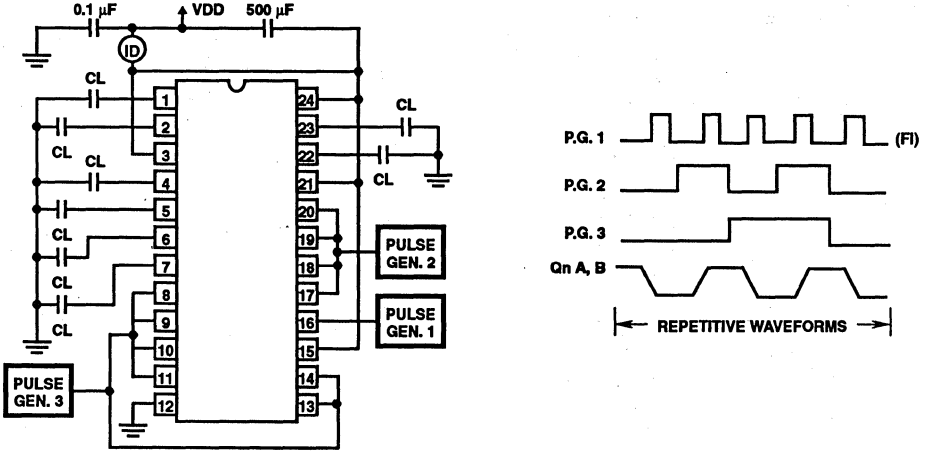
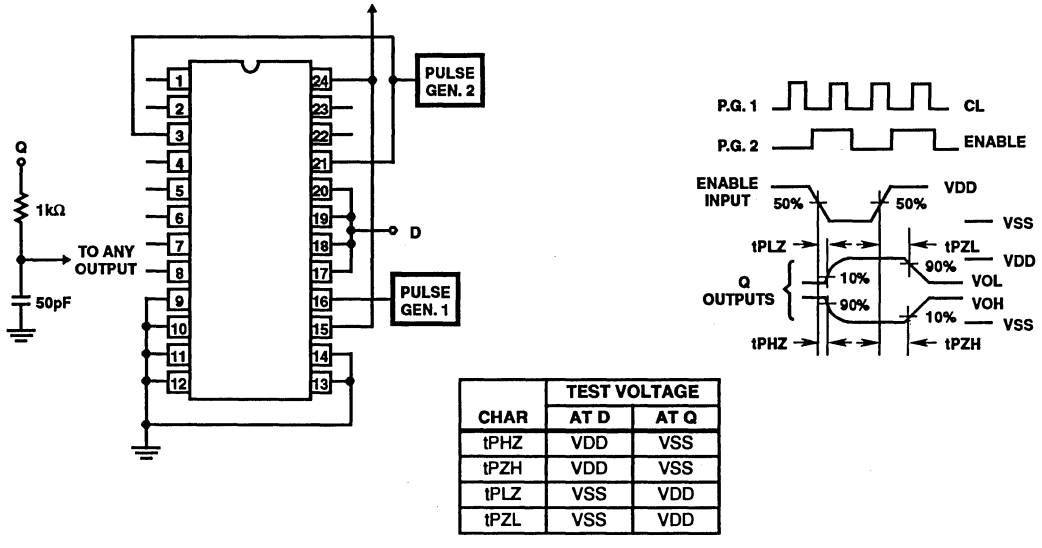


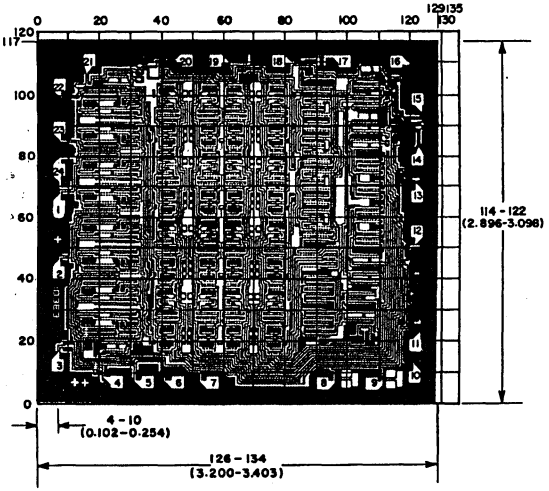
FIGURE 11. POWER-DISSIPATION TEST CIRCUIT AND WAVEFORMS



CHAR	TEST VOLTAGE AT D	AT Q
tPHZ	VDD	VSS
tPZH	VDD	VSS
tPLZ	VSS	VDD
tPZL	VSS	VDD

FIGURE 12. OUTPUT-ENABLE-DELAY-TIMES TEST CIRCUIT AND WAVEFORMS

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10-3 inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD40109BMS

December 1992

CMOS Quad Low-to-High Voltage Level Shifter

Features

- High Voltage Type (20V Rating)
- Independence of Power Supply Sequence Considerations
  - VCC can Exceed VDD
  - Input Signals can Exceed Both VCC and VDD
- Up and Down Level Shifting Capability
- Three-State Outputs with Separate Enable Controls
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VCC = 5V, VDD = 10V
  - 2V at VCC = 10V, VDD = 15V
- Standardized Symmetrical Output Characteristics
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- High or Low Level Shifting with Three-State Outputs for Unidirectional or Bidirectional Bussing
- Isolation of Logic Subsystems Using Separate Power Supplies from Supply Sequencing, Supply Loss and Supply Regulation Considerations

Description

CD40109BMS contains four low-to-high voltage level shifting circuits. Each circuit will shift a low voltage digital logic input signal (A, B, C, D) with logical 1 = VCC and logical 0 = VSS to a higher voltage output signal (E, F, G, H) with logical 1 = VDD and logical 0 = VSS.

The CD40109BMS, unlike other low-to-high level shifting circuits, does not require the presence of the high voltage supply (VDD) before the application of either the low voltage supply (VCC) or the input signals. There are no restrictions on the sequence of application of VDD, VCC, or the input signals. In addition, with one exception there are no restrictions on the relative magnitudes of the supply voltages or input signals within the device maximum ratings, provided that the input signal swings between VSS and at least 0.7VCC; VCC may exceed VDD, and input signals may exceed VCC and VDD. When operated in the mode VCC > VDD, the CD40109BMS will operate as a high-to-low level shifter.

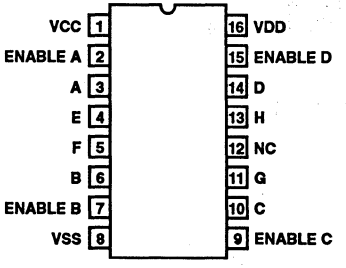
The CD40109BMS also features individual three-state output capability. A low level on any of the separately enabled three-state output controls produces a high impedance state in the corresponding output.

The CD40109BMS is supplied in these 16-lead outline packages:

Braze Seal DIP	H4T
Frit Seal DIP	H1E
Ceramic Flatpack	H6W

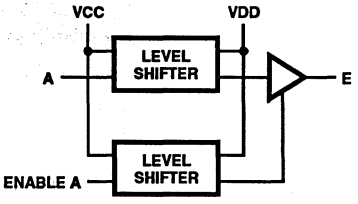
Pinout

CD40109BMS
TOP VIEW



Functional Diagram

1 OF 4 UNITS



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3196

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 10V, VOH > 9V, VOL < 1V VCC = 5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 10V, VOH > 9V, VOL < 1V VCC = 5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V, VCC = 10V		1, 2, 3	+25°C, +125°C, -55°C	-	3	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V, VCC = 10V		1, 2, 3	+25°C, +125°C, -55°C	7	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.4	-	µA
				2	+125°C	-12	-	µA
			VDD = 18V	3	-55°C	-0.4	-	µA
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.4	µA
				2	+125°C	-	12	µA
			VDD = 18V	3	-55°C	-	0.4	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Data In to Out Shift Mode L-H	TPHL1	VDD = 10V, VIN = VCC or GND VCC = 5V (Notes 1, 2)	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Propagation Delay Data In to Out Shift Mode L-H	TPLH1	VDD = 10V, VIN = VCC or GND VCC = 5V (Notes 1, 2)	9	+25°C	-	260	ns
			10, 11	+125°C, -55°C	-	351	ns
Propagation Delay Data In to Out Shift Mode H-L	TPHL2	VDD = 5V, VIN = VCC or GND VCC = 10V (Notes 1, 2)	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Propagation Delay Data In to Out Shift Mode H-L	TPLH2	VDD = 5V, VIN = VCC or GND VCC = 10V (Notes 1, 2)	9	+25°C	-	460	ns
			10, 11	+125°C, -55°C	-	621	ns
Transition Time Shift Mode L-H	TTHL1 TTLH1	VDD = 10V, VIN = VDD or GND VCC = 5V (Notes 1, 2)	9	+25°C	-	100	ns
			10, 11	+125°C, -55°C	-	135	ns
Transition Time Shift Mode H-L	TTHL2 TTLH2	VDD = 5V, VIN = VDD or GND VCC = 10V (Notes 1, 2)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Propagation Delay 3-State Shift Mode L-H	TPHZ1	VDD = 10V, VIN = VCC or GND VCC = 5V (Notes 2, 3)	9	+25°C	-	120	ns
			10, 11	+125°C, -55°C	-	162	ns
Propagation Delay 3-State Shift Mode H-L	TPHZ2	VDD = 5V, VIN = VCC or GND VCC = 10V (Notes 2, 3)	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay 3-State Shift Mode L-H	TPLZ1	VDD = 10V, VIN = VCC or GND VCC = 5V (Notes 2, 3)	9	+25°C	-	740	ns
			10, 11	+125°C, -55°C	-	999	ns
Propagation Delay 3-State Shift Mode H-L	TPLZ2	VDD = 5V, VIN = VCC or GND VCC = 10V (Notes 2, 3)	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Propagation Delay 3-State Shift Mode L-H	TPZH1	VDD = 10V, VIN = VCC or GND VCC = 5V (Notes 2, 3)	9	+25°C	-	640	ns
			10, 11	+125°C, -55°C	-	864	ns
Propagation Delay 3-State Shift Mode H-L	TPZH2	VDD = 5V, VIN = VCC or GND VCC = 10V (Notes 2, 3)	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Propagation Delay 3-State Shift Mode L-H	TPZL1	VDD = 10V, VIN = VCC or GND VCC = 5V (Notes 2, 3)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Propagation Delay 3-State Shift Mode H-L	TPZL2	VDD = 5V, VIN = VCC or GND VCC = 10V (Notes 2, 3)	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.
3. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V VCC = 5V	1, 2	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V VCC = 5V	1, 2	+25°C, +125°C, -55°C	3.5	-	V
Propagation Delay Data In to Data Out Shift Mode L-H	TPHL1	VDD = 15V, VCC = 5V	1, 2, 3	+25°C	-	440	ns
		VDD = 15V, VCC = 10V	1, 2, 3	+25°C	-	360	ns
Propagation Delay Data In to Out Shift Mode L-H	TPLH1	VDD = 15V, VCC = 5V	1, 2, 3	+25°C	-	240	ns
		VDD = 15V, VCC = 10V	1, 2, 3	+25°C	-	140	ns
Propagation Delay Data In to Out Shift Mode H-L	TPHL2	VDD = 5V, VCC = 15V	1, 2, 3	+25°C	-	500	ns
		VDD = 10V, VCC = 15V	1, 2, 3	+25°C	-	240	ns
Propagation Delay Data In to Out Shift Mode H-L	TPLH2	VDD = 5V, VCC = 15V	1, 2, 3	+25°C	-	460	ns
		VDD = 10V, VCC = 15V	1, 2, 3	+25°C	-	160	ns
Transition Time Shift Mode L-H	TTHL1 TTLH1	VDD = 15V, VCC = 5V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V, VCC = 10V	1, 2, 3	+25°C	-	80	ns
Transition Time Shift Mode H-L	TTHL2 TTLH2	VDD = 5V, VCC = 15V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V, VCC = 15V	1, 2, 3	+25°C	-	100	ns
Propagation Delay 3-State Shift Mode L-H	TPHZ1	VDD = 15V, VCC = 5V	1, 2, 4	+25°C	-	150	ns
		VDD = 15V, VCC = 10V	1, 2, 4	+25°C	-	70	ns
Propagation Delay 3-State Shift Mode H-L	TPHZ2	VDD = 5V, VCC = 5V	1, 2, 4	+25°C	-	400	ns
		VDD = 10V, VCC = 15V	1, 2, 4	+25°C	-	80	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay 3-State Shift Mode L-H	TPLZ1	VDD = 15V, VCC = 5V	1, 2, 4	+25°C	-	600	ns
		VDD = 15V, VCC = 10V	1, 2, 4	+25°C	-	500	ns
Propagation Delay 3-State Shift Mode H-L	TPLZ2	VDD = 5V, VCC = 15V	1, 2, 4	+25°C	-	500	ns
		VDD = 10V, VCC = 15V	1, 2, 4	+25°C	-	260	ns
Propagation Delay 3-State Shift Mode L-H	TPZH1	VDD = 15V, VCC = 5V	1, 2, 4	+25°C	-	460	ns
		VDD = 15V, VCC = 10V	1, 2, 4	+25°C	-	360	ns
Propagation Delay 3-State Shift Mode H-L	TPZH2	VDD = 5V, VCC = 15V	1, 2, 4	+25°C	-	600	ns
		VDD = 10V, VCC = 15V	1, 2, 4	+25°C	-	260	ns
Propagation Delay 3-State Shift Mode L-H	TPZL1	VDD = 15V, VCC = 5V	1, 2, 4	+25°C	-	160	ns
		VDD = 15V, VCC = 10V	1, 2, 4	+25°C	-	80	ns
Propagation Delay 3-State Shift Mode H-L	TPZL2	VDD = 5V, VCC = 15V	1, 2, 4	+25°C	-	400	ns
		VDD = 10V, VCC = 15V	1, 2, 4	+25°C	-	80	ns

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	4, 5, 11-13	2, 3, 6-10, 14, 15	1, 16			
Static Burn-In 2 (Note 1)	4, 5, 11-13	8	16	1-3, 4, 7, 9, 10, 14, 15		
Dynamic Burn-In (Note 4)	12	8	16	1, 4, 5, 11, 13	3, 6, 10, 14 (Note 3)	2, 7, 9, 15 (Note 3)
Irradiation (Note 2)	4, 5, 11-13	8	1-3, 6, 7, 9, 10, 14-16			

NOTES:

1. Each pin except Pin 1, VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except Pin 1, VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V
3. Pin voltage is VDD/2
4. Each pin except Pin 1, VDD and GND will have a series resistor of 4.75K ±5%, VDD = 18V ±0.5V.

Logic Diagram

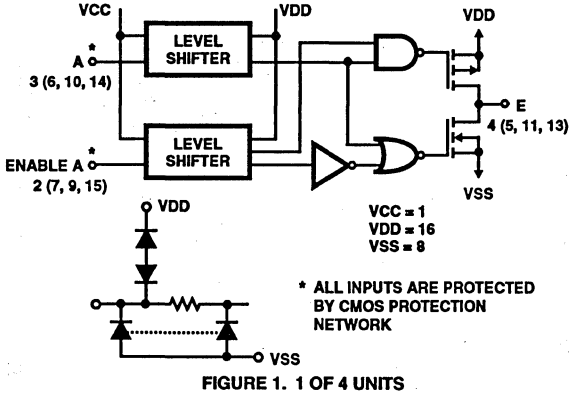


FIGURE 1. 1 OF 4 UNITS

TRUTH TABLE

INPUTS		OUTPUTS
A, B, C, D	ENABLE A, B, C, D	E, F, G, H
0	1	0
1	1	1
X	0	Z

Logic 0 = Low(VSS)
X = Don't care
Z = High Impedance
Logic 1 = VCC at Inputs and VDD at Outputs

7 LOGIC

Typical Performance Characteristics

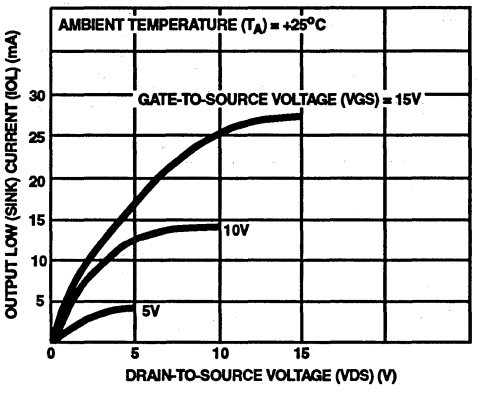


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

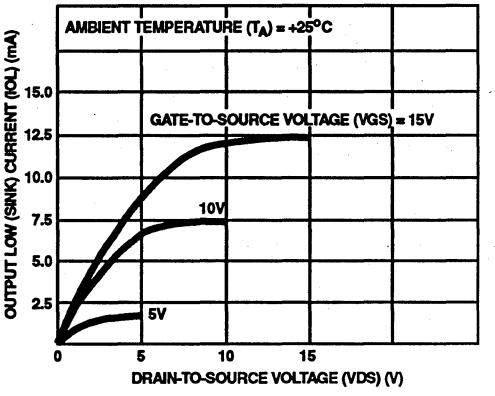


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

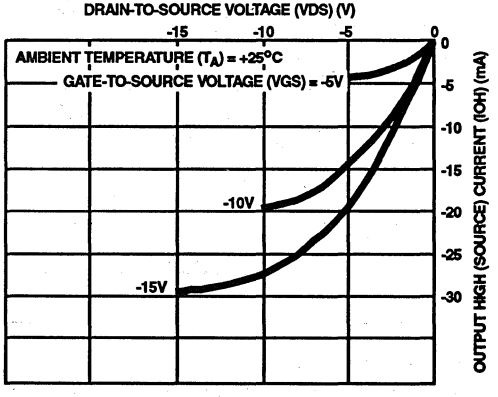


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

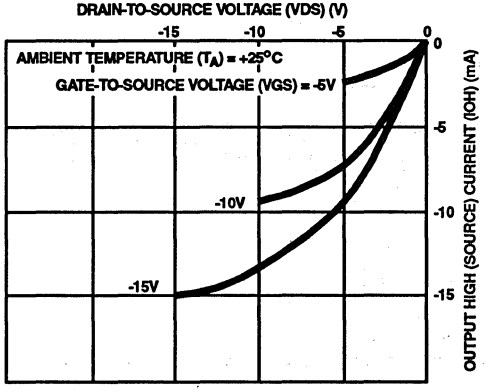


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

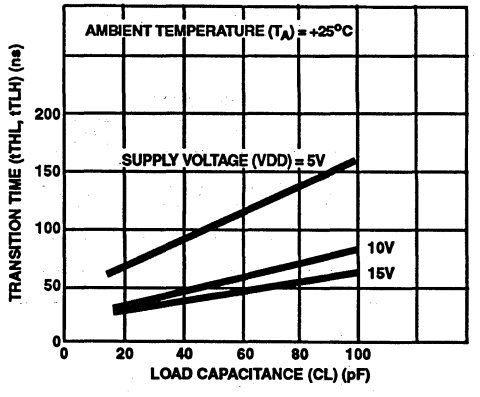


FIGURE 6. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

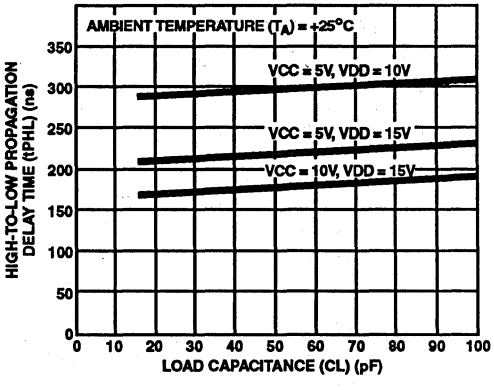


FIGURE 7. TYPICAL HIGH-TO-LOW PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

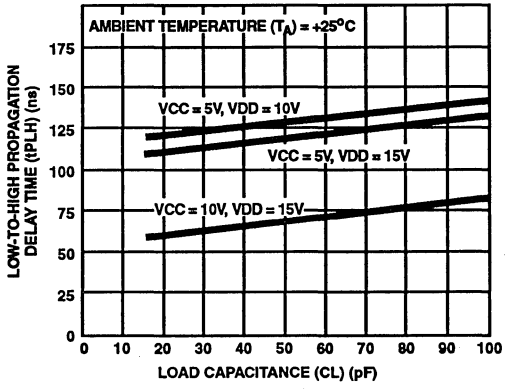


FIGURE 8. TYPICAL LOW-TO-HIGH PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

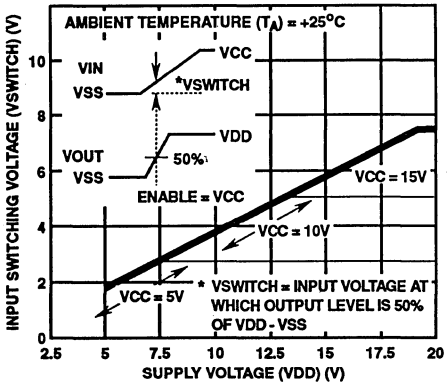


FIGURE 9. TYPICAL INPUT SWITCHING AS A FUNCTION OF HIGH LEVEL SUPPLY VOLTAGE

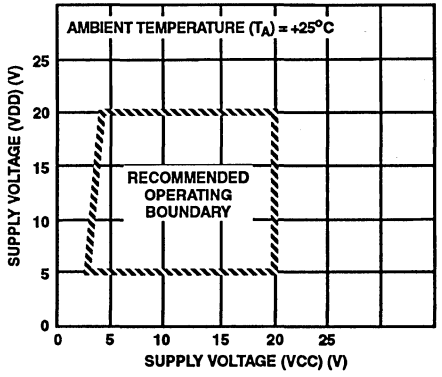


FIGURE 10. HIGH LEVEL SUPPLY VOLTAGE vs LOW LEVEL SUPPLY VOLTAGE

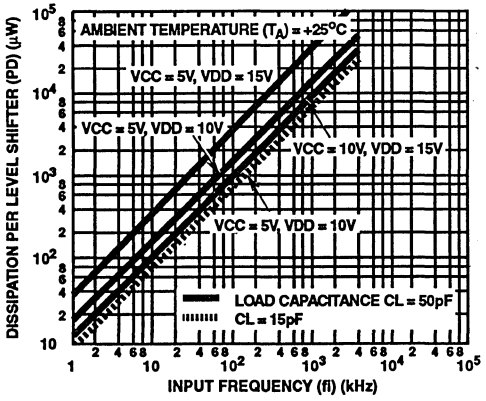
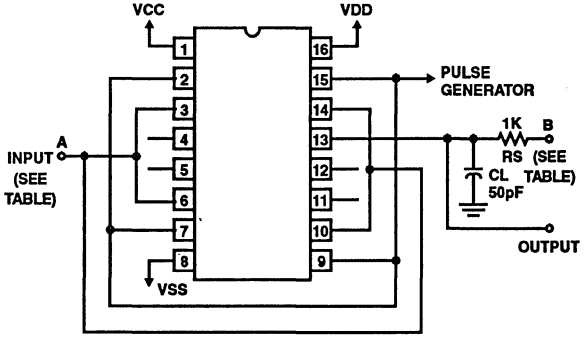


FIGURE 11. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

Test Circuit and Waveform



CHAR	TEST VOLTAGE AT A	AT B
tPHZ	VCC	VSS
tPLZ	VSS	VDD
tPZL	VSS	VDD
tPZH	VCC	VSS

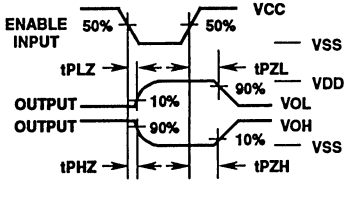
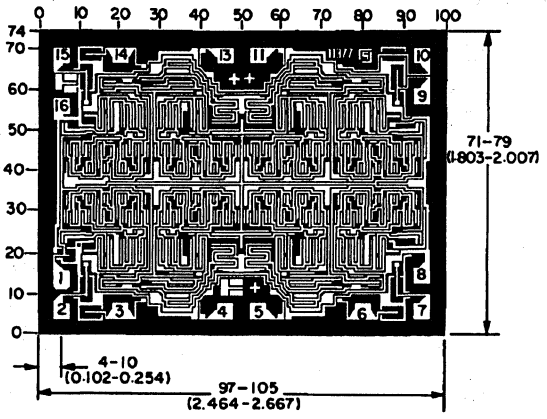


FIGURE 12. OUTPUT ENABLE DELAY TIMES TEST CIRCUIT AND WAVEFORMS

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

CD40147BMS

December 1992

10 Line to 4 Line BCD Priority Encoder

Features

- High Voltage Type (20V Rating)
- Encodes 10 Line to 4 Line BCD
- Active Low Inputs and Outputs
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Standardized Symmetrical Output Characteristics
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Keyboard Encoding
- 10 Line to BCD Encoding
- Range Selection

Description

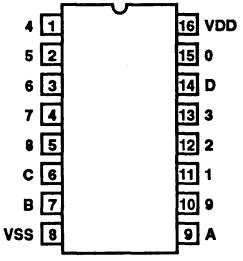
CD40147BMS CMOS encoder features priority encoding of the inputs to ensure that only the highest order data line is encoded. Ten data input lines (0-9) are encoded to four line (8, 4, 2, 1) BCD. The highest priority line is line 9. All four output lines are logic 1 (VSS) when all input lines are logic 0. All inputs and outputs are buffered, and each output can drive one TTL low power Schottky load. The CD40147BMS is functionally similar to the TTL 54/74147 if pin 15 is tied low.

The CD40147BMS is supplied in these 16-lead outline packages:

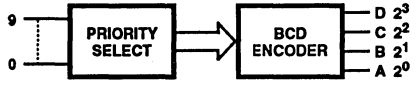
Braze Seal DIP	H4T
Frit Seal DIP	H1E
Ceramic Flatpack	H6W

Pinout

CD40147BMS
TOP VIEW



Functional Diagram



7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3357

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay In Phase Output	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	900	ns
			10, 11	+125°C, -55°C	-	1215	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay In Phase Output	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	400	ns
		VDD = 15V	1, 2, 3	+25°C	-	300	ns
Propagation Delay Out of Phase Output	TPHL TPLH	VDD = 5V	1, 2, 3	+25°C	-	850	ns
		VDD = 10V	1, 2, 3	+25°C	-	350	ns
		VDD = 15V	1, 2, 3	+25°C	-	250	ns
Transition Time	TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	6, 7, 9, 14	1-5, 8, 10-13, 15	16			
Static Burn-In 2 Note 1	6, 7, 9, 14	8	1-5, 10-13, 15, 16			
Dynamic Burn-In Note 1	-	8	16	6, 7, 9, 14	1, 3, 11, 13	2, 4, 5, 10, 12, 15
Irradiation Note 2	6, 7, 9, 14	8	1-5, 10-13, 15, 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram

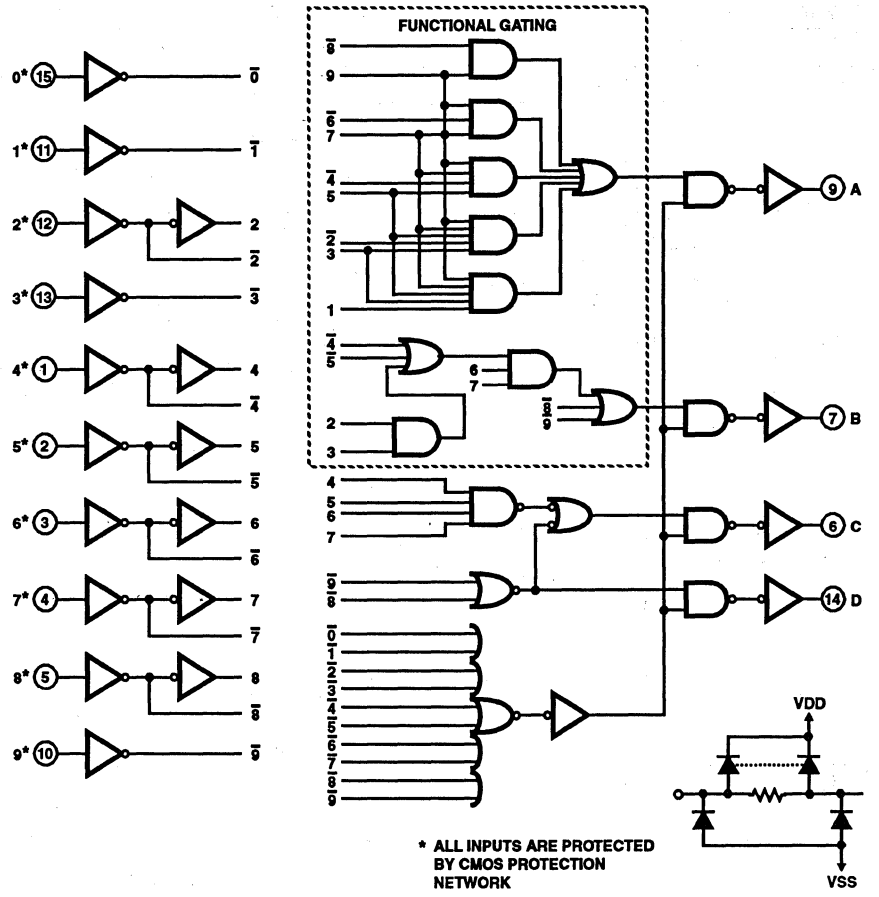


FIGURE 1.

TRUTH TABLE (Negative Logic)

INPUTS										OUTPUTS			
0	1	2	3	4	5	6	7	8	9	D	C	B	A
0	0	0	0	0	0	0	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0	0	0	0
X	1	0	0	0	0	0	0	0	0	0	0	0	1
X	X	1	0	0	0	0	0	0	0	0	0	1	0
X	X	X	1	0	0	0	0	0	0	0	0	1	1
X	X	X	X	1	0	0	0	0	0	0	1	0	0
X	X	X	X	X	1	0	0	0	0	0	1	0	1
X	X	X	X	X	X	1	0	0	0	0	1	1	0
X	X	X	X	X	X	X	1	0	0	0	1	1	1
X	X	X	X	X	X	X	X	1	0	1	0	0	0
X	X	X	X	X	X	X	X	X	1	1	0	0	1

0 = High level 1 = Low level X = Don't care

Typical Performance Characteristics

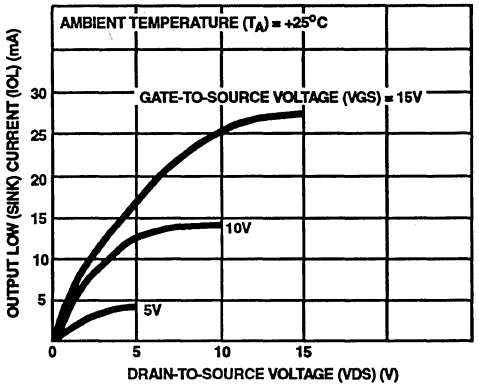


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

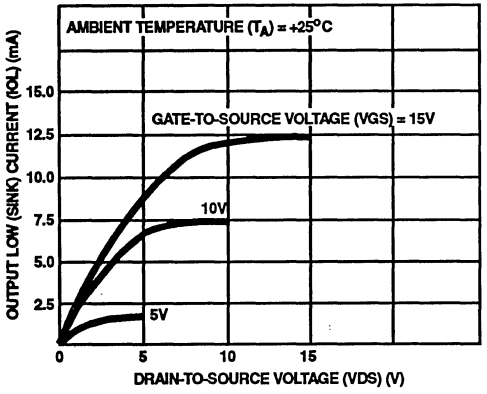


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

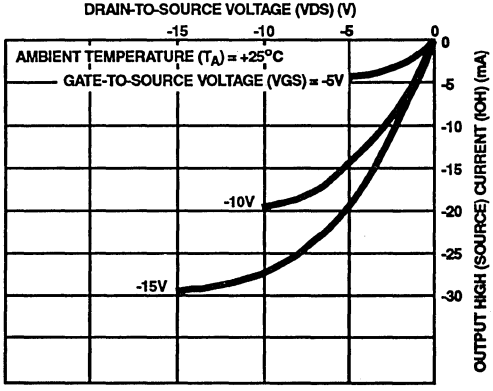


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

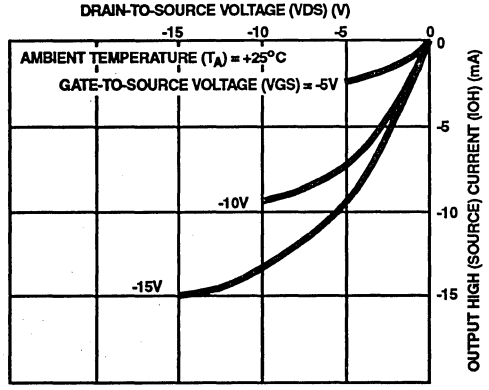


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

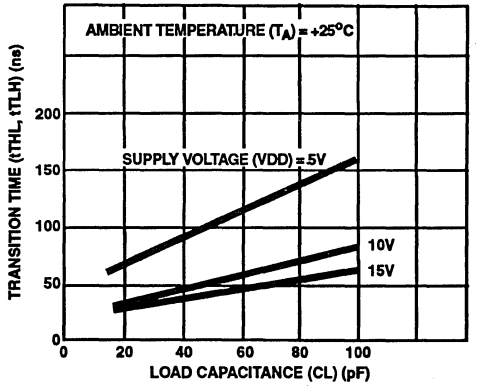


FIGURE 6. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

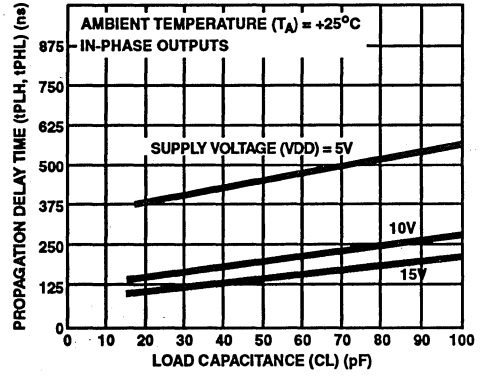


FIGURE 7. PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

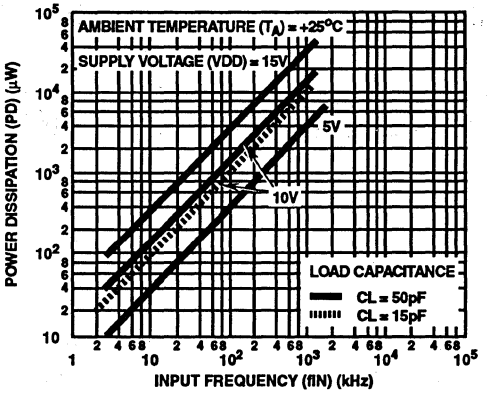
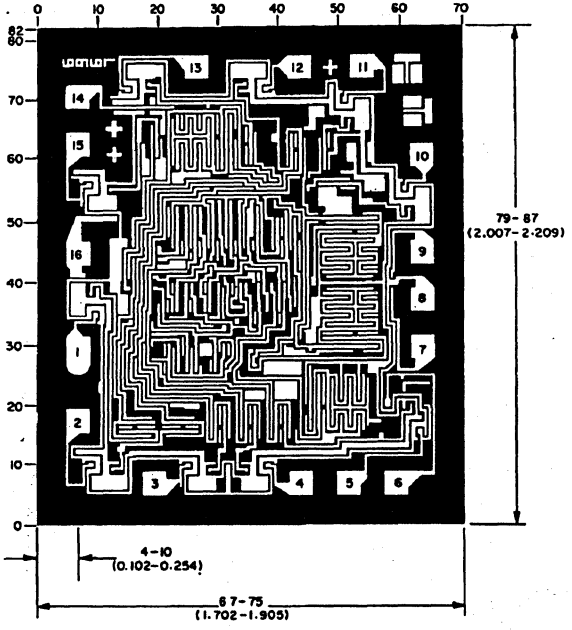


FIGURE 8. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD40160BMS, CD40161BMS CD40162BMS, CD40163BMS

CMOS Synchronous Programmable 4-Bit Counters

December 1992

Features

- High-Voltage Types (20V Rating)
- CD40160BMS Decade with Asynchronous Clear
- CD40161BMS Binary with Asynchronous Clear
- CD40162BMS Decade with Synchronous Clear
- CD40163BMS Binary with Synchronous Clear
- Internal Look-Ahead for Fast Counting
- Carry Output for Cascading
- Synchronously Programmable
- Clear Asynchronous Input (CD40160BMS, CD40161BMS)
- Clear Synchronous Input (CD40162BMS, CD40163BMS)
- Synchronous Load Control Input
- Low Power TTL Compatibility
- Standardized Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Programmable Binary and Decade Counting
- Counter Control/Timers
- Frequency Dividing

Description

CD40160BMS, CD40161BMS, CD40162BMS and CD40163BMS are 4-bit synchronous programmable counters. The CLEAR function of the CD40162BMS and CD40163BMS is synchronous and a low level at the $\overline{\text{CLEAR}}$ input sets all four outputs low on the next positive CLOCK edge. The CLEAR function of the CD40160BMS and CD40161BMS is asychronous and a low level at the $\overline{\text{CLEAR}}$ input sets all four outputs low regardless of the state of the CLOCK, $\overline{\text{LOAD}}$, or ENABLE inputs. A low level at the $\overline{\text{LOAD}}$ input disables the counter and causes the output to agree with the setup data after the next CLOCK pulse regardless of the conditions of the ENABLE inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output (COUT). Counting is enabled when both PE and TE inputs are high. The TE input is fed forward to enable COUT. This enabled output produces a positive output pulses with a duration approximately equal to the positive portion of the Q1 output. This positive overflow carry pulse can be used to enable successive cascaded stages. Logic transitions at the PE or TE inputs may occur when the clock is either high or low.

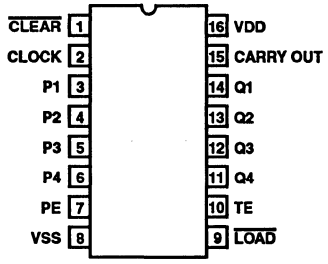
The CD40160BMS through CD40163BMS types are functionally equivalent to and pin-compatible with the TTL counter series 74LS160 through 74LS163 respectively.

The CD40160BMS, CD40161BMS, CD40162BMS and CD40163BMS are supplied in these 16 lead outline packages:

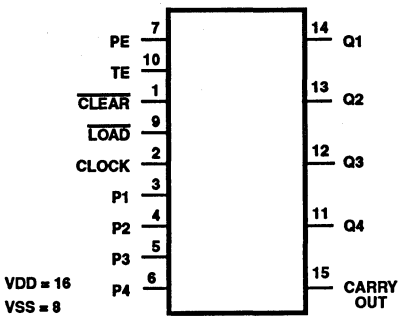
	CD40160	CD40161	CD40162	CD40163
Braze Seal DIP	H4W	H4X	H4X	H4W
Frit Seal DIP	H1F	H1F	H1L	H1F
Ceramic Flatpack	H6P	H6W	H6P	H6W

Pinout

CD40160BMS, CD40161BMS, CD40162BMS, CD40163BMS
TOP VIEW



Functional Diagram



7 LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3358

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Q	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay Clock to COut	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	450	ns
			10, 11	+125°C, -55°C	-	608	ns
Propagation Delay TE to COut	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	250	ns
			10, 11	+125°C, -55°C	-	338	ns
Propagation Delay CD40160BMS, $\overline{\text{CD40161BMS}}$ Clear to Q	TPHL4	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	2	-	MHz
			10, 11	+125°C, -55°C	1.48	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Clock to Q	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Propagation Delay Clock to C Out	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	190	ns
		VDD = 15V	1, 2, 3	+25°C	-	140	ns
Propagation Delay TE to C Out	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25°C	-	110	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Propagation Delay CD40160BMS, CD40161BMS Clear to Q	TPHL4	VDD = 10V	1, 2, 3	+25°C	-	220	ns
		VDD = 15V	1, 2, 3	+25°C	-	160	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	5.5	-	MHz
		VDD = 15V	1, 2, 3	+25°C	8	-	MHz
Maximum Clock Rise or Fall Time	TRCL TFCL	VDD = 5V	1, 2, 3, 4	+25°C	-	200	µs
		VDD = 10V	1, 2, 3, 4	+25°C	-	70	µs
		VDD = 15V	1, 2, 3, 4	+25°C	-	15	µs
Minimum Data Hold Time Clock Operation	TH	VDD = 5V	1, 2, 3	+25°C	-	0	ns
		VDD = 10V	1, 2, 3	+25°C	-	0	ns
		VDD = 15V	1, 2, 3	+25°C	-	0	ns
Minimum Clock Pulse Width Clock Operation	TW	VDD = 5V	1, 2, 3	+25°C	-	170	ns
		VDD = 10V	1, 2, 3	+25°C	-	70	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Setup Time Data to Clock	TS	VDD = 5V	1, 2, 3	+25°C	-	240	ns
		VDD = 10V	1, 2, 3	+25°C	-	90	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Minimum Setup Time $\overline{\text{Load}}$ to Clock	TS	VDD = 5V	1, 2, 3	+25°C	-	240	ns
		VDD = 10V	1, 2, 3	+25°C	-	90	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Minimum Setup Time PE to TE to Clock	TS	VDD = 5V	1, 2, 3	+25°C	-	340	ns
		VDD = 10V	1, 2, 3	+25°C	-	140	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Minimum $\overline{\text{Clear}}$ Pulse Width (CD40160BMS, CD40161BMS)	TW	VDD = 5V	1, 2, 3	+25°C	-	170	ns
		VDD = 10V	1, 2, 3	+25°C	-	70	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Setup Time $\overline{\text{Clear}}$ to Clock (CD40162BMS, CD40163BMS)	TS	VDD = 5V	1, 2, 3	+25°C	-	340	ns
		VDD = 10V	1, 2, 3	+25°C	-	140	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Minimum Hold Time $\overline{\text{Clear}}$ to Clock (CD40162BMS, CD40163BMS)	TH	VDD = 5V	1, 2, 3	+25°C	-	0	ns
		VDD = 10V	1, 2, 3	+25°C	-	0	ns
		VDD = 15V	1, 2, 3	+25°C	-	0	ns
Minimum $\overline{\text{Clear}}$ Removal Time (CD40160BMS, CD40161BMS)	TREM	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	70	ns

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. If more than one unit is cascaded, TRCL should be made less than or equal to the sumof the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	11 - 15	1 - 10	16			
Static Burn-In 2 Note 1	11 - 15	8	1 - 7, 9, 10, 16			
Dynamic Burn-In Note 1	-	8	1, 7, 9, 10, 16	11 - 15	2 - 6	-
Irradiation Note 2	11 - 15	8	1 - 7, 9, 10, 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagrams

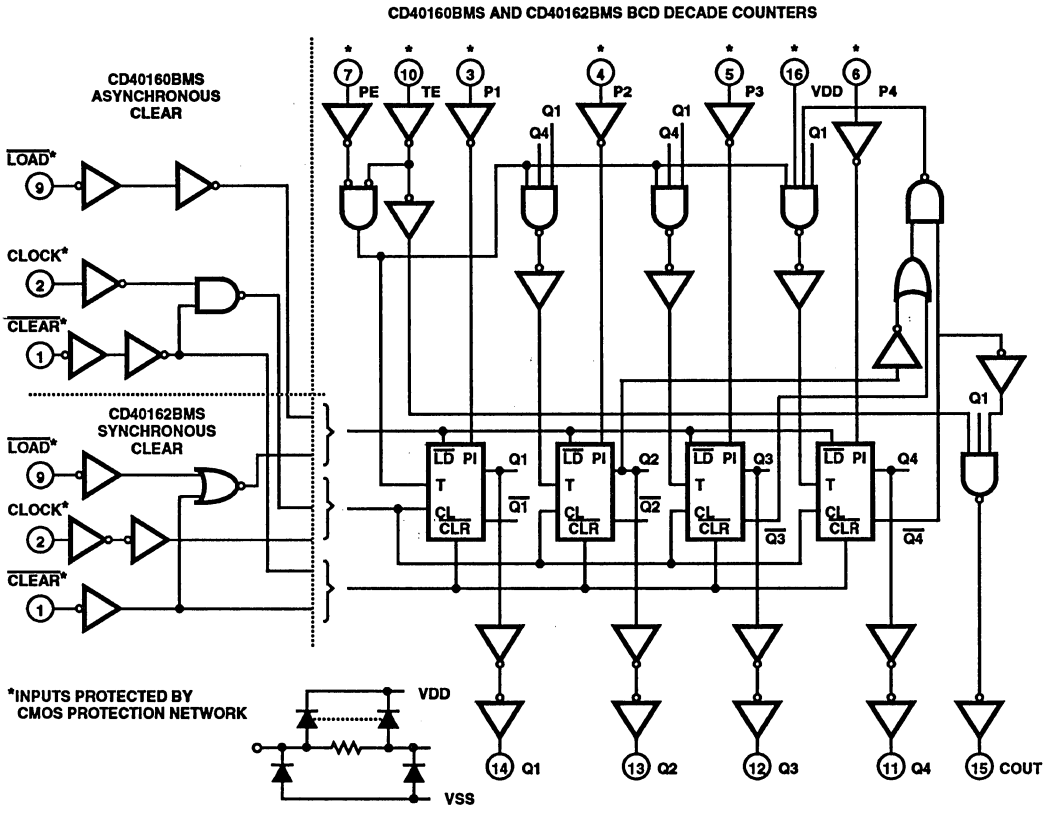


FIGURE 1. LOGIC DIAGRAM FOR CD40160BMS AND CD40162BMS BCD DECADE COUNTERS

Logic Diagrams (Continued)

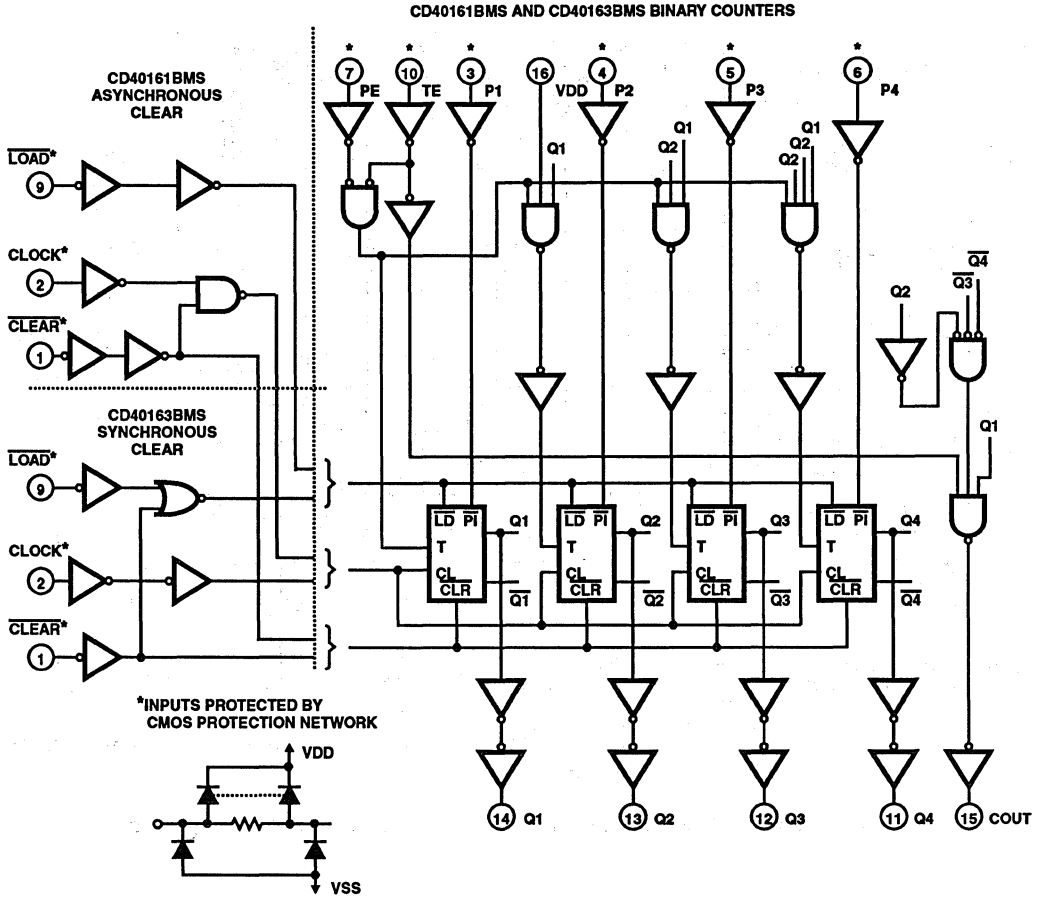


FIGURE 2. LOGIC DIAGRAM FOR CD40161BMS AND CD40163BMS BINARY COUNTERS

TRUTH TABLE

CLOCK	$\overline{CLR}$	$\overline{LOAD}$	PE	TE	OPERATION
⎍	1	0	X	X	Preset
⎍	1	1	0	X	NC
⎍	1	1	X	0	NC
⎍	1	1	1	1	Count
X	0	X	X	X	Reset (CD40160BMS, CD40161BMS)
⎍	0	X	X	X	Reset (CD40162BMS, CD40163BMS)
⎎	1	X	X	X	NC (CD40162BMS, CD40163BMS)

1 = High Level
0 = Low Level

X = Don't Care
NC = No Change

Typical Performance Characteristics

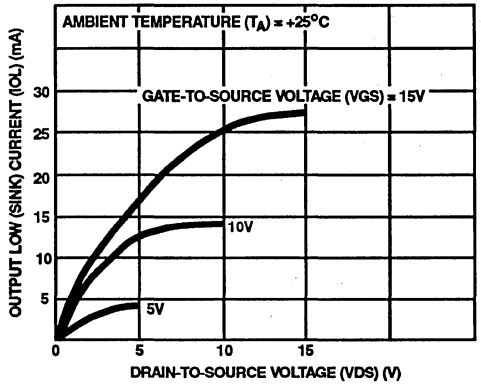


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

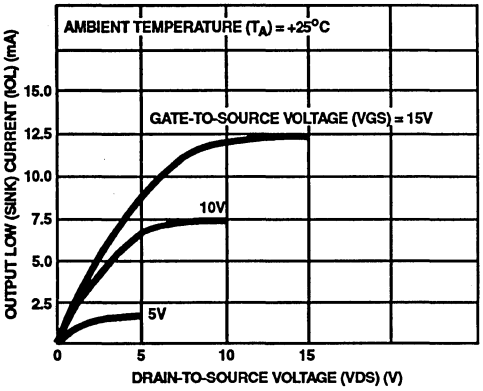


FIGURE 4. MIMIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

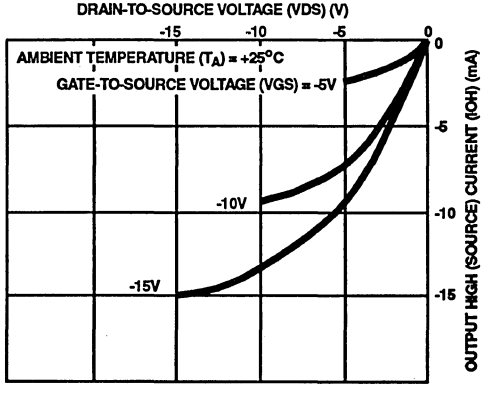


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

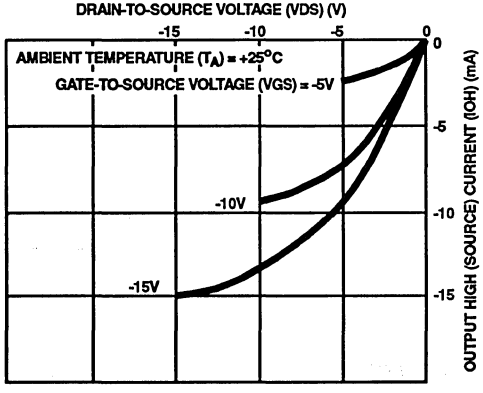


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

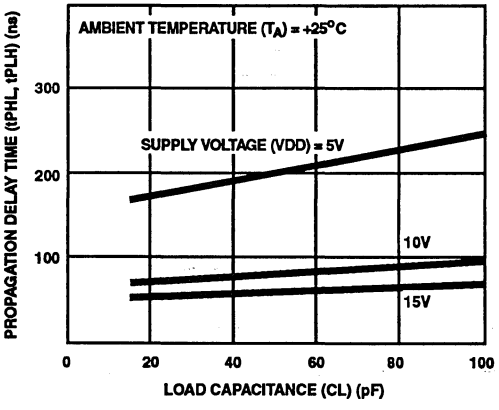


FIGURE 7. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (CLOCK TO Q)

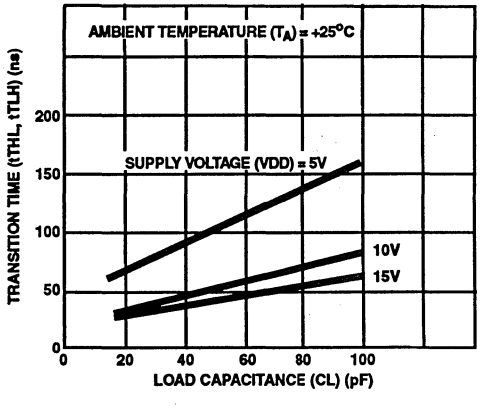


FIGURE 8. TYPICAL TRANSISTION TIME AS A FUNCTION OF LOAD CAPACITANCE

7 LOGIC

Typical Performance Characteristics (Continued)

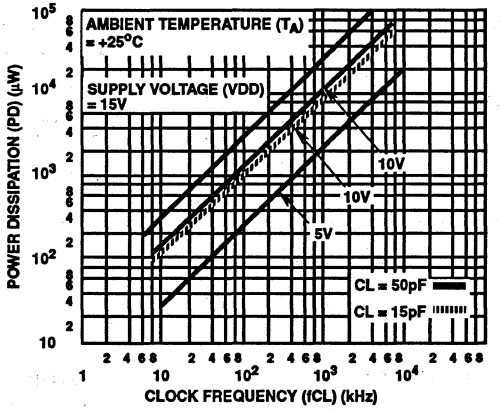


FIGURE 9. TYPICAL POWER DISSIPATION AS A FUNCTION OF CLOCK FREQUENCY

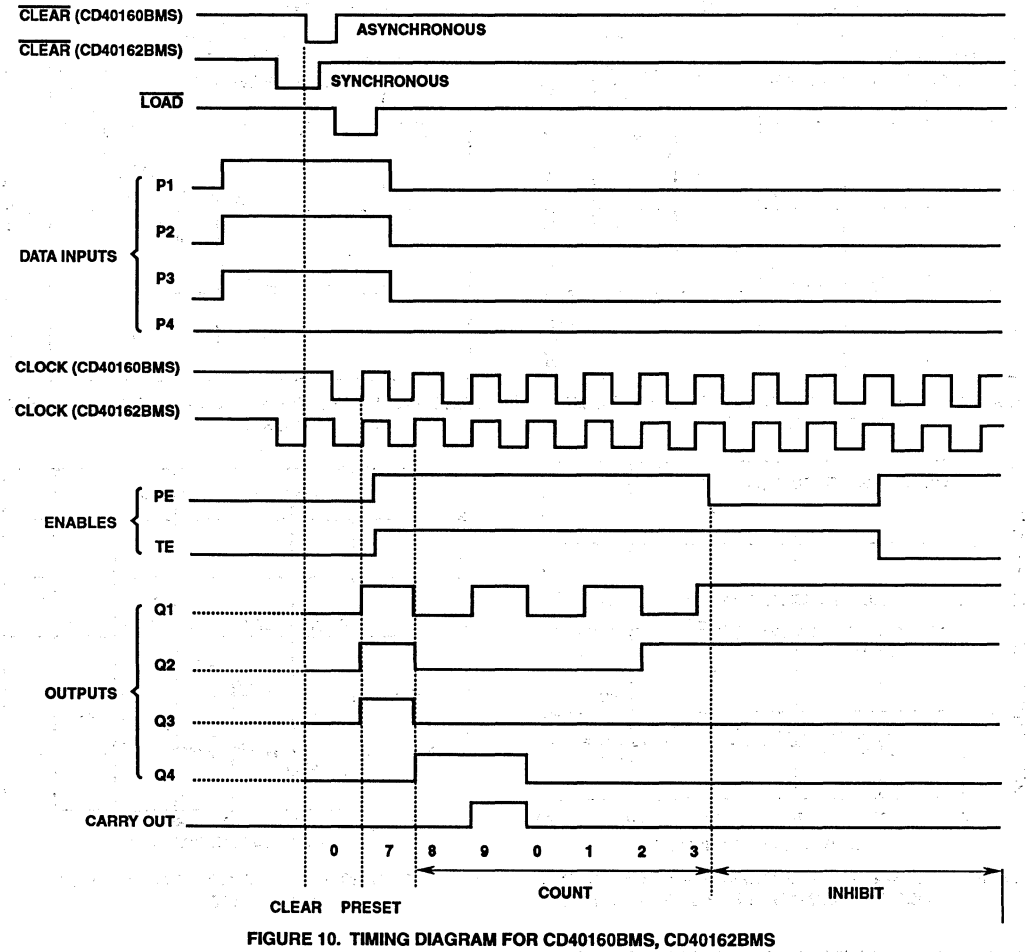


FIGURE 10. TIMING DIAGRAM FOR CD40160BMS, CD40162BMS

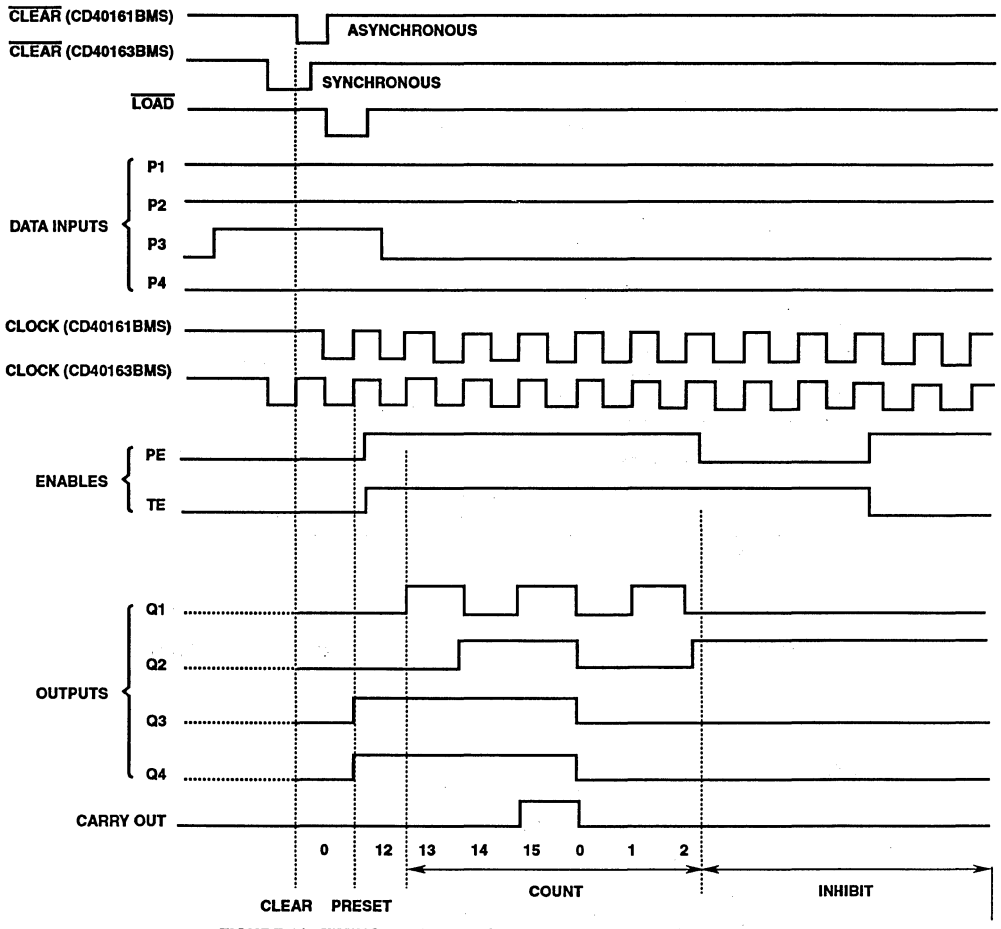


FIGURE 11. TIMING DIAGRAM FOR CD40161BMS AND CD40163BMS

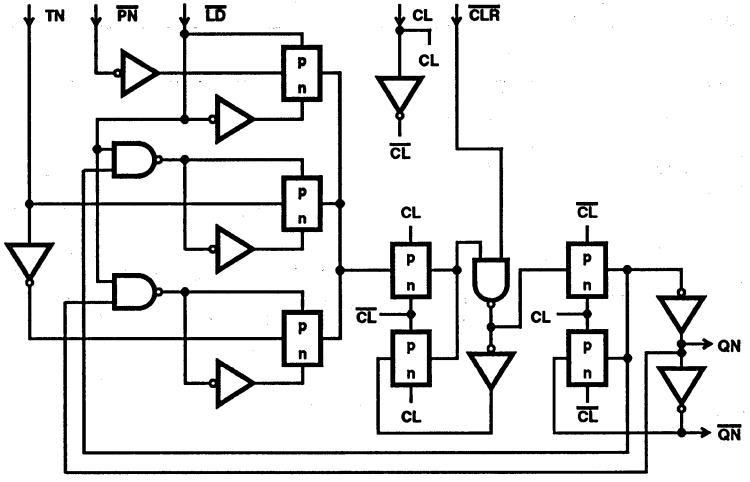


FIGURE 12. DETAIL OF FLIP-FLOPS OF CD40160BMS AND CD40161BMS (ASYNCHRONOUS CLEAR)

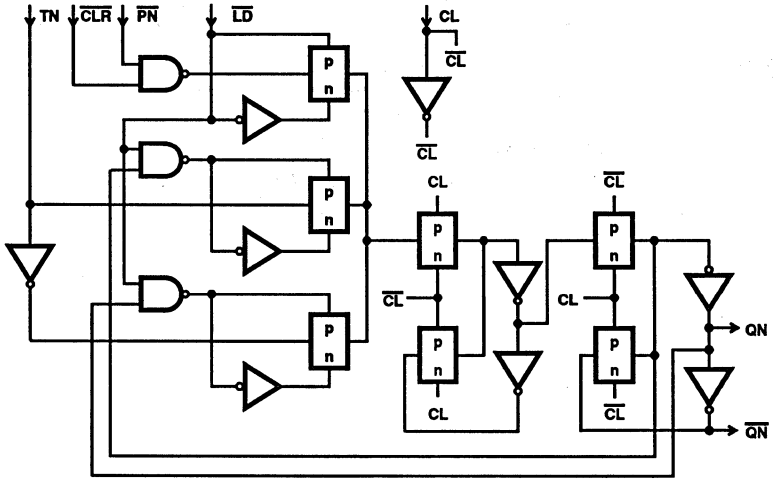


FIGURE 13. DETAIL OF FLIP-FLOPS OF CD40162BMS AND CD40163BMS (SYNCHRONOUS CLEAR)

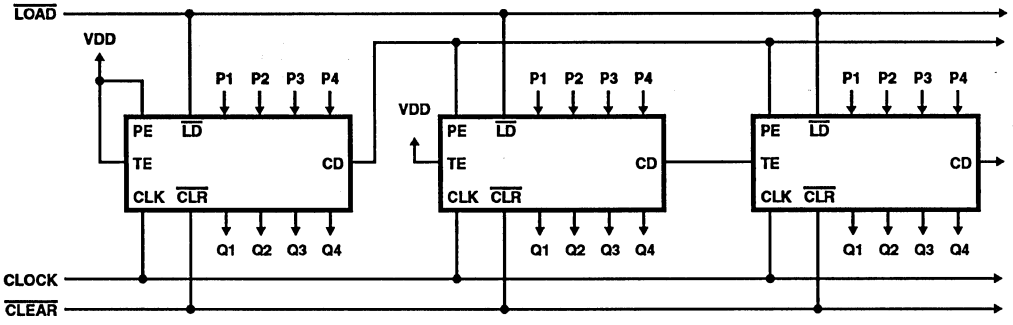


FIGURE 14. CASCADED COUNTER PACKAGES IN THE PARALLEL-CLOCKED MODE

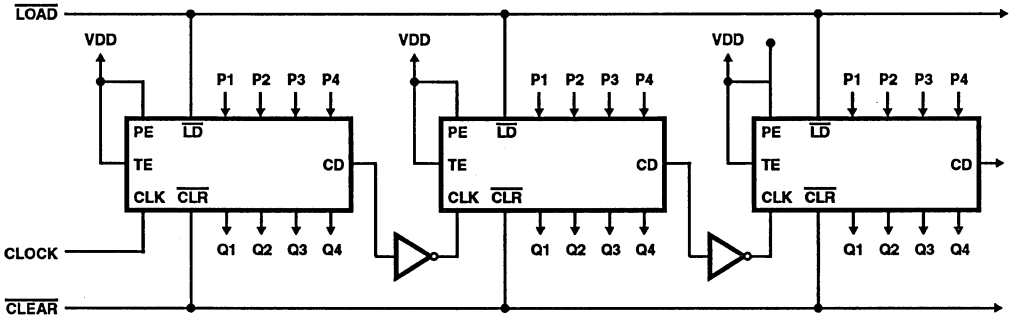
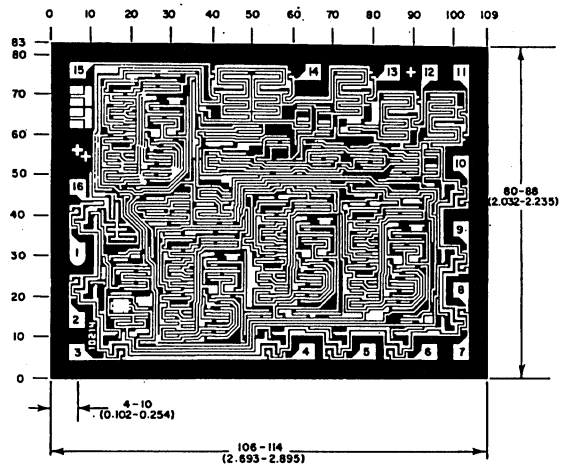


FIGURE 15. CASCADED COUNTER PACKAGES IN THE RIPPLE-CLOCKED MODE

Chip Dimensions and Pad Layout



Dimensions and pad layout for CD40160BMSH.
Dimensions and pad layout for CD40161BMS, CD40162BMSH, and CD40163BMSH are identical.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD40174BMS

December 1992

CMOS Hex 'D'-Type Flip-Flop

Features

- High Voltage Type (20V Rating)
- 5V, 10V and 15V Parametric Ratings
- Standardized, Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range, 100nA at 18V and +25°C
- Noise Margin (Over full Package Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Shift Registers
- Buffer/Storage Registers
- Pattern Generators

Description

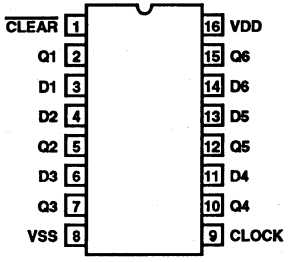
CD40174BMS consists of six identical 'D'-Type flip-flops having independent DATA inputs. The CLOCK and $\overline{\text{CLEAR}}$ inputs are common to all six units. Data is transferred to the Q outputs on the positive going transition of the clock pulse. All six flip-flops are simultaneously reset by a low level on the $\overline{\text{CLEAR}}$ input.

The CD40174BMS is supplied in these 16 lead outline packages:

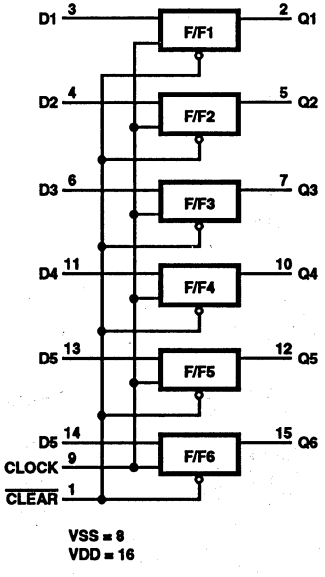
Braze Seal DIP	H4T
Frit Seal DIP	H1E
Ceramic Flatpack	H6W

Pinout

CD40174BMS
TOP VIEW



Functional Diagram



File Number 3359

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL5	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH5	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL15	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH15	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (Note 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Output	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	300	ns
			10, 11	+125°C, -55°C	-	405	ns
Propagation Delay $\overline{\text{CLEAR}}$ to Output	TPHL2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	3.5	-	MHz
			10, 11	+125°C, -55°C	3.5/1.35	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5B	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Clock to Output	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	140	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Propagation Delay $\overline{\text{CLEAR}}$ to Output	TPHL2	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	6	-	MHz
		VDD = 15V	1, 2, 3	+25°C	8	-	MHz
Minimum Data Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	40	ns
		VDD = 10V	1, 2, 3	+25°C	-	20	ns
		VDD = 15V	1, 2, 3	+25°C	-	10	ns
Minimum Data Hold Time	TH	VDD = 5V	1, 2, 3	+25°C	-	80	ns
		VDD = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V	1, 2, 3	+25°C	-	30	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	130	ns
		VDD = 10V	1, 2, 3	+25°C	-	60	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Maximum Clock Rise and Fall Time	TRCL TFCL	VDD = 5V	1, 2, 3, 4	+25°C	15	-	µs
		VDD = 10V	1, 2, 3, 4	+25°C	15	-	µs
		VDD = 15V	1, 2, 3, 4	+25°C	15	-	µs
Minimum $\overline{\text{CLEAR}}$ Removal Time	TREM	VDD = 5V	1, 2, 3	+25°C	-	0	ns
		VDD = 10V	1, 2, 3	+25°C	-	0	ns
		VDD = 15V	1, 2, 3	+25°C	-	0	ns
Minimum $\overline{\text{CLEAR}}$ Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	100	ns
		VDD = 10V	1, 2, 3	+25°C	-	50	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Input Capacitance	CIN	$\overline{\text{CLEAR}}$	1, 2	+25°C	-	40	pF
		All others	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. If more than one unit is cascaded, TRCL should be made less than or equal to the sumof the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	2, 5, 7, 10, 12, 15	1, 3, 4, 6, 8, 9, 11, 13, 14	16			
Static Burn-In 2 (Note 1)	2, 5, 7, 10, 12, 15	8	1, 3, 4, 6, 9, 11, 13, 14, 16			
Dynamic Burn-In (Note 1)	-	8	1, 16	2, 5, 7, 10, 12, 15	9	3, 4, 6, 11, 13, 14
Irradiation (Note 2)	2, 5, 7, 10, 12, 15	8	1, 3, 4, 6, 9, 11, 13, 14, 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram

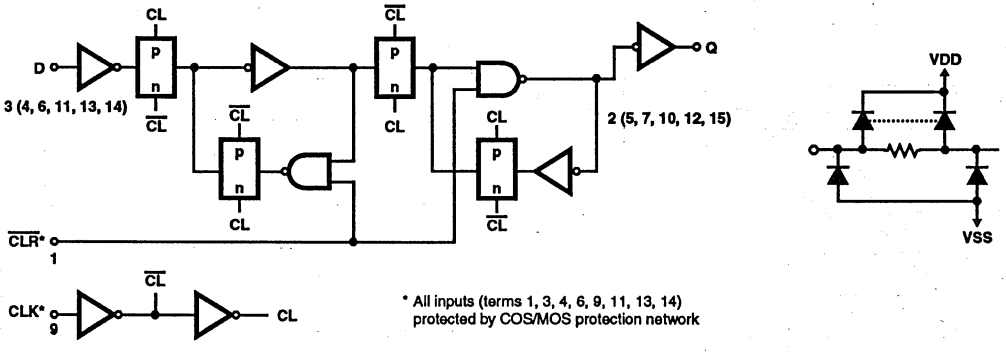


FIGURE 1. 1 OF 6 FLIP-FLOPS

TRUTH TABLE FOR 1 OF 6 FLIP-FLOPS

INPUTS			OUTPUT
CLOCK	DATA	$\overline{\text{CLEAR}}$	Q
⌐	0	1	0
⌐	1	1	1
⌐	X	1	NC
X	X	0	0

1 = High Level
2 = Low Level
X = Don't Care
NC = No Change

Typical Performance Curves

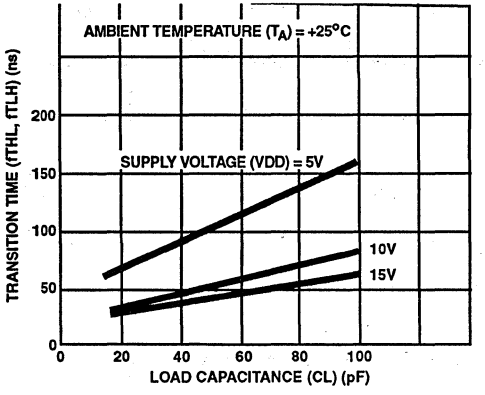


FIGURE 2. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

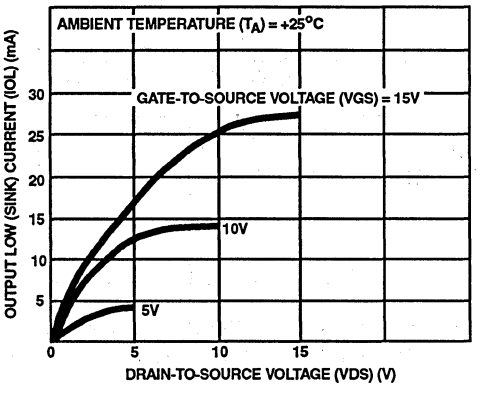


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

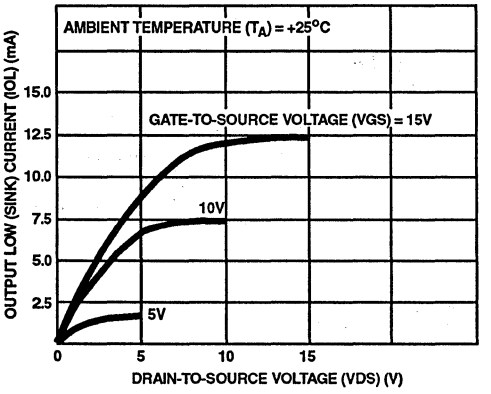


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

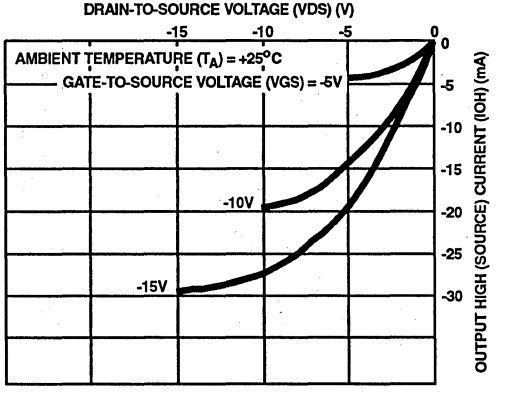


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

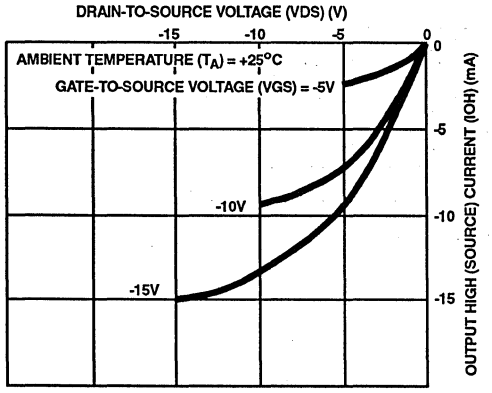


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

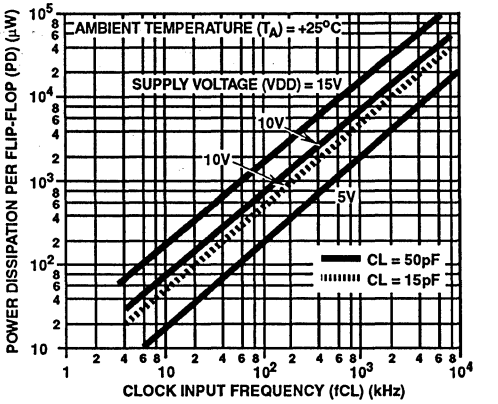


FIGURE 7. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF CLOCK FREQUENCY

Typical Performance Curves (Continued)

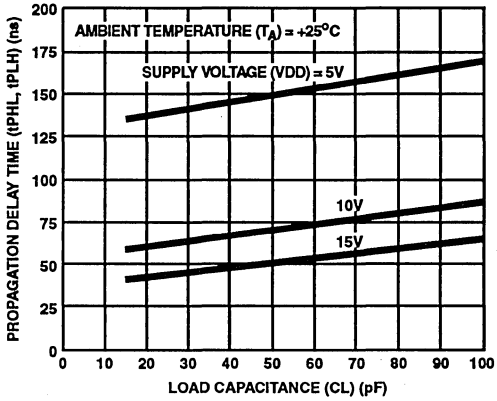


FIGURE 8. TYPICAL PROPAGATION DELAY TIME (CLOCK TO OUTPUT) AS A FUNCTION OF LOAD CAPACITANCE

Waveform

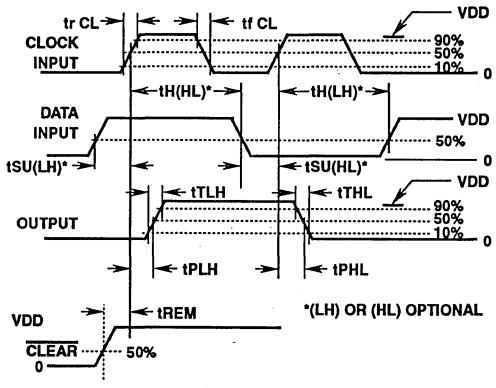
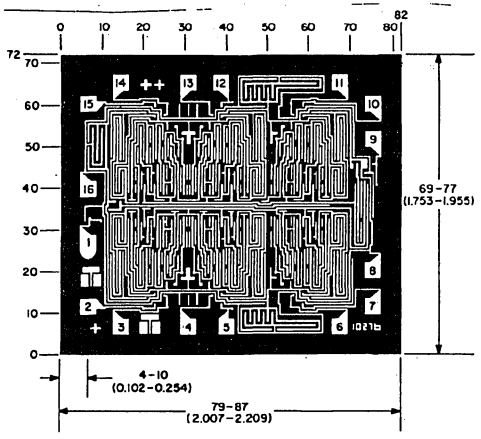


FIGURE 9. DEFINITION OF SETUP, HOLD, PROPAGATION DELAY, AND REMOVAL TIMES

Pad Layout



DIMENSIONS AND PAD LAYOUT FOR CD40174BMSH

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to +16 mils applicable to the nominal dimensions shown.

Dimension in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD40175BMS

December 1992

CMOS Quad 'D' Type Flip-Flop

Features

- High Voltage Type (20V Rating)
- Output Compatible with Two HTL Loads, Two Low Power TTL Loads, or One Low Power Schottky TTL Load
- Functional Equivalent to TTL74175
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Standardized Symmetrical Output Characteristics
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Shift Registers
- Buffer/Storage Registers
- Pattern Generators

Description

CD40175BMS consists of four identical D-type flip-flops. Each flip-flop has an independent DATA D input and complementary Q and $\overline{Q}$ outputs. The CLOCK and CLEAR inputs are common to all flip-flops. Data are transferred to the Q outputs on the positive going transition of the clock pulse. All four flip-flops are simultaneously reset by a low level on the CLEAR input.

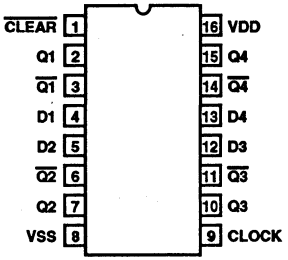
These devices can function as shift register elements or as T-type flip-flops for toggle and counter applications.

The CD40175BMS is supplied in these 16-lead outline packages:

Braze Seal DIP	H4T
Ceramic Flatpack	H6W

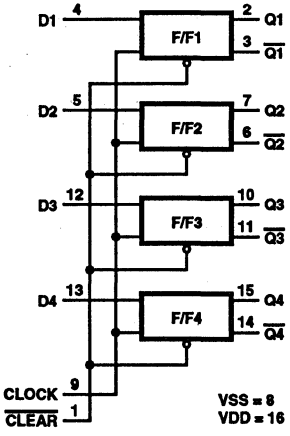
Pinout

CD40175BMS
TOP VIEW



VDD = PIN 16
VSS = PIN 8

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3360

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTES 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Q Output	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay Clear to Q Output	TPHL2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	2	-	MHz
			10, 11	+125°C, -55°C	1.48	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Clock to Q Output	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Propagation Delay $\overline{\text{Clear}}$ to Q Output	TPHL2	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	150	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Minimum Data Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	120	ns
		VDD = 10V	1, 2, 3	+25°C	-	50	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Minimum Data Hold Time	TH	VDD = 5V	1, 2, 3	+25°C	-	80	ns
		VDD = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V	1, 2, 3	+25°C	-	30	ns
Minimum $\overline{\text{Clear}}$ Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Maximum Clock Rise or Fall Time	TRCL TFCL	VDD = 5V	1, 2, 3, 4	+25°C	15	-	µs
		VDD = 10V	1, 2, 3, 4	+25°C	15	-	µs
		VDD = 15V	1, 2, 3, 4	+25°C	15	-	µs
Minimum $\overline{\text{Clear}}$ Removal Time ($\overline{\text{Clear}}$ to be High before Positive Transition of Clock)	TREM	VDD = 5V	1, 2, 3	+25°C	-	250	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	250	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	75	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. If more than one unit is cascaded, TRCL should be made less than or equal to the sumof the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

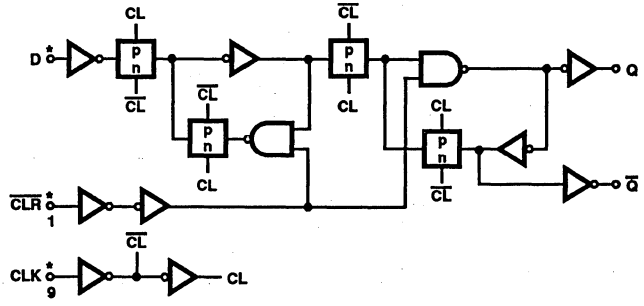
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

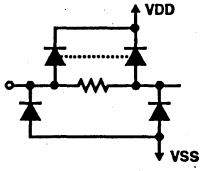
FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	2, 3, 6, 7, 10, 11, 14, 15	1, 4, 5, 8, 9, 12, 13	16			
Static Burn-In 2 (Note 1)	2, 3, 6, 7, 10, 11, 14, 15	8	1, 4, 5, 9, 12, 13, 16			
Dynamic Burn-In (Note 1)	-	8	1, 16	2, 3, 6, 7, 10, 11, 14, 15	9	4, 5, 12, 13
Irradiation (Note 2)	2, 3, 6, 7, 10, 11, 14, 15	8	1, 4, 5, 9, 12, 13, 16			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram





* ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

FIGURE 1. 1 OF 4 FLIP-FLOPS

TRUTH TABLE FOR 1 OF 4 FLIP-FLOPS (Positive Logic)

INPUTS			OUTPUTS	
CLOCK	DATA	$\overline{CLEAR}$	Q	$\overline{Q}$
⎍	0	1	0	1
⎍	1	1	1	0
⎎	X	1	Q	$\overline{Q}$
X	X	0	0	1

1 = High level
X = Don't care
0 = Low level

Electrical Performance Characteristics

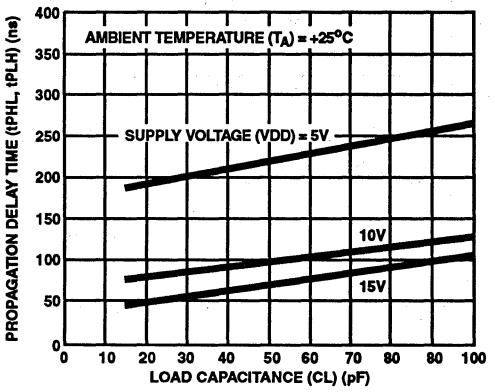


FIGURE 2. TYPICAL PROPAGATION DELAY TIME (CLOCK TO OUTPUT) AS A FUNCTION OF LOAD CAPACITANCE

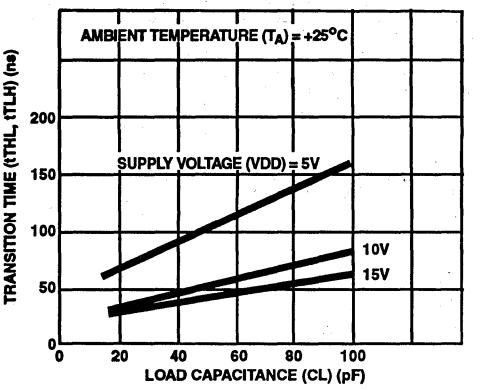


FIGURE 3. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

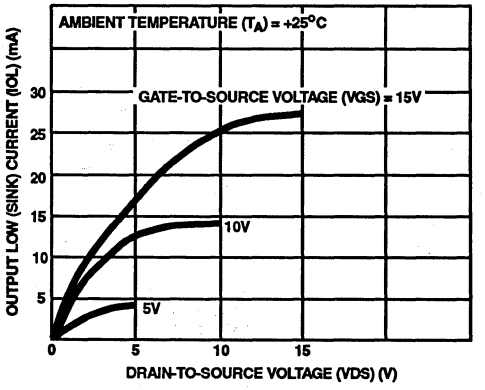


FIGURE 4. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

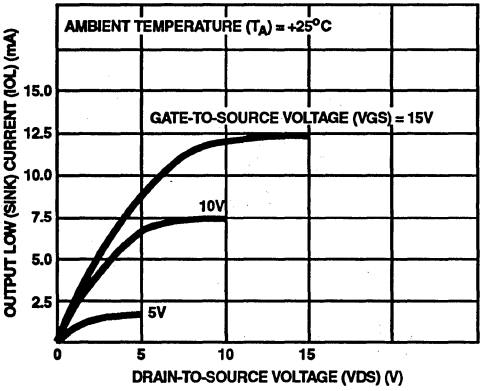


FIGURE 5. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

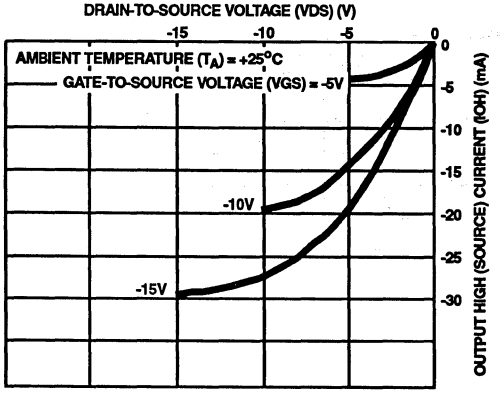


FIGURE 6. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

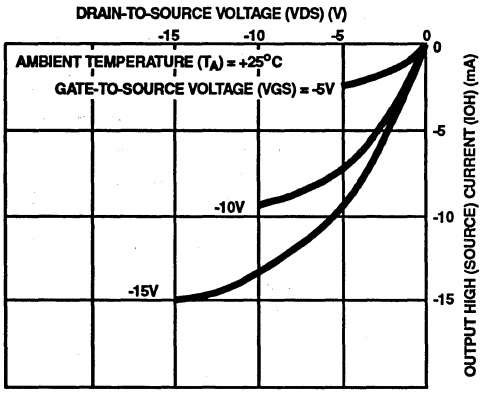


FIGURE 7. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Electrical Performance Characteristics (Continued)

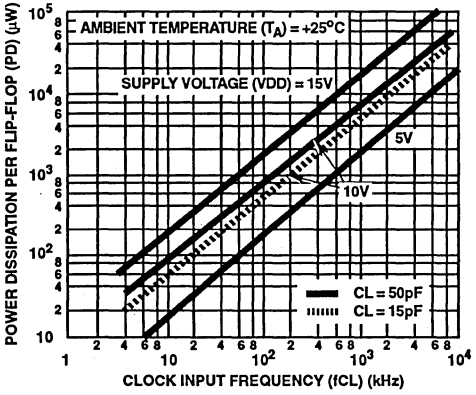
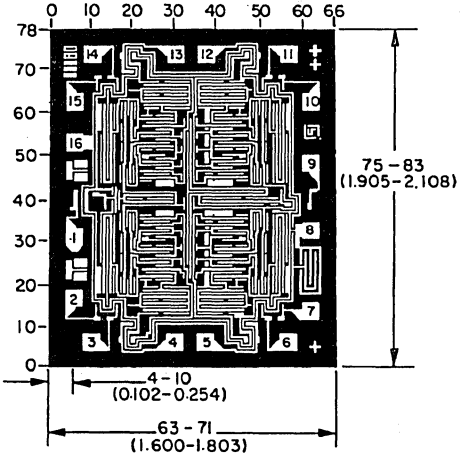


FIGURE 8. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF CLOCK FREQUENCY

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD40181BMS

CMOS 4 Bit Arithmetic Logic Unit

December 1992

Features

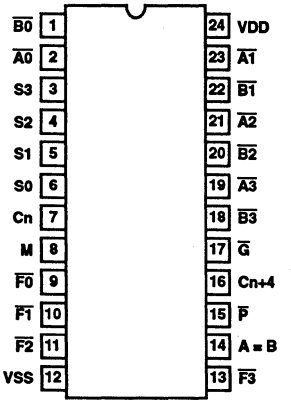
- High Voltage Type (20V Rating)
- Full Look Ahead Carry for Speed Operations on Long Words
- Generates 16 Logic Functions of Two Boolean Variables
- Generates 16 Arithmetic Functions of Two 4 Bit Binary Words
- A = B comparator Output Available
- Ripple Carry Input and Output Available
- Typical Addition Time 200ns at VDD = 10V
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Standardized Symmetrical Output Characteristics
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Parallel Arithmetic Units
- Process Controllers
- Low Power Minicomputers

Pinout

CD40181BMS ACTIVE-LOW DATA
TOP VIEW



Description

The CD40181BMS is a low power four bit parallel arithmetic logic unit (ALU) capable of providing 16 binary arithmetic operations on two four-bit words and 16 logical functions of two Boolean variables. The mode control input M selects logical (M = High) or arithmetic (M = Low) operation. The four select inputs (S0, S1, S2, and S3) select the desired logical or arithmetic functions, which include AND, OR, NAND, NOR and exclusive-OR and-NOR in the logic mode, and addition, subtraction, decrement, left-shift and straight transfer in the arithmetic mode, according to the truth table. The CD40181BMS operation may be interpreted with either active-low or active-high data at the A and B word inputs and the function outputs F, by using the appropriate truth table.

The CD40181BMS contains logic for full look ahead carry operation for fast carry generation using the carry-generate and carry-propagate outputs $\overline{G}$ and $\overline{P}$ for the four bits of the CD40181BMS. Use of the CD40182BMS look-ahead carry generator in conjunction with multiple CD40181BMS's permits high speed arithmetic operations on long words. A ripple carry output Cn+4 is available for use in systems where speed is not of primary importance.

Also included in the CD40181BMS is a comparator output A = B, which assumes a high level whenever the two four-bit input words A and B are equal and the device is in the subtract mode. In addition, relative magnitude information may be derived from the carry-in input Cn and ripple carry-out output Cn+4 by placing the unit in the subtract mode and externally decoding using the information in Table B.

The CD40181BMS is similar to industry types MC14581 and 74181.

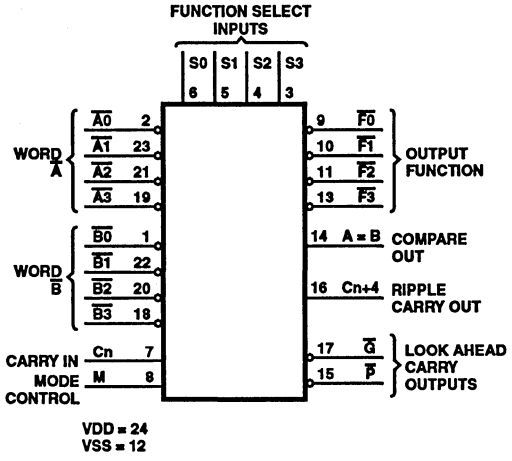
The CD40181BMS is supplied in these 24-lead outline packages:

Braze Seal DIP	HNZ
Ceramic Flatpack	H4P

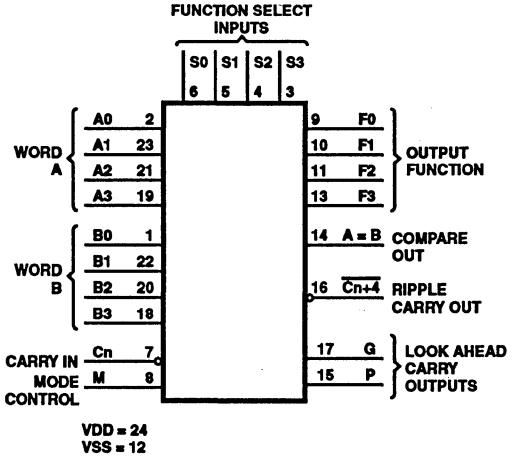
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3361**

Functional Diagrams



ACTIVE-LOW DATA



ACTIVE-HIGH DATA

7 LOGIC

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay A or B to F (Logic Mode), A or B to G or P	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	800	ns
			10, 11	+125°C, -55°C	-	1080	ns
Propagation Delay A or B to F, Cn+4, or A = B	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	1000	ns
			10, 11	+125°C, -55°C	-	1350	ns
Propagation Delay Cn to F	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	640	ns
			10, 11	+125°C, -55°C	-	864	ns
Propagation Delay Cn to Cn+4	TPHL4 TPLH4	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay A or B to F (Logic Mode) A or B to G or P	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	320	ns
		VDD = 15V	1, 2, 3	+25°C	-	240	ns
Propagation Delay A or B to F, Cn+4 or A = B	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	400	ns
		VDD = 15V	1, 2, 3	+25°C	-	280	ns
Propagation Delay Cn to F	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25°C	-	270	ns
		VDD = 15V	1, 2, 3	+25°C	-	200	ns
Propagation Delay Cn to Cn+4	TPHL4 TPLH4	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	140	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTND	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTPD	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	9-11, 13-17	1-8, 12, 18-23	24			
Static Burn-In 2 (Note 1)	9-11, 13-17	12	1-8, 18-24			
Dynamic Burn-In (Note 1)	-	4-6, 8, 12	3, 24	9-11, 13-17	1, 2, 18-23	7
Irradiation (Note 2)	9-11, 13-17	12	1-8, 18-24			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram

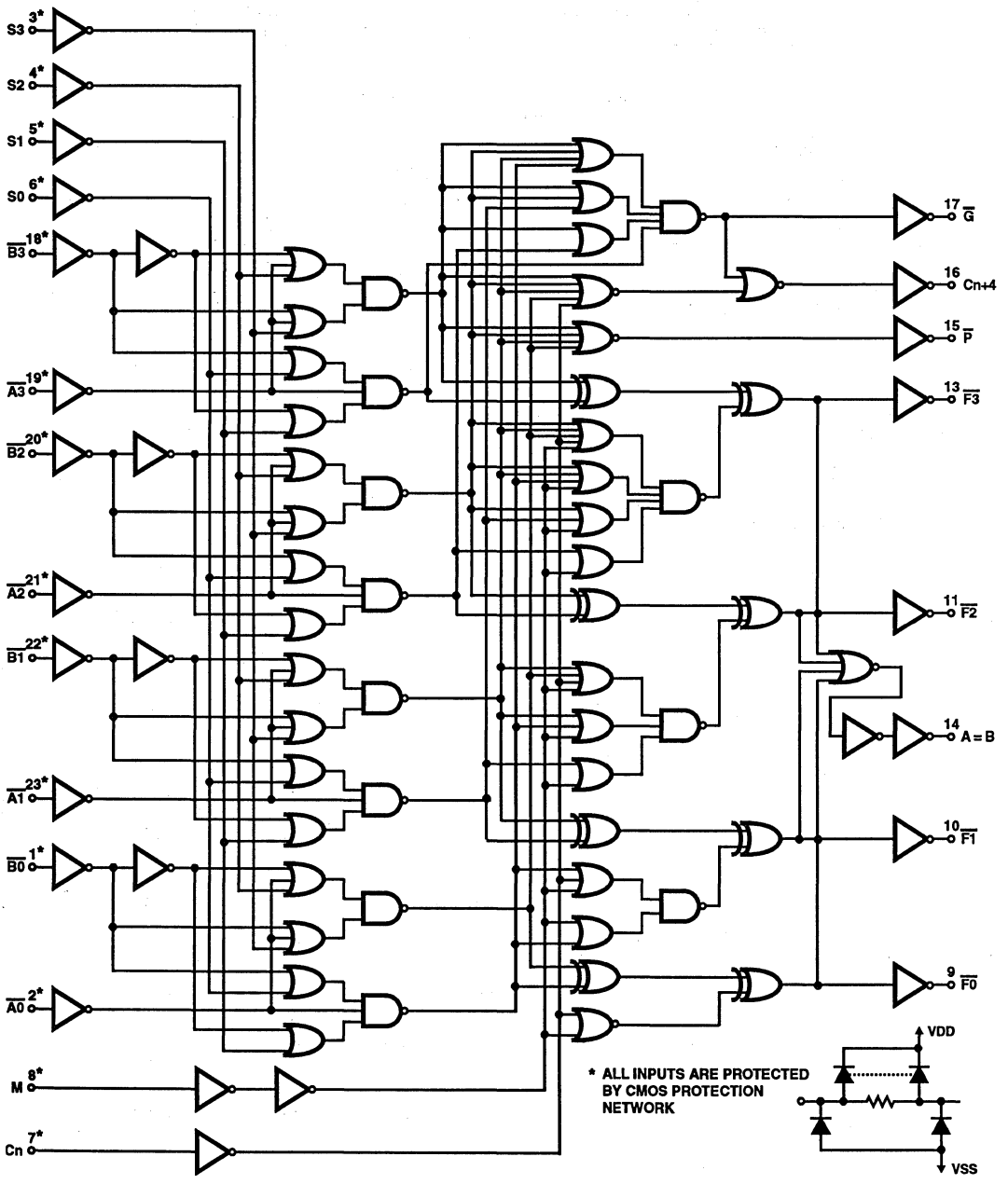


FIGURE 1. ACTIVE LOW DATA

TRUTH TABLE

FUNCTION SELECT				INPUTS/OUTPUTS ACTIVE LOW			FUNCTION SELECT				INPUTS/OUTPUTS ACTIVE HIGH		
				LOGIC FUNCTION	ARITHMETIC* FUNCTION M = L						LOGIC FUNCTION	ARITHMETIC* FUNCTION M = L	
S3	S2	S1	S0	M = H	Cn = L	Cn = H	S3	S2	S1	S0	M = H	Cn = H	Cn = L
0	0	0	0	$\overline{A}$	A minus 1	A	0	0	0	0	$\overline{A}$	A	A plus 1
0	0	0	1	$\overline{AB}$	AB minus 1	AB	0	0	0	1	$\overline{A+B}$	A + B	(A + B) plus 1
0	0	1	0	$\overline{A}+B$	$\overline{AB}$ minus 1	$A\overline{B}$	0	0	1	0	$A\overline{B}$	$A+\overline{B}$	$(A+\overline{B})$ plus 1
0	0	1	1	Logic 1	minus 1	Zero	0	0	1	1	Logic 0	minus 1	Zero
0	1	0	0	$\overline{A+B}$	A plus $(A+\overline{B})$	A plus $(A+\overline{B})$ plus 1	0	1	0	0	$\overline{AB}$	A plus $A\overline{B}$	A plus $A\overline{B}$ plus 1
0	1	0	1	$\overline{B}$	AB plus $(A+\overline{B})$	AB plus $(A+\overline{B})$ plus 1	0	1	0	1	$\overline{B}$	(A + B) plus $A\overline{B}$	(A + B) plus $A\overline{B}$ plus 1
0	1	1	0	$\overline{A \oplus B}$	A minus B minus 1	A minus B	0	1	1	0	$A \oplus B$	A minus B minus 1	A minus B
0	1	1	1	$A+\overline{B}$	$A+\overline{B}$	$(A+\overline{B})$ plus 1	0	1	1	1	$A\overline{B}$	$A\overline{B}$ minus 1	$A\overline{B}$
1	0	0	0	$\overline{AB}$	A plus (A + B)	A plus (A + B) plus 1	1	0	0	0	$\overline{A+B}$	A plus AB	A plus AB plus 1
1	0	0	1	$A \oplus B$	A plus B	A plus B plus 1	1	0	0	1	$\overline{A \oplus B}$	A plus B	A plus B plus 1
1	0	1	0	B	$A\overline{B}$ plus (A + B)	$A\overline{B}$ plus (A + B) plus 1	1	0	1	0	B	$(A+\overline{B})$ plus AB	$(A+\overline{B})$ plus AB plus 1
1	0	1	1	A + B	A + B	A + B plus 1	1	0	1	1	AB	AB minus 1	AB
1	1	0	0	Logic 0	A plus A	A plus A plus 1	1	1	0	0	Logic 1	A plus A	A plus A plus 1
1	1	0	1	$A\overline{B}$	AB plus A	AB plus A plus 1	1	1	0	1	$A+\overline{B}$	$(A+\overline{B})$ plus A	$(A+\overline{B})$ plus A plus 1
1	1	1	0	AB	$A\overline{B}$ plus A	$A\overline{B}$ plus A plus 1	1	1	1	0	A + B	$(A+\overline{B})$ plus A	$(A+\overline{B})$ plus A plus 1
1	1	1	1	A	A	A plus 1	1	1	1	1	A	A minus 1	A

* Expressed as two's complement

1 = High level

0 = Low level

Typical Performance Characteristics

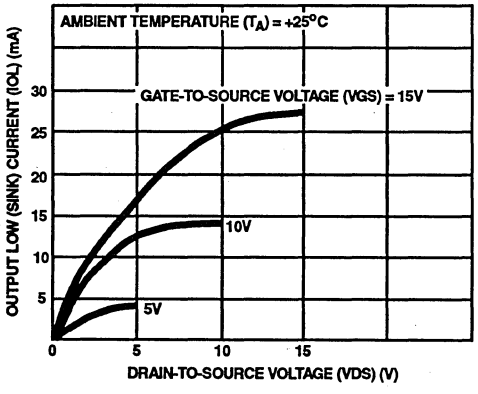


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

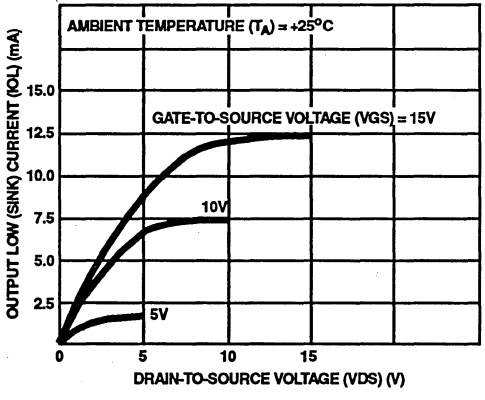


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

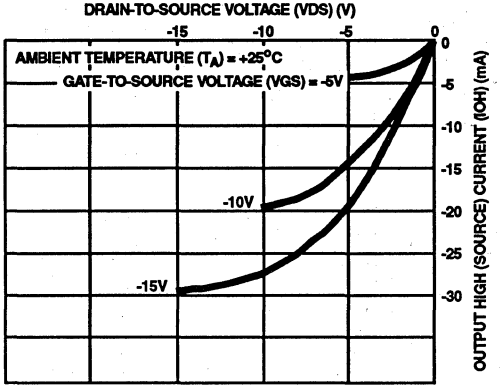


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

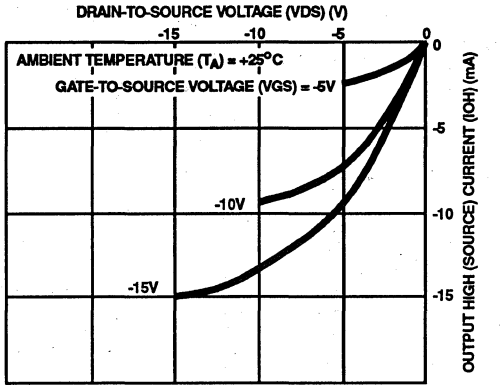


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

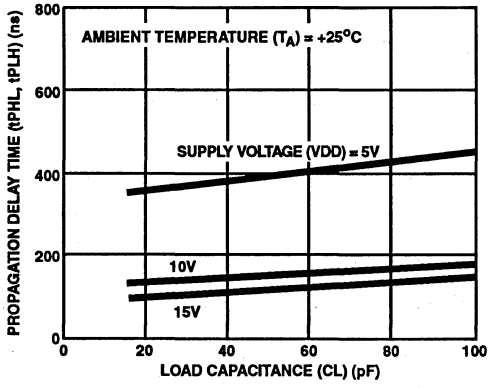


FIGURE 6. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (FOR A OR B TO F, LOGIC MODE

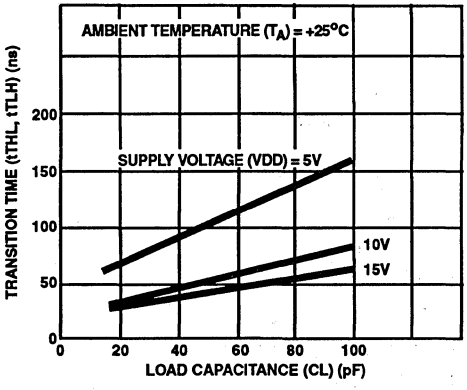


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

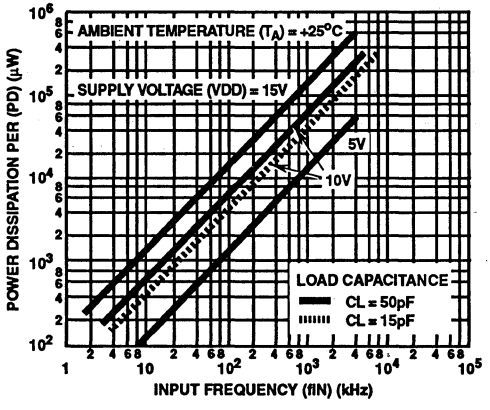


FIGURE 8. TYPICAL DYNAMIC DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

TABLE A. AC TEST SETUP REFERENCE (ACTIVE LOW DATA)

TEST DELAY TIMES	AC PATHS		DC DATA INPUTS		MODE*
	INPUTS	OUTPUTS	TO VSS	TO VDD	
SUMIN to SUMOUT	$\overline{B0}$	Any $\overline{F}$	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$, M, Cn	All $\overline{A}$'s	Add
SUMIN to $\overline{P}$	$\overline{A0}$	$\overline{P}$	$\overline{A1}$, $\overline{A2}$, $\overline{A3}$, M, Cn	All $\overline{B}$'s	Add
SUMIN to $\overline{G}$	$\overline{B0}$	$\overline{G}$	All $\overline{A}$'s, M, Cn	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$	Add
SUMIN to Cn+4	$\overline{B0}$	Cn+4	All $\overline{A}$'s, M, Cn	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$	Add
Cn to SUMOUT	Cn	Any $\overline{F}$	All $\overline{A}$'s, M	All $\overline{B}$'s	Add
Cn to Cn+4	Cn	Cn+4	All $\overline{A}$'s, M	All $\overline{B}$'s	Add
SUMIN to A = B	$\overline{B0}$	A = B	All A's, B1, B2, B3, M	Cn	Subtract
SUMIN to SUMOUT (Logic Mode)	All $\overline{B}$'s	Any $\overline{F}$	All $\overline{A}$'s, Cn	M	Exclusive OR

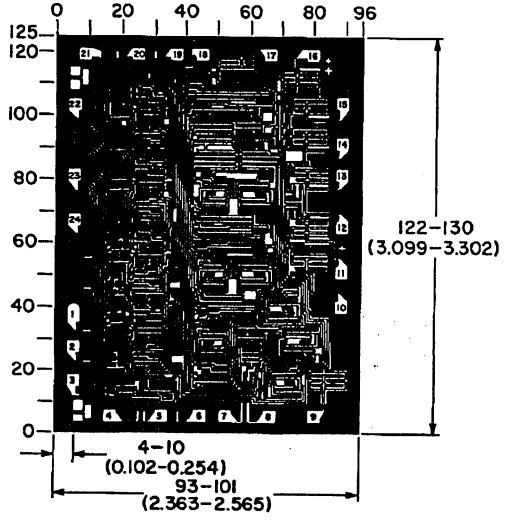
* Add Mode: S0, S3 = VDD; S1, S2 = VSS.
Subtract Mode: S0, S3 = VSS; S1, S2 = VDD.

TABLE B. MAGNITUDE COMPARISON

ACTIVE HIGH DATA			ACTIVE LOW DATA		
INPUT Cn	OUTPUT Cn+4	MAGNITUDE	INPUT Cn	OUTPUT Cn+4	MAGNITUDE
1	1	A ≤ B	0	0	A ≤ B
0	1	A < B	1	0	A < B
1	0	A > B	0	1	A > B
0	0	A ≥ B	1	1	A ≥ B

1 = High level 0 = Low level

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD40182BMS

December 1992

CMOS Look-Ahead Carry Generator

Features

- High Voltage Type (20V Rating)
- Generates High-Speed Carry Across Four Adders or Adder Groups
- High-Speed Operation
  - tPHL, tPLH =100 ns (typ) at VDD = 10V
- Cascadable for Fast Carries Over N Bits
- Designed for Use with CD40181BMS ALU
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Standardized Symmetrical Output Characteristics
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- High-Speed Parallel Arithmetic Units
- Multi-Level Look-Ahead Carry Generation for Long Word Lengths

Description

The CD40182BMS is a high-speed look-ahead carry generator capable of anticipating a carry across four binary adders or groups of adders. The CD40182BMS is cascadable to perform full look-ahead across n-bit adders. Carry, propagate-carry, and generate-carry functions are provided as enumerated in the terminal designation below.

The CD40182BMS, when used in conjuction with the CD40181BMS arithmetic logic unit (ALU), provides full high-speed look-ahead carry capability for up to n-bit words. Each CD40182BMS generates the look-ahead (anticipated carry) across a group of four ALU's. In addition, other CD40182BMS's may be employed to anticipate the carry across sections of four look-ahead blocks up to n-bits. Carry inputs and outputs of the CD40181BMS are active-high logic, and carry-generate (G) and carry-propagate (P) outputs are active-low. Therefore the inputs and outputs of the CD40182BMS are compatible.

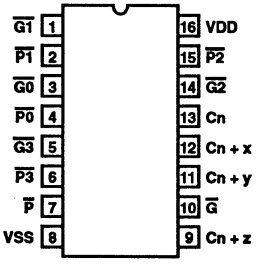
The CD40182BMS is supplied in these 16-lead outline packages:

Braze Seal DIP	H4V
Frit Seal DIP	H1E
Ceramic Flatpack	H6P

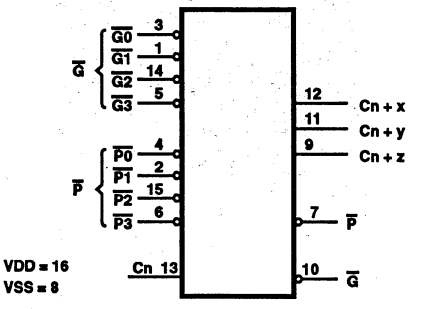
The CD40182BMS is similar to industry type MC14582.

Pinout

CD40182BMS
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3362

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) ..... Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20V	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20V	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTES 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay P, G In to P, G Out and Carry Outs	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay Cn to Carry Outs	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	480	ns
			10, 11	+125°C, -55°C	-	648	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay P, G In to P, G Out and Carry Outs	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	150	ns
Propagation Delay Cn to Carry Outs	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	240	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K., Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	7, 9 - 12	1 - 6, 8, 13 - 15	16			
Static Burn-In 2 (Note 1)	7, 9 - 12	8	1 - 6, 13 - 16			
Dynamic Burn-In (Note 1)	-	8	16	7, 9 - 12	1 - 6, 14, 15	13
Irradiation (Note 2)	7, 9 - 12	8	1 - 6, 13 - 16			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

TABLE 9. TERMINAL DESIGNATIONS

DESIGNATION	TERM.	FUNCTION
$\overline{G0}$, $\overline{G1}$, $\overline{G2}$, $\overline{G3}$	3, 1, 14, 5	Active-Low Carry-Generate Inputs
$\overline{P0}$, $\overline{P1}$, $\overline{P2}$, $\overline{P3}$	4, 2, 15, 6	Active-Low Carry-Propagate Inputs
Cn	13	Active-High Carry Input
Cn + x, Cn + y, Cn + z	12, 11, 9	Active-High Carry Outputs

TABLE 9. TERMINAL DESIGNATIONS (Continued)

DESIGNATION	TERM.	FUNCTION
$\overline{G}$	10	Active-Low Group Carry-Generate Output
$\overline{P}$	7	Active-Low Group Carry-Propagate Output

Logic Diagram

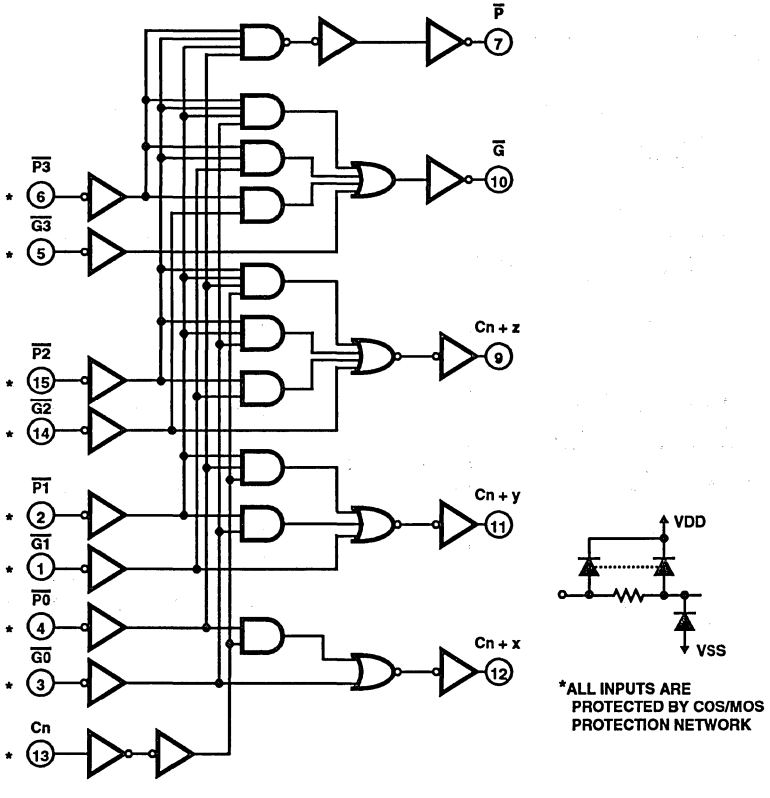


FIGURE 1. CD40182BMS LOGIC DIAGRAM

CD40182BMS LOGIC EQUATIONS

$$Cn+x = G0 + P0 \cdot Cn$$

$$Cn+y = G1 + P1 \cdot G0 + P1 \cdot P0 \cdot Cn$$

$$Cn+z = G2 + P2 \cdot G1 + P2 \cdot P1 \cdot G0 + P2 \cdot P1 \cdot P0 \cdot Cn$$

$$\overline{G} = \overline{G3 + P3 \cdot G2 + P3 \cdot P2 \cdot G1 + P3 \cdot P2 \cdot P1 \cdot G0}$$

$$\overline{P} = \overline{P3 \cdot P2 \cdot P1 \cdot P0}$$

Typical Performance Characteristics

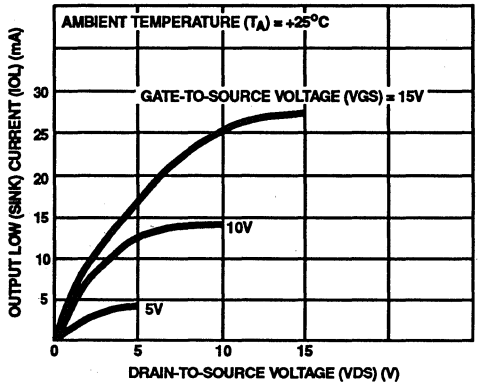


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

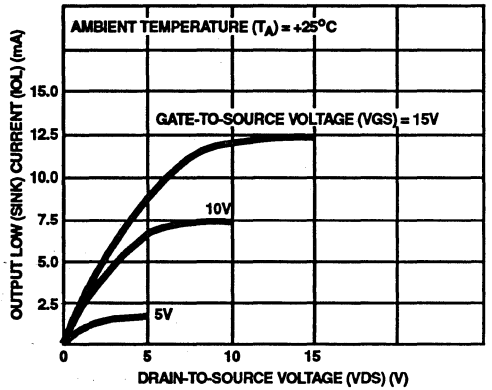


FIGURE 3. MIMIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

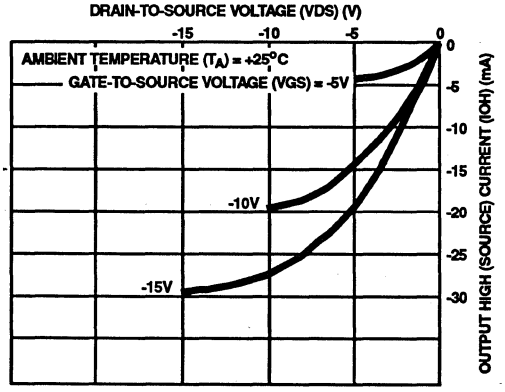


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

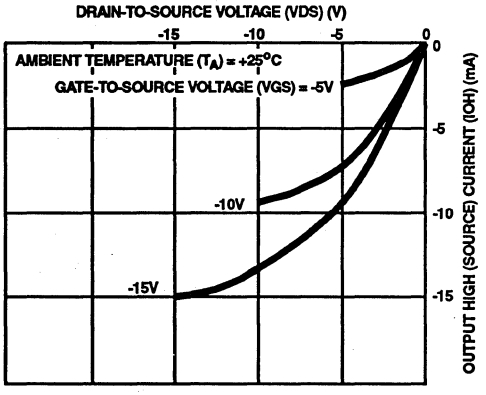


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

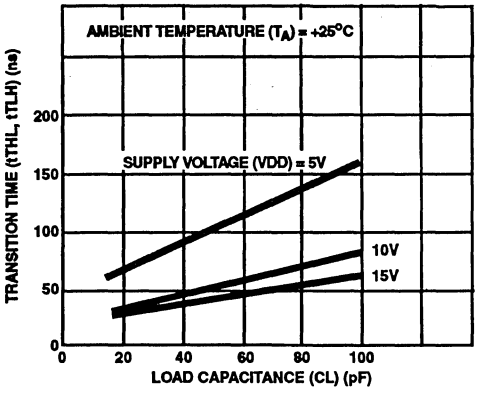


FIGURE 6. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

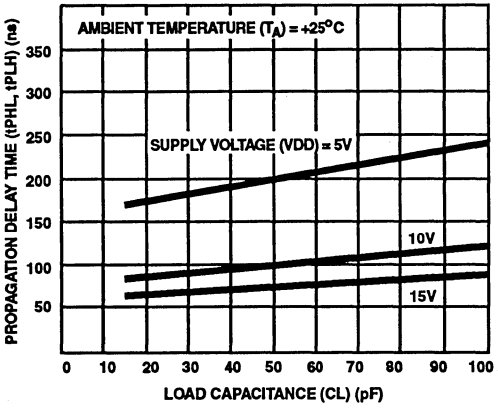


FIGURE 7. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (P, G IN TO P, G OUT AND CARRY-OUTS)

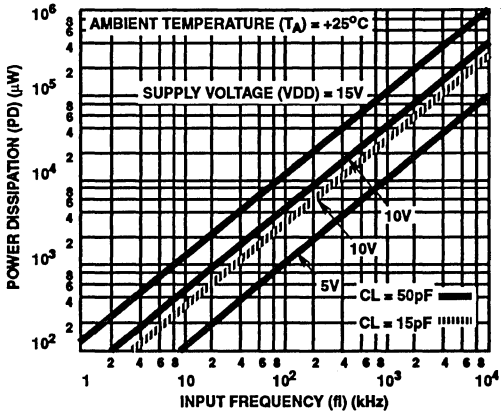


FIGURE 8. TYPICAL POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

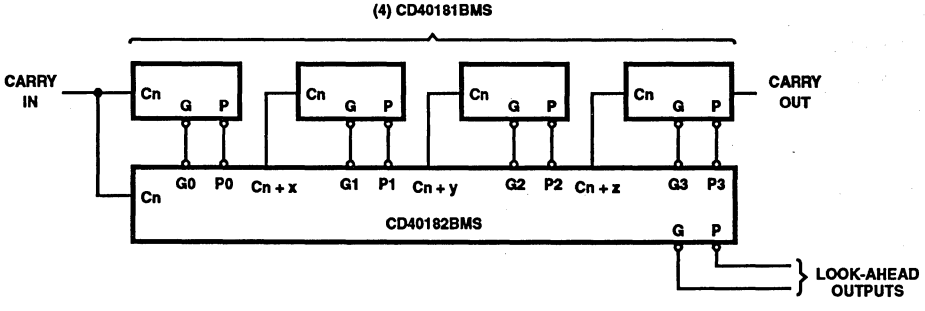


FIGURE 9. 16-BIT TWO-LEVEL LOOK-AHEAD ALU

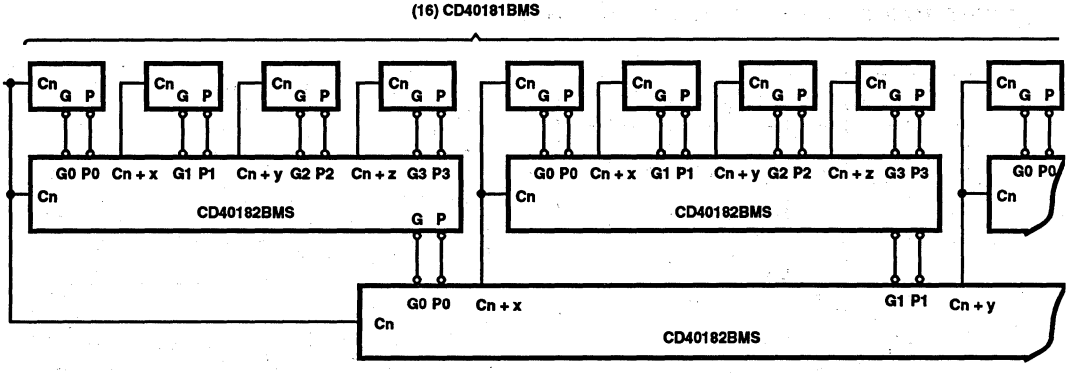


FIGURE 10. 64-BIT FULL CARRY LOOK-AHEAD ALU IN 3 LEVELS

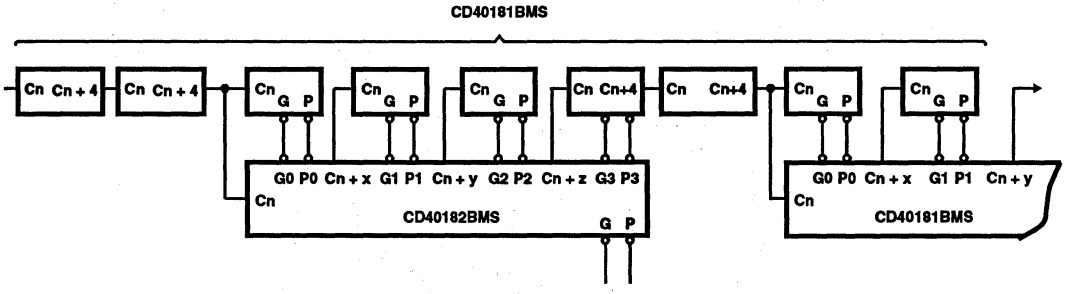
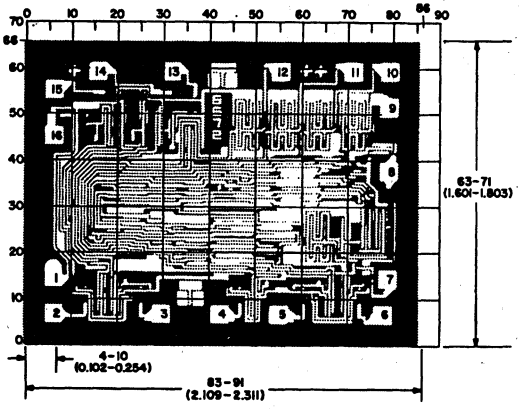


FIGURE 11. COMBINED TWO-LEVEL LOOK-AHEAD AND RIPPLE-CARRY ALU

Chip Dimensions and Pad Layout



METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to +16 mils applicable to the nominal dimensions shown.

Dimension in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

HARRIS SEMICONDUCTOR

CD40192BMS
CD40193BMS

CMOS Presettable Up/Down Counters (Dual Clock With Reset)

December 1992

Features

- CD40192BMS - BCD Type
- CD40193BMS - Binary Type
- High Voltage Type (20V Rating)
- Individual Clock Lines for Counting Up or Counting Down
- Synchronous High-Speed Carry and Borrow Propagation Delays for Cascading
- Asynchronous Reset and Preset Capability
- Medium Speed Operation
  - fCL = 8MHz (typ.) at 10V
- 5V, 10V and 15V Parametric Ratings
- Standardize Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Up/Down Difference Counting
- Multistage Ripple Counting
- Synchronous Frequency Dividers
- A/D and D/A Conversion
- Programmable Binary or BCD Counting

Description

CD40192BMS Presettable BCD Up/Down Counter and the CD40193BMS Presettable Binary Up/Down Counter each consist of 4 synchronously clocked, gated "D" type flip-flops connected as a counter. The inputs consist of 4 individual jam lines, a $\overline{\text{PRESET ENABLE}}$ control, individual CLOCK UP and CLOCK DOWN signals and a master RESET. Four buffered Q signal outputs as well as $\overline{\text{CARRY}}$ and $\overline{\text{BORROW}}$ outputs for multiple-stage counting schemes are provided.

The counter is cleared so that all outputs are in a low state by a high on the RESET line. A RESET is accomplished asynchronously with the clock. Each output is individually programmable asynchronously with the clock to the level on the corresponding jam input when the $\overline{\text{PRESET ENABLE}}$ control is low.

The counter counts up one count on the positive clock edge of the CLOCK UP signal provided the CLOCK DOWN line is high. The counter counts down one count on the positive clock edge of the CLOCK DOWN signal provided the CLOCK UP line is high.

The $\overline{\text{CARRY}}$ and $\overline{\text{BORROW}}$ signals are high when the counter is counting up or down. The $\overline{\text{CARRY}}$ signal goes low one-half clock cycle after the counter reaches its maximum count in the count-up mode. The $\overline{\text{BORROW}}$ signal goes low one-half clock cycle after the counter reaches its minimum count in the count-down mode. Cascading of multiple packages is easily accomplished without the need for additional external circuitry by tying the $\overline{\text{BORROW}}$ and $\overline{\text{CARRY}}$ outputs to the CLOCK DOWN and CLOCK UP inputs, respectively, of the succeeding counter package.

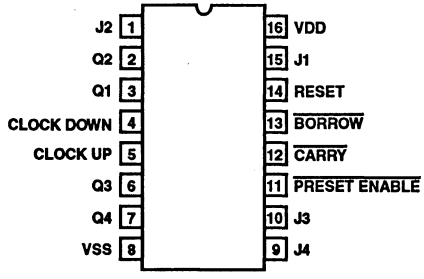
The CD40192BMS and CD40193BMS are supplied in these 16-lead outline packages:

Braze Seal DIP	*H4W,	†H4X
Frit Seal DIP	H1F	
Ceramic Flatpack	*H6P,	†H6W

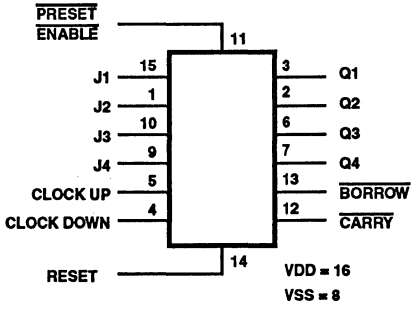
* CD40192B Only †CD40193B Only

Pinout

CD40192BMS, CD40193BMS
TOP VIEW



Functional Diagram



7 LOGIC

File Number 3363

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20V	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20V	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTES 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock Up or Clock Down to Q	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Propagation Delay Reset to Q	TPHL2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Propagation Delay $\overline{PE}$ to Q	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay Clock Up to $\overline{Carry}$, Clock Down to $\overline{Borrow}$	TPHL4 TPLH4	VDD = 5V, VIN = VDD or GND	9	+25°C	-	320	ns
			10, 11	+125°C, -55°C	-	432	ns
Propagation Delay $\overline{PE}$ to $\overline{Borrow}$ or $\overline{Carry}$	TPHL5 TPLH5	VDD = 5V, VIN = VDD or GND	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Propagation Delay Reset to $\overline{Borrow}$ or $\overline{Carry}$	TPHL6 TPLH6	VDD = 5V, VIN = VDD or GND	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	2	-	MHz
			10, 11	+125°C, -55°C	1.48	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Clock Up or Down to Q	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	240	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns
Propagation Delay Reset to Q	TPHL2	VDD = 10V	1, 2, 3	+25°C	-	240	ns
		VDD = 15V	1, 2, 3	+25°C	-	180	ns
Propagation Delay $\overline{PE}$ to Q	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	140	ns
Propagation Delay Clock Up to $\overline{Carry}$, Clock Down to $\overline{Borrow}$	TPHL4 TPLH4	VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Propagation Delay $\overline{PE}$ to $\overline{Borrow}$ or $\overline{Carry}$	TPHL5 TPLH5	VDD = 10V	1, 2, 3	+25°C	-	300	ns
		VDD = 15V	1, 2, 3	+25°C	-	220	ns
Propagation Delay Reset to $\overline{Borrow}$ or $\overline{Carry}$	TPHL6 TPLH6	VDD = 10V	1, 2, 3	+25°C	-	300	ns
		VDD = 15V	1, 2, 3	+25°C	-	220	ns
Transition Time	TTHL1 TTLH1	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Rise and Fall Time	TRCL TFCL	VDD = 5V	1, 2, 3, 4	+25°C	-	15	µs
		VDD = 10V	1, 2, 3, 4	+25°C	-	15	µs
		VDD = 15V	1, 2, 3, 4	+25°C	-	5	µs
Minimum Removal Time Reset or $\overline{PE}$	TREM	VDD = 5V	1, 2, 3, 5	+25°C	-	80	ns
		VDD = 10V	1, 2, 3, 5	+25°C	-	40	ns
		VDD = 15V	1, 2, 3, 5	+25°C	-	30	ns
Minimum Pulse Width Reset	TW	VDD = 5V	1, 2, 3	+25°C	-	480	ns
		VDD = 10V	1, 2, 3	+25°C	-	300	ns
		VDD = 15V	1, 2, 3	+25°C	-	260	ns
Minimum Pulse Width $\overline{PE}$	TW	VDD = 5V	1, 2, 3	+25°C	-	240	ns
		VDD = 10V	1, 2, 3	+25°C	-	170	ns
		VDD = 15V	1, 2, 3	+25°C	-	140	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	180	ns
		VDD = 10V	1, 2, 3	+25°C	-	90	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Input Capacitance	CIN	Reset	1, 2	+25°C	-	15	pF
Input Capacitance	CIN	All Other Inputs	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. If more than one unit is cascaded, TRCL should be made less than or equal to the sumof the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.
5. The time required for RESET or PRESET ENABLE control to be removed before clocking. See timing diagram defining TREM.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
PART NUMBER	CD40192BMS, CD40193BMS					
Static Burn-In 1 (Note 1)	2, 3, 6, 7, 12, 13	1, 4, 5, 8 - 11, 14, 15	16			
Static Burn-In 2 (Note 1)	2, 3, 6, 7, 12, 13	8	1, 4, 5, 9 - 11, 14 - 16			
Dynamic Burn-In (Note 1)	-	8, 14	1, 5, 9 - 11, 15, 16	2, 3, 6, 7, 12, 13	4	-
Irradiation (Note 2)	2, 3, 6, 7, 12, 13	8	1, 4, 5, 9 - 11, 14 - 16			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagrams

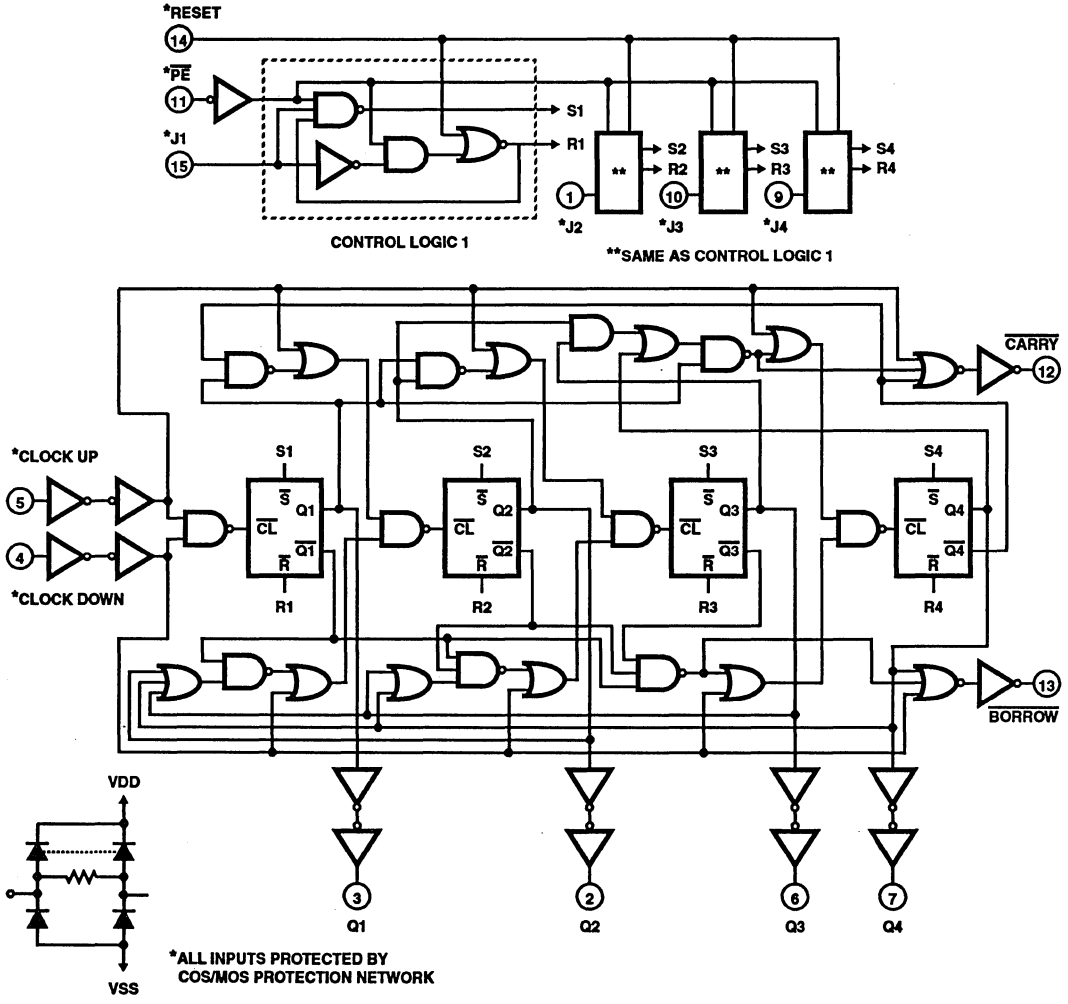


FIGURE 1. CD40192BMS LOGIC DIAGRAM (BCD)

Logic Diagrams (Continued)

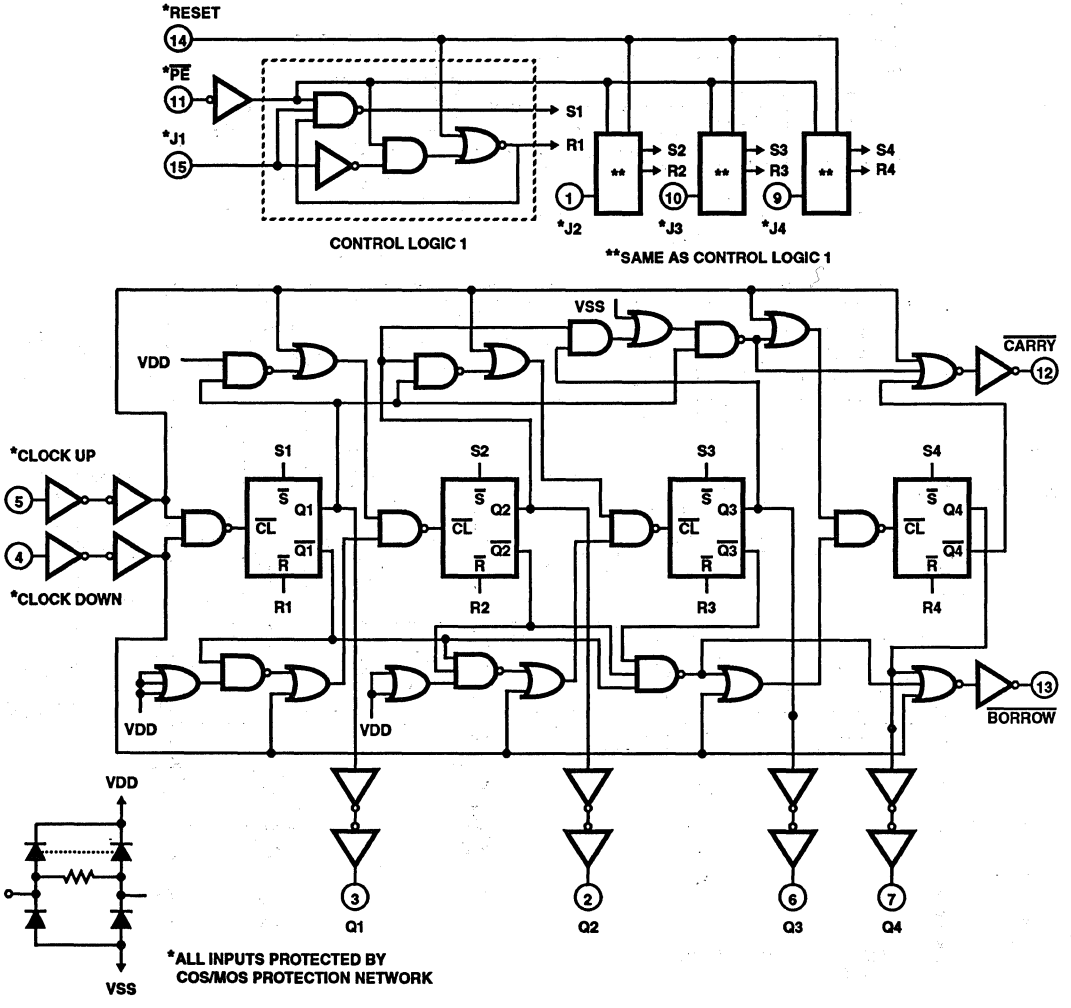


FIGURE 2. CD40193BMS LOGIC DIAGRAM (BINARY)

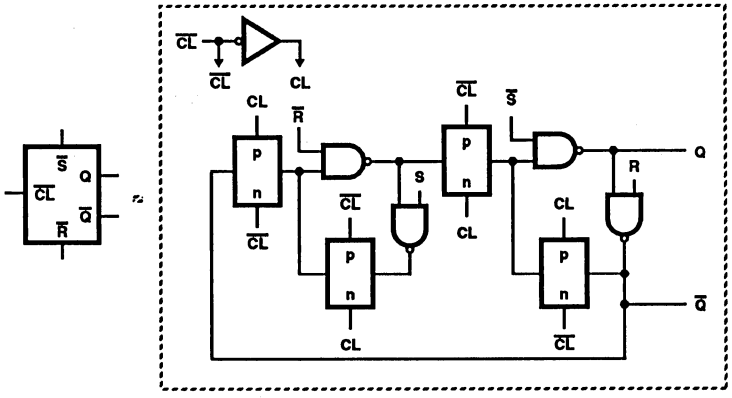


FIGURE 3. INTERNAL LOGIC OF FLIP-FLOP

TRUTH TABLE

CLOCK UP	CLOCK DOWN	$\overline{\text{PRESET ENABLE}}$	RESET	ACTION
↑	1	1	0	Count Up
↓	1	1	0	No Count
1	↑	1	0	Count Down
1	↓	1	0	No Count
X	X	0	0	Preset
X	X	X	1	Reset

1 = High Level 0 = Low Level X = Don't Care

Typical Performance Characteristics

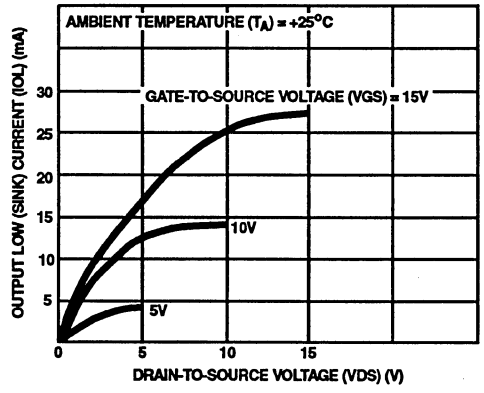


FIGURE 4. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

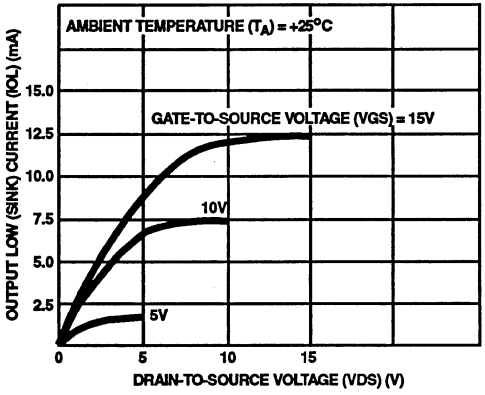


FIGURE 5. MIMIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

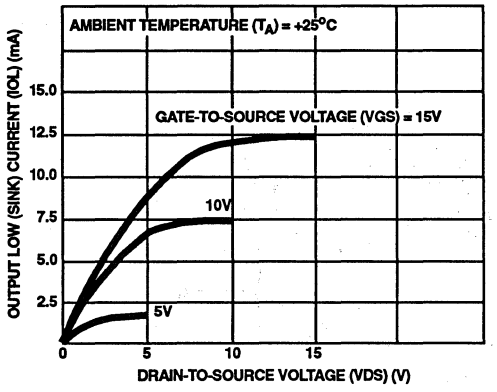


FIGURE 6. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

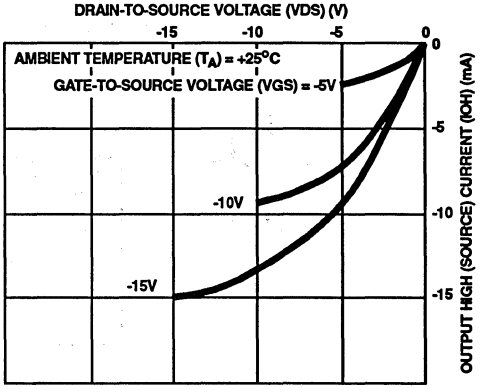


FIGURE 7. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

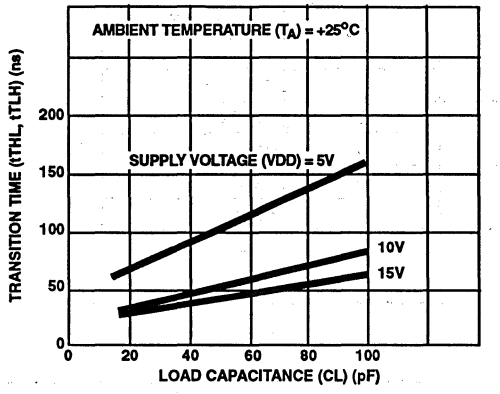


FIGURE 8. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

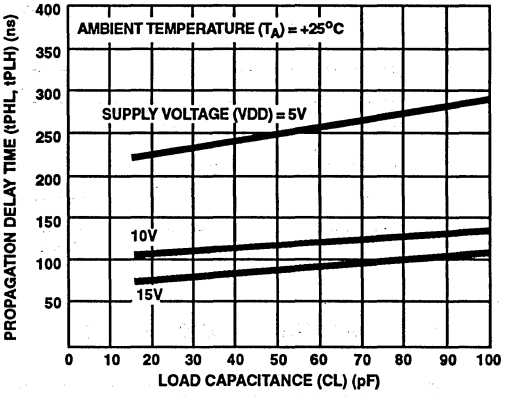


FIGURE 9. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

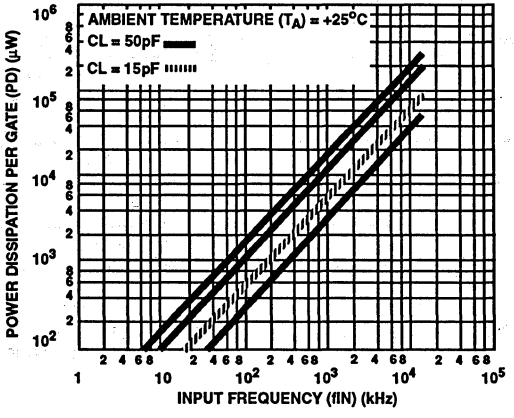


FIGURE 10. DYNAMIC POWER DISSIPATION

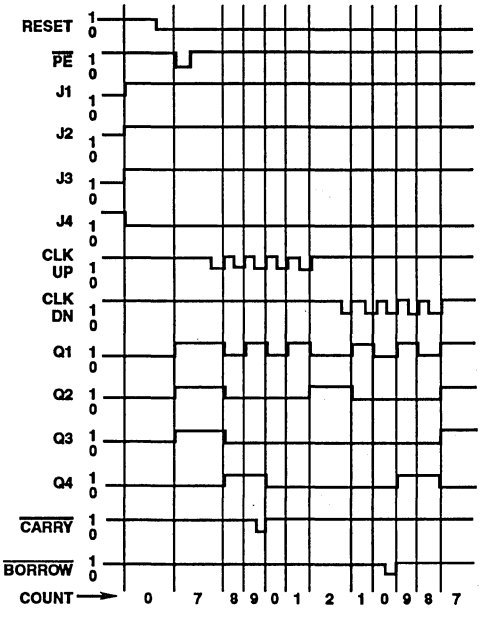


FIGURE 11. CD40192BMS TIMING DIAGRAM

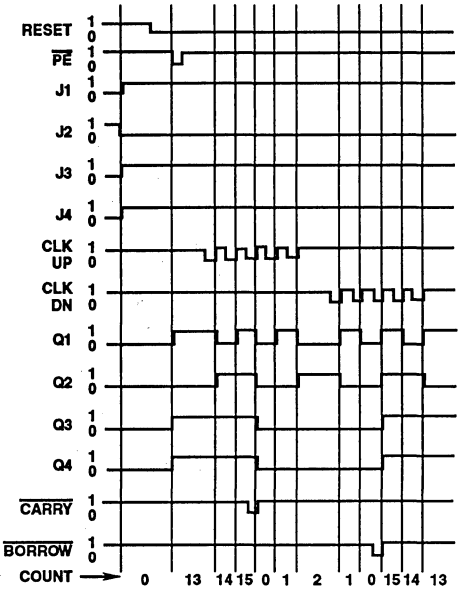


FIGURE 12. CD40193BMS TIMING DIAGRAM

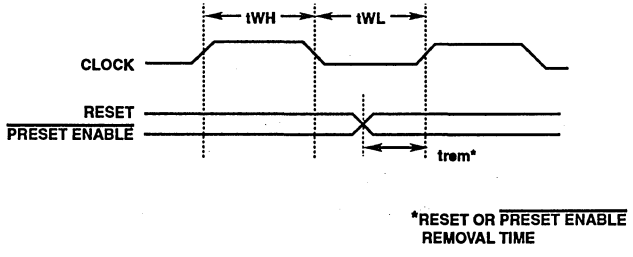


FIGURE 13. TIMING DIAGRAM DEFINING trem

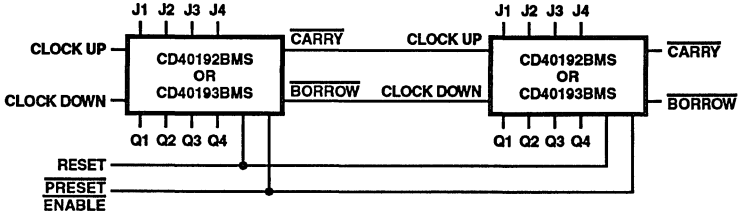
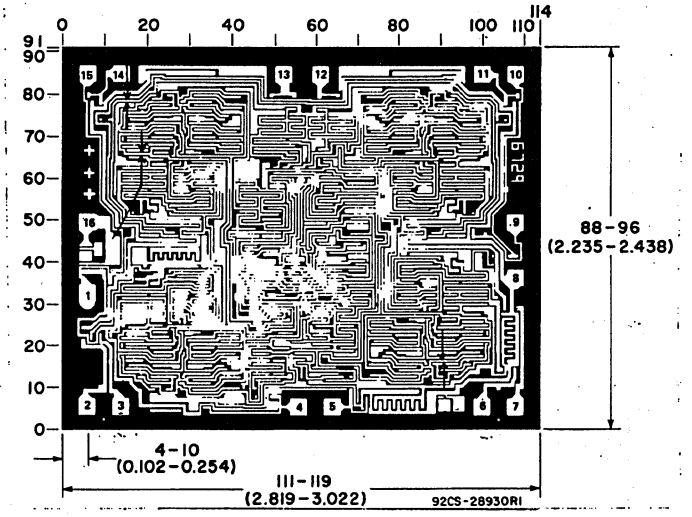


FIGURE 14. CASCADED COUNTER PACKAGES

Chip Dimensions and Pad Layout



Dimensions and pad layout for the CD40192BMSH (dimensions and pad layout for the CD40193BMSH are identical).

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD40208BMS

CMOS 4 x 4 Multiport Register

December 1992

Features

- High Voltage Types (20V Rating)
- One Input and Two Output Buses
- Unlimited Expansion in Bit and Word Directions
- Data Lines have Latched Inputs
- 3-State Outputs
- Separate Control of Each Bus, Allowing Simultaneous Independent Reading of any of Four Registers on Bus A and Bus B and Independent Writing into any of the Four Registers
- 100% Tested for Quiescent Current at 20V
- Standardized, Symmetrical Output Characteristics
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package-Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Full Package-Temperature Range):
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standards No. 13B, "Standard Specifications for Description of "B" Series CMOS Devices"

Applications

- Scratch Pad Memories
- Arithmetic Units
- Data Storage

Description

The CD40208BMS is a 4 x 4 multiport register containing four 4-bit registers, write address decoder, two separate read address decoders, and two 3-state output buses.

When the ENABLE input is low, the corresponding output bus is switched, independently of the clock, to a high impedance state. The high impedance third state provides the outputs with the capability of being connected to the bus lines in a bus organized system without the need for interface or pull-up components.

When the WRITE ENABLE input is high, all data input lines are latched on the positive transition of the CLOCK and the data is entered into the word selected by the write address lines. When WRITE ENABLE is low, the CLOCK is inhibited and no new data is entered. In either case, the contents of any word may be accessed via the read address lines independent of the state of the CLOCK input.

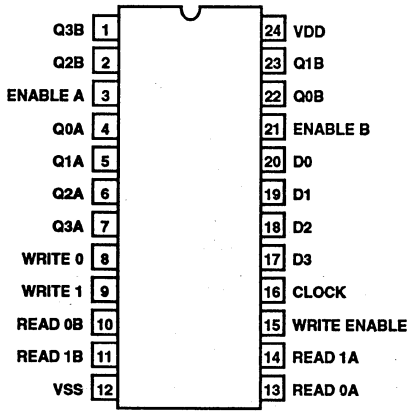
The CD40208BMS types are supplied in hermetic 24-lead dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).

The CD40208BMS is supplied in these 24-lead outline packages:

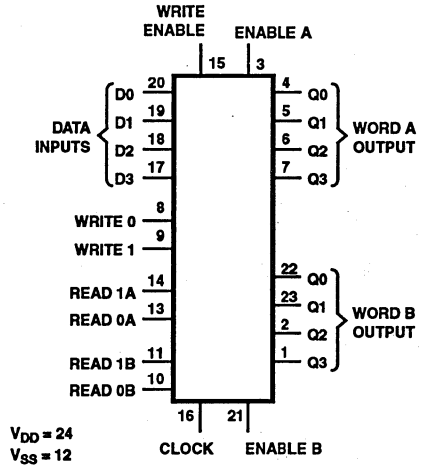
Braze Seal DIP	HNZ
Ceramic Flatpack	H4P

Pinout

CD40208BMS
TOP VIEW



Functional Diagram



7

LOGIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3396

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and Frit Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.4	-	µA
				2	+125°C	-12	-	µA
			VDD = 18V	3	-55°C	-0.4	-	µA
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.4	µA
				2	+125°C	-	12	µA
			VDD = 18V	3	-55°C	-	0.4	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/NoGo test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock or Write Enable to Q	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND (Notes 1, 2)	9	+25°C	-	720	ns
			10, 11	+125°C, -55°C	-	972	ns
Propagation Delay Read or Write Enable to Q	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND (Notes 1, 2)	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Propagation Delay 3-State Disable Delay Time	TPZH, HZ	VDD = 5V, VIN = VDD or GND (Notes 2, 3)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Propagation Delay 3-State Disable Delay Time	TPZL, LZ	VDD = 5V, VIN = VDD or GND (Notes 2, 3)	9	+25°C	-	260	ns
			10, 11	+125°C, -55°C	-	351	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND (Notes 1, 2)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	1.5	-	MHz
			10, 11	+125°C, -55°C	1.11	-	MHz

NOTES:

1. VDD = 5V, CL = 50pF, RL = 200K
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL4	VDD = 4.5V, VOUT = 0.4V	1, 2	+125°C	-	-	mA
				-55°C	-	-	mA
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Clock or Write Enable to Q	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	280	ns
		VDD = 15V	1, 2, 3	+25°C	-	200	ns
Propagation Delay Read or Write Address to Q	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	240	ns
		VDD = 15V	1, 2, 3	+25°C	-	170	ns
Propagation Delay Output Disable to Output	TPZL, LZ	VDD = 10V	1, 2, 4	+25°C	-	120	ns
		VDD = 15V	1, 2, 4	+25°C	-	100	ns
Propagation Delay Output Disable to Output	TPZH, HZ	VDD = 10V	1, 2, 4	+25°C	-	100	ns
		VDD = 15V	1, 2, 4	+25°C	-	80	ns
Minimum Write Enable to $\overline{\text{Clock}}$ Setup Time	TS (WE)	VDD = 5V	1, 2, 3	+25°C	-	250	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	70	ns
Minimum Data to Clock Setup Time	TS (D)	VDD = 5V	1, 2, 3	+25°C	-	0	ns
		VDD = 10V	1, 2, 3	+25°C	-	0	ns
		VDD = 15V	1, 2, 3	+25°C	-	0	ns
Minimum Write Address to $\overline{\text{Clock}}$ Setup Time	TS (WA)	VDD = 5V	1, 2, 3	+25°C	-	250	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	70	ns
Minimum Write Enable to Clock Hold Time	TH (WE)	VDD = 5V	1, 2, 3	+25°C	-	270	ns
		VDD = 10V	1, 2, 3	+25°C	-	130	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Minimum Data to Clock Hold Time	TH (D)	VDD = 5V	1, 2, 3	+25°C	-	220	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Minimum Write Address to $\overline{\text{Clock}}$ Hold Time	TH (WA)	VDD = 5V	1, 2, 3	+25°C	-	330	ns
		VDD = 10V	1, 2, 3	+25°C	-	140	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns
Minimum Clock Pulse Width, Clock or Write Enable	TW (CL)	VDD = 5V	1, 2, 3	+25°C	-	350	ns
		VDD = 10V	1, 2, 3	+25°C	-	130	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Minimum Clock Pulse Width, Write Address	TW (WA)	VDD = 5V	1, 2, 3	+25°C	-	300	ns
		VDD = 10V	1, 2, 3	+25°C	-	150	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	3.5	-	MHz
		VDD = 15V	1, 2, 3	+25°C	4.5	-	MHz
Clock Rise and Fall Time	tRCL tFCL	VDD = 5V	1, 2, 3	+25°C	-	15	µs
		VDD = 10V	1, 2, 3	+25°C	-	5	µs
		VDD = 15V	1, 2, 3	+25°C	-	5	µs
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K., Input TR, TF < 20ns
4. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS= -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES:

1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input tR, tF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record.

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	1, 2, 4-7, 22, 23	3, 8-21	24			
Static Burn-In 2 (Note 1)	1, 2, 4-7, 22, 23	12	3, 8-11, 13-21, 24			
Dynamic Burn-In (Note 1)		12	3, 15, 16, 21, 24	1, 2, 4-7, 22, 23	8, 10, 14, 19, 20	9, 11, 13, 17, 18
Irradiation (Note 2)	1, 2, 4-7, 22, 23	12	3, 8-11, 13-21, 24			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Block Diagram

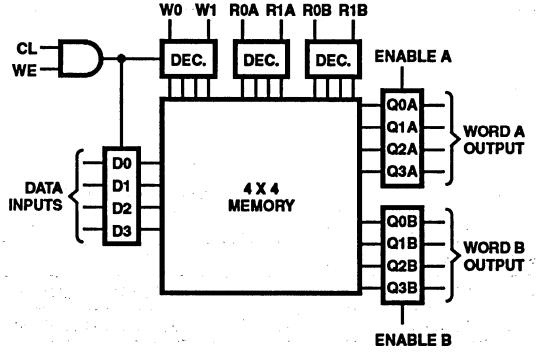


FIGURE 1.

Logic Diagram

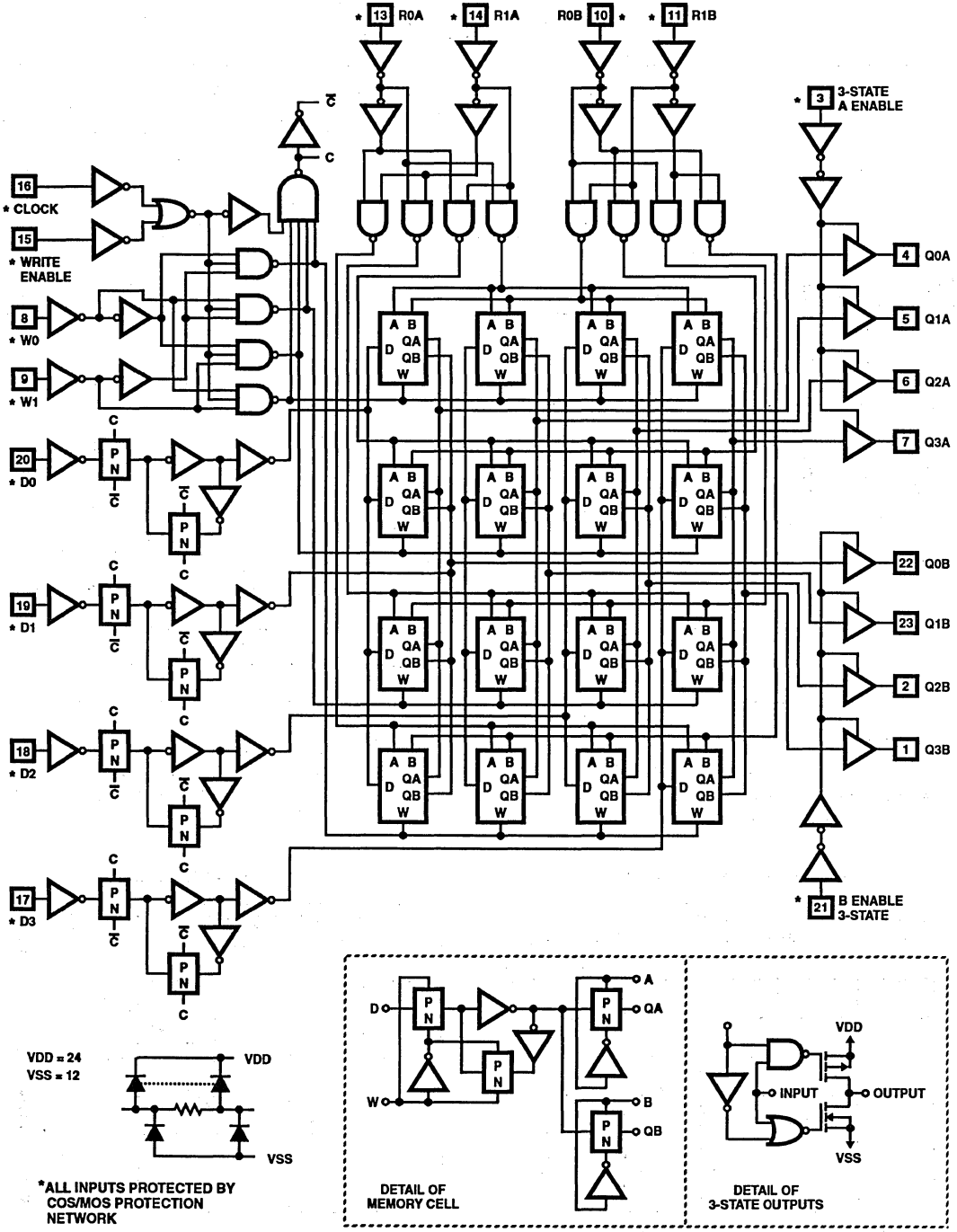


FIGURE 2.

TRUTH TABLE

CLOCK	WRITE ENABLE	WRITE 1	WRITE 0	READ 1A	READ 0A	READ 1B	READ 0B	ENABLE A	ENABLE B	Dn	QnA	QnB
↗	1	S1	S2	S1	S2	S1	S2	1	1	1	1	1
↗	1	S1	S2	S1	S2	S1	S2	1	1	0	0	0
X	X	X	X	X	X	X	X	0	0	X	Z	Z
↗	1	0	0	0	1	1	0	1	1	Dn to Word 0	Word 1 Out	Word 2 Out
↗	0	0	0	0	1	1	0	1	1	Word 0 Not Altered	Word 1 Out	Word 2 Out
X	X	X	X	1	0	0	1	1	1	X	Word 2 Out	Word 1 Out
↘	X	X	X	X	X	X	X	1	1	X	NC	NC

1 = High Level; 0 = Low Level; X = Don't Care; Z = High Impedance

NOTE: S1 and S2 refer to input states of either 1 or 0.

Typical Performance Characteristics

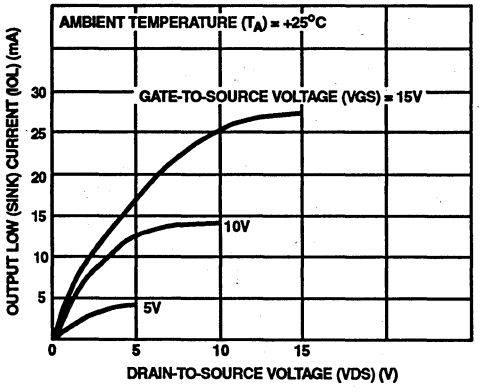


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

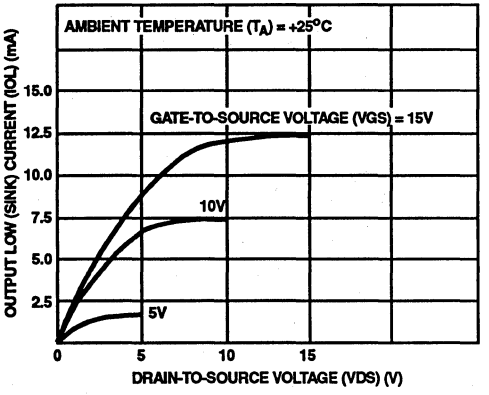


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

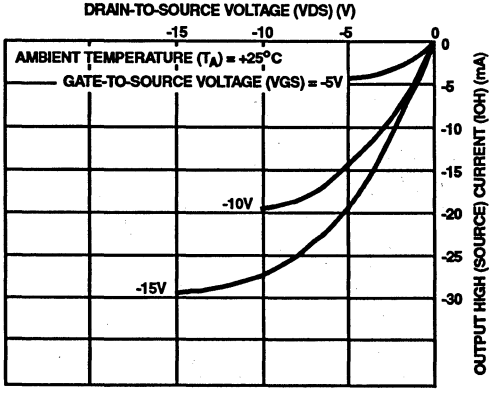


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

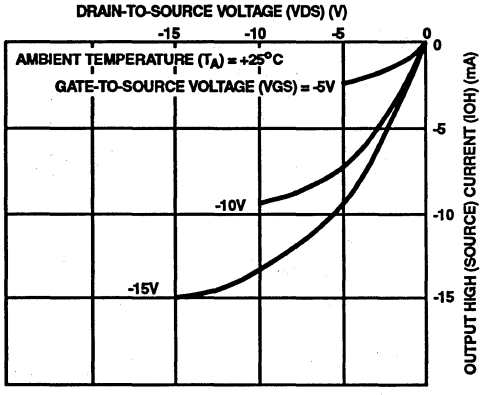


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

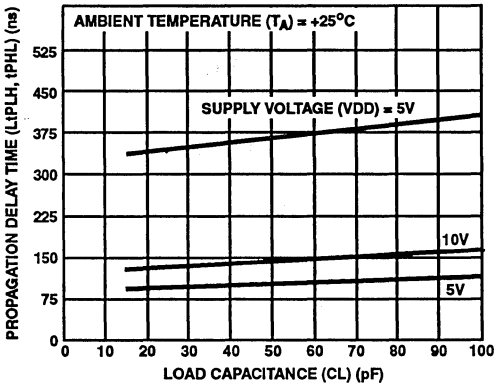


FIGURE 7. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (CL OR WE TO Q)

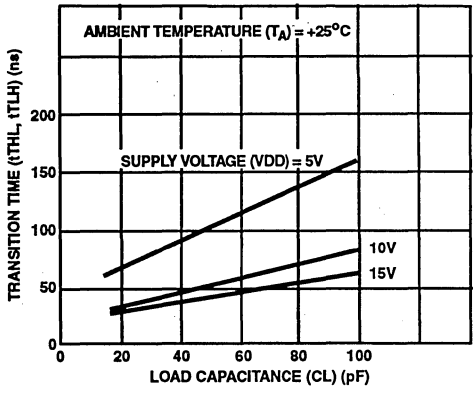


FIGURE 8. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

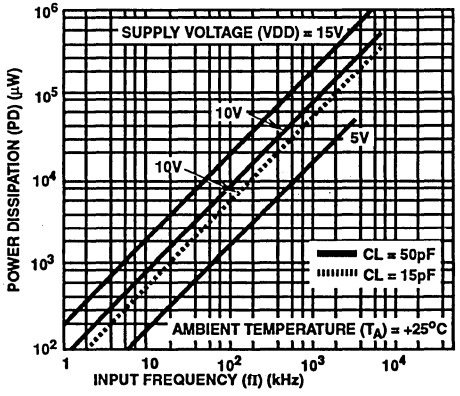


FIGURE 9. TYPICAL POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

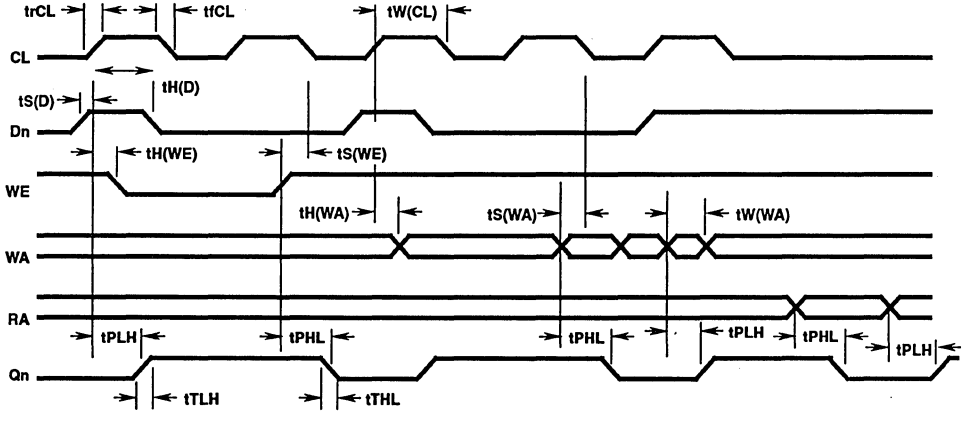


FIGURE 10. TIMING DIAGRAM

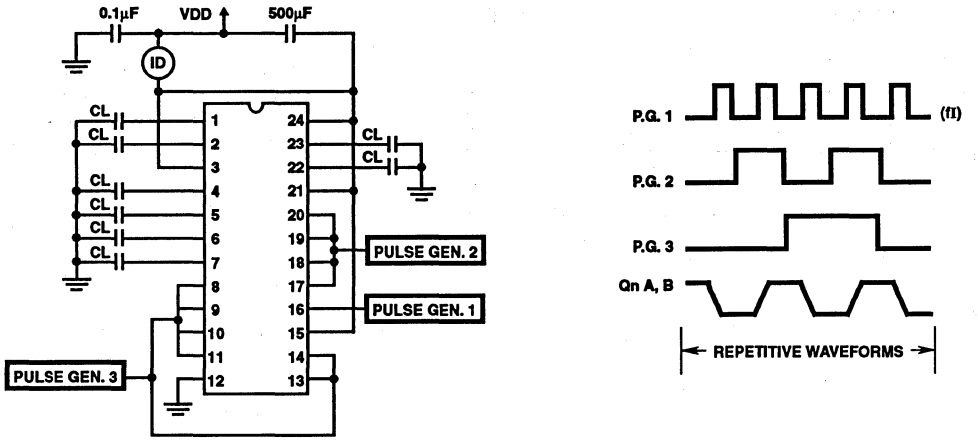
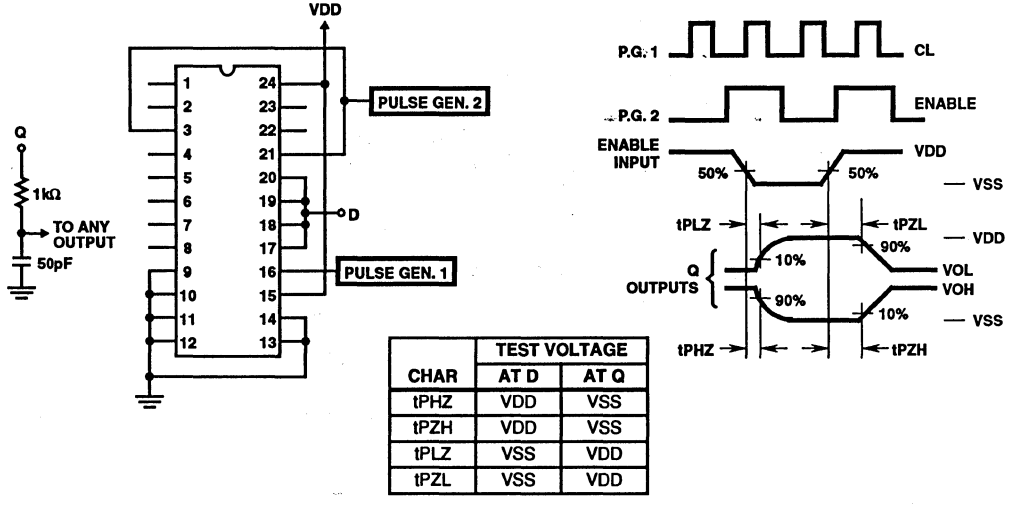


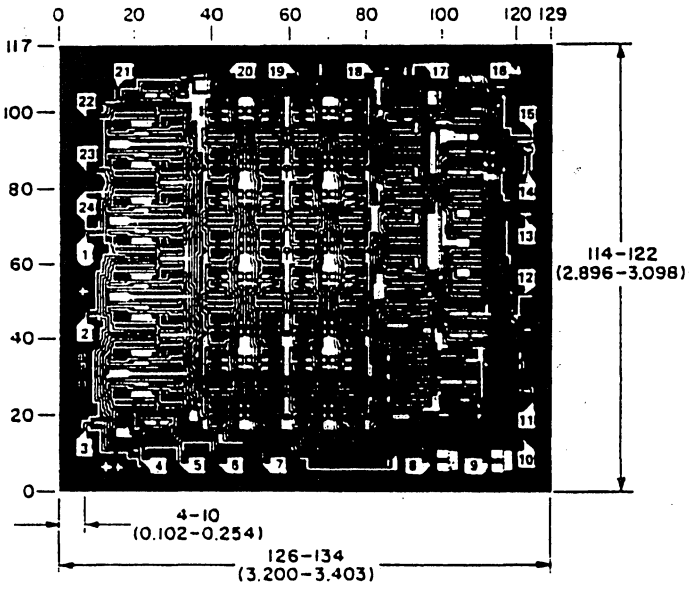
FIGURE 11. POWER-DISSIPATION TEST CIRCUIT AND WAVEFORMS



CHAR	TEST VOLTAGE AT D	AT Q
tPHZ	VDD	VSS
tPZH	VDD	VSS
tPLZ	VSS	VDD
tPZL	VSS	VDD

FIGURE 12. OUTPUT-ENABLE-DELAY-TIMES TEST CIRCUIT AND WAVEFORMS

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10-3 inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

HARRIS SEMICONDUCTOR

CD40257BMS

CMOS Quad 2 Line to 1 Line Data Selector/Multiplexer

December 1992

Features

- High Voltage Type (20V Rating)
- 3-State Outputs
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V
- Standardized Symmetrical Output Characteristics
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Digital Multiplexing
- Shift Right/Shift Left Registers
- True/Complement Selection

Description

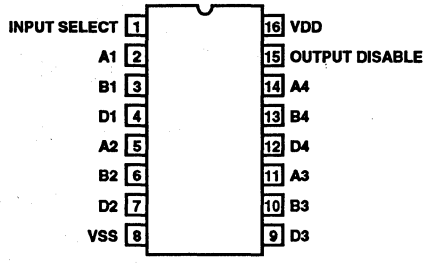
CD40257BMS is a data selector/multiplexer featuring three state outputs which can interface directly with and drive data lines of bus oriented systems.

The CD40257BMS is supplied in these 16-lead outline packages:

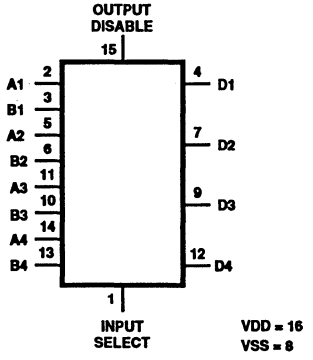
Braze Seal DIP	H4T
Frit Seal DIP	H1E
Ceramic Flatpack	H3X

Pinout

CD40257BMS
TOP VIEW



Functional Diagram



Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) ..... -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs .....-0.5V to VDD +0.5V
DC Input Current, Any One Input.....±10mA
Operating Temperature Range..... -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG)..... -65°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K)..... 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) .....Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature ..... +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.4	-	µA
				2	+125°C	-12	-	µA
			VDD = 18V	3	-55°C	-0.4	-	µA
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.4	µA
				2	+125°C	-	12	µA
			VDD = 18V	3	-55°C	-	0.4	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Data Input Output	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND (Notes 1, 2)	9	+25°C	-	300	ns
			10, 11	+125°C, -55°C	-	405	ns
Propagation Delay Select to Output	TPHL TPLH2	VDD = 5V, VIN = VDD or GND (Notes 1, 2)	9	+25°C	-	380	ns
			10, 11	+125°C, -55°C	-	513	ns
Propagation Delay Output Disable to Output	TPZH, HZ TPZL, LZ	VDD = 5V, VIN = VDD or GND (Notes 2, 3)	9	+25°C	-	190	ns
			10, 11	+125°C, -55°C	-	257	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND (Notes 1, 2)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.
3. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS(Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Data Input to Output	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	140	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Propagation Delay Select to Output	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	170	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Propagation Delay Output Disable to Output	TPZH, HZ TPZL, LZ	VDD = 10V	1, 2, 4	+25°C	-	100	ns
		VDD = 15V	1, 2, 4	+25°C	-	80	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN		1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

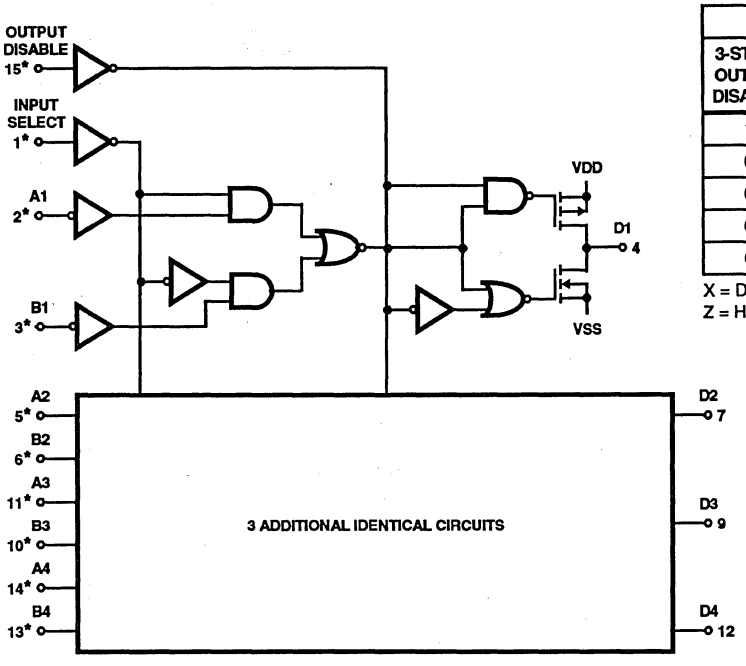
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	4, 7, 9, 12	1-3, 5, 6, 8, 10, 11, 13-15	16			
Static Burn-In 2 (Note 1)	4, 7, 9, 12	8, 15	1-3, 5, 6, 10, 11, 13, 14, 16			
Dynamic Burn-In (Note 1)	-	8, 15	16	4, 7, 9, 12	2, 3, 5, 6, 10, 11, 13, 14	1
Irradiation (Note 2)	4, 7, 9, 12	8	1-3, 5, 6, 10, 11, 13-16			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

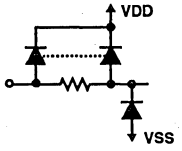
Logic Diagram



TRUTH TABLE

INPUTS				OUTPUT
3-STATE OUTPUT DISABLE	SELECT	A	B	D
1	X	X	X	Z
0	0	0	X	0
0	0	1	X	1
0	1	X	0	0
0	1	X	1	1

X = Don't care Logic 1 = High Logic 0 = Low
Z = High impedance



* ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

FIGURE 1.

Typical Performance Characteristics

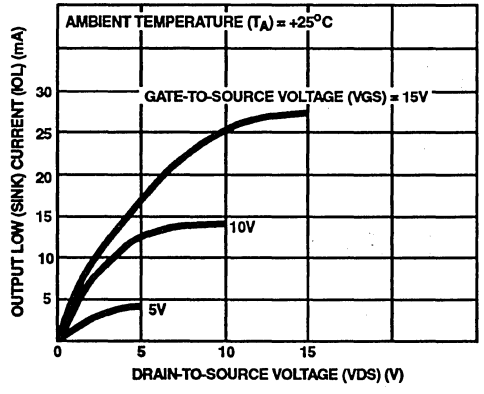


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

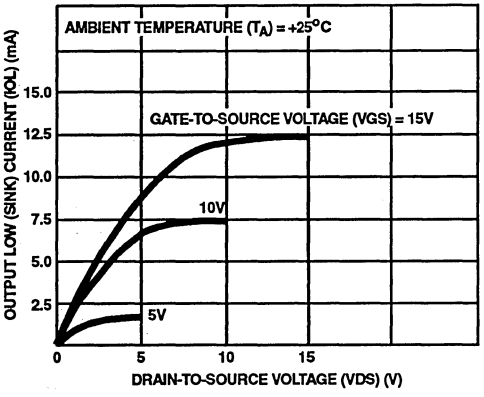


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

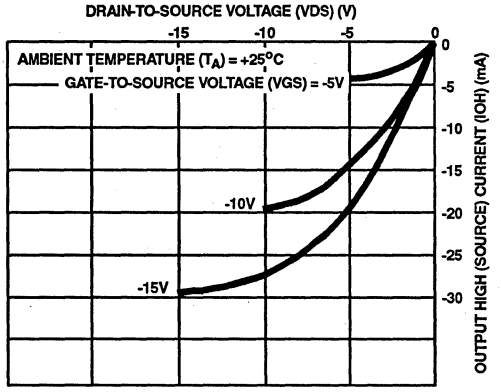


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

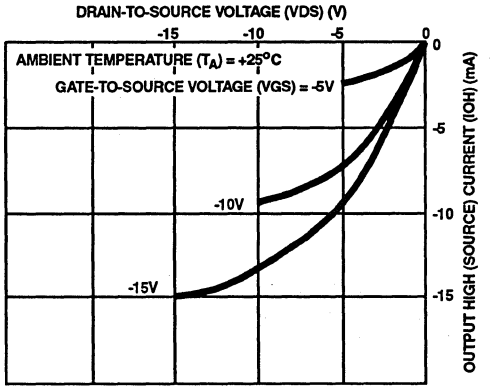


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

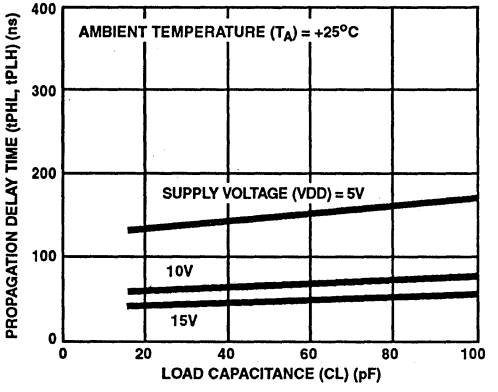


FIGURE 6. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (DATA INPUT TO OUTPUT)

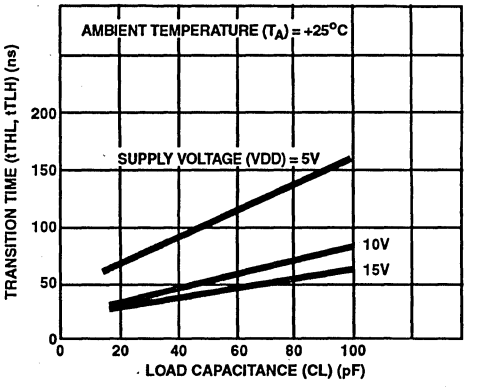


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

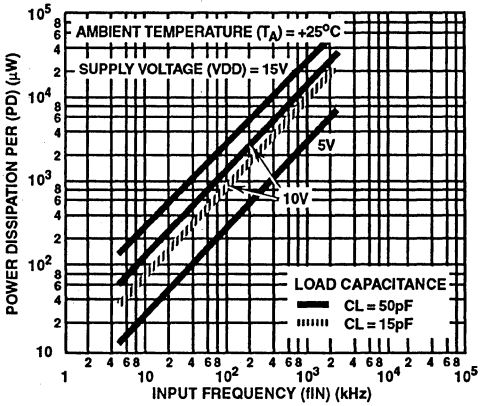
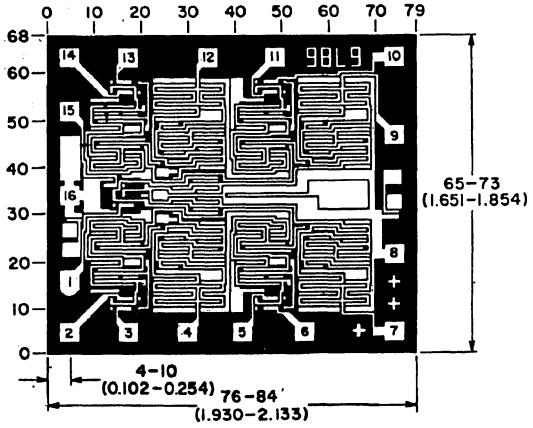


FIGURE 8. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY (ONE INPUT TO ONE OUTPUT)

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

RAD HARD 8

MEMORIES

HARRIS SEMICONDUCTOR

HS-65758RH
HS-65759RH

PRELIMINARY

December 1992

Radiation Hardened
32K x 8 SOI CMOS Static RAM

Features

- 0.8 Micron Radiation Hardened SOI CMOS
  - Total Dose 3 x 10^5 RAD (Si)
  - Transient Upset 1 x 10^{11} RAD (Si)/s
  - Single Event Upset 1 x 10^{-10} Errors/Bit-Day
- LET Threshold >90 Mev/mg/cm^2
- Latch-up Free
- Low Standby Supply Current 2mA (Max)
- Fast Access Time 35ns
- No Substrate Bias Required
- Gated Input Buffers
- Six Transistor Memory Cell
- Fully Static Design
- Asynchronous Operation
- CMOS Inputs
- 5V Single Power Supply
- Standard JEDEC DIP Pinout
- Military Temperature Range -55°C to +125°C

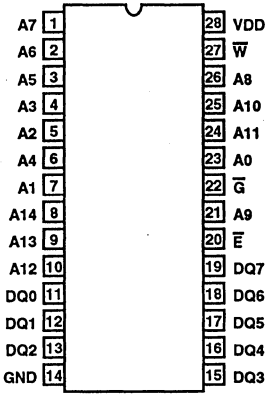
Description

The Harris HS-65758RH is an asynchronous, fully static RAM fabricated with the Harris SOI RHD1 radiation hardened process. The use of this process provides excellent total dose, dose rate and single event immunity. As with any oxide isolated circuits, the HS-65758RH will not latch-up under any conditions.

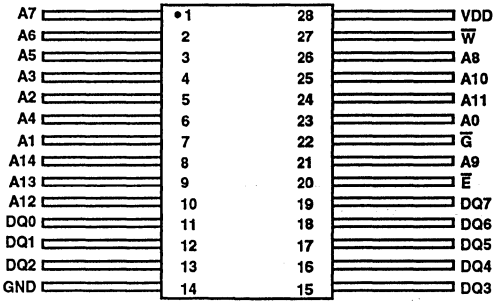
Low power operation is provided by a fully static design. Low standby power can be achieved without pull-up resistors, due to the gated input buffer design.

Pinouts

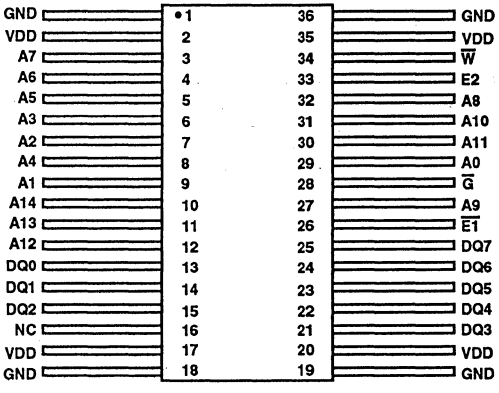
HS1-65758RH 28 PIN SIDEBRAZE DIP
TOP VIEW



HS9-65758RH 28 PIN FLATPACK
TOP VIEW



HS9-65759RH 36 PIN FLATPACK
TOP VIEW

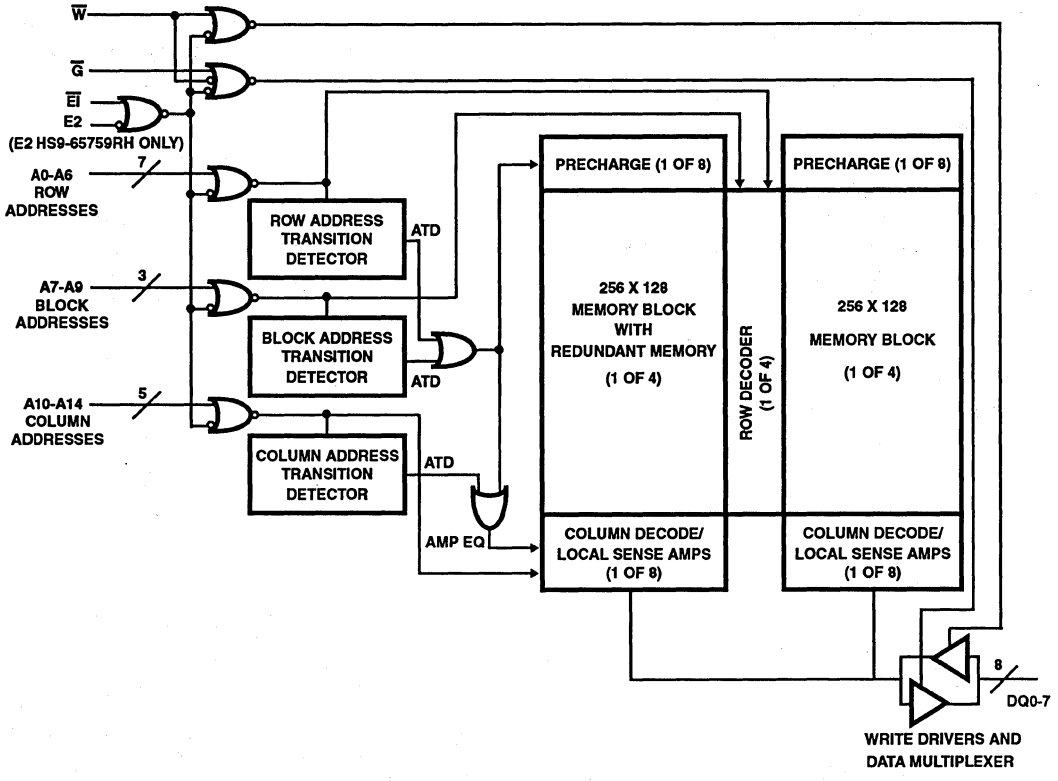


8 MEMORIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2860.1**

Functional Diagram



Truth Tables

HS-65758RH

28 PIN SIDEBRAZE DIP AND 28 PIN FLATPACK			
$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE
I	X	X	Low Power Standby
O	I	I	Enabled
O	O	I	Read
O	I	O	Write

HS9-65759RH

36 PIN FLATPACK ONLY				
$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	MODE
I	O	X	X	Low Power Standby
I	I	X	X	Low Power Standby
O	O	X	X	Low Power Standby
O	I	I	I	Enabled
O	I	O	I	Read
O	I	I	O	Write

Absolute Maximum Ratings

Supply Voltage ..... -0.3V to +6.0V
Input or Output Voltage
Applied for all Grades ..... GND-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 2.75mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
28 Pin Braze Seal DIP	28.5°C/W	8.0°C/W
28 Pin Braze Seal Flatpack	53.5°C/W	7.38°C/W
36 Pin Braze Seal Flatpack	TBD°C/W	TBD°C/W

Maximum Package Power Dissipation at +125°C
28 Pin Braze Seal DIP 1.75W
28 Pin Braze Seal Flatpack 0.935W
36 Pin Braze Seal Flatpack ..... TBD W
Gate Count ..... 400,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage Range (VDD) ..... +4.5V to +5.5V
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0V to 0.3VDD
Input High Voltage (VIH) ..... 0.7VDD to VDD
Data Retention Supply Voltage 2.0V
Input Rise and Fall Time ..... 40ns Max

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH 1	VDD = 4.5V, IO = -4.0mA, VI = VDD or GND	1, 2, 3	-55°C, +25°C, +125°C	2.4	-	V
	VOH 2	VDD = 4.5V, IO = -1mA, VI = VDD or GND	1, 2, 3	-55°C, +25°C, +125°C	VDD-0.4V	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, IO = 8.0mA, VI = VDD or GND	1, 2, 3	-55°C, +25°C, +125°C	-	0.4	V
High Impedance Output Leakage Current	IOZL or IOZH	VDD = 5.5V, VO = GND or VDD, VI = VDD or GND, $\overline{E}$ = VDD	1, 2, 3	-55°C, +25°C, +125°C	-10	10	µA
Input Leakage Current	IIH or IIL	VDD = 5.5V, VI = VDD or GND	1, 2, 3	-55°C, +25°C, +125°C	-10	10	µA
Standby Supply Current	IDDSB	VDD = 5.5V, IO = 0mA, VI = VDD or GND, $\overline{E}$ = VDD	1, 2, 3	-55°C, +25°C, +125°C	-	1	mA
Enable Supply Current	IDDEN	VDD = 5.5V, IO = 0mA, VI = VDD or GND, $\overline{E}$ = 0.0V, Checker Board Pattern	1, 2, 3	-55°C, +25°C, +125°C	-	65	mA
Operating Supply Current (Note 2)	IDDOP	VDD = 5.5V, IO = 0mA, VI = VDD or 0.0V, $\overline{E}$ = 0.0V, f = 10MHz, $\overline{G}$ = VDD, Checker Board Pattern	1, 2, 3	-55°C, +25°C, +125°C	-	95	mA
Data Retention Supply Current	IDDDR	VDD = 2.5V, IO = 0mA, VI = VDD or GND, $\overline{E}$ = VDD	1, 2, 3	-55°C, +25°C, +125°C	-	250	µA
Functional Tests	FT	VDD = 4.5V and 5.5V, VI = VDD or GND, f = 1MHz	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-
Noise Immunity Functional Test	FN	VDD = 4.5V and 5.5V, VIL = 0.2 VDD, VIH = 0.8 VDD, f = 1MHz	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-

NOTES:

1. All Voltages referenced to device GND.
2. Typical IDDOP derating = 2.75mA/MHz (2.75mA increase in IDDOP per 1MHz increase in address frequency.)

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Access Time	TAVQV	VDD = 4.5V and 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	35	ns
Chip Enable Access Time	TELQV	VDD = 4.5V and 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	35	ns
Write Recovery Time	TWHAX	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
Address Hold Time	TEHAX	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
Chip Enable to End-of-Write	TELWH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	30	-	ns
Address Valid to End-of-Write	TAVEH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	30	-	ns
Chip Enable Pulse Width	TELEH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	30	-	ns
Address Setup Time	TAVWL	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
	TAVEL	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
Write to End-of-Write	TWLEH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	30	-	ns
Write Enable Pulse Width	TWLWH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	30	-	ns
Data Setup Time	TDVWH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	18	-	ns
	TDVEH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	18	-	ns
Address Valid to End-of-Write	TAVWH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	30	-	ns
Data Hold Time	TWHDX	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
	TEHDX	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
Output Enable Valid Time	TGLQV	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	-	15	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V or VDD; timing reference levels = 1.5V; output load = 1TTL equivalent load and CL ≥ 50pF, for CL > 50pF, access times are derated 0.15ns/pF.
3. For timing waveforms see Low Voltage Data Retention and Read/Write Cycles.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance (Note 2)	CIN	VDD = Open, f = 1MHz	T_A = +25°C	-	10	pF
I/O Capacitance (Note 2)	COUT	VDD = Open, f = 1MHz	T_A = +25°C	-	12	pF
Write Enable to Output in High Z	TWLQZ	VDD = 4.5V and 5.5V	-55°C ≤ T_A ≤ +125°C	-	15	ns
Write Enable High to Output ON	TWHQX	VDD = 4.5V and 5.5V	-55°C ≤ T_A ≤ +125°C	5	-	ns
Chip Enable to Output ON	TELQX	VDD = 4.5V and 5.5V	-55°C ≤ T_A ≤ +125°C	5	-	ns
Chip Enable to Output in High Z	TEHQZ	VDD = 4.5V and 5.5V	-55°C ≤ T_A ≤ +125°C	-	15	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Read/Write/Cycle Time	TAVAX	VDD = 4.5V and 5.5V	-55°C, +25°C, +125°C	35	-	ns
Output Hold from Address Change	TAXQX	VDD = 4.5V and 5.5V	-55°C ≤ T_A ≤ +125°C	5	-	ns
Output Enable to Output ON	TGLQX	VDD = 4.5V and 5.5V	-55°C ≤ T_A ≤ +125°C	2	-	ns
Output Disable Time	TGHQZ	VDD = 4.5V and 5.5V	-55°C ≤ T_A ≤ +125°C	-	15	ns
Write Cycle Time	TAVAX	VDD = 4.5V and 5.5V	-55°C ≤ T_A ≤ +125°C	35	-	ns
Operating Supply Currents	IDDOP	VDD = 5.5V, IO = 0mA, VI = VDD or 0V, $\overline{E}$ = 0V, f = 20MHz, $\overline{G}$ = GND, Checker Board pattern	-55°C, +25°C, +125°C	-	120	mA

NOTES:

1. The parameters listed are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. All measurements referenced to device ground.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISITCS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Standby Supply Current	IDDSB	VDD = 5.5V, IO = 0mA, $\overline{E}$ = VDD, VI = VDD or 0.0V	+25°C	-	2	mA
Enabled Supply Current	IDDEN	VDD = 5.5V, IO = 0mA, $\overline{E}$ = 0.0V, VI = VDD or 0.0V, Checker Board Pattern	+25°C	-	65	mA
Operating Supply Current (Note 2)	IDDOP	VDD = 5.5V, IO = 0mA, f = 10MHz, $\overline{E}$ = 0.0V, VI = VDD or 0.0V, $\overline{G}$ = VDD, Checker Board Pattern	+25°C	-	95	mA
Data Retention Supply Current	IDDDR	VDD = 2.0V, IO = 0mA, $\overline{E}$ = VDD	+25°C	-	1.0	mA

NOTES:

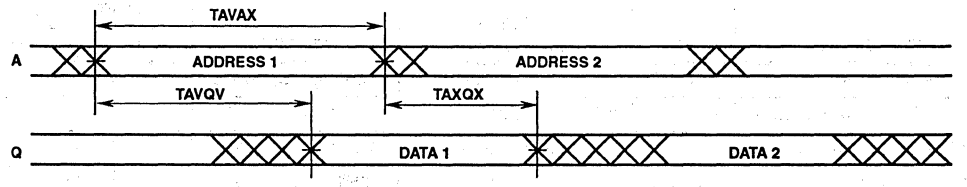
1. DC parameters not listed in this table are tested at the +25°C pre-irradiation test limits. All AC parameters are tested at the +25°C pre-irradiation test limits.
2. Typical IDDOP derating = 2.75mA/MHz. (2.75mA increase in IDDOP per 1MHz increase in address frequency.)

TABLE 5. APPLICABLE SUBGROUPS

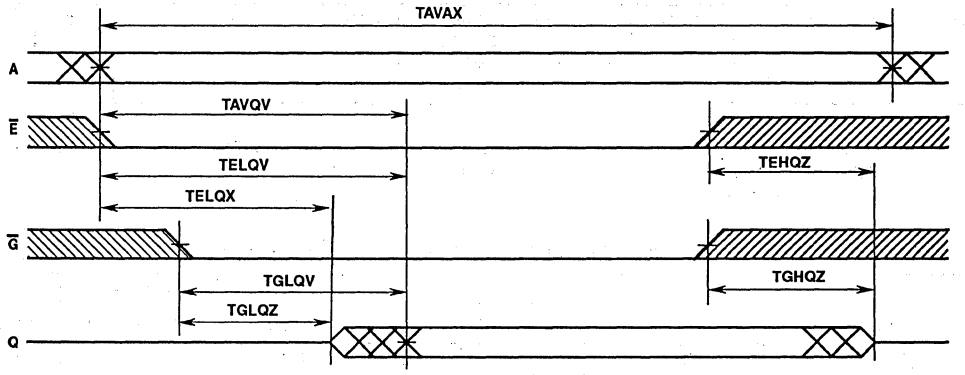
CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9
Interim Test 1 and 2		100%/5004	1, 7, 9	N/A
PDA 1 and 2		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A
	Others	Samples/5005	1, 7	N/A
Group C (Optional)		Samples/5005	N/A	1, 7
Group D (Optional)		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7, 9	1, 7, 9

Timing Waveforms

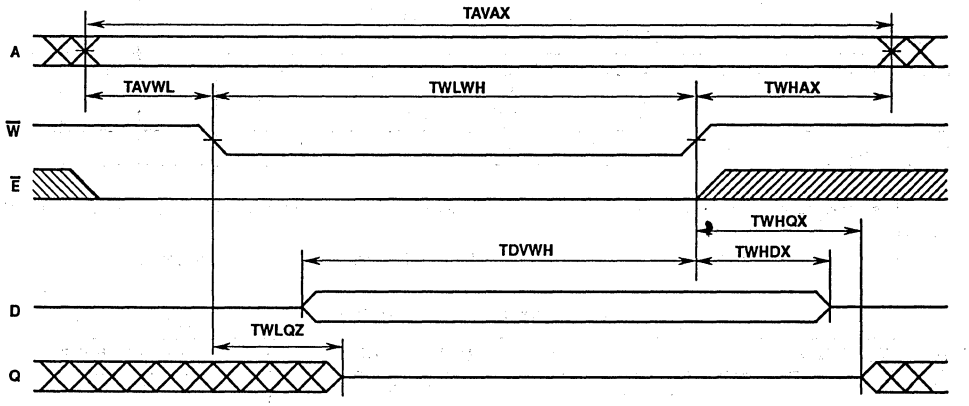
READ CYCLE I: $\overline{W}$, $\overline{G}$, $\overline{E}$ LOW



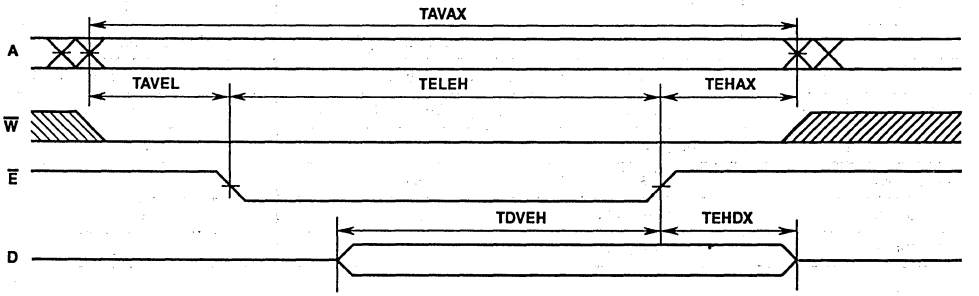
READ CYCLE II: $\overline{W}$ HIGH



WRITE CYCLE I: LATE WRITE

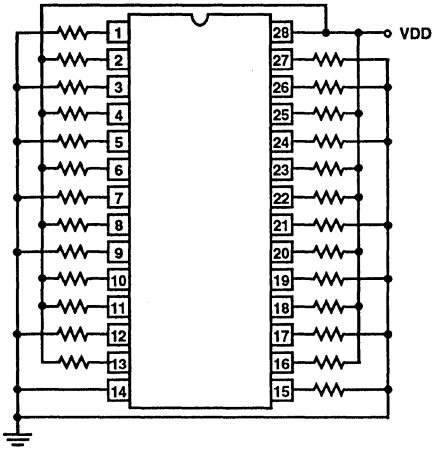


WRITE CYCLE II: EARLY WRITE - CONTROLLED BY $\overline{E}$



Burn-In Circuits

HS9-65758RH, HS1-65758RH

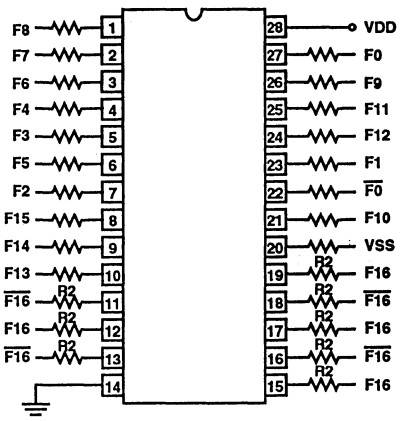


STATIC CONFIGURATION

NOTES:

Power Supply: VDD = 6.0V ± 0.5V
Resistors = 47KΩ ± 10%
IDD < 5mA per socket

HS9-65758RH, HS1-65758RH

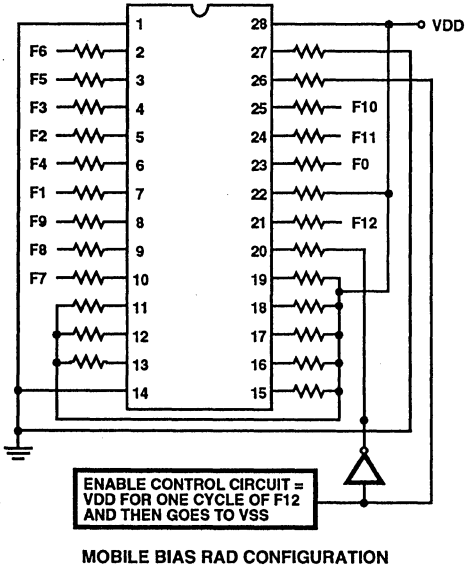


DYNAMIC CONFIGURATION

NOTES:

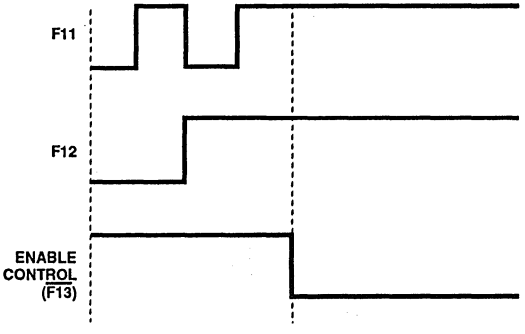
Power Supply: VDD = 6.0V ± 0.5V for Burn-In
Power Supply: VDD = 5.5V ± 0.5V for Life Test
Resistors = 10KΩ ± 10%, >0.25W, except
R2 = 47KΩ ± 10%, >0.25W
VIH = 5.5 ± 0.5V, VIL = 0.4V ± 0.4V for Burn-In
VIH = 5.0 ± 0.5V, VIL = 0.4V ± 0.4V for Life Test
IDD < 100mA per socket
F0 = 100KHz ± 10%, 50% Duty Cycle
F1 = F0/2; F2 = F1/2; F3 = F2/2; F4 = F3/2; F5 = F4/2 . . . F16 = F15/2

64K RAM GROUP E QUALIFICATION DEVICE



MOBILE BIAS RAD CONFIGURATION

RAD INITIALIZATION WAVEFORMS
MOBILE BIAS FOR RHD1 8K x 8

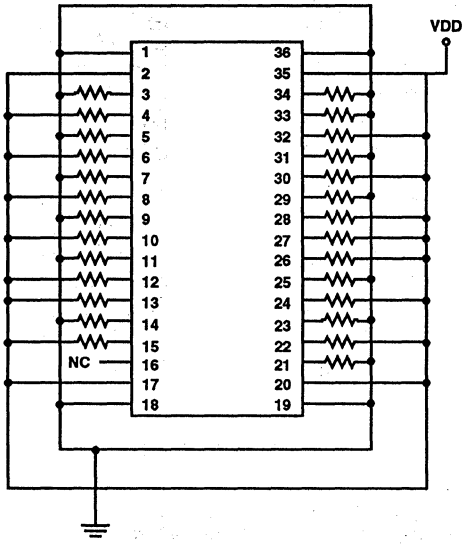


NOTES:

Power Supply: VDD = 5.5V
Resistors = 47KΩ ± 10%, >0.25W
VIH = 5.5 ± 0.5V, VIL = 0.4V ± 0.4V
F0 = 100KHz ± 10%, 50% Duty Cycle
F1 = F0/2; F2 = F1/2, F3 = F2/2; F4 = F3/2; F5 = F4/2 . . . F12 = F11/2

Burn-In Circuits (Continued)

HS9-65759RH

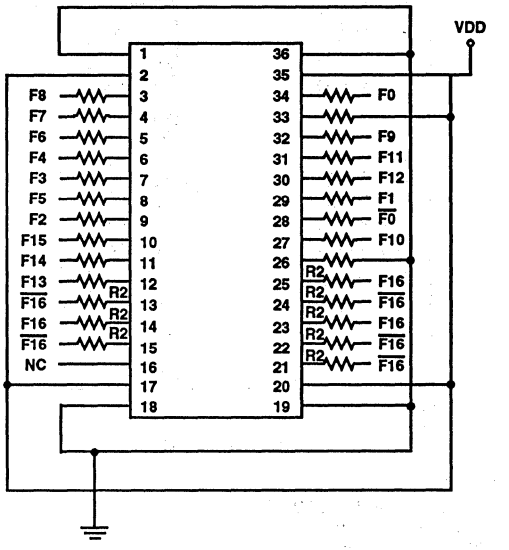


STATIC CONFIGURATION

NOTES:

Power Supply: VDD = 6.0V ± 0.5V
Resistors = 10KΩ ± 10%
IDD < 5mA per socket

HS9-65759RH



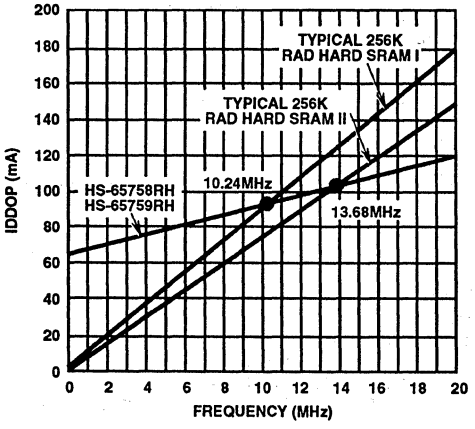
DYNAMIC CONFIGURATION

NOTES:

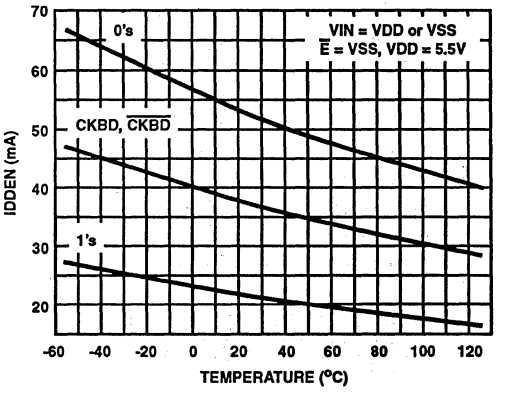
Power Supply: VDD = 6.0V ± 0.5V for Burn-In
Power Supply: VDD = 5.5V ± 0.5V for Life Test
Resistors = 10KΩ ± 10%, >0.25W, except
R2 = 47KΩ ± 10%, >0.25W
VIH = 5.5 ± 0.5V, VIL = 0.4V ± 0.4V for Burn-In
VIH = 5.0 ± 0.5V, VIL = 0.4V ± 0.4V for Life Test
IDD < 100mA per socket
F0 = 100KHz ± 10%, 50% Duty Cycle
F1 = F0/2; F2 = F1/2; F3 = F2/2; F4 = F3/2; F5 = F4/2 . . . F16 = F15/2

Typical Performance Curves

HS-65758, HS-65758RH (32K x 8 SOI SRAM) IDDOP COMPARISON WITH TYPICAL 256K RAD HARD SRAMS



HS-65758RH, HS-65759RH TYPICAL ENABLED CURRENT OVER TEMPERATURE FOR DIFFERENT PATTERNS



Harris - Space Level Product Flow

SEM - Traceable to Diffusion Method 2018
Wafer Lot Acceptance Method 5007
Internal Visual Inspection (Note 1)
Gamma Radiation Assurance Tests
100% Nondestructive Bond Pull Method 2023
Customer Pre-Cap Visual Inspection (Notes 1, 2)
Temperature Cycling Method 1010 Condition C
constant Acceleration method 2001 Y1 30KG
Particle Impact Noise Detection method 2020, Condition A 20G
Marking and Serialization
Initial Electrical Tests (T0)
Static Burn-In 72 Hour, +125°C method 1015 Condition A
Room Temperature Electrical Tests (T1)
Burn-In Delta Calculation (T0-T1)
PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ
Dynamic Burn-In 240 Hours, +125°C Method 1015 Condition D
Electrical Tests Subgroups 1, 7, 9 (T2)
Delta Calculation (T0 - T2)
PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ
Electrical Test +125°C, -55°C
Group A Inspection Method 5005
X-Ray Inspection Method 2012
Fine and Gross Leak Tests Method 1014
Customer Source Inspection (Note 2)
Group B Inspection (Notes 2, 4) Method 5005
Group D Inspection (Notes 2, 4) Method 5005
External Visual Inspection Method 2009
Data Package Generation (Note 3)

NOTES:

1. Visual Inspection is performed to MIL-STD-883 Method 2010, Condition B alternate screening in lieu of high power visual inspection.
2. These steps are optional, and should be listed on the purchase order if required.
3. Data package contains:
   - Assembly Attributes (post seal)
   - Test Attributes (includes Group A) -55°C, +25°C, +125°C
   - Shippable Serial Number List
   - Radiation Testing Certificate of Conformance
   - Wafer Lot Acceptance Report (includes SEM report)
   - X-Ray Report and Film
   - Test Variables Data, DC Test and TELQV
     - +25°C Initial Test
     - +25°C Interim Test 1
     - +25°C Interim Test 2
     - +25°C Delta Over Burn-In
4. Group B data package contains Attributes Data pulse Variables Data, DC Test and TELQV. Group D data package contains Attributes only.
5. Total Dose Radiation sample selection shall be in accordance with Method 5005, Group E Subgroup 2 except 64K RAM test devices from the HS-65758/9 wafers undergoing Group E qualification will be used for Rad testing.

Metallization Topology

DIE DIMENSIONS:
8310 x 11790µm x 584µm

METALLIZATION:
Metal 1 Thickness: 8kÅ ± 2kÅ
Metal 1 Type = TiW
Metal 2 Thickness: 16kÅ ± 2kÅ
Metal 2 Type = Al/Si/Cu

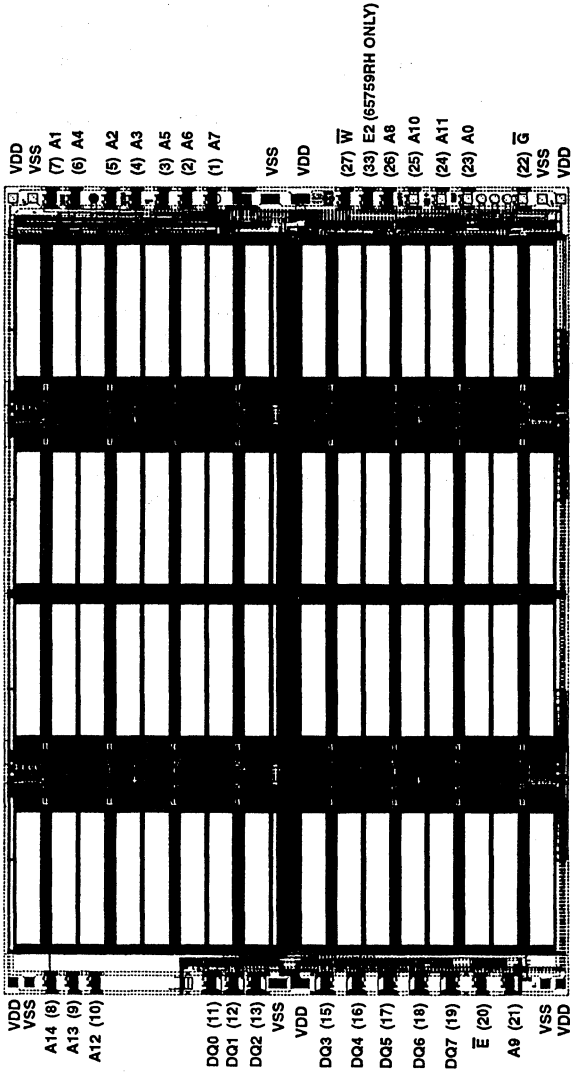
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Silver Glass

WORST CASE CURRENT DENSITY:
1.5×10^5 A/cm^2

Metallization Mask Layout

HS-65758RH



HARRIS SEMICONDUCTOR

HS-65647RH

Radiation Hardened 8K x 8 SOS CMOS Static RAM

December 1992

Features

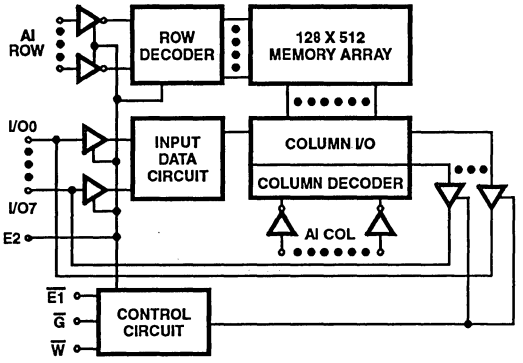
- 1.2 Micron Radiation Hardened SOS CMOS
  - Total Dose 3 x 10^5 RAD (Si)
  - Transient Upset >1 x 10^{11} RAD (Si)/s
  - Single Event Upset < 1 x 10^{-12} Errors/Bit-Day
- Latch-up Free
- LET Threshold >250 MeV/mg/cm2
- Low Standby Supply Current 10mA (Max)
- Low Operating Supply Current 100mA (2MHz)
- Fast Access Time 50ns (Max), 35ns (Typ)
- High Output Drive Capability
- Gated Input Buffers (Gated by E2)
- Six Transistor Memory Cell
- Fully Static Design
- Asynchronous Operation
- CMOS Inputs
- 5V Single Power Supply
- Military Temperature Range -55°C to +125°C
- Industry Standard JEDEC Pinout

Description

The Harris HS-65647RH is a fully asynchronous 8K x 8 radiation hardened static RAM. This RAM is fabricated using the Harris 1.2 micron silicon-on-sapphire CMOS technology. This technology gives exceptional hardness to all types of radiation, including neutron fluence, total ionizing dose, high intensity ionizing dose rates, and cosmic rays.

Low power operation is provided by a fully static design. Low standby power can be achieved without pull-up resistors, due to the gated input buffer design.

Functional Diagram



TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	MODE
X	0	X	X	Low Power Standby
1	1	X	X	Disabled
0	1	1	1	Enabled
0	1	0	1	Read
0	1	X	0	Write

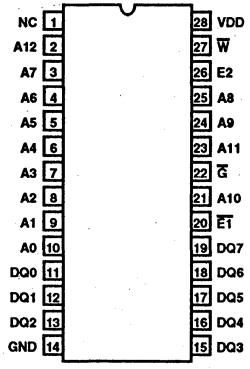
8 MEMORIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

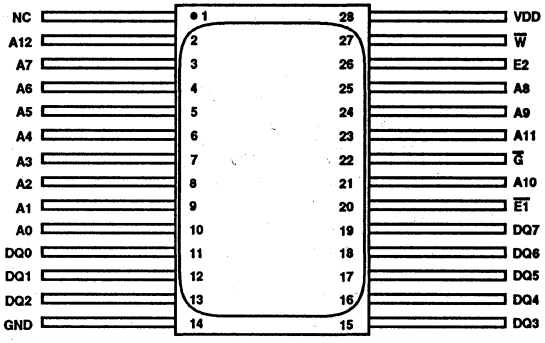
File Number 2928.1

Pinouts

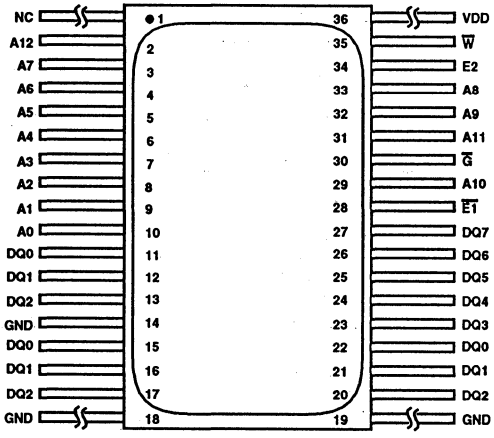
HS1-65647RH 28 PIN CERAMIC DIP
CASE OUTLINE D-10, CONFIGURATION 3
TOP VIEW



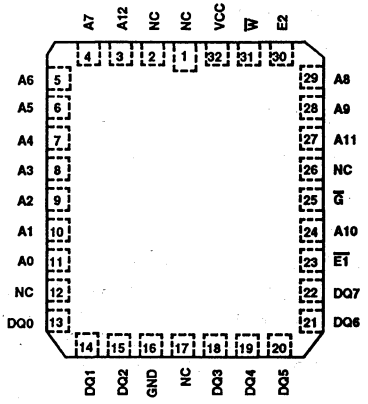
HS9-65647RH 28 PIN FLATPACK
CASE OUTLINE F11A, CONFIGURATION 2
TOP VIEW



HS9A65647RH 36 PIN FLATPACK
INTERNAL PACKAGE CODE "HFQ"
TOP VIEW



HM4-65647RH 32 PIN CERAMIC LCC
INTERNAL PACKAGE CODE "HPQ"
TOP VIEW



Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage ..... GND-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 3mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	28.5°C/W	8.0°C/W
Braze Seal Flatpack Package	53.4°C/W	7.4°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package 1.75W
Braze Seal Flatpack Package 936mW
Gate Count ..... 101,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range (VDD) ..... +4.5V to +5.5V
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0V to +0.2VDD
Input High Voltage (VIH) ..... 0.8VDD to VDD
Data Retention Supply Voltage 2.0V
Input Rise and Fall Time ..... 40ns Max.

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH	VDD = 4.5V, IO = -5mA VI = VDD or GND	1, 2, 3	-55°C, +25°C, +85°C, +125°C	VDD-0.4	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, IO = 8.0mA VI = VDD or GND	1, 2, 3	-55°C, +25°C, +85°C, +125°C	-	0.4	V
High Impedance Output Leakage Current	IOZL or IOZH	VDD = 5.5V, VO = GND or VDD, VI = VDD or GND $\overline{E1}$ = VDD, E2 = 0V	1, 3	-55°C, +25°C	-10	10	µA
			2	+85°C	-30	30	µA
			2	+125°C	-60	60	µA
Input Leakage Current	IIH or IIL	VDD = 5.5V, VI = VDD or GND	1, 2, 3	-55°C, +25°C, +85°C, +125°C	-1.0	1.0	µA
Standby Supply Current	IDDSB (Note 3)	VDD = 5.5V, IO = 0mA, VI = VDD or GND $\overline{E1}$ = VDD, E2 = 0V	1, 3	-55°C, +25°C	-	500	µA
			2	+85°C	-	4	mA
			2	+125°C	-	10	mA
Enable Supply Current	IDDEN	VDD = 5.5V, IO = 0mA, VI = VDD or GND $\overline{E1}$ = 0.0V, E2 = VDD	3	-55°C	-	77	mA
			1	+25°C	-	73	mA
			2	+85°C, +125°C	-	64	mA
Operating Supply Current (Note 2)	IDDOP	VDD = 5.5V, IO = 0mA, VI = VDD or GND, E2 = VDD, $\overline{E1}$ = 0V, f = 2MHz	3	-55°C	-	100	mA
			1	+25°C	-	86	mA
			2	+85°C, +125°C	-	75	mA
Data Retention Supply Current	IDDDR	VDD = 2.0V, IO = 0mA, VI = VDD or GND $\overline{E1}$ = VDD, E2 = 0V	1, 3	-55°C, +25°C	-	50	µA
			2	+85°C	-	1	mA
			2	+125°C	-	4	mA
Functional Tests	FT	VDD = 4.5V and 5.5V VI = VDD or GND, f = 1MHz	7, 8A, 8B	-55°C, +25°C, +85°C, +125°C	-	-	-
Noise Immunity Functional Test	FN	VDD = 4.5, VIL = 0.2 VDD VIH = 0.8 VDD, f = 1MHz	7, 8A, 8B	-55°C, +25°C, +85°C, +125°C	-	-	-

NOTE:

1. All voltages referenced to device GND.
2. Typical IDDOP derating = 3mA/MHz (3mA increase in IDDOP per 1MHz increase in address frequency.)
3. In order for this device to be in low power standby mode. E2 must be disabled (low).

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Access Time	TAVQV	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	-	50	ns
Output Enable Access Time	TGLQV	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	-	15	ns
Chip Enable Access Time	TE1LQV TE2HQV	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	-	50	ns
Write Recovery Time	TWHAX TE1HAX TE2LAX	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	0	-	ns
Chip Enable to End-of-Write	TE1LE1H TE2HE2L	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	35	-	ns
Address Setup Time	TAVWL TAVE1L TAVE2H	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	5	-	ns
Write Enable Pulse Width	TWLWH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	25	-	ns
Data Setup Time	TDVWH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	30	-	ns
	TDVE1H TDVE2L	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	30	-	ns
Data Hold Time	TWHDX	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	0	-	ns
Address Hold Time	TAVE1H TAVE2L	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	40	-	ns
	TE2LDX TE1HDX	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	0	-	ns

NOTES:

1. AC measurements tested at worst case VDD. Guaranteed over full operating range.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V to VDD; timing reference levels = 2.0V; output load = 1 TTL equivalent load and CL ≥ 50pF, for CL > 50pF, access times are derated 0.15ns/pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz	1, 2, 4	T_A = +25°C	-	12	pF
		VDD = Open, f = 1MHz	1, 2, 4	T_A = +25°C	-	12	pF
I/O Capacitance	CI/O	VDD = Open, f = 1MHz	1, 2, 4	T_A = +25°C	-	12	pF
		VDD = Open, f = 1MHz	1, 2, 4	T_A = +25°C	-	12	pF
Write Enable to Output in High Z	TWLQZ	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	-	10	ns
Write Enable High to Output ON	TWHQX	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	0	-	ns
Chip Enable to Output ON	TE1LQX TE2HQX	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	0	-	ns
Output Enable to Output ON	TGLQX	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	0	-	ns
Chip Enable to Output in High Z	TE1HQZ TE2LQZ	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	-	15	ns
Output Disable to Output in High Z	TGHQZ	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	-	15	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Hold from Address Change	TAXQX	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	0	-	ns

NOTES:

1. The parameters listed are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. Applies to DIP device types only.
3. Applies to Flatpack device types only.
4. All measurements referenced to device GND.

TABLE 4. POST 300K RAD DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Standby Supply Current	IDDSB	VDD = 5.5V, IO = 0mA, $\overline{E1}$ = VDD, E2 = 0V, VI = VDD or GND	+25°C	-	10	mA
Enabled Supply Current	IDDEN	VDD = 5.5V, IO = 0mA, $\overline{E1}$ = 0.0V, E2 = VDD, VI = VDD or GND	+25°C	-	82	mA
Operating Supply Current (Note 2)	IDDOP	VDD = 5.5V, IO = 0mA, f = 2MHz, $\overline{E}$ = 0V,VI = VDD or GND	+25°C	-	100	mA
Data Retention Supply Current	IDDDR	VDD = 2.0V, IO = 0mA, $\overline{E}$ = VDD	+25°C	-	6	mA

NOTES:

1. DC parameters not listed in this table are tested at the +25°C pre-irradiation test limits. All AC parameters are tested at the +25°C pre-irradiation test limits.
2. Typical IDDOP derating = 3mA/MHz (3mA increase in IDDOP per 1MHz increase in address frequency.)

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C), GROUP B, SUBGROUP 5

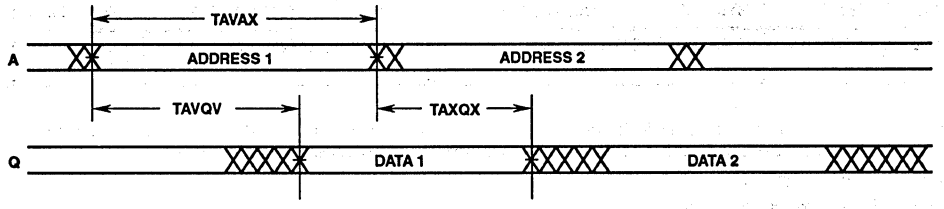
PARAMETER	SYMBOL	DELTA LIMITS
Standby Supply Current	IDDSB	±150µA
High Impedance Output Leakage Current	IOZH, IOZL	± 2µA
Input Leakage Current	IIH, IIL	± 150nA
Low Level Output Voltage	VOL	± 60mV
Output High Voltage	VOH	± 150mV

TABLE 6. APPLICABLE SUBGROUPS

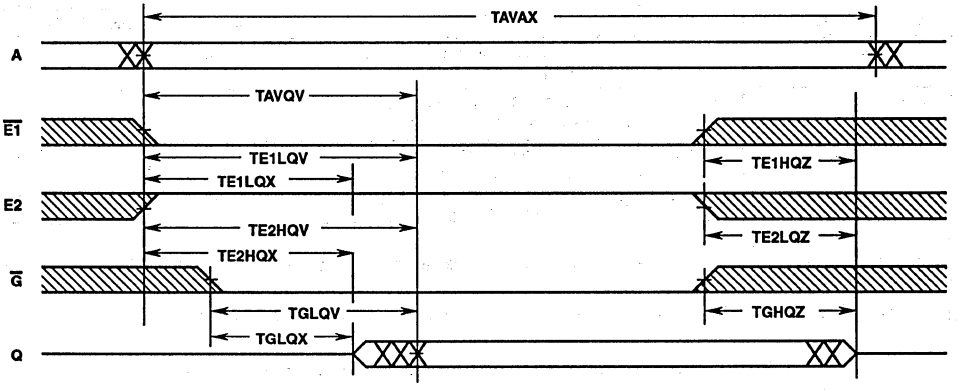
CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9
Interim Tests I and II		100%/5004	1, 7, 9, Δ	N/A
PDA I and II		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A
	Others	Samples/5005	1, 7	N/A
Group C (Optional)		Samples/5005	N/A	1, 7
Group D (Optional)		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7, 9	1, 7, 9

Timing Waveforms

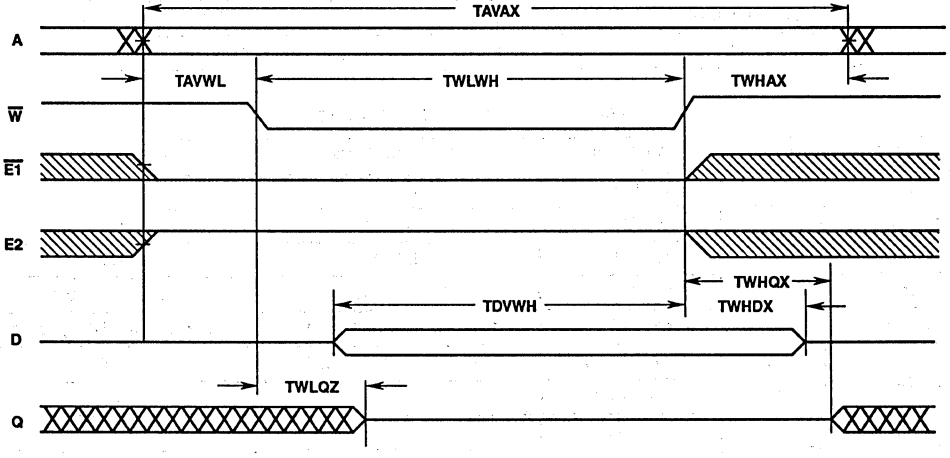
READ CYCLE I: $\overline{W}$, E2 HIGH; $\overline{G}$, $\overline{E1}$ LOW



READ CYCLE II: $\overline{W}$ HIGH

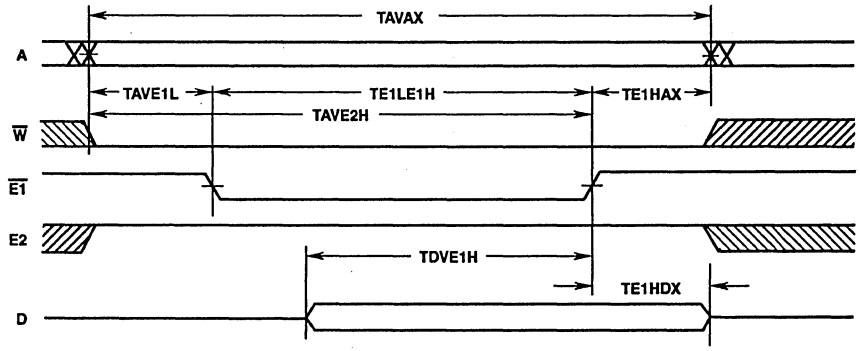


WRITE CYCLE I: LATE WRITE

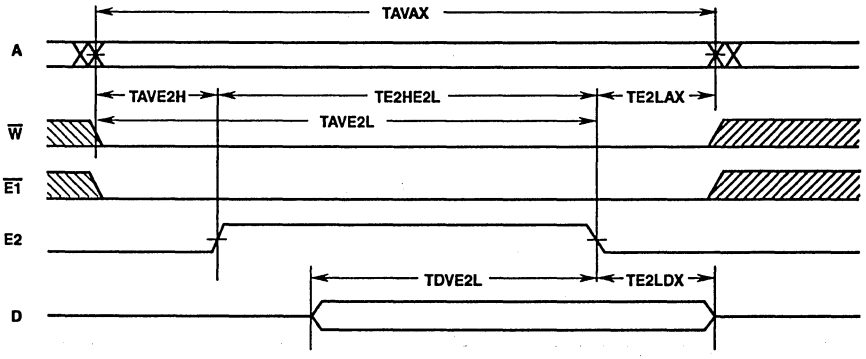


Timing Waveforms (Continued)

WRITE CYCLE II: EARLY WRITE - CONTROLLED BY $\overline{E1}$

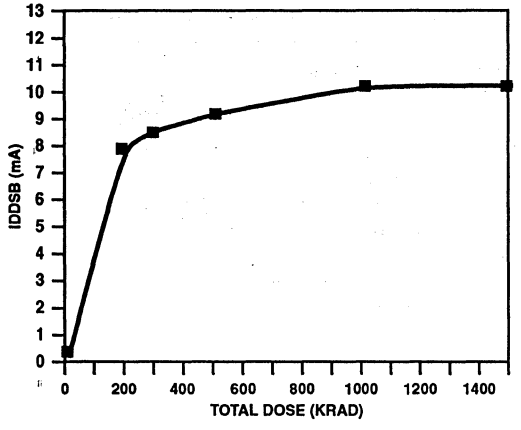


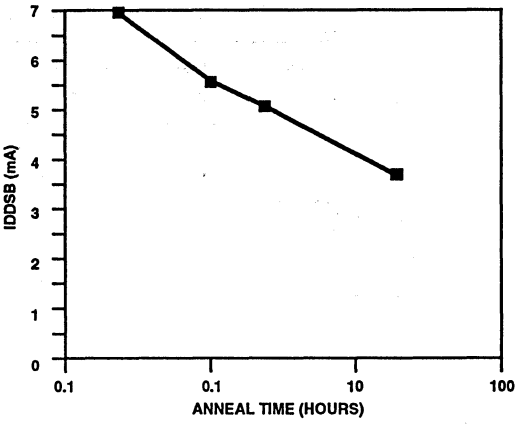
WRITE CYCLE III: EARLY WRITE - CONTROLLED BY E2

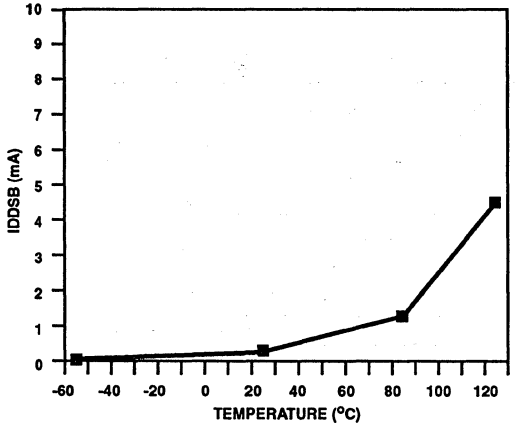


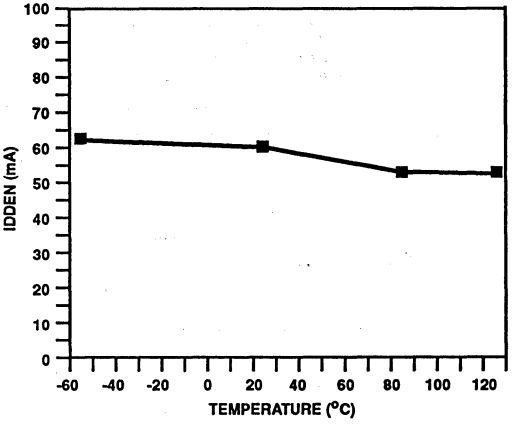
Performance Curves

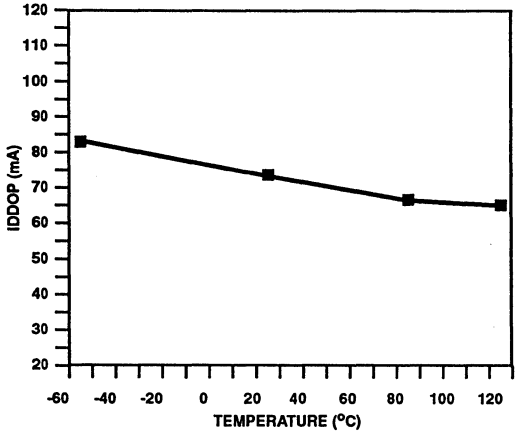
HS-65647RH TYPICAL PERFORMANCE CHARACTERISTICS
T_A = +25°C, Unless Otherwise Specified

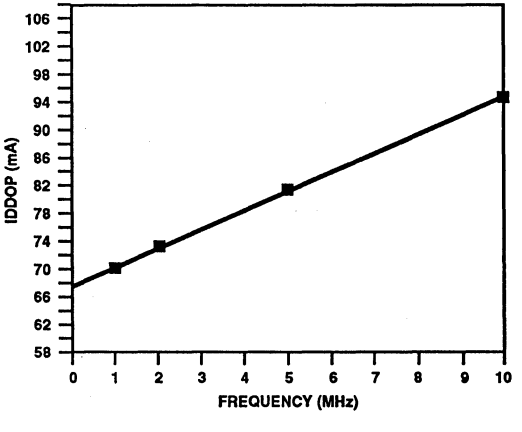






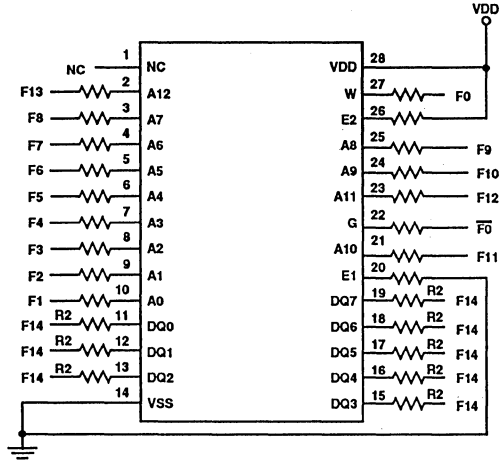






Burn-In Circuits

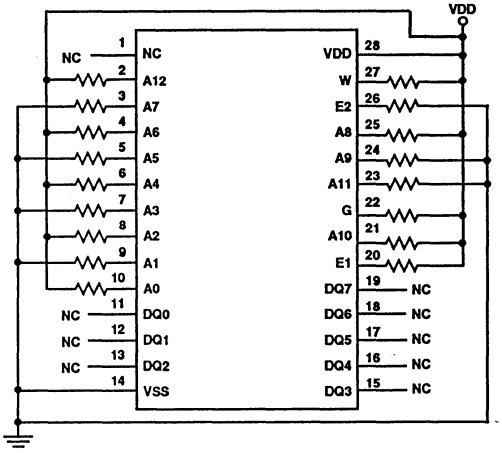
HS-65647RH 28 PIN FLATPACK AND CERAMIC DIP



DYNAMIC CONFIGURATION

NOTES:
VDD = 5.5V Min
R = 10kΩ ± 10%, except R2 = 47kΩ ± 10%
VIH: VDD ± 0.5V, VIL: 0.4V ± 0.4V
F0 = 100kHz ± 10%, 50% Duty Cycle
F1 = F0/2; F2 = F1/2; F3 = F2/2; . . . F14 = F13/2
$\overline{F0}$ = inverted F0

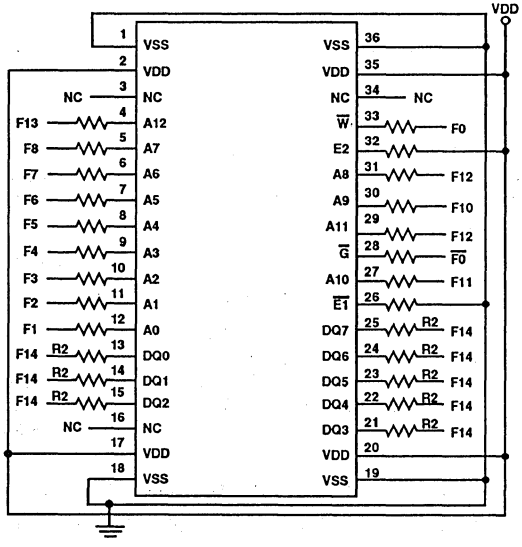
HS-65647RH 28 PIN FLATPACK AND CERAMIC DIP



STATIC CONFIGURATION

NOTES:
VDD = 5.5V Min
R = 10kΩ ± 10%

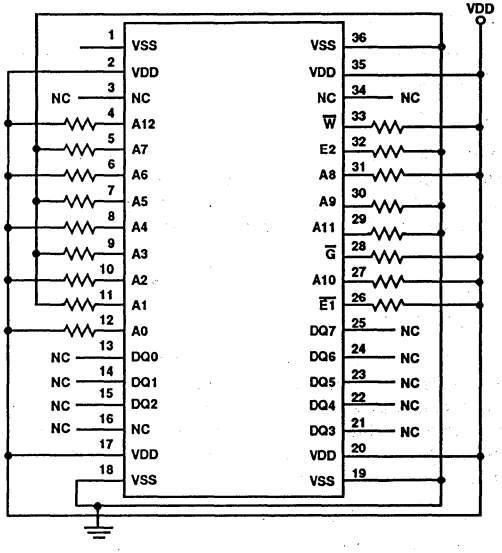
HS-65647RH 36 PIN FLATPACK



DYNAMIC CONFIGURATION

NOTES:
VDD = 5.5V Min
R = 10kΩ ± 10%, except R2 = 4.7kΩ ± 10%
VIH: VDD ± 0.5V, VIL: 0.4V ± 0.4V
F0 = 100kHz ± 10%, 50% Duty Cycle
F1 = F0/2; F2 = F1/2; F3 = F2/2; . . . F14 = F13/2
$\overline{F0}$ = Inverted F0

HS-65647RH 36 PIN FLATPACK



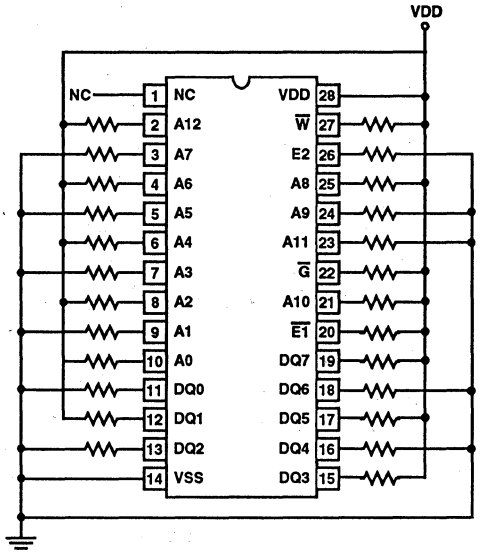
STATIC CONFIGURATION

NOTES:
VDD = 5.5V Min
R = 10kΩ ± 10%

8 MEMORIES

Irradiation Circuit

HS-65647RH (8K x 8 TSOS4 SRAM) 28 PIN CERAMIC DIP



NOTES:

1. VDD = 5.5V ± 0.5V
   R = 10kΩ ± 10%
2. All group E testing is performed in Ceramic DIP.
3. Group E sample size is two die/wafer.

Test Patterns

MARCH (II)PATTERN

After a background of zeros is written, each cell (from beginning to end in sequence) is read, written to a one and reread. When the array is full of ones each cell (from the end to the beginning) is read, restored to a zero and reread.

After this the pattern is repeated but with complemented data.

MASEST PATTERN (Multiple Address Select Pattern)

A checkerboard pattern is written into the memory. Then the first cell is read, then its binary address complement is read. The second cell is read and then its binary address complement is read. This pattern of incrementing the address and then reading its binary address complement is repeated until the entire memory is read.

This is then repeated but using a checkerboard bar pattern.

GALROW PATTERN (Row Galloping Pattern)

After a background of zeros is written into the memory a one is written into the first cell. It is then read alternately with each other cell in the row. The test cell is then rewritten back to a zero. The test cell is then incremented and the sequence is repeated until all cells in the memory have been used as a test cell.

This is pattern then repeated but using complemented data.

GALCOL PATTERN (Column Galloping Pattern)

After a background of zeros is written into the memory a one is written into the first cell. It is then read alternately with each other cell in the column. The test cell is then rewritten back to a zero. The test cell is then incremented and the sequence is repeated until all cells in the memory have been used as a test cell.

This is pattern then repeated but using complemented data.

CHECKERBOARD PATTERN and CHECKERBOARD BAR

A checkerboard is written (101010) into the memory and then the pattern is read back. This is then repeated but using complemented data.

Harris - Q Product Flow

SEM - Traceable to Diffusion Method 2018
Wafer Lot Acceptance Method 5007
Internal Visual Inspection (Note 1)
Gamma Radiation Assurance Tests Method 1019
100% Nondestructive Bond Pull Method 2023
Customer Pre-Cap Visual Inspection (Notes 1, 2)
Temperature Cycling Method 1010 Condition C
Constant Acceleration Method 2001 Y1 30KG
Particle Impact Noise Detection Method 2020, (Condition A 20G)
Marking and Serialization
Initial Electrical Tests (T0)
Static Burn-In 72 Hour, +125°C Method 1015 Condition A
Room Temperature Electrical Tests (T1)
Burn-In Delta Calculation (T0-T1)
PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ
Dynamic Burn-In 240 Hours, +125°C Method 1015 Condition D
Electrical Tests Subgroups 1, 7, 9 (T2) Method 5004
Burn-In Delta Calculations (T0 - T2)
PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ Method 5004
Electrical Test +125°C, +85°C, -55°C Method 5004
Group A Inspection Method 5005
X-Ray Inspection Method 2012
Fine and Gross Leak Tests Method 1014
Customer Source Inspection (Note 2)
Group B Inspection (Notes 2, 4) Method 5005 (Optional)
Group D Inspection (Notes 2, 4) Method 5005 (Optional)
External Visual Inspection Method 2009
Data Package Generation (Note 3)

NOTES:

1. Visual Inspection is performed to MIL-STD-883 Method 2010, Condition A, with the following modification for SOS technology devices: Semicircular cracks not in an active area which start and end at the die edge are acceptable.
2. These steps are optional, and should be listed on the purchase order if required.
3. Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A) -55°C, +25°C, +85°C, +125°C
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (includes SEM report)
   X-Ray Report and Film
   Test Variables Data, DC Test and TELQV
   +25°C Initial Test
   +25°C Interim Test 1
   +25°C Interim Test 2
   +25°C Delta Over Burn-In
4. Group B data package contains Attributes Data plus Variables Data, DC Test and TE2HQV. Group D data package contains Attributes only.

Harris -8 Product Flow

Internal Visual Inspection , Alternate Condition B (Note 1)
Gamma Radiation Assurance Tests Method 1019
Customer Pre-Cap Visual Inspection (Notes 1, 2)
Temperature Cycling Method 1010 Condition C (50 Cycles)
Constant Acceleration Method 2001 Y1 30KG
Fine and Gross Leak Tests Method 1014
Marking
Initial Electrical Tests (T0)
Dynamic Burn-In 160 Hours, +125°C Method 1015 or Equivalent Condition D
Electrical Tests Subgroups 1, 7, 9 (T1) Method 5004
PDA Calculation 5% Subgroups 1, 7 Method 5004
Electrical Test +125°C, +85°C, -55°C Method 5004
Group A Inspection Method 5005
Customer Source Inspection (Note 2)
Group B Inspection (Notes 2, 4) Method 5005 (Optional)
Group C Inspection (Notes 2, 4) Method 5005 (Optional)
Group D Inspection (Notes 2, 4) Method 5005 (Optional)
External Visual Inspection Method 2009
Data Package Generation (Note 3)

NOTES:

1. Visual Inspection is performed to MIL-STD-883 Method 2010, Alternate Condition B, with the following modification for SOS technology devices: Semicircular cracks not in an active area which start and end at the die edge are acceptable.
2. These steps are optional, and should be listed on the purchase order if required.
3. Data package contains:
   Test Attributes (includes Group A) -55°C, +25°C, +85°C, +125°C
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
4. Group B, C and D data package contains Attributes Data only.

Metallization Topology

DIE DIMENSIONS:
313 x 291 x 21 ±1mils

METALLIZATION:
Type: Al/Si/Cu
Metal 1 Thickness: 7500Å ± 2kÅ
Metal 2 Thickness: 10kÅ ± 2kÅ

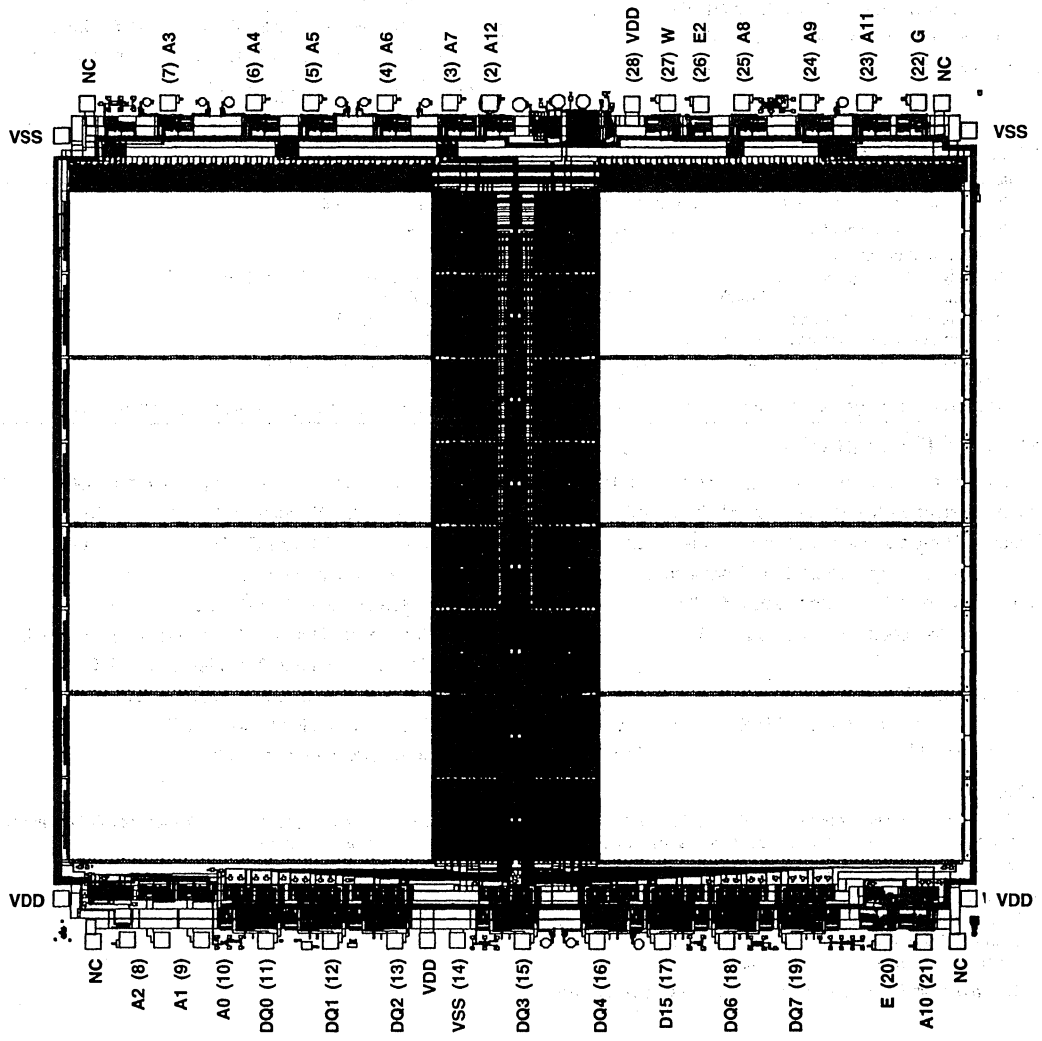
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Silver Glass

WORST CASE CURRENT DENSITY:
1.5×10^5 Amps/cm^2

Metallization Mask Layout

HS-65647RH



HARRIS SEMICONDUCTOR

HS-65643RH

Radiation Hardened 64K x 1 SOS CMOS Static RAM

December 1992

Features

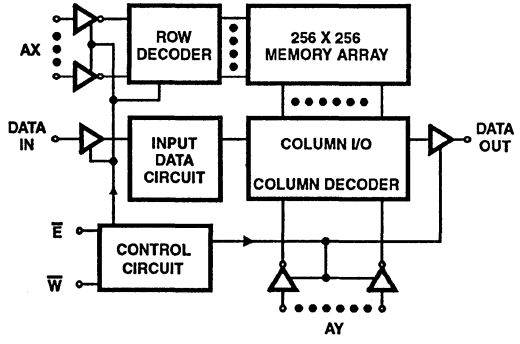
- 1.2 Micron Radiation Hardened SOS CMOS
  - Total Dose 3 x 10^5 RAD (Si)
  - Transient Upset >1 x 10^{11} RAD (Si)/s
  - Single Event Upset < 1 x 10^{-12} Errors/Bit-Day
- Latch-up Free
- LET Threshold >250 MeV/mg/cm2
- Low Standby Supply Current 10mA (Max)
- Low Operating Supply Current 35mA (Max)
- Fast Access Time 50ns (Max), 35ns (Typ)
- High Output Drive Capability ±8mA
- Gated Input Buffers
- Six Transistor Memory Cell
- Fully Static Design
- Asynchronous Operation
- CMOS Inputs
- 5V Single Power Supply
- Military Temperature Range -55°C to +125°C

Description

The Harris HS-65643RH is a fully asynchronous 64K x 1 radiation hardened static RAM. This RAM is fabricated using the Harris 1.2 micron silicon-on-sapphire CMOS technology. This technology gives exceptional hardness to all types of radiation, including neutron fluence, total ionizing dose, high intensity ionizing dose rates, and cosmic rays.

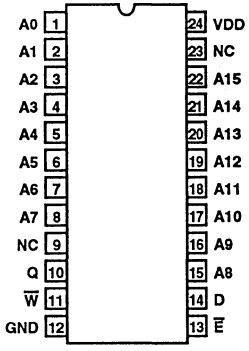
Low power operation is provided by a fully static design. Low standby power can be achieved without pull-up resistors, due to the gated input buffer design.

Functional Diagram

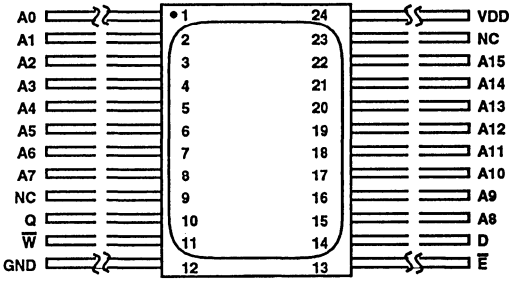


Pinouts

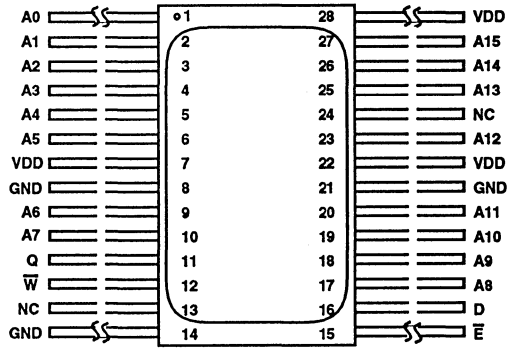
HS1-65643RH 24 PIN CERAMIC DIP
CASE OUTLINE D3, CONFIGURATION 3
TOP VIEW



HS9-65643RH 24 PIN FLATPACK
CASE OUTLINE F6A, CONFIGURATION 2
TOP VIEW



HS9A-65643RH 28 PIN FLATPACK
CASE OUTLINE F11A, CONFIGURATION 2
TOP VIEW



8 MEMORIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2794.2**

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage ..... GND-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 3mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	25°C/W	8.0°C/W
Braze Seal Flatpack Package	64°C/W	8.8°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package 2.0W
Braze Seal Flatpack Package 781mW
Gate Count ..... 101,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range (VDD) ..... +4.5V to +5.5V
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0V to +0.2VDD
Input High Voltage (VIH) ..... 0.8VDD to VDD
Data Retention Supply Voltage 2.0V
Input Rise and Fall Time ..... 40ns Max.

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VDD = 4.5V, IO = -8.0mA VI = VDD or GND	1, 2, 3	-55°C, +25°C, +85°C, +125°C	2.4	-	V
	VOH2	VDD = 4.5V, IO = -100µA VI = VDD or GND	1, 2, 3	-55°C, +25°C, +85°C, +125°C	VDD-0.4	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, IO = 8.0mA VI = VDD or GND	1, 2, 3	-55°C, +25°C, +85°C, +125°C	-	0.4	V
High Impedance Output Leakage Current	IOZL or IOZH	VDD = 5.5V, VO = GND or VDD, VI = VDD or GND $\overline{E}$ = VDD	1, 3	-55°C, +25°C	-10	10	µA
			2	+85°C	-30	30	µA
			2	+125°C	-60	60	µA
Input Leakage Current	IIH or IIL	VDD = 5.5V, VI = VDD or GND	1, 2, 3	-55°C, +25°C, +85°C, +125°C	-1.0	1.0	µA
Standby Supply Current	IDDSB	VDD = 5.5V, IO = 0mA, VI = VDD or GND $\overline{E}$ = VDD	1, 3	-55°C, +25°C	-	500	µA
			2	+85°C	-	4	mA
			2	+125°C	-	10	mA
Enable Supply Current	IDDEN	VDD = 5.5V, IO = 0mA, VI = VDD or GND $\overline{E}$ = 0.0V	1, 2, 3	-55°C, +25°C, +85°C, +125°C	-	30	mA
Operating Supply Current (Note 2)	IDDOP	VDD = 5.5V, IO = 0mA, VI = VDD or GND $\overline{E}$ = 0.0V, f = 1MHz	1, 2, 3	-55°C, +25°C, +85°C, +125°C	-	35	mA
Data Retention Supply Current	IDDDR	VDD = 2.0V, IO = 0mA, VI = VDD or GND $\overline{E}$ = VDD	1, 3	-55°C, +25°C	-	50	µA
			2	+85°C	-	1	mA
			2	+125°C	-	4	mA
Functional Tests	FT	VDD = 4.5V and 5.5V VI = VDD or GND, f = 1MHz	7, 8A, 8B	-55°C, +25°C, +85°C, +125°C	-	-	-
Noise Immunity Functional Test	FN	VDD = 4.5, VIL = 0.2 VDD VIH = 0.8 VDD, f = 1MHz	7, 8A, 8B	-55°C, +25°C, +85°C, +125°C	-	-	-

NOTE:

1. All voltages referenced to device GND.
2. Typical IDDOP derating = 3mA/MHz (3mA increase in IDDOP per 1MHz increase in address frequency.)

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Access Time	TAVQV	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	-	50	ns
Chip Enable Access Time	TELQV	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	-	50	ns
Write Recovery Time	TWHAX	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	0	-	ns
Address Hold Time	TEHAX	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	0	-	ns
Chip Enable to End-of-Write	TELWH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	30	-	ns
Address Valid to End-of-Write	TAVEH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	35	-	ns
Chip Enable Pulse Width	TELEH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	30	-	ns
Address Setup Time	TAVWL	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	10	-	ns
	TAVEL	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	5	-	ns
Write to End-of-Write	TWLEH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	30	-	ns
Write Enable Pulse Width	TWLWH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	25	-	ns
Data Setup Time	TDVWH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	30	-	ns
	TDVEH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	30	-	ns
Address Valid to End-of-Write	TAVWH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	30	-	ns
Data Hold Time	TWHDX	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	0	-	ns
	TEHDX	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	0	-	ns

NOTES:

1. AC measurements tested at worst case VDD. Guaranteed over full operating range.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V to VDD; timing reference levels = 2.0V; output load = 1 TTL equivalent load and CL ≥ 50pF, for CL > 50pF, access times are derated 0.15ns/pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz	1, 2, 4	T_A = +25°C	-	12	pF
		VDD = Open, f = 1MHz	1, 2, 4	T_A = +25°C	-	12	pF
I/O Capacitance	COUT	VDD = Open, f = 1MHz	1, 2, 4	T_A = +25°C	-	12	pF
		VDD = Open, f = 1MHz	1, 2, 4	T_A = +25°C	-	12	pF
Write Enable to Output in High Z	TWLQZ	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	-	15	ns
Write Enable High to Output ON	TWHQX	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	0	-	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable to Output ON	TELQX	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	0	-	ns
Chip Enable to Output High Z	TEHQZ	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	-	15	ns
Read/Write/Cycle Time	TAVAX	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	50	-	ns
Output Hold from Address Change	TAXQX	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	0	-	ns

NOTES:

1. The parameters listed are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. Applies to DIP device types only.
3. Applies to Flatpack device types only.
4. All measurements referenced to device GND.

TABLE 4. POST 300K RAD DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Standby Supply Current	IDDSB	VDD = 5.5V, IO = 0mA, $\overline{E}$ = VDD, VI = VDD or GND	+25°C	-	10	mA
Enabled Supply Current	IDDEN	VDD = 5.5V, IO = 0mA, $\overline{E}$ = 0.0V, VI = VDD or GND	+25°C	-	30	mA
Operating Supply Current (Note 2)	IDDOP	VDD = 5.5V, IO = 0mA, f = 1MHz, $\overline{E}$ = 0.0V,VI = VDD or GND	+25°C	-	35	mA
Data Retention Supply Current	IDDDR	VDD = 2.0V, IO = 0mA, $\overline{E}$ = VDD	+25°C	-	6	mA

NOTES:

1. DC parameters not listed in this table are tested at the +25°C pre-irradiation test limits. All AC parameters are tested at the +25°C pre-irradiation test limits.
2. Typical IDDOP derating = 3mA/MHz (3mA increase in IDDOP per 1MHz increase in address frequency.)

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C) GROUP B, SUBGROUP 5

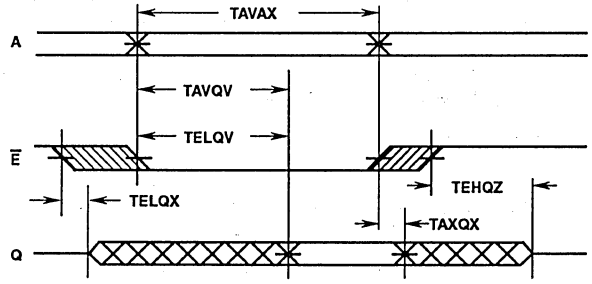
PARAMETER	SYMBOL	DELTA LIMITS
Standby Supply Current	IDDSB	±150µA
High Impedance Output Leakage Current	IOZH	± 2µA
	IOZL	±2µA
Input Leakage Current	IIH	± 150nA
	IIL	±150nA
Low Level Output Voltage	VOL	± 60mV
Output High Voltage	VOH1	± 400mV

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9
Interim Test I and II		100%/5004	1, 7, 9, Δ	N/A
PDA I and II		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A
	Others	Samples/5005	1, 7	N/A
Group C (Optional)		Samples/5005	N/A	1, 7, 9
Group D (Optional)		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7, 9	1, 7, 9

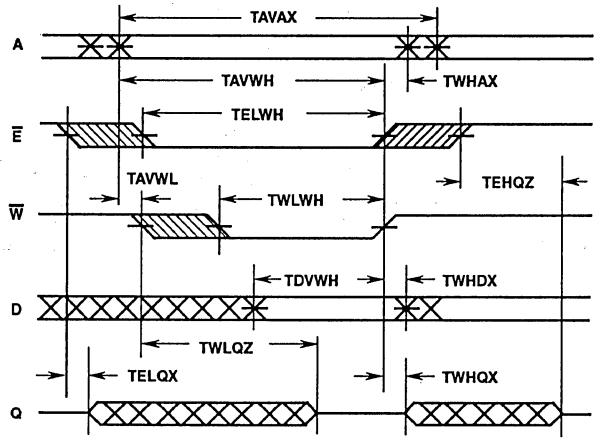
Timing Waveforms

READ CYCLE



NOTE: $\overline{W}$ is high for the entire cycle and D is ignored. $\overline{E}$ is stable prior to A becoming valid and after A becomes invalid.

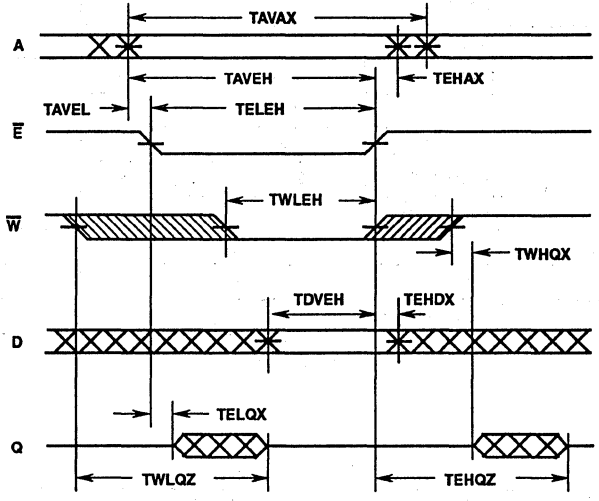
WRITE CYCLE I: CONTROLLED BY $\overline{W}$ (LATE WRITE)



NOTE: In this mode, $\overline{E}$ rises after $\overline{W}$. The address must remain stable whenever both $\overline{E}$ and $\overline{W}$ are low.

Timing Waveforms (Continued)

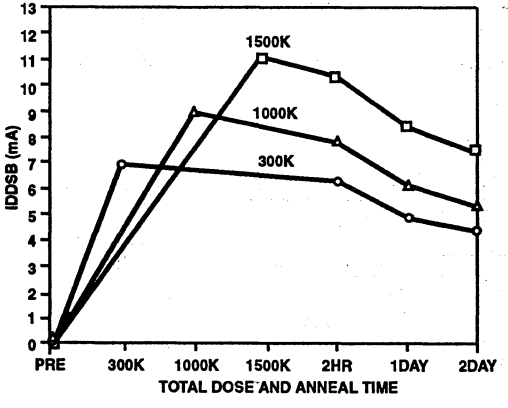
WRITE CYCLE II: EARLY WRITE - CONTROLLED BY $\overline{E}$ (EARLY WRITE)

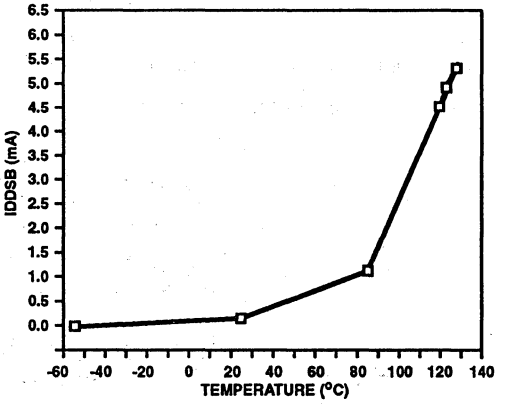


NOTE: In this mode, $\overline{W}$ rises after $\overline{E}$ is high. If $\overline{W}$ falls before $\overline{E}$ by a time exceeding TWLQZ and rises after $\overline{E}$ by a time exceeding TEHQZ then the output will remain in the high impedance state throughout the write cycle.

Performance Curves

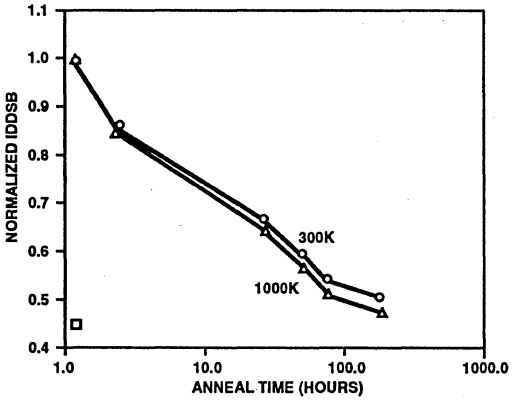
HS-65643RH TYPICAL PERFORMANCE CHARACTERISTICS
T_A = +25°C, Unless Otherwise Specified

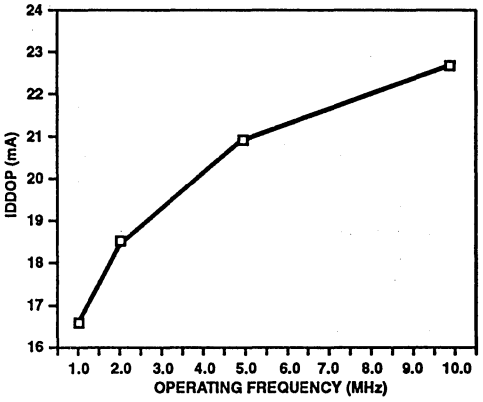


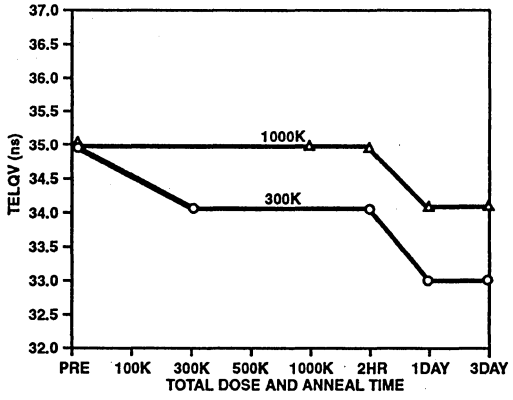


Performance Curves (Continued)

HS-65643RH TYPICAL PERFORMANCE CHARACTERISTICS
T_A = +25°C, Unless Otherwise Specified



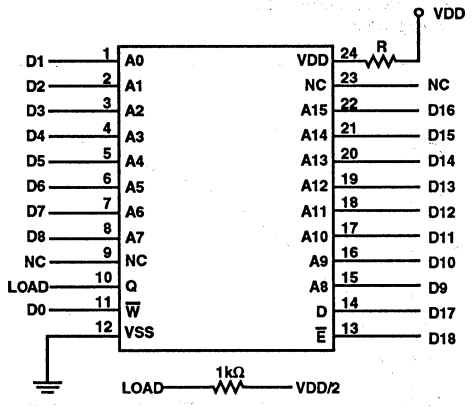




8 MEMORIES

Burn-In Circuits

HS-65643RH 24 PIN FLATPACK AND CERAMIC DIP

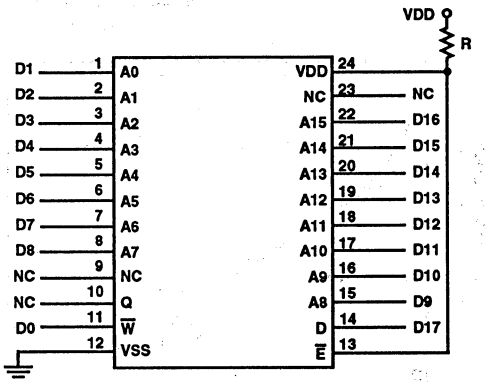


DYNAMIC CONFIGURATION

NOTES:

VDD = 5.5V Min
R = 10Ω ± 10%
D0 - D18 are signals from the driver EPROM
F = 100kHz

HS-65643RH 24 PIN FLATPACK AND CERAMIC DIP

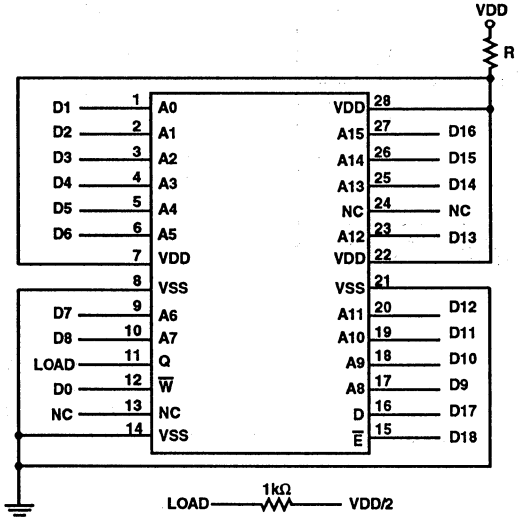


STATIC CONFIGURATION

NOTES:

VDD = 5.5V Min
R = 10Ω ± 10%
Static 1 Checkerboard patterns are loaded into the memory for static burn-in. After the pattern is written, $\overline{E}$ is raised to VDD and a random address selected with inputs at either VDD or VSS
Static 2 Repeat above except with inverse pattern.

HS-65643RH 28 PIN FLATPACK

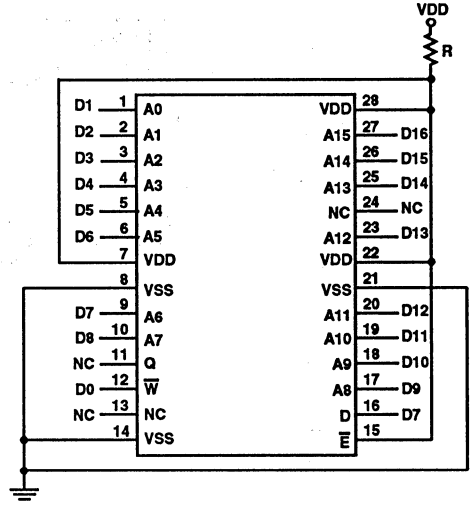


DYNAMIC CONFIGURATION

NOTES:

VDD = 5.5V Min
R = 10Ω ± 10%
D0 - D18 are signals from the driver EPROM
F = 100kHz

HS-65643RH 28 PIN FLATPACK



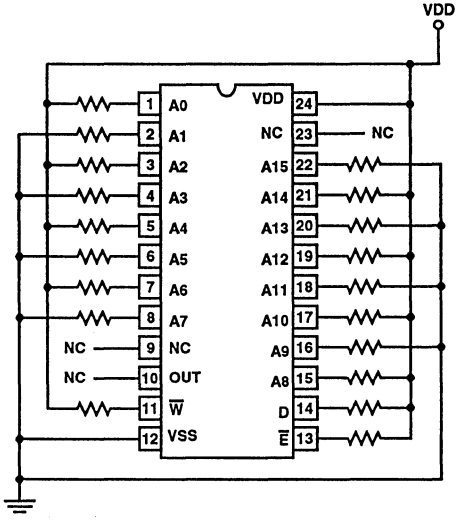
STATIC CONFIGURATION

NOTES:

VDD = 5.5V Min
R = 10Ω ± 10%
Static 1 Checkerboard patterns are loaded into the memory for static burn-in. After the pattern is written, $\overline{E}$ is raised to VDD and a random address selected with inputs at either VDD or VSS
Static 2 Repeat above except with inverse pattern.

Irradiation Circuit

HS-65643RH (64K x 1 TSOS4 SRAM) 24 PIN CERAMIC DIP



NOTES:

1. VDD = 5.5V ± 0.5V
   R = 10kΩ ± 10%
2. All group E testing is performed in Ceramic DIP.
3. Group E sample size is two die/wafer.

Test Patterns

MARCH (II)PATTERN

After a background of zeros is written, each cell (from beginning to end in sequence) is read, written to a one and reread. When the array is full of ones each cell (from the end to the beginning) is read, restored to a zero and reread.

After this the pattern is repeated but with complemented data.

MASEST PATTERN (Multiple Address Select Pattern)

A checkerboard pattern is written into the memory. Then the first cell is read, then its binary address complement is read. The second cell is read and then its binary address complement is read. This pattern of incrementing the address and then reading its binary address complement is repeated until the entire memory is read.

This is then repeated but using a checkerboard bar pattern.

GALROW PATTERN (Row Galloping Pattern)

After a background of zeros is written into the memory a one is written into the first cell. It is then read alternately with each other cell in the row. The test cell is then rewritten back to a zero. The test cell is then incremented and the sequence is repeated until all cells in the memory have been used as a test cell.

This is pattern then repeated but using complemented data.

GALCOL PATTERN (Column Galloping Pattern)

After a background of zeros is written into the memory a one is written into the first cell. It is then read alternately with each other cell in the column. The test cell is then rewritten back to a zero. The test cell is then incremented and the sequence is repeated until all cells in the memory have been used as a test cell.

This is pattern then repeated but using complemented data.

CHECKERBOARD PATTERN and CHECKERBOARD BAR

A checkerboard is written (101010) into the memory and then the pattern is read back. This is then repeated but using complemented data.

Harris - Space Level (-Q) Product Flow

SEM - Traceable to Diffusion Method 2018
Wafer Lot Acceptance Method 5007
Internal Visual Inspection (Note 1)
Gamma Radiation Assurance Tests Method 1019
100% Nondestructive Bond Pull Method 2023
Customer Pre-Cap Visual Inspection (Notes 1, 2)
Temperature Cycling Method 1010 Condition C
Constant Acceleration Method 2001 Y1 30KG
Particle Impact Noise Detection
Marking and Serialization
Initial Electrical Tests (T0)
Static Burn-In 1.36 Hour, +125°C Method 1015 or Equivalent Condition A
Static Burn-In 2.36 Hour, +125°C Method 1015 or Equivalent Condition B
Room Temperature Electrical Tests (T1)
Burn-In Delta Calculation (T0-T1)
PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ Method 1015
Dynamic Burn-In 240 Hours, +125°C Method 1015 or Equivalent Condition D
Electrical Tests Subgroups 1, 7, 9 (T2) Method 5004
Burn-In Delta Calculation (T0 - T2)
PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ Method 5004
Electrical Test +125°C, +85°C, -55°C Method 5004
Group A Inspection Method 5005
X-Ray Inspection Method 2012
Fine and Gross Leak Tests Method 1014
Customer Source Inspection (Note 2)
Group B Inspection (Notes 2, 4) Method 5005 (Optional)
Group D Inspection (Notes 2, 4) Method 5005 (Optional)
External Visual Inspection Method 2009
Data Package Generation (Note 3)

NOTES:

1. Visual Inspection is performed to MIL-STD-883 Method 2010, Condition A, with the following modification for SOS technology devices: Semicircular cracks not in an active area which start and end at the die edge are acceptable.
2. These steps are optional, and should be listed on the purchase order if required.
3. Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A) -55°C, +25°C, +85°C, +125°C
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (includes SEM report)
   X-Ray Report and Film
   Test Variables Data, DC Test and TELQV
   +25°C Initial Test
   +25°C Interim Test 1
   +25°C Interim Test 2
   +25°C Delta Over Burn-In
4. Group B data package contains Attributes Data plus Variables Data, DC Test and TELQV. Group D data package contains Attributes only.

Harris -8 Product Flow

Internal Visual Inspection , Alternate Condition B (Note 1)
Gamma Radiation Assurance Tests Method 1019
Customer Pre-Cap Visual Inspection (Notes 1, 2)
Temperature Cycling Method 1010 Condition C (50 Cycles)
Constant Acceleration Method 2001 Y1 30KG
Fine and Gross Leak Tests Method 1014
Marking
Initial Electrical Tests (T0)
Dynamic Burn-In 160 Hours, +125°C Method 1015 or Equivalent Condition D
Electrical Tests Subgroups 1, 7, 9 (T1) Method 5004
PDA Calculation 5% Subgroups 1, 7 Method 5004
Electrical Test +125°C, +85°C, -55°C Method 5004
Group A Inspection Method 5005
Customer Source Inspection (Note 2)
Group B Inspection (Notes 2, 4) Method 5005 (Optional)
Group C Inspection (Notes 2, 4) Method 5005 (Optional)
Group D Inspection (Notes 2, 4) Method 5005 (Optional)
External Visual Inspection Method 2009
Data Package Generation (Note 3)

NOTES:

1. Visual Inspection is performed to MIL-STD-883 Method 2010, Alternate Condition B, with the following modification for SOS technology devices: Semicircular cracks not in an active area which start and end at the die edge are acceptable.
2. These steps are optional, and should be listed on the purchase order if required.
3. Data package contains:
   Test Attributes (includes Group A) -55°C, +25°C, +85°C, +125°C
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
4. Group B, C and D data package contains Attributes Data only.

Metallization Topology

DIE DIMENSIONS:
297 x 310 x 21 ±1mils

METALLIZATION:
Type: Al/Si/Cu
Metal 1 Thickness: 7500Å ± 2kÅ
Metal 2 Thickness: 10kÅ ± 2kÅ

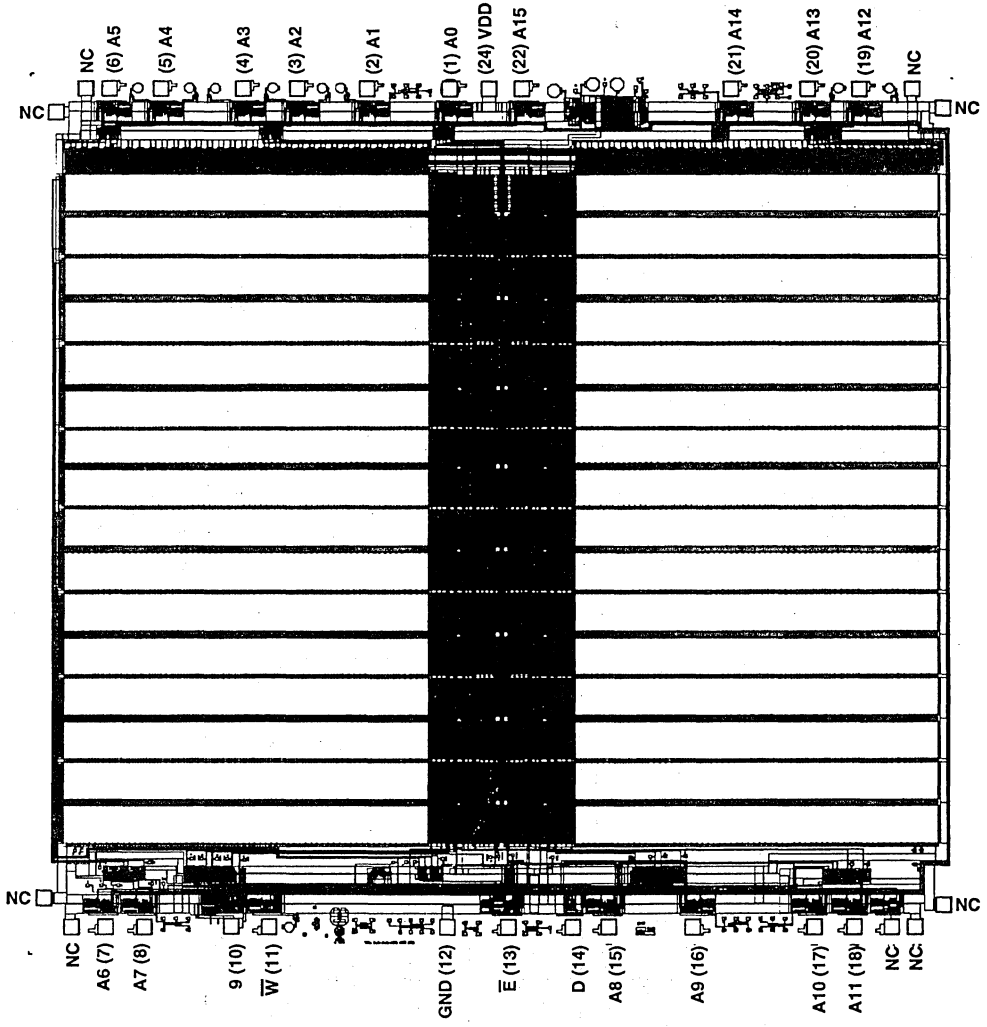
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Silver Glass

WORST CASE CURRENT DENSITY:
1.5×10^5 Amps/cm^2

Metallization Mask Layout

HS-65643RH



HARRIS SEMICONDUCTOR

HS-6564RH

Radiation Hardened 8K x 8, 16K x 4 CMOS RAM Module

December 1992

Features

- Radiation Hardened EPI CMOS
  - Total Dose 1 x 10^5 RAD (Si)
  - Transient Upset > 1 x 10^8 RAD (Si)/s
  - Latch-Up Free to > 1 x 10^{12} RAD (Si)/s
- Low Power Standby 4.4mW Maximum
- Low Power Operation 308mW/MHz Maximum
- Data Retention 3.0V Minimum
- TTL Compatible In/Out
- Three State Outputs
- Fast Access Time 250ns Maximum
- Military Temperature Range -55°C to +125°C
- On Chip Address Registers
- Organizable 8K x 8 or 16K x 4
- 40 Pin DIP Pinout 2.000" x 0.900"

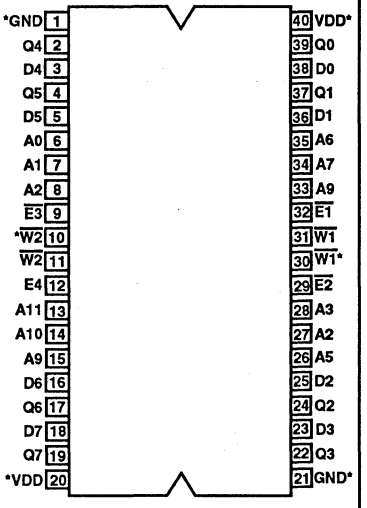
Description

The HS-6564RH is a radiation hardened 64K bit, synchronous CMOS RAM module. It consists of 16 HS-6504RH 4K x 1 radiation hardened CMOS RAMs, in leadless carriers, mounted on a ceramic substrate. The individual RAMs are fabricated using the Harris radiation hardened guard ring, self-aligned silicon gate technology. The HS-6564RH is configured as an extra wide, standard length 40 pin DIP. The memory appears to the system as an array of 16 4K x 1 static RAMs. The array is organized as two 8K by 4 blocks of RAM sharing only the address bus. The data inputs, data outputs, chip enables and write enables are seperate for each block of RAM. This allows the user to organize the HS-6564RH RAM as either an 8K by 8 or a 16K by 4 array.

This 64K memory provides a unique blend of low power CMOS semiconductor technology and advanced packaging techniques. The HS-6564RH is intended for use in radiation environments where a large amount of RAM is needed, and where power consumption and board space are prime concerns. On-chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance for use in expanded memory arrays. The guaranteed low voltage data retention characteristics allow easy implementation of non-volatile readswrite memory by using very small batteries mounted directly on the memory circuit board.

Pinout

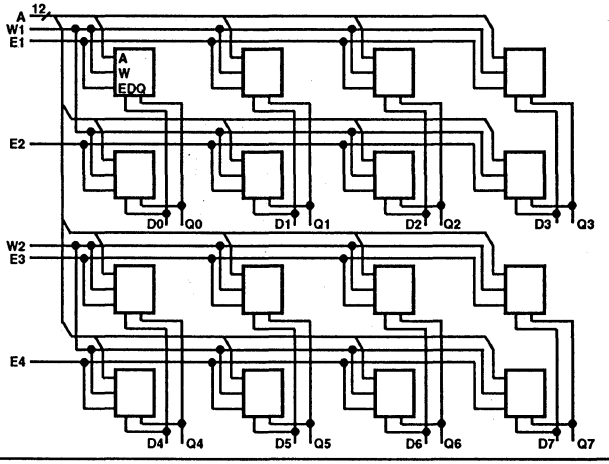
HS5-6564RH 40 PIN CERAMIC MODULE
INTERNAL PACKAGE CODE "HSQ"
TOP VIEW



* Pins 20 and 40 (VDD) are internally connected. Similarly pins 1 and 21 (Ground) are connected. The user is advised to connect both VDD pins and both Ground pins to the board busses. This will improve power distribution across the array and will enhance decoupling.

Pin 10 is internally connected to pin 11, and pin 30 is connected to pin 31. For those users wishing to preserve board compatibility with possible future RAM arrays, we recommend connections to the write lines be made at pins 11 and 31, leaving pins 10 and 30 free for future expansion.

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3032

Absolute Maximum Ratings

Supply Voltage ..... -3.0V to +7.0V
Input or Output Voltage Applied ..... GND-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 48mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
40 Pin Ceramic Module Package	TBD	TBD

Maximum Package Power Dissipation at +125°C
40 Pin Ceramic Module Package ..... TBD
Gate Count ..... 53,336 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Standby Supply Current	IDDSB	IO = 0, VI = GND or VDD	-	1600	µA
Operating Supply Current (8K x 8) (Note 1)	IDDOP1	f = 1MHz, IO = 0 VI = VDD or GND	-	56	mA
Operating Supply Current (16K x 4) (Note 1)	IDDOP2	f = 1MHz, IO = 0 VI = VDD or GND	-	28	mA
Data Retention Supply Current	IDDDR	IO = 0, VDD = 3.0 VI = VDD or GND	-	1200	µA
Data Retention Supply Current	VDDDR		3.0	-	V
Address Input Leakage	IIA	GND ≤ VI ≤ VDD	-20	+20	µA
Data Input Leakage (8K x 8)	IID1	GND ≤ VI ≤ VDD	-3	+3	µA
Data Input Leakage (16K x 4)	IID2	GND ≤ VI ≤ VDD	-5	+5	µA
Enable Input Leakage (8K x 8)	IIE1	GND ≤ VI ≤ VDD	-10	+10	µA
Enable Input Leakage (16K x 4)	IIE2	GND ≤ VI ≤ VDD	-5	+5	µA
Write Enable Input Leakage (Each)	IIW	GND ≤ VI ≤ VDD	-10	+10	µA
Output Leakage (8K x 8)	IOZ1	GND ≤ VO ≤ VDD	-20	+20	µA
Output Leakage (16K x 4)	IOZ2	GND ≤ VO ≤ VDD	-40	+40	µA
Input Low Voltage	VIL		-	0.8	V
Input High Level (Except $\overline{E}$ and $\overline{W}$)	VIH1		VDD -1.5	-	V
Input High Level ($\overline{E}$ and $\overline{W}$)	VIH2		VDD -1.0	-	V
Output Low Voltage	VOL	IOL = 2.0mA	-	0.4	V
Output High Voltage	VOH	IOH = -1.0mA	2.4	-	V

NOTES:
1. Operating supply current is proportional to operating frequency. IDDOP is specified at an operating frequency of 1MHz indicating repetitive accessing at a 1µs rate. Operating at slower rates will decrease IDDOP proportionally.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Chip Enable Access Time	TELQV	Note 1	-	350	ns
Address Access Time (TAVQV = TELQV + TAVEL)	TAVQV	Note 1	-	400	ns
Chip Enable Low	TELEH	Note 1	350	-	ns
Chip Enable High	TEHEL	Note 1	130	-	ns
Address Setup Time	TAVEL	Note 1	50	-	ns
Address Hold Time	TELAX	Note 1	50	-	ns
Write Enable Low	TWLWH	Note 1	150	-	ns
Write Enable Setup Time	TWLEH	Note 1	250	-	ns
Early Write Setup Time	TWLEL	Note 1	10	-	ns
Early Write Hold Time	TELWX	Note 1	100	-	ns
Data Setup Time	TDVWL	Note 1	10	-	ns
Early Write Data Setup Time	TDVEL	Note 1	90	-	ns
Data Hold Time	TWLDX	Note 1	100	-	ns
Early Write Data Hold Time	TELDX	Note 1	100	-	ns
Early Write Pulse Hold Time	TELWH	Note 1	250	-	ns

NOTE:

1. Inputs TRISE = TFALL ≤ 20ns: Outputs : CLOAD = 50pF. All timing measurements at 1/2 VDD.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Guaranteed, but not tested)

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Address Input Capacitance	CIA	f = 1MHz, VI = VDD or GND	-	200	pF
Data Input Capacitance (8K x 8)	CID1	f = 1MHz, VI = VDD or GND	-	50	pF
Data Input Capacitance (16K x 4)	CID2	f = 1MHz, VI = VDD or GND	-	100	pF
Enable Input Capacitance (8K x 8)	CIE1	f = 1MHz, VI = VDD or GND	-	160	pF
Enable Input Capacitance (16K x 4)	CIE2	f = 1MHz, VI = VDD or GND	-	80	pF
Write Enable Input Capacitance (Each)	CIW	f = 1MHz, VI = VDD or GND	-	100	pF
Output Capacitance (8K x 8)	CO1	f = 1MHz, VO = VDD or GND	-	50	pF
Output Capacitance (16K x 4)	CO2	f = 1MHz, VO = VDD or GND	-	100	pF

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Guaranteed, but not tested) **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Output Enable Time	TELQX		-	75	ns
Output Disable Time	TEHQZ		-	75	ns
Data Valid to Write (Read-Modify-Write)	TQVWL		100	-	ns
Read or Write Cycle Time	TELEL		480	-	ns

NOTE:

1. Inputs: TRISE = TFALL ≤ 20ns. Outputs: CLOAD = 50pF. All timing measurements at 1/2 VDD.

TABLE 4. POST RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The post irradiation test conditions and limits are the same as those listed in Tables 1 and 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Output Low Voltage	VOL	± 0.08V
Output High Voltage	VOH	± 0.48V
Input Leakage Current	II	± 0.20µA

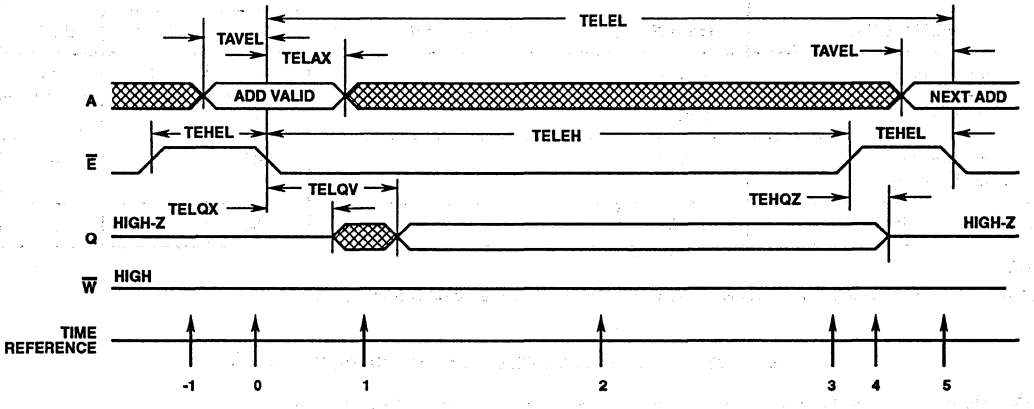
NOTE: Circuits are Burned-in as HS-6504RH discrete units, see HS-6504RH for appropriate burn-in delta information.

TABLE 6. APPLICABLE SUBGROUPS

NOTE: Quality Conformance Inspection (QCI) applies to the individual HS-6564RH devices, not to the assembled module. See HS-6504RH for further information.

Timing Waveforms

READ CYCLE



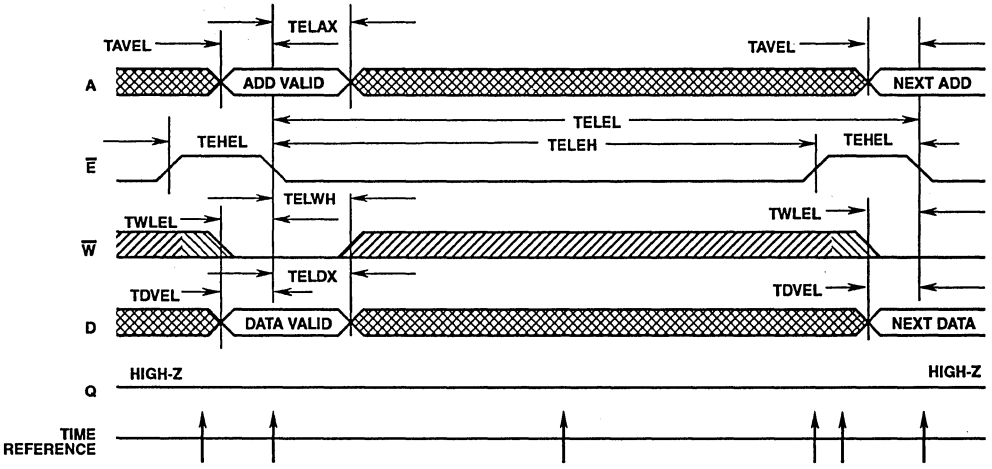
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	INPUTS $\overline{W}$	INPUTS A	OUTPUT Q	FUNCTION
-1	H	X	X	Z	Memory Disabled
0	↓	H	V	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	Output Enabled
2	L	H	X	V	Output Valid
3	↑	H	X	V	Read Accomplished
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and ready the RAM for the next memory cycle (T = 4).

Timing Waveforms (Continued)

EARLY WRITE CYCLE



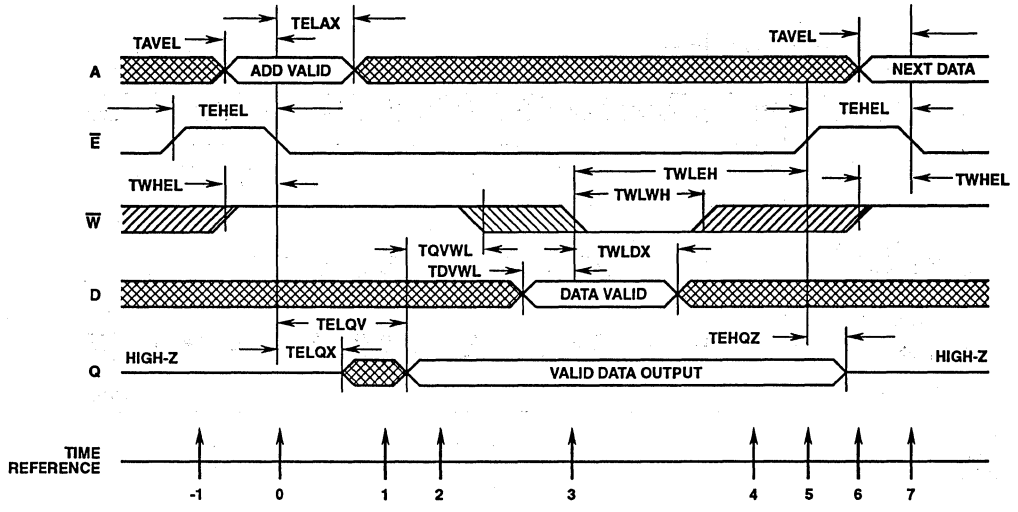
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	INPUTS $\overline{W}$	INPUTS A	INPUTS D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	Memory Disabled
0	↘	L	V	V	Z	Cycle Begins, Addresses are Latched
1	L	X	X	X	Z	Write in Progress Internally
2	↗	X	X	X	Z	Write Complete
3	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
4	↘	L	V	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls determines the state of the output buffer for the cycle. Since $\overline{W}$ is low when $\overline{E}$ falls, the output buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; therefore data set up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state the output buffer disables and all signals are unlatched. The device is now ready for the next cycle.

Timing Waveforms (Continued)

READ MODIFY WRITE CYCLE



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	INPUTS $\overline{W}$	INPUTS A	INPUTS D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	Memory Disabled
0	↓	H	V	X	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	X	Output Enabled
2	L	H	X	X	V	Output Valid, Read and Modify Time
3	L	↓	X	V	V	Write Begins, Data is Latched
4	L	X	X	X	V	Write in Progress Internally
5	↑	X	X	X	V	Write Complete
6	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
7	↓	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The read modify write cycle begins as all other cycles on the falling edge of $\overline{E}$ (T = 0). The $\overline{W}$ line should be high at (T = 0) in order to latch the output buffers in the active state. During (T = 1) the output will be active but not valid until (T = 2). On the falling edge of the $\overline{W}$ (T = 3) the data present at the output and input are latched. The $\overline{W}$ signal also latches itself on its low going edge. All input signals excluding $\overline{E}$ have been latched and have no further effect on the RAM. The rising edge of $\overline{E}$ (T = 5) completes the write portion of the cycle and unlatches all inputs and output. The output goes to a high impedane and the RAM is ready for the next cycle.

NOTE: In the above descriptions the numbers in parenthesis (T = n) refers to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

Organization Guide

To Organize 8K x 8:

Connect:	$\overline{E1}$ with $\overline{E3}$	(Pins 9 + 32)
	$\overline{E2}$ with $\overline{E4}$	(Pins 12 + 29)
	$\overline{W1}$ with $\overline{W2}$	(Pins 11 + 31)

To Organize 16K x 4:

Connect:	Q0 with Q4	(Pins 2 + 39)
	D0 with D4	(Pins 3 + 38)
	Q1 with Q5	(Pins 4 + 37)
	D1 with D5	(Pins 5 + 36)
	D2 with D6	(Pins 16 + 25)
	Q2 with Q6	(Pins 17 + 24)
	D3 with D7	(Pins 18 + 23)
	Q3 with Q7	(Pins 19 + 22)
Optional	$\overline{W1}$ may be common with $\overline{W2}$	(Pins 11 + 31)

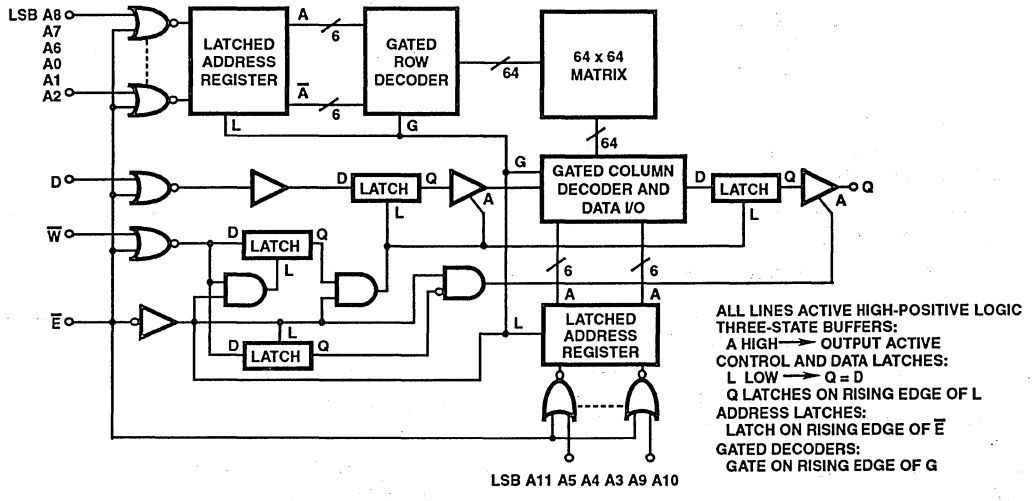
Concerns for Proper Operation of Chip Enables:

The transition between blocks of RAM requires a change in the chip enable being used. When operating in the 8K x 8 mode, use the chip enables as if there were only two, $\overline{E1}$ and $\overline{E2}$. In the 16K x 4 mode, all chip enables must be treated separately. Transitions between chip enables must be treated with the same timing constraints that apply to any one chip enable. All chip enables must be high at least one chip enable high time (TEHEL) before any chip enable can fall. More than one chip enable low simultaneously, for devices whose outputs are tied common either internally or externally, is an illegal input condition and must be avoid.

Printed Circuit Board Mounting:

The leadless chip carrier packages used in the HS-6564RH have conductive lids. These lids are electrically floating, not connected to VDD or GND. The designer should be aware of the possibility that the carriers on the bottom side could short conductors below if pressed completely down against the surface of the circuit board. The pins on the package are designed with a standoff feature to help prevent the leadless carriers from touching the circuit board surface.

HS-6504RH (One of Sixteen)



Board Size Tradeoffs

Printed circuit board real estate is a costly commodity. Actual board costs depend on layout tolerances, density, complexity, number of layers, choice of board material, and other factors.

The following table compares board space for 16 standard DIP 4K RAMs to the HS-6564RH RAM array. Both fine line, close tolerance layout and standard "easy" layout board sizes are shown in the comparison.

We urge you to contact your local Harris office of sales representative for accurate pricing allowing cost tradeoff analysis. In your cost analysis, also consider the advantages of a lighter, smaller overall package for your system. Con sider how much more valuable your system will be when the memory array size is decreased to about 1/6 of normal size.

64K ARRAY OR 16 4K RAMs ON A PC BOARD vs. THE HS-6564RH

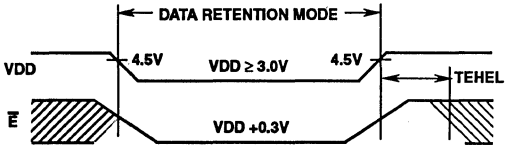
PACKAGE	CIRCUIT SUBSTRATE	SIZE
18 Pin DIP	Standard Two Sided PCB	12 to 15 Square Inches
18 Pin DIP	Fine Line or Multilayer PCB	9 to 11 Square Inches
18 Pin Leadless Carrier	Multilayer Alumina Substrate	3 to 5 Square Inches
HS-6564RH	Two Sided Mounting Multilayer Alumina Substrate	2 Square Inches

Low Voltage Data Retention

HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VDD +0.3V to VDD - 0.3V.
2. All other inputs should be held either high (at CMOS VDD) or at ground to minimize IDDDR.
3. Inputs which are held high (e.g. $\overline{E}$) must be kept between VDD +0.3V and 70% of VDD during the power up and power down transitions.
4. The RAM can begin operation one TEHEL after VDD reaches the minimum operating voltage (4.5 volts).

DATA RETENTION MODE



Burn-In/Irradiation Circuits

NOTE: See HS-6504RH for appropriate irradiation bias and BI circuits.

Harris - Space Level Product Flow

HS4-6504RH LCCs are fully tested and processed through the Harris space level (-Q) product flow (see page 8-91) and are assembled onto a ceramic substrate for the HS5-6564RH module.

Temperature Cycle - 10 Cycles

Serialization

Electrical Tests Subgroups 1, 7, 9; Read and Record Subgroup 1 only

Electrical Tests Subgroups 3, 8B, 11; Read and Record Subgroup 3 only

Electrical Tests Subgroups 2, 8A, 10; Read and Record Subgroups 2 only

Gross Leak Method 1014, 100%

Fine Lead Method 1014, 100%

Customer Source Inspection (Note 1)

External Visual Inspection Method 2009

Data package Generation (Note 3)

NOTES:

1. These steps are optional, and should be listed on the purchase order if required.
2. This data comes from the testing and processing of the HS5-6504RH LCC's.
3. Data package contains:
   - Assembly Attributes (post seal)
   - Test Attributes (includes Group A)
   - Shippable Serial Number List
   - Radiation Testing Certificate of Conformance (Note 2)
   - Wafer Lot Acceptance Report (includes SEM report) (Note 2)
   - X-Ray Report and Film (Note 2)
   - Test Variables Data

HS-65C162RRH

Radiation Hardened 2048 x 8-Bit Asynchronous CMOS Static RAM

December 1992

Features

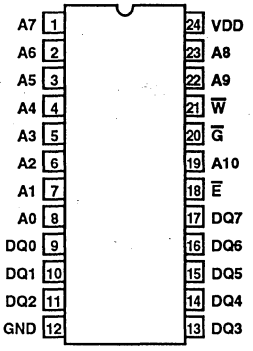
- Radiation Hardened EPI-CMOS
- Total Dose 2 x 10^5 RAD(Si)
- Transient Upset > 1 x 10^9 RAD(Si)/s
- Latch-Up Free > 1 x 10^{12} RAD(Si)/s
- Single Event Upset Hardened Option
- Low Standby Current 200µA Max
- Fast Access Time 160ns Max
- 2048 x 8-Bit
- Single +5V Power Supply
- Asynchronous Operation
- CMOS Compatible Inputs
- Completely Static Operation
- Three-State Output
- Military Temperature Range -55°C to +125°C Operation
- Functionally Equivalent to Harris HM-65162

Description

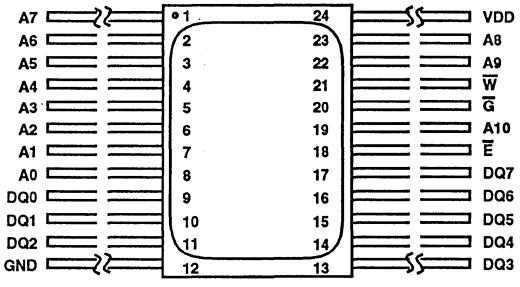
The HS-65C162RRH is designed to be functionally compatible with the Harris HM-65162. This device is a asynchronous 2048 x 8-bit static CMOS RAM fabricated using the Harris radiation hardened, self-aligned junction isolated silicon gate technology. The HS-65C162RRH is designed to have a maximum access time of 160ns after exposure to 2 x 10^5 Rads(Si) over the full military temperature range. Latch-up free operation is achieved by the use of epitaxial starting material. In addition, the device is single event upset hardened. Operation is designed for +5V.

Pinouts

24 PIN SIDEBRAZED DIP
CASE OUTLINE D3, CONFIGURATION 3
TOP VIEW



24 PIN FLATPACK
CASE OUTLINE F6A, CONFIGURATION 2
TOP VIEW

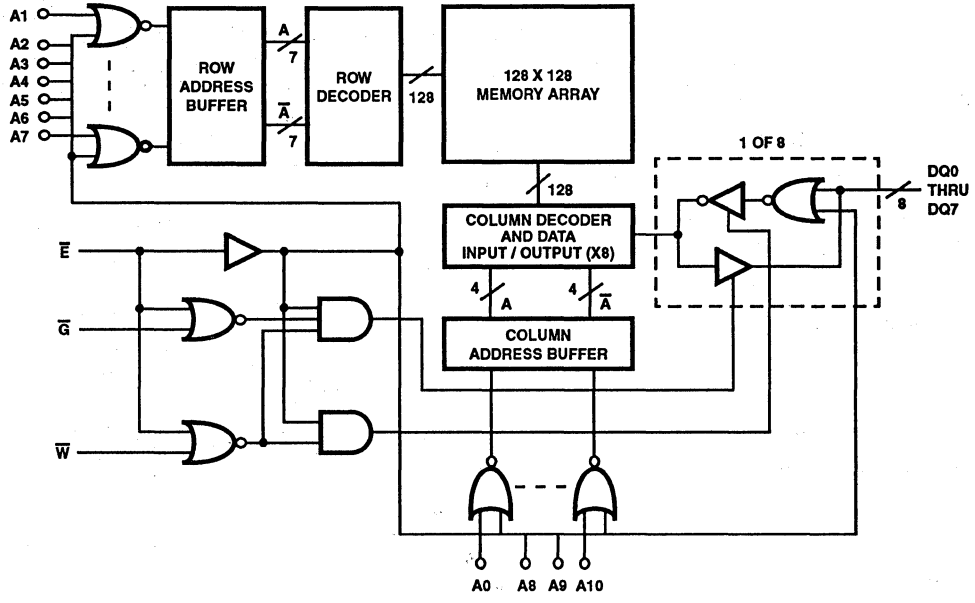


PIN	DESCRIPTION
A	Address Input
DQ	Data In/Data Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
NC	No Connect
$\overline{W}$	Write Enable

8 MEMORIES

File Number 3030

Functional Diagram



TRUTH TABLE

Ē	Ḡ	W̄	MODE
1	X	X	Disabled
0	1	1	Enabled
0	0	1	Read
0	X	0	Write

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage ..... GND-0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 5mA/MHz Increase in ICCOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	56°C/W	12°C/W
Braze Seal Flatpack Package	66°C/W	11°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package 0.89W
Braze Seal Flatpack Package 0.76W
Gate Count ..... 26000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
SEU Immunity Operating Temperature Range ..... -20°C to +80°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... VDD -1.5V to VDD
Data Retention Supply Voltage ..... 3.0V to 4.5V
Input Rise and Fall Time ..... 40ns Max.

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VDD = 4.5V, IO = -5.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.4	-	V
	VOH2	VDD = 4.5V, IO = -100mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	VDD-0.4	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, IO = 5.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
High Impedance Output Leakage Current	IOZ	VDD = 5.5V, G = 5.5V, or E = 5.5V, VI/O = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10.0	10.0	µA
Input Leakage Current	II	VDD = 5.5V, VI = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	1.0	µA
Standby Supply Current	IDDSB1	VDD = 5.5V, IO = 0mA, E = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	200	µA
Operating Supply Current	IDDOP	VDD = 5.5V, G = 5.5V, (Note 2), f = 1MHz, E = 0.8V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	100	mA
Enable Supply Current	ENIDD	VDD = 5.5V, IO = 0mA, E = 0.8V, VDD = VIH, VIL = 0V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	100	mA
Data Retention Supply Current	IDDDR	VDD = 3.0V, IO = 0mA, E = VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	100	µA
Functional Test	FT	VCC = 4.5V (Note 3)	7, 8A, 8B	-55°C ≤ T_A ≤ +125°C	-	-	-

NOTE:

1. All voltages referenced to device GND.
2. Typical derating = 5mA/MHz increase in ICCOP.
3. Tested as follows: f = 1MHz, VIH = 4.5V, VIL = 0V, IOH = -4.0mA, IOL = 4.0mA, VOH ≥ 1.5V, and VOL ≤ 1.5V.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Address Access Time	TAVQV	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	-	160	ns
Output Enable Access Time	TGLQV	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	-	120	ns
Chip Enable Access Time	TELQV	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	-	160	ns
Write Enable Read Setup Time	TWHAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	20	-	ns
Address Setup Time	TAVWL	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	20	-	ns
Chip Selection to End of Write	TELWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	180	-	ns
Write Enable Pulse Setup Time	TWLEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	175	-	ns
Chip Enable Data Setup Time	TDVEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	175	-	ns
Address Valid to End of Write	TAVWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	180	-	ns
Write Enable Pulse Width	TWLWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	160	-	ns
Data Setup Time	TDVWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	160	-	ns
Data Hold Time	TWHDX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	30	-	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V to VDD-1.5; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL ≥ 50pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS, AC AND DC

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CIN	VCC = Open, f = 1MHz	1, 2, 4	$T_A = +25°C$	-	15	pF
			1, 3, 4	$T_A = +25°C$	-	12	pF
I/O Capacitance	CI/O	VCC = Open, f = 1MHz	1, 2, 4	$T_A = +25°C$	-	12	pF
			1, 3, 4	$T_A = +25°C$	-	10	pF
Write Enable to Output in High Z	TWLQZ	VCC = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	-	60	ns
Write Enable High to Output ON	TWHQX	VCC = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	5	-	ns
Chip Enable to Output ON	TELQX	VCC = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	5	-	ns
Output Enable to Output ON	TGLQX	VCC = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	5	-	ns
Chip Enable High to Output High Z	TEHQZ	VCC = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	-	60	ns
Output Disable to Output in High Z	TGHQZ	VCC = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	-	40	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS, AC AND DC (Continued)

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Hold from Address Change	TAVQX	VCC = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	5	-	ns
Cycle Time	TAVAX	VCC = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	200	-	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. Applies to DIP device types only.
3. Applies to Flatpack device types only.
4. All measurements referenced to device grounds.

TABLE 4. POST 200K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The post irradiation test conditions and limits are the same as those listed in Tables 1 and 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

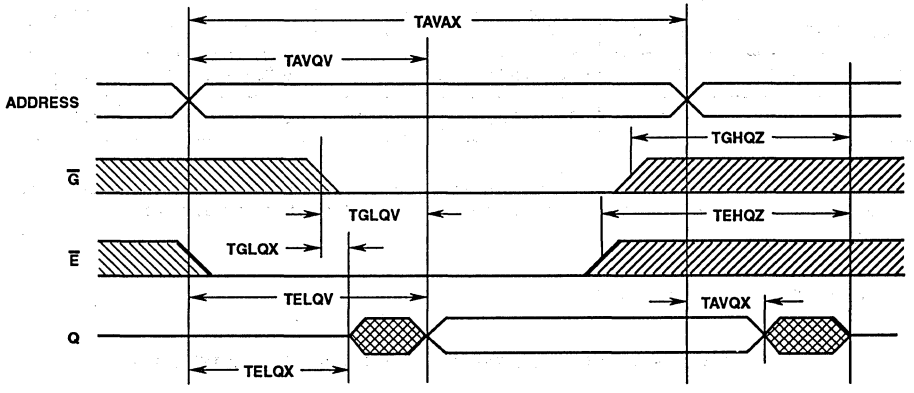
PARAMETER	SYMBOL	DELTA LIMITS
Output Low Voltage	VOL	± 80mV
Output High Voltage	VOH	± 400mV
Input Leakage Current	IIL	± 100nA
	IIH	±100nA
Standby Supply Current	IDDSB1	±30µA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	-	-
Interim Test		100%/5004	1, 7, 9	1, 7, 9
PDA		100%/5004	1, 7, Δ	1
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A
	Others	Samples/5005	1, 7, 9	N/A
Group C (Optional)		Samples/5005	N/A	1, 7, 9
Group D (Optional)		Samples/5005	1, 7, 9	1, 7, 9

Timing Waveforms

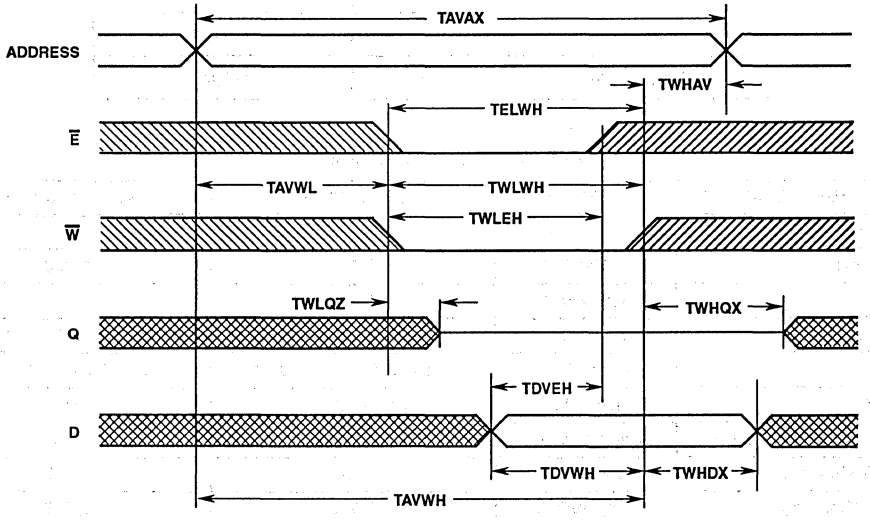
READ CYCLE



NOTE: $\overline{W}$ is high for a Read Cycle

Addresses must remain stable for the duration of the read cycle. To read, $\overline{G}$ and $\overline{E}$ must be ≤ VIL and W ≥ VIH. The output buffers can be controlled independently by $\overline{G}$ while $\overline{E}$ is low. To execute consecutive read cycles, $\overline{E}$ may be tied low continuously until all desired locations are accessed. When $\overline{E}$ is low, addresses must be driven by stable logic levels and must not be in the high impedance state.

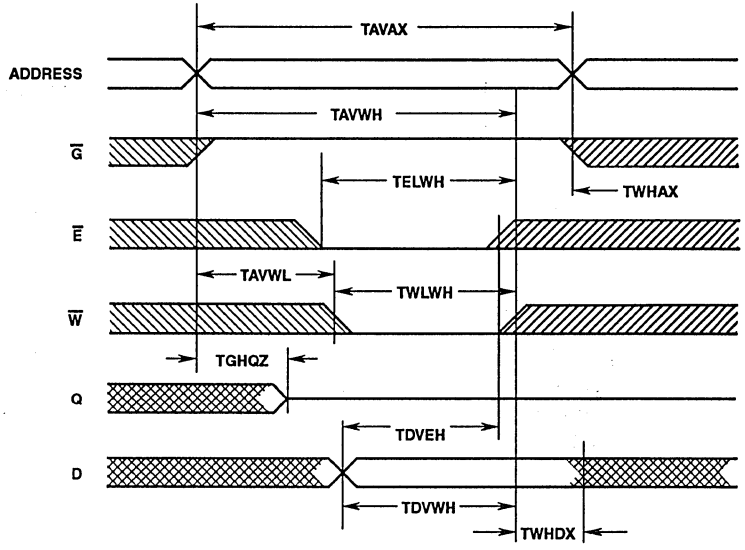
WRITE CYCLE I



NOTE: $\overline{W}$ is high for a Read Cycle

To write, addresses must be stable, E low and W falling low for a period no shorter than TWLWH. Data in is referenced with the rising edge of W. (TDVWH and TWHDX). While addresses are changing, W must be high. When W falls low, the I/O pins are still in the output state for a period of TWLQZ and input data of the opposite phase to the outputs must not be applied. (Bus contention). If E transitions low simultaneously with the W line transitioning low or after the W transition, the output will remain in a high impedance state. G is held continuously low.

WRITE CYCLE II



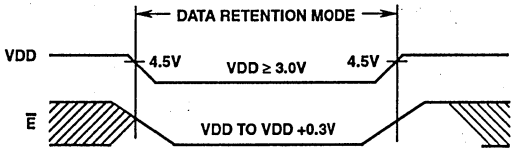
In this write cycle $\overline{G}$ has control of the output after a period, TGHQZ. $\overline{G}$ switching the output to a high impedance state allows data in to be applied without bus contention after TGHQZ. When $\overline{W}$ transitions high, the data in can change after TWHDX to complete the write cycle.

Low Voltage Data Retention

Harris CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

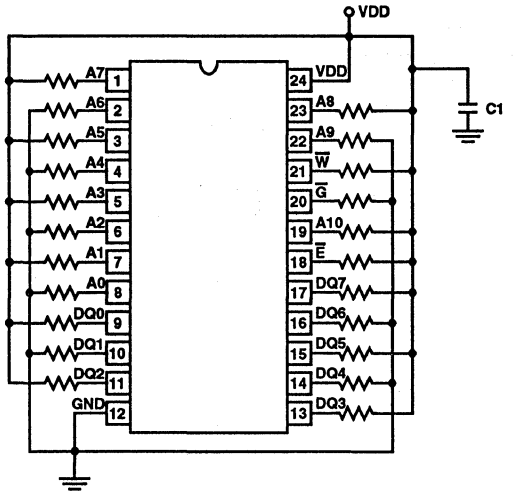
1. Chip Enable ($\overline{E}$) must be held high during data retention; within VDD to VDD +0.3V.
2. $\overline{E}$ must be kept between VDD +0.3V and 70% of VDD during the power up and power down transitions.

DATA RETENTION TIMING



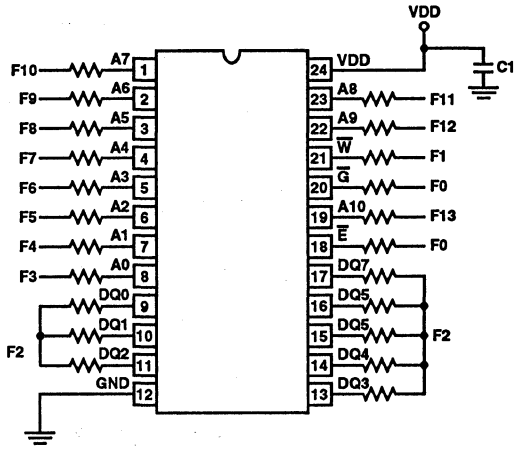
Burn-In Circuits

HS-65C162RRH (CERAMIC DIP)



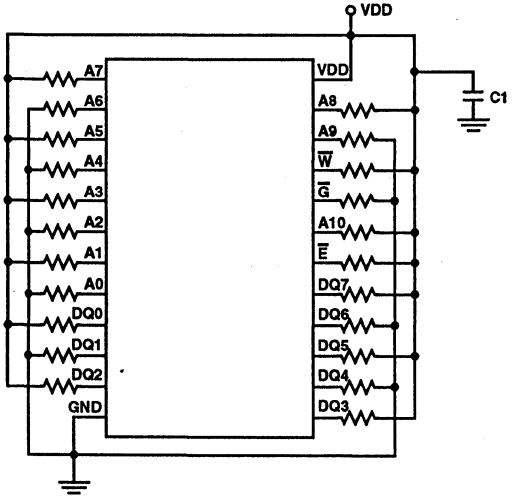
STATIC CONFIGURATION

HS-65C162RRH (CERAMIC DIP)



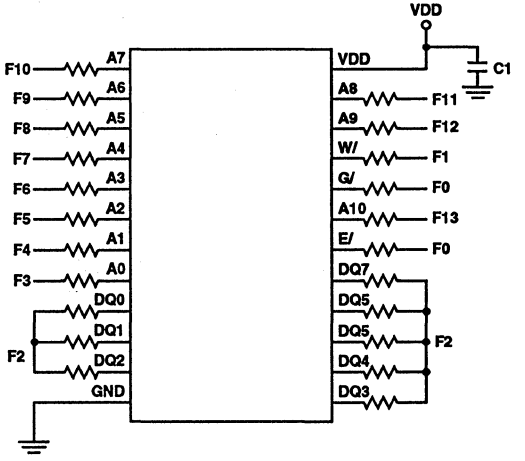
DYNAMIC CONFIGURATION

HS-65C162RRH (FLATPACK)



STATIC CONFIGURATION

HS-65C162RRH (FLATPACK)



DYNAMIC CONFIGURATION

NOTE:

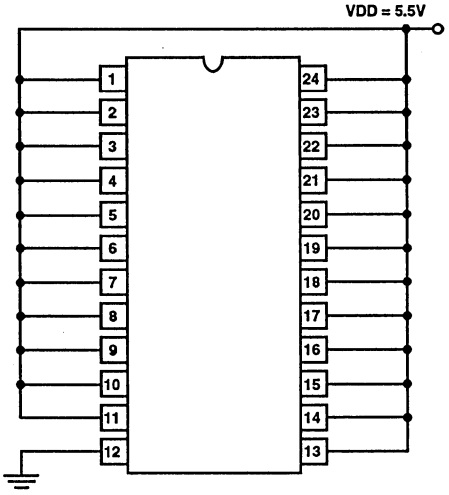
C1 = 0.01µF (min)

NOTES:

VCC = 6.0V ± 0.5V
VIH = 4.0V to VCC
VIL = 0.8V (max)
C1 = 0.01µF (min)
All Resistors = 27kΩ ± 10%
F0 = 100KHz ± 10%, 50% duty cycle
F1 = F0/2, F2 = F1/2, . . . F13 = F12/2

Irradiation Circuit

HS-65C162RRH (CERAMIC DIP)



NOTE:

1. Pin 12 to Ground
2. All other pins tied to VDD

Harris - Space Level (-Q) Product Flow (Note 1)

SEM - Traceable to Diffusion Method 2018
Wafer Lot Acceptance Method 5007
Internal Visual Inspection Method 2010, Condition A
Gamma Radiation Assurance Tests Method 1019
Nondestructive Bond Pull Method 2023
Customer Pre-Cap Visual Inspection (Note 2)
Temperature Cycling Method 1010, Condition C
Constant Acceleration Method 2001, Condition E Min, Y1
Particle Impact Noise Detection Method 2020, Condition A
Electrical Tests (Harris' Option)
Serialization
X-Ray Inspection Method 2012
Electrical Tests - Subgroup 1; Read and Record (T0)
Static Burn-In Method 1015, Condition B, 72 Hrs, +125°C Min.
Interim 1 Electrical Tests - Subgroup 1; Read and Record (T1)
Burn-In Delta Calculation (T0 -T1)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Dynamic Burn-In Method 1015, Condition D, 240 Hrs, +125°C (Note 3)
Interim 2 Electrical Tests - Subgroup 1; Read and Record (T2)
Alternate Group A - Subgroups 1, 7, 9; Method 5005; Para 3.5.1.1
Burn-In Delta Calculation (T0 - T2)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Electrical Tests - Subgroup 3; Read and Record
Alternate Group A - Subgroups 3, 8B, 11; Method 5005; Para 3.5.1.1
Marking
Electrical Tests - Subgroup 2; Read and Record
Alternate Group A - Subgroups 2, 8A, 10; Method 5005; Para 3.5.1.1
Gross Leak Tests Method 1014, 100%
Fine Leak Tests Method 1014, 100%
Customer Source Inspection (Note 2)
Group B Inspection Method 5005 (Note 2)
End-Point Electrical Parameters: B-5 - Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11; B-6 - Subgroups 1, 7, 9
Group D Inspection Method 5005 (Notes 2, 4)
End-Point Electrical Parameters: Subgroups 1, 7, 9
External Visual Inspection Method 2009
Data Package Generation (Note 5)

NOTES:

1. The notes of Method 5004, Table 1 shall apply; Unless Otherwise Specified.
2. These steps are optional, and should be listed on the individual purchase order(s), when required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table 1 of Method 1015.
4. For Group D, Subgroup 3 inspection of package configurations which utilizes a gold plated lid in its construction; the inspection criteria for illegible markings criteria of Method 1010, paragraph 3.3 and of Method 1004, paragraph 3.8.a shall not apply.
5. Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (Including SEM Report)
   X-Ray Report and Film
   Test Variables Data

Harris -8 Product Flow

Internal Visual Inspection
Gamma Radiation Assurance Tests Method 1019
Customer Pre-Cap Visual Inspection (Note 1)
Temperature Cycling Method 1010, Condition C
Fine and Gross Leak Tests Method 1014
Constant Acceleration Method 2001 Y1 30KG
Initial Electrical Tests
Dynamic Burn-In Method 1015, Condition D, 160 Hrs, +125°C
+25°C Electrical Tests - Subgroups 1, 7, 9
PDA Calculation 5% Subgroups 1, 7
Electrical Tests +125°C, -55°C
Group A Inspection Method 5005. 5% PDA (Note 3)
Brand
Customer Source Inspection (Note 1)
Group C Inspection Method 5005 (Notes 1, 2)
Group D Inspection Method 5005 (Notes 1, 2)
External Visual Inspection Method 2009
Data Package Generation (Note 4)

NOTES:

1. These steps are optional, and must be negotiated as part of order.
2. Group B and D data package contains Attributes Data plus Variables Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable.
4. '-8' Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Radiation Testing Certificate of Conformance
   Certificate of Conformance (as found on shipper)

Metallization Topology

DIE DIMENSIONS:
198 x 270 x 19 ±1mils

METALLIZATION:
Type: Silicon-Aluminum
Thickness: 13kÅ ± 1.5kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

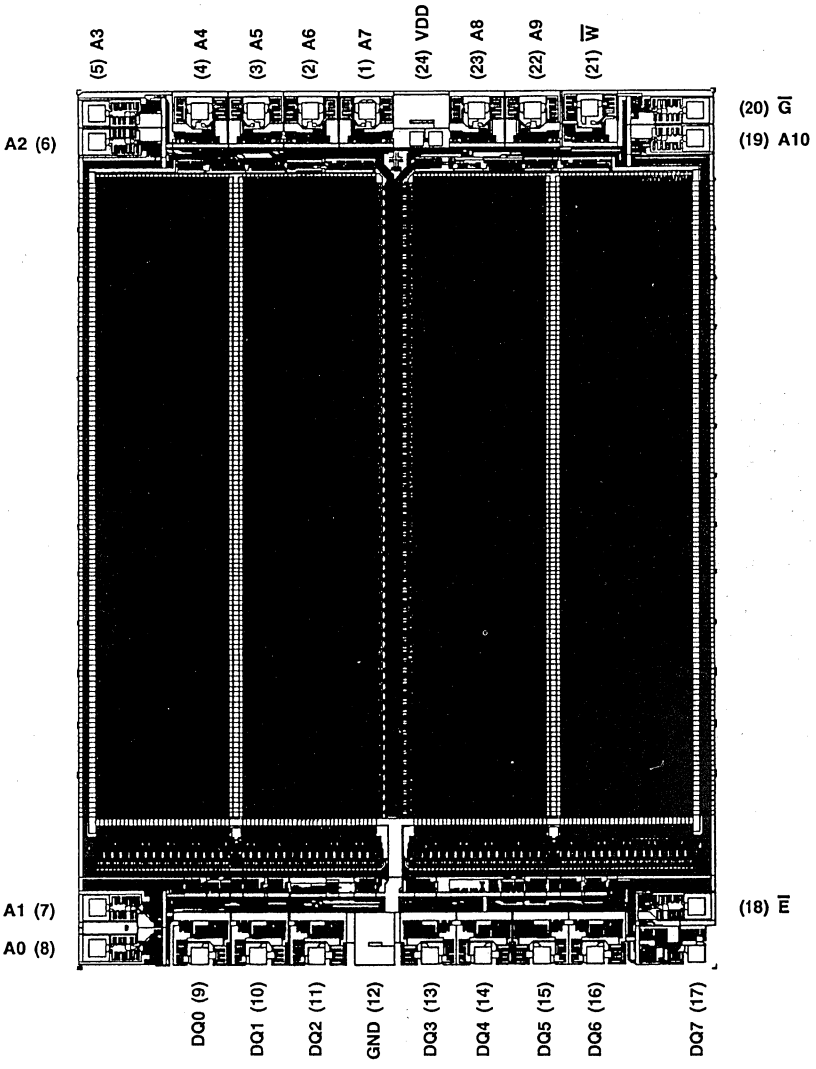
DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Braze Seal DIP - 460°C (Max)
Braze Seal Flatpack - 460°C (Max)

WORST CASE CURRENT DENSITY:
1.4×10^5 A/cm^2

SUBSTRATE POTENTIAL: VDD

Metallization Mask Layout

HS-65C162RRH



HARRIS SEMICONDUCTOR

HS-65C262RH/RRH
HS-65T262RRH

Radiation Hardened 16K x 1 CMOS RAM

December 1992

Features

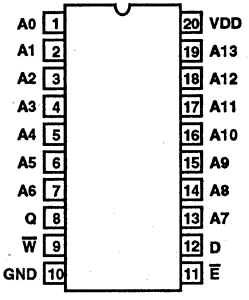
- Radiation Hardened EPI-CMOS
  - Total Dose 2 x 10^5 RAD(Si)
  - Transient Upset > 5 x 10^8 RAD(Si)/s
  - Latch-up Free > 1 x 10^{12} RAD(Si)/s
- Single Event Upset Resistant Option
- Low Standby Current 200µA (Max)
- Low Operating Current 6mA/MHz (Max)
- Fast Access Time 150ns (Typ)
- 16,384 x 1-Bit
- Single +5V Power Supply
- Asynchronous Operation
- CMOS or TTL Compatible Inputs
- Completely Static Operation
- Three-State Output
- Military Temperature Range -55°C to +125°C

Description

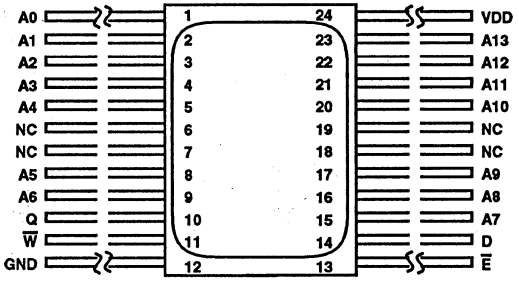
The HS-65C262RH and HS-65T262RRH are both designed to be functionally compatible with the Harris HM-65262. Two versions of the radiation hardened CMOS RAM are offered to provide both CMOS input levels (HS-65C262RH) and TTL compatible input levels (HS-65T262RRH). Both RAMs are asynchronous 16,384 x 1 bit static CMOS RAMs fabricated using the Harris radiation hardened, self-aligned junction isolated silicon gate technology. The devices are designed to have a maximum access time of 150ns for CMOS input levels and 175ns for TTL input levels after exposure to 2 x 10^5 Rads(Si) over the full military temperature range. Latch-up free operation is achieved by the use of epitaxial starting material. In addition, the devices have the option to be single event upset resistant. Operation is designed for +5V. Contact your nearest Harris represent- ative for sample availability.

Pinouts

20 PIN CERAMIC DIP
CASE OUTLINE D8, CONFIGURATION 3
TOP VIEW



24 PIN FLATPACK
CASE OUTLINE F-6A, CONFIGURATION 2
TOP VIEW

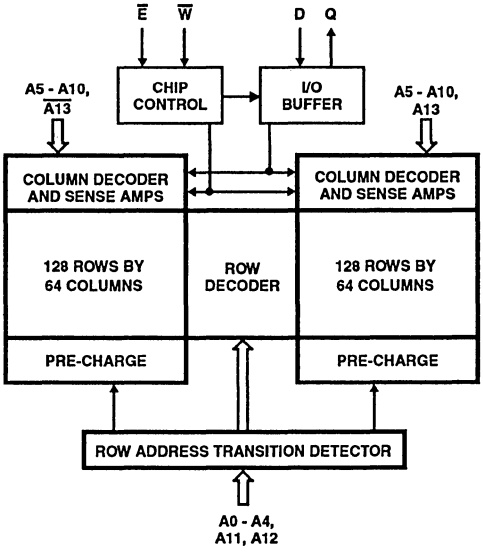


PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output
NC	No Connect

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3031

Functional Diagram



TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE
1	X	X	Disabled
0	1	1	Enabled
0	0	1	Read
0	X	0	Write

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage ..... GND-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 6mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	78°C/W	13°C/W
Braze Seal FP Package	91°C/W	11°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package 0.64W
Braze Seal FP Package 0.55W
Gate Count ..... 26256 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... VDD -1.5V to VDD
Data Retention Supply Voltage ..... 3.0V to 4.5V
Input Rise and Fall Time ..... 40ns Max.

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VDD = 4.5V, IO = -5.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.4	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, IO = 5.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VDD = 5.5V, E = 5.5V, VO = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10.0	10.0	µA
Input Leakage Current	II	VDD = 5.5V, VI = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	1.0	µA
Standby Supply Current	IDDSB1	VDD = 5.5V, IO = 0mA, E = VDD-0.3V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	200	µA
Operating Supply Current	IDDOP	VDD = 5.5V, (Note 2), f = 1MHz, E = 0.8V, VI = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	6	mA
Data Retention Supply Current	IDDDR	VDD = 3.0V, IO = 0mA, E = VDD-0.3V, VI = VDD or GND	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	100	µA
Enable Supply Current	IDDEN	VDD = 5.5, IO = 0mA, E = 0.8V, VI = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	200	µA
Functional Test	FT	VDD = 4.5V (Note 3)	7, 8A, 8B	-55°C ≤ T_A ≤ +125°C	-	-	-

NOTE:

1. All voltages referenced to device GND. Negative undershoots to a minimum of -0.3V are allowed with a maximum of 50ns pulse width.
2. Typical derating = 6mA/MHz increase in IDDOP.
3. Tested as follows: f = 3MHz, VIH = 4.5V, VIL = 0V, IOH = -4.0mA, IOL = 4.0mA, VOH ≤ 1.5V, and VOL ≤ 1.5V.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

PARAMETERS	SYMBOL	CONDITIONS	(NOTES 1, 2, 3) GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Access Time	(2) TAVQV	VDD = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	145	ns
Chip Enable to End of Write	(3) TELWH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	95	-	ns
Chip Enable Access Time	(4) TELQV	VDD = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	150	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Guaranteed and 100% Tested.

PARAMETERS	SYMBOL	CONDITIONS	(NOTES 1,2,3) GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Hold Time	(5) TWHAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	0	-	ns
Address Setup Time	(6) TAVWL	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	10	-	ns
Address Valid to End of Write	(7) TAVWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	95	-	ns
Address Setup Time	(8) TAVEL	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	0	-	ns
Address Hold Time	(9) TEHAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	0	-	ns
Address Valid to End of Write	(10) TAVEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	95	-	ns
Write Enable Pulse Width	(11) TWLWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	85	-	ns
Data Setup Time	(12) TDVWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	85	-	ns
Data Hold Time	(13) TWHDX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	10	-	ns
Enable Pulse Width	(14) TELEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	150	-	ns
Write to End of Write	(15) TWLEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	85	-	ns
Data Setup Time	(16) TDVEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	85	-	ns
Data Hold Time	(17) TEHDX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	10	-	ns

NOTES:

1. All voltages referenced to device GND. Negative undershoots to a minimum of -0.3V are allowed with a maximum of 50ns pulse width.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V to VDD-1.5; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL ≥ 50pF; for CL > 50pF, access times are derated 0.15ns/pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS, AC AND DC

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz	1, 2, 4	$T_A = +25°C$	-	8	pF
			1, 3, 4	$T_A = +25°C$	-	10	pF
Output Capacitance	CO	VDD = Open, f = 1MHz	1, 2, 4	$T_A = +25°C$	-	10	pF
			1, 3, 4	$T_A = +25°C$	-	12	pF
Read/Write	(1) TAVAX	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	150	-	ns
Write Enable to Output in High Z	(18) TWLQZ	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	-	30	ns
Write Enable High to Output ON	(19) TWHQX	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	5	-	ns
Chip Enable to Output ON	(20) TELQX	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	5	-	ns
Output Enable High to Output High Z	(21) TEHQZ	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	-	25	ns
Chip Disable to Output Hold Time	(22) TEHQX	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	5	-	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS, AC AND DC (Continued)

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Address Invalid Output Hold Time	(23) TAXQX	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	5	-	ns
Cycle Time	TAVAX	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	150	-	ns
High Level Output Voltage	VOH2	VDD = 4.5V, IO = -100µA	1	-55°C ≤ T_A ≤ +125°C	VDD - 0.4V	-	V

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. Applies to DIP device types only.
3. Applies to Flatpack device types only.
4. All measurements referenced to device grounds.

TABLE 4. POST 200K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The post irradiation test conditions and limits are the same as those listed in Tables 1 and 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Output Low Voltage	VOL	± 60mV
Output High Voltage	VOH	± 400mV
Input Leakage Current	IIL	± 100nA
	IIH	±100nA
Low Impedance Output Leakage Current	IOZL	±1µA
High Impedance Output Leakage Current	IOZH	±1µA
Standby Supply Current	IDDSB1	±30µA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	-	-
Interim Test		100%/5004	1, 7, 9	1, 7, 9
PDA		100%/5004	1, 7, Δ	1
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B	N/A
	Others	Samples/5005	1, 7	N/A
Group C (Optional)		Samples/5005	N/A	1, 7
Group D (Optional)		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7	1, 7

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage ..... GND-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 6mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	78°C/W	13°C/W
Braze Seal FP Package	91°C/W	11°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package 0.64W
Braze Seal FP Package 0.55W
Gate Count ..... 26256 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... VDD -1.5V to VDD
Data Retention Supply Voltage ..... 3.0V to 4.5V
Input Rise and Fall Time ..... 40ns Max.
SEU Immunity Operating Temperature Range ..... -20°C to +80°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VDD = 4.5V, IO = -5.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.4	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, IO = 5.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VDD = 5.5V, $\overline{E}$ = 5.5V, VO = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10.0	10.0	µA
Input Leakage Current	II	VDD = 5.5V, VI = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	1.0	µA
Standby Supply Current	IDDSB1	VDD = 5.5V, IO = 0mA, $\overline{E}$ = VDD-0.3V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	200	µA
Operating Supply Current	IDDOP	VDD = 5.5V, (Note 2), f = 1MHz, $\overline{E}$ = 0.8V, VI = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	6	mA
Data Retention Supply Current	IDDDR	VDD = 3.0V, IO = 0mA, E = VDD-0.3V, VI = VDD or GND	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	100	µA
Enable Supply Current	IDDEN	VDD = 5.5, IO = 0mA, E = 0.8V, VI = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	200	µA
Functional Test	FT	VDD = 4.5V (Note 3)	7, 8A, 8B	-55°C ≤ T_A ≤ +125°C	-	-	-

NOTE:

1. All voltages referenced to device GND. Negative undershoots to a minimum of -0.3V are allowed with a maximum of 50ns pulse width.
2. Typical derating = 6mA/MHz increase in IDDOP.
3. Tested as follows: f = 3MHz, VIH = 4.5V, VIL = 0V, IOH = -4.0mA, IOL = 4.0mA, VOH ≤ 1.5V, and VOL ≤ 1.5V.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

PARAMETERS	SYMBOL	CONDITIONS	(NOTES 1, 2, 3) GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Access Time	(2) TAVQV	VDD = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	145	ns
Chip Enable to End of Write	(3) TELWH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	150	-	ns
Chip Enable Access Time	(4) TELQV	VDD = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	150	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Guaranteed and 100% Tested.

PARAMETERS	SYMBOL	CONDITIONS	(NOTES 1,2,3) GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Hold Time	(5) TWHAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	ns
Address Setup Time	(6) TAVWL	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	10	-	ns
Address Valid to End of Write	(7) TAVWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	150	-	ns
Address Setup Time	(8) TAVEL	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	ns
Address Hold Time	(9) TEHAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	ns
Address Valid to End of Write	(10) TAVEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	150	-	ns
Write Enable Pulse Width	(11) TWLWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	150	-	ns
Data Setup Time	(12) TDVWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	140	-	ns
Data Hold Time	(13) TWHDX	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	10	-	ns
Enable Pulse Width	(14) TELEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	150	-	ns
Write to End of Write	(15) TWLEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	140	-	ns
Data Setup Time	(16) TDVEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	140	-	ns
Data Hold Time	(17) TEHDX	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	10	-	ns

NOTES:

1. All voltages referenced to device GND. Negative undershoots to a minimum of -0.3V are allowed with a maximum of 50ns pulse width.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V to VDD-1.5; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL ≥ 50pF; for CL > 50pF, access times are derated 0.15ns/pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS, AC AND DC

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VCC = Open, f = 1MHz	1, 2, 4	$T_A = +25^oC$	-	8	pF
			1, 3, 4	$T_A = +25^oC$	-	TBD	pF
Output Capacitance	CO	VDD = Open, f = 1MHz	1, 2, 4	$T_A = +25^oC$	-	10	pF
			1, 3, 4	$T_A = +25^oC$	-	TBD	pF
Read/Write	(1) TAVAX	VDD = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	150	-	ns
Write Enable to Output in High Z	(18) TWLQZ	VDD = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	-	30	ns
Write Enable High to Output ON	(19) TWHQX	VDD = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	5	-	ns
Chip Enable to Output ON	(20) TELQX	VDD = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	5	-	ns
Output Enable High to Output High Z	(21) TEHQZ	VDD = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	-	25	ns
Chip Disable to Output Hold Time	(22) TEHQX	VDD = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	5	-	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS, AC AND DC (Continued)

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	(23) TAXQX	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	5	-	ns
High Level Output Voltage	VOH2	VDD = 4.5, IO = -100µA	1	-55°C ≤ T_A ≤ +125°C	VDD-0.4V	-	V
Cycle Time	TAVAX	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	150	-	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. Applies to DIP device types only.
3. Applies to Flatpack device types only.
4. All Measurements Referenced To Device Grounds

TABLE 4. POST 200K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The post irradiation test conditions and limits are the same as those listed in Tables 1 and 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Output Low Voltage	VOL	± 60mV
Output High Voltage	VOH	± 400mV
Input Leakage Current	IIL	± 100nA
	IIH	±100nA
Low Impedance Output Leakage Current	IOZL	±1µA
High Impedance Output Leakage Current	IOZH	±1µA
Standby Supply Current	IDDSB1	±30µA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	-	-
Interim Test		100%/5004	1, 7, 9	1, 7, 9
PDA		100%/5004	1, 7, Δ	1
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B	N/A
	Others	Samples/5005	1, 7	N/A
Group C (Optional)		Samples/5005	N/A	1, 7
Group D (Optional)		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7	1, 7

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage ..... GND-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 6mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	78°C/W	13°C/W
Braze Seal FP Package	91°C/W	11°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package 0.64W
Braze Seal FP Package 0.55W
Gate Count ..... 26256 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... +2.3V to VDD
Data Retention Supply Voltage ..... 3.0V to 4.5V
Input Rise and Fall Time ..... 40ns Max.
SEU Immunity Operating Temperature Range ..... -20°C to +80°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VDD = 4.5V, IO = -5.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.4	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, IO = 8.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VDD = 5.5V, $\overline{E}$ = 5.5V, VO = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10.0	10.0	µA
Input Leakage Current	II	VDD = 5.5V, VI = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	1.0	µA
Standby Supply Current	IDDSB1	VDD = 5.5V, IO = 0mA, $\overline{E}$ = VDD-0.3V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	200	µA
Standby Supply Current	IDDSB2	VDD = 5.5V, IO = 0mA, $\overline{E}$ = 2.3V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	500	µA
Operating Supply Current	IDDOP	VDD = 5.5V, (Note 2), f = 1MHz, $\overline{E}$ = 0.8V, VI = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	6	mA
Data Retention Supply Current	IDDDR	VDD = 3.0V, IO = 0mA, $\overline{E}$ = VDD-0.3V, VI = VDD or GND	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	100	µA
Enable Supply Current	IDDEN	VDD = 5.5, IO = 0mA, E = 0.8V, VI = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	200	µA
Functional Test	FT	VDD = 4.5V (Note 3)	7, 8A, 8B	-55°C ≤ T_A ≤ +125°C	-	-	-

NOTE:

1. All voltages referenced to device GND. Negative undershoots to a minimum of -0.3V are allowed with a maximum of 50ns pulse width.
2. Typical derating = 6mA/MHz increase in IDDOP.
3. Tested as follows: f = 3MHz, VIH = 4.5V, VIL = 0V, IOH = -4.0mA, IOL = 4.0mA, VOH ≤ 1.5V, and VOL ≤ 1.5V.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

PARAMETERS	SYMBOL	CONDITIONS	(NOTES 1,2,3) GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Access Time	(2) TAVQV	VDD = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	165	ns
Chip Enable to End of Write	(3) TELWH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	175	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Guaranteed and 100% Tested.

PARAMETERS	SYMBOL	CONDITIONS	(NOTES 1,2,3) GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable Access Time	(4) TELQV	VDD = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	175	ns
Address Hold Time	(5) TWHAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	0	-	ns
Address Setup Time	(6) TAVWL	VDD = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	10	-	ns
Address Valid to End of Write	(7) TAVWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	175	-	ns
Address Setup Time	(8) TAVEL	VDD = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	0	-	ns
Address Hold Time	(9) TEHAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	0	-	ns
Address Valid to End of Write	(10) TAVEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	175	-	ns
Write Enable Pulse Width	(11) TWLWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	175	-	ns
Data Setup Time	(12) TDVWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	165	-	ns
Data Hold Time	(13) TWHDX	VDD = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	15	-	ns
Enable Pulse Width	(14) TELEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	175	-	ns
Write to End of Write	(15) TWLEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	165	-	ns
Data Setup Time	(16) TDVEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	165	-	ns
Data Hold Time	(17) TEHDX	VDD = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	15	-	ns

NOTES:

1. All voltages referenced to device GND. Negative undershoots to a minimum of -0.3V are allowed with a maximum of 50ns pulse width.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V to VDD-1.5; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL ≥ 50pF; for CL > 50pF, access times are derated 0.15ns/pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS, AC AND DC

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz	1, 2, 4	$T_A = +25^{\circ}C$	-	8	pF
			1, 3, 4	$T_A = +25^{\circ}C$	-	TBD	pF
Output Capacitance	CO	VDD = Open, f = 1MHz	1, 2, 4	$T_A = +25^{\circ}C$	-	10	pF
			1, 3, 4	$T_A = +25^{\circ}C$	-	TBD	pF
Read/Write	(1) TAVAX	VDD = 4.5V and 5.5V	1	$-55^{\circ}C \le T_A \le +125^{\circ}C$	175	-	ns
Write Enable to Output in High Z	(18) TWLQZ	VDD = 4.5V and 5.5V	1	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	30	ns
Write Enable High to Output ON	(19) TWHQX	VDD = 4.5V and 5.5V	1	$-55^{\circ}C \le T_A \le +125^{\circ}C$	5	-	ns
Chip Enable to Output ON	(20) TELQX	VDD = 4.5V and 5.5V	1	$-55^{\circ}C \le T_A \le +125^{\circ}C$	5	-	ns
Output Enable High to Output High Z	(21) TEHQZ	VDD = 4.5V and 5.5V	1	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	30	ns
Chip Disable to Output Hold Time	(22) TEHQX	VDD = 4.5V and 5.5V	1	$-55^{\circ}C \le T_A \le +125^{\circ}C$	15	-	ns
Address Invalid Output Hold Time	(23) TAXQX	VDD = 4.5V and 5.5V	1	$-55^{\circ}C \le T_A \le +125^{\circ}C$	10	-	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS, AC AND DC (Continued)

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH2	VDD = 4.5, IO = -100µA	1	-55°C ≤ T_A ≤ +125°C	VDD-0.4V	-	V
Cycle Time	TAVAX	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	175	-	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. Applies to DIP device types only.
3. Applies to Flatpack device types only.
4. All Measurements Referenced To Device Grounds

TABLE 4. POST 200K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The post irradiation test conditions and limits are the same as those listed in Tables 1 and 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Output Low Voltage	VOL	± 60mV
Output High Voltage	VOH	± 400mV
Input Leakage Current	IIL	± 100nA
	IIH	±100nA
Low Impedance Output Leakage Current	IOZL	±1µA
High Impedance Output Leakage Current	IOZH	±1µA
Standby Supply Current	IDDSB1	±30µA

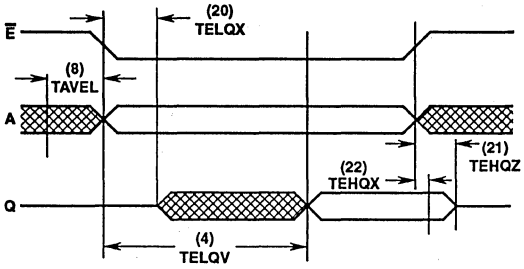
TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	-	-
Interim Test		100%/5004	1, 7, 9	1, 7, 9
PDA		100%/5004	1, 7, Δ	1
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B	N/A
	Others	Samples/5005	1, 7	N/A
Group C (Optional)		Samples/5005	N/A	1, 7
Group D (Optional)		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7	1, 7

Timing Waveforms

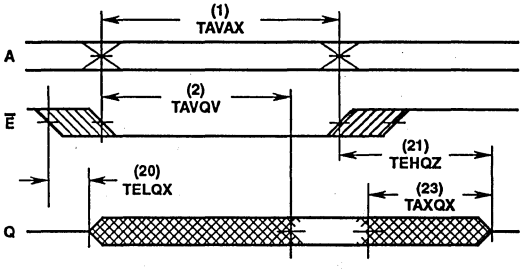
READ CYCLES

READ CYCLE 1: CONTROLLED BY E



NOTE: $\overline{W}$ is held high for entire cycle and D is ignored. Address is stable by the time $\overline{E}$ goes low and remains valid until E goes high.

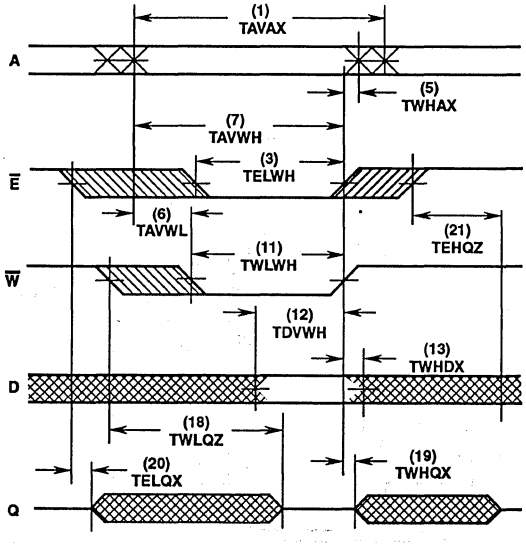
READ CYCLE 2: CONTROLLED BY ADDRESS



NOTE: $\overline{W}$ is high for the entire cycle and D is ignored. $\overline{E}$ stable prior to A becoming valid and after A becomes invalid.

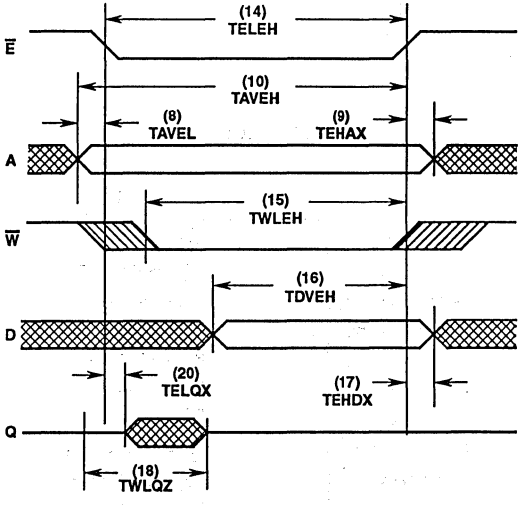
WRITE CYCLES

WRITE CYCLE 1: CONTROLLED BY $\overline{W}$ (LATE WRITE



NOTE: In this mode, $\overline{E}$ rises after $\overline{W}$. The address must remain stable whenever both $\overline{E}$ and $\overline{W}$ are low.

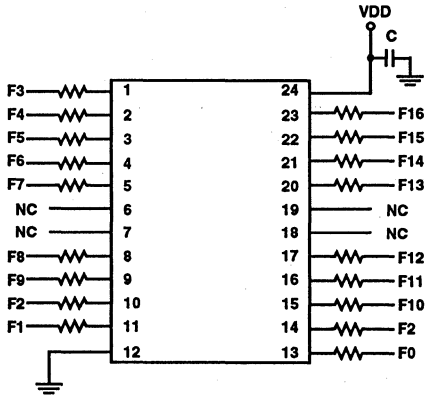
WRITE CYCLE 2: CONTROLLED BY $\overline{E}$ (EARLY WRITE)



NOTE: In this mode, $\overline{W}$ rises after $\overline{E}$. If $\overline{W}$ falls before $\overline{E}$ by a time exceeding TWLQZ (Max) TELQX (Min), and rises after $\overline{E}$ by a time exceeding TEHQZ (Max) - TWHQZ (Min), then Q will remain in the high impedance state throughtout the cycle.

Burn-In Circuits

HS-65C262RH 24 PIN FLATPACK

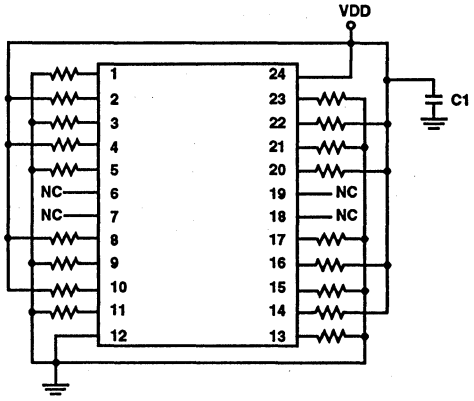


DYNAMIC CONFIGURATION

NOTES:

All Resistors = 47kΩ ± 10%
F0 = 100kHz ± 10%
F1 = F0/2 = F1/2; F3 = F2/2; F4 = F3/2 . . . F16 = F15/2
VDD = 6.0V ± 0.5V
VIH = 4.5V ± 10%
VIL = -0.2V to +0.8V
C = 0.01µf (min)

HS-65C262RH 24 PIN FLATPACK

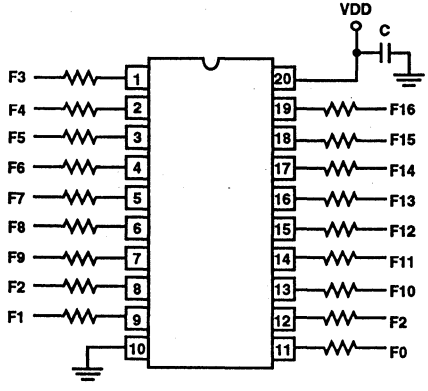


STATIC CONFIGURATION

NOTES:

All Resistors = 47kΩ ± 10%
VDD = 6.0V ± 0.5V
C1 = 0.01µf (min)

HS-65C262 20 PIN DIP

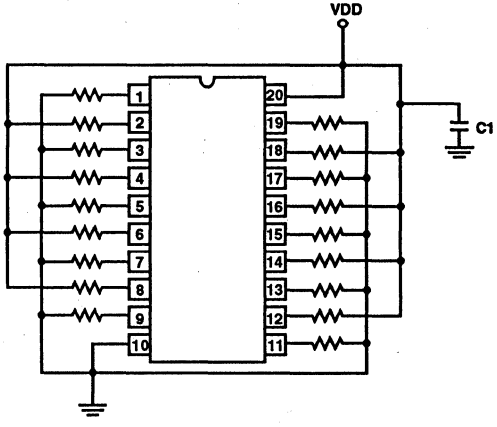


DYNAMIC CONFIGURATION

NOTES:

All Resistors = 47kΩ ± 10%
F0 = 100kHz ± 10%
F1 = F0/2 = F1/2; F3 = F2/2; F4 = F3/2 . . . F16 = F15/2
VDD = 6.0V ± 0.5V
VIH = 4.5V ± 10%
VIL = -0.2V to +0.8V
C = 0.01µf (min)

HS-65C262RH 20 PIN DIP



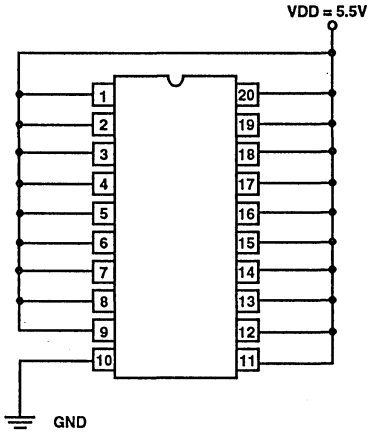
STATIC CONFIGURATION

NOTES:

All Resistors = 47kΩ ± 10%
VDD = 6.0V ± 0.5V
C1 = 0.01µf (min)

Irradiation Circuits

HS-65C262RH AND HS-65T262RH 20 PIN DIP



NOTES:

Pin 10 is tied to GND
Output (Pin 8) floats
All other pins tied to VDD
VDD = 5.5V

Harris - Space Level (-Q) Product Flow (Note 1)

SEM - Traceable to Diffusion Method 2018
Wafer Lot Acceptance Method 5007
Internal Visual Inspection Method 2010, Condition A
Gamma Radiation Assurance Tests Method 1019
Nondestructive Bond Pull Method 2023
Customer Pre-Cap Visual Inspection (Note 2)
Temperature Cycling Method 1010, Condition C
Constant Acceleration Method 2001, Condition E Min, Y1
Particle Impact Noise Detection Method 2020, Condition A
Electrical Tests (Harris' Option)
Serialization
X-Ray Inspection Method 2012
Electrical Tests - Subgroup 1; Read and Record (T0)
Static Burn-In Method 1015, Condition B, 72 Hrs, +125°C Min.
Interim 1 Electrical Tests - Subgroup 1; Read and Record (T1)
Burn-In Delta Calculation (T0 -T1)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Dynamic Burn-In Method 1015, Condition D, 240 Hrs, +125°C (Note 3)
Interim 2 Electrical Tests - Subgroup 1; Read and Record (T2)
Alternate Group A - Subgroups 1, 7, 9; Method 5005; Para 3.5.1.1
Burn-In Delta Calculation (T0 - T2)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Electrical Tests - Subgroup 3; Read and Record
Alternate Group A - Subgroups 3, 8B, 11; Method 5005; Para 3.5.1.1
Marking
Electrical Tests - Subgroup 2; Read and Record
Alternate Group A - Subgroups 2, 8A, 10; Method 5005; Para 3.5.1.1
Gross Leak Tests Method 1014, 100%
Fine Leak Tests Method 1014, 100%
Customer Source Inspection (Note 2)
Group B Inspection Method 5005 (Note 2)
End-Point Electrical Parameters: B-5 - Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11; B-6 - Subgroups 1, 7, 9
Group D Inspection Method 5005 (Notes 2, 4)
End-Point Electrical Parameters: Subgroups 1, 7, 9
External Visual Inspection Method 2009
Data Package Generation (Note 5)

NOTES:

1. The notes of Method 5004, Table 1 shall apply; Unless Otherwise Specified.
2. These steps are optional, and should be listed on the individual purchase order(s), when required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table 1 of Method 1015.
4. For Group D, Subgroup 3 inspection of package configurations which utilizes a gold plated lid in its construction; the inspection criteria for illegible markings criteria of Method 1010, paragraph 3.3 and of Method 1004, paragraph 3.8.a shall not apply.
5. Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (Including SEM Report)
   X-Ray Report and Film
   Test Variables Data

Harris -8 Product Flow

Internal Visual Inspection
Gamma Radiation Assurance Tests Method 1019
Customer Pre-Cap Visual Inspection (Note 1)
Temperature Cycling Method 1010, Condition C
Fine and Gross Leak Tests Method 1014
Constant Acceleration Method 2001 Y1 30KG
Initial Electrical Tests
Dynamic Burn-In Method 1015, Condition D, 160 Hrs, +125°C
+25°C Electrical Tests - Subgroups 1, 7, 9
PDA Calculation 5% Subgroups 1, 7
Electrical Tests +125°C, -55°C
Group A Inspection Method 5005. 5% PDA (Note 3)
Brand
Customer Source Inspection (Note 1)
Group C Inspection Method 5005 (Notes 1, 2)
Group D Inspection Method 5005 (Notes 1, 2)
External Visual Inspection Method 2009
Data Package Generation (Note 4)

NOTES:

1. These steps are optional, and must be negotiated as part of order.
2. Group B and D data package contains Attributes Data plus Variables Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable.
4. '-8' Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Radiation Testing Certificate of Conformance
   Certificate of Conformance (as found on shipper)

Metallization Topology

DIE DIMENSIONS:
258 x 177 x 19 ± 1mils

METALLIZATION:
Type: Si - Al
Thickness: 13kÅ ± 1.5kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

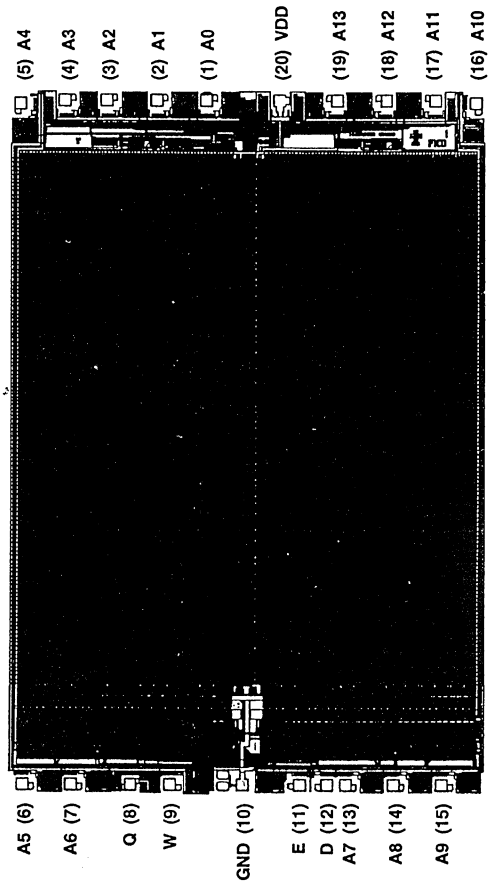
DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Braze Seal DIP - 460°C (Max)
Braze Seal Flatpack - 460°C (Max)

WORST CASE CURRENT DENSITY:
1.6×10^5 A/cm^2

SUBSTRATE POTENTIAL: VDD

Metallization Mask Layout

HS-65C262 AND HS-65T262RH



HARRIS SEMICONDUCTOR

CMM6167

High Reliability, Radiation Hardened CMOS 16,384 Word by 1 Bit Static RAM

December 1992

Features

- Aerospace Class S Screening
- Radiation Hardened to 100K Rads (Si)
- Cosmic Ray Upset Immunity Typically 2 x 10^{-9} Errors/Bit Day
- Latch Up Free Under Transient Radiation
- Transient Upset > 10^{10} RADS/s, 20ns Pulse
- Fast Access Time tAVQV = 95ns at T_A = +25°C, (Typ.)
- Single Power Supply 4.5V to 6.5V
- Low Standby and Operating Power
- All Inputs and Outputs TTL Compatible
- Fully Static Operation
- Tri-State Outputs

Description

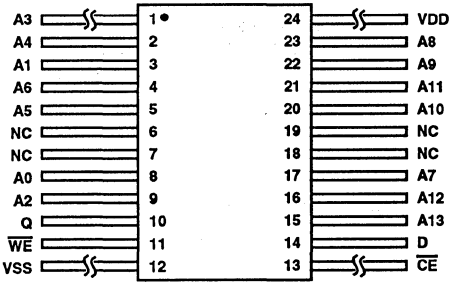
The CMM6167 is a high reliability 16,384 word by 1 bit static random access memory using CMOS/SOS technology. It is designed for use in memory systems where low power and simplicity in use are desirable.

CMOS/SOS technology permits operation in high radiation environments. It is insensitive to neutrons, cannot latch up at any dose rate and is resistant to single event upset caused by cosmic rays or heavy ions.

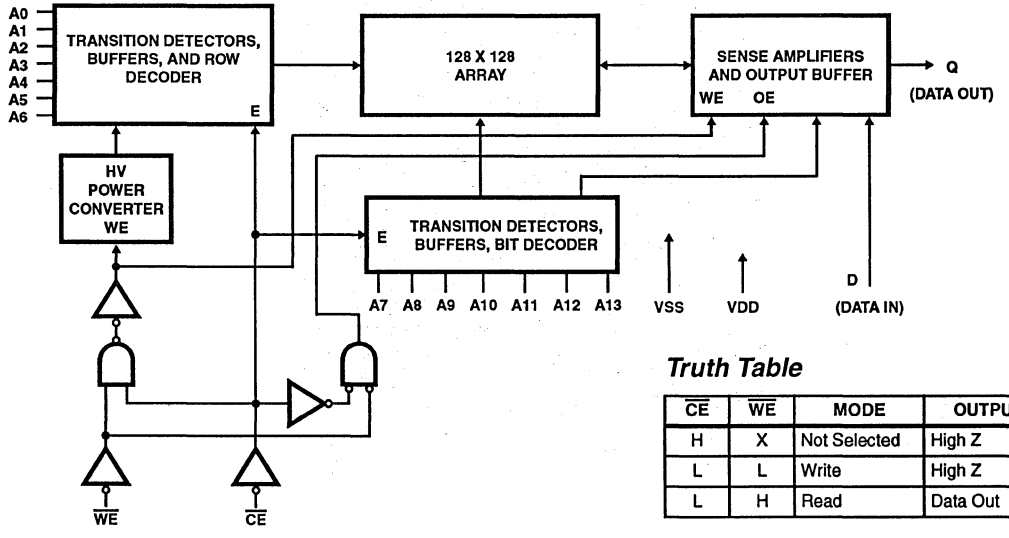
The CMM6167 is available in a 24 lead flatpack ceramic package (K suffix).

Pinout

24 LEAD CERAMIC FLATPACK
INTERNAL PACKAGE CODE "H9L"
TOP VIEW



Functional Diagram



Truth Table

$\overline{CE}$	$\overline{WE}$	MODE	OUTPUT
H	X	Not Selected	High Z
L	L	Write	High Z
L	H	Read	Data Out

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **1831.1**

Absolute Maximum Ratings

Supply Voltage (VDD)
All voltage values referenced to VSS terminal ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5 to VDD +0.5V
Input Current, Any One Input ..... ±10mA
DC Drain Current, Output (I/O) = -0.5V < VO < VDD +0.5V..... ±25mA
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10s)..... +265°C

Reliability Information

Maximum Package Power Dissipation
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearly at 12mW/°C to 200mW
Power Dissipation per Output Transistor
For T_A = Full Package Temperature Range 100mW
Operating Temperature Range (TA) ..... -55°C to +125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range (VDD) ..... +4.5V to +6.5V
Operating Temperature Range..... -55°C to +95°C
Input Low Voltage..... 0V to +1.5V
Input High Voltage (VIH)..... 3.5V to VDD
Data Retention Supply Voltage..... 2.5V
Input Rise and Fall Time..... 40ns Max.

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS VDD = 5V ± 5%, VIN = 0V or VDD, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	LIMITS				UNITS
			-55°C, +25°C		+95°C		
			MIN	MAX	MIN	MAX	
Quiescent Device Current	IDD	VIN = 0V or VDD, VCC = VDD	-	0.1	-	1.0	mA
Operating Device Current (Note 1)	IDD1	Cycle Time = 1µs	-	4.5	-	5	mA
Output (Sink) Current	IOL	VOUT = 0.4V	5.0	-	3.5	-	mA
Output (Source) Current	IOH	VOUT = VDD - 0.4V	-3	-	-2	-	mA
Input Low Voltage	VIL		-	1.5	-	1.5	V
Input High Voltage	VIH		3.5	-	3.5	-	V
Input Leakage Current	IIN	VIN = 0V or VDD	-	±2	-	±10	µA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VDD	-	±5	-	±30	µA
Minimum Data Retention Voltage	VDR		-	2	-	2.5	V
Data Retention Quiescent Current	IDDDR		-	40	-	400	µA

NOTES:
1. Operating current measured using 1MHz cycle with output open.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS VDD = 5V ± 5%

PARAMETER	SYMBOL	LIMITS				UNITS
		-55°C, +25°C		+95°C		
		MIN	MAX	MIN	MAX	
READ CYCLE TIMES						
Read Cycle	tAVAV	105	-	125	-	ns
Access from Address	tAVQV	-	105	-	125	ns
Access from $\overline{CE}$	tELQV	-	105	-	125	ns
WRITE CYCLE TIMES						
Write Cycle	tAVAV	130	-	145	-	ns
Write Pulse Width (Note 1)	tWLWH	100	-	115	-	ns
Write Recovery Time	tWHAX	10	-	10	-	ns
Address Set-Up to End of Write	tAVWH	120	-	135	-	ns
Address to $\overline{CE}$ Set Up Time	tAVEL	0	-	0	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS VDD = 5V ± 5% (Continued)

PARAMETER	SYMBOL	LIMITS				UNITS
		-55°C, +25°C		+95°C		
		MIN	MAX	MIN	MAX	
$\overline{CE}$ to End of Write	tELWH	120	-	135	-	ns
Data Set Up to End of Write	tDVWH	35	-	45	-	ns
Data Hold After End of Write	tWHDX	25	-	30	-	ns

NOTE:

1. $\overline{CE}$ and $\overline{WE}$ must overlap for at least tWLWH minimum value, tDVWH minimum value must occur during this overlap.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Note 1)

PARAMETER	SYMBOL	LIMITS				UNITS
		-55°C, +25°C		+95°C		
		MIN	MAX	MIN	MAX	
Output Voltage Low Level	VOL	-	0.1	-	0.2	V
Output Voltage High Level	VOH	VDD - 0.1	-	VDD - 0.2	-	V
Input Capacitance (Note 1)	CIN	-	5	-	5	pF
Output Capacitance (Note 1)	COUT	-	7	-	7	pF
Chip Enable to Output Active	tELQX	5	-	5	-	ns
Chip Enable to Output Disable	tEHQZ	-	40	-	50	ns
Output Hold After Address Change	tAXQX	5	-	5	-	ns
Address Set Up Before Write Low	tAVWL	0	-	0	-	ns

NOTE:

1. Capacitance measurements are made with no bias applied.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			POST RADIATION +25°C		
			MIN	MAX	
Quiescent Device Current	IDD	VIN = 0V or VDD, VCC = VDD	-	4	mA
Operating Device Current (Note 2)	IDD1	Cycle Time = 1µs	-	7.5	mA
Output (Sink) Current	IOL	VOUT = 0.4V	5	-	mA
Output (Source) Current	IOH	VOUT = VDD - 0.4V	-3	-	mA
Input Low Voltage	VIL		-	1.5	V
Input High Voltage	VIH		3.5	-	V
Input Leakage Current	IIN	VIN = 0V or VDD	-	±2	µA
Tri-State Output Leakage Current	IOZ	Applied Voltages = 0V or VDD	-	±50	µA
Minimum Data Retention Voltage	VDR		-	2.5	V
Read Cycle Time	tAVAV		125	-	ns
Address Access Time	tAVQV		-	125	ns

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	LIMITS POST RADIATION +25°C MIN	LIMITS POST RADIATION +25°C MAX	UNITS
Chip Enable Access Time	tELQV		-	125	ns
Write Cycle Time	tAVAV		145	-	ns
Write Pulse Width (Note 1)	tWLWH		115	-	ns
Write Recovery Time	tWHAX		10	-	ns
Address Set Up to End of Write	tAVWH		135	-	ns
Address to Chip Enable Set Up Time	tAVEL		0	-	ns
$\overline{CE}$ to End of Write	tELWH		135	-	ns
Data Set Up to End of Write	tDVWH		45	-	ns
Data Hold After End of Write	tWHDX		30	-	ns

NOTES:

1. $\overline{CE}$ and $\overline{WE}$ must overlap for at least tWLWH minimum value, tDVWH minimum value must occur during this overlap.
2. Operating current measured using 1MHz cycle with output open..

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

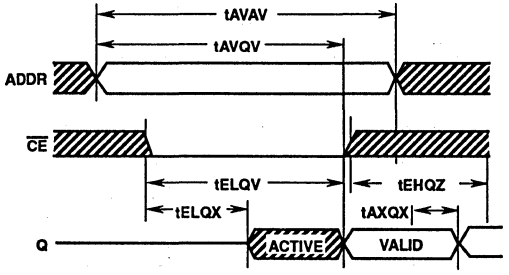
PARAMETER	SYMBOL	DELTA LIMITS
Quiescent Device Current	IDD	+30µA
Output Low Drive Current (Sink)	IOL	-15% of 0 hr. value
Output High Drive Current (Source)	IOH	-15% of 0 hr. value
Tri-State Output Leakage Current	IOZL	-500nA
Tri-State Output Leakage Current	IOZH	+500nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-IRZ SUBGROUPS	3 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9
Interim Test		100%/5004	1, 7, 9	N/A
PDA		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A
	Others	Samples/5005	1, 7	N/A
Group C (Optional)		Samples/5005	N/A	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group D (Optional)		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7, 9	1, 7, 9

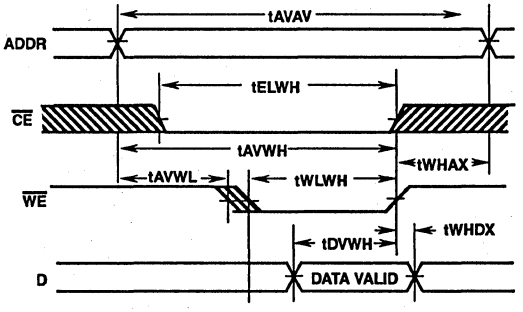
Timing Waveforms

READ CYCLE

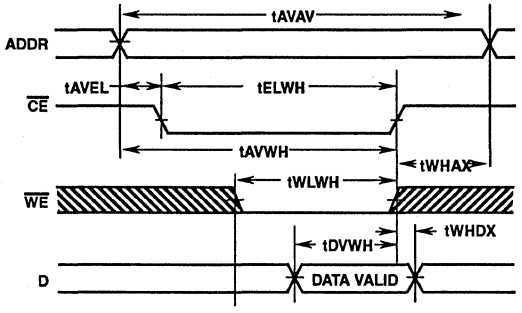


NOTE: $\overline{WE}$ is high during the Read Cycle
Timing measurement reference level is VDD/2

WRITE CYCLE NO 1 ($\overline{WE}$ CONTROLLED)

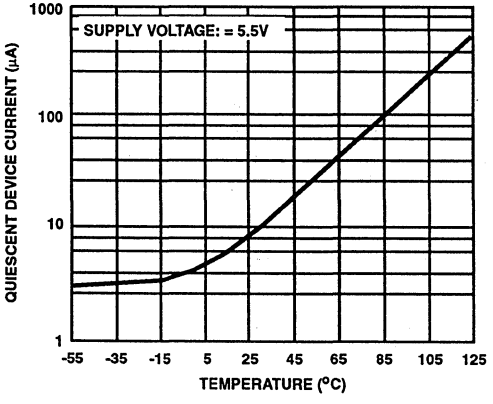


WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED)

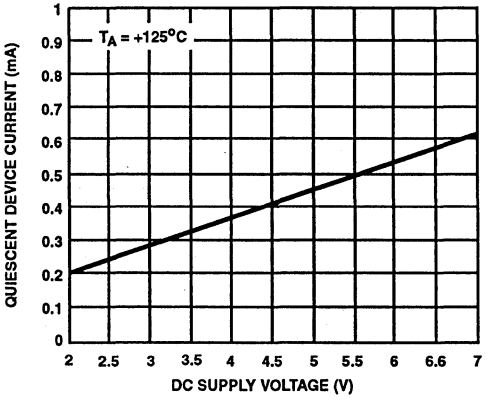


Typical Performance Curves

QUIESCENT DEVICE CURRENT vs AMBIENT TEMPERATURE

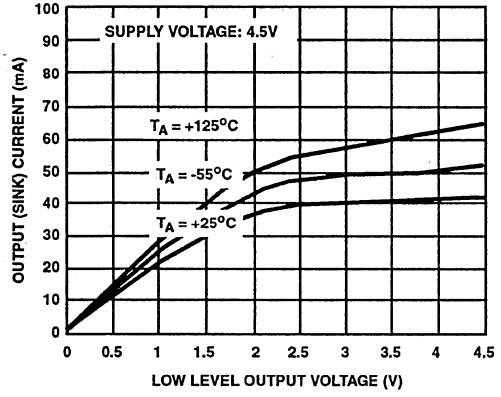


QUIESCENT DEVICE CURRENT vs DC SUPPLY VOLTAGE

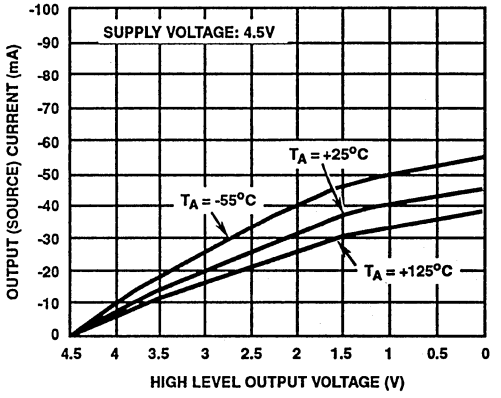


Typical Performance Curves (Continued)

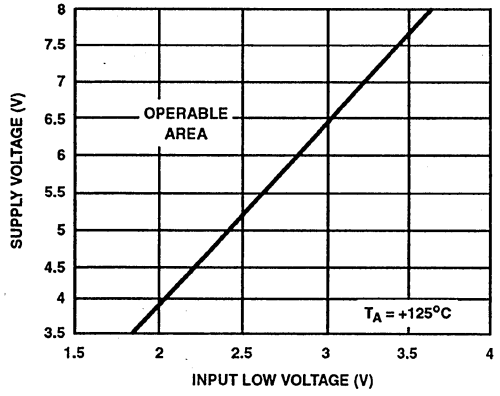
OUTPUT (SINK) CURRENT vs LOW LEVEL OUTPUT VOLTAGE



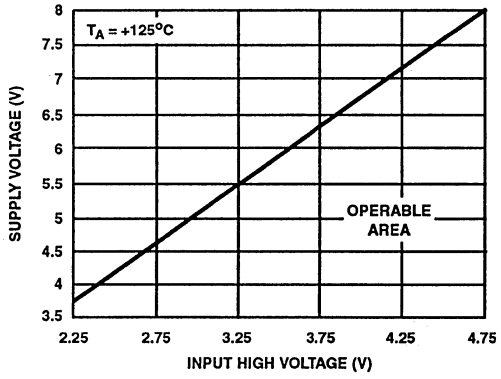
OUTPUT (SOURCE) CURRENT vs HIGH OUTPUT VOLTAGE LEVEL



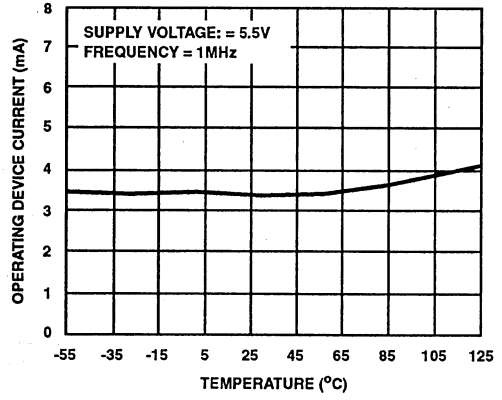
DC SUPPLY VOLTAGE vs INPUT LOW VOLTAGE



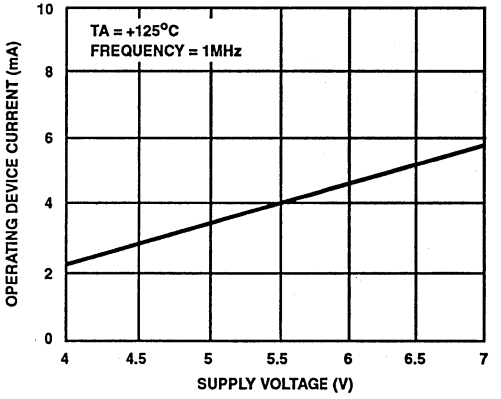
DC SUPPLY VOLTAGE vs INPUT HIGH VOLTAGE



OPERATING DEVICE CURRENT vs AMBIENT TEMPERATURE



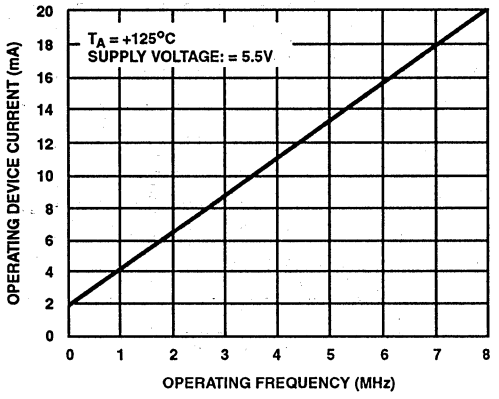
OPERATING DEVICE CURRENT vd DC SUPPLY VOLTAGE



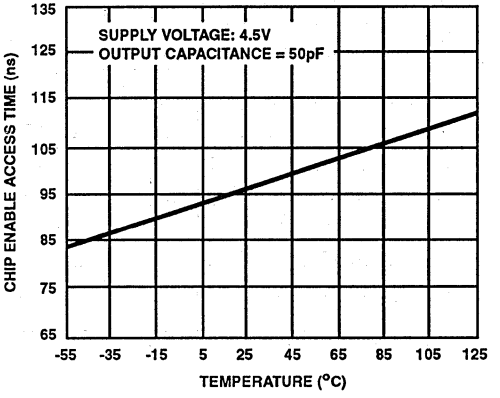
8 MEMORIES

Typical Performance Curves (Continued)

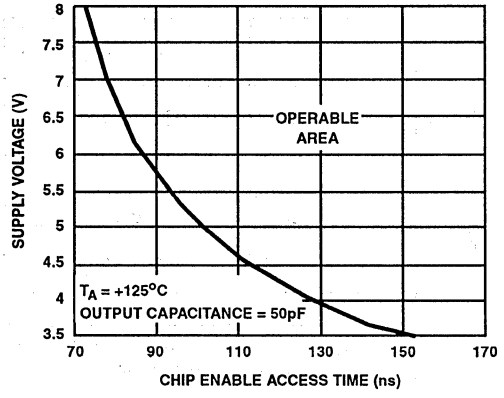
OPERATING DEVICE CURRENT vs OPERATING FREQUENCY



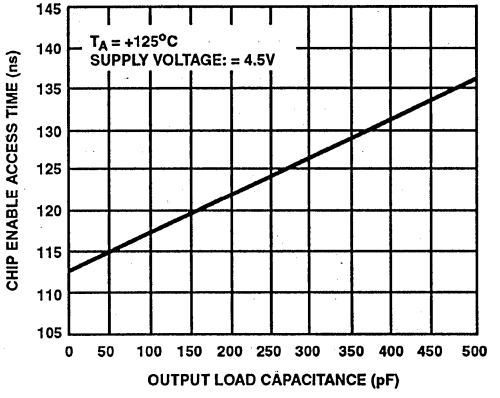
CHIP ENABLE ACCESS TIME vs AMBIENT TEMPERATURE



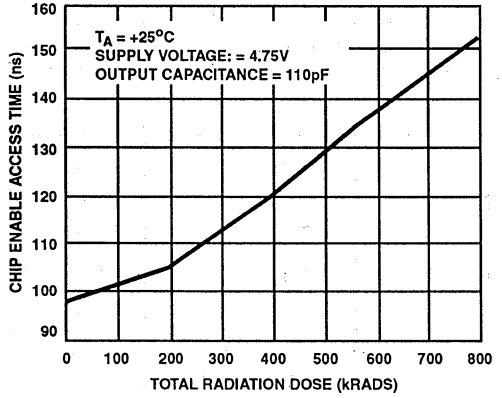
DC SUPPLY vs CHIP ENABLE ACCESS TIME



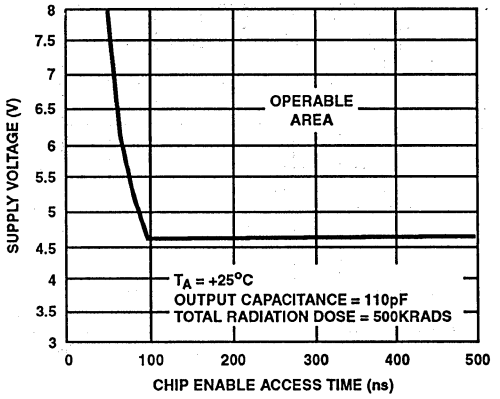
CHIP ENABLE ACCESS TIME vs OUTPUT LOAD CAPACITANCE



CHIP ENABLE ACCESS TIME s TOTAL RADIATION DOSE

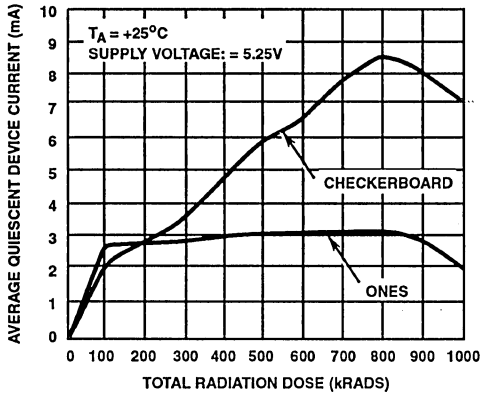


DC SUPPLY VOLTAGE vs CHIP ENABLE ACCESS TIME

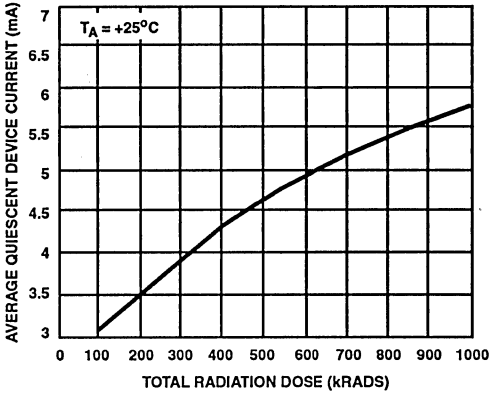


Typical Performance Curves (Continued)

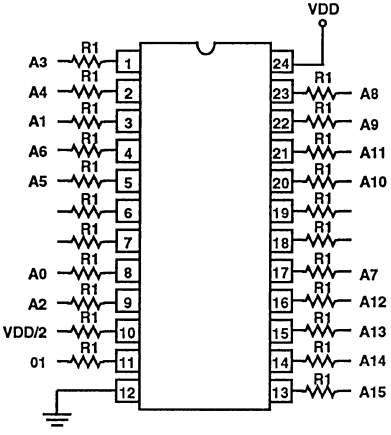
AVERAGE QUIESCENT DEVICE CURRENT vs TOTAL RADIATION DOSE



MINIMUM DC SUPPLY VOLTAGE vs TOTAL RADIATION DOSE

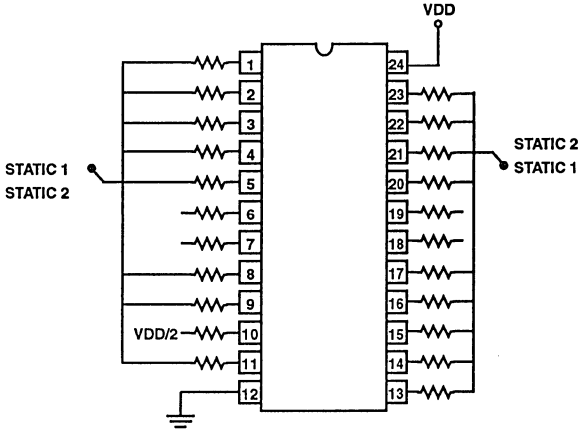


Burn-In Circuits



DYNAMIC CONFIGURATION

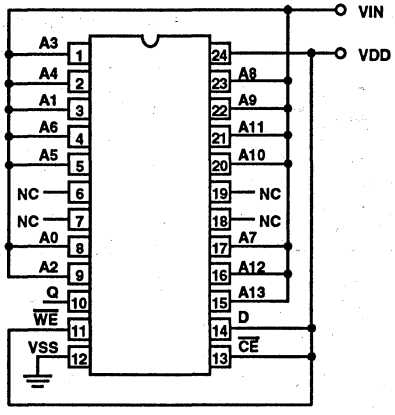
NOTES:
VDD = 6V (Min)
Resistors = 4.7kΩ ±5%
Frequency: A0 = 100kHZ ± 5%; A1 = A0/2 . . . A13 = A12/2;
01 = 200kHz ± 5%, 0.6µs low, 4.4µs high



STATIC CONFIGURATION

NOTES:
VDD = 6V (Min)
Resistors = 4.7kΩ ±5%
Notes:
Static Burn-In 1 memory array pre-initialized with all HIGHS at VDD, VIN = VDD
Static Burn-In 2 memory array pre-initialized with all LOWS at VSS, VIN = VSS

Irradiation Circuit



VIN = 5V OR VIN = 0V
VDD = 5V

Harris - IRZ Product Flow

Wafer Lot Acceptance Method 5007 (Includes SEM)

Radiation Verification (Each Wafer) Method 1019, 100K RADS(Si) Total Dose 2 Samples/Wafer, 0 Reject

Nondestructive Bond Pull Method 2023

Internal Visual (100%) Method 2010 (See "Visual Inspection")

Stabilization Bake (100%) Method 1008, Condition C, 24 Hrs Min., +150°C Min

Temperature Cycling (100%) Method 1010, Condition C, -65°C to +150°C

Constant Acceleration (100%) Method 2001, Condition E, Y1 (30,000g)

Particle Impact Noise Detection Method 2020, Condition A, 20g Peak at 60Hz

Visual Inspection (100%)

Serialization (100%)

Initial Electrical Tests (100%)

High Temperature Stress (100%) 48 Hrs, +125°C

Interim 1 Electrical Tests (100%), PDA 10% All Tests

Static Burn-In I (100%) 24 Hrs, +125°C

Interim 2 Electrical Tests (100%) (Note 1)

Static Burn-In 2 (100%) 24 Hrs, +125°C

Interim 3 Electrical Tests (100%) (Note 1)

Dynamic Burn-In (100%) 240 Hrs, +125°C

Interim 4 Electrical Tests (100%) PDA 5% All Tests, PDA 3% Functional

Fine and Gross Seal (100%) Method 1014

Final Electrical Tests (100%)

Radiographic (100%) Method 2012 (1 View)

External Visual (100%) Method 2009

Quality Conformance
- Group A (All Tests) Method 5005 (Class S)
- Group B (Optional) Method 5005 (Class S)
- Group D (Optional) Method 5005 (Class S)

CSI and/or GSI (Optional)

NOTES:

1. Failures from Interim Electrical Tests 2 and 3 are combined for determining PDA (PDA = 5% All Tests, 3% Functional)

Visual Inspection

Visual Inspection for Class S is performed to MIL-STD-883, Method 2010, Condition A **except** as follows:

Use:

3.2.1.1 - Metallization Scratches

3.2.1.2 - Metallization Voids

3.2.1.6 - Metallization Bridging

3.2.1.7 - Metallization Alignment

3.2.3 - Scribing and Die Defects. In addition, semicircular cracks that point away from the active circuit area are acceptable

3.2.3c - A crack that exceeds 5 mils in length must also point towards or cross a scribe grid line

3.1.7b - Lifting or Peeling of Glassivation, add Note of 3.2.7b to 3.1.7b

NOTES:

1. High magnification inspection is performed at 200X to 300X and applies to the high current areas of the chip. The remainder of the chip is inspected at 75X to 150X where high magnification is required.
2. Criteria 3.2.1.1a Metallization Scratches, and 3.2.1.2a Metallization Voids shall also apply to metallization over a passivation step (3.2.1.1d, 3.2.1.2b). Underlying oxide must also be exposed.
3. Criteria 3.2.1.7 Metallization Alignment and 3.1.2 Diffusion and Passivation Faults are applied to the center and two opposite corners of the chip. Areas of sufficient complexity are viewed to assure general alignment and contact coverage and shall consist only of the area exposed to the immediate field of view.
4. SOS Technology Devices
   - Diffusion faults 3.1.2.1 are not applicable. SOS devices are inspected for complete islands, bridging between islands and missing adjacent contacts from a row in a contact chain.
   - The 1 mil wire clearance criteria is not applicable
   - Passivation faults are not applicable when a second free flow oxide is used prior to metallization
   - Oxide gate bridge inspection is not applicable
   - Semicircular cracks not in an active area which start and end at the pellet edge are acceptable

Harris - 3Z Product Flow

Radiation Verification (Each Wafer) Method 1019, 100KRADS(Si) Total Dose 2 Samples/Wafer, 0 Reject (3Z Product Flow continues below)

Harris - 3 Product Flow (Without Radiation Verifications)

Internal Visual (100%) Method 2010, Condition B (Modified) (See "Internal Visual Inspection Modified for LSI")

Pre-Seal Bake (100%)

Stabilization Bake (100%) Method 1008, Condition C, 24 Hrs, +25°C , No End Point Measurements Required

Temperature Cycling (100%) Method 1010, Condition C

Constant Acceleration (100%) Method 2001, Condition E, Y1, Direction, Centrifuge

Seal:
- Fine (100%) Method 1014, Condition A or B
- Gross (100%) Method 1014, Condition C

Initial Electrical Tests (100%) Per Applicable Device Specification, +25°C

High Temperature Stress (100%) 48 Hrs, +125°C

Interim Electrical Tests 1 (100%) Per Applicable Device Specifications, +25°C PDA 10%, All Tests

Static Burn-In (100%) 160 Hrs, +125°C

Interim Electrical Tests 2 (100%) Per Applicable Device Specifications, +25°C PDA 5%, All Tests, PDA 3% Functional

Final Electrical Tests (100%) Per Applicable Device Specifications, +25°C

External Visual (100%) Method 2009

Quality Conformance
- Group A (All Tests) Method 5005 (Class B)
- Group B (Optional) Method 5005 (Class B)
- Group C (Optional) Method 5005 (Class B)
- Group D (Optional) Method 5005 (Class B)

Internal Visual Inspection Modified for LSI

Internal Visual Inspection is performed to MIL-STD-883, Method 2010, Condition B **except** as follows:

A. **High Magnification Inspection** is performed at 200X to 300X and applies to the high current areas of the chip. The remainder of the chip is inspected at 75X to 150X where high magnification is required

B. **Metallization Voids** (3.2.1.2) Criteria 3.2.1.1a Metallization Scratches and 3.2.1.2a Metallization Voids shall also apply to metallization over a passivation step (3.2.1.1d, 3.2.1.2b). Underlying oxide must also be exposed

C. **Metallization Alignment** (3.2.1.7) Diffusion and Passivation Layer(s) Faults (3.2.0)

High magnification inspection is performed at 200X to 300X, applied to the center and two opposite corners of the chip, consisting only of the area exposed to the immediate field of view

D. **Scribing and Die Defects** (3.2.3) in addition:

A crack that exceeds 5 mils in length must also point towards or cross a scribe grid line to be unacceptable

Semicircular cracks that point away from the active circuit area are acceptable

E. **SOS Technology Devices:**

- Diffusion faults are not applicable. SOS devices are inspected for complete islands, bridging between islands and missing adjacent contacts from a row in a contact chain.
- The 1 mil wire clearance criteria is not applicable
- Passivation faults are not applicable when a second free flow oxide is used prior to metallization
- Oxide gate bridge inspection is not applicable
- Semicircular cracks not in an active area which start and end at the pellet edge are acceptable

HARRIS SEMICONDUCTOR

HS-6504RH

Radiation Hardened 4096 x 1 CMOS RAM

December 1992

Features

- Total Dose 1 x 10^5 RAD (Si)
- Data Upset > 10^8 RAD (Si)/s
- Latch-Up Free To > 1 x 10^{12} RAD (Si)/s
- Low Power Standby 1100μW Max
- Low Power Operation 38.5mW/MHz Max
- Fast Access Time 150ns Typ
- Extremely Low Speed Power Product
- Single Event Upset Immune Option
- TTL Compatible Output
- Three-State Outputs
- Standard JEDEC Pinout
- 18 Pin Package for High Density
- On-Chip Address Register
- Military Temperature Range -55°C to +125°C

Description

The HS-6504RH is a synchronous 4096 x 1 static CMOS RAM fabricated using the radiation hardened guard band, self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

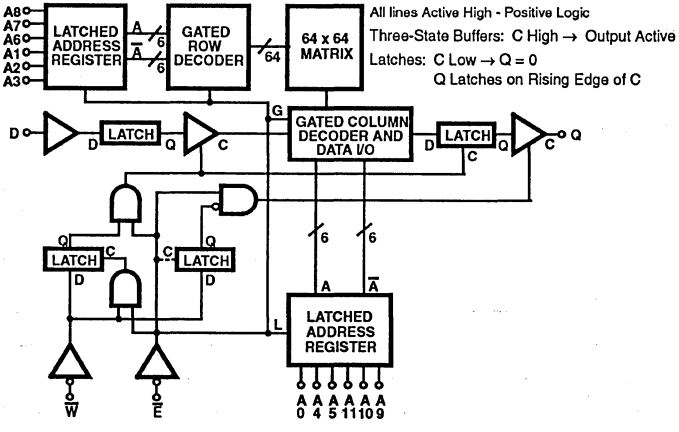
Latch-up free operation is achieved by the use of epitaxial starting material to eliminate the parasitic SCR effect seen in conventional bulk CMOS devices. On-chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory arrays.

The HS-6504RH is a fully static RAM and may be maintained in any state for an indefinite period of time. A single event upset immune version of the HS6504RRH is also offered. See page 11-5.

JAN

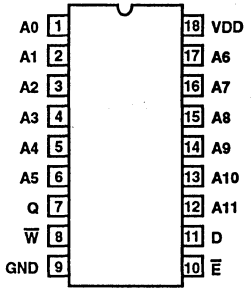
On January 28, 1987, Harris received JAN line certification as a Rad-Hard Class S fabrication facility for the HS-6504RH. Specifications can be found in JAN 38510/245 under device type 03.

Functional Diagram

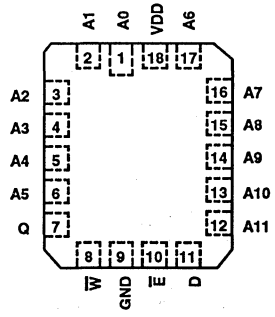


Pinouts

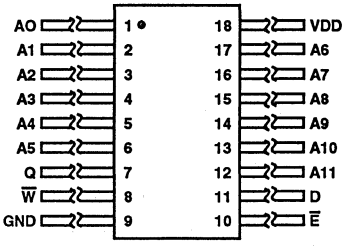
HS1-6504RH 18 PIN CERAMIC DIP
CASE OUTLINE D-6, CONFIGURATION 3
TOP VIEW



HS4-6504RH 18 PIN LCC
INTERNAL PACKAGE CODE "HPQ"
TOP VIEW



HS9-6504RH 18 LEAD FLATPACK
INTERNAL PACKAGE CODE "HRF"
TOP VIEW



PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output

8 MEMORIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3028

Absolute Maximum Ratings

Supply Voltage -(VDD-GND) ..... -0.3 to +7.0V
Input or Output Voltage Applied ..... GND-0.3V to VDD +0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 3.0mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
18 Pin Ceramic DIP Package	73°C/W	10°C/W
18 Pin LCC Package	60°C/W	9°C/W
18 Lead Flatpack Package	62°C/W	10°C/W

Maximum Package Power Dissipation at +125°C
18 Pin Ceramic DIP Package 0.68W
18 Pin LCC Package 0.83W
18 Lead Flatpack Package 0.80W
Gate Count ..... 6667 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Rise and Fall Time ..... 40ns Max

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Standby Supply Current	IDDSB	IO = 0, VI = GND or VDD	-	200	µA
Operating Supply Current (Note 1)	IDDOP	f = 1MHz, IO = VI = VDD or GND	-	7	mA
Data Retention Supply Current	IDDDR		-	100	µA
Data Retention Supply Voltage	VDDDR		-	3.0	V
Input Leakage Current	II	GND ≤ VI ≤ VDD	-1.0	+1.0	µA
Output Leakage Current	IOZ	GND ≤ VO ≤ VDD	-10	+10	µA
Input Low Voltage	VIL		0.0	0.8	V
Input High Voltage All Except E and R/W	VIH		VDD -2.0	VDD	V
Input High Voltage E and R/W	VIH		VDD -1.5	VDD +0.3	
Output Low Voltage	VOL	IOL = 2.0mA	-	0.4	V
Output High Voltage	VOH	IOH = -1.0mA	2.4	-	V

NOTE:
1. Operating Supply Current (IDDOP) is proportional to Operating Frequency.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Chip Enable Access Time	TELQV	Note 1	-	200	ns
Address Access Time	TAVQV	Note 1	-	210	ns
Chip EnableTime	TELEH	Note 1	200	-	ns
Chip Disable Time	TEHEL	Note 1	50	-	ns
Address Setup Time	TAVEL	Note 1	10	-	ns
Address Hold Time	TELAX	Note 1	40	-	ns
Write Enable Pulse Width	TWLWH	Note 1	50	-	ns
Write Enable Setup Time	TWLEH	Note 1	200	-	ns
Early Write Pulse Setup Time	TWLEL	Note 1	0	-	ns
Write Enable Hold Time	TELWH	Note 1	50	-	ns
Data Setup Time	TDVWL	Note 1	10	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Early Write Data Setup Time	TDVEL	Note 1	0	-	ns
Data Hold Time	TWLDX	Note 1	50	-	ns
Early Write Data Hold	TELDX	Note 1	50	-	ns
Data Valid to Write Time	TQVWL	Note 1	0	-	ns

NOTE:

1. Inputs TRISE = TFALL ≤ 20nsec: Outputs : 1TTL load and 50pF. All timing measurements at 1/2 VDD.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Guaranteed but not tested)

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Input Capacitance	CI	VI = VDD or GND	-	8.0	pF
Output Capacitance	CO	VO = VDD or GND, f = 1MHz	-	10.0	pF
Chip Enable/Output Enable Time	TELQX	Note 1	5	-	ns
Chip Enable/Output Disable Time	TEHQZ	Note 1	-	50	ns
Read Mode Write Enable Setup Time	TWHEL	Note 1	0	-	ns
Read or Write Cycle Time	TELEL	Note 1	250	-	ns

NOTE:

1. Inputs TRISE = TFALL ≤ 20nsec: Outputs : 1TTL load and 50pF. All timing measurements at 1/2 VDD.

TABLE 4. POST RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The post irradiation test conditions and limits are the same as those listed in Tables 1 and 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Output Low Voltage	VOL	± 0.08V
Output High Voltage	VOH	± 0.48V
Input Leakage Current	II	± 0.20µA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9
Interim Test 1 and 2		100%/5004	1, 7, 9	N/A
PDA 1 and 2		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A
	Others	Samples/5005	1, 7	N/A
Group C (Optional)		Samples/5005	N/A	1, 7
Group D (Optional)		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7, 9	1, 7, 9

Specifications HS-6504RRH (S.E.U. Immune Option)

Absolute Maximum Ratings

Supply Voltage -(VDD-GND) ..... -0.3 to +7.0V
Input or Output Voltage Applied .....GND-0.3V to VDD +0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature..... +175°C
Lead Temperature (Soldering 10s)..... +300°C
Typical Derating Factor.....3.0mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
18 Pin Ceramic DIP Package	73°C/W	10°C/W
18 Pin LCC Package.....	60°C/W	9°C/W
18 Lead Flatpack Package	62°C/W	10°C/W

Maximum Package Power Dissipation at +125°C
18 Pin Ceramic DIP Package 0.68W
18 Pin LCC Package.....0.83W
18 Lead Flatpack Package 0.80W
Gate Count .....6667 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage Range..... +4.5V to +5.5V
Operating Temperature Range..... -20°C to +80°C
Input Rise and Fall Time..... 40ns Max

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Standby Supply Current	IDDSB	IO = 0, VI = GND or VDD	-	200	µA
Operating Supply Current (Note 1)	IDDOP	f = 1MHz, IO = VI = VDD or GND	-	7	mA
Data Retention Supply Current	IDDDR		-	100	µA
Data Retention Supply Voltage	VDDDR		-	3.0	V
Input Leakage Current	II	GND ≤ VI ≤ VDD	-1.0	+1.0	µA
Output Leakage Current	IOZ	GND ≤ VO ≤ VDD	-10	+10	µA
Input Low Voltage	VIL		0.0	0.8	V
Input High Voltage All Except E and R/W	VIH		VDD -2.0	VDD	V
Input High Voltage E and R/W	VIH		VDD -1.5	VDD +0.3	
Output Low Voltage	VOL	IOL = 2.0mA	-	0.4	V
Output High Voltage	VOH	IOH = -1.0mA	2.4	-	V

NOTE:

1. Operating Supply Current (IDDOP) is proportional to Operating Frequency.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable Access Time	TELQV	Note 1	-	200	ns
Address Access Time	TAVQV	Note 1	-	210	ns
Chip EnableTime	TELEH	Note 1	200	-	ns
Chip Disable Time	TEHEL	Note 1	50	-	ns
Address Setup Time	TAVEL	Note 1	10	-	ns
Address Hold Time	TELAX	Note 1	40	-	ns
Write Enable Pulse Width	TWLWH	Note 1	50	-	ns
Write Enable Setup Time	TWLEH	Note 1	200	-	ns
Early Write Pulse Setup Time	TWLEL	Note 1	0	-	ns
Write Enable Hold Time	TELWH	Note 1	50	-	ns
Data Setup Time	TDVWL	Note 1	10	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Early Write Data Setup Time	TDVEL	Note 1	0	-	ns
Data Hold Time	TWLDX	Note 1	50	-	ns
Early Write Data Hold	TELDX	Note 1	50	-	ns
Data Valid to Write Time	TQVWL	Note 1	0	-	ns

NOTE:

1. Inputs TRISE = TFALL ≤ 20nsec: Outputs : 1TTL load and 50pF. All timing measurements at 1/2 VDD.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Guaranteed but not tested)

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Input Capacitance	CI	VI = VDD or GND	-	8.0	pF
Output Capacitance	CO	VO = VDD or GND, f = 1MHz	-	10.0	pF
Chip Enable/Output Enable Time	TELQX	Note 1	5	-	ns
Chip Enable/Output Disable Time	TEHQZ	Note 1	-	50	ns
Read Mode Write Enable Setup Time	TWHEL	Note 1	0	-	ns
Read or Write Cycle Time	TELEL	Note 1	250	-	ns

NOTE:

1. Inputs TRISE = TFALL ≤ 20nsec: Outputs : 1TTL load and 50pF. All timing measurements at 1/2 VDD.

TABLE 4. POST RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The post irradiation test conditions and limits are the same as those listed in Tables 1 and 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

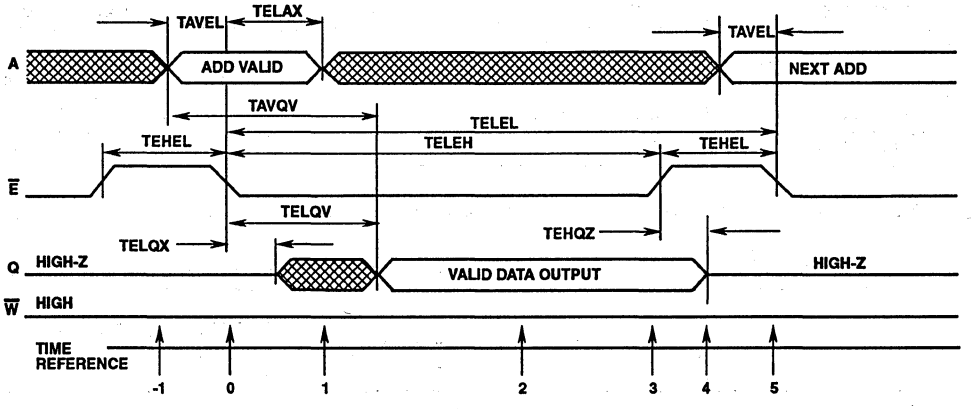
PARAMETER	SYMBOL	DELTA LIMITS
Output Low Voltage	VOL	± 0.08V
Output High Voltage	VOH	± 0.48V
Input Leakage Current	II	± 0.20µA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9
Interim Test 1 and 2		100%/5004	1, 7, 9	N/A
PDA 1 and 2		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A
	Others	Samples/5005	1, 7	N/A
Group C (Optional)		Samples/5005	N/A	1, 7
Group D (Optional)		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7, 9	1, 7, 9

Timing Waveforms

READ CYCLE



TRUTH TABLE

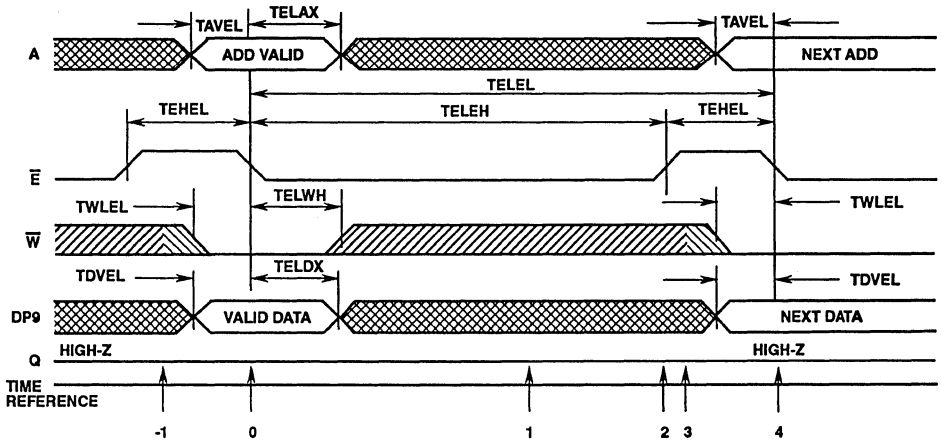
TIME REFERENCE	INPUTS			OUTPUT	FUNCTION
	$\overline{E}$	$\overline{W}$	A	Q	
-1	H	X	X	Z	Memory Disabled
0	↘	H	V	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	Output Enabled
2	L	H	X	V	Output Valid
3	↗	H	X	V	Read Accomplished
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but the data is not valid until during time (T = 2). $\overline{W}$ must remain high for the read cycle. After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and all input and ready the RAM for the next memory cycle (T = 4).

NOTE: In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

Timing Waveforms (Continued)

EARLY WRITE CYCLE



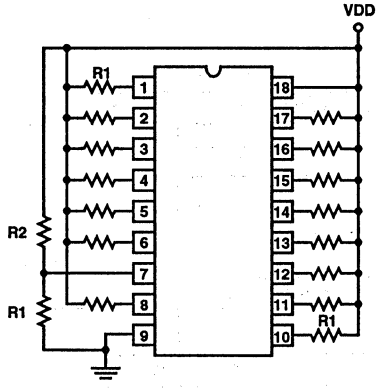
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	INPUTS $\overline{W}$	INPUTS A	INPUTS D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	Memory Disabled
0	↘	L	V	V	Z	Cycle Begins, Addresses are Latched
1	L	X	X	X	Z	Write in Progress Internally
2	↗	X	X	X	Z	Write Completed
3	H	X	X	X	Z	Prepare for Next Cycle (Same as - 1)
4	↘	L	V	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls determines the state of the output buffer for that cycle. Since $\overline{W}$ is low when $\overline{E}$ falls, the output buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; therefore data set up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state the output buffer and all inputs are disabled and all signals are unlatched. The device is now ready for the next cycle.

NOTE: In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

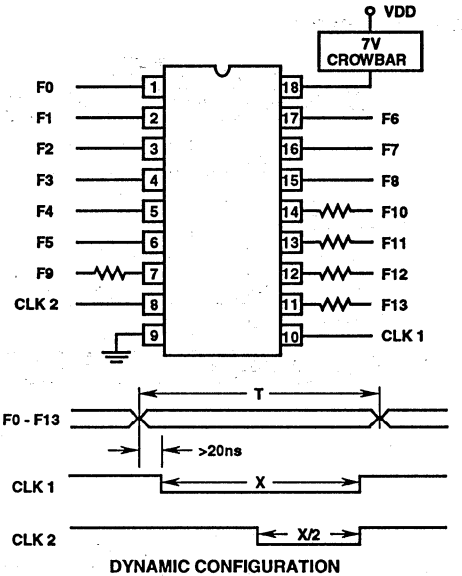
Burn-In Circuits



STATIC CONFIGURATION

NOTES:

VDD = 6.0V ± 0.5V
R1 = 1K
R2 = 1.5k
Minimum Ambient Temperature = +125°C

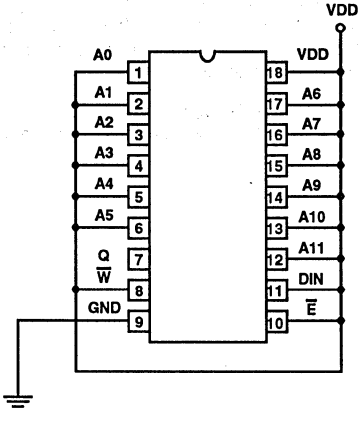


DYNAMIC CONFIGURATION

NOTES:

VDD = 6.0V ± 0.5V
All Resistors = 27KΩ
Minimum Ambient Temperature = +125°C
VDD must be applied before or at the same time as input signals
x > 700ns, T = 5µs
F0 = 100kHz
F1 = F0/2
F2 = F0/4
F3 = F0/8 . . . F13 = F0/8192

Irradiation Circuit



NOTES:

VDD = 5V
GND = 0V
All Inputs = 5V
All outputs float
MONITOR: IDD at 5V

Harris - Space Level (-Q) Product Flow (Note 1)

SEM - Traceable to Diffusion Method 2018
Wafer Lot Acceptance Method 5007
Internal Visual Inspection Method 2010, Condition A
Gamma Radiation Assurance Tests Method 1019
Nondestructive Bond Pull Method 2023
Customer Pre-Cap Visual Inspection (Note 2)
Temperature Cycling Method 1010, Condition C
Constant Acceleration Method 2001, Condition E Min, Y1
Particle Impact Noise Detection Method 2020, Condition A
Electrical Tests (Harris' Option)
Serialization
X-Ray Inspection Method 2012
Electrical Tests - Subgroup 1; Read and Record (T0)
Static Burn-In Method 1015, Condition B, 72 Hrs, +125°C Min.
Interim 1 Electrical Tests - Subgroup 1; Read and Record (T1)
Burn-In Delta Calculation (T0 -T1)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Dynamic Burn-In Method 1015, Condition D, 240 Hrs, +125°C (Note 3)
Interim 2 Electrical Tests - Subgroup 1; Read and Record (T2)
Alternate Group A - Subgroups 1, 7, 9; Method 5005; Para 3.5.1.1
Burn-In Delta Calculation (T0 - T2)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Electrical Tests - Subgroup 3; Read and Record
Alternate Group A - Subgroups 3, 8B, 11; Method 5005; Para 3.5.1.1
Marking
Electrical Tests - Subgroup 2; Read and Record
Alternate Group A - Subgroups 2, 8A, 10; Method 5005; Para 3.5.1.1
Gross Leak Tests Method 1014, 100%
Fine Leak Tests Method 1014, 100%
Customer Source Inspection (Note 2)
Group B Inspection Method 5005 (Note 2)
End-Point Electrical Parameters: B-5 - Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11; B-6 - Subgroups 1, 7, 9
Group D Inspection Method 5005 (Notes 2, 4)
End-Point Electrical Parameters: Subgroups 1, 7, 9
External Visual Inspection Method 2009
Data Package Generation (Note 5)

NOTES:

1. The notes of Method 5004, Table 1 shall apply; Unless Otherwise Specified.
2. These steps are optional, and should be listed on the individual purchase order(s), when required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table 1 of Method 1015.
4. For Group D, Subgroup 3 inspection of package configurations which utilizes a gold plated lid in its construction; the inspection criteria for illegible markings criteria of Method 1010, paragraph 3.3 and of Method 1004, paragraph 3.8.a shall not apply.
5. Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (Including SEM Report)
   X-Ray Report and Film
   Test Variables Data

Harris -8 Product Flow

Internal Visual Inspection
Gamma Radiation Assurance Tests Method 1019
Customer Pre-Cap Visual Inspection (Note 1)
Temperature Cycling Method 1010, Condition C
Fine and Gross Leak Tests Method 1014
Constant Acceleration Method 2001 Y1 30KG
Initial Electrical Tests
Dynamic Burn-In Method 1015, Condition D, 160 Hrs, +125°C
+25°C Electrical Tests - Subgroups 1, 7, 9
PDA Calculation 5% Subgroups 1, 7
Electrical Tests +125°C, -55°C
Group A Inspection Method 5005. 5% PDA (Note 3)
Brand
Customer Source Inspection (Note 1)
Group C Inspection Method 5005 (Notes 1, 2)
Group D Inspection Method 5005 (Notes 1, 2)
External Visual Inspection Method 2009
Data Package Generation (Note 4)

NOTES:

1. These steps are optional, and must be negotiated as part of order.
2. Group B and D data package contains Attributes Data plus Variables Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable.
4. '-8' Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Radiation Testing Certificate of Conformance
   Certificate of Conformance (as found on shipper)

Metallization Topology

DIE DIMENSIONS:
Die Size: 154 x 236 mils
Die Thickness: 14 ±1 mils

METALLIZATION:
Type: Al, 14kÅ ± 2kÅ
Back: Gold

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

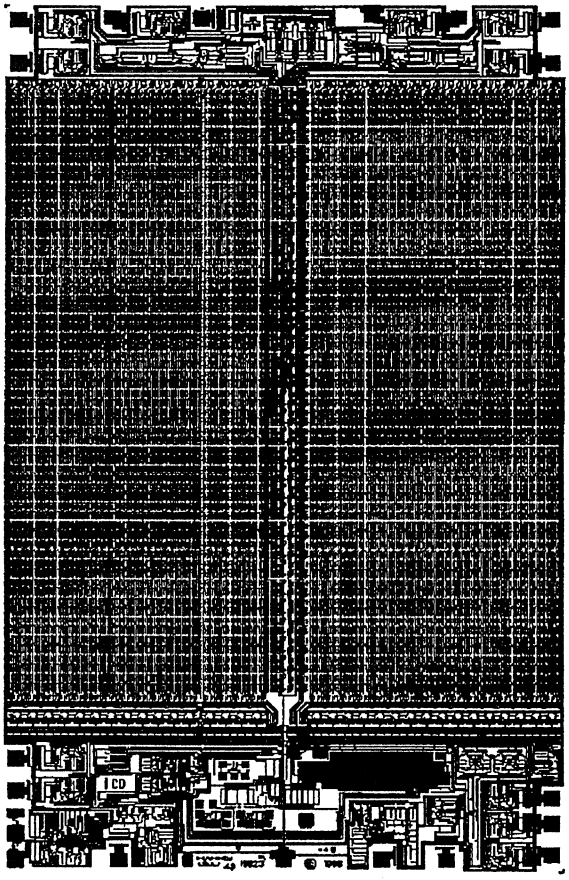
DIE ATTACH:
Material: Gold
Temperature: Sidebrazed Ceramic DIP - 460°C±10°C (Max)
Braze Seal Flatpack - 460°C ± 10°C (Max)

WORST CASE CURRENT DENSITY: 6.44×10^4 A/cm^2

SUBSTRATE POTENTIAL: VDD

Metallization Mask Layout

HS-6504RH



HARRIS SEMICONDUCTOR

CMM5104

Radiation Hardened, High Reliability, CMOS/SOS 4096 Word by 1 Bit LSI Static RAM

December 1992

Features

- Radiation Hardened to 100KRAD(Si)
- Cosmic Ray Upset Immunity Typically 2 x 10^{-9} Errors/Bit Day
- Latch Up Free Under Transient Radiation
- Transient Upset > 10^{10} RADS/s, 20ns Pulse
- Fully Static Operation
- Single Power Supply 4.5V to 6.5V
- All Inputs and Outputs TTL Compatible
- Tri-State Outputs
- Industry Standard 18 Pin Configuration
- Fast Access Time tAVQV = 200ns
- Low Standby and Operating Power

Description

The CMM5104 is a high reliability 4096 word by 1 bit static random access memory using CMOS/SOS technology. It is designed for use in memory systems where low power and simplicity in use are desirable.

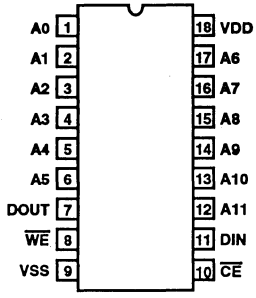
CMOS/SOS technology permits operation in high radiation environments. It is insensitive to neutrons, cannot latch up at any dose rate and is resistant to single event upset caused by cosmic rays or heavy ions.

TTL compatibility on all input and output terminals permits easy system integration. The data out signal has the same polarity as the input data. A separate data input and a separate tri-state output are used.

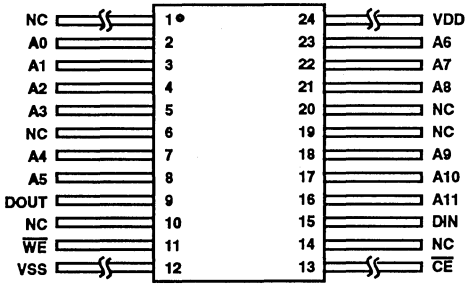
The CMM5104 is supplied in 18 lead dual-in-line sidebrazed ceramic package (D suffix). The part is also available in a 24 lead flatpack ceramic package (K suffix).

Pinout

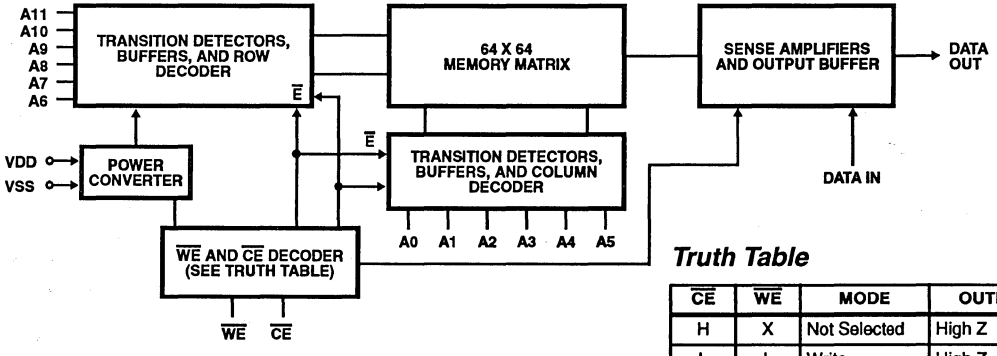
18 PIN CERAMIC DIP
CASE OUTLINE D6, CONFIGURATION 3
TOP VIEW



24 PIN FLATPACK
INTERNAL PACKAGE CODE "H9L"
TOP VIEW



Functional Diagram



Truth Table

CE	WE	MODE	OUTPUT
H	X	Not Selected	High Z
L	L	Write	High Z
L	H	Read	Data Out

8 MEMORIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3406

Absolute Maximum Ratings

Supply Voltage (VDD),
All voltage values referenced to VSS terminal ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5 to VDD +0.5V
Input Current, Any One Input ..... ±10mA
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +265°C
Typical Derating Factor ..... 3.0 mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Maximum Package Power Dissipation
For T_A = -55°C to +100°C 100mW
For T_A = +100°C to +125°C ..... Derate Linearly at 12mW/°C to 200mW
Power Dissipation per Output Transistor
For T_A = Full Package Temperature Range 100mW
Gate Count ..... 5400 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +6.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... VDD/2 to VDD
Data Retention Supply Voltage 2.5V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS VDD = 5V ± 5%, VIN = 0V or VDD, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	LIMITS				UNITS
			-55°C, +25°C		+125°C		
			MIN	MAX	MIN	MAX	
Quiescent Device Current	IDD	VIN = 0V or VDD, VCC = VDD	-	0.1	-	1.0	mA
Operating Device Current (Note 1)	IOPER	Cycle Time = 1µs	-	4.5	-	4.5	mA
Operating Device Current (Deselected)	IOPRD	Cycle Time = 1µs	-	0.1	-	1.0	mA
Output Low Drive (Sink) Current	IDN	VOUT = 0.4V	4.0	-	2.5	-	mA
Output High Drive (Source) Current	IDP	VOUT = VDD - 0.4V	3	-	2	-	mA
Input Low Voltage (Note 2)	VIL		-	0.8	-	0.8	V
Input High Voltage (Note 2)	VIH		VDD/2	-	VDD/2	-	V
Input Leakage Current	IIN	VIN = 0V or VDD	-	±2	-	±10	µA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VDD	-	±5	-	±30	µA
Minimum Data Retention Voltage	VDR		-	2	-	2.5	V
Data Retention Quiescent Current	IDDDR		-	40	-	400	µA

NOTES:
1. Operating current measured using 1MHz cycle and CL = 50pF.
2. Measured using 1MHz cycle.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS VDD = 5V ± 5%

PARAMETER	SYMBOL	LIMITS				UNITS
		-55°C, +25°C		+125°C		
		MIN	MAX	MIN	MAX	
READ CYCLE TIMES						
Read Cycle	tAVAV	200	-	250	-	ns
Access from Address	tAVQV	-	200	-	250	ns
Access from $\overline{CE}$	tELQV	-	220	-	280	ns
WRITE CYCLE TIMES						
Write Cycle	tAVAV	200	-	250	-	ns
Write Pulse Width (Note 1)	tWLWH	125	-	145	-	ns
Address Set Up to Beginning of Write	tAVWL	0	-	0	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS VDD = 5V ± 5% **(Continued)**

PARAMETER	SYMBOL	LIMITS				UNITS
		-55°C, +25°C		+125°C		
		MIN	MAX	MIN	MAX	
Address Set Up to End of Write	tAVWH	160	-	205	-	ns
Address Hold Time	tWHAV	40	-	45	-	ns
$\overline{CE}$ to Write Set Up Time	tELWH	160	-	205	-	ns
$\overline{CE}$ Pulse Width (Note 1)	tELEH	180	-	220	-	ns
Data to Write Set Up Time	tDVWH	100	-	120	-	ns
Data Hold From Write	tWHDX	5	-	10	-	ns

NOTE:

1. $\overline{CE}$ and $\overline{WE}$ must overlap for at least tWLWH minimum value, tDVWH minimum value must occur during this overlap.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Note 1)

PARAMETER	SYMBOL	LIMITS				UNITS
		-55°C, +25°C		+125°C		
		MIN	MAX	MIN	MAX	
Output Voltage Low Level	VOL	-	0.1	-	0.1	V
Output Voltage High Level	VOH	VDD - 0.1	-	VDD - 0.1	-	V
Input Capacitance (Note 2)	CIN	-	5	-	5	pF
Output Capacitance (Note 2)	COUT	-	7	-	7	pF
Output Hold From Address	tAVQZ	-	80	-	100	ns
Output Hold From $\overline{CE}$	tEHQZ	-	80	-	100	ns

NOTE:

1. Parameters in this table are not directly 100% tested, but are characterized at initial design and after design or processing changes affating these parameters.
2. Capacitance measurements are made with no bias applied.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			POST RADIATION +25°C		
			MIN	MAX	
Quiescent Device Current	IDD	VIN = 0V or VDD, VCC = VDD	-	1.0	mA
Operating Device Current (Note 1)	IOPER	Cycle Time = 1µs	-	4.5	mA
Operating Device Current (Deselected)	IOPRD	Cycle Time = 1µs	-	1.0	mA
Output Low Drive Current (Sink)	IDN	VOUT = 0.4V	2.5	-	mA
Output High Drive Current (Source)	IDP	VOUT = VDD - 0.4V	2.0	-	mA
Input Low Voltage (Note 2)	VIL		-	0.8	V
Input High Voltage (Note 2)	VIH		VDD/2	-	V
Input Leakage Current	IIN	VIN = 0V or VDD	-	±10	µA
Tri-State Output Leakage Current	IOZ	Applied Voltages = 0V or VDD	-	±30	µA
Minimum Data Retention Voltage	VDR		-	2.5	V
Data Retention Quiescent Current	IDDDR		-	400	µA
Read Cycle	tAVAV		250	-	ns
Access from Address	tAVQV		-	250	ns
Access from $\overline{CE}$	tELQV		-	280	ns

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	LIMITS POST RADIATION +25°C MIN	LIMITS POST RADIATION +25°C MAX	UNITS
Write Cycle	tAVAV		250	-	ns
Write Pulse Width (Note 3)	tWLWH		145	-	ns
Address Set Up to Beginning of Write	tAVWL		0	-	ns
Address Set Up to End of Write	tAVWH		205	-	ns
Address Hold Time	tWHAV		45	-	ns
$\overline{CE}$ to Write Set Up Time	tELWH		205	-	ns
$\overline{CE}$ Pulse Width (Note 3)	tELEH		220		ns
Data to Write Set Up Time	tDVWH		120	-	ns
Data Hold From Write	tWHDX		10	-	ns

NOTES:

1. $\overline{CE}$ and $\overline{WE}$ must overlap for at least tWLWH minimum value, tDVWH minimum value must occur during this overlap.
2. Measured using 1MHz cycle.
3. Operating current measured using 1MHz cycle and CL = 50pF.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

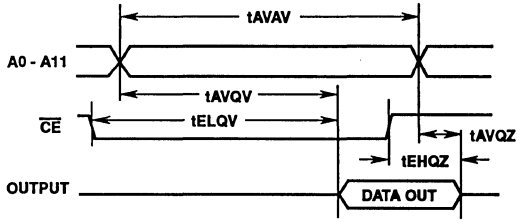
PARAMETER	SYMBOL	DELTA LIMITS
Quiescent Device Current	IDD	+30µA
Output Low Drive Current (Sink)	IDN	-15% of 0 hr. value
Output High Drive Current (Source)	IDP	-15% of 0 hr. value
Tri-State Output Leakage Current	IOZ	+500nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-IRZ SUBGROUPS	3Z SUBGROUPS	3 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9	1, 7, 9
Interim Test		100%/5004	1, 7, 9	N/A	N/A
PDA		100%/5004	1, 7, Δ	1, 7	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A	N/A
	Others	Samples/5005	1, 7	N/A	N/A
Group C (Optional)		Samples/5005	N/A	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group D (Optional)		Samples/5005	1, 7	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7, 9	1, 7, 9	N/A

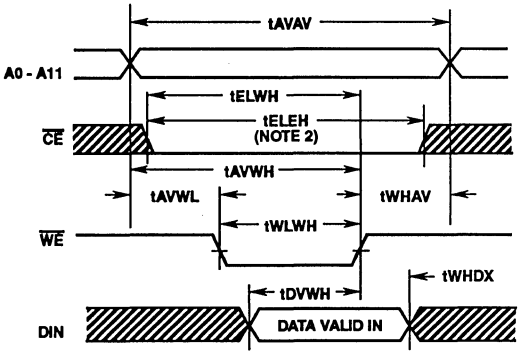
Timing Waveforms

READ CYCLE



NOTE: Timing measurement is referenced to VDD/2.

WRITE CYCLE

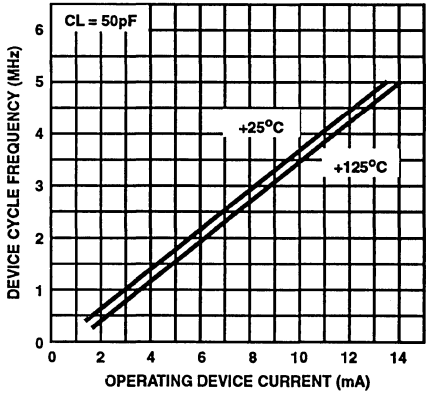


NOTES:

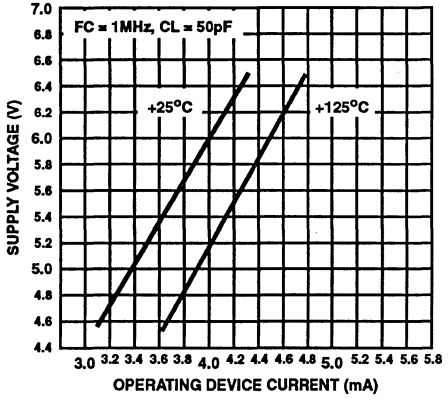
1. Timing measurement is referenced to VDD/2.
2. $\overline{CE}$ and $\overline{WE}$ must overlap for at least TWLWH minimum value, tDVWH minimum value must occur during this overlap.

Typical Performance Curves

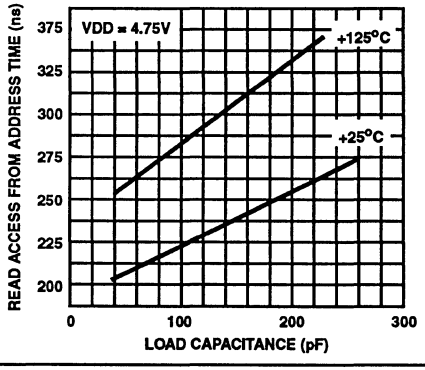
TYPICAL OPERATING DEVICE CURRENT (SELECTED) AS A FUNCTION OF CYCLE FREQUENCY



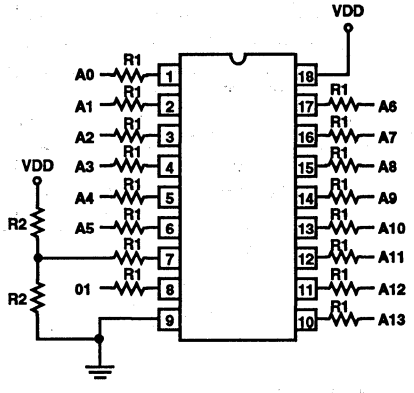
TYPICAL OPERATING DEVICE CURRENT (SELECTED) AS A FUNCTION OF SUPPLY VOLTAGE



READ ACCESS FROM ADDRESS TIME (tAVQV) AS A FUNCTION OF LOAD CAPACITANCE. (TIME MEASUREMENTS MADE AT 50% VDD POINT)



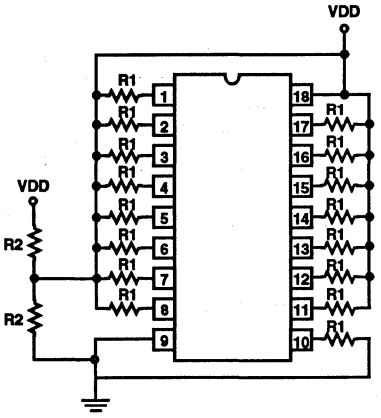
Burn-In Circuits



DYNAMIC CONFIGURATION

NOTES:

R1 = 1kΩ to 60kΩ ± 5%
R2 = 9.1kW ± 5%
VDD = 5.5V (Min)
VIN = 0V, VDD
Frequency: A0 = 100kHz ± 5%; A1 = A0/2 . . . . A13 = A12/2
01 = 200kHz ± 5%, 0.6µs Low, 4.4µs High

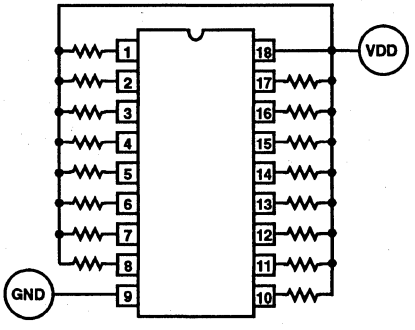


STATIC CONFIGURATION

NOTES:

R1 = 1kΩ to 60kΩ ± 5%
R2 = 9.1kΩ ± 5%
VDD = 5.5V (Min)
Static Burn-In 1 memory array pre-initialized with all Highs at VDD,
VIN = VDD
Static Burn-In 2 memory array pre-initalized with all Lows at VSS,
VIN = VSS

Irradiation Circuit



NOTES:

VDD = +5V, +5%
GND = 0V
All Resistors are 47kΩ ± 5%

Harris - IRZ Product Flow

Wafer Lot Acceptance Method 5007 (Includes SEM)

Radiation Verification (Each Wafer) Method 1019, 100K RADS(Si) Total Dose 2 Samples/Wafer, 0 Reject

Nondestructive Bond Pull Method 2023

Internal Visual (100%) Method 2010 (See "Visual Inspection")

Stabilization Bake (100%) Method 1008, Condition C, 24 Hrs Min., +150°C Min

Temperature Cycling (100%) Method 1010, Condition C, -65°C to +150°C

Constant Acceleration (100%) Method 2001, Condition E, Y1 (30,000g)

Particle Impact Noise Detection Method 2020, Condition A, 20g Peak at 60Hz

Visual Inspection (100%)

Serialization (100%)

Initial Electrical Tests (100%)

High Temperature Stress (100%) 48 Hrs, +125°C

Interim 1 Electrical Tests (100%), PDA 10% All Tests

Static Burn-In I (100%) 24 Hrs, +125°C

Interim 2 Electrical Tests (100%) (Note 1)

Static Burn-In 2 (100%) 24 Hrs, +125°C

Interim 3 Electrical Tests (100%) (Note 1)

Dynamic Burn-In (100%) 240 Hrs, +125°C

Interim 4 Electrical Tests (100%) PDA 5% All Tests, PDA 3% Functional

Fine and Gross Seal (100%) Method 1014

Final Electrical Tests (100%)

Radiographic (100%) Method 2012 (1 View)

External Visual (100%) Method 2009

Quality Conformance
- Group A (All Tests) Method 5005 (Class S)
- Group B (Optional) Method 5005 (Class S)
- Group D (Optional) Method 5005 (Class S)

CSI and/or GSI (Optional)

NOTES:

1. Failures from Interim Electrical Tests 2 and 3 are combined for determining PDA (PDA = 5% All Tests, 3% Functional)

Visual Inspection

Visual Inspection for Class S is performed to MIL-STD-883, Method 2010, Condition A **except** as follows:

Use:

3.2.1.1 - Metallization Scratches

3.2.1.2 - Metallization Voids

3.2.1.6 - Metallization Bridging

3.2.1.7 - Metallization Alignment

3.2.3 - Scribing and Die Defects. In addition, semicircular cracks that point away from the active circuit area are acceptable

3.2.3c - A crack that exceeds 5 mils in length must also point towards or cross a scribe grid line

3.1.7b - Lifting or Peeling of Glassivation, add Note of 3.2.7b to 3.1.7b

NOTES:

1. High magnification inspection is performed at 200X to 300X and applies to the high current areas of the chip. The remainder of the chip is inspected at 75X to 150X where high magnification is required.
2. Criteria 3.2.1.1a Metallization Scratches, and 3.2.1.2a Metallization Voids shall also apply to metallization over a passivation step (3.2.1.1d, 3.2.1.2b). Underlying oxide must also be exposed.
3. Criteria 3.2.1.7 Metallization Alignment and 3.1.2 Diffusion and Passivation Faults are applied to the center and two opposite corners of the chip. Areas of sufficient complexity are viewed to assure general alignment and contact coverage and shall consist only of the area exposed to the immediate field of view.
4. SOS Technology Devices
   - Diffusion faults 3.1.2.1 are not applicable. SOS devices are inspected for complete islands, bridging between islands and missing adjacent contacts from a row in a contact chain.
   - The 1 mil wire clearance criteria is not applicable
   - Passivation faults are not applicable when a second free flow oxide is used prior to metallization
   - Oxide gate bridge inspection is not applicable
   - Semicircular cracks not in an active area which start and end at the pellet edge are acceptable

Harris - 3Z Product Flow

Radiation Verification (Each Wafer) Method 1019, 100KRADS(Si) Total Dose 2 Samples/Wafer, 0 Reject (3Z Product Flow continues below)

Harris - 3 Product Flow (Without Radiation Verifications)

Internal Visual (100%) Method 2010, Condition B (Modified) (See "Internal Visual Inspection Modified for LSI")

Pre-Seal Bake (100%)

Stabilization Bake (100%) Method 1008, Condition C, 24 Hrs, +25°C , No End Point Measurements Required

Temperature Cycling (100%) Method 1010, Condition C

Constant Acceleration (100%) Method 2001, Condition E, Y1, Direction, Centrifuge

Seal:
Fine (100%) Method 1014, Condition A or B
Gross (100%) Method 1014, Condition C

Initial Electrical Tests (100%) Per Applicable Device Specification, +25°C

High Temperature Stress (100%) 48 Hrs, +125°C

Interim Electrical Tests 1 (100%) Per Applicable Device Specifications, +25°C PDA 10%, All Tests

Static Burn-In (100%) 160 Hrs, +125°C

Interim Electrical Tests 2 (100%) Per Applicable Device Specifications, +25°C PDA 5%, All Tests, PDA 3% Functional

Final Electrical Tests (100%) Per Applicable Device Specifications, +25°C

External Visual (100%) Method 2009

Quality Conformance
Group A (All Tests) Method 5005 (Class B)
Group B (Optional) Method 5005 (Class B)
Group C (Optional) Method 5005 (Class B)
Group D (Optional) Method 5005 (Class B)

Internal Visual Inspection Modified for LSI

Internal Visual Inspection is performed to MIL-STD-883, Method 2010, Condition B **except** as follows:

A. **High Magnification Inspection** is performed at 200X to 300X and applies to the high current areas of the chip. The remainder of the chip is inspected at 75X to 150X where high magnification is required

B. **Metallization Voids** (3.2.1.2) Criteria 3.2.1.1a Metallization Scratches and 3.2.1.2a Metallization Voids shall also apply to metallization over a passivation step (3.2.1.1d, 3.2.1.2b). Underlying oxide must also be exposed

C. **Metallization Alignment** (3.2.1.7) Diffusion and Passivation Layer(s) Faults (3.2.0)

High magnification inspection is performed at 200X to 300X, applied to the center and two opposite corners of the chip, consisting only of the area exposed to the immediate field of view

D. **Scribing and Die Defects** (3.2.3) in addition:

A crack that exceeds 5 mils in length must also point towards or cross a scribe grid line to be unacceptable

Semicircular cracks that point away from the active circuit area are acceptable

E. **SOS Technology Devices:**

- Diffusion faults are not applicable. SOS devices are inspected for complete islands, bridging between islands and missing adjacent contacts from a row in a contact chain.
- The 1 mil wire clearance criteria is not applicable
- Passivation faults are not applicable when a second free flow oxide is used prior to metallization
- Oxide gate bridge inspection is not applicable
- Semicircular cracks not in an active area which start and end at the pellet edge are acceptable

HARRIS SEMICONDUCTOR

HS-6514RH

Radiation Hardened 1024 x 1 CMOS RAM

December 1992

Features

- Total Dose 1 x 10^5 RAD (Si)
- Data Upset > 10^8 RAD (Si)/s
- Latch-Up Free To > 1 x 10^{12} RAD (Si)/s
- Low Power Standby 1100µW Max
- Low Power Operation 38.5mW/MHz Max
- Fast Access Time 150ns Typ
- Single Event Upset Immune Option
- TTL Compatible Output
- Common Data I/O
- Three-State Outputs
- Standard JEDEC Pinouts
- 18 Pin Package for High Density
- On-Chip Address Register
- Military Temperature Range -55°C to +125°C

Description

The HS-6514RH is a synchronous 1024 x 1 static CMOS RAM fabricated using the radiation hardened guard band ring, self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

Latch-up free operation is achieved by the use of epitaxial starting material to eliminate the parasitic SCR effect seen in conventional bulk CMOS devices. On-chip latches are provided for addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory arrays.

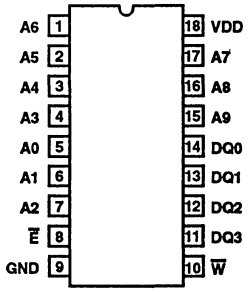
The HS-6514RH is a fully static RAM and may be maintained in any state for an indefinite period of time. A single event upset immune version of the HS-6514RRH is also offered.

JAN

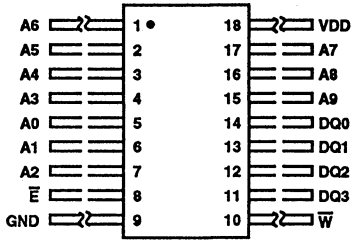
On January 28, 1987, Harris received JAN line certification as a Rad-Hard Class S fabrication facility for the HS-6514RH. Specifications can be found in JAN 38510/245 under device type 04.

Pinouts

HS1-6514RH 18 PIN CERAMIC DIP
CASE OUTLINE D-6, CONFIGURATION 3
TOP VIEW



TOP VIEW
HS9-6514RH 18 LEAD FLATPACK
INTERNAL PACKAGE CODE "HRF"
TOP VIEW



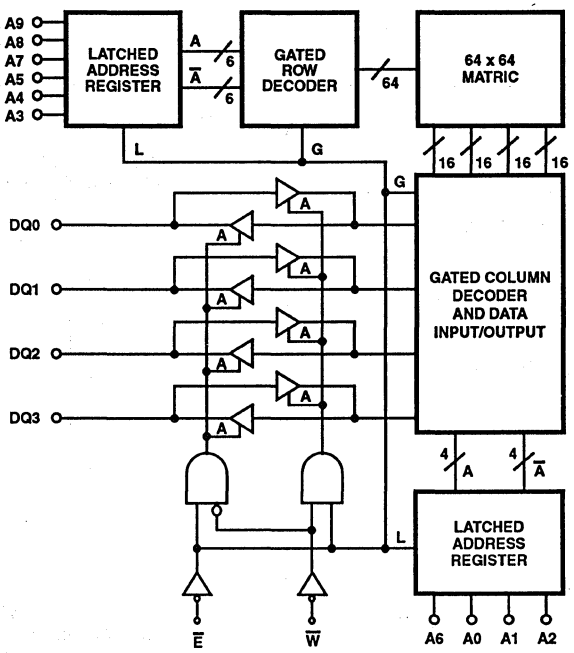
PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
DQ	Data In/Out

8 MEMORIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3029**

Functional Diagram



All Lines Active High - Positive Logic
Three-State Buffers: A High Output Active
Address Registers: Latch on Rising Edge of L
Gated Decoders: Gate on Rising Edge of G

Absolute Maximum Ratings

Supply Voltage -(VDD-GND) ..... -0.3 to +7.0V
Input or Output Voltage Applied .....GND-0.3V to VDD +0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature..... +175°C
Lead Temperature (Soldering 10s)..... +300°C
Typical Derating Factor.....3.0mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

	θ_{ja}	θ_{jc}
Thermal Resistance		
18 Pin Ceramic DIP Package	73°C/W	10°C/W
18 Lead Flatpack Package	62°C/W	10°C/W

Maximum Package Power Dissipation at +125°C
18 Pin Ceramic DIP Package 0.68W
18 Lead Flatpack Package 0.80W
Gate Count .....6672 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage Range..... +4.5V to +5.5V
Operating Temperature Range..... -55°C to +125°C
Input Rise and Fall Time..... 40ns Max

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Standby Supply Current	IDDSB	IO = 0, VI = GND or VDD	-	200	µA
Operating Supply Current (Note 1)	IDDOP	f = 1MHz, IO = 0, VI = VDD or GND	-	7	mA
Data Retention Supply Current	IDDDR		-	100	µA
Data Retention Supply Voltage	VDDDR		-	3.0	V
Input Leakage Current	II	GND ≤ VI ≤ VDD	-1.0	+1.0	µA
Output Leakage Current	IOZ	GND ≤ VO ≤ VDD	-10	+10	µA
Input Low Voltage	VIL		0.0	0.8	V
Input High Voltage	VIH		VDD -2.0	VDD	V
Output Low Voltage	VOL	IOL = 2.0mA	-	0.4	V
Output High Voltage	VOH	IOH = -1.0mA	2.4	-	V

NOTE:

1. Operating Supply Current (IDDOP) is proportional to Operating Frequency.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable Access Time	TELQV	Note 1	-	225	ns
Address Access Time	TAVQV	Note 1	-	235	ns
Chip EnableTime	TELEH	Note 1	225	-	ns
Chip Disable Time	TEHEL	Note 1	75	-	ns
Address Setup Time	TAVEL	Note 1	10	-	ns
Address Hold Time	TELAX	Note 1	50	-	ns
Write Enable Pulse Width	TWLWH	Note 1	225	-	ns
Write Enable Setup Time	TWLEH	Note 1	225	-	ns
Write Enable Hold Time	TELWH	Note 1	225	-	ns
Data Setup Time	TDVWH	Note 1	190	-	ns
Data Hold Time	TWHDZ	Note 1	50	-	ns

NOTE:

1. Inputs TRISE = TFALL ≤ 20nsec: Outputs : 1TTL load and 50pF. All timing measurements at 1/2 VDD.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Guaranteed but not tested)

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Input Capacitance	CI	VI = VDD or GND	-	8.0	pF
Output Capacitance	CO	VO = VDD or GND, f = 1MHz	-	10.0	pF
Chip Enable/Output Enable Time	TELQX	Note 1	5	-	ns
Chip Enable/Output Disable Time	TEHQZ	Note 1	-	75	ns
Write Enable/Output Disable Time	TWLQZ	Note 1	-	75	ns
Early Output High Z Time	TWLEL	Note 1	0	-	ns
Late Output High Z Time	TEHWH	Note 1	0	-	ns
Read or Write Cycle Time	TELEL	Note 1	300	-	ns

NOTE:

1. Inputs TRISE = TFALL ≤ 20nsec. Outputs : 1TTL load and 50pF. All timing measurements at 1/2 VDD.

TABLE 4. POST RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The post irradiation test conditions and limits are the same as those listed in Tables 1 and 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Output Low Voltage	VOL	± 0.08V
Output High Voltage	VOH	± 0.48V
Input Leakage Current	II	± 0.20µA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9
Interim Test 1 and 2		100%/5004	1, 7, 9	N/A
PDA 1 and 2		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A
	Others	Samples/5005	1, 7	N/A
Group C (Optional)		Samples/5005	N/A	1, 7
Group D (Optional)		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7, 9	1, 7, 9

Absolute Maximum Ratings

Supply Voltage -(VDD-GND) ..... -0.3 to +7.0V
Input or Output Voltage Applied .....GND-0.3V to VDD +0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature..... +175°C
Lead Temperature (Soldering 10s)..... +300°C
Typical Derating Factor.....3.0mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
18 Pin Ceramic DIP Package	73°C/W	10°C/W
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Maximum Package Power Dissipation at +125°C
18 Pin Ceramic DIP Package 0.68W
18 Lead Flatpack Package 0.80W
Gate Count ..... 6672 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage Range..... +4.5V to +5.5V
Operating Temperature Range..... -20°C to +80°C
Input Rise and Fall Time..... 40ns Max

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

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Data Retention Supply Current	IDDDR		-	100	µA
Data Retention Supply Voltage	VDDDR		-	3.0	V
Input Leakage Current	II	GND ≤ VI ≤ VDD	-1.0	+1.0	µA
Output Leakage Current	IOZ	GND ≤ VO ≤ VDD	-10	+10	µA
Input Low Voltage	VIL		-0.3	0.8	V
Input High Voltage	VIH		VDD -2.0	VDD +0.3	V
Output Low Voltage	VOL	IOL = 2.0mA	-	0.4	V
Output High Voltage	VOH	IOH = -1.0mA	2.4	-	V

NOTE:

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Address Setup Time	TAVEL	Note 1	10	-	ns
Address Hold Time	TELAX	Note 1	50	-	ns
Write Enable Pulse Width	TWLWH	Note 1	225	-	ns
Write Enable Setup Time	TWLEH	Note 1	225	-	ns
Write Enable Hold Time	TELWH	Note 1	225	-	ns
Data Setup Time	TDVWH	Note 1	190	-	ns
Data Hold Time	TWHDZ	Note 1	50	-	ns

NOTE:

1. Inputs TRISE = TFALL ≤ 20nsec: Outputs : 1TTL load and 50pF. All timing measurements at 1/2 VDD.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Guaranteed but not tested)

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			MIN	MAX	
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Chip Enable/Output Disable Time	TEHQZ	Note 1	-	75	ns
Write Enable/Output Disable	TWLQZ	Note 1	-	75	ns
Early Output High Z Time	TWLEL	Note 1	0	-	ns
Late Output High Z Time	TEHWH	Note 1	0	-	ns
Read or Write Cycle Time	TELEL	Note 1	300	-	ns

NOTE:

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TABLE 4. POST RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The post irradiation test conditions and limits are the same as those listed in Tables 1 and 2.

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PARAMETER	SYMBOL	DELTA LIMITS
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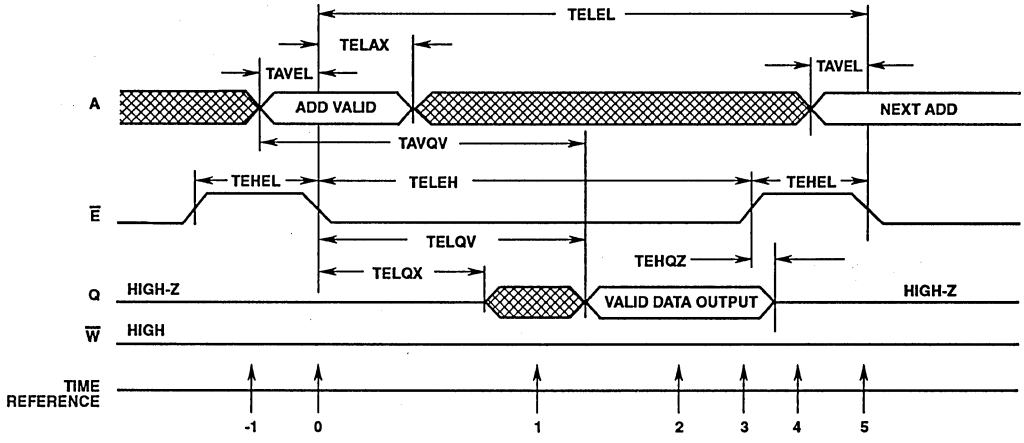
Output High Voltage	VOH	± 0.48V
Input Leakage Current	II	± 0.20µA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9
Interim Test 1 and 2		100%/5004	1, 7, 9	N/A
PDA 1 and 2		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A
	Others	Samples/5005	1, 7	N/A
Group C (Optional)		Samples/5005	N/A	1, 7
Group D (Optional)		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7, 9	1, 7, 9

Timing Waveforms

READ CYCLE



TRUTH TABLE

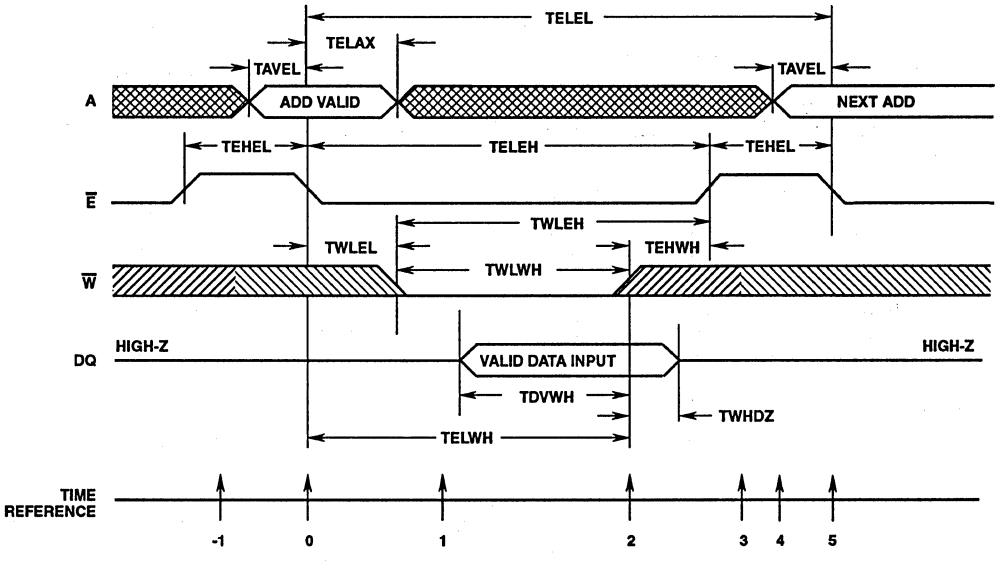
TIME REFERENCE	INPUTS $\overline{E}$	INPUTS $\overline{W}$	INPUTS A	OUTPUT DQ	FUNCTION
-1	H	X	X	Z	Memory Disabled
0	↘	H	V	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	Output Enabled
2	L	H	X	V	Output Valid
3	↗	H	X	V	Read Accomplished
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but the data is not valid until during time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). The memory is now ready for the next cycle.

NOTE: In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

Timing Waveforms (Continued)

WRITE CYCLE



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	INPUTS $\overline{W}$	INPUTS A	OUTPUT DQ	FUNCTION
-1	H	X	X	Z	Memory Disabled
0	↘	X	V	Z	Cycle Begins, Addresses are Latched
1	L	L	X	Z	Write Period Begins
2	L	↗	X	V	Data In is Written
3	↗	H	X	Z	Write Completed
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	X	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The write cycle is initiated by the falling edge of $\overline{E}$ (T = 0), which latches the addrss information in the on chip registers. There are two basic types of write cycle, which differ in the control of the common data-in/data-out bus.

Case 1: $\overline{E}$ falls before $\overline{W}$ falls.

The output buffers may become enabled (reading) if $\overline{E}$ falls before $\overline{W}$ falls. $\overline{W}$ is used to disable (three-state) the outputs so input data can be applied. TWLDV must be met to allow the $\overline{W}$ signal time to disable the outputs before applying input data. Also, at the end of the cycle the outputs may become active if $\overline{W}$ rises before $\overline{E}$. The RAM outputs will disable (three-state) after $\overline{E}$ rises (TEHQZ). In this type of write cycle TWLEL and TEHWH may be ignored.

Case 2: $\overline{E}$ falls equal to or after $\overline{W}$ falls, and $\overline{E}$ rises before or equal to $\overline{W}$ rises.

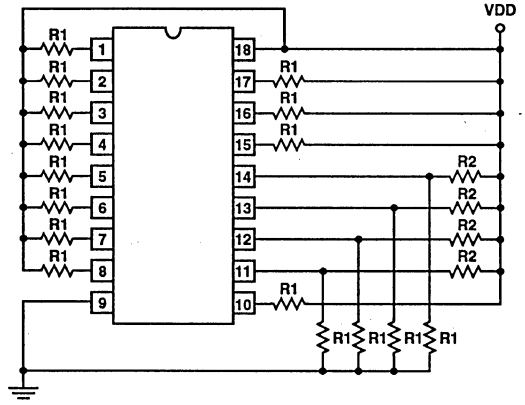
This $\overline{E}$ and $\overline{W}$ control timing will guarantee that the data output will stay disable throughout the cycle, thus simplifying the data input timing. TWLEL and TEHWH must be met but TWLDV becomes meaningless and can be ignored. In this cycle TDVWH and TWHDZ become TDVEH and TEHDZ. In other words, reference data setup and hold times to the $\overline{E}$ rising edge.

	IF	OBSERVE	IGNORE
Case 1	$\overline{E}$ falls before $\overline{W}$	TWLDV	TWLEL
Case 2	$\overline{E}$ falls after $\overline{W}$ and $\overline{E}$ rises before $\overline{W}$	TWLEL TEHWH	TWLDV TWHDV

If a series of consecutive write cycles are to be performed, $\overline{W}$ may be held low until all desired locations have been written (an extension of Case 2).

NOTE: In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

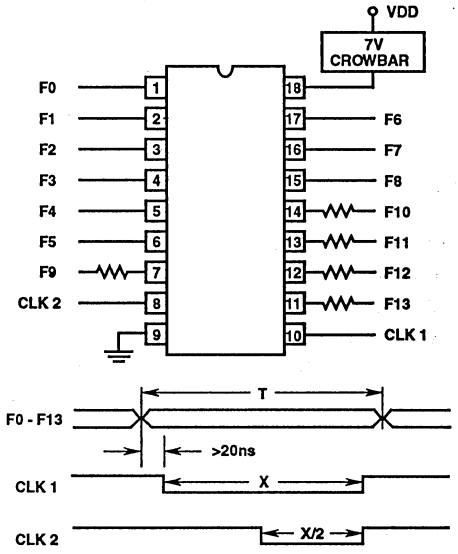
Burn-In Circuits



STATIC CONFIGURATION

NOTES:

VDD = 6.0V ± 0.5V
R1 = 1K
R2 = 1.5K
Minimum Ambient Temperature = +125°C

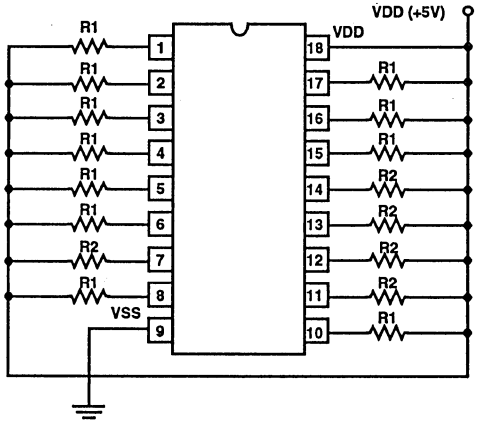


DYNAMIC CONFIGURATION

NOTES:

VDD = 6.0V ± 0.5V
All Resistors = 27KΩ
Minimum Ambient Temperature = +125°C
VDD must be applied before or at the same time as input signals
x > 700ns, T = 5µs
F0 = 100kHz
F1 = F0/2
F2 = F0/4
F3 = F0/8 . . . F13 = F0/8192

Irradiation Circuit



NOTES:

VDD = 5V
VSS = 0V
All Inputs = 5V
MONITOR: IDD at 5V
R1 = 47KΩ and R2 = 2.7KΩ

Harris - Space Level (-Q) Product Flow (Note 1)

SEM - Traceable to Diffusion Method 2018
Wafer Lot Acceptance Method 5007
Internal Visual Inspection Method 2010, Condition A
Gamma Radiation Assurance Tests Method 1019
Nondestructive Bond Pull Method 2023
Customer Pre-Cap Visual Inspection (Note 2)
Temperature Cycling Method 1010, Condition C
Constant Acceleration Method 2001, Condition E Min, Y1
Particle Impact Noise Detection Method 2020, Condition A
Electrical Tests (Harris' Option)
Serialization
X-Ray Inspection Method 2012
Electrical Tests - Subgroup 1; Read and Record (T0)
Static Burn-In Method 1015, Condition B, 72 Hrs, +125°C Min.
Interim 1 Electrical Tests - Subgroup 1; Read and Record (T1)
Burn-In Delta Calculation (T0 -T1)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Dynamic Burn-In Method 1015, Condition D, 240 Hrs, +125°C (Note 3)
Interim 2 Electrical Tests - Subgroup 1; Read and Record (T2)
Alternate Group A - Subgroups 1, 7, 9; Method 5005; Para 3.5.1.1
Burn-In Delta Calculation (T0 - T2)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Electrical Tests - Subgroup 3; Read and Record
Alternate Group A - Subgroups 3, 8B, 11; Method 5005; Para 3.5.1.1
Marking
Electrical Tests - Subgroup 2; Read and Record
Alternate Group A - Subgroups 2, 8A, 10; Method 5005; Para 3.5.1.1
Gross Leak Tests Method 1014, 100%
Fine Leak Tests Method 1014, 100%
Customer Source Inspection (Note 2)
Group B Inspection Method 5005 (Note 2)
End-Point Electrical Parameters: B-5 - Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11; B-6 - Subgroups 1, 7, 9
Group D Inspection Method 5005 (Notes 2, 4)
End-Point Electrical Parameters: Subgroups 1, 7, 9
External Visual Inspection Method 2009
Data Package Generation (Note 5)

NOTES:

1. The notes of Method 5004, Table 1 shall apply; Unless Otherwise Specified.
2. These steps are optional, and should be listed on the individual purchase order(s), when required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table 1 of Method 1015.
4. For Group D, Subgroup 3 inspection of package configurations which utilizes a gold plated lid in its construction; the inspection criteria for illegible markings criteria of Method 1010, paragraph 3.3 and of Method 1004, paragraph 3.8.a shall not apply.
5. Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (Including SEM Report)
   X-Ray Report and Film
   Test Variables Data

Harris -8 Product Flow

Internal Visual Inspection
Gamma Radiation Assurance Tests Method 1019
Customer Pre-Cap Visual Inspection (Note 1)
Temperature Cycling Method 1010, Condition C
Fine and Gross Leak Tests Method 1014
Constant Acceleration Method 2001 Y1 30KG
Initial Electrical Tests
Dynamic Burn-In Method 1015, Condition D, 160 Hrs, +125°C
+25°C Electrical Tests - Subgroups 1, 7, 9
PDA Calculation 5% Subgroups 1, 7
Electrical Tests +125°C, -55°C
Group A Inspection Method 5005. 5% PDA (Note 3)
Brand
Customer Source Inspection (Note 1)
Group C Inspection Method 5005 (Notes 1, 2)
Group D Inspection Method 5005 (Notes 1, 2)
External Visual Inspection Method 2009
Data Package Generation (Note 4)

NOTES:

1. These steps are optional, and must be negotiated as part of order.
2. Group B and D data package contains Attributes Data plus Variables Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable.
4. '-8' Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Radiation Testing Certificate of Conformance
   Certificate of Conformance (as found on shipper)

Metallization Topology

DIE DIMENSIONS:
Die Size: 155 x 237 mils
Die Thickness: 14 ±1 mils

METALLIZATION:
Type: Al, 14kÅ ± 2kÅ
Back: Gold

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

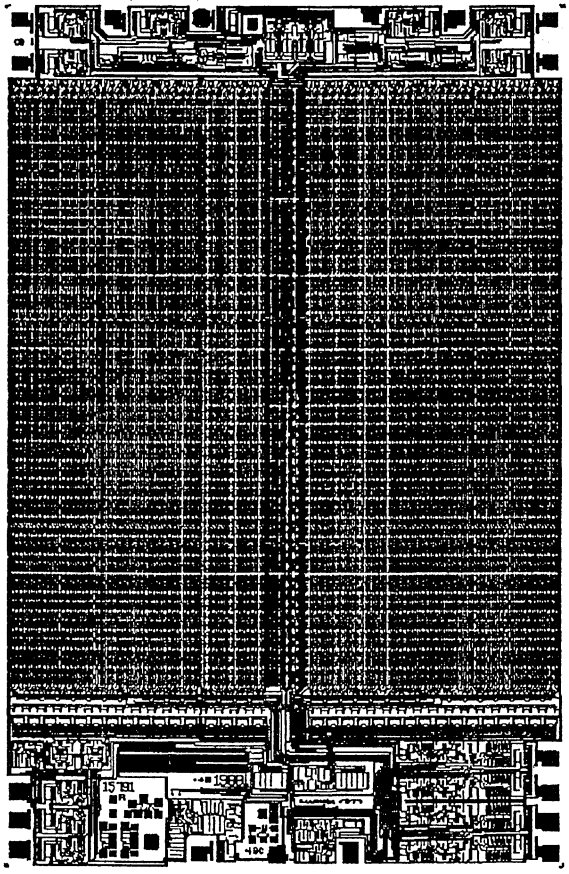
DIE ATTACH:
Material: Gold
Temperature: Sidebrazed Ceramic DIP - 460°C±10°C (Max)
Braze Seal Flatpack - 460°C ± 10°C (Max)

WORST CASE CURRENT DENSITY: 4.37×10^4 A/cm^2

SUBSTRATE POTENTIAL: VDD

Metallization Mask Layout

HS-6514RH



HARRIS SEMICONDUCTOR

CMM5114A

Radiation Hardened, High Reliability, CMOS/SOS 1024 Word by 4 Bit LSI Static RAM

December 1992

Features

- Radiation Hardened to 100KRAD(Si)
- Cosmic Ray Upset Immunity 2 x 10^{-9} Errors/Bit Day (TYP)
- Latch Up Free Under Transient Radiation
- Transient Upset > 10^{10} RADS/s, 20ns Pulse
- Fully Static Operation
- Single Power Supply 4.5V to 6.5V
- All Inputs and Outputs TTL Compatible
- Tri-State Outputs
- Industry Standard 18 Pin Configuration
- Low Standby and Operating Power
- Common Data Inputs and Outputs
- Gated Address Inputs by $\overline{CE}$

Description

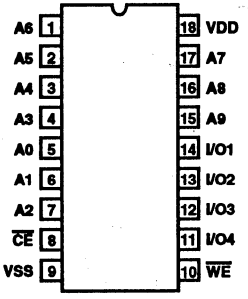
The CMM5114A is a high reliability 1024 word by 4 bit static random access memory using CMOS/SOS technology. It is designed for use in memory systems where low power and simplicity in use are desirable. TTL compatibility on all I/O terminals permits easy system integration.

CMOS/SOS technology permits operation in high radiation environments. It is insensitive to neutrons, cannot latch up at any dose rate and is resistance to single event upset caused by cosmic rays or heavy ions.

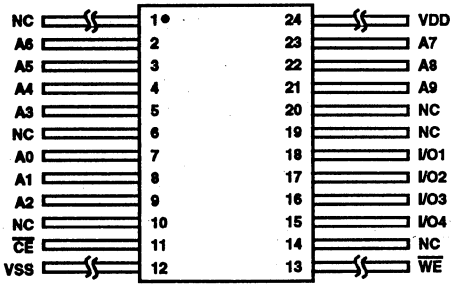
The CMM5114A is supplied in 18 lead dual-in-line side-brazed ceramic package (D suffix). The part is also available in a 24 lead flatpack ceramic package (K suffix).

Pinout

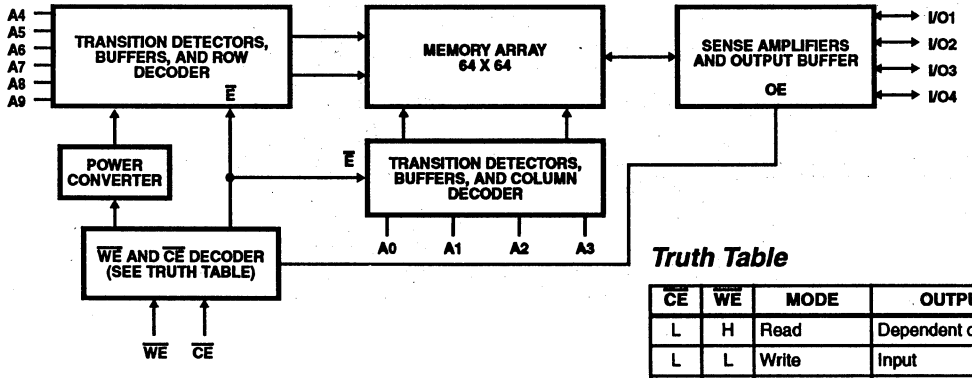
18 PIN CERAMIC DIP
CASE OUTLINE D6, CONFIGURATION 3
TOP VIEW



24 PIN FLATPACK
INTERNAL PACKAGE CODE "H9L"
TOP VIEW



Functional Diagram



Truth Table

$\overline{CE}$	$\overline{WE}$	MODE	OUTPUT
L	H	Read	Dependent on Data
L	L	Write	Input
H	X	Not Selected	High Impedance

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 2081.1

Absolute Maximum Ratings

Supply Voltage (VDD),
All voltage values referenced to VSS terminal ..... -0.5V to +7.0V
Input Voltage Range, All Inputs ..... -0.5 to VDD +0.5V
Input Current, Any One Input ..... ±10mA
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +265°C
Typical Derating Factor ..... 3.0mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Maximum Package Power Dissipation
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearly at 12mW/°C to 200mW
Power Dissipation per Output Transistor
For T_A = Full Package Temperature Range 100mW
Gate Count ..... 5400 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +6.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... VDD/2 to VDD
Data Retention Supply Voltage 2.5V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS VDD = 5V ± 5%, VIN = 0V or VDD, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	LIMITS -55°C, +25°C MIN	LIMITS -55°C, +25°C MAX	LIMITS +125°C MIN	LIMITS +125°C MAX	UNITS
Quiescent Device Current	IDD	VIN = 0V or VDD, $\overline{VCS}$ = VDD	-	0.1	-	1.0	mA
Operating Device Current (Note 1)	IDD1	Output Open Circuited Cycle Time = 1µs	-	5.0	-	6.0	mA
Output (Sink) Current	IOL	VOUT = 0.4V	2.6	-	1.7	-	mA
Output (Source) Current	IOH	VOUT = VDD - 0.4V	1.8	-	1.1	-	mA
Input Low Voltage (Note 2)	VIL		-	0.8	-	0.8	V
Input High Voltage (Note 2)	VIH		VDD/2	-	VDD/2	-	V
Input Leakage Current	IIN	VIN = 0V or VDD	-	±2	-	±10	µA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VDD	-	±5	-	±50	µA
Minimum Data Retention Voltage	VDR		-	2	-	2.5	V
Data Retention Quiescent Current	IDDDR		-	50	-	500	µA

NOTES:
1. Operating current measured using 1MHz cycle and CL = 50pF.
2. Measured using 1MHz cycle.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS VDD = 5V ± 5%, CL = 50pF

PARAMETER	SYMBOL	LIMITS -55°C, +25°C MIN	LIMITS -55°C, +25°C MAX	LIMITS +125°C MIN	LIMITS +125°C MAX	UNITS
READ CYCLE TIMES						
Read Cycle	tAVAV	200	-	250	-	ns
Access	tAVQV	-	200	-	250	ns
Chip Enable to Output Valid	tELQV	-	220	-	280	ns
WRITE CYCLE TIMES						
Write Cycle	tAVAV	250	-	300	-	ns
Write Pulse Width (Note 1)	tWLWH	200	-	200	-	ns
Address Hold Time from Write Enable	tWHAV	40	-	50	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS VDD = 5V ± 5%, CL = 50pF **(Continued)**

PARAMETER	SYMBOL	LIMITS				UNITS
		-55°C, +25°C		+125°C		
		MIN	MAX	MIN	MAX	
Address to Write Set Up Time	tAVWL	0	-	0	-	ns
Address Set Up to End of Write	tAVWH	200	-	250	-	ns
$\overline{CE}$ to Write Set Up Time	tELWH	200	-	250	-	ns
$\overline{CE}$ Pulse Width (Note 1)	tELEH	200	-	250	-	ns
Data to Write Set Up Time	tDVWH	90	-	105	-	ns
Data Hold From Write	tWHDX	5	-	5	-	ns

NOTE:

1. $\overline{CE}$ and $\overline{WE}$ must overlap for at least tWLWH minimum value, tDVWH minimum value must occur during this overlap and $\overline{CE}$ must be held low for 10ns after $\overline{WE}$ goes high.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	LIMITS				UNITS
		-55°C, +25°C		+125°C		
		MIN	MAX	MIN	MAX	
Output Voltage Low Level	VOL	-	0.1	-	0.2	V
Output Voltage High Level	VOH	VDD - 0.1	-	VDD - 0.2	-	V
Input Capacitance	CIN	-	5	-	5	pF
Output Capacitance	COUT	-	7	-	7	pF
Chip Enable to Output Active	tELQA	20	-	20	-	ns
Output Tri-State from Disable	tEHQZ	-	100	-	140	ns
Output Hold from Address Change	tAVQZ	30	110	55	150	ns

NOTE:

1. The parameters listed are controlled via design or process parameters and are not directly tested. These parameters are characterize upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			POST RADIATION +25°C		
			MIN	MAX	
Quiescent Device Current	IDD	VIN = 0V or VDD, $\overline{CS}$ = VDD	-	1.0	mA
Operating Device Current (Note 1)	IDD1	Output Open Circuited Cycle Time = 1µs	-	6.0	mA
Output Current (Sink)	IOL	VOUT = 0.4V	1.7	-	mA
Output Current (Source)	IOH	VOUT = VDD - 0.4V	1.7	-	mA
Input Low Voltage (Note 2)	VIL		-	0.8	V
Input High Voltage (Note 2)	VIH		VDD/2	-	V
Input Leakage Current	IIN	VIN = 0V or VDD	-	±10	µA
Tri-State Output Leakage Current	IOZ	Applied Voltages = 0V or VDD	-	±50	µA
Minimum Data Retention Voltage	VDR		-	2.5	V
Data Retention Quiescent Current	IDDDR		-	500	µA
Read Cycle	tAVAV		250	-	ns
Access	tAVQV		-	250	ns
$\overline{CE}$ to Output Valid	tELQV		-	280	ns

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	LIMITS POST RADIATION +25°C MIN	LIMITS POST RADIATION +25°C MAX	UNITS
Write Cycle	tAVAV		300	-	ns
Write Pulse Width (Note 3)	tWLWH		200	-	ns
Address Hold Time from Write Enable	tWHAV		50	-	ns
Address to Write Set Up Time	tAVWL		1	0	ns
Address Set Up to End of Write	tAVWH		250	-	ns
$\overline{CE}$ to Write Set Up Time	tELWH		250	-	ns
$\overline{CE}$ Pulse Width (Note 3)	tELEH		250		ns
Data to Write Set Up Time	tDVWH		105	-	ns
Data Hold From Write	tWHDX		5	-	ns

NOTES:

1. $\overline{CE}$ and $\overline{WE}$ must overlap for at least tWLWH minimum value, tDVWH minimum value must occur during this overlap.
2. Measured using 1MHz cycle.
3. Operating current measured using 1MHz cycle and CL = 50pF.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

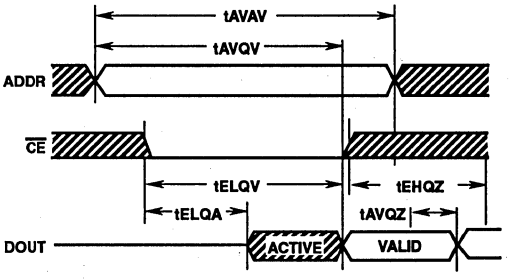
PARAMETER	SYMBOL	DELTA LIMITS
Quiescent Device Current	IDD	+30µA
Output Low Drive Current (Sink)	IDN	-10% of 0 hr. value
Output High Drive Current (Source)	IDP	-10% of 0 hr. value
Tri-State Output Leakage Current	IOZ	+500nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-IRZ SUBGROUPS	3Z SUBGROUPS	3 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9	1, 7, 9
Interim Test		100%/5004	1, 7, 9	N/A	N/A
PDA		100%/5004	1, 7, Δ	1, 7	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A	N/A
	Others	Samples/5005	1, 7	N/A	N/A
Group C (Optional)		Samples/5005	N/A	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group D (Optional)		Samples/5005	1, 7	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7, 9	1, 7, 9	N/A

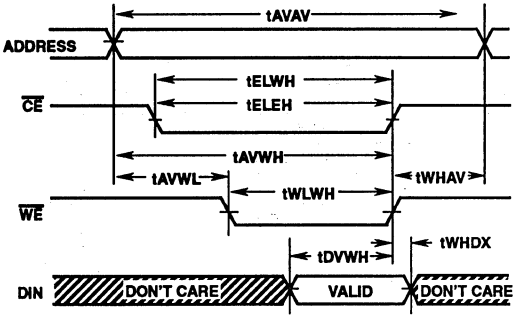
Timing Waveforms

READ CYCLE



NOTE: $\overline{WE}$ is high during the READ cycle timing measurement reference level is VDD/2

WRITE CYCLE

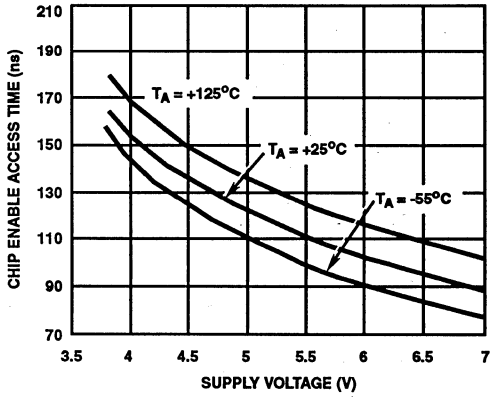


NOTE:

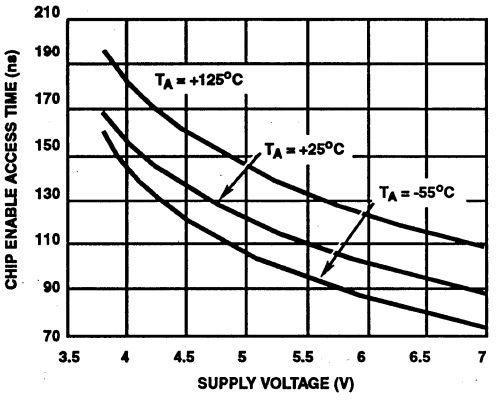
1. Timing measurement is referenced to VDD/2.

Typical Performance Curves

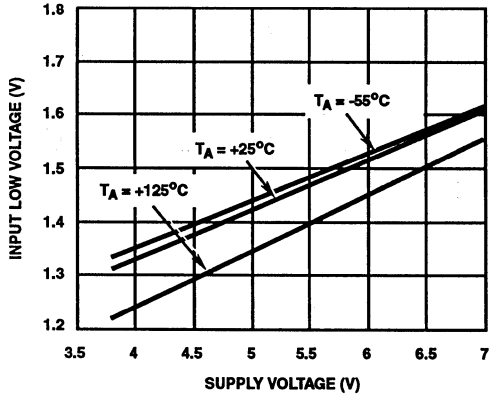
ADDRESS ACCESS TIME CHARACTERISTICS



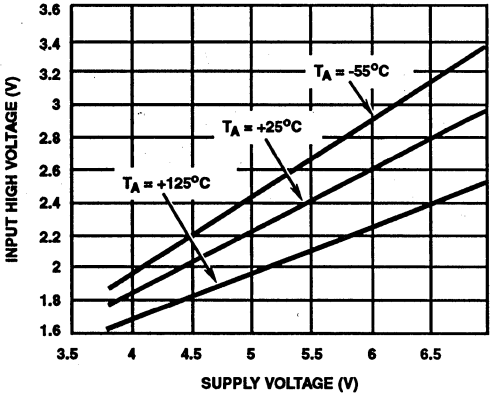
CHIP ENABLE ACCESS TIME CHARACTERISTICS



INPUT LOW VOLTAGE CHARACTERISTICS

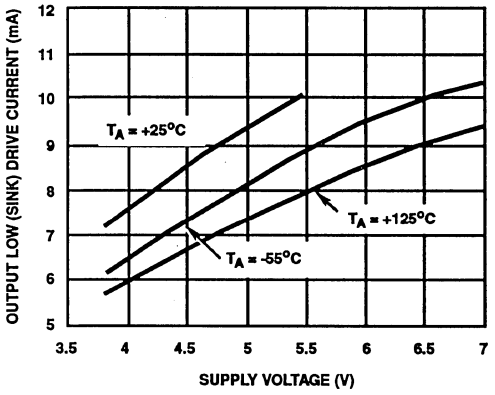


INPUT HIGH VOLTAGE CHARACTERISTICS

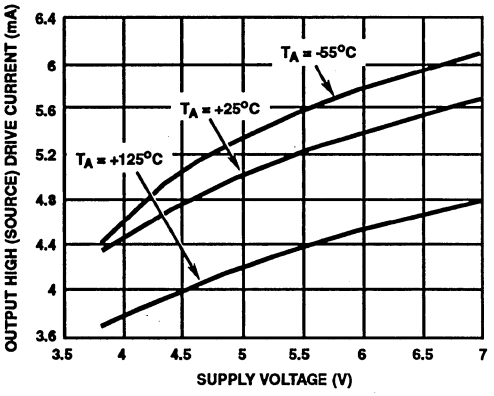


Typical Performance Curves (Continued)

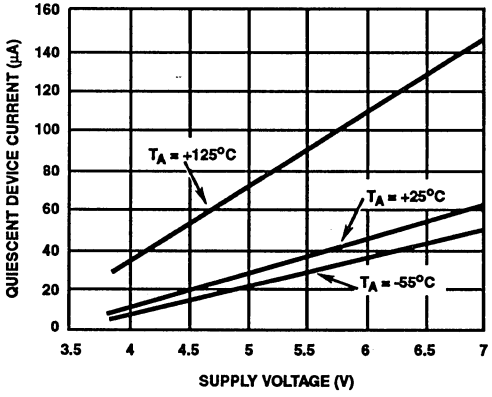
OUTPUT LOW (SINK) DRIVE CURRENT CHARACTERISTICS



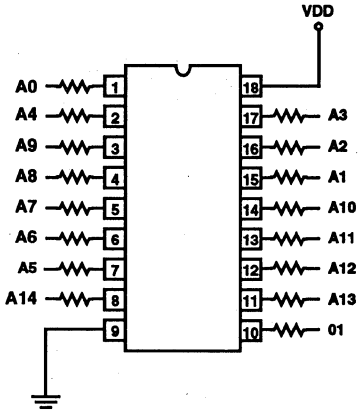
OUTPUT HIGH (SOURCE) DRIVE CURRENT CHARACTERISTICS



QUIESCENT DEVICE CURRENT CHARACTERISTICS



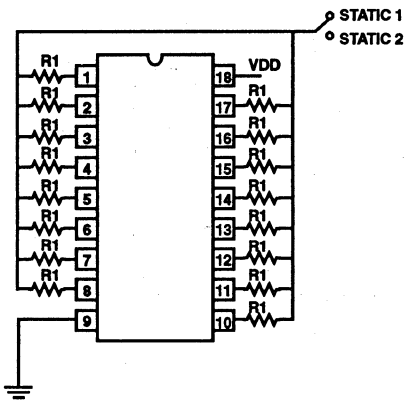
Burn-In Circuits



DYNAMIC CONFIGURATION

NOTES:

R1 = 1kΩ to 6kΩ, Unless Otherwise Specified
VDD = 5.5V (Min)
Frequencies: A0 = 100KHz ±5%
A1 = A0/2 . . . . A13 = A12/2
01 = 200KHz ±5%, 0.6µs Low, 4.4µs High

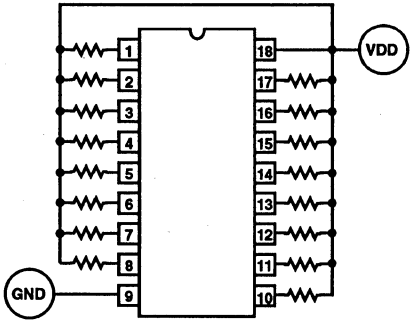


STATIC CONFIGURATION

NOTES:

R1 = 1kΩ to 6kΩ
VDD = 5.5V (Min)
Stress Test; Switch is at VSS
Static 1: Switch is at VDD
Static 2: Switch is at VSS

Irradiation Circuit



NOTES:

VDD = +5V, ±5%
GND = Ground
All Resistors are 47kΩ ± 5%

Harris - IRZ Product Flow

Wafer Lot Acceptance Method 5007 (Includes SEM)

Radiation Verification (Each Wafer) Method 1019, 100K RADS(Si) Total Dose 2 Samples/Wafer, 0 Reject

Nondestructive Bond Pull (100%) Method 2023

Internal Visual (100%) Method 2010 (See "Visual Inspection")

Stabilization Bake (100%) Method 1008, Condition C, 24 Hrs Min., +150°C Min

Temperature Cycling (100%) Method 1010, Condition C, -65°C to +150°C

Constant Acceleration (100%) Method 2001, Condition E, Y1 (30,000g)

Particle Impact Noise Detection Method 2020, Condition A, 20g Peak at 60Hz

Visual Inspection (100%)

Serialization (100%)

Initial Electrical Tests (100%)

High Temperature Stress (100%) 48 Hrs, +125°C

Interim 1 Electrical Tests (100%), PDA 10% All Tests

Static Burn-In I (100%) 24 Hrs, +125°C

Interim 2 Electrical Tests (100%) (Note 1)

Static Burn-In 2 (100%) 24 Hrs, +125°C

Interim 3 Electrical Tests (100%) (Note 1)

Dynamic Burn-In (100%) 240 Hrs, +125°C

Interim 4 Electrical Tests (100%) PDA 5% All Tests, PDA 3% Functional

Fine and Gross Seal (100%) Method 1014

Final Electrical Tests (100%)

Radiographic (100%) Method 2012 (1 View)

External Visual (100%) Method 2009

Quality Conformance
- Group A (All Tests) Method 5005 (Class S)
- Group B (Optional) Method 5005 (Class S)
- Group D (Optional) Method 5005 (Class S)

CSI and/or GSI (Optional)

NOTES:

1. Failures from Interim Electrical Tests 2 and 3 are combined for determining PDA (PDA = 5% All Tests, 3% Functional)

Visual Inspection

Visual Inspection for Class S is performed to MIL-STD-883, Method 2010, Condition A **except** as follows:

Use:

3.2.1.1 - Metallization Scratches

3.2.1.2 - Metallization Voids

3.2.1.6 - Metallization Bridging

3.2.1.7 - Metallization Alignment

3.2.3 - Scribing and Die Defects. In addition, semicircular cracks that point away from the active circuit area are acceptable

3.2.3c - A crack that exceeds 5 mils in length must also point towards or cross a scribe grid line

3.1.7b - Lifting or Peeling of Glassivation, add Note of 3.2.7b to 3.1.7b

NOTES:

1. High magnification inspection is performed at 200X to 300X and applies to the high current areas of the chip. The remainder of the chip is inspected at 75X to 150X where high magnification is required.
2. Criteria 3.2.1.1a Metallization Scratches, and 3.2.1.2a Metallization Voids shall also apply to metallization over a passivation step (3.2.1.1d, 3.2.1.2b). Underlying oxide must also be exposed.
3. Criteria 3.2.1.7 Metallization Alignment and 3.1.2 Diffusion and Passivation Faults are applied to the center and two opposite corners of the chip. Areas of sufficient complexity are viewed to assure general alignment and contact coverage and shall consist only of the area exposed to the immediate field of view.
4. SOS Technology Devices
   - Diffusion faults 3.1.2.1 are not applicable. SOS devices are inspected for complete islands, bridging between islands and missing adjacent contacts from a row in a contact chain.
   - The 1 mil wire clearance criteria is not applicable
   - Passivation faults are not applicable when a second free flow oxide is used prior to metallization
   - Oxide gate bridge inspection is not applicable
   - Semicircular cracks not in an active area which start and end at the pellet edge are acceptable

Harris - 3Z Product Flow

Radiation Verification (Each Wafer) Method 1019, 100KRADS(Si) Total Dose 2 Samples/Wafer, 0 Rejects (3Z Product Flow continues below)

Harris - 3 Product Flow (Without Radiation Verification)

Internal Visual (100%) Method 2010, Condition B (Modified) (See "Internal Visual Inspection Modified for LSI")

Pre-Seal Bake (100%)

Stabilization Bake (100%) Method 1008, Condition C, 24 Hrs, +25°C , No End Point Measurements Required

Temperature Cycling (100%) Method 1010, Condition C

Constant Acceleration (100%) Method 2001, Condition E1, Y1, Direction, Centrifuge

Seal:
- Fine (100%) Method 1014, Condition A or B
- Gross (100%) Method 1014, Condition C

Initial Electrical Tests (100%) Per Applicable Device Specification, +25°C

High Temperature Stress (100%) 48 Hrs, +125°C

Interim Electrical Tests 1 (100%) Per Applicable Device Specifications, +25°C PDA 10%, All Tests

Static Burn-In (100%) 160 Hrs, +125°C

Interim Electrical Tests 2 (100%) Per Applicable Device Specifications, +25°C PDA 5%, All Tests, PDA 3% Functional

Final Electrical Tests (100%) Per Applicable Device Specifications, +25°C

External Visual (100%) Method 2009

Quality Conformance
- Group A (All Tests) Method 5005 (Class B)
- Group B (Optional) Method 5005 (Class B)
- Group C (Optional) Method 5005 (Class B)
- Group D (Optional) Method 5005 (Class B)

Internal Visual Inspection Modified for LSI

Internal Visual Inspection is performed to MIL-STD-883, Method 2010, Condition B **except** as follows:

A. **High Magnification Inspection** is performed at 200X to 300X and applies to the high current areas of the chip. The remainder of the chip is inspected at 75X to 150X where high magnification is required

B. **Metallization Voids** (3.2.1.2) Criteria 3.2.1.1a Metallization Scratches and 3.2.1.2a Metallization Voids shall also apply to metallization over a passivation step (3.2.1.1d, 3.2.1.2b). Underlying oxide must also be exposed

C. **Metallization Alignment** (3.2.1.7) Diffusion and Passivation Layer(s) Faults (3.2.0)

High magnification inspection is performed at 200X to 300X, applied to the center and two opposite corners of the chip, consisting only of the area exposed to the immediate field of view

D. **Scribing and Die Defects** (3.2.3) in addition:

A crack that exceeds 5 mils in length must also point towards or cross a scribe grid line to be unacceptable

Semicircular cracks that point away from the active circuit area are acceptable

E. **SOS Technology Devices:**

- Diffusion faults are not applicable. SOS devices are inspected for complete islands, bridging between islands and missing adjacent contacts from a row in a contact chain.
- The 1 mil wire clearance criteria is not applicable
- Passivation faults are not applicable when a second free flow oxide is used prior to metallization
- Oxide gate bridge inspection is not applicable
- Semicircular cracks not in an active area which start and end at the pellet edge are acceptable

HARRIS SEMICONDUCTOR

HS-6508RH

Radiation Hardened 1024 x 1 CMOS RAM

December 1992

Features

- Functional Total Dose 2 x 10^4 RAD(Si)
- Latch-Up Free To > 5.0 x 10^{11} RAD(Si)/s
- Data Upset > 10^8 RAD(Si)/s
- Low Standby Power 550µW Max.
- Low Operating Power 25mW/MHz Max.
- Fast Access Time 300ns Max.
- TTL Compatible Outputs
- High Output Drive - 2 TTL Loads
- High Noise Immunity
- On-Chip Address Register
- Three-State Outputs
- 16 Pin Package for High Density
- Military Temperature Range -55°C to +125°C

Description

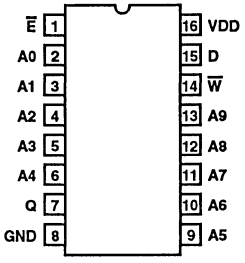
The Harris HS-6508RH is a 1024 by 1 static CMOS RAM fabricated using the Harris radiation hardened self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation. Latch-up free operation is achieved by the use of epitaxial starting material to eliminate the parasitic SCR effect seen in conventional CMOS devices.

On-Chip latches are provided for addresses allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HS-6508RH is a fully static RAM and may be maintained in any state for an indefinite period of time.

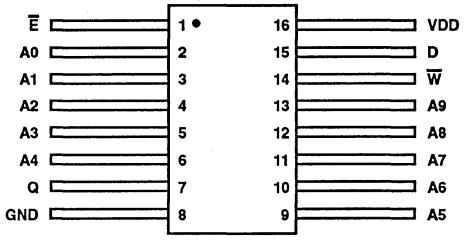
Pinouts

HS1-6508RH 16 PIN CERAMIC DIP
CASE OUTLINE D2, CONFIGURATION 3
TOP VIEW

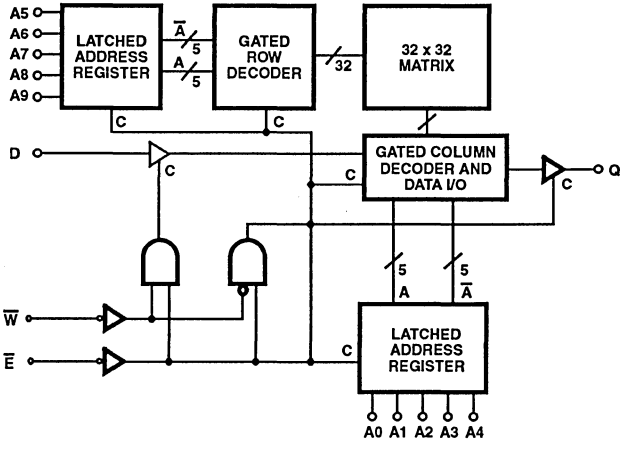


PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output

HS9-6508RH 16 PIN FLATPACK
INTERNAL PACKAGE CODE "H6P"
TOP VIEW



Functional Diagram



8 MEMORIES

File Number 3026

Absolute Maximum Ratings

Supply Voltage (VDD) ..... -0.3 to +7.0V
Input, Output or I/O Voltage ..... GND-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 1.5mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	74°C/W	11.4°C/W
Ceramic Flatpack Package	62.8°C/W	10.5°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 0.67W
Ceramic Flatpack Package 0.79W
Gate Count ..... 1839 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Rise and Fall Time ..... 40ns Max

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Standby Supply Current	IDDSB	IO = 0, VI = VDD or GND	-	100	µA
Operating Supply Current (Note 1)	IDDOP	f = 1MHz, IO = 0, VI = VDD or GND	-	4	mA
Input Leakage Current	II	GND ≤ VI ≤ VDD	-1.0	+1.0	µA
Output Leakage Current	IOZ	GND ≤ VI ≤ VDD	-1.0	+1.0	µA
Output High Voltage	VOH	IOH = -3mA	2.4	-	V
Output Low Voltage	VOL	IOL = 3.2mA	-	0.4	V
Input High Voltage	VIH		VDD-2.0	VDD	V
Input Low Voltage	VIL		0.0	0.8	V

NOTE:

1. Operating Supply Current (IDDOP) is proportional to Operating Frequency. Example: Typical IDDOP = 1.5mA/MHz

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Chip Enable Access Time	TELQV	Note 1	-	300	ns
Address Access Time	TAVQV	Note 1	-	310	ns
Chip Enable Pulse Negative Width	TELEH	Note 1	300	-	ns
Chip Enable Pulse Positive Width	TEHEL	Note 1	150	-	ns
Address Setup Time	TAVEL	Note 1	10	-	ns
Address Hold Time	TELAX	Note 1	70	-	ns
Data Setup Time	TDVWH	Note 1	130	-	ns
Data Hold Time	TWHDX	Note 1	0	-	ns
Chip Enable Write Pulse Setup Time	TWLEH	Note 1	160	-	ns
Chip Enable Write Pulse Hold Time	TELWH	Note 1	160	-	ns
Write Enable Pulse Width	TWLWH	Note 1	160	-	ns

NOTE:

1. Inputs - TRISE = TFALL ≤ 20ns; Outputs - 1 TTL load and 50pF. All timing measurements at $^1/_2$ VDD.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Guaranteed, but not tested)

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Input Capacitance	CI	VI = VDD or GND, f = 1MHz	-	6	pF
Output Capacitance	CO	VO = VDD or GND, f = 1MHz	-	10	pF
Chip Enable Output Enable Time	TELQX	Note 1	-	200	ns
Write Enable Output Disable Time	TWLQZ	Note 1	-	200	ns
Chip Enable Output Disable Time	TEHQZ	Note 1	-	200	ns
Read or Write Cycle Time	TELEL	Note 1	450	-	ns

NOTE:

1. Inputs - TRISE = TFALL ≤ 20ns; Outputs - 1 TTL load and 50pF. All timing measurements at $^1/_2$ VDD.

TABLE 4. POST RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

DC PARAMETER	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Stand By Current	IDDSB	VDD = 5 ± 0.5V	+25°C	-	10	mA

NOTE:

1. Based on the average of the entire sample.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

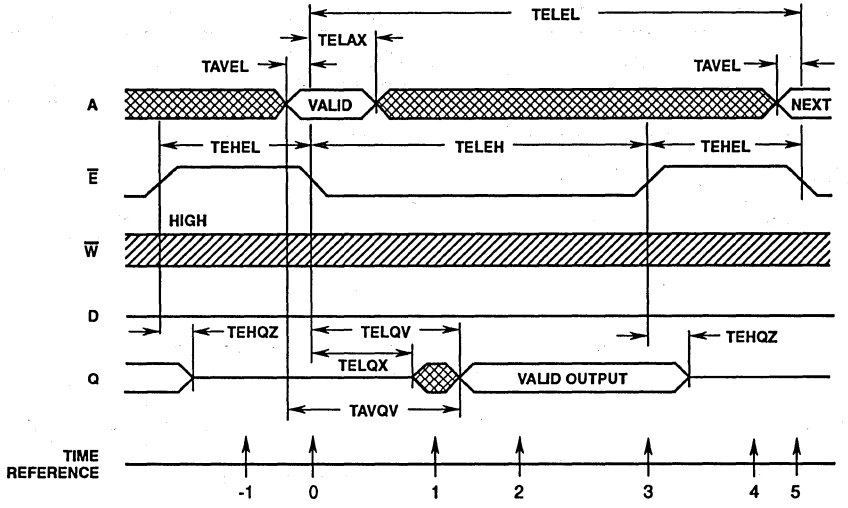
PARAMETER	SYMBOL	DELTA LIMITS
Output Low Voltage	VOL	± 0.15V
Output High Voltage	VOH	± 0.40V
Output Leakage Current	IOZ	± 300nA
Stand By Current	IDDSB	± 30µA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9
Interim Test 1 and 2		100%/5004	1, 7, 9	N/A
PDA 1 and 2		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A
	Others	Samples/5005	1, 7	N/A
Group C (Optional)		Samples/5005	N/A	1, 7
Group D (Optional)		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7, 9	1, 7, 9

Timing Waveforms

READ CYCLE



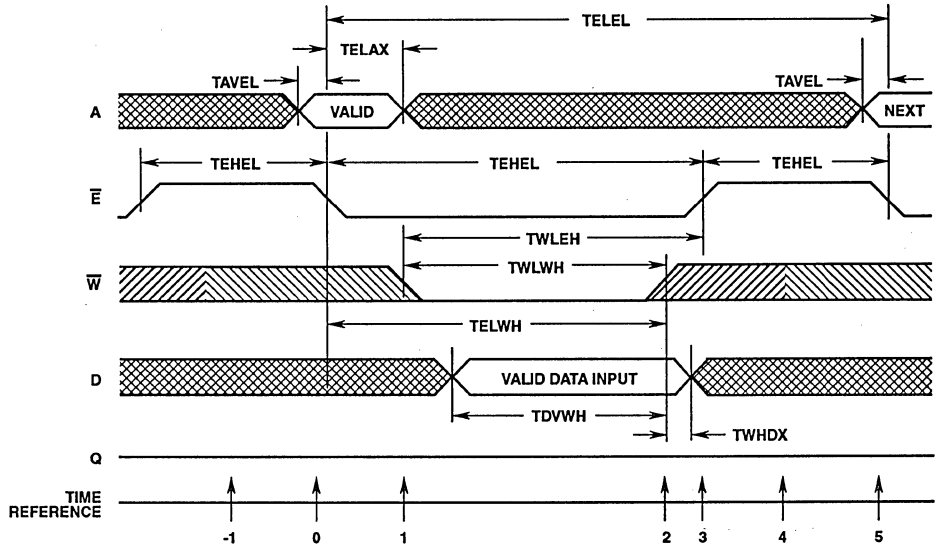
TRUTH TABLE

TIME REFERENCE	INPUTS				OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{W}$	A	D	Q	
-1	H	X	X	X	Z	Memory Disabled
0	↘	H	V	X	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	X	Output Enabled
2	L	H	X	X	V	Output Valid
3	↗	H	X	X	V	Read Accomplished
4	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

In the HS-6508RH Read Cycle, the address information is latched into the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the data output becomes enabled; however, the data is not valid until during time (T = 2). $\overline{W}$ must remain high for the read cycle. After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the chip and force the output buffer to a high impedance state. After the required $\overline{E}$ high time (TEHEL) the RAM is ready for the next memory cycle (T = 4).

Timing Waveforms (Continued)

WRITE CYCLE



TRUTH TABLE

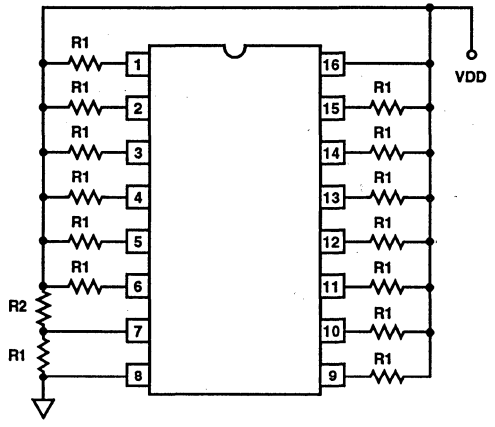
TIME REFERENCE	INPUTS				OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{W}$	A	D	Q	
-1	H	X	X	X	Z	Memory Disabled
0	↓	X	V	X	Z	Cycle Begins, Addresses are Latched
1	L	↓	X	X	Z	Write Period Begins
2	L	↑	X	V	Z	Data is Written
3	↑	H	X	X	Z	Write Completed
4	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	X	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The write cycle is initiated by the falling edge of $\overline{E}$ which latches the address information into the on chip registers. The write portion of the cycle is defined as both $\overline{E}$ and $\overline{W}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle provided that the write enable pulse setup time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $\overline{E}$ or $\overline{W}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$. By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed.

If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TELQX), a combination read write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH). The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method allow a minimum of one output disable time (TWLQZ) after $\overline{W}$ goes low before applying input data to the bus. This will insure that the output buffers are not active.

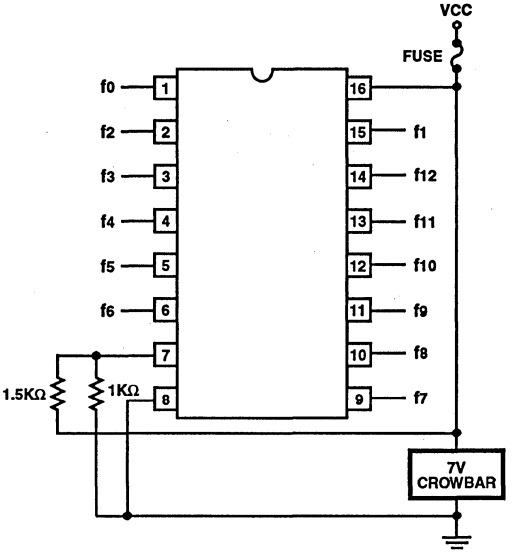
Burn-In Circuit



STATIC CONFIGURATION

NOTES:

Minimum Ambient Temperature = +125°C
VDD = 5.0V ± 10%
R1 = 1K
R2 = 1.5K

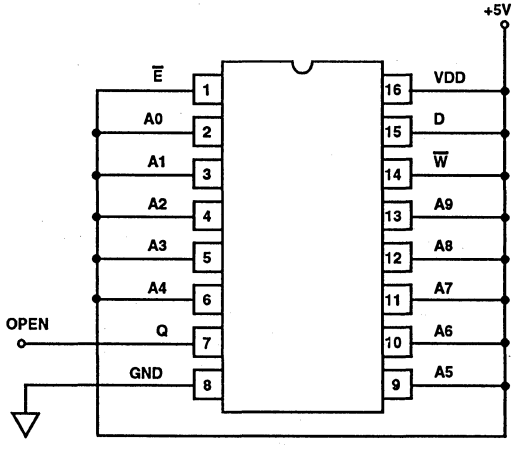


DYNAMIC CONFIGURATION

NOTES:

All Resistors are 1/4W, ±10% or better
50% Duty Cycles
f0 = 50KHz; f1 = f11/2; f2 = 25KHz; f3 = f2/2; f4 = f3/2; f5 = f4/2; f6 = f5/2 . . . f11 = f10/2; f12 = 100KHz

Irradiation Circuit



NOTES:

VDD = 5.0V
GND = 0V
All inputs = 5V
Q outputs float open

Harris - Space Level (-Q) Product Flow (Note 1)

SEM - Traceable to Diffusion Method 2018
Wafer Lot Acceptance Method 5007
Internal Visual Inspection Method 2010, Condition A
Gamma Radiation Assurance Tests Method 1019
Nondestructive Bond Pull Method 2023
Customer Pre-Cap Visual Inspection (Note 2)
Temperature Cycling Method 1010, Condition C
Constant Acceleration Method 2001, Condition E Min, Y1
Particle Impact Noise Detection Method 2020, Condition A
Electrical Tests (Harris' Option)
Serialization
X-Ray Inspection Method 2012
Electrical Tests - Subgroup 1; Read and Record (T0)
Static Burn-In Method 1015, Condition B, 72 Hrs, +125°C Min.
Interim 1 Electrical Tests - Subgroup 1; Read and Record (T1)
Burn-In Delta Calculation (T0 -T1)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Dynamic Burn-In Method 1015, Condition D, 240 Hrs, +125°C (Note 3)
Interim 2 Electrical Tests - Subgroup 1; Read and Record (T2)
Alternate Group A - Subgroups 1, 7, 9; Method 5005; Para 3.5.1.1
Burn-In Delta Calculation (T0 - T2)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Electrical Tests - Subgroup 3; Read and Record
Alternate Group A - Subgroups 3, 8B, 11; Method 5005; Para 3.5.1.1
Marking
Electrical Tests - Subgroup 2; Read and Record
Alternate Group A - Subgroups 2, 8A, 10; Method 5005; Para 3.5.1.1
Gross Leak Tests Method 1014, 100%
Fine Leak Tests Method 1014, 100%
Customer Source Inspection (Note 2)
Group B Inspection Method 5005 (Note 2)
End-Point Electrical Parameters: B-5 - Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11; B-6 - Subgroups 1, 7, 9
Group D Inspection Method 5005 (Notes 2, 4)
End-Point Electrical Parameters: Subgroups 1, 7, 9
External Visual Inspection Method 2009
Data Package Generation (Note 5)

NOTES:

1. The notes of Method 5004, Table 1 shall apply; Unless Otherwise Specified.
2. These steps are optional, and should be listed on the individual purchase order(s), when required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table 1 of Method 1015.
4. For Group D, Subgroup 3 inspection of package configurations which utilizes a gold plated lid in its construction; the inspection criteria for illegible markings criteria of Method 1010, paragraph 3.3 and of Method 1004, paragraph 3.8.a shall not apply.
5. Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (Including SEM Report)
   X-Ray Report and Film
   Test Variables Data

Harris -8 Product Flow

Internal Visual Inspection
Gamma Radiation Assurance Tests Method 1019
Customer Pre-Cap Visual Inspection (Note 1)
Temperature Cycling Method 1010, Condition C
Fine and Gross Leak Tests Method 1014
Constant Acceleration Method 2001 Y1 30KG
Initial Electrical Tests
Dynamic Burn-In Method 1015, Condition D, 160 Hrs, +125°C
+25°C Electrical Tests - Subgroups 1, 7, 9
PDA Calculation 5% Subgroups 1, 7
Electrical Tests +125°C, -55°C
Group A Inspection Method 5005. 5% PDA (Note 3)
Brand
Customer Source Inspection (Note 1)
Group C Inspection Method 5005 (Notes 1, 2)
Group D Inspection Method 5005 (Notes 1, 2)
External Visual Inspection Method 2009
Data Package Generation (Note 4)

NOTES:

1. These steps are optional, and must be negotiated as part of order.
2. Group B and D data package contains Attributes Data plus Variables Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable.
4. '-8' Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Radiation Testing Certificate of Conformance
   Certificate of Conformance (as found on shipper)

Metallization Topology

DIE DIMENSIONS:
132 x 160 x 14 ± 1mils

METALLIZATION:
Type: Si - Al
Thickness: 14kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP - 460°C (Max)

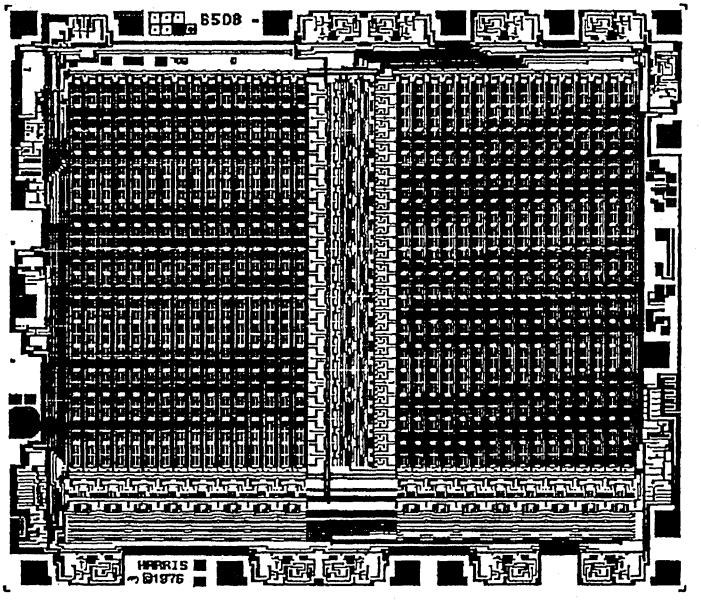
WORST CASE CURRENT DENSITY:
1.07×10^5 A/cm^2

LEAD TEMPERATURE (10 seconds soldering): ≤ 300°C

Substrate Potential: VDD

Metallization Mask Layout

HS-6508RH



HARRIS SEMICONDUCTOR

HS-6551RH

Radiation Hardened 256 x 4 CMOS RAM

December 1992

Features

- Functional Total Dose 2 x 10^4 RAD(Si)
- Latch-Up Free To > 5.0 x 10^{11} RAD(Si)/s
- Data Upset > 10^8 RAD(Si)/s
- Low Standby Power 550µW Max.
- Low Operating Power 22mW/MHz Max.
- Fast Access Time 300ns Max. 160ns Typ.
- TTL Compatible Outputs
- High Output Drive - 1 TTL Loads
- High Noise Immunity
- On-Chip Address Register
- Three-State Outputs
- 22 Pin Package for High Density
- Military Temperature Range -55°C to +125°C

Description

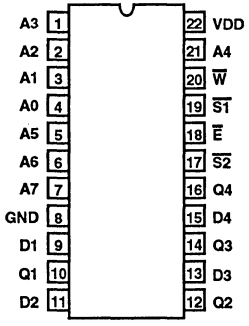
The HS-6551RH is a 256 by 4 static CMOS RAM fabricated using the Harris radiation hardened self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation. Latch-up free operation is achieved by the use of epitaxial starting material to eliminate the parasitic SCR effect seen in conventional bulk CMOS devices.

On-chip latches are provided for addresses, and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HS-6551RH is a fully static RAM and may be maintained in any state for an indefinite period of time.

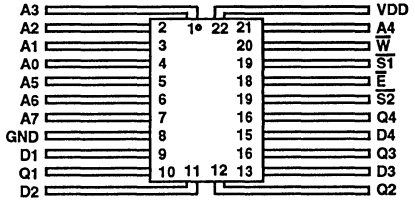
Pinouts

HS1-6551RH 22 PIN CERAMIC DIP
CASE OUTLINE D7, CONFIGURATION 3
TOP VIEW

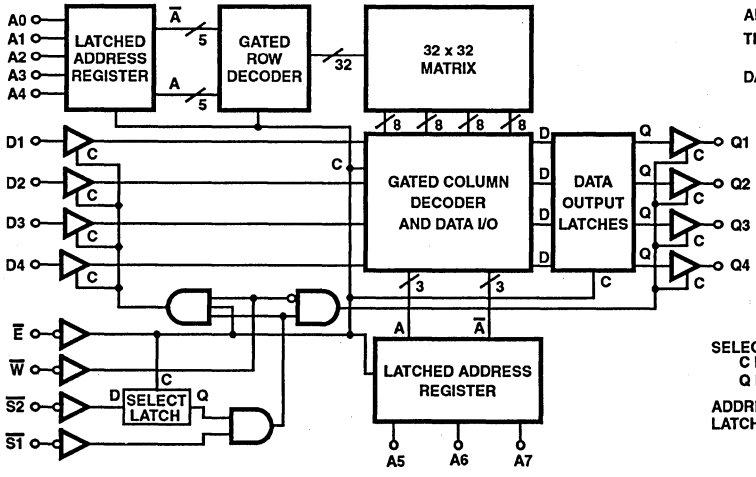


PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{S}$	Chip Select
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output

HS9-6551RH 22 PIN FLATPACK
INTERNAL PACKAGE CODE "HRE"



Functional Diagram



ALL LINES POSITIVE LOGIC-ACTIVE HIGH
THREE STATE BUFFERS:
C HIGH → OUTPUT ACTIVE
DATA LATCHES:
C HIGH → Q = D
Q LATCHES ON FALLING EDGE OF C

SELECT LATCH:
C LOW → Q = D
Q LATCHES ON RISING EDGE OF C
ADDRESS LATCHES AND DECODERS
LATCH AND GATE ON RISING EDGE OF C

8 MEMORIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3027

Absolute Maximum Ratings

Supply Voltage (VDD) ..... -0.3 to +7.0V
Input, Output or I/O Voltage ..... GND-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 1.5mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	73.9°C/W	11.3°C/W
Ceramic Flatpack Package	69.8°C/W	12.2°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 0.67W
Ceramic Flatpack Package 0.72W
Gate Count ..... 1841 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Rise and Fall Time ..... 40ns Max

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Standby Supply Current	IDDSB	IO = 0, VI = VDD or GND	-	100	µA
Operating Supply Current (Note 1)	IDDOP	f = 1MHz, IO = 0, VI = VDD or GND	-	4	mA
Input Leakage Current	II	GND ≤ VI ≤ VDD	-1.0	+1.0	µA
Output Leakage Current	IOZ	GND ≤ VI ≤ VDD	-1.0	+1.0	µA
Output High Voltage	VOH	IOH = -1.0mA	2.4	-	V
Output Low Voltage	VOL	IOL = 2.0mA	-	0.4	V
Input High Voltage	VIH		VDD-2.0	VDD	V
Input Low Voltage	VIL		0.0	0.8	V

NOTE:

1. Operating Supply Current (IDDOP) is proportional to Operating Frequency. Example: Typical IDDOP = 1.5mA/MHz

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable Access Time	TELQV	Note 1	-	300	ns
Address Access Time	TAVQV	Note 1	-	315	ns
Chip Enable Pulse Negative Width	TELEH	Note 1	300	-	ns
Chip Enable Pulse Positive Width	TEHEL	Note 1	150	-	ns
Address Setup Time	TAVEL	Note 1	15	-	ns
Chip Select 2 Setup Time	TS2LEL	Note 1	15	-	ns
Address Hold Time	TELAX	Note 1	70	-	ns
Chip Select 2 Hold Time	TELS2X	Note 1	70	-	ns
Data Setup Time	TDVWH	Note 1	180	-	ns
Data Hold Time	TWHDX	Note 1	0	-	ns
Chip Select 1 Write Pulse Setup Time	TWLS1H	Note 1	315	-	ns
Chip Enable Write Pulse Setup Time	TWLEH	Note 1	300	-	ns
Chip Select 1 Write Pulse Hold Time	TS1LWH	Note 1	195	-	ns
Chip Enable Write Pulse Hold Time	TELWH	Note 1	180	-	ns
Write Enable Pulse Width	TWLWH	Note 1	180	-	ns

NOTE:

1. Inputs - TRISE = TFALL ≤ 20ns; Outputs - 1 TTL load and 50pF. All timing measurements at $^1/_2$ VDD.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Guaranteed, but not tested)

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Input Capacitance	CI	VI = VDD or GND, f = 1MHz	-	6	pF
Output Capacitance	CO	VI = VDD or GND, f = 1MHz	-	10	pF
Chip Select 1 Output Enable Time	TS1LQX	Note 1	-	150	ns
Write Enable Output Disable Time	TWLQZ	Note 1	-	150	ns
Chip Select 1 Output Disable Time	TS1HQZ	Note 1	-	150	ns
Read or Write Cycle Time	TELEL	Note 1	450	-	ns

NOTE:

1. Inputs - TRISE = TFALL ≤ 20ns; Outputs - 1 TTL load and 50pF. All timing measurements at $^1/_2$ VDD.

TABLE 4. POST RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

DC PARAMETER	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Stand By Current	IDDSB	VDD = 5 ± 0.5V	+25°C	-	10	mA

NOTE:

1. Based on the average of the entire sample.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

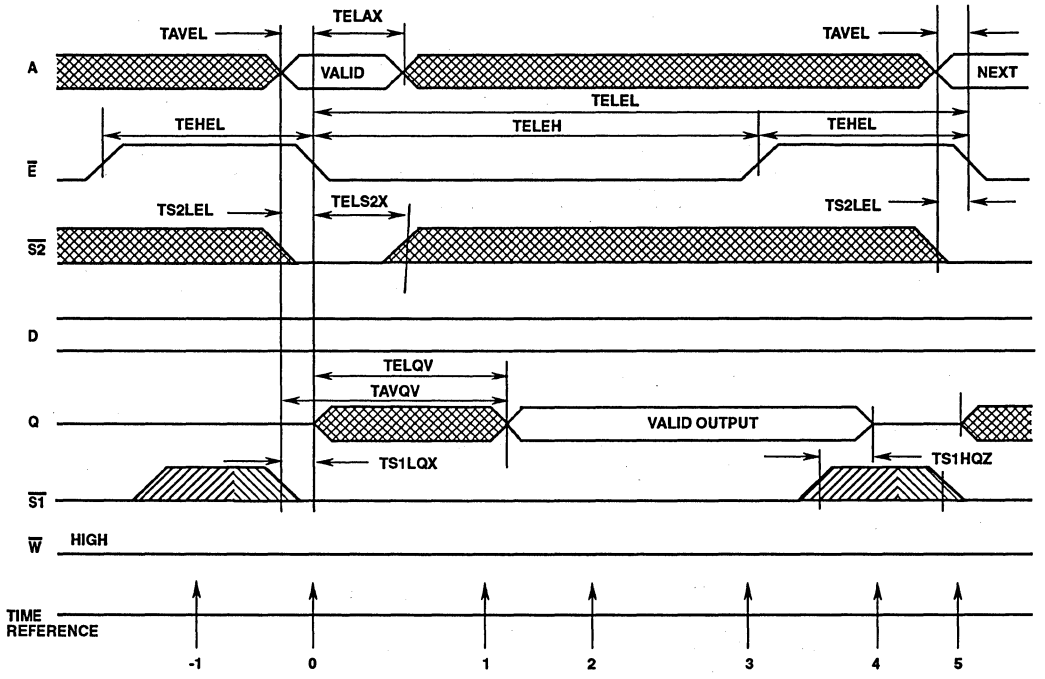
PARAMETER	SYMBOL	DELTA LIMITS
Output Low Voltage	VOL	± 0.15V
Output High Voltage	VOH	± 0.40V
Output Leakage Current	IOZ	± 300nA
Stand By Current	IDDSB	± 30µA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9
Interim Test 1 and 2		100%/5004	1, 7, 9	N/A
PDA 1 and 2		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A
	Others	Samples/5005	1, 7	N/A
Group C (Optional)		Samples/5005	N/A	1, 7
Group D (Optional)		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7, 9	1, 7, 9

Timing Waveforms

READ CYCLE



TRUTH TABLE

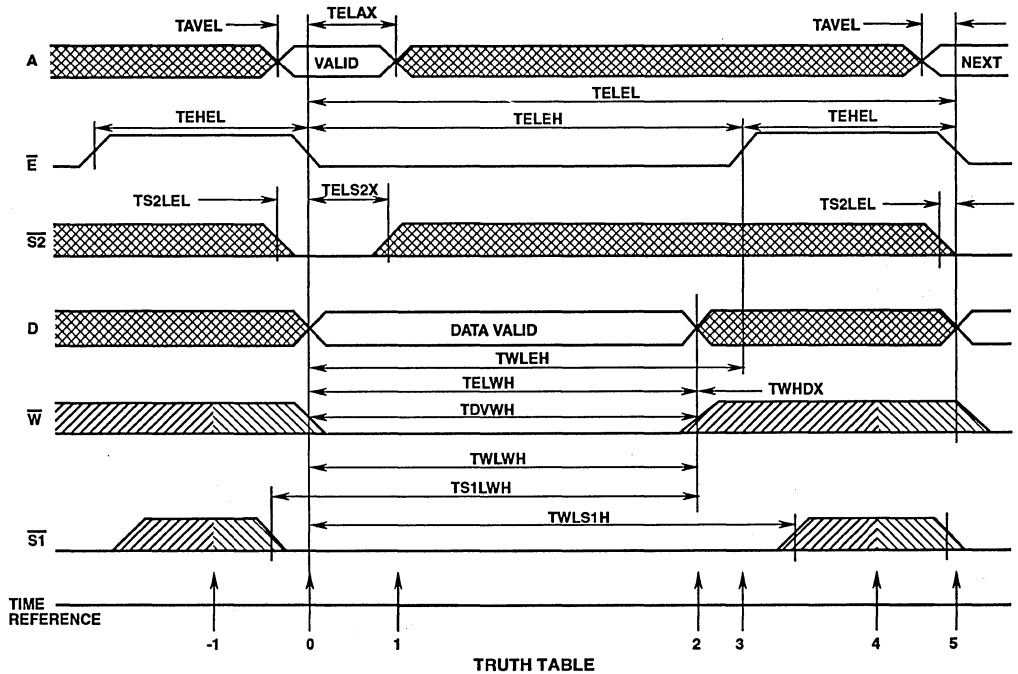
TIME REFERENCE	INPUTS						OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{S2}$	$\overline{W}$	A	D	Q	
-1	H	H	X	X	X	X	Z	Memory Disabled
0	↘	L	L	H	V	X	Z	Addresses and $\overline{S2}$ are Latched, Cycle Begins
1	L	L	X	H	X	X	X	Output Enabled but Undefined
2	L	L	X	H	X	X	V	Data Output Valid
3	↗	L	X	H	X	X	V	Outputs Latched, Valid Data
4	H	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	X	L	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The HS-6551RH Read Cycle is initiated by the falling edge of $\overline{E}$. This signal latches the input address word and $\overline{S2}$ into on chip registers providing the minimum setup and hold times are met. After the required hold time, these inputs may change state without affecting device operation. $\overline{S2}$ acts as a high order address and simplifies decoding. For the output to be read, $\overline{E}$, $\overline{S1}$ must be low and $\overline{W}$ must be high. $\overline{S2}$ must have been latched low on the falling edge of $\overline{E}$. The output data will be valid at access time (TELQV).

The HS-6551RH has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains in that state until $\overline{E}$ falls. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Timing Waveforms (Continued)

WRITE CYCLE



TRUTH TABLE

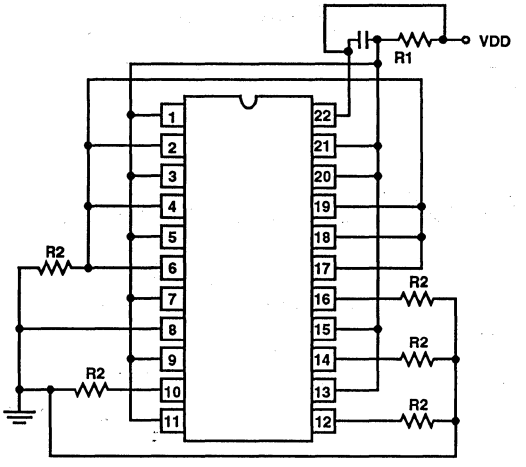
TIME REFERENCE	INPUTS						OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{S2}$	$\overline{W}$	A	D	Q	
-1	H	H	X	X	X	X	Z	Memory Disabled
0	↘	L	L	↘	V	X	Z	Cycle Begins, Addresses and $\overline{S2}$ are Latched
1	L	L	X	L	X	V	Z	Write Period Begins
2	L	L	X	↗	X	X	Z	Data In is Written
3	↗	L	X	H	X	X	Z	Write is Completed
4	H	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	X	L	X	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

In the Write Cycle the falling edge of $\overline{E}$ latches the addresses and $\overline{S2}$ into on chip registers. $\overline{S2}$ must be latched in the low state to enable the device. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$ being low and $\overline{S2}$ being latched low simultaneously. The $\overline{W}$ line may go low at any time during the cycle providing that the write pulse setup times (TWLEH and TWLS1H) are met. The write portion of the cycle is terminated on the first rising edge of either $\overline{E}$, $\overline{W}$, or $\overline{S1}$.

If a series of consecutive write cycles are to be executed, the $\overline{W}$ line may be held low until all desired locations have been written. If this method is used, data setup and hold times must be referenced to the first rising edge of $\overline{E}$ or $\overline{S1}$. By positioning the write pulse at different times within the $\overline{E}$ and $\overline{S1}$ low time (TELEH), various types of write cycles may be performed. If the $\overline{S1}$ low time (TS1LS1H) is greater than the $\overline{W}$ pulse plus an output enable time (TS1LQX), a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The HS-6551RH may be used on a common I/O bus structure by tying the input and output pins together. The multiplexing is accomplished internally by the $\overline{W}$ line. In the write cycle, when $\overline{W}$ goes low, the output buffers are forced to a high impedance state. One output disable time delay (TWLQZ) must be allowed before applying input data to the bus.

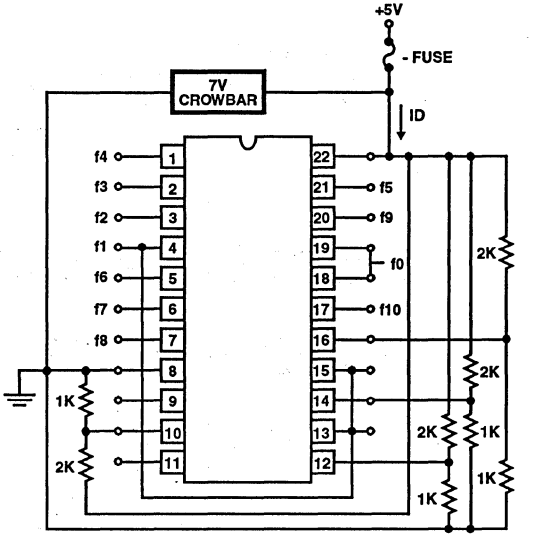
Burn-In Circuits



STATIC CONFIGURATION

NOTES:

VDD = 5.0V ± 10%
IDD + 1.5mA
R1 = 100K
R2 = 10k
Minimum Ambient Temperature = +125°C

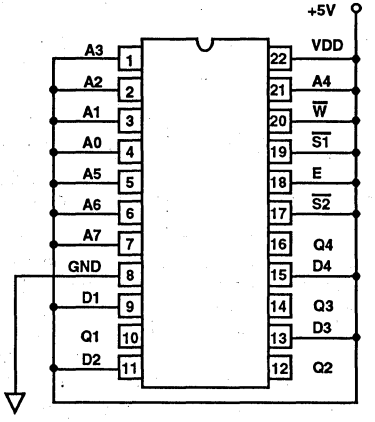


DYNAMIC CONFIGURATION

NOTES:

All resistors are ±20%, 1/4W
Use standard crowbar circuit with +7V zener diode
50% Duty Cycle square wave
IDMAX = 8mA/part
VIH = 4.0V, VIL = 0.8V
IL = ±1nA, CIN = 10pF
f0 = 500KHz; f1 = f0/2; f2 = f1/2; . . . f10 = f9/2

Irradiation Circuit



NOTES:

VDD = 5V
GND = 0V
All Inputs = 5V
All Q outputs float open

Harris - Space Level (-Q) Product Flow (Note 1)

SEM - Traceable to Diffusion Method 2018
Wafer Lot Acceptance Method 5007
Internal Visual Inspection Method 2010, Condition A
Gamma Radiation Assurance Tests Method 1019
Nondestructive Bond Pull Method 2023
Customer Pre-Cap Visual Inspection (Note 2)
Temperature Cycling Method 1010, Condition C
Constant Acceleration Method 2001, Condition E Min, Y1
Particle Impact Noise Detection Method 2020, Condition A
Electrical Tests (Harris' Option)
Serialization
X-Ray Inspection Method 2012
Electrical Tests - Subgroup 1; Read and Record (T0)
Static Burn-In Method 1015, Condition B, 72 Hrs, +125°C Min.
Interim 1 Electrical Tests - Subgroup 1; Read and Record (T1)
Burn-In Delta Calculation (T0 -T1)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Dynamic Burn-In Method 1015, Condition D, 240 Hrs, +125°C (Note 3)
Interim 2 Electrical Tests - Subgroup 1; Read and Record (T2)
Alternate Group A - Subgroups 1, 7, 9; Method 5005; Para 3.5.1.1
Burn-In Delta Calculation (T0 - T2)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Electrical Tests - Subgroup 3; Read and Record
Alternate Group A - Subgroups 3, 8B, 11; Method 5005; Para 3.5.1.1
Marking
Electrical Tests - Subgroup 2; Read and Record
Alternate Group A - Subgroups 2, 8A, 10; Method 5005; Para 3.5.1.1
Gross Leak Tests Method 1014, 100%
Fine Leak Tests Method 1014, 100%
Customer Source Inspection (Note 2)
Group B Inspection Method 5005 (Note 2)
End-Point Electrical Parameters: B-5 - Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11; B-6 - Subgroups 1, 7, 9
Group D Inspection Method 5005 (Notes 2, 4)
End-Point Electrical Parameters: Subgroups 1, 7, 9
External Visual Inspection Method 2009
Data Package Generation (Note 5)

NOTES:

1. The notes of Method 5004, Table 1 shall apply; Unless Otherwise Specified.
2. These steps are optional, and should be listed on the individual purchase order(s), when required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table 1 of Method 1015.
4. For Group D, Subgroup 3 inspection of package configurations which utilizes a gold plated lid in its construction; the inspection criteria for illegible markings criteria of Method 1010, paragraph 3.3 and of Method 1004, paragraph 3.8.a shall not apply.
5. Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (Including SEM Report)
   X-Ray Report and Film
   Test Variables Data

Harris -8 Product Flow

Internal Visual Inspection
Gamma Radiation Assurance Tests Method 1019
Customer Pre-Cap Visual Inspection (Note 1)
Temperature Cycling Method 1010, Condition C
Fine and Gross Leak Tests Method 1014
Constant Acceleration Method 2001 Y1 30KG
Initial Electrical Tests
Dynamic Burn-In Method 1015, Condition D, 160 Hrs, +125°C
+25°C Electrical Tests - Subgroups 1, 7, 9
PDA Calculation 5% Subgroups 1, 7
Electrical Tests +125°C, -55°C
Group A Inspection Method 5005. 5% PDA (Note 3)
Brand
Customer Source Inspection (Note 1)
Group C Inspection Method 5005 (Notes 1, 2)
Group D Inspection Method 5005 (Notes 1, 2)
External Visual Inspection Method 2009
Data Package Generation (Note 4)

NOTES:

1. These steps are optional, and must be negotiated as part of order.
2. Group B and D data package contains Attributes Data plus Variables Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable.
4. '-8' Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Radiation Testing Certificate of Conformance
   Certificate of Conformance (as found on shipper)

Metallization Topology

DIE DIMENSIONS:
Die Size: 132 x 160 mils
Die Thickness: 14 ±1 mils

METALLIZATION:
Type: Si-Al, 14kÅ ± 2kÅ
Back: Gold

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

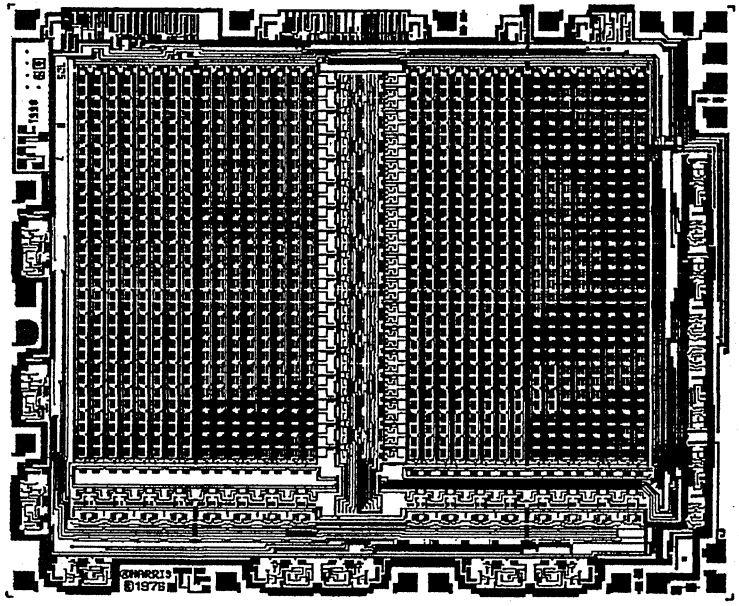
DIE ATTACH:
Material: Si-Au Eutectic Alloy
Temperature: Sidebrazed Ceramic DIP - 460°C±10°C (Max)
Braze Seal Flatpack- 460°C ± 10°C (Max)

WORST CASE CURRENT DENSITY: 5.8 x 10^4 A/cm^2

SUBSTRATE POTENTIAL: VDD

Metallization Mask Layout

HS-6551RH



HARRIS SEMICONDUCTOR

HS-6664RH

ADVANCE INFORMATION

December 1992

Radiation Hardened 8K x 8 CMOS PROM

Features

- 1.2 Micron Radiation Hardened Bulk CMOS
- Total Dose 3 x 10^6 RAD (Si)
- Transient Output Upset >1 x 10^9 RAD (Si)/s
- Single Event Upset < 1 x 10^{-10} Errors/Bit-Day
- Fast Access Time 50ns
- Single 5V Power Supply
- Single PUlse 10V Field Programmable
- Synchronous Operation
- On-Chip Address Latches
- Three-State Outputs
- NiCr Fuses
- Low Standby Current <500mA (Pre-Rad)
- Low Operating Current <30mA/MHz
- Military Temperature Range -55°C to +125°C

Description

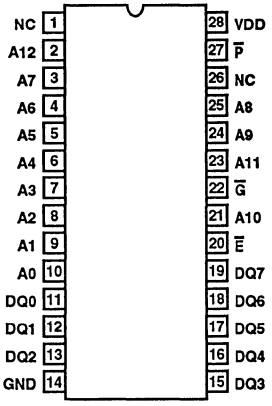
The Harris HS-6664RH is a radiation hardened 64K CMOS PROM, organized in an 8K word by 8-bit format. The chip is manufactured using a radiation hardened CMOS process, and utilizes synchronous circuit design techniques to achieve high speed performance with very low power dissipation.

On-chip address latches are provided, allowing easy interfacing with microprocessors that use a multiplexed address/data bus structure. The output enable control ($\overline{G}$) simplifies system interfaceing by allowing output data bus control in addition to the chip enable control ($\overline{E}$). All bits are manufactured storing a logical "0" and can be selectively programmed for a logical "1" at any bit location.

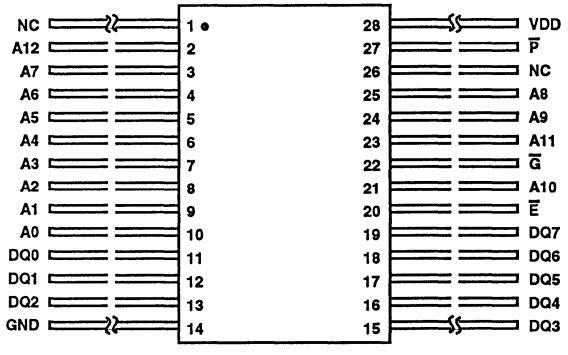
Applications for the HS-6664RH CMOS PROM include low power microprocessor based instrumentation and communcations systems, remote data acquisition and processing systems, and processor control store.

Pinouts

28 PIN CERAMIC DIP
CASE OUTLINE D10, CONFIGURATION 3
TOP VIEW



28 PIN FLATPACK
CASE OUTLINE F11A, CONFIGURATION 2
TOP VIEW

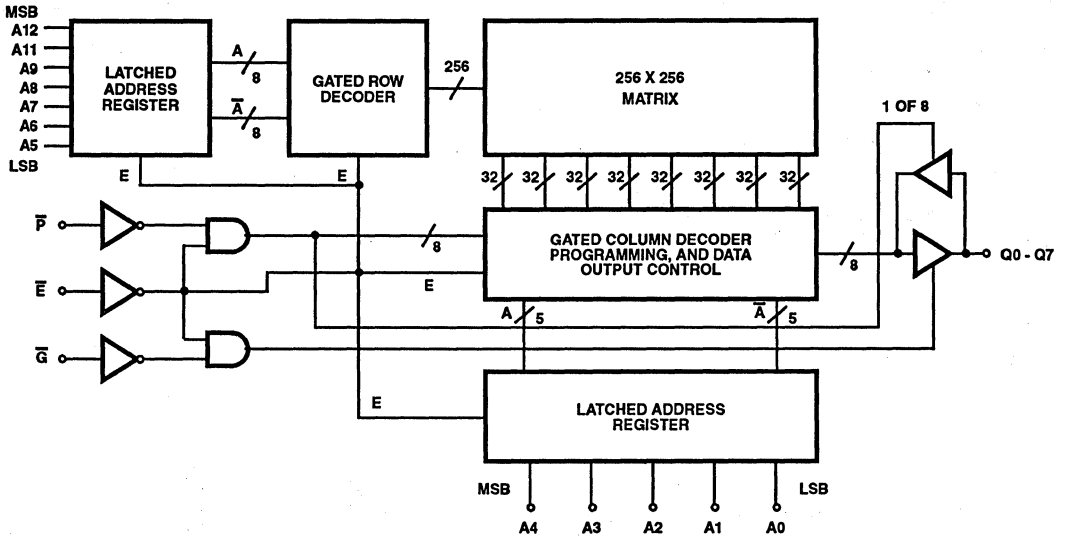


8 MEMORIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3197

Functional Diagram



HARRIS SEMICONDUCTOR

HS-6617RH

Radiation Hardened 2K x 8 CMOS PROM

December 1992

Features

- Total Dose 1 x 10^5 RAD (Si)
- Latch-Up Free >1 x 10^{12} RAD (Si)/s
- Field Programmable
- Functionally Equivalent to HM-6617
- Pin Compatible with Intel 2716
- Low Standby Power 550µW Max.
- Low Operating Power 137.5mW/MHz Max.
- Fast Access Time 100ns Max.
- TTL Compatible Inputs/Outputs
- Synchronous Operation
- On Chip Address Latches
- Three-State Outputs
- Nicrome Fuse Links
- Easy Microprocessor Interfacing
- Military Temperature Range -55°C to +125°C

Description

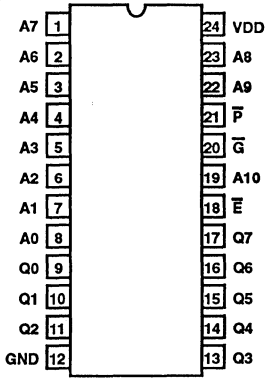
The Harris HS-6617RH is a radiation hardened 16K CMOS PROM, organized in a 2K word by 8-bit format. The chip is manufactured using a radiation hardened CMOS process, and is designed to be functionally equivalent to the HM-6617. Synchronous circuit design techniques combine with CMOS processing to give this device high speed performance with very low power dissipation.

On chip address latches are provided, allowing easy interfacing with recent generation microprocessors that use multiplexed address/data bus structure, such as the HS-80C85RH or HS-80C86RH. The output enable control ($\overline{G}$) simplifies microprocessor system interfacing by allowing output data bus control, in addition to, the chip enable control. Synchronous operation of the HS-6617RH is ideal for high speed pipe-lined architecture systems and also in synchronous logic replacement functions.

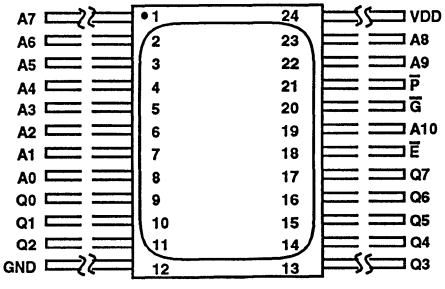
Applications for the HS-6617RH CMOS PROM include low power microprocessor based instrumentation and communications systems, remote data acquisition and processing systems, processor control store, and synchronous logic replacement.

Pinouts

24 PIN BRAZE SEAL DIP
CASE OUTLINE D3, CONFIGURATION 3
TOP VIEW



24 PIN FLATPACK CARRIER
CASE OUTLINE F6A, CONFIGURATION 2
TOP VIEW

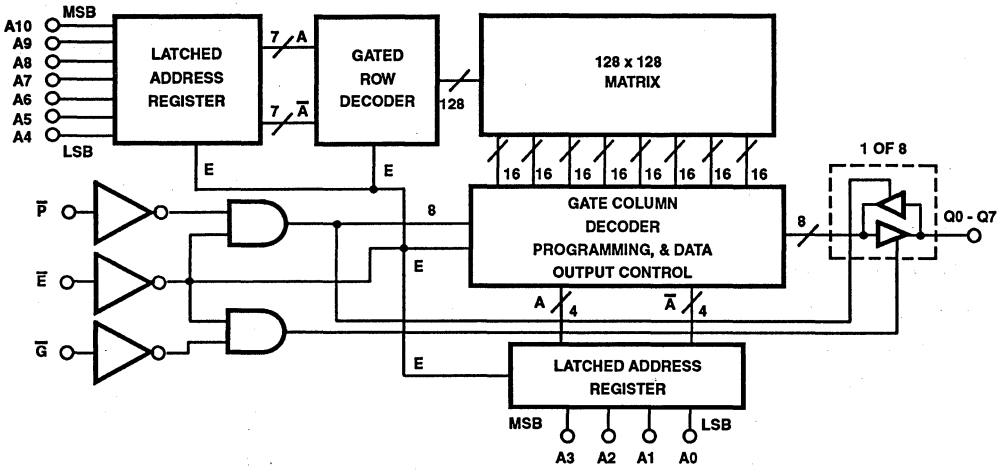


PIN	DESCRIPTION
A	Address Input
Q	Data Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program Enable ($\overline{P}$ Hardwired to VDD, except during programming)

8 MEMORIES

File Number 3033

Functional Diagram



ALL LINES POSITIVE LOGIC:
ACTIVE HIGH
THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

ADDRESS LATCHES & GATED DECODERS:
LATCH ON FALLING EDGE OF $\overline{E}$
GATE ON FALLING EDGE OF $\overline{G}$
$\overline{P}$ = HARDWIRED TO VDD EXCEPT DURING PROGRAMMING

TRUTH TABLE

$\overline{E}$	$\overline{G}$	MODE
0	0	Enabled
0	1	Output Disabled
1	X	Disabled

Absolute Maximum Ratings

Supply Voltage (All Voltages Reference to Device GND) . . . . +7.0V
Input or Output Voltage
Applied for All Grades. . . . . GND-0.3V to VDD+0.3V
Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature. . . . . +175°C
Lead Temperature (Soldering 10s). . . . . +300°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	56°C/W	12°C/W
Braze Seal Flatpack Package	91.3°C/W	11°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package 0.89W
Braze Seal Flatpack Package 0.55W
Gate Count . . . . . 5473 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage Range (VDD) . . . . . +4.5V to +5.5V
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input Low Voltage (VIL). . . . . 0V to +0.8V
Input High Voltage (VIH) . . . . . +2.4V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VDD = 4.5V, IO = -2.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.4	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, IO = 4.8mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
High Impedance Output Leakage Current	IOZ	VDD = 5.5V, $\overline{G}$ = 5.5V, VI/O = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10.0	10.0	µA
Input Leakage Current	II	VDD = 5.5V, VI = GND or VDD, $\overline{P}$ Not Tested	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	1.0	µA
Standby Supply Current	IDDSB	VDD = 5.5V, IO = 0mA, VI = VDD or GND	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	100	µA
Operating Supply Current	IDDOP	VDD = 5.5V, $\overline{G}$ = GND, (Note 3), f = 1MHz, IO = 0mA, VI = VDD or GND	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	25	mA
Functional Test	FT	VDD = 4.5V (Note 4)	7, 8A, 8B	-55°C ≤ T_A ≤ +125°C	-	-	-

NOTE:

1. All voltages referenced to device GND.
2. All tests performed with $\overline{P}$ hardwired to VDD.
3. Typical derating = 20mA/MHz increase in IDDOP.
4. Tested as follows: f = 1MHz, VIH = 2.4V, VIL = 0.8V, IOH = -1mA, IOL = +1mA, VOH ≥ 1.5V, VOL ≤ 1.5V.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

PARAMETERS	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Access Time	TAVQV	VDD = 4.5V and 5.5V (Note 4)	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	120	ns
Output Enable Access Time	TGLQV	VDD = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	50	ns
Chip Enable Access Time	TELQV	VDD = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	100	ns
Address Setup Time	TAVEL	VDD = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	20	-	ns
Address Hold Time	TELAX	VDD = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	25	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Guaranteed and 100% Tested.

PARAMETERS	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable Low Width	TELEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	120	-	ns
Chip Enable High Width	TEHEL	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	40	-	ns
Read Cycle Time	TELEL	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	160	-	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL ≥ 50pF.
3. All tests performed with $\overline{P}$ hardwired to VDD.
4. TAVQV = TELQV + TAVEL.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS, AC AND DC

PARAMETERS	SYMBOL	(NOTE 2) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz	1, 3	$T_A = +25°C$	-	10	pF
I/O Capacitance	CI/O	VDD = Open, f = 1MHz	1, 3	$T_A = +25°C$	-	12	pF
Chip Enable Time	TELQX	VDD = 4.5V and 5.5V	3	$-55°C \le T_A \le +125°C$	5	-	ns
Output Enable Time	TGLQX	VDD = 4.5V and 5.5V	3	$-55°C \le T_A \le +125°C$	5	-	ns
Chip Disable Time	TEHQZ	VDD = 4.5V and 5.5V	3	$-55°C \le T_A \le +125°C$	-	50	ns
Output Disable Time	TGHQZ	VDD = 4.5V and 5.5V	3	$-55°C \le T_A \le +125°C$	-	50	ns
Output High Voltage	VOH2	VDD = 4.5V, IO = 100µA	3	$-55°C \le T_A \le +125°C$	VDD-1V	-	V

NOTES:

1. All measurements referenced to device GND.
2. All tests performed with $\overline{P}$ hardwired to VDD.
3. The parameters listed are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after design or process changes which would affect these characteristics.

TABLE 4. POST 100K RAD AC AND DC ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: All AC and DC parameters are tested at the +25°C pre-irradiation limits.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

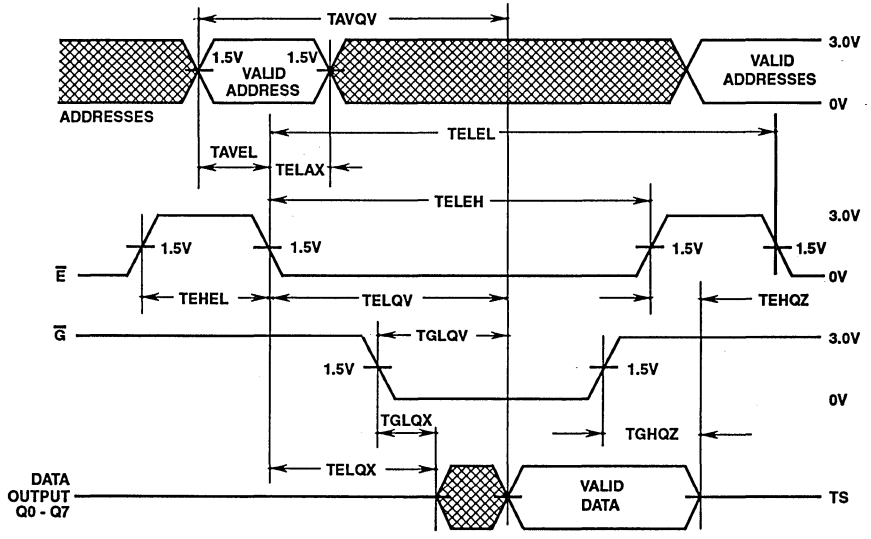
PARAMETER	SYMBOL	DELTA LIMITS
Standby Supply Current	IDDSB	±10µA
Input Leakage Current	IOZ	± 1µA
	II	±100nA
Output Low Voltage	VOL	± 60mV
Output High Voltage	VOH	± 400mV

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	-	-
Interim Test		100%/5004	1, 7, 9	1, 7, 9
PDA		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (*Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B	N/A
	Others	Samples/5005	1, 7	N/A
Group C (Optional)		Samples/5005	N/A	1, 7
Group D (Optional)		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7	1, 7

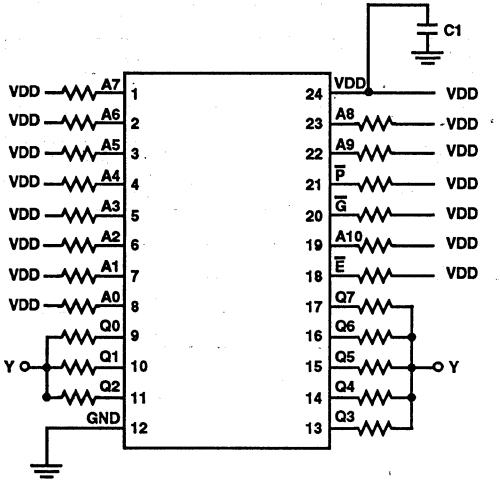
Timing Waveform

READ CYCLE



Burn-In Circuits

HS-6617RH 24 PIN BRAZE SEAL DIP AND FLATPACK

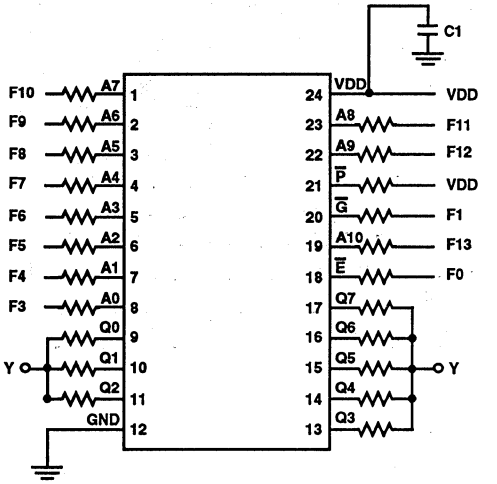


STATIC CONFIGURATION

NOTES:

VDD = 6.0V ± 0.5V
C1 = 0.01µF (Min)
All Resistors = 47kΩ ± 5%
Y = 2.7V ± 10%

HS-6617RH 24 PIN BRAZE SEAL DIP AND FLATPACK



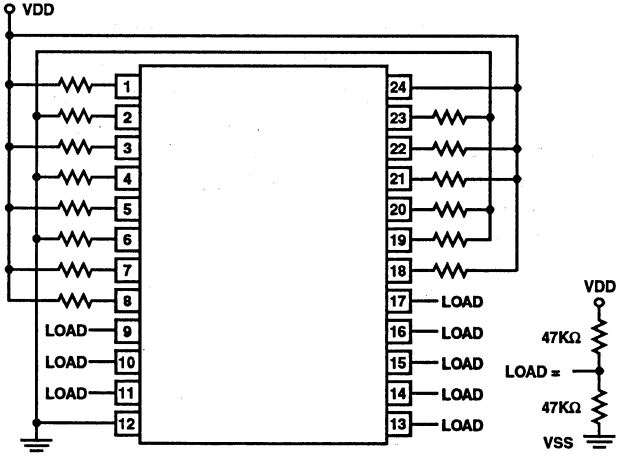
DYNAMIC CONFIGURATION

NOTES:

VDD = 6.0V ± 0.5V
VIH = 4.5V± 10%
VIL = 6V (Max)
C1 = 0.01µF (Min)
All Resistors = 47kΩ ± 5%
F0 = 100KHz ± 10%, 40 - 60% duty cycle
F1 = F0/2 . . . F13 = F12/2
Y = 2.7V ± 10%

Irradiation Circuit

HS-6617RH 24 PIN FLATPACK



NOTES:

Power Supply: VDD = 5.5V
All Registors = 47KΩ

Harris - Space Level (-Q) Product Flow (Note 1)

SEM - Traceable to Diffusion Method 2018
Wafer Lot Acceptance Method 5007
Internal Visual Inspection Method 2010, Condition A
Gamma Radiation Assurance Tests Method 1019
Nondestructive Bond Pull Method 2023
Customer Pre-Cap Visual Inspection (Note 2)
Temperature Cycling Method 1010, Condition C
Constant Acceleration Method 2001, Condition E Min, Y1
Particle Impact Noise Detection Method 2020, Condition A
Electrical Tests (Harris' Option)
Serialization
X-Ray Inspection Method 2012
Electrical Tests - Subgroup 1; Read and Record (T0)
Static Burn-In Method 1015, Condition B, 72 Hrs, +125°C Min.
Interim 1 Electrical Tests - Subgroup 1; Read and Record (T1)
Burn-In Delta Calculation (T0 -T1)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Dynamic Burn-In Method 1015, Condition D, 240 Hrs, +125°C (Note 3)
Interim 2 Electrical Tests - Subgroup 1; Read and Record (T2)
Alternate Group A - Subgroups 1, 7, 9; Method 5005; Para 3.5.1.1
Burn-In Delta Calculation (T0 - T2)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Electrical Tests - Subgroup 3; Read and Record
Alternate Group A - Subgroups 3, 8B, 11; Method 5005; Para 3.5.1.1
Marking
Electrical Tests - Subgroup 2; Read and Record
Alternate Group A - Subgroups 2, 8A, 10; Method 5005; Para 3.5.1.1
Gross Leak Tests Method 1014, 100%
Fine Leak Tests Method 1014, 100%
Customer Source Inspection (Note 2)
Group B Inspection Method 5005 (Note 2)
End-Point Electrical Parameters: B-5 - Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11; B-6 - Subgroups 1, 7, 9
Group D Inspection Method 5005 (Notes 2, 4)
End-Point Electrical Parameters: Subgroups 1, 7, 9
External Visual Inspection Method 2009
Data Package Generation (Note 5)

NOTES:

1. The notes of Method 5004, Table 1 shall apply; Unless Otherwise Specified.
2. These steps are optional, and should be listed on the individual purchase order(s), when required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table 1 of Method 1015.
4. For Group D, Subgroup 3 inspection of package configurations which utilizes a gold plated lid in its construction; the inspection criteria for illegible markings criteria of Method 1010, paragraph 3.3 and of Method 1004, paragraph 3.8.a shall not apply.
5. Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (Including SEM Report)
   X-Ray Report and Film
   Test Variables Data

Harris -8 Product Flow

Internal Visual Inspection
Gamma Radiation Assurance Tests Method 1019
Customer Pre-Cap Visual Inspection (Note 1)
Temperature Cycling Method 1010, Condition C
Fine and Gross Leak Tests Method 1014
Constant Acceleration Method 2001 Y1 30KG
Initial Electrical Tests
Dynamic Burn-In Method 1015, Condition D, 160 Hrs, +125°C
+25°C Electrical Tests - Subgroups 1, 7, 9
PDA Calculation 5% Subgroups 1, 7
Electrical Tests +125°C, -55°C
Group A Inspection Method 5005. 5% PDA (Note 3)
Brand
Customer Source Inspection (Note 1)
Group C Inspection Method 5005 (Notes 1, 2)
Group D Inspection Method 5005 (Notes 1, 2)
External Visual Inspection Method 2009
Data Package Generation (Note 4)

NOTES:

1. These steps are optional, and must be negotiated as part of order.
2. Group B and D data package contains Attributes Data plus Variables Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable.
4. '-8' Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Radiation Testing Certificate of Conformance
   Certificate of Conformance (as found on shipper)

Metallization Topology

DIE DIMENSIONS:
164 x 250 x 19 ±1mils

METALLIZATION:
Type: Silicon-Aluminum
Thickness: 13kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

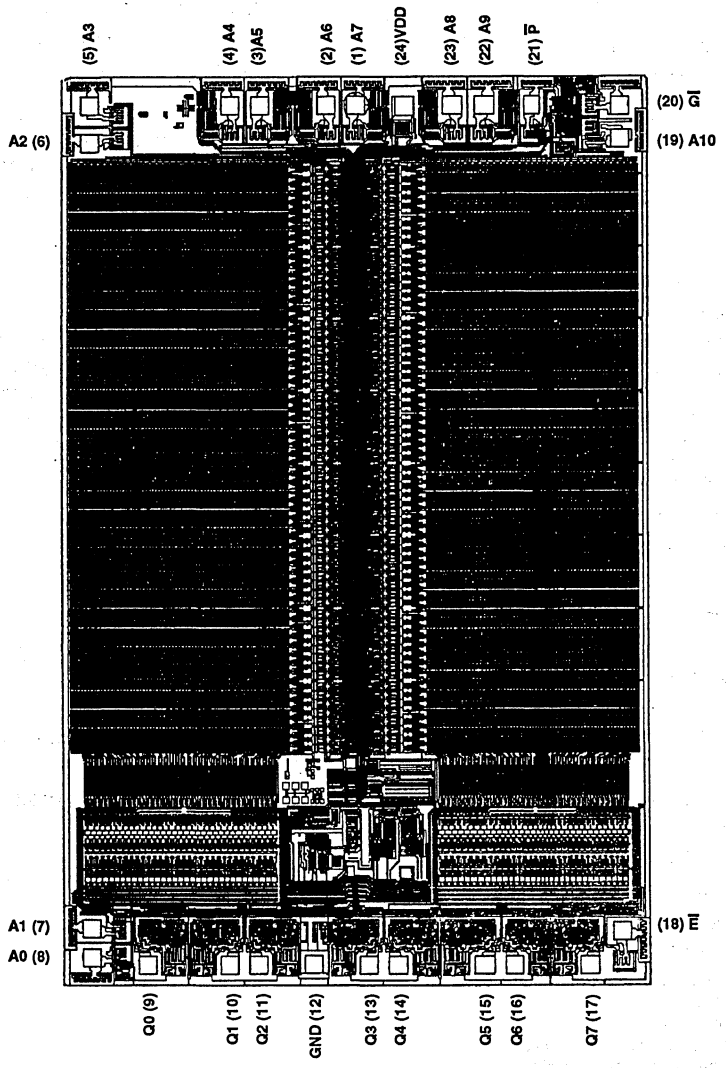
DIE ATTACH:
Material: SI - Au Eutectic Alloy
Temperature: Ceramic DIP - 460°C (Max)
Braze Seal Flatpack - 460°C (Max)

WORST CASE CURRENT DENSITY:
1×10^5 A/cm^2

SUBSTRATE POTENTIAL: VDD

Metallization Mask Layout

HS-6617RH



DESIGN INFORMATION

December 1992

2K x 8 CMOS PROM

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Background Information HS-6617RH Programming

PROGRAMMING SPECIFICATIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input "0"	VIL	0.0	0.2	0.8	V	
Voltage "1"	VIH	VDD-2	VDD	VDD+0.3	V	6
Programming VDD	VDDPROG	10.0	10.0	10.0	V	2
Operating VDD	VDD1	4.5	5.5	5.5	V	
Special Verify	VDD2	4.0	-	6.0	V	3
Delay Time	td	1.0	1.0	-	µs	
Rise Time	tr	1.0	10.0	10.0	µs	
Fall Time	tf	1.0	10.0	10.0	µs	
Chip Enable Pulse Width	TEHEL	50	-	-	ns	
Address Valid to Chip Enable Low Time	TAVEL	20	-	-	ns	
Chip Enable Low to Output Valid Time	TELQV	-	-	120	ns	
Programming Pulse Width	tpw	90	100	110	µs	4
Input Leakage at VDD = VDDPROG	tIP	-10	+1.0	10	µA	
Data Output Current at VDD = VDDPROG	IOP	-	-5.0	-10	mA	
Output Pull-Up Resistor	Rn	5	10	15	kΩ	5
Ambient Temperature	T_A	-	25	-	°C	

NOTES:

1. All inputs must track VDD (pin 24) within these limits.
2. VDDPROG must be capable of supplying 500mA. VDDPROG Power Supply tolerence ±3% (Max.)
3. See Steps 22 through 29 of the Programming Algorithm.
4. See Step 11 of the Programming Algorithm.
5. All outputs should be pulled up to VDD through a resistor of value Rn.
6. Except during programming (See Programming Cycle Waveforms).

DESIGN INFORMATION (Continued)

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Background Information Programming

The HS-6617 CMOS PROM is manufactured with all bits containing a logical zero (output low). Any bit can be programmed selectively to a logical one (output high) state by following the procedure shown below. To accomplish this, a programmer can be built that meets the specifications shown, or use of an approved commercial programmer is recommended.

PROGRAMMING SEQUENCE OF EVENTS

1. Apply a voltage of VDD1 to VDD of the PROM.
2. Read all fuse locations to verify that the PROM is blank (output low).
3. Place the PROM in the initial state for programming: $\overline{E}$ = VIH, $\overline{P}$ = VIH, $\overline{G}$ = VIL.
4. Apply the correct binary address for the word to be programmed. No inputs should be left open circuit.
5. After a delay of td, apply voltage of VIL to $\overline{E}$ (pin 18) to access the addressed word.
6. The address may be held through the cycle, but must be held valid at least for a time equal to td after the falling edge of $\overline{E}$. None of the inputs should be allowed to float to an invalid logic level.
7. After a delay of td, disable the outputs by applying a voltage of VIH to $\overline{G}$ (pin 20).
8. After a delay of td, apply voltage of VIL to $\overline{P}$ (pin 21).
9. After delay of td, raise VDD (pin 24) to VDDPROG with a rise time of tr. All outputs at VIH should track VDD within VDD-2.0V to VDD+0.3V. This could be accomplished by pulling outputs at VIH to VDD through pull-up resistors of value Rn.
10. After a delay of td, pull the output which corresponds to the bit to be programmed to VIL. Only one bit should be programmed at a time.
11. After a delay of tpw, allow the output to be pulled to VIH through pull-up resistor Rn.
12. After a delay of td, reduce VDD (pin 24) to VDD1 with a fall time of tf. All outputs at VIH should track VDD with VDD-2.0V to VDD+0.3V. This could be accomplished by pulling outputs at VIH to VDD through pull-up resis- tors of value Rn.
13. Apply a voltage of VIH to $\overline{P}$ (pin 21).
14. After a delay of td, apply a voltage of VIL to $\overline{G}$ (pin 20).
15. After a delay of td, examine the outputs for correct data. If any location verifies incorrectly, it should be considered a programming reject.
16. Repeat steps 3 through 15 for all other bits to be programmed in the PROM.

POST-PROGRAMMING VERIFICATION

17. Place the PROM in the post-programming verification mode: $\overline{E}$ = VIH, $\overline{G}$ = VIL, $\overline{P}$ = VIH, VDD (pin 24) = VDD1.
18. Apply the correct binary address of the word to be verified to the PROM.
19. After a delay of td, apply a voltage of VIL to $\overline{E}$ (pin 18).
20. After a delay of td, examine the outputs for correct data. If any location fails to verify correctly, the PROM should be considered a programming reject.
21. Repeat steps 17 through 20 for all possible programming locations.

POST-PROGRAMMING READ

22. Apply a voltage of VDD2 = 4.0V to VDD (pin 24).
23. After a delay of td, apply a voltage of VIH to $\overline{E}$ (pin 18).
24. Apply the correct binary address of the word to be read.
25. After a delay of TAVEL, apply a voltage of VIL to $\overline{E}$ (pin 18).
26. After a delay of TELQV, examine the outputs for correct data. If any location fails to verify correctly, the PROM should be considered a programming reject.
27. Repeat steps 23 through 26 for all address locations.
28. Apply a voltage of VDD2 = 6.0V to VDD (pin 24).
29. Repeat steps 23 through 26 for all address locations.

DESIGN INFORMATION (Continued)

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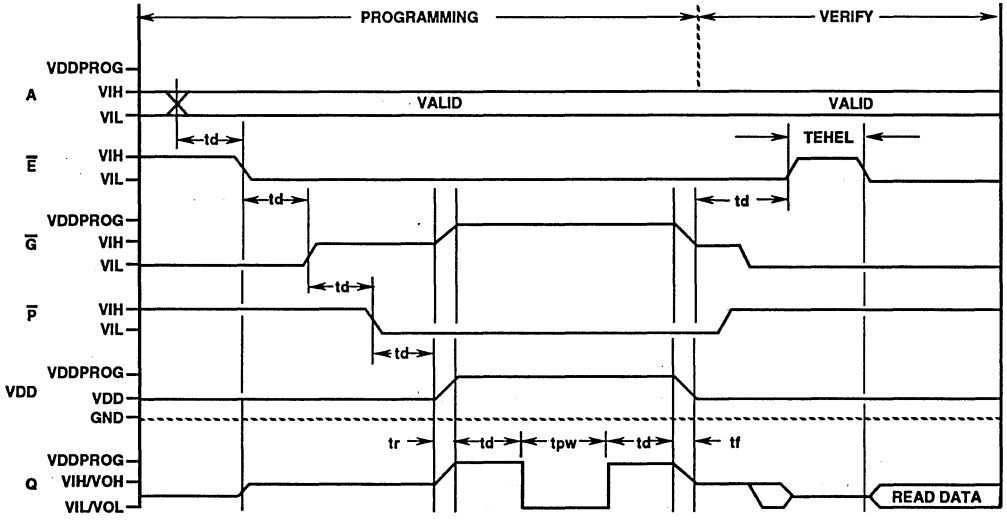
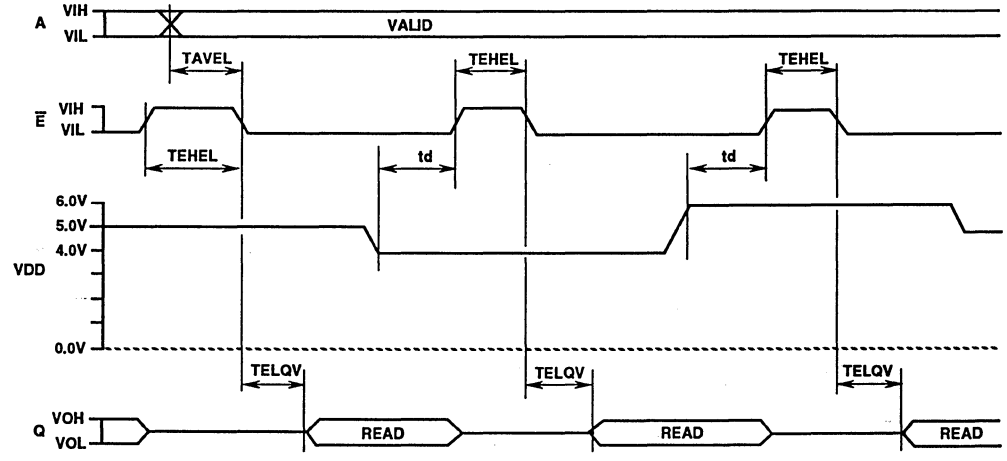
HS-6617RH PROGRAMMING CYCLE



HS-6617RH POST PROGRAMMING VERIFY CYCLE



RAD HARD 9

SERIAL COMMUNICATIONS

HARRIS SEMICONDUCTOR

HS-245RH
RADIATION HARDENED TRIPLE LINE TRANSMITTER

HS-246RH, HS-249RH
RADIATION HARDENED TRIPLE LINE RECEIVERS

HS-248RH
RADIATION HARDENED TRIPLE PARTY-LINE RECEIVER

December 1992

Features

- Radiation Hardened DI Processing
  - Total Dose (γ) 2 x 10^5 Rads (Si)
  - Transient Upset ($\dot{\gamma}$) Upset 1 x 10^9 Rads (Si)/s
  - Latchup Free
  - Neutron Fluence 5 x 10^{12} N/cm2
- Replaces HD-245/246/248/249
- Current Mode Operation
- High Speed 15MHz with 50 Foot Cable; 2MHz with 1000 Foot Cable
- High Noise Immunity
- Low EMI Generation
- Low Power Dissipation
- High Common Mode Rejection
- Transmitter and Receiver Party Line Capability
- Tolerates -2.0V to +20.0V Ground Differential (Transmitter with Respect to Receiver)
- Transmitter Input/Receiver Output TTL/DTL Compatible

Description

The HS-245RH/246RH/248RH/249RH radiation hardened triple line transmitter and triple line receivers are fabricated using the Harris dielectric isolation process. These parts are identical in pinout and function to the original HD-245/246/248/249. They are also die size and bond pad placement compatible with the original parts for those customers who buy dice for hybrid assembly.

Each transmitter-receiver combination provides a digital interface between systems linked by 100Ω twisted pair, shielded cable. Each device contains three circuits fabricated within a single monolithic chip. Data rates greater than 15MHz are possible depending on transmission line loss characteristics and length.

The transmitter employs constant current switching which provides high noise immunity along with high speeds, low power dissipation, low EMI generation and the ability to drive high capacitance loads. In addition, the transmitters can be turned "off" allowing several transmitters to time-share a single line.

Receiver input/output differences are shown in the table:

PART NO.	INPUT	OUTPUT
HS-246RH	100Ω	Open Collector
HS-248RH	Hi-Z	6K Pull-Up Resistors
HS-249RH	100Ω	6K Pull-Up Resistors

The internal 100V cable termination consists of 50Ω from each input to ground.

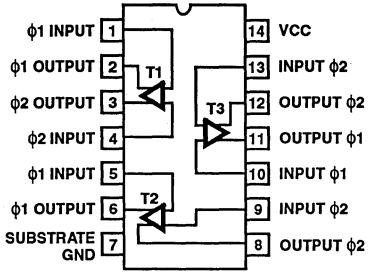
HS-248RH "party line" receivers have a Hi-Z input such that as many as ten of these receivers can be used on a single transmission line.

Each transmitter input and receiver output can be connected to TTL and DTL systems. When used with shielded transmission line, the transmitter-receiver system has very high immunity to capacitance and magnetic noise coupling from adjacent conductors. The system can tolerate ground differentials of -2.0V to +20.0V (transmitter with respect to receiver).

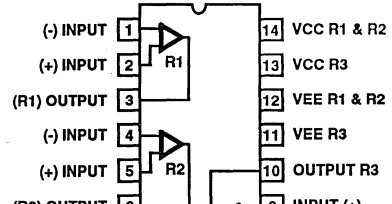
These parts are available in Class B or Class S processing.

Pinouts

HS9-245RH 14 PIN FLATPACK
HS1-245RH 14 CERAMIC DIP
CASE OUTLINE D1, CONFIGURATION 3
TOP VIEW



HS9-245RH/248RH/249RH 14 PIN FLATPACK
HS1-246RH/248RH/249RH 14 PIN CERAMIC DIP
CASE OUTLINE F-2A CONFIGURATION 2
TOP VIEW



9 SERIAL COMMUNICATIONS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3034

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +10V
Output Voltage ..... -30V to 0.5V with respect to VCC
Input Voltage ..... -0.5V to 10V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +275°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Flatpack Package	75°C/W	13°C/W
Sidebraze DIP Package	67°C/W	16°C/W

Maximum Package Power Dissipation at +125°C
Flatpack Package 0.5W
Sidebraze DIP Package 0.5W
Transistor Count 6

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C

TABLE 1. HS-245RH DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Low Current	IIL	VCC = 5.5V, Note 1	1, 2, 3	-55°C < T_A < +125°C	-2.8	-	mA
ON Output Current	IOUT "On"	VCC = 4.5V, 5.5V, Notes 1, 2	1, 2, 3	-55°C < T_A < +125°C	-5.6	-1.0	mA
ON Output Current Unbalance	ΔIOUT	VCC = 5.5V, Note 3	1, 2, 3	-55°C < T_A < +125°C	-	380	µA
OFF Output Current	IOUT "Off"	VCC = 4.5V, Note 1	1, 2, 3	-55°C < T_A < +125°C	-100	-	µA
Output Breakdown	BVCER	VCC = 0.0V, Note 4	1	T_A = +25°C	-30	-	V
Power Supply Current	ICC	VCC = 5.5V, Note 5, 6	1	T_A = +25°C	-	21	mA

NOTES:

1. One input at GND, one input open, each output at GND.
2. One input at 0.45V, one input open, each output at GND.
3. Difference between ϕ1 and ϕ2 "ON" output data current.
4. Each input at GND, one output at GND, ILIMIT > -100µA on output tested with -30V applied.
5. One input of each transmitter at GND and the other input open. All six output lines at GND.
6. All six input lines open, all six output lines at GND.

TABLE 2. HS-245RH AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPLH TPHL	VCC = 4.5V, 5.5V	9, 10, 11	-55°C < T_A < +125°C	-	14	ns

Absolute Maximum Ratings

Supply Voltage (VCC) ..... -0.5V to +8.0V
Supply Voltage (VEE) ..... -8.0V to +0.5V
Output Voltage ..... -0.5V to +6.0V
Input Voltage ..... -1.0V to +1.0V
Input Current ..... -25mA to +25mA
Output Current 50mA
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +275°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Flatpack Package	75°C/W	13°C/W
Sidebraze DIP Package	67°C/W	16°C/W

Maximum Package Power Dissipation at +125°C
Flatpack Package 0.5W
Sidebraze DIP Package 0.5W
Transistor Count 9

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C

TABLE 1. HS-246RH, HS-248RH, HS-249RH DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Resistance	RIN	VCC = 5.0V, VEE = -5.0V (HS-246RH & HS-249RH)	1, 2, 3	-55°C < T_A < +125°C	39	90	Ω
Pullup Resistance	RPU	VCC = 5.0V, VEE = -5.0V (HS-246RH & HS-249RH)	1, 2, 3	-55°C < T_A < +125°C	4.1	10.5	kΩ
Logical "1" Output Voltage	VOH	VCC = 4.5V, VEE = -4.5, IOH = -120mA (HS-248RH & HS-249RH) Note 1	1, 2, 3	-55°C < T_A < +125°C	2.5	-	V
Logical "0" Output Voltage	VOL	VCC = 4.5V, VEE = -4.5, IOH = 9.6mA (HS-248RH & HS-249RH) Note 2	1, 2, 3	-55°C < T_A < +125°C	-	0.45	V
		VCC = 4.5V, VEE = -4.5, IOH = 10mA (HS-246) Note 2	1, 2, 3	-55°C < T_A < +125°C	-	0.45	V
Logical "0" Output Voltage, Input Short Circuit	VOLSC	VCC = 4.5V, VEE = -4.5, IOL = 3.2mA, Note 3	1	T_A = +25°C	-	0.45	V
Power Supply Current	ICC	VCC = 5.5V, VEE = -5.5V (HS-246RH) Note 4, 5	1	T_A = +25°C	-	6.6	mA
		VCC = 5.5, VEE = -5.5V (HS-248RH & HS-249RH) Note 4, 5	1	T_A = +25°C	-	7.8	mA
Power Supply Current	IEE	VCC = 5.5V, VEE = -5.5V Note 4, 5	1	T_A = +25°C	-	6.0	mA

NOTES:

1. (+) IIN = 1.5mA; (-) Input = Open. (For HS-248RH Ext. 50Ω Res. or 0.75mV)
2. (+) Input = Open; (-) IIN = 1.5mA. (For HS-248 Ext. 50Ω Res. or 0.75mV)
3. Both inputs shorted to GND; or both input open such that 50Ω termination resistors are in the circuit.
4. (+) Input = Open; (-) IIN = 3mA
5. (+) IIN = 3mA; (-) Input = Open

TABLE 2. HS-246RH, HS-248RH, HS-249RH AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay	TPLH TPHL	VCC = 4.5V, VEE = -4.5V	9, 10, 11	-55°C < T_A < +125°C	-	30	ns

TABLE 4. POST RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

The post RAD electrical performance characteristics are the same as the parameters listed in tables 1 and 2

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C) AND GROUP B, SUBGROUP 5 DELTA PARAMETERS

PARAMETER	SYMBOL	DELTA LIMITS
Input Leakage Current (HS-245RH)	IIL	±280nA
ON Output Current (HS-245RH)	IOUT(ON)	±560µA
OFF Output Current (HS-245RH)	IOUT(OFF)	±20µA
Power Supply Current (HS-245RH)	ICC	±2.1mA
Low Level Output Voltage (HS-246RH, HS-248RH, HS-249RH)	VOL	±90mV
High Level Output Voltage (HS-246RH, HS-248RH, HS-249RH)	VOH	±500mV
Power Supply Current (HS-245RH, HS-248RH, HS-249RH)	ICC	±2mA
Power Supply Current (HS-246RH, HS-248RH, HS-249RH)	IEE	±2mA

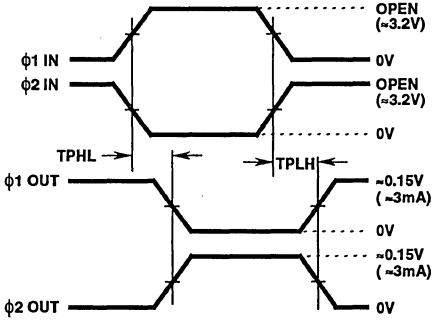
TABLE 6. HS-245RH, HS-246RH, HS-248RH, HS-249RH APPLICABLE SUBGROUPS

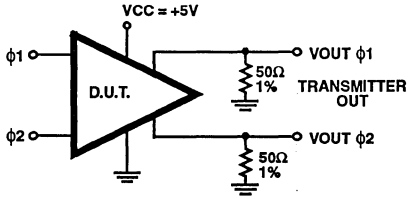
CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS
Initial Test		100%/5004	1
Interim Test		100%/5004	1
PDA		100%/5004	1
Final Test		100%/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B	B5	Samples/5005	1, 2, 3
	Others	Samples/5005	1
Group D		Samples/5005	1
Group E, Subgroup 2		Samples/5005	1, 7

Test Circuits and Applications

CIRCUIT #1 TRANSMITTER PROPAGATION DELAY

NOTES:
Input: TTLH ≤ 10ns
TTHL ≤ 10ns
pw = 500ns
f = 1MHz
$IOUT = \frac{VOUT}{50\Omega}$

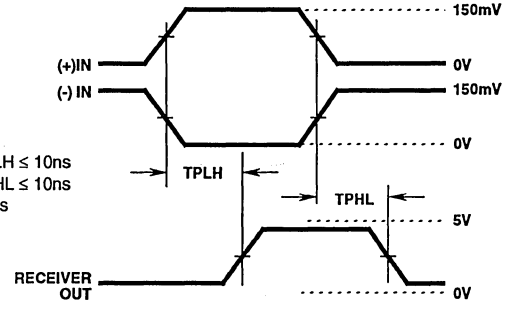


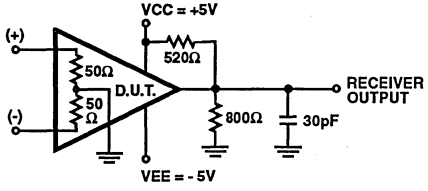


All timing measurements referenced to 50% V points

CIRCUIT #2 RECEIVER PROPAGATION DELAY

NOTES:
Input: TTLH ≤ 10ns
TTHL ≤ 10ns
pw = 500ns
f = 1MHz

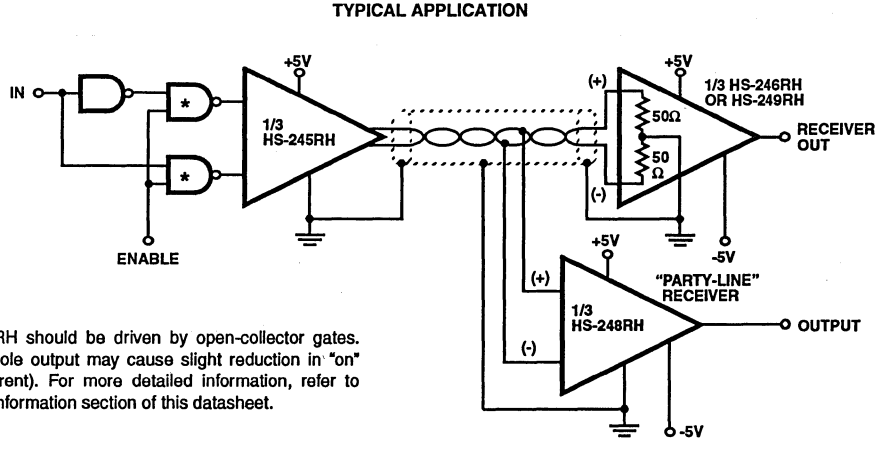




All timing measurements referenced to 50% V points

NOTE: External 50Ω resistors needed for HS-248RH

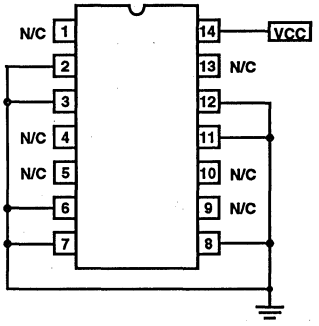
TYPICAL APPLICATION



* HS-245RH should be driven by open-collector gates. (Totem-pole output may cause slight reduction in "on" data current). For more detailed information, refer to Design Information section of this datasheet.

Burn-In Circuits

HS9-245RH (FLATPACK)
HS1-245RH (CERAMIC DIP)

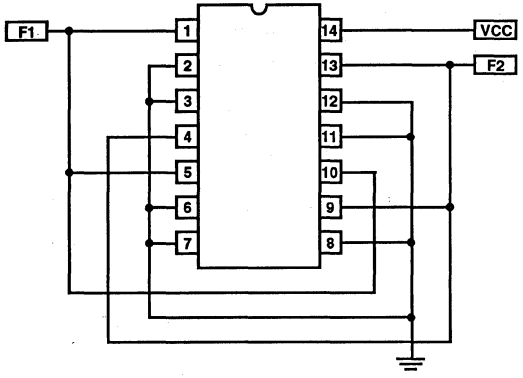


STATIC

NOTES:

VCC = 5.0V ± 10%
T_A (Min) = +125°C

HS9-245RH (FLATPACK)
HS1-245RH (CERAMIC DIP)

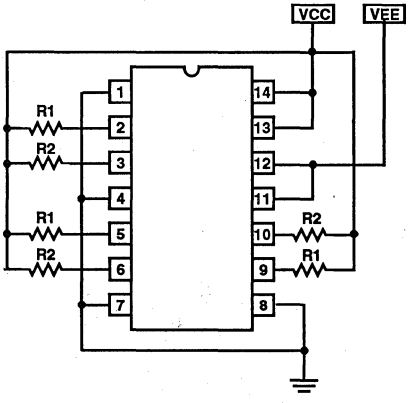


DYNAMIC

NOTES:

VCC = 5.0V ± 10%
T_A (Min) = +125°C
F1 = 10KHz, 0V to +4.5V Squarewave
F2 = 10KHz, +4.5 V to 0V Squarewave

HS9-246RH, HS9-248RH, HS9-249RH (FLATPACK)
HS1-246RH, HS1-248RH, HS1-249RH (CERAMIC DIP)

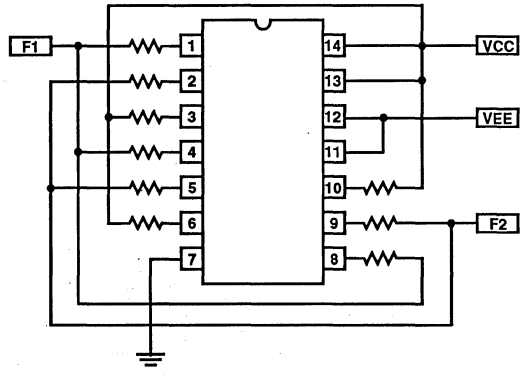


STATIC

NOTES:

VCC = 5.0V ± 10%
VEE = -5.0V ± 10%
T_A (Min) = +125°C
R1 = 2.1kΩ ± 10%, 1/4W
R2 = 6.0kΩ ± 10%, 1/4W

HS9-246RH, HS9-248RH, HS9-249RH (FLATPACK)
HS1-246RH, HS1-248RH, HS1-249RH (CERAMIC DIP)



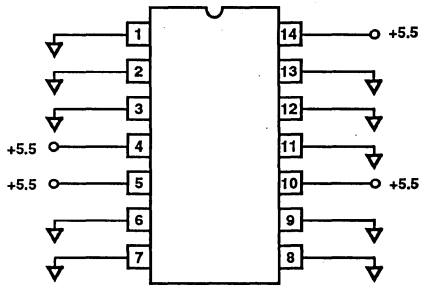
DYNAMIC

NOTES:

VCC = 5.0V ± 10%
VEE = -5.0V ± 10%
T_A (Min) = +125°C
F1 = 10KHz, 0V to +1V Squarewave
F2 = 10KHz, +1V to 0V Squarewave
All resistors 1.0kΩ ± 10%, 1/4W (Min)

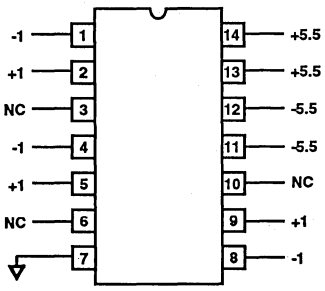
Irradiation Circuits

HS1-245RH



GAMMA BIAS CIRCUIT

HS1-246RH, HS1-248RH, HS1-249RH

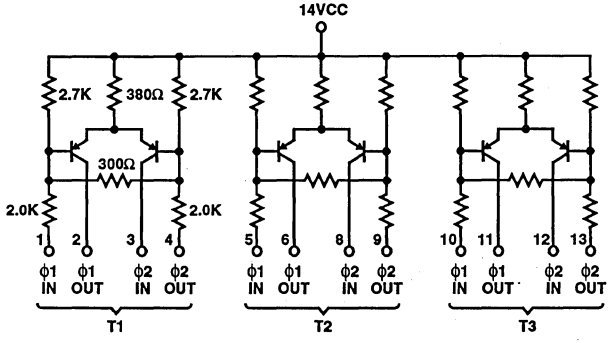


GAMMA BIAS CIRCUIT

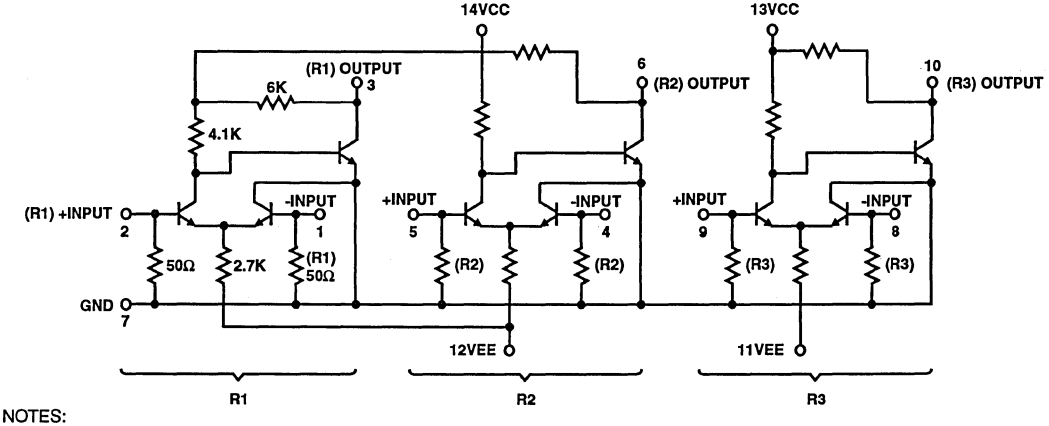
NOTE: All irradiation testing is performed in the ceramic DIP package

Schematics

HS-245RH



HS-246RH, HS-248RH, HS249RH



NOTES:

1. HS-249RH is as shown
2. HS-246RH does not have 6K output pull-up resistors
3. HS-248RH does not have 50Ω input termination resistors

Harris - Space Level Product Flow

SEM - Traceable to Diffusion Method 2018

Wafer Lot Acceptance Method 5007

Internal Visual Inspection (Note 1)

Gamma Radiation Assurance Tests Method 1019

100% Nondestructive Bond Pull Method 2023

Customer Pre-Cap Visual Inspection (Notes 1, 2)

Temperature Cycling Method 1010 Condition C

Constant Acceleration Method 2001 Y1 30KG

Particle Impact Noise Detection method 2020, Condition A 20G

Marking and Serialization

X-Ray Inspection Method 2012

Initial Electrical Tests (T0)

Static Burn-In 72 Hour, +125°C method 1015 Condition A

Room Temperature Electrical Tests (T1)

Burn-In Delta Calculation (T0-T1)

PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ

Dynamic Burn-In 240 Hours, +125°C Method 1015 Condition D

Electrical Tests Subgroups 1, 7, 9 (T2)

Burn-In Delta Calculation (T0-T2)

PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ

Electrical Test +125°C, -55°C

Group A Inspection Method 5005

Fine and Gross Leak Tests Method 1014

Customer Source Inspection (Note 2)

Group B Inspection (Notes 2, 4) Method 5005

Group D Inspection (Notes 2, 4) Method 5005

External Visual Inspection Method 2009

Data Package Generation (Note 3)

NOTES:

1. Visual Inspection is performed to MIL-STD-883 Method 2010, Condition A.
2. These steps are optional, and should be listed on the purchase order if required.
3. Data package contains: Assembly Attributes (post seal)
   Test Attributes (includes Group A) -55°C, +25°C, +125°C
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (includes SEM report)
   X-Ray Report and Film
   Test Variables Data, DC Test and TELQV
   +25°C Initial Test
   +25°C Interim Test 1
   +25°C Interim Test 2
   +25°C Delta Over Burn-In
4. Group B data package contains Attributes Data pulse Variables Data, DC Test and TE2HQV. Group D data package contains Attributes only.

Metallization Topology

DIE DIMENSIONS:
45 x 45 x 11 mils
(1140 x 1140 x 280µm

METALLIZATION:
Type: Aluminum
Thickness: 12.5kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
7.8×10^4 A/cm^2

GLASSIVATION:
Type: Silox
Thickness: 8kÅ ± 1kÅ

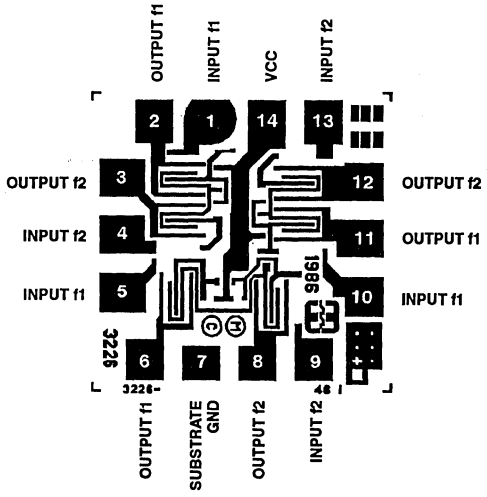
TRANSISTOR COUNT: 6

PROCESS:
HFSB Bipolar/Dielectric Isolation

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP - 460°C (Max)

Metallization Mask Layout

HS-245RH



Metallization Topology

DIE DIMENSIONS:
45 x 47 x 11 mils
(1140 x 1190 x 280µm

METALLIZATION:
Type: T.W.
Thickness: 2.5kÅ ± 0.5kÅ
Type: Al
Thickness: 14kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
1.4×10^5 A/cm^2

GLASSIVATION:
Type: Silox
Thickness: 8kÅ ± 1kÅ

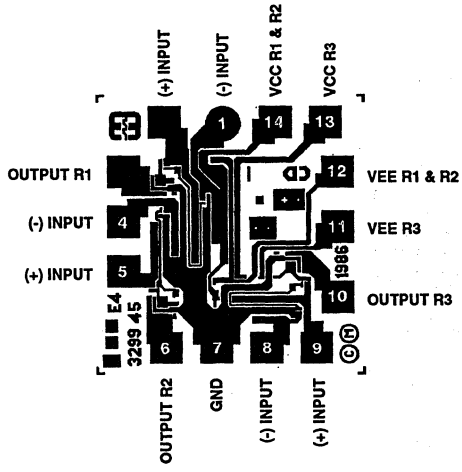
TRANSISTOR COUNT: 9

PROCESS:
ALPS Bipolar/Dielectric Isolation

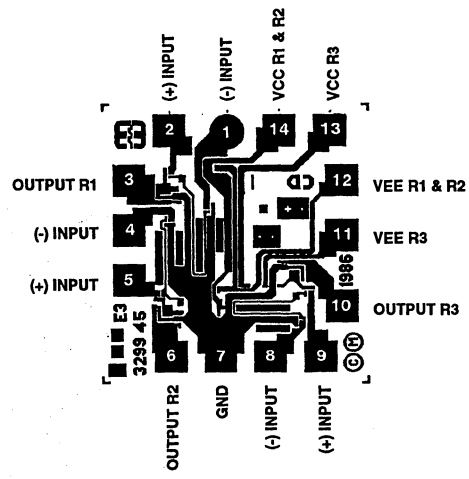
DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP - 460°C (Max)
Flatpack - 460°C (Max)

Metallization Mask Layout

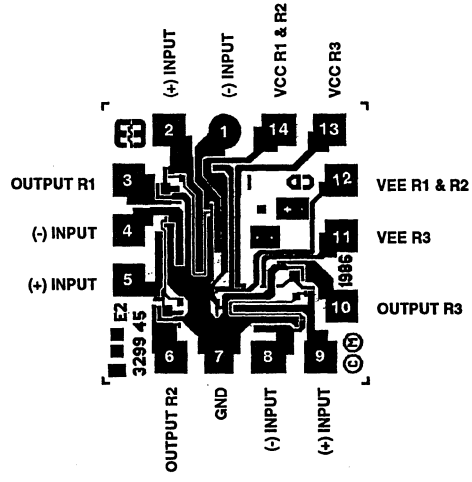
HS-246RH



HS-248RH



HS-249RH



DESIGN INFORMATION

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Voltage Mode Transmission

Data rates of up to 10 million bits per second can be obtained with standard TTL logic; however, the transmission distance must be very short. For example, a typical 50 foot low capacitance cable will have a capacitance of approximately 750pF which requires a current of greater than 50mA to drive 5V into this cable at 10MHz; therefore, voltage mode transmitters are undesirable for long transmission lines at high data rates due to the large current required to charge the transmission line capacitance.

Current Mode Transmission

An alternate method of driving high data rates down long transmission lines is to use a current mode transmitter. Current mode logic changes the current in a low impedance transmission line and requires very little change in voltage. For example, a 2mA change in transmitter current will produce a 100mV change in receiver voltage independent of the series transmission line resistance. The rise time at the receiver for a typical 50 foot cable (750pF) is approximately 30ns for a 2mA pulse.

An emitter coupled logic gate is frequently used for a current mode transmitter. However, ECL gates are not compatible with TTL and DTL logic and they require considerable power. The Harris Semiconductor HS-245RH is a TTL/DTL compatible current mode transmitter designed for high data rates on long transmission lines. Data rates of 15 megabits per second can be obtained with 50 feet of transmission line when using the companion HS-246RH or HS-249RH receiver. Data rates of 2 megabits per second are easily obtained on transmission lines as long as 1,000 feet. The Harris transmitter and receivers feature very low power, typically 25mW for the transmitter and 15mW for the receiver.

Harris Transmitter/Receivers

The Harris transmitter/receiver family consists of a triple line transmitter, two triple line receivers with internal terminations and a triple party-line receiver. The general characteristics of the transmitter and receivers are outlined in Table A.

TABLE A. GENERAL TRANSMITTER/RECEIVER CHARACTERISTICS

TRIPLE LINE TRANSMITTER			
PARAMETER	**HS-245RH**	**UNITS**	**COMMENTS**
Operating Temperature Range	-55°C to +125°C	°C	
"ON" Output Current	1.0 Min	mA	Over Full Temperature Range
Power Supply Current	7.0 Max	mA	Per Transmitter Section
Standby Current	33 Max	µA	Per Transmitter Section
Propagation Delay	14 Max	ns	Over Full Temperature Range

TRIPLE LINE RECEIVER				
PARAMETER	**RECEIVER TYPE**	**LIMITS**	**UNITS**	**COMMENTS**
Operating Temperature Range	HS-246RH/248RH/249RH	-55°C to +125°C	°C	
Power Supply ICC (VCC = +5.0V)	HS-246RH/248RH/249RH	2.6	mA	Per Receiver Section
Propagation Delay	All Receivers	30	ns	Over Full Temperature Range
Input Impedance and Output Circuit		**INPUT**		OUTPUT
	HS-246RH	100	Ω	Open Collector
	HS-248RH	Hi-Z		6K Pull-Up Resistor
	HS-249RH	100	Ω	6K Pull-Up Resistor

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Transmitter

The HS-245RH transmitters have two inputs per transmitter, either of which is low while the other is open during normal operation and both inputs are open during standby. For optimum transmitter performance, the "off" input should be open circuit rather than being pulled towards +5V, because this will reduce the "on" output data current. On the other hand, the "on" and "off" output data current will be increase if the "off" input is held below its open circuit voltage. Open collector gates such as the 7401 and 7403 or 7405 Hex-Inverter are suitable for driving the HS-245RH transmitter inputs. By using 2-input gates as shown in Figure 1, an enable line can be provided so that more than one transmitter may be connected to a line for time sharing. When the enable line is low the transmitter will be disabled and will present a high impedance to the transmission line as well as requiring very little power supply current.

Complementary input signals may be derived from high speed inverter gates as shown, or by using the complementary outputs of a flip-flop. When the transmitter is connected near the midpoint of a long transmission line or to a line with terminations at both ends, two transmitter sections should be paralleled with respective inputs and outputs connected together in order to drive the reduced impedance. This parallel transmitter technique can also be used to increase the data rate on long transmission lines.

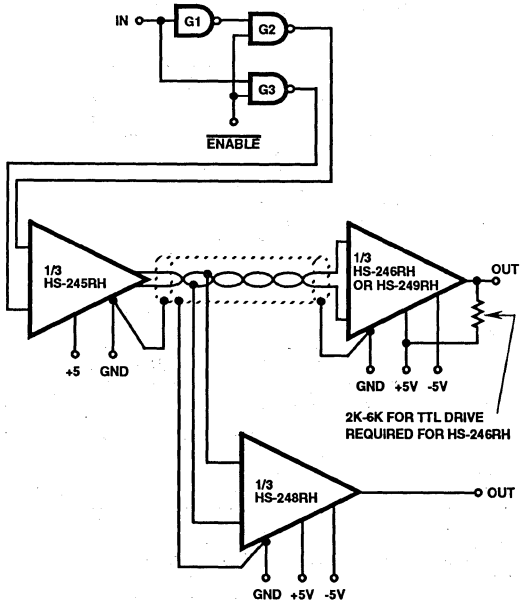


FIGURE 1. TYPICAL DATA TRANSMISSION SYSTEM

Transmitter Operation

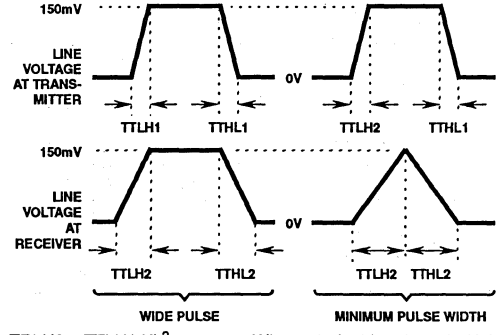
The transmitter alternately applies the current to each of the two conductors in the twisted pair line such that the total current in the twisted pair is constant and always in the same direction. This current flows through either of the two 50V terminating resistors at the receiver and returns to the transmitter as a steady DC current on the transmission line shield. The DC power supply return for the transmitter is through the receiver terminating resistors (the transmitter ground pin is only a substrate ground). Therefore, it is essential that the shield be connected to the power supply common at both the transmitter and receiver, preferably at the integrated circuit "ground" pin. More than fifteen twisted pair lines can share the same shield without crosstalk.

Receivers

The HS-248RH "party-line" receiver presents a high impedance load to the transmission line allowing as many as ten HS-248RH receivers to be distributed along a line without excessive loading. Figure 1 shows a typical system of a transmitter, a terminating receiver and a party-line receiver. The transmission line is terminated in its characteristics impedance by an HS-246RH, HS-249RH, or by a pair of 50V resistors connecting each line to the ground return shield.

Transmission Lines

The maximum frequency (or minimum pulse width) which can be carried by a certain length of a given transmission line is dependent on the loss characteristics of the particular line. At low frequencies, there will be virtually no loss in pulse amplitude, but there will be a degradation of rise and fall-time which is roughly proportional to the square of the line length. This is shown in Figure 2. If the pulse width is less than the rise-time at the receiver end, the pulse amplitude will be diminished, approaching the point where it cannot be detected by the receiver.



$TRLH2 = TTLH1\ KL^2$

$TTHL2 = TTHL1\ KL^2$

Where: L is Line Length K is determined by line loss characteristics

FIGURE 2. TRANSMISSION LINE WAVE-SHAPING

DESIGN INFORMATION (Continued)

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

The transmission line used with the Harris HS-245RH series transmitter and receivers can be any ordinary shielded, twisted pair line with a characteristic impedance of 100Ω. Twisted pair lines consisting of number 20 or 22 gauge wire will generally have this characteristic impedance. Special high quality transmission lines are not necessary and standard audio, shielded-twisted pair, cable is generally suitable.

Since the necessary characteristics for various twisted pair lines are not readily available, it may be necessary to take some measurements on a length of the proposed line. To do this, connect an HS-245RH transmitter to one end of the line (100 feet or more) and an HS-246RH or an HS-249RH receiver to the other end. The rise and fall-times can be measured on the line at both ends and the constant "K", for that line can be computed as shown in Figure 2 so that the minimum pulse width can be determined for any length of line.

Data rates of 2MHz have been obtained using 1,000 feet of standard shielded, twisted pair, audio cable. Data rates of 15MHz are possible on shorter lengths of transmission line (50 feet).

Electromagnetic Interference

Very little electromagnetic interference is generated by the Harris current mode system because the total current through the twisted pair is constant, while the current through the shield is also constant and in the opposite direction. This can be verified by observing, with a current probe, the total current through the twisted pair, through the shield and through the complete shielded, twisted pair cable. In each case a constant current will be observed with only small variations. Small pulses may be observed if the complementary inputs to the transmitter do not switch at the same time. The current will decrease during the time both inputs are high, and will increase during the time both inputs are low. These switching pulses may be observed when using the circuit shown in Figure 1. The amplitude and shape of these pulses will depend of the propagation delay of G1, and transition times G2 and G3. These pulses are generally of no concern because of their small amplitude and width, but they may be reduced by increasing the similarity of the waveforms and timing synchronization of the complementary signals applied to the transmitter.

In addition to generating very little noise, the system is also highly immune to outside noise since it is difficult to capacitively couple a differential signal into the low impedance twisted pair cable and it is even more difficult in induce a differential current into the line due to the very high impedance of the constant current transmitter. Therefore, differential mode interference is generally not a problem with the Harris current mode system. Large common mode voltages can also be tolerated because the output current of the transmitter is constant as long as the receiver termination ground is less than 2V positive with respect to the grounded input of the transmitter, and is less than 25V negative with respect to the transmitter VCC. The current mode system is totally unaffected by ground differential noise of +2V at frequencies as high as 1MHz.

Propagation Delay

The worst case propagation delay of a transmitter and receiver, connected as shown in Figure 1, can be determined by adding the maximum delay shown on the data sheet for the transmitter and receiver. These overall switching characteristics are shown in Table B. For the entire system, however, the propagation delay of the transmission line must also be considered. This delay, of course, depends on the length of the line and the characteristics of the line, but in general, delays of between 1.5ns and 3.0ns per foot can be expected.

TABLE B. OVERALL TRANSMITTER/RECEIVER SWITCHING CHARACTERISTICS

CHARACTERISTICS	-55°C to +125°C HS-245RH, HS-246RH HS-248RH, HS-249RH			UNITS
	MIN	TYP	MAX	
Progagation Delay TPLH	-	18	40	ns
Propagation Delay TPHL	-	18	40	ns
Duty Cycle Distortion TPLH - TPHL	-	2	15	ns

NOTE: VCC = +5V, VEE = -5V

HARRIS SEMICONDUCTOR

HS-15530RH

Radiation Hardened CMOS Manchester Encoder-Decoder

December 1992

Features

- Functional Total Dose 1 x 10^5 RAD(Si)
- Latch-Up Free to 5 x 10^{11} RAD(Si)/s
- Support of MIL-STD-1553
- Low Operating Power 50mW at 5V
- 1.0 Megabit/s Data Rate
- Sync Identification and Lock-In
- Clock Recovery
- Manchester II Encode, Decode
- Separate Encode and Decode
- Military Temperature Range -55°C to +125°C

Description

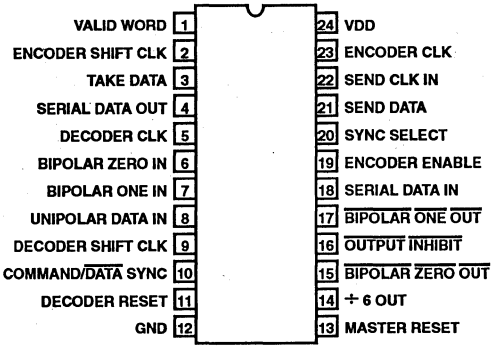
The Harris HS-15530 is a high performance, radiation resistant, CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocols. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate completely independent of each other, except for the Master Reset functions.

This circuit meets many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over temperature while residing in a radiation environment. It interfaces with CMOS, TTL or N channel support circuitry, and uses a standard 5V supply.

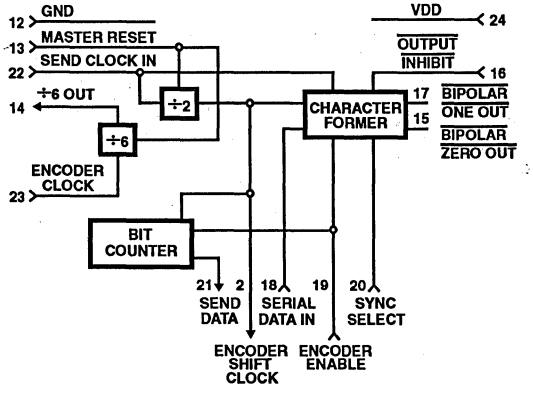
Pinout

24 PIN DIP
CASE OUTLINE D-3, CONFIGURATION 1
TOP VIEW

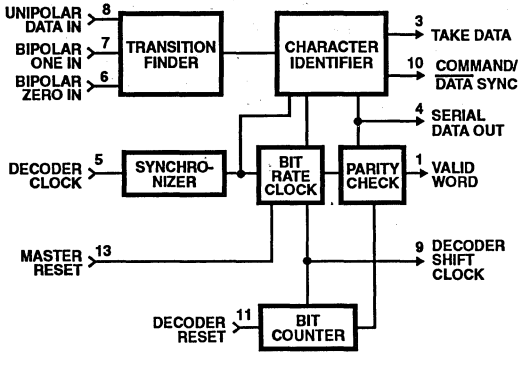


Block Diagrams

ENCODER



DECODER



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3203

Pin Description

NAME	PIN NO.	TYPE	SECTION	DESCRIPTION
VALID WORD	1	O	Decoder	Output high indicates receipt of a valid word, (valid parity and no Manchester errors).
ENCODER SHIFT CLOCK	2	O	Encoder	Output for shifting data into the Encoder. The Encoder samples SDI on the low-to-high transition of Encoder Shift Clock
TAKE DATA	3	O	Decoder	Output is high during receipt of data after identification of a sync pulse and two valid Manchester data bits
SERIAL DATA OUT	4	O	Decoder	Delivers received data in correct NRZ format
DECODER CLOCK	5	I	Decoder	Input drives the transition finder, and the synchronizer which in turn supplies the clock to balance of the decoder, input a frequency equal to 12X the data rate
BIPOLAR ZERO IN	6	I	Decoder	A high input should be applied when the bus is in its negative state. This pin must be held high when the Unipolar input is used.
BIPOLAR ONE IN	7	I	Decoder	A high input should be applied when the bus is in its positive state. The pin must be held low when the Unipolar input is used.
UNIPOLAR DATA IN	8	I	Decoder	With pin 6 high and pin low, this pin enters unipolar data into the transition finder circuit. If not used this input must be held low.
DECODER SHIFT CLOCK	9	O	Decoder	Output which delvers a frequency (DECODER CLOCK + 12), synchronized by the recovered serial data stream.
COMMAND SYNC	10	O	Decoder	Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character. A low output indicates a Data synchronizing character.
DECODER RESET	11	I	Decoder	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
GROUND	12	I	Both	Ground Supply pin.
MASTER RESET	13	I	Both	A high on this pin clears 2:1 counters in both Encoder and Decoder, and reset the +6 circuit.
+6 OUT	14	O	Encoder	Output from 6:1 divider which is driven by the ENCODER CLOCK
BIPOLAR ZERO OUT	15	O	Encoder	An active low output designed to drive the zero or negative sense of a bipolar line driver.
OUTPUT INHIBIT	16	I	Encoder	A low on this pin forces pin 15 and 17 high, the inactive states.
BIPOLAR ONE OUT	17	O	Encoder	An active low output designed to drive the one or positive sense of a bipolar line driver.
SERIAL DATA IN	18	I	Encoder	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK
ENCODER ENABLE	19	I	Encoder	A high on this pin initiates the encode cycle. (Subject to the preceeding cycle being complete).
SYNC SELECT	20	I	Encoder	Actuates a Command sync for an input high and Data sync for an input low.
SEND DATA	21	O	Encoder	An active high output which enables the external source of serial data.
SEND CLOCK IN	22	I	Encoder	Clock input at a frequency equal to the data rate X2, usually driven by +6 output
ENCODER CLOCK	23	I	Encoder	Input to the 6:1 divider, a frequency equal to the data rate X12 is usually input here.
VDD	24	I	Both	VDD is the +5V power supply pin. A 0.1µF decoupling capacitor from VDD (pin 24) to GROUND (pin 12) is recommended.

NOTE: I = Input and O = Output

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
I/O Voltage (applied for all grades) ..... VSS-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 10mA/MHz in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
CERDIP Package	48.9°C/W	9.9°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 0.715W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.75V to +5.25V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.2VDD
Input High Voltage ..... 0.7VDD to VDD
Clock Input Low Voltage (VILC) ..... 0V to 0.5V
Clock Input High Voltage (VIHC) ..... VDD-0.5V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output High Voltage	VOH	VDD = 4.75V; IO = -3mA, VIN = 0V or 4.75V	1, 2, 3	-55°C, +25°C, +125°C	2.4	-	V
Output Low Voltage	VOL	VDD = 4.75V, IO = +1.8mA, VIN = 0V or 4.75V	1, 2, 3	-55°C, +25°C, +125°C	-	0.4	V
Input Leakage Current	IIL or IIH	VDD = 5.25V, VIN = 0V or 5.25V	1, 2, 3	-55°C, +25°C, +125°C	-1.0	1.0	µA
Standby Power Supply Current	IDDSB	VDD = 5.25V, VIN = 5V, IO = 0mA	1, 2, 3	-55°C, +25°C, +125°C	-	2	mA
Functional Tests	FT	VDD = 4.75 and 5.25V, VIN = GND or VDD, f = 1MHz	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-
Noise Immunity Functional Test	FN	VDD = 5.25V, VIN = 1.95V or 3.68V and VDD = 4.75V, VIN = 0.95V or 3.32V	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

AC's tested at worst case VDD, AC's guaranteed over full operating specifications.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
ENCODER TIMING							
Encoder Clock Frequency	FEC	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	15	MHz
Send Clock Frequency	FESC	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	2.5	MHz
Data Rate	FED	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	1.25	MHz
Shift Clock Delay	TE1	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	125	ns
Sync Pulse Width	TE7	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	150	-	ns
Bipolar Output Delay	TE9	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	125	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

AC's tested at worst case VDD, AC's guaranteed over full operating specifications.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
DECODER TIMING							
Decoder Clock Frequency	FDC	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	15	MHz
Data Rate	FDD	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	1.25	MHz
Decoder Reset Setup Time	TDRS	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	75	-	ns
Sync Delay "ON"	TD6	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	110	ns
Take Data Delay "ON"	TD7	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	110	ns
Sync Delay "OFF"	TD9	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	110	ns
Take Data Delay "OFF"	TD10	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	110	ns
Valid Word Delay	TD11	VDD = 4.75 and 5.25, CL = 50pF	7, 8, 9	-55°C, +25°C, +125°C	-	110	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz (Note 1)	T_A = +25°C	-	5	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz (Note 1)	T_A = +25°C	-	8	pF
Operating Supply Current	IDDOP	VDD = 5.25V, VIN = VDD or GND, f = 1MHz, IO = 0mA	-55°C < T_A < +125°C	-	10	mA
ENCODER TIMING REQUIREMENTS						
Encoder Clock Rise Time	TECR	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	-	8	ns
Encoder Clock Fall Time	TECF	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	-	8	ns
Master Reset Pulse Width	TMR	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	150	-	ns
Serial Data Setup	TE2	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	75	-	ns
Serial Data Hold	TE3	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	75	-	ns
Enable Setup	TE4	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	90	-	ns
Enable Pulse Width	TE5	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	100	-	ns
Sync Setup	TE6	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	55	-	ns
Send Data Delay	TE8	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	0	50	ns
DECODER TIMING REQUIREMENTS						
Decoder Clock Rise Time	TDCR	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	-	8	ns
Decoder Clock Fall Time	TDCF	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	-	8	ns
Decoder Reset Pulse Width	TDR	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	150	-	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Master Reset Pulse Width	TDMR	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	150	-	ns
Bipolar Data Pulse Width (Note 2)	TD1	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	TDC+10	-	ns
Sync Transition Span (Notes 2, 3)	TD2	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	18TDC	-	ns
One Zero Overlap (Note 2)	TD3	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	-	TDC-10	ns
Short Data Transition Span (Notes 2, 3)	TD4	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	6TDC	-	ns
Long Data Transition Span (Note 2, 3)	TD5	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	12TDC	-	ns
Serial Data Out Delay	TD8	VDD = 4.5V and 5.25V	-55°C < T_A < +125°C	-	80	ns

NOTES:

1. All measurements referenced to device ground.
2. TDC = Decoder Clock Period = 1/FDC
3. These parameters are given for information only and are typical values.
4. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

IDDSB at VDD = 5.0V will be measured and recorded for each device within one hour (±15 minutes) after irradiation. The lot will be accepted only if the average of these IDDSB measurements is less than or equal to 5mA.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C) GROUP B, SUBGROUP 5

Table 5 Intentionally left blank.

TABLE 6. APPLICABLE SUBGROUPS

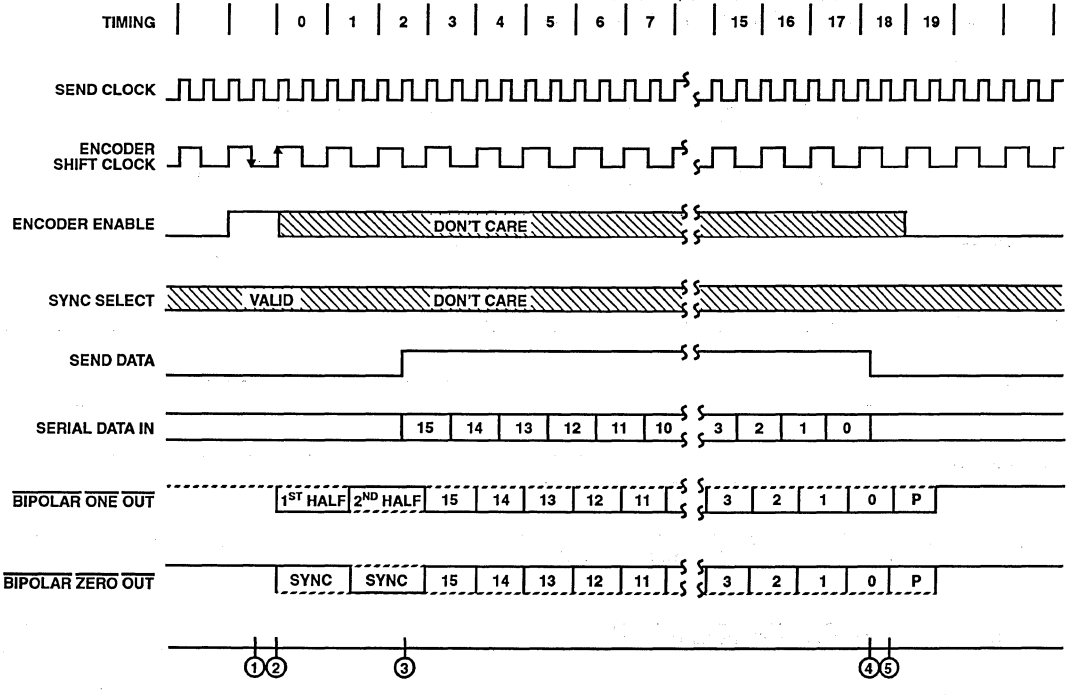
CONFORMANCE GROUPS	METHOD	-8 SUBGROUPS
Initial Test	100%/5004	1, 7, 9
PDA	100%/5004	1, 7
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group C	Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group D Others	Samples/5004	1, 7
Group E Subgroup 2	Samples/5004	1, 7, 9

Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the DECODER CLOCK.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK (1). This cycle lasts for one word length or twenty ENCODER SHIFT CLOCK periods. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high SYNC SELECT input actuates a command sync or a low will produce a data sync for the word (2). When the Encoder is ready to accept data, the SEND DATA output will go high and remain high for sixteen ENCODER SHIFT CLOCK periods (3). During these sixteen periods the data should be clocked into the SERIAL DATA input with every high-to-low transition of the ENCODER SHIFT CLOCK so it can be sampled on the low-to-high transition (3) - (4). After the sync and Manchester II coded data are transmitted through the $\overline{\text{BIPOLAR ONE}}$ and $\overline{\text{BIPOLAR ZERO}}$ outputs, the ENCODER adds on an addtional bit which is the parity for that word (5). If ENCODER ENABLE is held high continuously, consecutive words will be encoded without an interframe gap. ENCODER ENABLE must go low by time (5) as shown to prevent a consecutive word from being encoded. At any time a low on $\overline{\text{OUTPUT INHIBIT}}$ input will force both bipolar outputs to a high state but will not affect the ENCODER in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Anytime after or during this pulse, a low-to-high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.



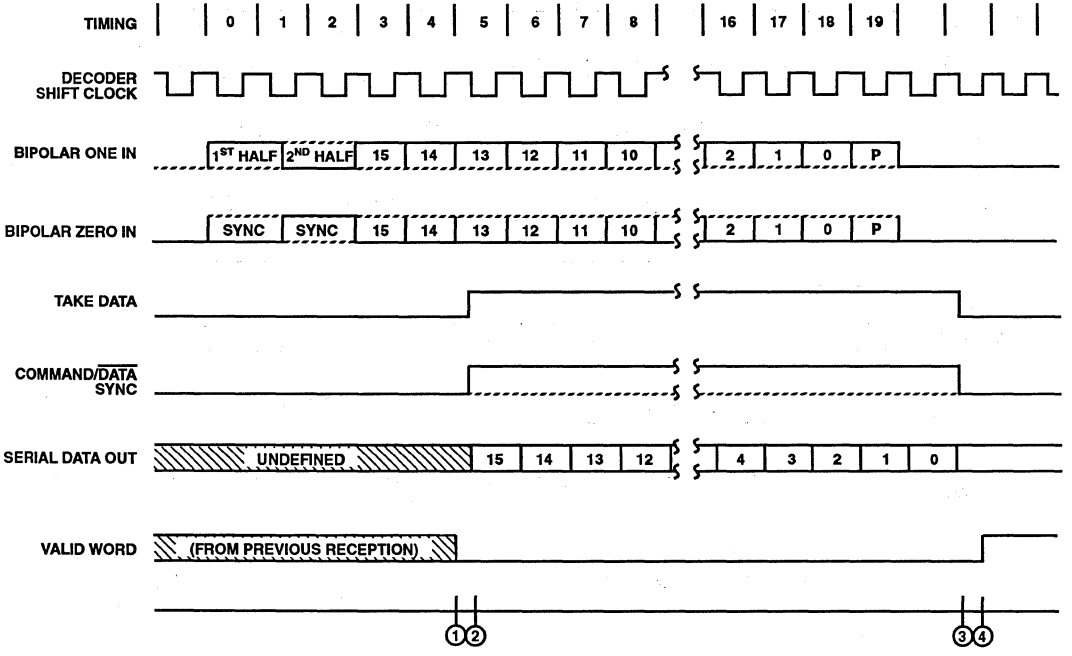
Decoder Operation

The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept non-inverted Manchester II coded data. (e.g. from $\overline{\text{BIPOLAR ONE OUT}}$ of an Encoder through an inverter to Unipolar Data Input).

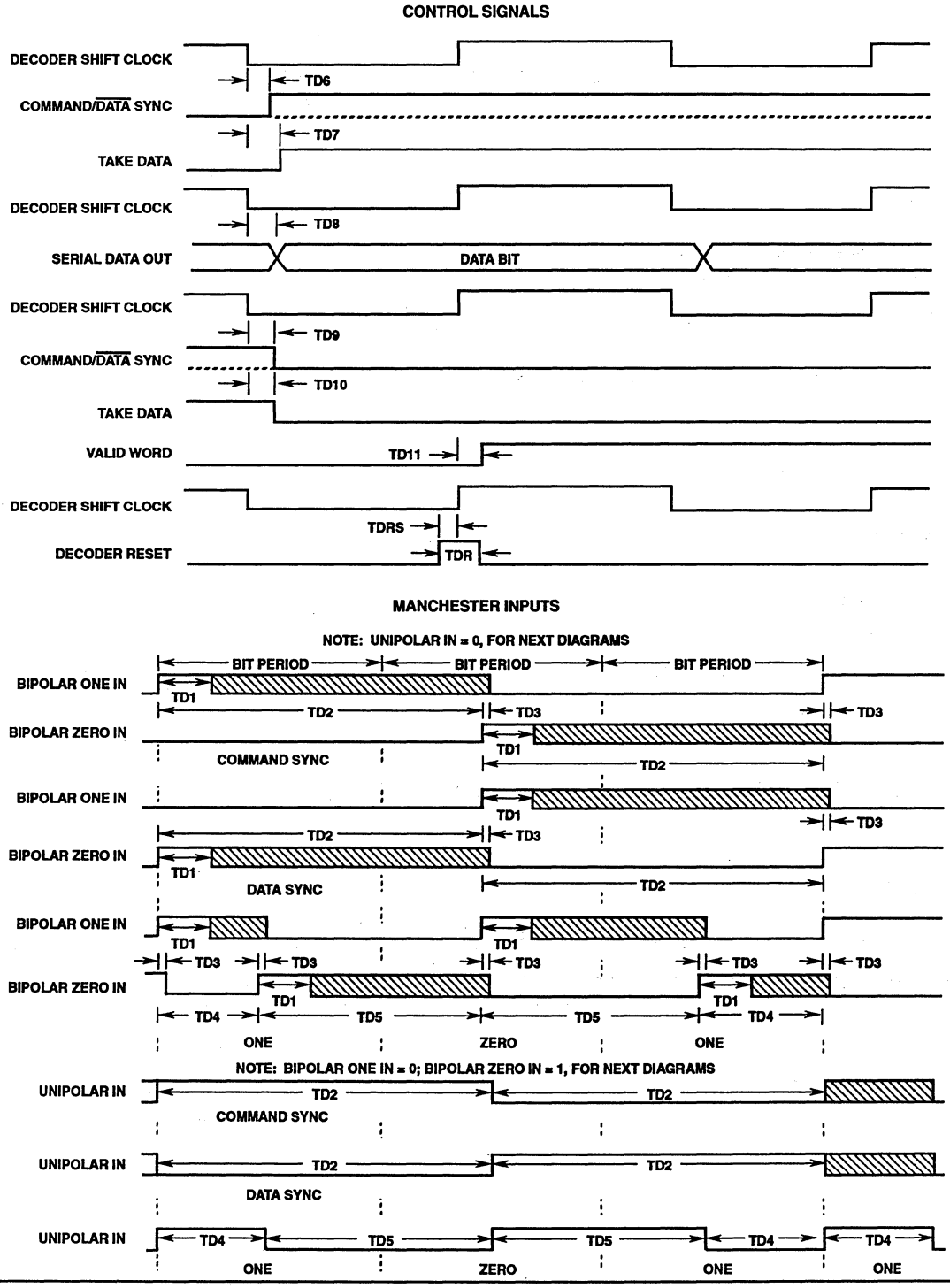
The Decoder is free running and countinuously monitors its data input lines for a valid sync character and two valid sync is recognized (1), the type of sync is indicated on COMMAND/$\overline{\text{DATA}}$ SYNC output. If the sync character was a command sync, this output will go high (2) and remain high for sixteen DECODER SHIFT CLOCK periods (3), otherwise it will remain low. The TAKE DATA output will go high and remain high (2) - (3). While the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can be shifted into an external register on every low-to-high transition of this clock (2) - (3). Note that DECODER SHIFT CLOCK may adjust its phase up until the time that TAKE DATA goes high.

After all sixteen decoded bits have been transmitted (3) the data is checked for odd parity. A high on VALID WORD output (4) indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence VALID WORD will go low approximately 20 DECODER SHIFT CLOCK periods after it goes high if not reset low sooner by a valid sync and two valid Manchester bits as shown (1).

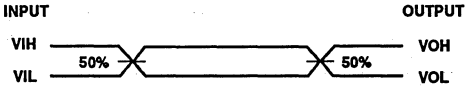
At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.



Decoder Timing

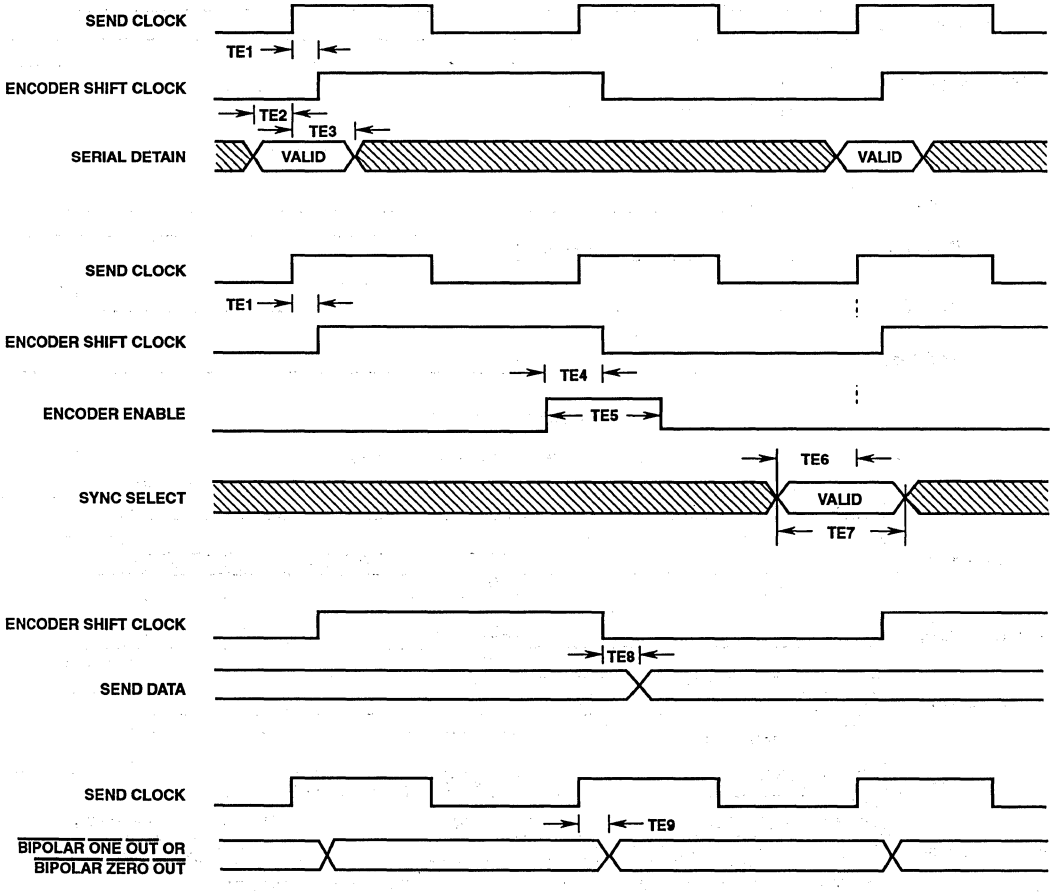


AC Testing Input, Output Waveform



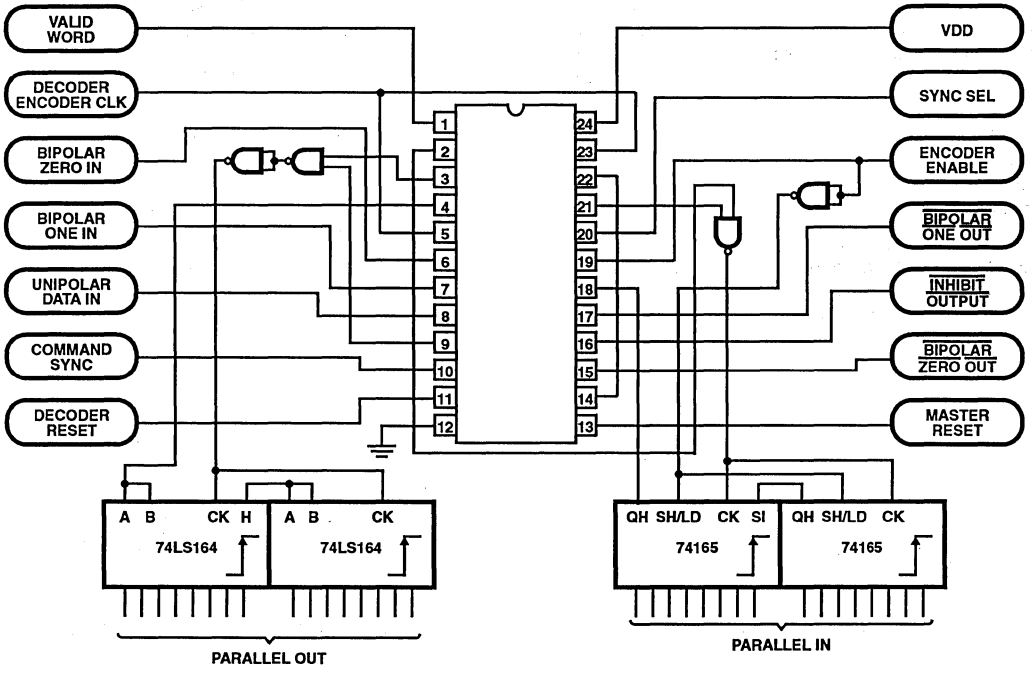
NOTE: AC Testing: All input signals must switch between VIL and VIH. Input rise and fall times are driven at 1ns/V.

Encoder Timing

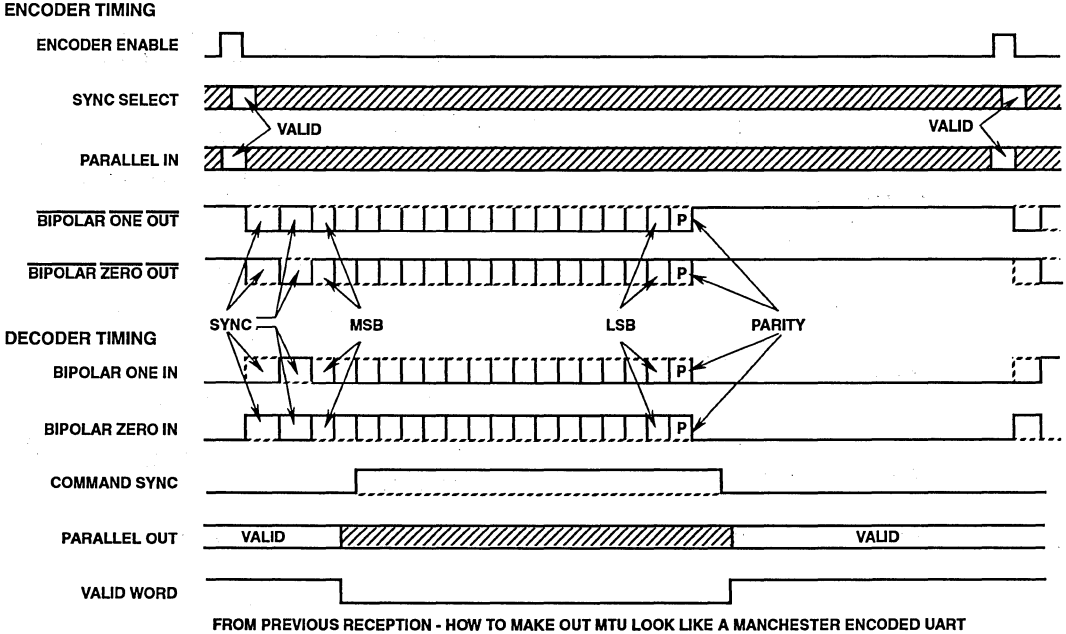


Applications

HOW TO MAKE OUR MTU LOOK LIKE A MANCHESTER ENCODED UART



TYPICAL TIMING DIAGRAM FOR A MANCHESTER ENCODED UART



FROM PREVIOUS RECEPTION - HOW TO MAKE OUT MTU LOOK LIKE A MANCHESTER ENCODED UART

MIL-STD-1553

The 1553 standard defines a time division multiplexed data bus for application within aircraft. The bus is defined to be bipolar, and encoded in a Manchester II format, so no DC component appears on the bus. This allows transformer coupling and excellent isolation among systems and their environment.

The HS-15530RH supports the full bipolar configuration, assuming a bus driver configuration similar to that in Figure 1. Bipolar inputs from the bus, like Figure 2, are also accommodated.

The signaling format in MIL-STD-1553 is specified on the assumption that the network of 32 or fewer terminals are controlled by a central control unit by means of Command Words. Terminals respond with Status Words. Each word is preceded by a synchronizing pulse, and followed by parity bit, occupying a total of 20ms. The word formats are shown in Figure 4. The special abbreviations are as follows:

- P — Parity, which is defined to be odd, taken across all 17 bits.
- R/T — Receive on logical zero, transmit on ONE.
- ME — Message Error if logical 1.
- TF — Terminal Flag, if set, calls for controller to request self-test data.

The paragraphs above are intended only to suggest the content of MIL-STD-1553, and do not completely describe its bus requirements, timing or protocols.

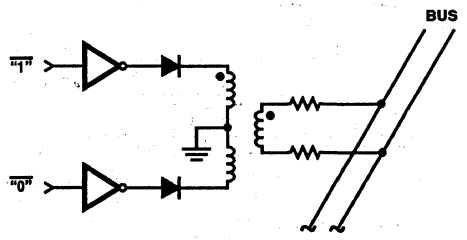


FIGURE 1. SIMPLIFIED MIL-STD-1553 DRIVER

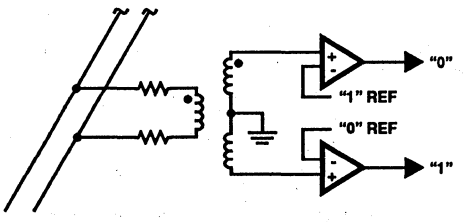


FIGURE 2. SIMPLIFIED MIL-STD-1553 RECEIVER

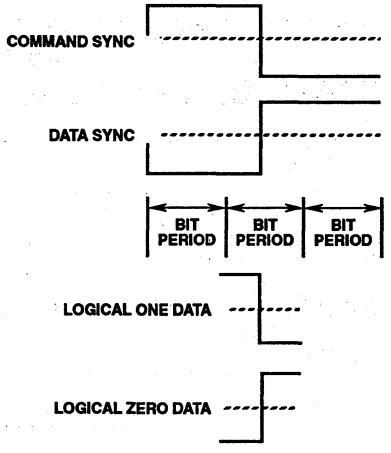


FIGURE 3. MIL-STD-1553 CHARACTER FORMATS

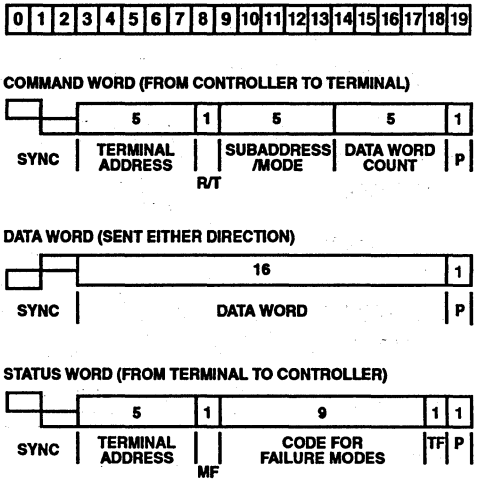
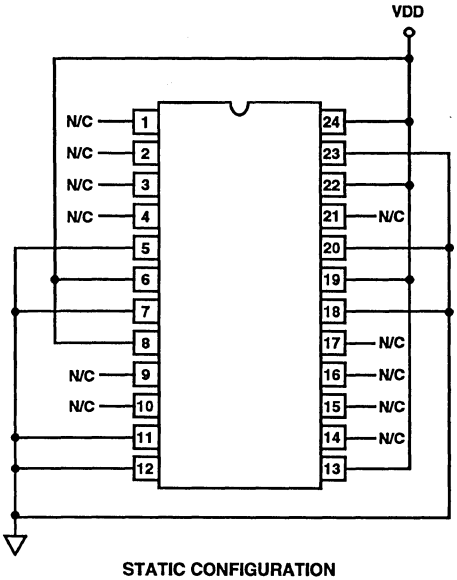


FIGURE 4. MIL-STD-1553 WORD FORMATS

NOTE: This page is a summary of MIL-STD-1553 and is not intended to describe the operation of the HS-15530RH.

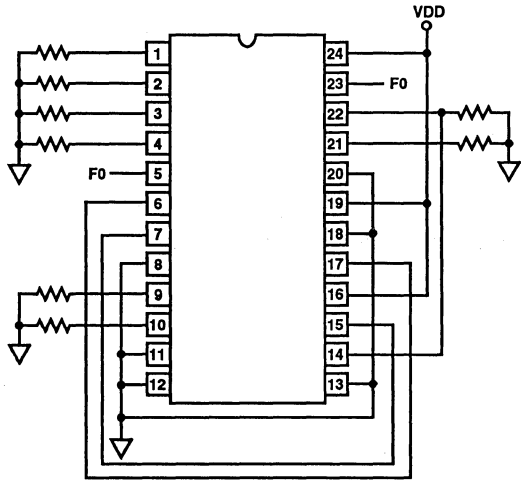
Burn-In Circuits



STATIC CONFIGURATION

NOTES:

VDD = 5.0V
IDD < 2mA
T_A min = +125°C

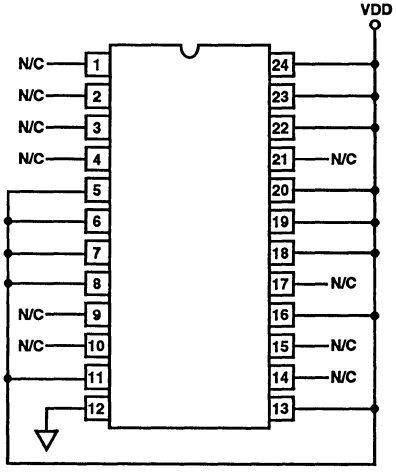


DYNAMIC CONFIGURATION

NOTES:

VDD = 5.0V
IDD < 10mA
T_A min = +125°C
All resistors 1.8kΩ 1/4 watt
F0 = 200KHz Square Wave, 50% Duty cycle
VIL = 0.5V
VIH = 4.5V

Irradiation Circuit



NOTES:

VDD = 5.0V
Group E Sample Size is 2 die/wafer from 20% of yielding wafers

Harris - '-8' Flow

Internal Visual Inspection	+25°C Electrical Tests +125°C, -55°C
Gamma Radiation Assurance Tests Method 1019	Group A Inspection Method 5005. 5% PDA (Note 3)
Customer Pre-Cap Visual Inspection (Note 1)	Brand
Temperature Cycling Method 1010 Condition C	Customer Source Inspection (Note 1)
Fine and Gross Leak Tests Method 1014	Group C Inspection Method 5005 (Note 1, 2)
Constant Acceleration Method 2001 Y1 30KG	Group D Inspection Method 5005 (Note 1, 2)
Initial Electrical Tests	External Visual Inspection Method 2009
Dynamic Burn-In 160 Hours, +125°C Method 1015 Condition D	Data Package Generation (Note 4)

NOTES:

1. These steps are optional, and must be negotiated as part of order.
2. Group B and D data package contains Attributes Data plus Variables Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable
4. '-8' Data Pack Contains:
   Assembly Attributes (post seal)
   Test Attributes (including Group A)
   Radiation Testing Certificate of Conformance
   Certificate of Conformance (as found on shipper).

Metallization Topology

DIE DIMENSIONS:
3934 x 4953µm x 485µm ±25µm

METALLIZATION:
Type: Silicon-Aluminum
Thickness: 11kÅ ± 1kÅ

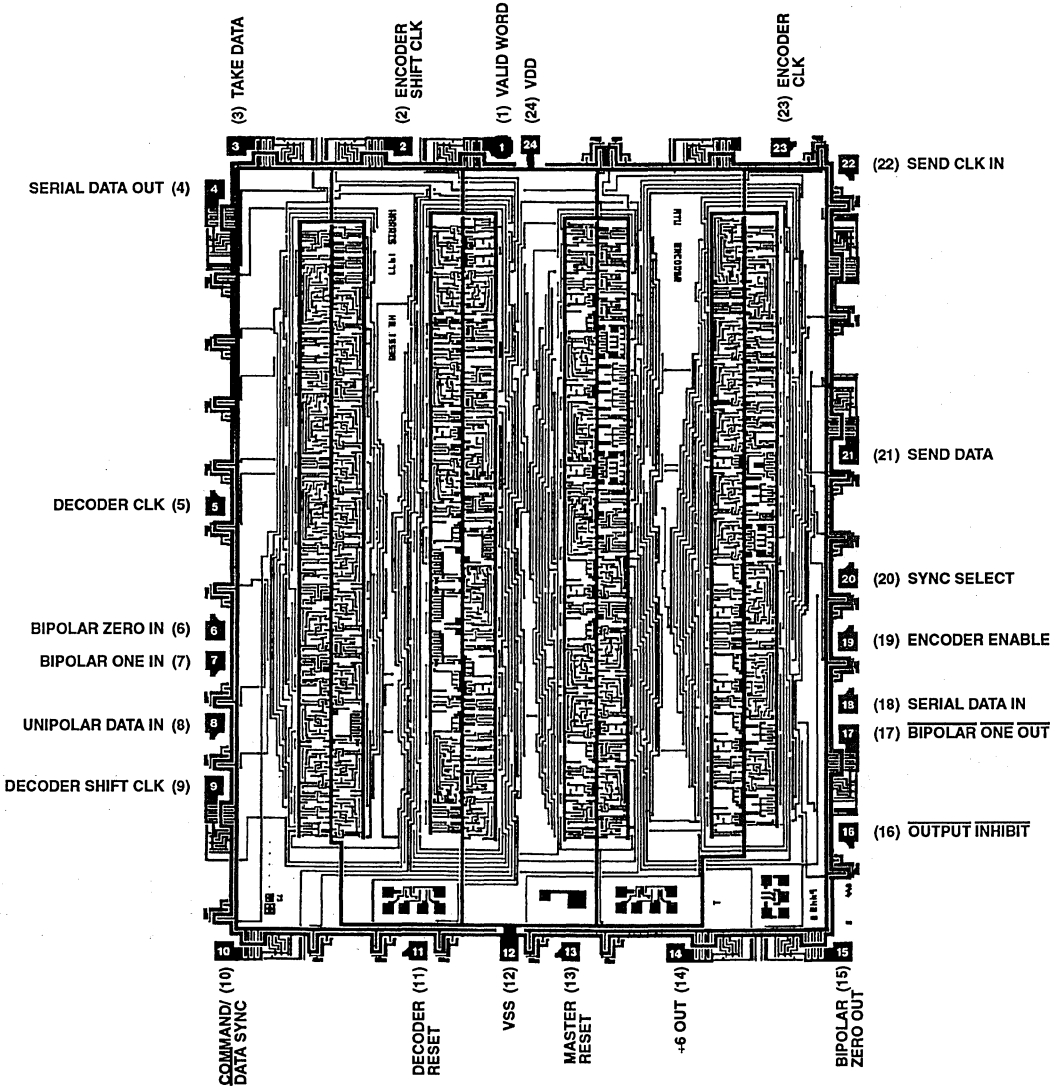
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy

WORST CASE CURRENT DENSITY:
$1.8 \times 10^5 A/cm^2$

Metallization Mask Layout

HS-15530RH



HARRIS SEMICONDUCTOR

HS-26C31MS

Radiation Hardened Quad Differential Line Driver

December 1992

Features

- 1.2 Micron Radiation Hardened CMOS
  - Total Dose Up to 300K RAD(Si)
  - Dose Rate Upset > $1x10^9$ RAD/Sec (20nS Pulse)
- Latchup Free
- EIA RS-422 Compatible Outputs (Except for IOS)
- TTL Compatible Inputs
- High Impedance Outputs when Disabled or Powered Down
- Low Power Dissipation 2.75mW Standby (Max)
- Single 5V Supply
- Low Output Impedance 10Ω or Less
- Full -55°C to +125°C Military Temperature Range

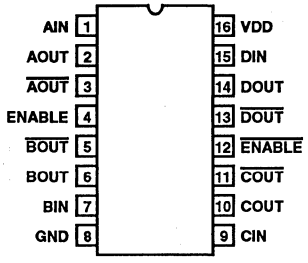
Description

The Harris HS-26C31MS is a quad differential line driver designed for digital data transmission over balanced lines and meets the requirements of EIA standard RS-422. Radiation hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

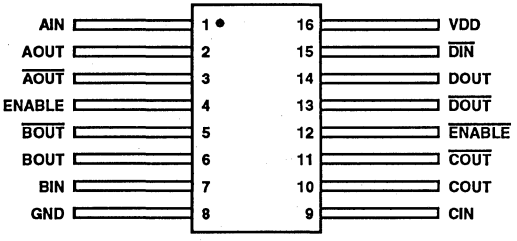
The HS-26C31MS accepts CMOS and converts them to RS-422 compatible outputs. This circuit uses special outputs that enable the drivers to power down without loading down the bus. Enable and disable pins allow several devices to be connected to the same data source and addressed independantly.

Pinouts

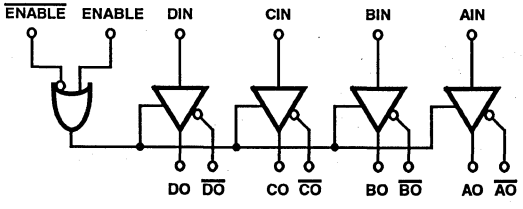
HS1-26C31MSR 16 PIN CERAMIC DUAL-IN-LINE
CASE OUTLINE D2, CONFIGURATION 3
TOP VIEW



HS9-26C31MSR 16 PIN FLATPACK
CASE OUTLINE F5A, CONFIGURATION 2
TOP VIEW



Logic Diagram



TRUTH TABLE

DEVICE POWER ON/OFF	INPUTS			OUTPUT	
	ENABLE	$\overline{ENABLE}$	IN	OUT	$\overline{OUT}$
ON	0	1	X	HI-Z	HI-Z
ON	1	X	0	0	1
ON	X	0	0	0	1
ON	1	X	1	1	0
ON	X	0	1	1	0
OFF	X	X	X	HI-Z	HI-Z

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3401**

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input, Output or I/O Voltage ..... -0.5 to VDD+0.5V
DC Diode Input Current (Any Input) ..... ±20mA
DC Drain Current (Any One Input) 350mA
DC VDD or Ground Current 400mA
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
DIC Package	75°C/W	16°C/W
Flatpack Package	64°C/W	12°C/W

Maximum Package Power Dissipation at +125°C
For T = -55°C to +100°C 1W
For T = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Rise and Fall Time ..... 500ns Max
Input Low Voltage (VIL) ..... 0V to 0.3VDD Max
Input High Voltage (VIH) ..... VDD to 0.7VDD Min

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH	VDD = 4.5V, and 5.5V IO = -20mA (Notes 2, 6)	1, 2, 3	-55°C, +25°C, +125°C	2.5	-	V
Low Level Output Voltage	VOL	VDD = VIH = 4.5V, IO = 20mA , VIL = 0V (Note 2)	1, 2, 3	-55°C, +25°C, +125°C	-	0.5	V
Differential Output Voltage	VT	VDD = VIH = 4.5V, RL = 100Ω , VIL = 0V (Note 3)	1, 2, 3	-55°C, +25°C, +125°C	2.0	-	V
Difference in Differential Output	IVTI - IVTI	VDD = VIH = 4.5V, RL = 100Ω , VIL = 0V (Note 3)	1, 2, 3	-55°C, +25°C, +125°C	-	0.4	V
Common Mode Output Voltage	VOS	VDD = VIH = 4.5V, RL = 100Ω , VIL = 0V (Note 3)	1, 2, 3	-55°C, +25°C, +125°C	-	3.0	V
Difference in Common Mode Output	IVOS - VOSI	VDD = VIH = 4.5V, RL = 100Ω , VIL = 0V (Note 3)	1, 2, 3	-55°C, +25°C, +125°C	-	0.4	V
High Level Input Voltage	VIH	VDD = 4.5V, 5.5V (Note 5)	1, 2, 3	-55°C, +25°C, +125°C	0.7 VDD	-	V
Low Level Input Voltage	VIL	VDD = 4.5V, 5.5V (Note 5)	1, 2, 3	-55°C, +25°C, +125°C	-	0.3 VDD	V
Standby Supply Current	IDDSB	VDD = 5.5V, Output = 0, VIN = VDD or GND	1, 2, 3	-55°C, +25°C, +125°C	-	500	µA
Tristate Output Leakage Current	IOZ	VDD = 5.5V, Force Voltage = 0V or VCC	1, 2, 3	-55°C, +25°C, +125°C	-	±5	µA
Input Leakage	IIN	VDD = 5.5V, VIN = VDD or GND	1, 2, 3	-55°C, +25°C, +125°C	-	±1.0	µA
Output Leakage Current Power OFF	IOFF	VDD = 0V, VOUT = 6V, 0V	1, 2, 3	-55°C, +25°C, +125°C	-100	100	µA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Clamp Voltage	VIC	At -1.0mA	1, 2, 3	-55°C, +25°C, +125°C	-	-1.5	V
		At +1.0mA	1, 2, 3	-55°C, +25°C, +125°C	-	+1.5	V

NOTES:

1. All voltages referenced to device ground.
2. Force/Measure functions may be interchanged.
3. These test conditions are detailed in EIA specification RS-422.
4. Only one input pin set up to VIN per test. All other pins set to VCC or GND.
5. This parameter tested as inputs levels in VOL/VOH, IOZ, functional test.
6. VIL = 0.3VDD, VIH = 0.7VDD.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPLH, TPHL	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	2	18	ns
Propagation Delay	TPZH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	5	28	ns
Propagation Delay	TPZL	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	5	28	ns
Propagation Delay	TPHZ	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	2	18	ns
Propagation Delay	TPLZ	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	2	18	ns
Rise and Fall Times	TTHL, TTLH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	1	10	ns
Output Skew	TSKEW	VDD = 4.5V, RL = 100Ω, CL = 40pF	9, 10, 11	-55°C, +25°C, +125°C	-	3	ns

NOTES:

1. All voltages referenced to device ground.
2. See Table EIA RS-422

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz	1	-55°C, +25°C, +125°C	-	12	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz	1	-55°C, +25°C, +125°C	-	12	pF

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Operating Short Circuit	IOS	VDD = 5.5V, VIN = VDD or GND, VOUT = 0V	2	-55°C, +25°C, +125°C	-30	-150	mA
On-State Resistance	RON	VDD = 4.5V, VOUT = 1.5V, VIN = VDD or GND	1	-55°C, +25°C, +125°C	-	10	Ω

NOTES:

1. Parameters listed in table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major design or process changes that affect these parameters.
2. Only one output at a time may be shorted.
3. Power Up/Down Feature: Outputs will remain in the Hi-Z state with VDD ≤ 2.5V and become active at VDD ≥ 4.0V. The active output state will be determined by the input conditions.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

The post irradiation electrical performance characteristics are the same as the parameters listed in tables 1, 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C) AND GROUP B, SUBGROUP 5 DELTA PARAMETERS

PARAMETER	SYMBOL	DELTA LIMITS
Standby Supply Current	IDDSB	±100µA
Tri-State Output Leakage Current	IOZ	±1.0µA
Low Level Output Voltage	VOL	±60mV
High Level Output Voltage	VOH	±150mV
Input Leakage Current	IIL, IIH	±150nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100%/5004	1, 7, 9	See Table 5
Interim Test I (Post Burn-In)		100%/5004	1, 7, 9	See Table 5
Interim Test II (Post Burn-In)		100%/5004	1, 7, 9	See Table 5
PDA		100%/5004	1, 7, 9, Δ	-
Interim Test III (Post-Burn-In)		100%/5004	1, 7, 9	See Table 5
PDA		100%/5004	1, 7, 9, Δ	-
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	-
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	-
Group B	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Δ	Subgroups 1, 2, 3, 9, 10, 11
	B6	Samples/5005	1, 7, 9	-
Group D		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	-

TABLE 7. TOTAL DOSE IRRADIATION

CONFOMRANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE-RAD	POST-RAD	PRE-RAD	POST-RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 7, 9	Table 4

TABLE 8. BURN-IN TEST CONNECTIONS (+125°C < T_A < 139°C, VCC = 6V, ±0.5V)

TEST	OPEN	GROUND	VDD	1/2VDD	50KHz	25KHz
Static Burn-In I	2, 3, 5, 6, 10, 11, 13, 14	1, 4, 7, 8, 9, 12, 15	16	-	-	-
Static Burn-In II	2, 3, 5, 6, 10, 11, 13, 14	8	1, 4, 7, 9, 12, 15, 16	-	-	-
Dynamic Burn-In	-	8, 12	4, 16	2, 3, 5, 6, 10, 11, 13, 14	1, 7, 9, 15	-

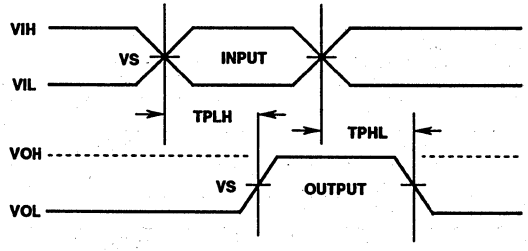
NOTE: Each pin except for VDD and Ground will have a series resistor.

TABLE 9. IRRADIATION TEST CONNECTIONS (T_A = +25°C, ±5°C, VDD = 5V, ±10%)

TEST	OPEN	GROUND	VDD	1/2VDD	50KHz	25KHz
Radiation Exposure	2, 3, 5, 6, 10, 11, 13, 14	8	1, 4, 7, 9, 12, 15, 16	-	-	-

NOTE: Each pin except for VDD and Ground will have a series resistor.

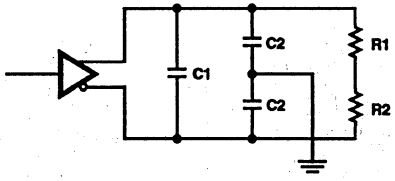
Propagation Delay Timing Diagram



AC VOLTAGE LEVELS

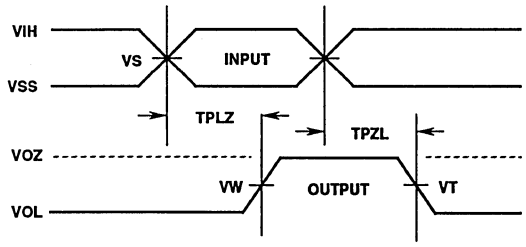
PARAMETER	HS-26C31MSR	UNITS
VDD	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V
VT	2.25	V

Propagation Delay Load Circuit



C1 = C2 = C3 = 40pF
R1 = R2 = 50Ω

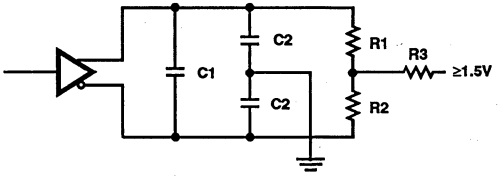
Tri-State Low Timing Diagrams



TRI-STATE LOW VOLTAGE LEVELS

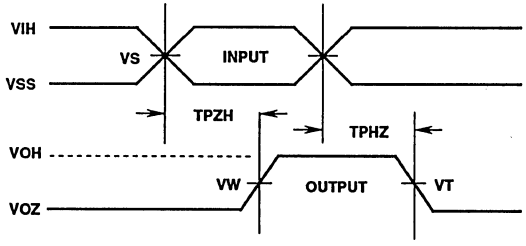
PARAMETER	HS-26C31MSR	UNITS
VDD	4.50	V
VIH	3.00	V
VS	1.30	V
VW	VOL + 0.3	V
VT	0.80	V

Tri-State Low Load Circuit



C1 = C2 = C3 = 40pF
R1 = R2 = 50Ω
R3 = 500Ω

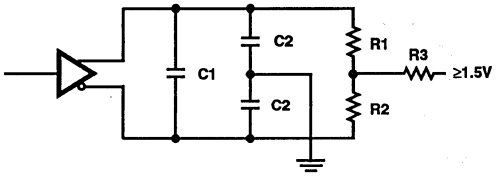
Tri-State High Timing Diagrams



TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	HS-26C31MSR	UNITS
VDD	4.50	V
VIH	3.00	V
VS	1.30	V
VT	VOH - 0.3	V
VW	2.00	V

Tri-State High Load Circuit



C1 = C2 = C3 = 40pF
R1 = R2 = 50Ω
R3 = 500Ω

Harris - Space Level Product Flow

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

Radiation Verification (Each Wafer) Method 1019, 300k RAD (Si), 4 Samples/Wafer, 0 Rejects

100% Nondestructive Bond Pull Method 2023

100% Internal Visual Inspection Method 2010

100% Temperature Cycling Method 1010 Condition C

100% Constant Acceleration

100% Particle Impact Noise Detection Testing

100% External Visual Inspection

100% Serialization

100% Initial Electrical Test

100% Static Burn-In1: 24 Hour, +125°C Min, Method 1015

100% Interim Electrical Test 1 (Note 1)

100% Static Burn-In 2: 24 Hour, +125°C Min, Method 1015

100% Interim Electrical Test 2 (Note 1)

100% Dynamic Burn-In 240 Hour, +125°C or Equivalent, Method 1015

100% Interim Electrical 3 (Note 1)

100% Final Electrical Test

100% Fine and Gross Seal Method 1014

100% Radiographics Method 2012 (2 Views)

100% External Visual Method 2009

Group A (All Tests) Method 5005 (Class S)

Group B (Optional) Method 5005 (Class S) (Note 2)

Group D (Optional) Method 5005 (Class S) (Note 2)

CSI and/or GSI (Optional Note 2)

Data Package Generation (Note 3)

NOTES:

1. Failure from interim electrical tests 1 and 2 are combined for determining PDA (PDA = 5% for subgroups 1, 7, 9 and delta failures combined, PDA = 3% for subgroup 7 failures). Interim electrical tests 3 PDA (PDA = 5% for subgroups 1, 7, 9 and delta failures combined, PDA = 3% for subgroup 7 failures).
2. These steps are optional, and should be listed on the purchase order if required.
3. Data Package Contents:
   Cover Sheet (P.O. Number, Customer Number, Lot Date Code, Harris Number, Lot Number, Quantity).
   Certificate of Conformance (as found on shipper).
   Lot Serial Number Sheet (Good Unit(s) Serial Number and Lot Number).
   Variables Data (All Read, Record, and delta operations).
   Group A Attributes Data Summary.
   Wafer Lot Acceptance Report (Method 5007) to include SEM photos. NOTE: SEM photos to include % of step coverage.
   X-Ray Report and File(s), including parameter measurements.
   GAMMA Radiation Report with initial shipment of devices from the same wafer lot; containing a Cover Page, Disposition, Rad Dose, Lot Number, Test Package, Spec Number(s), Test Equipment, etc. Irradiation Read and Record data will be on file at Harris.

Metallization Topology

DIE DIMENSIONS:
87 mils x 188 mils
(2219 x 4770)

METALLIZATION:
M1: Mo/Tiw
Thickness: 5800Å

M2: Al/Si/Cu
Thickness: 10kÅ ±1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 10kÅ ± 1kÅ

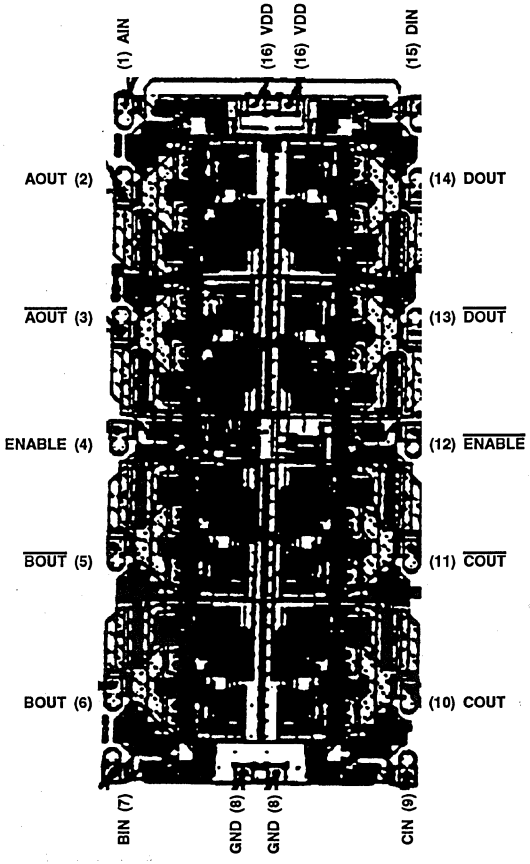
DIE ATTACH:
Silver Glass

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE: 110µm x 100µm

Metallization Mask Layout

HS-26C31MS



HARRIS SEMICONDUCTOR

HS-26C32MS

Radiation Hardened Quad Differential Line Receiver

December 1992

Features

- 1.2 Micron Radiation Hardened CMOS
  - Total DoseUp to 300K RAD(Si)
  - Dose Rate Upset > $1x10^9$ RADs (Si)/s (20nS Pulse)
- Latchup Free
- EIA RS-422 Compatible Outputs
- TTL/CMOS Compatible Inputs
- Input Fail Safe Circuitry
- High Impedance Inputs when Disabled or Powered Down
- Low Power Dissipation 138mW Standby (Max)
- Single 5V Supply
- Full -55°C to +125°C Military Temperature Range

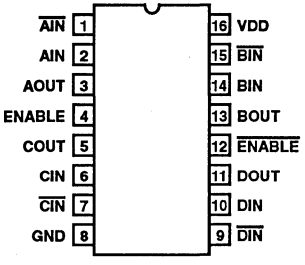
Description

The Harris HS-26C32MSR is a differential line receiver designed for digital data transmission over balanced lines and meets the requirements of EIA standard RS-422. Radiation hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

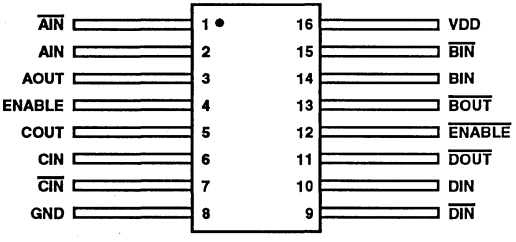
The HS-26C32MSR has an input sensitivity of 200mV over the common mode input voltage range of ±7V. The receivers are also equipped with input fail safe circuitry, which causes the outputs to go to a logic "1" when the inputs are open. Enable and Disable functions are common to all four receivers.

Pinouts

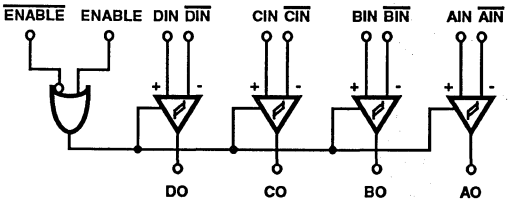
HS1-26C32MSR 16 PIN CERAMIC DUAL-IN-LINE
CASE OUTLINE D2, CONFIGURATION 3
TOP VIEW



HS9-26C32MSR 16 PIN FLATPACK
CASE OUTLINE F5A, CONFIGURATION 2
TOP VIEW



Logic Diagram



TRUTH TABLE

DEVICE POWER ON/OFF	INPUTS			OUTPUT
	ENABLE	$\overline{ENABLE}$	INPUT	OUT
ON	0	1	X	HI-Z
ON	1	X	VID > VTH	1
ON	1	X	VID > VTH	0
ON	X	0	VID > VTH	1
ON	X	0	VID > VTH	0
ON	1	X	Open	1
ON	X	0	Open	1
OFF	X	X	X	HI-Z

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3402**

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Differential Input Voltage ..... ±12V
Common Mode Range ..... ±12V
Enable Pins Input Voltage ..... -0.5V to VDD+0.5V
DC Drain Current (Any One Output) ..... ±25mA
DC Diode Input Current Enable Pin ..... ±1µA
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
DIC Package	75°C/W	16°C/W
Flatpack Package	64°C/W	12°C/W

Maximum Package Power Dissipation at +125°C
For T = -55°C to +100°C 1W
For T = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Common Mode Range ..... ±7.0V
Input Low Voltage (VIL) ..... 0V to 0.3VDD Max
Input High Voltage (VIH) ..... VDD to 0.7VDD Min
Input Rise and Fall Time ..... 500ns Max

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	(NOTE 2) LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH	VDD = 4.5V, VDIFF = 1.0V, IO = -6mA (Notes 2, 5)	1, 2, 3	-55°C, +25°C, +125°C	3.8	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, VDIFF = -1.0V, IO = 6mA (Note 5)	1, 2, 3	-55°C, +25°C, +125°C	-	0.3	V
Differential Input Voltage	VTH	VDD = VIH = 4.5V, -7.0V < VCM < 7.0V	1, 2, 3	-55°C, +25°C, +125°C	±200 Typical	±400	mV
Enabled High Level Input Voltage	VIH	VDD = 4.5V, 5.5V (Note 4)	1, 2, 3	-55°C, +25°C, +125°C	0.7 VDD	-	V
Enabled Low Level Input Voltage	VIL	VDD = 4.5V, 5.5V (Note 4)	1, 2, 3	-55°C, +25°C, +125°C	-	0.3 VDD	V
Input Current High (Differential Inputs)	IINH	VDD = 5.5, +V = 10V, -V = 0V and +V = 0V, -V = 10V	1, 2, 3	-55°C, +25°C, +125°C	-	1.8	mA
Input Current Low (Differential Inputs)	IINL	VDD = 5.5, +V = -10V, -V = 0V and +V = 0V, -V = -10V	1, 2, 3	-55°C, +25°C, +125°C	-	-2.7	mA
Input Leakage Enable Pins	IIN	VDD = 5.5V, VIN = 0V, 5.5V	1, 2, 3	-55°C, +25°C, +125°C	-	±1.0	µA
Tri-State Output Leakage Current	IOZ	VDD = 5.5V, VO = VDD or GND	1, 2, 3	-55°C, +25°C, +125°C	-5.0	5.0	µA
Standby Supply Current	IDDSB	VDD = 5.5V, VDIFF = 1.0V Outputs = Open	1, 2, 3	-55°C, +25°C, +125°C	-	25	mA
Enable Clamp Voltage	VIC	At -1mA	1, 2, 3	-55°C, +25°C, +125°C	-	-1.5	V
Input Hysteresis	VHYST		1	-55°C, +25°C, +125°C	20	100	mV
Input Resistance	RIN	-7V ≤ VCM ≤ 7V	1	-55°C, +25°C, +125°C	4	20	kΩ

NOTES:

1. All voltages referenced to device ground.
2. Force/Measure functions may be interchanged
3. These test condition are detailed in EIA specification RS-422
4. This parameter tested as inputs for the VOL, VOH and IOZ tests.
5. VIL = 0.3VDD, VIH = 0.7 VDD.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Time	TPLH, TPHL	VDD = 4.5V, VDIFF = 2.5V	9, 10, 11	-55°C, +25°C, +125°C	6	40	ns
Propagation Delay Time	TPZH, TPZL	VDD = 4.5V, VDIFF = 2.5V	9, 10, 11	-55°C, +25°C, +125°C	3	18	ns
Propagation Delay Time	TPLZ, TPHZ	VDD = 4.5V, VDIFF = 2.5V	9, 10, 11	-55°C, +25°C, +125°C	6	29	ns
Propagation Delay Time TRISE/TFALL	TTHL, TTLH	VDD = 4.5V, VDIFF = 2.5V	9, 10, 11	-55°C, +25°C, +125°C	2	12	ns

NOTES:

1. All voltages referenced to device ground.
2. See Table EIA RS-422

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz	1	-55°C, +25°C, +125°C	-	12	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz	1	-55°C, +25°C, +125°C	-	12	pF
Fail Safe	FSAFE	+ and - Inputs are Open, VOUT = Logic "1"	1	-55°C, +25°C, +125°C	3.8	-	V

NOTE:

1. The parameters listed on Table 3 are controlled via design or process parameters. Min and Max limits are guaranteed but not directly tested. These parameters are characterized at initial design release and upon design changes which would affect these characteristics.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

The post irradiation electrical performance characteristics are the same as the parameters listed in tables 1, 2 and 3.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C) AND GROUP B, SUBGROUP 5 DELTA PARAMETERS

PARAMETER	SYMBOL	DELTA LIMITS
Standby Supply Current	IDDSB	±4mA
Tri-State Output Leakage Current	IOZ	±1.0µA
Low Level Output Voltage	VOL	±60mV
High Level Output Voltage	VOH	±150mV
Input Leakage Current	IIL, IIH	±150nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100%/5004	1, 7, 9	See Table 5
Interim Test I (Post Burn-In)		100%/5004	1, 7, 9	See Table 5
Interim Test II (Post Burn-In)		100%/5004	1, 7, 9	See Table 5
PDA		100%/5004	1, 7, 9, Δ	
Interim Test III (Post-Burn-In)		100%/5004	1, 7, 9	See Table 5
PDA		100%/5004	1, 7, 9, Δ	-
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	-
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	-
Group B	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Δ	Subgroups 1, 2, 3, 9, 10, 11
	B6	Samples/5005	1, 7, 9	-
Group D		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	Subgroups 1, 2, 3, 9, 10, 11

TABLE 7. TOTAL DOSE IRRADIATION

CONFOMRANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE-RAD	POST-RAD	PRE-RAD	POST-RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 7, 9	Table 4

TABLE 8. BURN-IN TEST CONNECTIONS (+125°C < T_A < 139°C, VCC = 6V, ±0.5V)

TEST	OPEN	GROUND	POWER SUPPLY A VCC	POWER SUPPLY B 1/2VCC	POWER SUPPLY C 1/2 VCC	50KHz
Static Burn-In I	3, 5, 11, 13	2, 4, 6, 8, 10, 12, 14	1, 7, 9, 15, 16	-	-	-
Static Burn-In II	3, 5, 11, 13	1, 7, 8, 9, 15	2, 4, 6, 10, 12, 14, 16	-	-	-
Dynamic Burn-In Option 1	-	8, 12	4, 16	1, 3, 5, 7, 9, 11, 13, 15 (Note 2)	-	2, 6, 10, 14
Dynamic Burn-In Option 2	-	12, 8	4, 16	1, 7, 9, 15	3, 5, 11, 13	2, 6, 10, 14

NOTES:

1. Each pin except for VCC and GND will have a series resistor.
2. When connecting the - inputs and their associated outputs to the same supply, a power supply bypass capacitor of 22µF must be used.

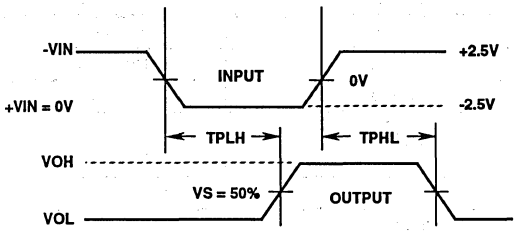
TABLE 9. IRRADIATION TEST CONNECTIONS (T_A = +25°C, ±5°C, VDD = 5V, ±10%)

TEST	OPEN	GROUND	VCC	1/2VCC	50KHz	25KHz
Radiation Exposure	3, 5, 11, 13	2, 4, 6, 8, 10, 12, 14	1, 7, 9, 15, 16	-	-	-

NOTES:

1. Each pin except for VCC and GND will have a series resistor.
2. When connecting the - inputs and their associated outputs to the same supply, a power supply bypass capacitor of 22µF must be used.

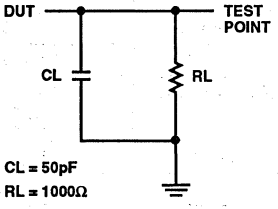
Propagation Delay Timing Diagram



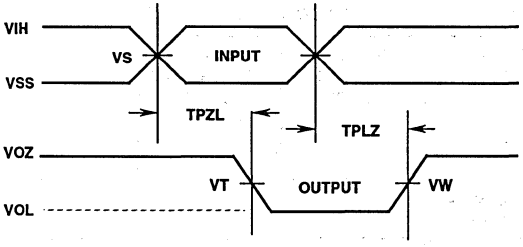
TRI-STATE LOW VOLTAGE LEVELS

PARAMETER	HS-26C32MSR	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	50	%
VW	VOH - 0.5	V
GND	0	V

Propagation Delay Load Circuit



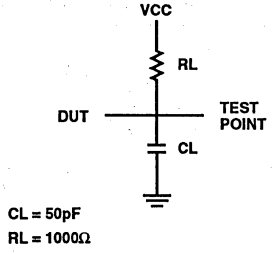
Tri-State Low Timing Diagrams



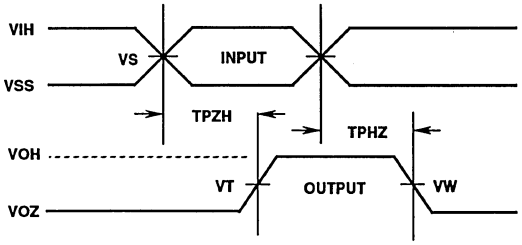
TRI-STATE LOW VOLTAGE LEVELS

PARAMETER	HS-26C32MSR	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	50	%
VW	VOL + 0.5	V
GND	0	V

Tri-State Low Load Circuit



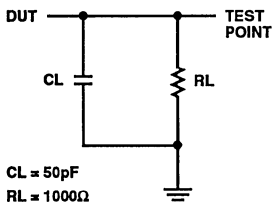
Tri-State High Timing Diagrams



TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	HS-26C32MSR	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	50	%
VW	VOH - 0.5	V
GND	0	V

Tri-State High Load Circuit



Harris - Space Level Product Flow

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

Radiation Verification (Each Wafer) Method 1019, 300k RAD (Si), 4 Samples/Wafer, 0 Rejects

100% Nondestructive Bond Pull Method 2023

100% Internal Visual Inspection Method 2010

100% Temperature Cycling Method 1010 Condition C

100% Constant Acceleration

100% Particle Impact Noise Detection Testing

100% External Visual Inspection

100% Serialization

100% Initial Electrical Test

100% Static Burn-In1: 24 Hour, +125°C Min, Method 1015

100% Interim Electrical Test 1 (Note 1)

100% Static Burn-In 2: 24 Hour, +125°C Min, Method 1015

100% Interim Electrical Test 2 (Note 1)

100% Dynamic Burn-In 240 Hour, +125°C or Equivalent, Method 1015

100% Interim Electrical 3 (Note 1)

100% Final Electrical Test

100% Fine and Gross Seal Method 1014

100% Radiographics Method 2012 (2 Views)

100% External Visual Method 2009

Group A (All Tests) Method 5005 (Class S)

Group B (Optional) Method 5005 (Class S) (Note 2)

Group D (Optional) Method 5005 (Class S) (Note 2)

CSI and/or GSI (Optional Note 2)

Data Package Generation (Note 3)

NOTES:

1. Failure from interim electrical tests 1 and 2 are combined for determining PDA (PDA = 5% for subgroups 1, 7, 9 and delta failures combined, PDA = 3% for subgroup 7 failures). Interim electrical tests 3 PDA (PDA = 5% for subgroups 1, 7, 9 and delta failures combined, PDA = 3% for subgroup 7 failures).
2. These steps are optional, and should be listed on the purchase order if required.
3. Data Package Contents:
   Cover Sheet (P.O. Number, Customer Number, Lot Date Code, Harris Number, Lot Number, Quantity).
   Certificate of Conformance (as found on shipper).
   Lot Serial Number Sheet (Good Unit(s) Serial Number and Lot Number).
   Variables Data (All Read, Record, and delta operations).
   Group A Attributes Data Summary.
   Wafer Lot Acceptance Report (Method 5007) to include SEM photos. NOTE: SEM photos to include % of step coverage.
   X-Ray Report and File(s), including parameter measurements.
   GAMMA Radiation Report with initial shipment of devices from the same wafer lot; containing a Cover Page, Disposition, Rad Dose, Lot Number, Test Package, Spec Number(s), Test Equipment, etc. Irradiation Read and Record data will be on file at Harris.

Metallization Topology

DIE DIMENSIONS:
84 mils x 130 mils
(2140µm x 3290µm)

METALLIZATION:
M1: Mo/Tiw
Thickness: 5800Å
M2: Al/Si/Cu
Thickness: 5800Å

GLASSIVATION:
Type: SiO_2
Thickness: 10kÅ ± 1kÅ

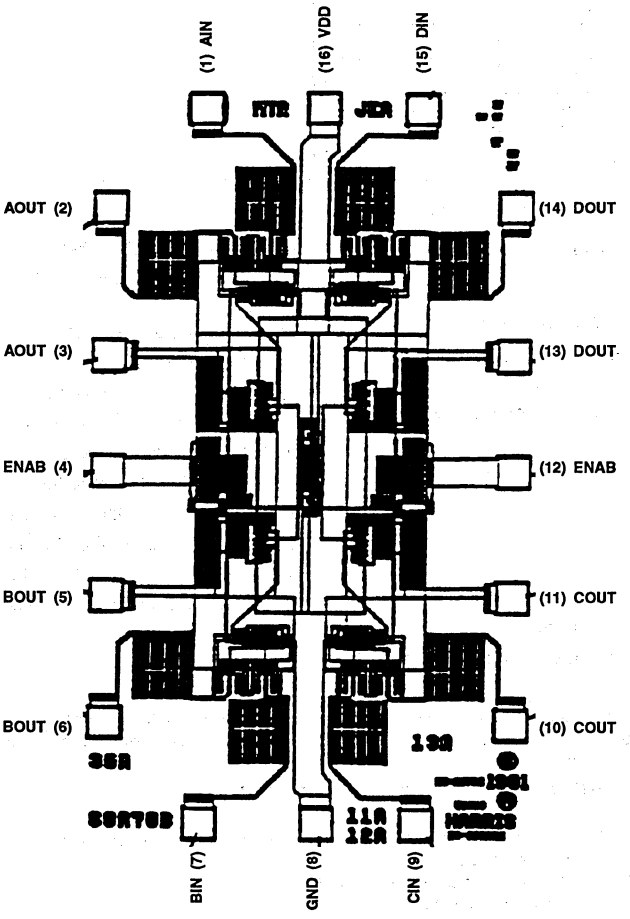
DIE ATTACH:
Silver Glass

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE: 110µm x 100µm

Metallization Mask Layout

HS-26CT32MS



HARRIS SEMICONDUCTOR

HS-26CT31MS

Radiation Hardened Quad Differential Line Driver

December 1992

Features

- 1.2 Micron Radiation Hardened CMOS
  - Total Dose Up to 300K RAD(Si)
  - Dose Rate Upset > $1x10^9$ RAD/Sec (20nS Pulse)
- Latchup Free
- EIA RS-422 Compatible Outputs (Except for IOS)
- TTL Compatible Inputs
- High Impedance Outputs when Disabled or Powered Down
- Low Power Dissipation 2.75mW Standby (Max)
- Single 5V Supply
- Low Output Impedance 10Ω or Less
- Full -55°C to +125°C Military Temperature Range

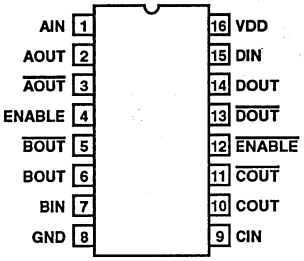
Description

The Harris HS-26CT31MSR is a quad differential line driver designed for digital data transmission over balanced lines and meets the requirements of EIA standard RS-422. Radiation hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

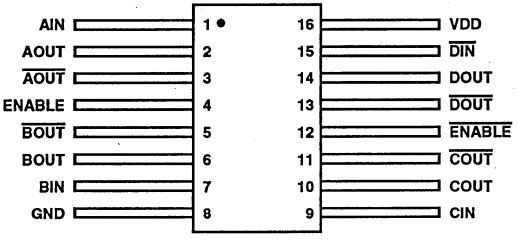
The HS-26CT31MSR accepts TTL and converts them to RS-422 compatible outputs. This circuit uses special outputs that enable the drivers to power down without loading down the bus. Enable and disable pins allow several devices to be connected to the same data source and addressed independantly.

Pinouts

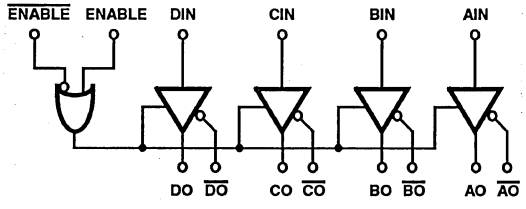
HS1-26CT31MSR 16 PIN CERAMIC DUAL-IN-LINE
CASE OUTLINE D2, CONFIGURATION 3
TOP VIEW



HS9-26CT31MSR 16 PIN FLATPACK
CASE OUTLINE F5A, CONFIGURATION 2
TOP VIEW



Logic Diagram



TRUTH TABLE

DEVICE POWER ON/OFF	INPUTS			OUTPUT	
	ENABLE	$\overline{ENABLE}$	IN	OUT	$\overline{OUT}$
ON	0	1	X	HI-Z	HI-Z
ON	1	X	0	0	1
ON	X	0	0	0	1
ON	1	X	1	1	0
ON	X	0	1	1	0
OFF	X	X	X	HI-Z	HI-Z

9 SERIAL COMMUNICATIONS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 2929

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input, Output or I/O Voltage ..... -0.5 to VDD+0.5V
DC Diode Input Current (Any Input) ..... ±20mA
DC Drain Current (Any One Input) 350mA
DC VDD or Ground Current 400mA
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
DIC Package	75°C/W	16°C/W
Flatpack Package	64°C/W	12°C/W

Maximum Package Power Dissipation at +125°C
For T = -55°C to +100°C 1W
For T = +100°C to +125°C. ..... Derate Linearly at 13mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Rise and Fall Time ..... 500ns Max
Input Low Voltage (VIL) ..... 0V to 0.8V Max
Input High Voltage (VIH) ..... VDD to VDD/2V Min

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH	VDD = 4.5V, and 5.5V IO = -20mA (Notes 2, 6)	1, 2, 3	-55°C, +25°C, +125°C	2.5	-	V
Low Level Output Voltage	VOL	VDD = VIH = 4.5V and 5.5V IO = 20mA , VIL = 0V (Notes 2, 6)	1, 2, 3	-55°C, +25°C, +125°C	-	0.5	V
Differential Output Voltage	VT	VDD = VIH = 4.5V, RL = 100Ω , VIL = 0V (Note 3)	1, 2, 3	-55°C, +25°C, +125°C	2.0	-	V
Difference in Differential Output	IVTI - IVTI	VDD = VIH = 4.5V, RL = 100Ω , VIL = 0V (Note 3)	1, 2, 3	-55°C, +25°C, +125°C	-	0.4	V
Common Mode Output Voltage	VOS	VDD = VIH = 4.5V, RL = 100Ω , VIL = 0V (Note 3)	1, 2, 3	-55°C, +25°C, +125°C	-	3.0	V
Difference in Common Mode Output	IVOS - VOSI	VDD = VIH = 4.5V, RL = 100Ω , VIL = 0V (Note 3)	1, 2, 3	-55°C, +25°C, +125°C	-	0.4	V
High Level Input Voltage	VIH	VDD = 4.5V, 5.5V (Note 5)	1, 2, 3	-55°C, +25°C, +125°C	VDD/ 2.0	-	V
Low Level Input Voltage	VIL	VDD = 4.5V, 5.5V (Note 5)	1, 2, 3	-55°C, +25°C, +125°C	-	0.8	V
Standby Supply Current	IDDSB	VDD = 5.5V, Output = 0, VIN = VDD or GND	1, 2, 3	-55°C, +25°C, +125°C	-	500	µA
Tristate Output Leakage Current	IOZ	VDD = 5.5V, Force Voltage = 0V or VCC	1, 2, 3	-55°C, +25°C, +125°C	-	±5	µA
Delta Supply Current	ΔICC	VDD = 5.5V, VIN = 2.4V, 0.5V	1, 2, 3	-55°C, +25°C, +125°C	-	2.0	mA
Input Leakage	IIN	VDD = 5.5V, VIN = VDD or GND	1, 2, 3	-55°C, +25°C, +125°C	-	±1.0	µA
Output Leakage Current Power OFF	IOFF	VDD = 0V, VOUT = 6V, 0V	1, 2, 3	-55°C, +25°C, +125°C	-100	100	µA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Clamp Voltage	VIC	At -1.0mA	1, 2, 3	-55°C, +25°C, +125°C	-	-1.5	V
		At +1.0mA	1, 2, 3	-55°C, +25°C, +125°C	-	+1.5	V

NOTES:

1. All voltages referenced to device ground.
2. Force/Measure functions may be interchanged.
3. These test conditions are detailed in EIA specification RS-422.
4. Only one input pin set up to VIN per test. All other pins set to VCC or GND.
5. This parameter tested as inputs levels in VOL/VOH, IOZ, functional test.
6. VIL = 0.8V, VIH = VCC/2.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPLH, TPHL	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	2	18	ns
Propagation Delay	TPZH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	5	28	ns
Propagation Delay	TPZL	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	5	28	ns
Propagation Delay	TPHZ	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	2	18	ns
Propagation Delay	TPLZ	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	2	18	ns
Rise and Fall Times	TTHL, TTLH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	1	10	ns
Output Skew	TSKEW	VDD = 4.5V, RL = 100Ω, CL = 40pF	9, 10, 11	-55°C, +25°C, +125°C	-	3	ns

NOTES:

1. All voltages referenced to device ground.
2. See Table EIA RS-422

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz	1	-55°C, +25°C, +125°C	-	12	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz	1	-55°C, +25°C, +125°C	-	12	pF

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Operating Short Circuit	IOS	VDD = 5.5V, VIN = VDD or GND, VOUT = 0V	2	-55°C, +25°C, +125°C	-30	-150	mA
On-State Resistance	RON	VDD = 4.5V, VOUT = 1.5V, VIN = VDD or GND	1	-55°C, +25°C, +125°C	-	10	Ω

NOTES:

1. Parameters listed in table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major design or process changes that affect these parameters.
2. Only one output at a time may be shorted.
3. Power Up/Down Feature: Outputs will remain in the Hi-Z state with VDD ≤ 2.5V and become active at VDD ≥ 4.0V. The active output state will be determined by the input conditions.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

The post irradiation electrical performance characteristics are the same as the parameters listed in tables 1, 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C) AND GROUP B, SUBGROUP 5 DELTA PARAMETERS

PARAMETER	SYMBOL	DELTA LIMITS
Standby Supply Current	IDDSB	±100µA
Tri-State Output Leakage Current	IOZ	±1.0µA
Low Level Output Voltage	VOL	±60mV
High Level Output Voltage	VOH	±150mV
Input Leakage Current	IIL, IIH	±150nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100%/5004	1, 7, 9	See Table 5
Interim Test I (Post Burn-In)		100%/5004	1, 7, 9	See Table 5
Interim Test II (Post Burn-In)		100%/5004	1, 7, 9	See Table 5
PDA		100%/5004	1, 7, 9, Δ	-
Interim Test III (Post-Burn-In)		100%/5004	1, 7, 9	See Table 5
PDA		100%/5004	1, 7, 9, Δ	-
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	-
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	-
Group B	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Δ	Subgroups 1, 2, 3, 9, 10, 11
	B6	Samples/5005	1, 7, 9	-
Group D		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	-

TABLE 7. TOTAL DOSE IRRADIATION

CONFOMRANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE-RAD	POST-RAD	PRE-RAD	POST-RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 7, 9	Table 4

TABLE 8. BURN-IN TEST CONNECTIONS (+125°C < T_A < 139°C, VCC = 6V, ±0.5V)

TEST	OPEN	GROUND	VDD	1/2VDD	50KHz	25KHz
Static Burn-In I	2, 3, 5, 6, 10, 11, 13, 14	1, 4, 7, 8, 9, 12, 15	16	-	-	-
Static Burn-In II	2, 3, 5, 6, 10, 11, 13, 14	8	1, 4, 7, 9, 12, 15, 16	-	-	-
Dynamic Burn-In	-	8, 12	4, 16	2, 3, 5, 6, 10, 11, 13, 14	1, 7, 9, 15	-

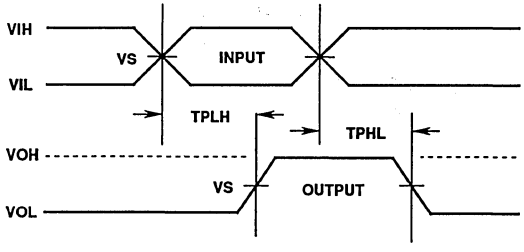
NOTE: Each pin except for VDD and Ground will have a series resistor.

TABLE 9. IRRADIATION TEST CONNECTIONS (T_A = +25°C, ±5°C, VDD = 5V, ±10%)

TEST	OPEN	GROUND	VDD	1/2VDD	50KHz	25KHz
Radiation Exposure	2, 3, 5, 6, 10, 11, 13, 14	8	1, 4, 7, 9, 12, 15, 16	-	-	-

NOTE: Each pin except for VDD and Ground will have a series resistor.

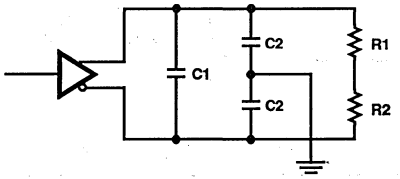
Propagation Delay Timing Diagram



AC VOLTAGE LEVELS

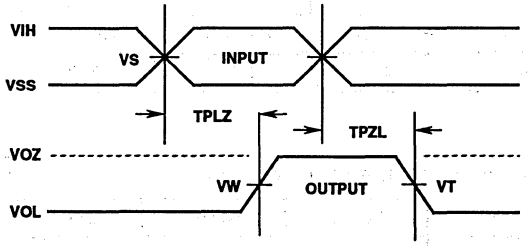
PARAMETER	HS-26CT31MSR	UNITS
VDD	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V
VT	2.25	V

Propagation Delay Load Circuit



C1 = C2 = C3 = 40pF
R1 = R2 = 50Ω

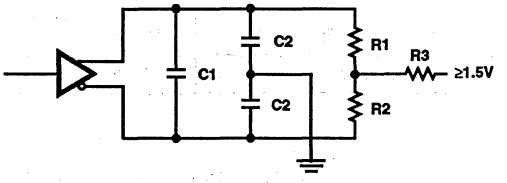
Tri-State Low Timing Diagrams



TRI-STATE LOW VOLTAGE LEVELS

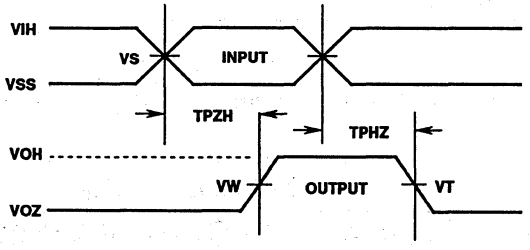
PARAMETER	HS-26CT31MSR	UNITS
VDD	4.50	V
VIH	3.00	V
VS	1.30	V
VW	VOL + 0.3	V
VT	0.80	V

Tri-State Low Load Circuit



C1 = C2 = C3 = 40pF
R1 = R2 = 50Ω
R3 = 500Ω

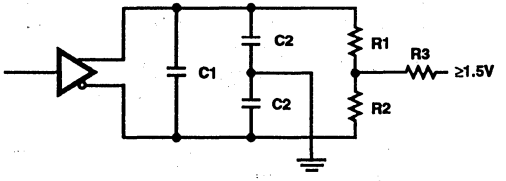
Tri-State High Timing Diagrams



TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	HS-26CT31MSR	UNITS
VDD	4.50	V
VIH	3.00	V
VS	1.30	V
VT	VOH - 0.3	V
VW	2.00	V

Tri-State High Load Circuit



C1 = C2 = C3 = 40pF
R1 = R2 = 50Ω
R3 = 500Ω

Harris - Space Level Product Flow

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

Radiation Verification (Each Wafer) Method 1019, 300k RAD (Si), 4 Samples/Wafer, 0 Rejects

100% Nondestructive Bond Pull Method 2023

100% Internal Visual Inspection Method 2010

100% Temperature Cycling Method 1010 Condition C

100% Constant Acceleration

100% Particle Impact Noise Detection Testing

100% External Visual Inspection

100% Serialization

100% Initial Electrical Test

100% Static Burn-In1: 24 Hour, +125°C Min, Method 1015

100% Interim Electrical Test 1 (Note 1)

100% Static Burn-In 2: 24 Hour, +125°C Min, Method 1015

100% Interim Electrical Test 2 (Note 1)

100% Dynamic Burn-In 240 Hour, +125°C or Equivalent, Method 1015

100% Interim Electrical 3 (Note 1)

100% Final Electrical Test

100% Fine and Gross Seal Method 1014

100% Radiographics Method 2012 (2 Views)

100% External Visual Method 2009

Group A (All Tests) Method 5005 (Class S)

Group B (Optional) Method 5005 (Class S) (Note 2)

Group D (Optional) Method 5005 (Class S) (Note 2)

CSI and/or GSI (Optional (Note 2)

Data Package Generation (Note 3)

NOTES:

1. Failure from interim electrical tests 1 and 2 are combined for determining PDA (PDA = 5% for subgroups 1, 7, 9 and delta failures combined, PDA = 3% for subgroup 7 failures). Interim electrical tests 3 PDA (PDA = 5% for subgroups 1, 7, 9 and delta failures combined, PDA = 3% for subgroup 7 failures).
2. These steps are optional, and should be listed on the purchase order if required.
3. Data Package Contents:
   Cover Sheet (P.O. Number, Customer Number, Lot Date Code, Harris Number, Lot Number, Quantity).
   Certificate of Conformance (as found on shipper).
   Lot Serial Number Sheet (Good Unit(s) Serial Number and Lot Number).
   Variables Data (All Read, Record, and delta operations).
   Group A Attributes Data Summary.
   Wafer Lot Acceptance Report (Method 5007) to include SEM photos. NOTE: SEM photos to include % of step coverage.
   X-Ray Report and File(s), including parameter measurements.
   GAMMA Radiation Report with initial shipment of devices from the same wafer lot; containing a Cover Page, Disposition, Rad Dose, Lot Number, Test Package, Spec Number(s), Test Equipment, etc. Irradiation Read and Record data will be on file at Harris.

Metallization Topology

DIE DIMENSIONS:
84 mils x 130 mils
(2140µm x 3290µm)

METALLIZATION:
M1: Mo/Tiw
Thickness: 5800Å
M2: Al/Si/Cu
Thickness: 5800Å

GLASSIVATION:
Type: SiO_2
Thickness: 10kÅ ± 1kÅ

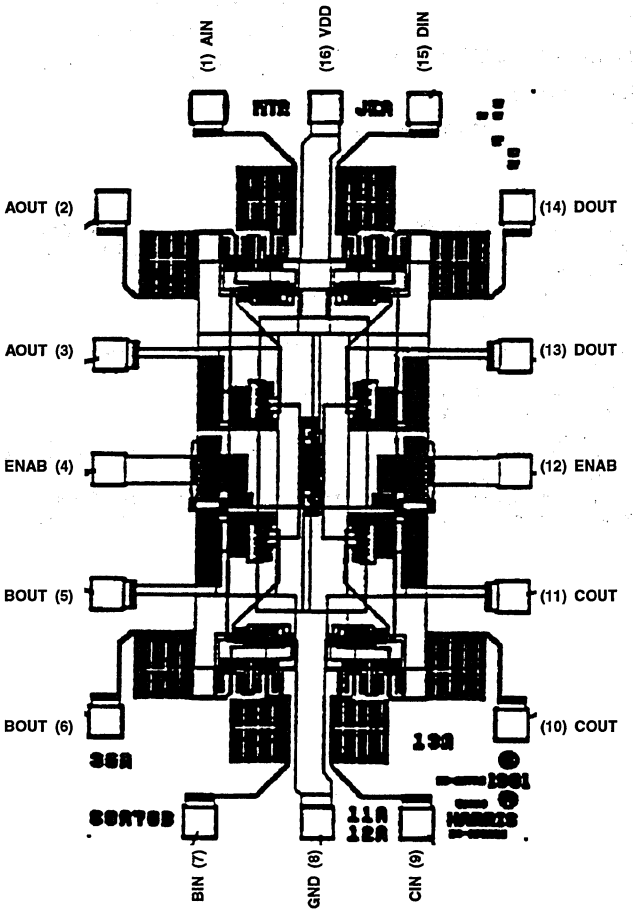
DIE ATTACH:
Silver Glass

WORST CASE CURRENT DENSITY:
<2.0 x 10^5A/cm^2

BOND PAD SIZE: 110µm x 100µm

Metallization Mask Layout

HS-26C32MS



HARRIS SEMICONDUCTOR

HS-26CT32MS

Radiation Hardened Quad Differential Line Receiver

December 1992

Features

- 1.2 Micron Radiation Hardened CMOS
  - Total DoseUp to 300K RAD(Si)
  - Dose Rate Upset > $1x10^9$ RADs (Si)/s (20nS Pulse)
- Latchup Free
- EIA RS-422 Compatible Outputs
- TTL/CMOS Compatible Inputs
- Input Fail Safe Circuitry
- High Impedance Inputs when Disabled or Powered Down
- Low Power Dissipation 138mW Standby (Max)
- Single 5V Supply
- Full -55°C to +125°C Military Temperature Range

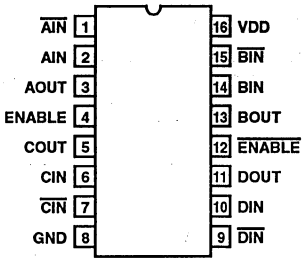
Description

The Harris HS-26CT32MSR is a differential line receiver designed for digital data transmission over balanced lines and meets the requirements of EIA standard RS-422. Radiation hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

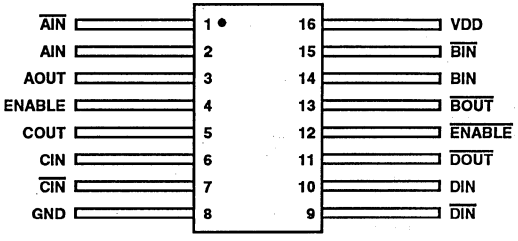
The HS-26CT32MSR has an input sensitivity of 200mV over the common mode input voltage range of ±7V. The receivers are also equipped with input fail safe circuitry, which causes the outputs to go to a logic "1" when the inputs are open. Enable and Disable functions are common to all four receivers.

Pinouts

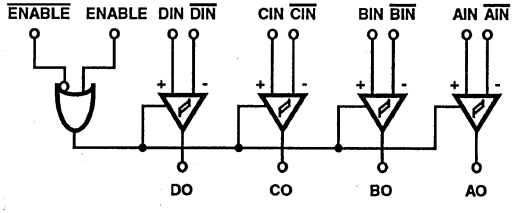
HS1-26CT32MSR 16 PIN CERAMIC DUAL-IN-LINE
CASE OUTLINE D2, CONFIGURATION 3
TOP VIEW



HS9-26CT32MSR 16 PIN FLATPACK
CASE OUTLINE F5A, CONFIGURATION 2
TOP VIEW



Logic Diagram



TRUTH TABLE

DEVICE POWER ON/OFF	INPUTS			OUTPUT
	ENABLE	$\overline{\text{ENABLE}}$	INPUT	OUT
ON	0	1	X	HI-Z
ON	1	X	VID > VTH	1
ON	1	X	VID > VTH	0
ON	X	0	VID > VTH	1
ON	X	0	VID > VTH	0
ON	1	X	Open	1
ON	X	0	Open	1
OFF	X	X	X	HI-Z

9 SERIAL COMMUNICATIONS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 2930

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Differential Input Voltage ..... ±12V
Common Mode Range ..... ±12V
Enable Pins Input Voltage ..... -0.5V to VDD+0.5V
DC Drain Current (Any One Output) ..... ±25mA
DC Diode Input Current Enable Pin ..... ±1µA
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
DIC Package	75°C/W	16°C/W
Flatpack Package	64°C/W	12°C/W

Maximum Package Power Dissipation at +125°C
For T = -55°C to +100°C 1W
For T = +100°C to +125°C ..... Derate Linearly at 13mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Common Mode Range ..... ±7.0V
Input Low Voltage (VIL) ..... 0V to 0.8V Max
Input High Voltage (VIH) ..... VDD to VDD/2V Min
Input Rise and Fall Time ..... 500ns Max

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	(NOTE 2) LIMITS MIN	(NOTE 2) LIMITS MAX	UNITS
High Level Output Voltage	VOH	VDD = 4.5V, VDIFF = 1.0V, IO = -6mA (Notes 2, 5)	1, 2, 3	-55°C, +25°C, +125°C	3.8	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, VDIFF = -1.0V, IO = 6mA (Note 5)	1, 2, 3	-55°C, +25°C, +125°C	-	0.3	V
Differential Input Voltage	VTH	VDD = VIH = 4.5V, -7.0V < VCM < 7.0V	1, 2, 3	-55°C, +25°C, +125°C	±200 Typical	±400	mV
Enabled High Level Input Voltage	VIH	VDD = 4.5V, 5.5V (Note 4)	1, 2, 3	-55°C, +25°C, +125°C	VDD/ 2.0	-	V
Enabled Low Level Input Voltage	VIL	VDD = 4.5V, 5.5V (Note 4)	1, 2, 3	-55°C, +25°C, +125°C	-	0.8	V
Input Current High (Differential Inputs)	IINH	VDD = 5.5, +V = 10V, -V = 0V and +V = 0V, -V = 10V	1, 2, 3	-55°C, +25°C, +125°C	-	1.8	mA
Input Current Low (Differential Inputs)	IINL	VDD = 5.5, +V = -10V, -V = 0V and +V = 0V, -V = -10V	1, 2, 3	-55°C, +25°C, +125°C	-	-2.7	mA
Input Leakage Enable Pins	IIN	VDD = 5.5V, VIN = 0V, 5.5V	1, 2, 3	-55°C, +25°C, +125°C	-	±1.0	µA
Tri-State Output Leakage Current	IOZ	VDD = 5.5V, VO = VDD or GND	1, 2, 3	-55°C, +25°C, +125°C	-5.0	5.0	µA
Standby Supply Current	IDDSB	VDD = 5.5V, VDIFF = 1.0V Outputs = Open	1, 2, 3	-55°C, +25°C, +125°C	-	25	mA
Enable Clamp Voltage	VIC	At -1mA	1, 2, 3	-55°C, +25°C, +125°C	-	-1.5	V
Input Hysteresis	VHYST		1	-55°C, +25°C, +125°C	20	100	mV
Input Resistance	RIN	-7V ≤ VCM ≤ 7V	1	-55°C, +25°C, +125°C	4	20	kΩ

NOTES:

1. All voltages referenced to device ground.
2. Force/Measure functions may be interchanged
3. These test condition are detailed in EIA specification RS-422.
4. This parameter tested as inputs for the VOL, VOH, IOZ tests.
5. VIL = 0.8V and VIN = VDD/2.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Time	TPLH, TPHL	VDD = 4.5V, VDIFF = 2.5V	9, 10, 11	-55°C, +25°C, +125°C	6	40	ns
Propagation Delay Time	TPZH, TPZL	VDD = 4.5V, VDIFF = 2.5V	9, 10, 11	-55°C, +25°C, +125°C	3	18	ns
Propagation Delay Time	TPLZ, TPHZ	VDD = 4.5V, VDIFF = 2.5V	9, 10, 11	-55°C, +25°C, +125°C	6	29	ns
Propagation Delay Time TRISE/TFALL	TTHL, TTLH	VDD = 4.5V, VDIFF = 2.5V	9, 10, 11	-55°C, +25°C, +125°C	2	12	ns

NOTES:

1. All voltages referenced to device ground.
2. See Table EIA RS-422

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz	1	-55°C, +25°C, +125°C	-	12	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz	1	-55°C, +25°C, +125°C	-	12	pF
Fail Safe	FSAFE	+ and - Inputs are Open, VOUT = Logic "1"	1	-55°C, +25°C, +125°C	3.8	-	V

NOTE:

1. The parameters listed on Table 3 are controlled via design or process parameters. Min and Max limits are guaranteed but not directly tested. These parameters are characterized at initial design release and upon design changes which would affect these characteristics.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

The post irradiation electrical performance characteristics are the same as the parameters listed in tables 1, 2 and 3.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C) AND GROUP B, SUBGROUP 5 DELTA PARAMETERS

PARAMETER	SYMBOL	DELTA LIMITS
Standby Supply Current	IDDSB	±4mA
Tri-State Output Leakage Current	IOZ	±1.0µA
Low Level Output Voltage	VOL	±60mV
High Level Output Voltage	VOH	±150mV
Input Leakage Current	IIL, IIH	±150nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100%/5004	1, 7, 9	See Table 5
Interim Test I (Post Burn-In)		100%/5004	1, 7, 9	See Table 5
Interim Test II (Post Burn-In)		100%/5004	1, 7, 9	See Table 5
PDA		100%/5004	1, 7, 9, Δ	
Interim Test III (Post-Burn-In)		100%/5004	1, 7, 9	See Table 5
PDA		100%/5004	1, 7, 9, Δ	-
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	-
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	-
Group B	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Δ	Subgroups 1, 2, 3, 9, 10, 11
	B6	Samples/5005	1, 7, 9	-
Group D		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	Subgroups 1, 2, 3, 9, 10, 11

TABLE 7. TOTAL DOSE IRRADIATION

CONFOMRANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE-RAD	POST-RAD	PRE-RAD	POST-RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 7, 9	Table 4

TABLE 8. BURN-IN TEST CONNECTIONS (+125°C < T_A < 139°C, VCC = 6V, ±0.5V)

TEST	OPEN	GROUND	POWER SUPPLY A VCC	POWER SUPPLY B 1/2VCC	POWER SUPPLY C 1/2 VCC	50KHz
Static Burn-In I	3, 5, 11, 13	2, 4, 6, 8, 10, 12, 14	1, 7, 9, 15, 16	-	-	-
Static Burn-In II	3, 5, 11, 13	1, 7, 8, 9, 15	2, 4, 6, 10, 12, 14, 16	-	-	-
Dynamic Burn-In Option 1	-	8, 12	4, 16	1, 3, 5, 7, 9, 11, 13, 15 (Note 2)	-	2, 6, 10, 14
Dynamic Burn-In Option 2	-	12, 8	4, 16	1, 7, 9, 15	3, 5, 11, 13	2, 6, 10, 14

NOTES:

1. Each pin except for VCC and GND will have a series resistor. (For static BI, R = 10kΩ ±5%, for dynamic BI, R = 680Ω ±5%)
2. When connecting the - inputs and their associated outputs to the same supply, a power supply bypass capacitor of 22µF must be used.

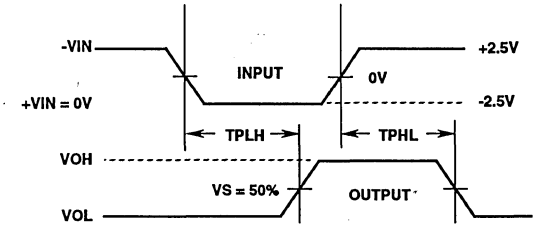
TABLE 9. IRRADIATION TEST CONNECTIONS (T_A = +25°C, ±5°C, VDD = 5V, ±10%)

TEST	OPEN	GROUND	VCC	1/2VCC	50KHz	25KHz
Radiation Exposure	3, 5, 11, 13	2, 4, 6, 8, 10, 12, 14	1, 7, 9, 15, 16	-	-	-

NOTES:

1. Each pin except for VCC and GND will have a series resistor. (R = 47kΩ ±5%).
2. When connecting the - inputs and their associated outputs to the same supply, a power supply bypass capacitor of 22µF must be used.

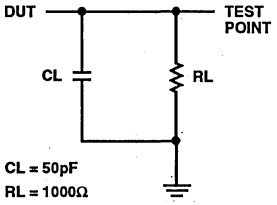
Propagation Delay Timing Diagram



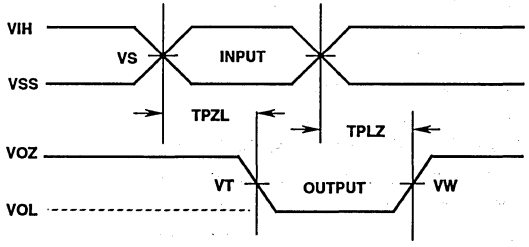
TRI-STATE LOW VOLTAGE LEVELS

PARAMETER	HS-26CT32MSR	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	50	%
VW	VOH - 0.5	V
GND	0	V

Propagation Delay Load Circuit



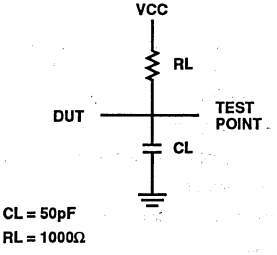
Tri-State Low Timing Diagrams



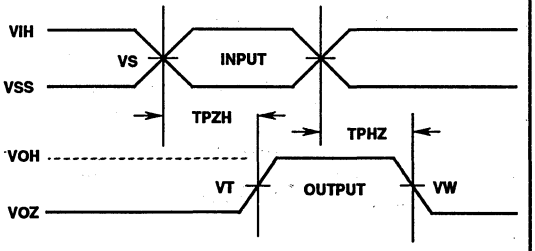
TRI-STATE LOW VOLTAGE LEVELS

PARAMETER	HS-26CT32MSR	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	50	%
VW	VOL + 0.5	V
GND	0	V

Tri-State Low Load Circuit



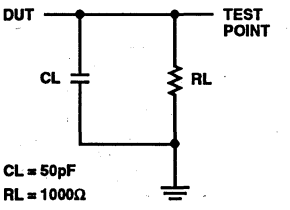
Tri-State High Timing Diagrams



TRI-STATE HIGH VOLTAGE LEVELS

PARAMETER	HS-26CT32MSR	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	50	%
VW	VOH - 0.5	V
GND	0	V

Tri-State High Load Circuit



Harris - Space Level Product Flow

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

Radiation Verification (Each Wafer) Method 1019, 300k RAD (Si), 4 Samples/Wafer, 0 Rejects

100% Nondestructive Bond Pull Method 2023

100% Internal Visual Inspection Method 2010

100% Temperature Cycling Method 1010 Condition C

100% Constant Acceleration

100% Particle Impact Noise Detection Testing

100% External Visual Inspection

100% Serialization

100% Initial Electrical Test

100% Static Burn-In1: 24 Hour, +125°C Min, Method 1015

100% Interim Electrical Test 1 (Note 1)

100% Static Burn-In 2: 24 Hour, +125°C Min, Method 1015

100% Interim Electrical Test 2 (Note 1)

100% Dynamic Burn-In 240 Hour, +125°C or Equivalent, Method 1015

100% Interim Electrical 3 (Note 1)

100% Final Electrical Test

100% Fine and Gross Seal Method 1014

100% Radiographics Method 2012 (2 Views)

100% External Visual Method 2009

Group A (All Tests) Method 5005 (Class S)

Group B (Optional) Method 5005 (Class S) (Note 2)

Group D (Optional) Method 5005 (Class S) (Note 2)

CSI and/or GSI (Optional (Note 2)

Data Package Generation (Note 3)

NOTES:

1. Failure from interim electrical tests 1 and 2 are combined for determining PDA (PDA = 5% for subgroups 1, 7, 9 and delta failures combined, PDA = 3% for subgroup 7 failures). Interim electrical tests 3 PDA (PDA = 5% for subgroups 1, 7, 9 and delta failures combined, PDA = 3% for subgroup 7 failures).
2. These steps are optional, and should be listed on the purchase order if required.
3. Data Package Contents:
   Cover Sheet (P.O. Number, Customer Number, Lot Date Code, Harris Number, Lot Number, Quantity).
   Certificate of Conformance (as found on shipper).
   Lot Serial Number Sheet (Good Unit(s) Serial Number and Lot Number).
   Variables Data (All Read, Record, and delta operations).
   Group A Attributes Data Summary.
   Wafer Lot Acceptance Report (Method 5007) to include SEM photos. NOTE: SEM photos to include % of step coverage.
   X-Ray Report and File(s), including parameter measurements.
   GAMMA Radiation Report with initial shipment of devices from the same wafer lot; containing a Cover Page, Disposition, Rad Dose, Lot Number, Test Package, Spec Number(s), Test Equipment, etc. Irradiation Read and Record data will be on file at Harris.

Metallization Topology

DIE DIMENSIONS:
84mils x 130 mils
(2140µm x 3290µm)

METALLIZATION:
M1: Mo/Tiw
Thickness: 5800Å

M2: Al/Si/Cu
Thickness: 10kÅ ±1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 10kÅ ± 1kÅ

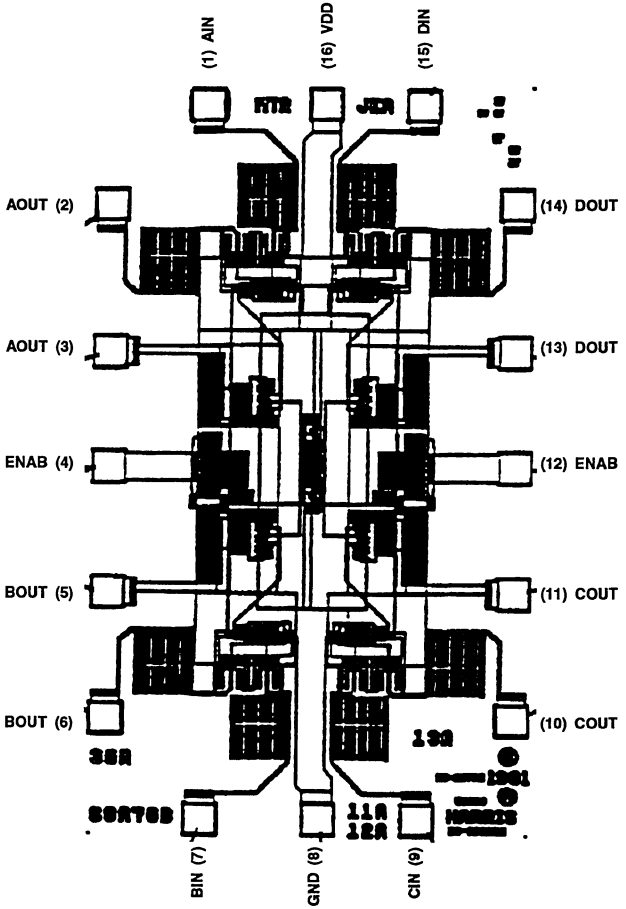
DIE ATTACH:
Silver Glass

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE: 110µm x 100µm

Metallization Mask Layout

HS-26C/T32RH



RAD HARD 10

MICROPROCESSORS

HARRIS SEMICONDUCTOR

HS-80C85RH

Radiation Hardened 8-Bit CMOS Microprocessor

December 1992

Features

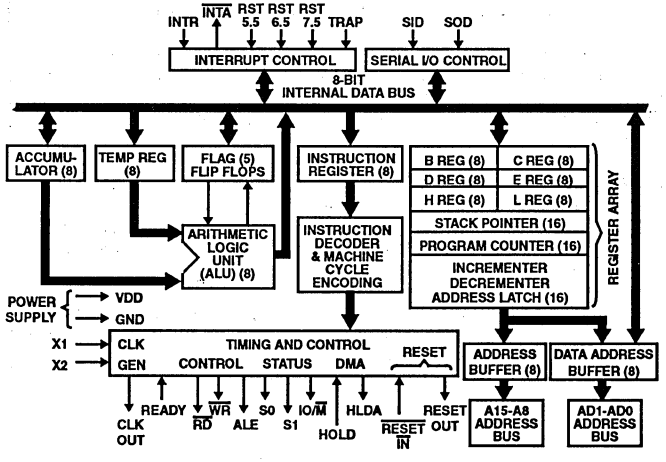
- Radiation Hardened EPI-CMOS
  - Parametrics Guaranteed 1 x 10^5 RAD(Si)
  - Transient Upset > 1 x 10^8 RAD(Si)/s
  - Latch-up Free > 1 x 10^{12} RAD(Si)/s
- Low Standby Current 500µA Max
- Low Operating Current 5.0mA/MHz (X_1 Input)
- Electrically Equivalent to Sandia SA 3000
- 100% Software Compatible with INTEL 8085
- Operation from DC to 2MHz, Post Radiation
- Single 5 Volt Power Supply
- On-Chip Clock Generator and System Controller
- Four Vectored Interrupt Inputs
- Completely Static Design
- Self Aligned Junction Isolated (SAJI) Process
- Military Temperature Range -55°C to +125°C

Description

The HS-80C85RH is an 8-bit CMOS microprocessor fabricated using the Harris radiation hardened self-aligned junction isolated (SAJI) silicon gate technology. Latch-up free operation is achieved by the use of epitaxial starting material to eliminate the parasitic SCR effect seen in conventional bulk CMOS devices.

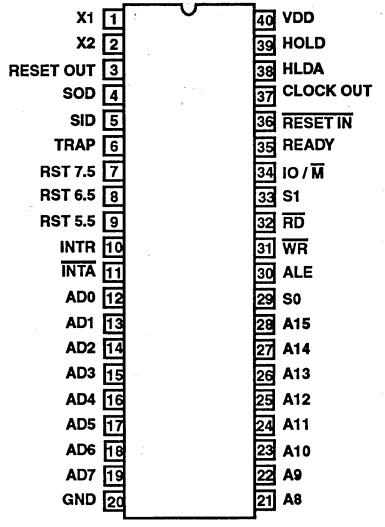
The HS-80C85RH is a functional logic emulation of the HMOS 8085 and its instruction set is 100% software compatible with the HMOS device. The HS80C85RH is designed for operation with a single 5 volt power supply. Its high level of integration allows the construction of a radiation hardened microcomputer system with as few as three ICs (HS-80C85RH CPU, HS83C55RH ROM I/O, and the HS-81C55/56RH RAM I/O.

Functional Diagram

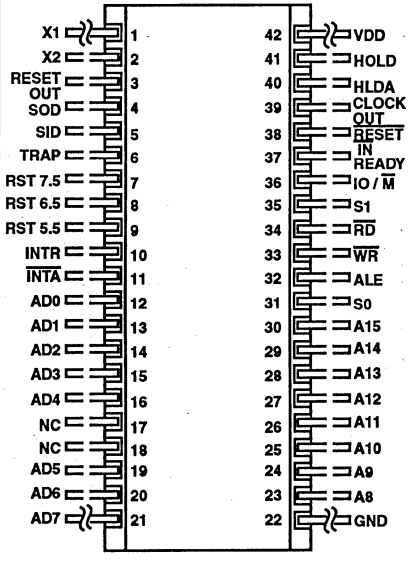


Pinouts

HS-80C85RH 40 LEAD BRAZE SEAL DIP
COMPLIANT OUTLINE D5, CONFIGURATION 3
TOP VIEW



HS-80C85RH 42 LEAD BRAZE SEAL FLATPACK
HARRIS PACKAGE CODE HWN
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

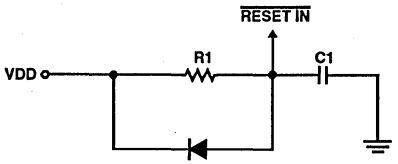
File Number **3036**

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
A8 - A15	21-28	O	Address Bus: The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.
AD0-7	12-19	I/O	Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.
ALE	32	O	Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.
S0, S1, and IO/$\overline{M}$	31, 35, & 36	O	Machine Cycle Status: IO/$\overline{M}$ S1 S0 Status 0 0 1 Memory write 0 1 0 Memory write 1 0 1 I/O write 1 1 0 I/O read 0 1 1 Opcode fetch 1 1 1 Opcode fetch 1 1 1 Interrupt acknowledge T 0 0 Halt T X X Hold T X X Reset T = 3-State (high impedance) X = Unspecified S1 can be used as an advanced R/$\overline{W}$ status. IO/$\overline{M}$, S0 and S1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.
$\overline{RD}$	34	O	Read Control: A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.
$\overline{WR}$	33	O	Write Control: A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$, 3-stated during Hold and Halt modes and during RESET.
READY	35	I	Ready: If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times.
HOLD	39	I	Hold: Indicates that another master is requesting the use of the address and data buses. The cpu, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data Bus, $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.
HLDA	38	O	Hold Acknowledge: Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle after HLDA goes low.

Pin Description (Continued)

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
INTR	10	I	Interrupt Request: Is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.
$\overline{INTA}$	11	O	Interrupt Acknowledge: Is used instead of (and has the same timing as) $\overline{RD}$ during the Instruction cycle after an INTR is accepted. It can be used to activate an 8259A Interrupt chip or some other interrupt port.
RST 5.5 RST 6.5 RST 7.5	9 8 7	I	Restart Interrupts: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 6. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.
TRAP	6	I	Trap: Trap interrupt is a non-maskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt. (See Table 6.)
$\overline{RESET\ IN}$	36	I	Reset In: Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{RESET\ IN}$ is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay (see Figure 1). Upon power-up, $\overline{RESET\ IN}$ must remain low for at least 10 "clock cycle" after minimum VDD has been reached. For proper reset operation after the power-up duration, $\overline{RESET\ IN}$ should be kept low a minimum of three clock periods. The CPU is held in the reset condition as long as $\overline{RESET\ IN}$ is applied.
RESET OUT	3	O	Reset Out: Reset Out indicates cpu is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X1 X2	1 2	I O	X1 and X2: Are connected to a crystal, LC, or RC network to drive the internal clock generator. X, can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK	37	O	Clock: Clock output for use as a system clock. The period of CLK is twice the X1, X2 input period.
SID	5	I	Serial Input Data Line: The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
SOD	4	O	Serial Output Data Line: The output SOD is set or reset as specified by the SIM instruction.
VCC	40	I	Power: +5V supply.
GND	20	I	Ground: Reference.



TYPICAL POWER-ON RESET RC VALUES*
R1 = 75KΩ
C1 = 1μF

* Values may have to vary due to applied power supply ramp up time.

FIGURE 1. POWER-ON RESET CIRCUIT

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage ..... GND-0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 2.0mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	25.8°C/W	9.9°C/W
Braze Seal Flatpack Package	36.1°C/W	9.0°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package 1.94W
Braze Seal Flatpack Package 1.39W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage Range (VDD) ..... +4.75V to +5.25V
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... VDD -0.5V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current	IIH or IIL	VDD = 5.25V, VI = VDD or GND	1, 2, 3	-55°C, +25°C, or +125°C	-1.0	1.0	µA
High Level Output Voltage	VOH	VDD = 4.75V, IOH = -1.0mA	1, 2, 3	-55°C, +25°C, or +125°C	VDD -0.5	-	V
Low Level Output Voltage	VOL	VDD = 5.25V, IOL = 1.0mA,	1, 2, 3	-55°C, +25°C, or +125°C	-	0.5	V
Static Current	IDDSB	VDD = 5.25V, Clock Out = Hi and Low	1, 2, 3	-55°C, +25°C, or +125°C	-	500	µA
Operating Supply Current (Note 2)	IDDOP	VDD = 5.25V, f = 1MHz (Note 2)	1, 2, 3	-55°C, +25°C, or +125°C	-	5.0	mA/MHz
Functional Tests	FT	VDD = 4.75V and 5.25V, TCYC = 500ns, VOL ≤ VDD/2, VOH ≥ VDD/2	7, 8A, 8B	-55°C, +25°C, or +125°C	-	-	-

NOTES:

1. All devices guaranteed at worst case limits and over radiation.
2. Operating supply current (IDDOP) is proportional to crystal frequency.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CLK Low Time (Standard CLK Loading)	T1	9, 10, 11	-55°C, +25°C, +125°C	40	-	ns
CLK High Time (Standard CLK Loading)	T2	9, 10, 11	-55°C, +25°C, +125°C	100	-	ns
CLK Rise Time	Tr	9, 10, 11	-55°C, +25°C, +125°C	-	115	ns
CLK Fall Time	Tf	9, 10, 11	-55°C, +25°C, +125°C	-	115	ns
X1 Rising to CLK Rising	TXKR	9, 10, 11	-55°C, +25°C, +125°C	30	250	ns
X1 Rising to CLK Falling	TXKF	9, 10, 11	-55°C, +25°C, +125°C	50	275	ns
A8-15 Valid to Leading Edge of Control (Note 5)	TAC	9, 10, 11	-55°C, +25°C, +125°C	300	-	ns
A0-7 Valid to Leading Edge of Control	TACL	9, 10, 11	-55°C, +25°C, +125°C	300	-	ns
A0-15 Valid to Valid Data In	TAD	9, 10, 11	-55°C, +25°C, +125°C	875	-	ns
Address Float After Leading Edge of READ (INTA)	TAFR	9, 10, 11	-55°C, +25°C, +125°C	-	70	ns
A8-15 Valid Before Trailing Edge of ALE (Note 5)	TAL	9, 10, 11	-55°C, +25°C, +125°C	75	-	ns
A0-7 Valid Before Trailing Edge of ALE	tALL	9, 10, 11	-55°C, +25°C, +125°C	125	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
READY Valid from Address Valid	TARY	9, 10, 11	-55°C, +25°C, +125°C	250	-	ns
Address (A8-15) Valid After Control	TCA	9, 10, 11	-55°C, +25°C, +125°C	150	-	ns
Width of Control Low (RD, WR, INTA) Edge of ALE	TCC	9, 10, 11	-55°C, +25°C, +125°C	575	-	ns
Trailing Edge of Control to Leading Edge of ALE	TCL	9, 10, 11	-55°C, +25°C, +125°C	60	-	ns
Data Valid to Trailing Edge of WRITE	TDW	9, 10, 11	-55°C, +25°C, +125°C	575	-	ns
HLDA to Bus Enable	THABE	9, 10, 11	-55°C, +25°C, +125°C	-	375	ns
Bus Float After HLDA	THABF	9, 10, 11	-55°C, +25°C, +125°C	-	375	ns
HLDA Valid to Trailing Edge of CLK	THACK	9, 10, 11	-55°C, +25°C, +125°C	90	-	ns
HOLD Hold Time	THDH	9, 10, 11	-55°C, +25°C, +125°C	-	0	ns
HOLD Setup Time to Trailing Edge of CLK	THDS	9, 10, 11	-55°C, +25°C, +125°C	-	300	ns
INTR Hold Time	THINH	9, 10, 11	-55°C, +25°C, +125°C	-	0	ns
INTR, RST and TRAP Setup Time to Falling Edge of CLK	TINS	9, 10, 11	-55°C, +25°C, +125°C	-	375	ns
Address Hold Time After ALE	TLA	9, 10, 11	-55°C, +25°C, +125°C	75	-	ns
Trailing Edge of ALE to Leading Edge of Control	TLC	9, 10, 11	-55°C, +25°C, +125°C	150	-	ns
ALE Low During CLK High	TLCK	9, 10, 11	-55°C, +25°C, +125°C	125	-	ns
ALE to Valid Data During Read	TLDR	9, 10, 11	-55°C, +25°C, +125°C	675	-	ns
ALE to Valid Data During Write	TLDW	9, 10, 11	-55°C, +25°C, +125°C	-	350	ns
ALE Width	TLL	9, 10, 11	-55°C, +25°C, +125°C	200	-	ns
ALE to READY Stable	TLRY	9, 10, 11	-55°C, +25°C, +125°C	-	175	ns
Trailing Edge of READ to Re-Enabling the Address	TRAE	9, 10, 11	-55°C, +25°C, +125°C	120	-	ns
READ (or INTA) to Valid Data	TRD	9, 10, 11	-55°C, +25°C, +125°C	375	-	ns
Control Trailing Edge to Leading Edge of Next Control	TRV	9, 10, 11	-55°C, +25°C, +125°C	550	-	ns
Data Hold Time After READ INTA	TRDH	9, 10, 11	-55°C, +25°C, +125°C	-	0	ns
READY Hold Time	TRYH	9, 10, 11	-55°C, +25°C, +125°C	-	0	ns
READY Setup Time to Leading Edge of CLK	TRYS	9, 10, 11	-55°C, +25°C, +125°C	-	250	ns
Data Valid After Trailing Edge of WRITE	TWD	9, 10, 11	-55°C, +25°C, +125°C	150	-	ns
LEADING Edge of WRITE to Data Valid	TWDL	9, 10, 11	-55°C, +25°C, +125°C	-	50	ns

NOTES:

1. Output timings are measured with a purely capacitive load, CL = 150pF
2. VDD = 4.75V, VIH = 4.25V, VIL = 0.8V
3. Delay times are measured with a 1MHz clock. An algorithm is used to convert the delays into the AC timings above with a TCYC = 500ns.
4. The AC table is tested as shown above to guarantee the processor system timing.
5. A8 - A15 address specifications also apply to IO/M, S0 and S1 except A8 - A15 are undefined during T4-T6 of off cycle whereas IO/M, So, and S1 are stable.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Input Capacitance	CIN	VDD = Open, f = 1MHz	T_A = +25°C	-	12	pF
I/O Capacitance	CI/O	VDD = Open, f = 1MHz	T_A = +25°C	-	13	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz	T_A = +25°C	-	12	pF

NOTE:

1. All measurements referenced to device ground.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The post irradiation test conditions and limits are the same as those listed in Table 1 & 2

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Output Low Voltage	VOL	± 60mV
Output High Voltage	VOH	± 400mV
Input Leakage Current	IIL	± 100nA
Input Leakage Current	IIH	± 100nA
Static Current	IDDSB	±50µA

TABLE 6. INTERRUPT PRIORITY, RESTART ADDRESS, AND SENSITIVITY

NAME	PRIORITY	ADDRESS BRANCHED TO (1) WHEN INTERRUPT OCCURS	TYPE TRIGGER
TRAP	1	24H	Rising edge and high level until sampled.
RST 7.5	2	3CH	Rising edge (latched)
RST 6.5	3	34CH	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	See Note 2	High level until sampled.

NOTES:

1. The processor pushes the PC on the stack before branching to the indicated address.
2. The address branched to depends on the instruction provided to the cpu when the interrupt is acknowledged.

TABLE 5. BUS TIMING SPECIFICATION AS A t_{CYC} DEPENDENT

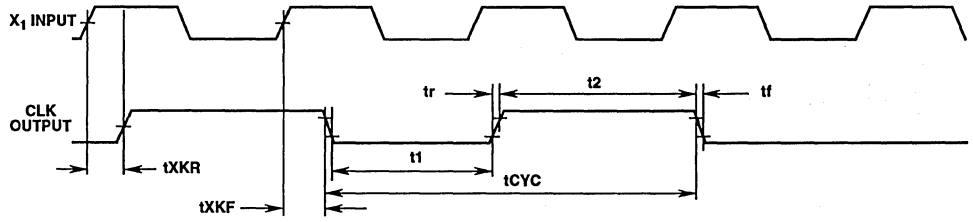
SYMBOL	HS-80C85RH	
tAL	(1/2)T- 175	Minimum
tLA	(1/2)T- 175	Minimum
tLL	(1/2)T-50	Minimum
tLCK	(1/2)T- 125	Minimum
tLC	(1/2)T- 100	Minimum
tAD	(5/2 + N)T - 375	Maximum
tRD	(3/2 + N)T - 375	Maximum
tRAE	(1/2)T- 130	Minimum
tCA	(1/2)T - 100	Minimum
tDW	(3/2 + N)T - 175	Minimum
tWD	(1/2)T-100	Minimum

SYMBOL	HS-80C85RH	
tCC	(3/2 + N)T - 175	Minimum
tCL	(1/2)T - 190	Minimum
tARY	(3/2)T - 500	Maximum
tHACK	(1/2)T - 160	Minimum
tHABF	(1/2)T +125	Maximum
tHABE	(1/2)T +125	Maximum
tAC	(2/2)T - 200	Minimum
t1	(1/2)T-210	Minimum
t2	(1/2)T- 150	Minimum
tRV	(3/2)T - 200	Minimum
tLDR	(4/2)T - 325	Maximum

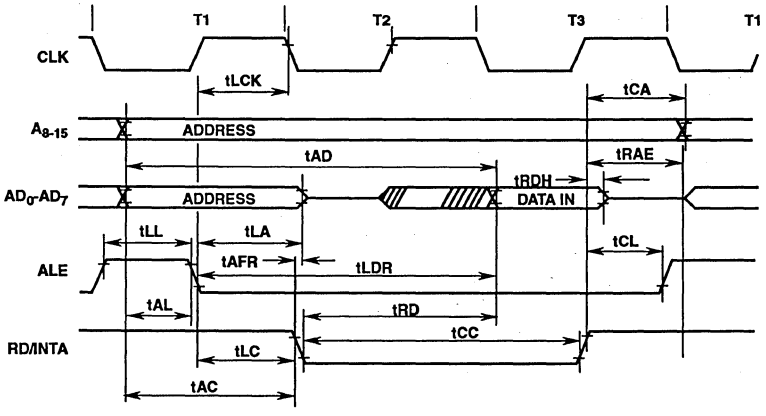
NOTE: N is equal to the total WAIT states T = tCYC

Waveforms

CLOCK

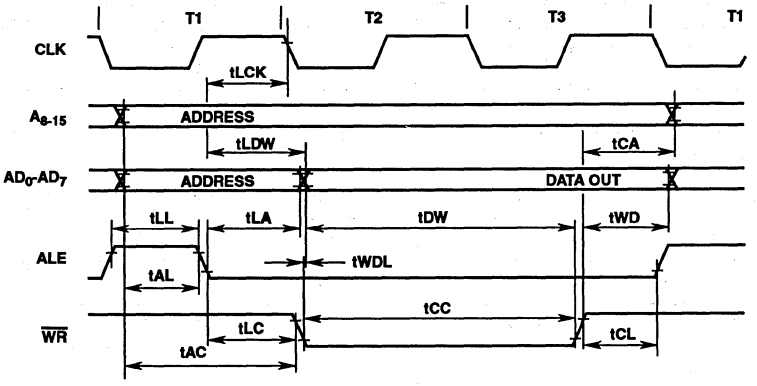


READ

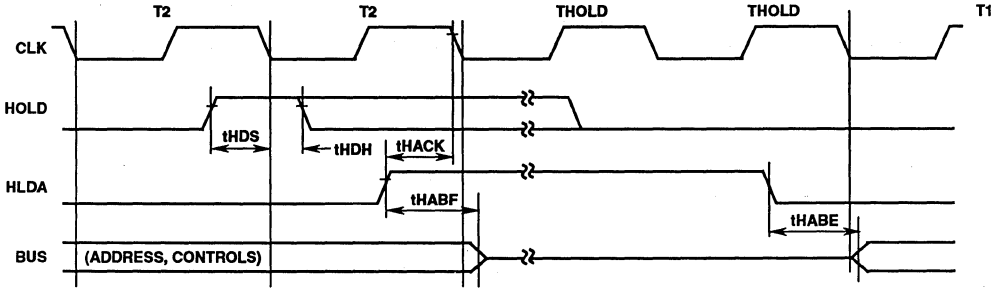


Waveforms (Continued)

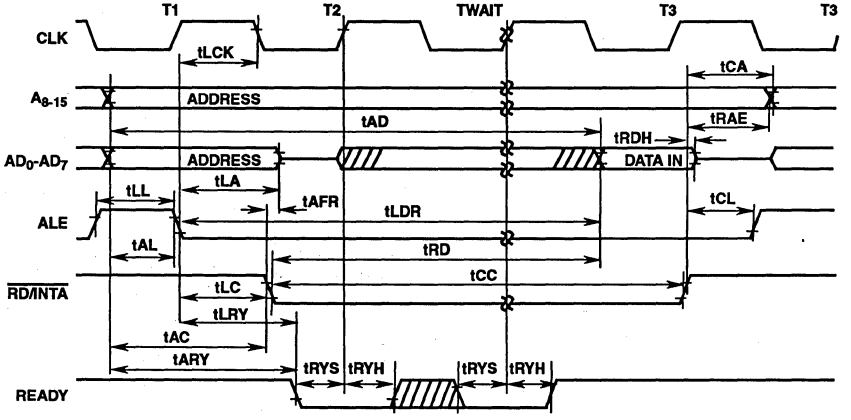
WRITE



HOLD



READ OPERATION WITH WAIT CYCLE (TYPICAL) - SAME READY TIMING APPLIES TO WRITE



NOTE 1: READY MUST REMAIN STABLE DURING SETUP AND HOLD TIMES.

Waveforms (Continued)

INTERRUPT AND HOLD

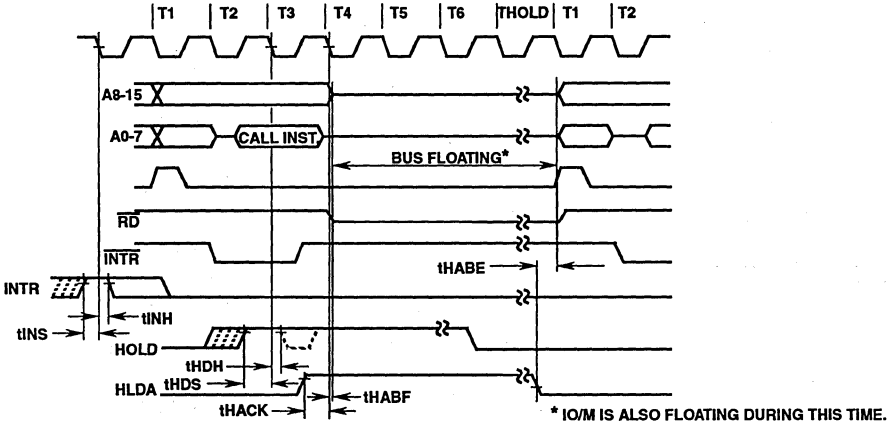


TABLE 6. INSTRUCTION SET SUMMARY

MNEMONIC	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OPERATIONS DESCRIPTION
MOVE, LOAD, AND STORE									
MOVr1, r2	0	1	D	D	D	S	S	S	Move register to register
MOV M.r	0	1	1	1	0	S	S	S	Move register to memory
MOV r.M	0	1	D	D	D	1	1	0	Move memory to register
MVI r	0	0	D	D	D	1	1	0	Move immediate register
MVI M	0	0	1	1	0	1	1	0	Move immediate memory
LXI B	0	0	0	0	0	0	0	1	Load immediate register Pair B & C
LXI D	0	0	0	1	0	0	0	1	Load immediate register Pair D & E
LXI H	0	0	1	0	0	0	0	1	Load immediate register Pair H & L
STAX B	0	0	0	0	0	0	1	0	Store A indirect
STAX D	0	0	0	1	0	0	1	0	Store A indirect
LDAX B	0	0	0	0	1	0	1	0	Load A indirect
LDAX D	0	0	0	1	1	0	1	0	Load A indirect
STA	0	0	1	1	0	0	1	0	Store A direct
LDA	0	0	1	1	1	0	1	0	Load A direct
SHLD	0	0	1	0	0	0	1	0	Store H & L direct
LHLD	0	0	1	0	1	0	1	0	Load H & L direct
XCHG	1	1	1	0	1	0	1	1	Exchange D & E, H & L Registers
STACK OPS									
PUSH B	1	1	0	0	0	1	0	1	Push register Pair B & C on stack
PUSH D	1	1	0	1	0	1	0	1	Push register Pair D & E on stack
PUSH H	1	1	1	0	0	1	0	1	Push register Pair H & L on stack
PUSH PSW	1	1	1	1	0	1	0	1	Push A and Flags on stack

MNEMONIC	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OPERATIONS DESCRIPTION
CZ	1	1	0	0	1	1	0	0	Call on zero
CNZ	1	1	0	0	0	1	0	0	Call on no zero
CP	1	1	1	1	0	1	0	0	Call on positive
CM	1	1	1	1	1	1	0	0	Call on minus
CPE	1	1	1	0	1	1	0	0	Call on parity even
CPO	1	1	1	0	0	1	0	0	Call on parity odd
RETURN									
RET	1	1	0	0	1	0	0	1	Return
RC	1	1	0	1	1	0	0	0	Return on carry
RNC	1	1	0	1	0	0	0	0	Return on no carry
RZ	1	1	0	0	1	0	0	0	Return on zero
RNZ	1	1	0	0	0	0	0	0	Return on no zero
RP	1	1	1	1	0	0	0	0	Return on positive
RM	1	1	1	1	1	0	0	0	Return on minus
RPE	1	1	1	0	1	0	0	0	Return on parity even
RPO	1	1	1	0	0	0	0	0	Return on parity odd
RESTART									
RST	1	1	A	A	A	1	1	1	Restart
INPUT/OUTPUT									
IN	1	1	0	1	1	0	1	1	Input
OUT	1	1	0	1	0	0	1	1	Output
INCREMENT AND DECREMENT									
INR r	0	0	D	D	D	1	0	0	Increment register
DCR r	0	0	D	D	D	1	0	1	Decrement register
INR M	0	0	1	1	0	1	0	0	Increment memory
DCR M	0	0	1	1	0	1	0	1	Decrement memory
INX B	0	0	0	0	0	0	1	1	Increment B & C registers
INX D	0	0	0	1	0	0	1	1	Increment D & E registers
POP B	1	1	0	0	0	0	0	1	Pop register Pair B & C off stack

MNEMONIC	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OPERATIONS DESCRIPTION
POP D	1	1	0	1	0	0	0	1	Pop register Pair D & E off stack
POP H	1	1	1	0	0	0	0	1	Popregister Pair H & L off stack
POP PSW	1	1	1	1	0	0	0	1	Pop A and Flags off stack
XTHL	1	1	1	0	0	0	1	1	Exchange top ot stack, H & L
SPHL	1	1	1	1	1	0	0	1	H & L to stack pointer
LXI SP	0	0	1	1	0	0	0	1	Load immediate stack pointer
INX SP	0	0	1	1	0	0	1	1	Increment stack pointer
DCX SP	0	0	1	1	1	0	1	1	Decrement stack pointer
JUMP									
JMP	1	1	0	0	0	0	1	1	Jump unconditional
JC	1	1	0	1	1	0	1	0	Jump on carry
JNC	1	1	0	1	0	0	1	0	Jump on no carry
JZ	1	1	0	0	1	0	1	0	Jump on zero
JNZ	1	1	0	0	0	0	1	0	Jump on no zero
JP	1	1	1	1	0	0	1	0	Jump on positive
JM	1	1	1	1	1	0	1	0	Jump on minus
JPE	1	1	1	0	1	0	1	0	Jump on parity even
JPO	1	1	1	0	0	0	1	0	Jump on parity odd
PCHL	1	1	1	0	1	0	0	1	H & L to program counter
CALL									
CALL	1	1	0	0	1	1	0	1	Call unconditional
CC	1	1	0	1	1	1	0	0	Call on carry
CNC	1	1	0	1	0	1	0	0	Call on no carry
LOGICAL									
ANA r	1	0	1	0	0	S	S	S	And register with A
XRA r	1	0	1	0	1	S	S	S	Exclusive OR register with A
ORA r	1	0	1	1	0	S	S	S	OR register with A
CMP r	1	0	1	1	1	S	S	S	Compare register with A
ANA M	1	0	1	0	0	1	1	0	And memory with A
XRA M	1	0	1	0	1	1	1	0	Exclusive OR memory with A
ORA M	1	0	1	1	0	1	1	0	OR memory with A
CMP M	1	0	1	1	1	1	1	0	Compare memory with A
ANI	1	1	1	0	0	1	1	0	And immediate with A
XRI	1	1	1	0	1	1	1	0	Exclusive OR immediate with A
ORI	1	1	1	1	0	1	1	0	OR immediate with A
CPI	1	1	1	1	1	1	1	0	Compare immediate with A
ROTATE									
RLC	0	0	0	0	0	1	1	1	Rotate A left
RRC	0	0	0	0	1	1	1	1	Rotate A right

MNEMONIC	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OPERATIONS DESCRIPTION
RAL	0	0	0	1	0	1	1	1	Rotate A left through carry
RAR	0	0	0	1	1	1	1	1	Rotate A right through carry
INX H	0	0	1	0	0	0	1	1	Increment H & L registers
DCX B	0	0	0	0	1	0	1	1	Decrement B & C
DCX D	0	0	0	1	1	0	1	1	Decrement D & E
DCX H	0	0	1	0	1	0	1	1	Decrement H & L
ADD									
ADD r	1	0	0	0	0	S	S	S	Add register to A
ADC r	1	0	0	0	1	S	S	S	Add register to A with carry
ADD M	1	0	C	0	0	1	1	0	Add memory to A
ADC M	1	0	0	0	1	1	1	0	Add memory to A with carry
ADI	1	1	0	0	0	1	1	0	Add immediate to A
ACI	1	1	0	0	1	1	1	0	Add immediate to A with carry
DAD B	0	0	0	0	1	0	0	1	Add B & C to H & L
DAD D	0	0	0	1	1	0	0	1	Add D & E to H & L
DAD H	0	0	1	0	1	0	0	1	Add H & L to H & L
DAD SP	0	0	1	1	1	0	0	1	Add stack pointer to H&L
SUBTRACT									
SUB r	1	0	0	1	0	S	S	S	Subtract register from A
SBB r	1	0	0	1	1	S	S	S	Subtract register from A with borrow
SUB M	1	0	0	1	0	1	1	0	Subtract memory from A
SBB M	1	0	0	1	1	1	1	0	Subtract memory from A with borrow
SUI	1	1	0	1	0	1	1	0	Subtract immediate from A
SBI	1	1	0	1	1	1	1	0	Subtract immediate from A with borrow
SPECIALS									
CMA	0	0	1	0	1	1	1	1	Complement A
STC	0	0	1	1	0	1	1	1	Set carry
CMC	0	0	1	1	1	1	1	1	Complement carry
DAA	0	0	1	0	0	1	1	1	Decimal adjust A
CONTROL									
EI	1	1	1	1	1	0	1	1	Enable Interrupts
DI	1	1	1	1	0	0	1	1	Disable Interrupt
NOP	0	0	0	0	0	0	0	0	No-operation
HLT	0	1	1	1	0	1	1	0	Halt
RIM	0	0	1	0	0	0	0	0	Read Interrupt Mask
SIM	0	0	1	1	0	0	0	0	Set Interrupt Mask

NOTES:

1. DDS or SSS: B000, C001, D010, E011, H100, L101, Memory 110, A111
2. Two possible cycle times (6/12) indicate instruction cycles dependent on condition flags.

Functional Description

The HS-80C85RH is a complete 8-bit parallel central processing unit implemented in a self aligned, silicon gate, CMOS technology. Its static design allows the device to be operated at any external clock frequency from a maximum of 4MHz down to DC. The processor clock can be stopped in either the high or low state and held there indefinitely. This type of operation is especially useful for system debug or power critical applications. The device is designed to fit into a minimum system of three ICs: CPU (HS-80C85RH), RAM/IO (HS-81C55/56RH) and ROM/IO Chip (HS-83C55RH).

Since the HS-80C85RH is implemented in CMOS, all of the advantages of CMOS technology are inherent in the device. These advantages include low standby and operating power, high noise immunity, moderately high speed, wide operating temperature range, and designed-in radiation hardness. Thus the HS-80C85RH is ideal for weapons and space applications.

The HS-80C85RH has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The HS-80C85RH register set is as follows:

MNEMONIC	REGISTER	CONTENTS
ACC or A	Accumulator	8 -bits
PC	Program Counter	16-bit Address
BC, DE, HL	General-Purpose Registers; Data Pointer(HL)	8-bits x 6 or 16-bits x 3
SP	Stack Pointer	16-bit Address
Flags or F	Flag Register	5 Flags (8-bit space)

The HS-80C85RH uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The HS-80C85RH provides $\overline{RD}$, $\overline{WR}$, S0, S1, and IO/$\overline{M}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{INTA}$) is also provided. HOLD and all Interrupts are synchronized with the processor's internal clock. The HS-80C85RH also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, the HS-80C85RH has three maskable, vector interrupt pins, one nonmaskable TRAP interrupt, and a bus vectored interrupt, INTR.

Interrupt and Serial I/O

The HS-80C85RH has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP INTR is maskable (can be enabled or disabled by EI or DI software instructions), and causes the CPU to fetch in an RST instruction, externally placed on the data bus, which vectors a branch to any one of eight fixed memory locations (Restart addresses). The decimal addresses of these dedicated locations are: 0, 8, 16, 24, 32, 40, 48, and 56. Any of these addresses may be used to store the first instruction(s) of a routine designed to service the requirements of an interrupting device. Since the (RST) is a call, completion of the instruction also stores the old program counter contents on the STACK. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table 6.)

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are high level-sensitive and are recognized with the same timing as INTR. RST 7.5 is rising edge sensitive.

For RST 7.5, only a pulse is required to set an internal flipflop which generates the internal interrupt request (a normally high level signal with a low going pulse is recommended for highest system noise immunity). The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a $\overline{RESET\ IN}$ to the 80C85RH. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and $\overline{RESET\ IN}$.

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP-highest priority, RST 7.5, RST 6.5, RST 5.5, INTR-lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both edge and level sensitive. The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure 2 illustrates the TRAP interrupt request circuitry within the HS-80C85RH. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

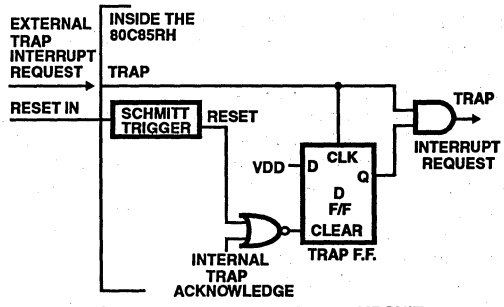


FIGURE 2. TRAP AND RESET IN CIRCUIT

The TRAP interrupt is special in that is disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR, or RST 5.5-7.5 will provide current interrupt enable status, revealing that interrupts are disabled.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

Driving the X1 and X2 Inputs

You may drive the clock inputs of the HS-80C85RH with a crystal, an LC tuned circuit, an RC network, or an external clock source. The driving frequency may be any value from DC to 4MHz and must be twice the desired internal clock frequency.

The following guidelines should be observed when a crystal is used to drive the HS-80C85RH clock input:

1. A 20pF capacitor should be connected from X2 to ground to assure oscillator start-up at the correct frequency.
2. A 10MΩ resistor is required between X1 and X2 for bias point stabilization. In addition, the crystal should have the following characteristics:
   1) Parallel resonance at twice the desired internal clock frequency
   2) CL (load capacitance) ≤ 30pF
   3) CS (shunt capacitance) ≤ 7pF
   4) RS (equivalent shunt resistance) ≤ 75Ω
   5) Drive level: 10mW
   6) Frequency tolerance: ±0.005% (suggested)

A parallel-resonant LC circuit may be used as the frequency-determining network for the HS-80C85RH, providing that its frequency tolerance of approximately ±10% is acceptable. The components are chosen from the formula:

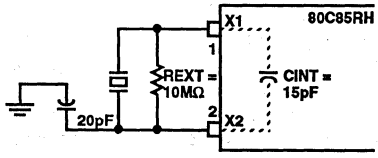
$$f = \frac{1}{2\pi\sqrt{L\,(Cext + Cint)}}$$

To minimize variations in frequency, it is recommended that you choose a value for Cext that is at least twice that of Cint, or 30pF. The use of an LC circuit is not recommended for frequencies higher than approximately 4MHz.

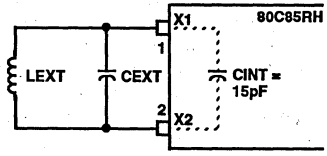
An RC circuit may be used as the frequency-determining network for the HS-80C85RH if maintaining a precise clock frequency is of no importance. Variations in the on-chip timing generation can cause a wide variation in frequency when using the RC mode. Its advantage is its low component cost. The driving frequency generated by the circuit shown is approximately 3MHz. It is not recommended that frequencies greatly higher or lower than this be attempted.

Figure 3 shows the recommended clock driver circuits.

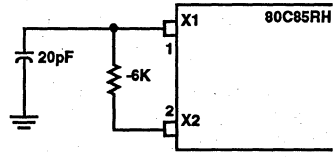
For driving frequencies up to and including 4MHz you may supply the driving signal to X1 and leave X2 open-circuited (Figure 3D).



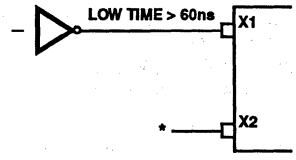
a.) QUARTZ CRYSTAL CLOCK DRIVER



b.) LC TUNED CIRCUIT CLOCK DRIVER



c.) RC CIRCUIT CLOCK DRIVER



* X2 Left Floating

d.) 0-4MHz INPUT FREQUENCY EXTERNAL CLOCK DRIVER CIRCUIT

FIGURE 3. CLOCK DRIVER CIRCUITS

HS-80C85RH Caveats

1. An important caveat that is applicable to CMOS devices in general is that unused inputs should never be left floating. This rule also applies to inputs connected to a tri- state bus. The need for external pull-up resistors during tri-state bus conditions is eliminated by the presence of regenerative latches on the following HS-80C85RH output pins: AD0-AD7, A8-A15, and IO/M. Figure 4 depicts an output and corresponding regenerative latch. When the output driver assumes the high impedance state, the latch holds the bus in whatever logic state (high or low) it was before the tri-state condition. A transient drive current of approximately ±1.0mA at 0.5 VDD for 10nsec is required to switch the latch. Thus, CMOS device inputs connected to the bus are not allowed to float during tri-state conditions.
2. The $\overline{RD}$ and $\overline{WR}$ pins of the HS-80C85RH contain internal dynamic pull-up transistors to avoid spurious selection of memory devices when the $\overline{RD}$ and $\overline{WR}$ pins assume the high impedance state. This eliminates the need for external resistive pull-ups on these pins.
3. The $\overline{RESET\ IN}$ and X1 inputs on the HS-80C85RH are schmit trigger inputs. This eliminates the possibility of internal oscillations in response to slow rise time input signals at these pins.
4. A high frequency bypass capacitor of approximately 0.1 µF should be connected between VDD and GND to shunt power supply transients.
5. The HS-80C85RH is functional within 10 input clock cycles after application of power (assuming that reset has been asserted from power-on). Start up conditions in the crystal controlled oscillator mode must also account for the characteristics of the oscillator.

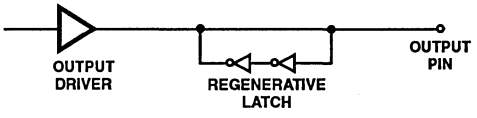


FIGURE 4. OUTPUT DRIVER AND LATCH FOR PINS ADO-AD7, A8-A15 AND IO/$\overline{M}$.

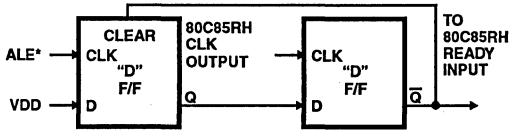
Generating An HS-80C85RH Wait State

If your system requirements are such that slow memories or peripheral devices are being used, the circuit shown in Figure 5 may be used to insert one WAIT state in each HS-80C85RH machine cycle.

The D flip-flops should be chosen so that:

1. CLK is rising edge-triggered
2. CLEAR is low-level active.

The READY line is used to extend the read and write pulse lengths so that the 80C85RH can be used with slow memory. HOLD causes the CPU to relinquish the bus when it is through with it by floating the Address and Data Buses.



* ALE and CLK (OUT) should be buffered if CLK input of latch exceeds 80C85RH IOL or IOH.

FIGURE 5. GENERATION OF A WAIT STATE FOR HS-80C85RH CPU.

System Interface

The HS-80C85RH family includes memory components, which are directly compatible to the HS-8OC8SRH CPU. For example, a system consisting of the three radiation-hardened chips, HS-80C85RH, HS-81C56RH, and HS-83C55RH will have the following features:

1. 2K Bytes ROM
2. 256 Bytes RAM
3. 1 Timer/Counter
4. 4 8-bit I/O Ports
5. 1 6-bit I/O Port
6. 4 Interrupt Levels
7. Serial In/Serial Out Ports

This minimum system, using the standard I/O technique is as shown in Figure 6.

In addition to standard 1/0, the memory mapped I/O offers an efficient I/O addressing technique. With this technique, an area of memory address space is assigned for I/O address, thereby, using the memory address for I/O manipulation. Figure 7 shows the system configuration of Memory Mapped I/O using HS-80C85RH.

The HS-80C85RH CPU can also interface with the standard radiation-hardened memory that does not have the multiplexed address/data bus. It will require use of the HS-82C12RH (8-bit latch) as shown in Figure 8.

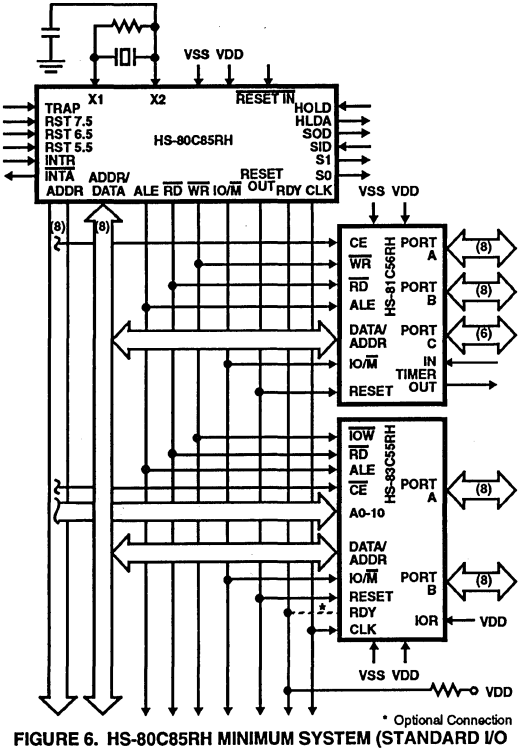


FIGURE 6. HS-80C85RH MINIMUM SYSTEM (STANDARD I/O TECHNIQUE)

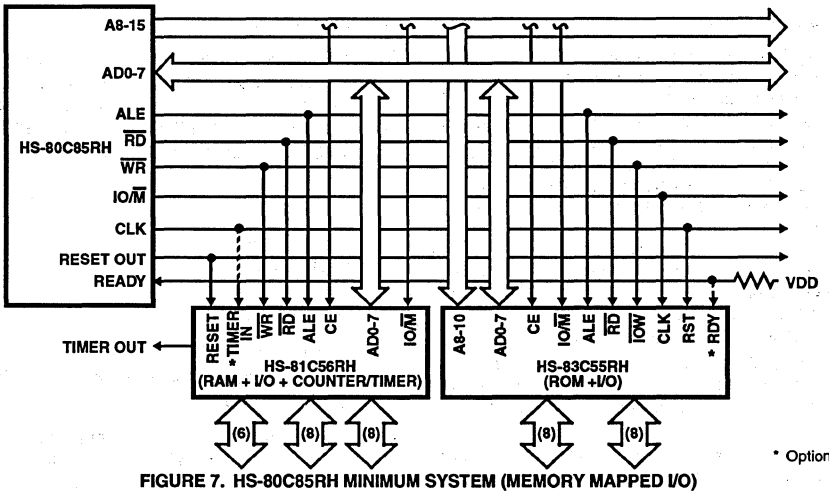


FIGURE 7. HS-80C85RH MINIMUM SYSTEM (MEMORY MAPPED I/O)

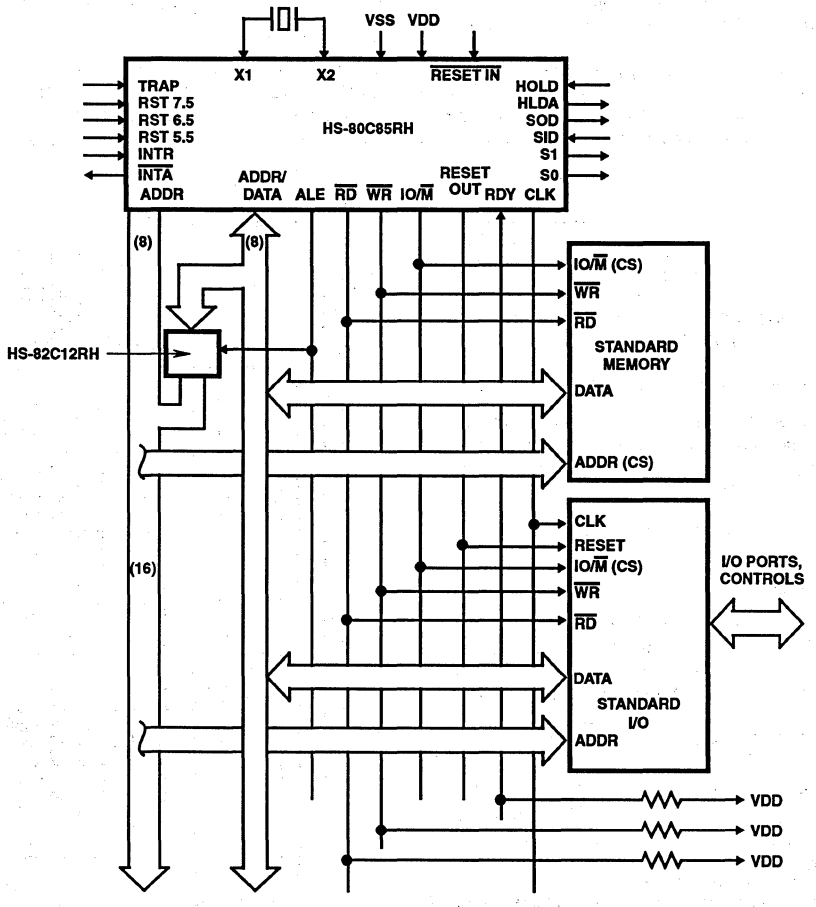


FIGURE 8. HS-80C85RH SYSTEM (USING STANDARD MEMORIES)

Basic System Timing

The HS-80C85RH has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 9 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines ($IO/\overline{M}$, S1, S0) and the three control signals ($\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$). (See Table 7.) The status lines can be used as advanced controls (for device selection, for example), since they become active at the T1 state, at the outset of each machine cycle. Control lines $\overline{RD}$ and $\overline{WR}$ are used as command lines since they become active when the transfer of data is to take place.

TABLE 7. HS-80C85RH MACHINE CYCLE CHART

MACHINE CYCLE			STATUS			CONTROL		
			$IO/\overline{M}$	S1	S0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
Opcode Fetch	(OF)		0	1	1	0	1	1
Memory Read	(MR)		0	1	0	0	1	1
Memory Write	(MW)		0	0	1	1	0	1
I/O Read	(IOR)		1	1	0	0	1	1
I/O Write	(IOW)		1	0	1	1	0	1
Acknowledge of INTR	(INA)		1	1	1	1	1	0
Bus Idle	(BI)	DAD	0	1	0	1	1	1
		Ack. of RST, TRAP	1	1	1	1	1	1
		HALT	TS	0	0	TS	TS	1

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of $\overline{READY}$ or HOLD inputs). Any T state must be one of ten possible states, shown in Table 8.

TABLE 8. HS-80C85RH MACHINE STATE CHART

MACHINE STATE	STATUS & BUSES				CONTROL		
	S1, S0	$IO/\overline{M}$	A8-15	AD0-7	$\overline{RD}$,$\overline{WR}$	$\overline{INTA}$	ALE
T1	X	X	X	X	1	1	1*
T2	X	X	X	X	X	X	0
TWAIT	X	X	X	X	X	X	0
T3	X	X	X	X	X	X	0
T4	1	0**	X	TS	1	1	0
T5	1	0**	X	TS	1	1	0
T6	1	0**	X	TS	1	1	0
TRESET	X	TS	TS	TS	TS	1	0
THALT	0	TS	TS	TS	TS	1	0
THOLD	X	TS	TS	TS	TS	1	0

0 = Logic "0" TS = High Impedance
1 = Logic "1" X = Unspecified

* ALE not generated during 2nd and 3rd machine cycles of DAD instruction.

* * IO/M = 1 during T4, T6 of INA machine cycle.

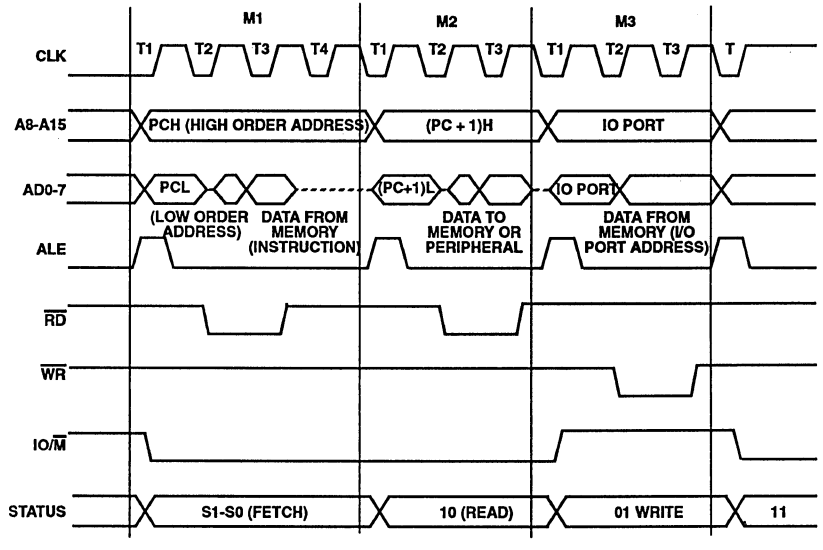
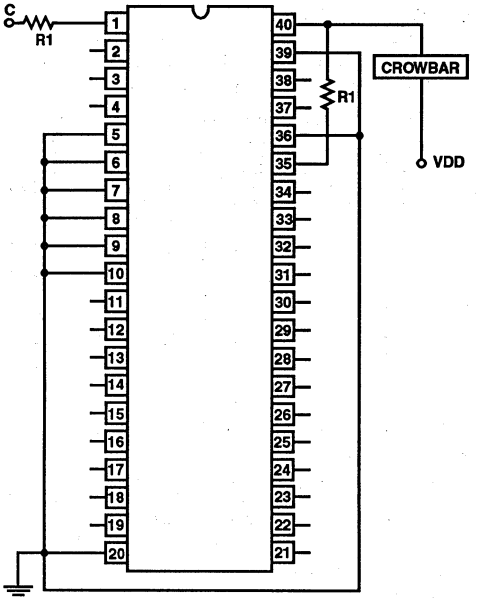


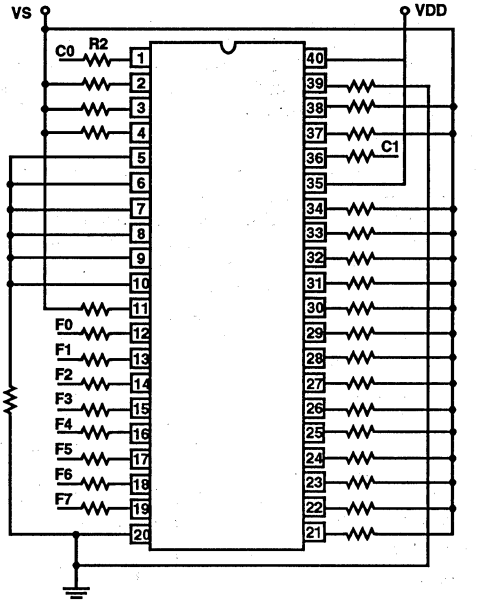
FIGURE 9. 80C85RH BASIC SYSTEM TIMING

Burn-In Circuits

HS-80C85RH 40 PIN DIP

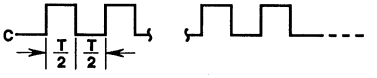


HS-80C85RH 40 PIN DIP



STATIC

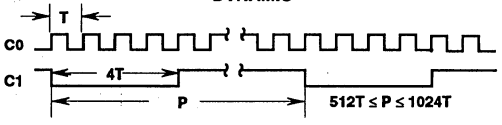
MINIMUM OF 10 PULSES



NOTES:

VDD = 10V ± 10%
R1 = 1K
T > 200ns
C must be pulsed a minimum of 10 times.
After initial pulses, C should be left low.

DYNAMIC

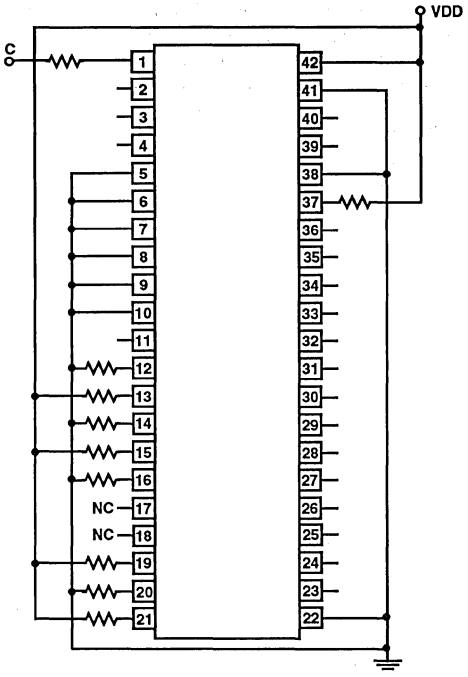


NOTES:

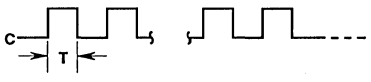
VDD = 10V ± 5%
VS = 5V ± 10%
R2 = 10KΩ
All other resistors 100KΩ
T = 5µs
CO = 200KHz
F0 thru F7 have 50% duty cycles.
F0 = 50kHz, F1 = F0/2, F2 = F1/2 . . . F7 = F6/2

Burn-In Circuits (Continued)

HS-80C85RH 42 LEAD FLATPACK



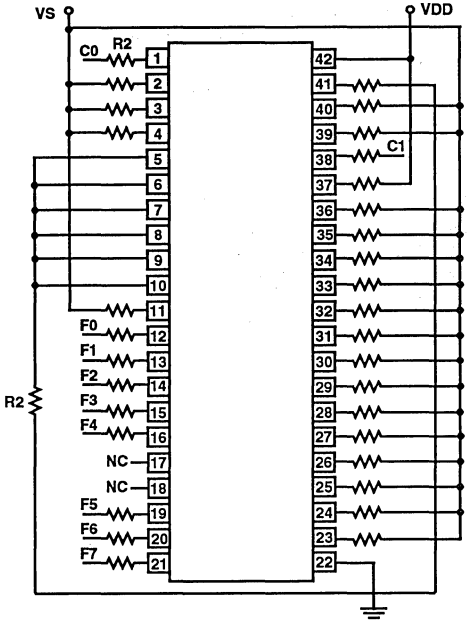
STATIC



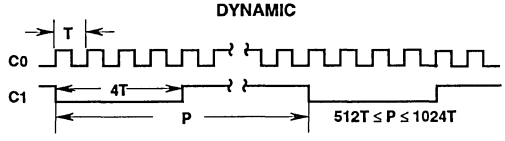
NOTES:

VDD = 10V ± 5%
All resistors are 10KΩ
T > 200ns
C must be pulsed a minimum of 10 times.
After initial pulses, C is grounded.

HS-80C85RH 42 LEAD FLATPACK



DYNAMIC



NOTES:

VDD = 10V ± 5%
VS = 5V ± 5%
R1 = 100KΩ
R2 = 10KΩ
R3 = 5.1KΩ (Pins 12-16, 19-21)
CO = 200KHz 50% duty cycle square wave
C1 used to periodically reset processor
T = 5µs
F0 thru F7 have 50% duty cycles.
F0 = 50kHz, F1 = F0/2, F2 = F1/2 . . . F7 = F6/2

Radiation Screening Procedure

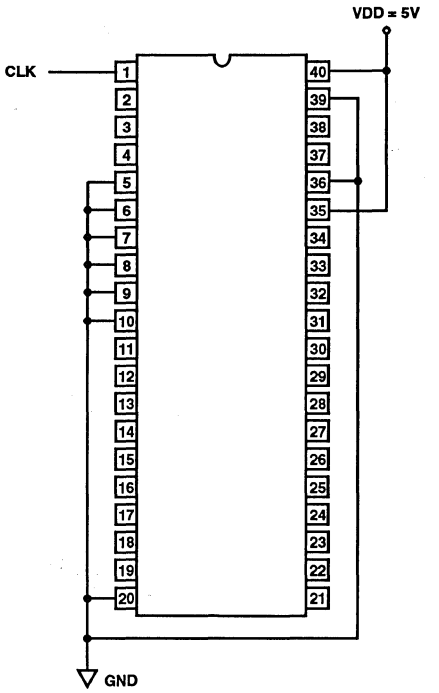
1. A random sample of two dice per wafer is drawn from the wafer lot. Wafer identity is retained.
2. The sample die shall be assembled and tested for functionality in a ceramic DIP.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad(Si) +10% from a Gammacell 220 cobalt 60 source or equivalent. The devices will be powered with VSUPPLY = +5V. The dose rate shall be between 50 rads/sec and 300 rads/sec.
4. The Irradiation Circuit is shown below.
5. The sample devices shall be started into test within 1 hour of irradiation and have completed test within 2 hours of irradiation. The wafers are accepted only if the sample, exclusive of non-radiation failures, meets all electrical specifications at room temperature.
6. Radiation screening to a higher total dose is available. Customers should contact their closest Harris Representative for details.

Radiation Effects

The HS-80C85RH has been designed to survive in a radiation environment and to meet the electrical characteristics. Latch-up free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained with special low temperature processing cycles. On a production basis, Harris performs screens for total dose hardness to a level of 1 x 10^5 Rad-Si. Transient radiation tests have shown the following results:

1. Latch-up free to doses ≥ 1 x 10^{12} rads/sec.
2. Upset (loss of stored data ≥ 1 x 10^8 rads/sec.

Irradiation Circuit



Harris - Space Level Product Flow -Q (Note 1)

SEM - Traceable to Diffusion Method 2018

Wafer Lot Acceptance Method 5007

Internal Visual Inspection Method 2010, Condition A

Gamma Radiation Assurance Tests Method 1019

Nondestructive Bond Pull Method 2023

Customer Pre-Cap Visual Inspection (Note 2)

Temperature Cycling Method 1010, Condition C

Constant Acceleration Method 2001, Condition E Min, Y1

Particle Impact Noise Detection Method 2020, Condition A

Electrical Tests Harris' Option

Serialization

X-Ray Inspection Method 2012

Electrical Tests Subgroup 1; Read and Record (TO)

Static Burn-In Method 1015, Condition B, 72 Hours, +125°C Minimum

Electrical Tests Subgroup 1; Read and Record (T1)

Burn-In Delta Calculation (T0-T1)

PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ

Dynamic Burn-In Method 1015 Condition D, 240 Hours, +125°C (Note 3)

Electrical Tests Subgroup 1; Read and Record (T2)

Alternate Group A Subgroups 1, 7, 9; Method 5005; Para 3.5.1.1

Burn-In Delta Calculation (TO-T2)

PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ

Electrical Test Subgroup 3; Read and Record

Alternate Group A Subgroups 3, 8B, 11; Method 5005; Para 3.5.1.1

Marking

Electrical Tests Subgroup 2; Read and Record

Alternate Group A Subgroups 2, 8A, 10; Method 5005; Para 3.5.1.1

Gross Leak Method 1014, 100%

Fine Leak Method 1014, 100%

Customer Source Inspection (Note 2)

Group B Inspection Method 5005 (Note 2)
End-Point Electrical Parameters:
B-5/ Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11

B-6; Subgroups 1, 7, 9

Group D Inspection Method 5005 (Notes 2, 4)
End-Point Electrical Parameters: Subgroups 1, 7, 9

External Visual Inspection Method 2009

Data Package Generation (Note 5)

NOTES:

1. The notes of Method 5004, Table 1 Shall apply; unless otherwise specified.
2. These steps are optional and should be listed on the individual purchase order(s), when required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table 1 of Method 1015
4. For group D, subgroup 3 inspection of package configurations which utilize a gold plated lid in its construction; the inspection criteria for illegible markings criteria of Method 1010, paragraph 3.3 and of Method 1004, paragraph 3.8.a shall not apply.
5. Data package contains:
   Assembly attributes (Post Seal)
   Test attributes (includes Group A)
   Shippable serial number list
   Radiation testing certificate of conformance
   Wafer lot acceptance report (including SEM report)
   X-ray report and film
   Test variables data

Metallization Topology

DIE DIMENSIONS:
229 x 240 x 14 ± 1mils

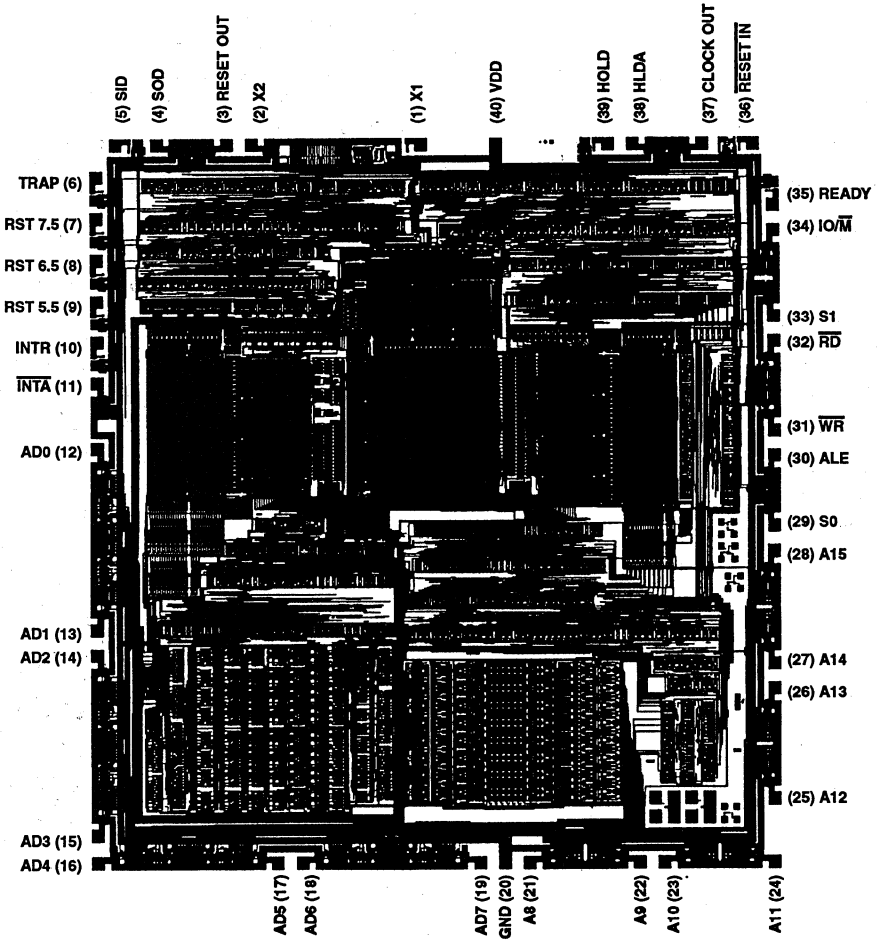
METALLIZATION:
Type: SiAl
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP + Flatpack - 460°C (Max)

Metallization Mask Layout

HS-80C85RH



HARRIS SEMICONDUCTOR

HS-80C86RH

Radiation Hardened 16-Bit CMOS Microprocessor

December 1992

Features

- Radiation Hardened
  - Latch Up Free EPI-CMOS
  - Total Dose >100K RAD(Si)
  - Transient Upset > 10^8 RAD(Si)/sec
  - Functional after Total Dose 1 x 10^6 RAD(Si)
- Low Power Operation
  - ICCSB = 500µA Maximum
  - ICCOP = 12mA/MHz Maximum
- Pin Compatible with NMOS 8086 and Harris 80C86
- Completely Static Design DC to 5MHz
- 1 Mbyte of Direct Memory Addressing Capability
- 24 Operand Addressing Modes
- Bit, Byte, Word, and Block Move Operations
- 8 and 16 Bit Signed/Unsigned Arithmetic
  - Binary or Decimal
  - Multiply and Divide
- Bus-hold Circuitry Eliminates Pull-up Resistors for CMOS Designs
- Hardened Field, Self Aligned, Junction Isolated CMOS Process
- Single 5V Power Supply
- Military Temperature Range -35°C to + 125°C

Description

The Harris HS-80C86RH high performance radiation hardened 16 bit CMOS CPU is manufactured using a hardened field, self aligned silicon gate CMOS process. Two modes of operation, MINimum for small systems and MAXimum for larger applications such as multi-processing, allow user configuration to achieve the highest performance level. Industry standard operation allows use of existing NMOS 8086 hardware and software designs.

Pinouts

HS-80C86RH 40 LEAD BRAZE SEAL DIP
COMPLIANT OUTLINE D5, CONFIGURATION 3
TOP VIEW

		MAX		MIN
GND	1	40	VDD	
AD14	2	39	AD15	
AD13	3	38	AD16/S3	
AD12	4	37	A17/S4	
AD11	5	36	A18/S5	
AD10	6	35	A19/S6	
AD9	7	34	$\overline{BHE}$/S7	
AD8	8	33	MN/$\overline{MX}$	
AD7	9	32	$\overline{RD}$	
AD6	10	31	$\overline{RQ}$/$\overline{GT0}$	(HOLD)
AD5	11	30	$\overline{RQ}$/$\overline{GT1}$	(HLDA)
AD4	12	29	$\overline{LOCK}$	($\overline{WR}$)
AD3	13	28	$\overline{S2}$	(M/$\overline{IO}$)
AD2	14	27	$\overline{S1}$	(DT/$\overline{R}$)
AD1	15	26	$\overline{S0}$	($\overline{DEN}$)
AD0	16	25	QS0	(ALE)
NMI	17	24	QS1	($\overline{INTA}$)
INTR	18	23	$\overline{TEST}$	
CLK	19	22	READY	
GND	20	21	RESET	

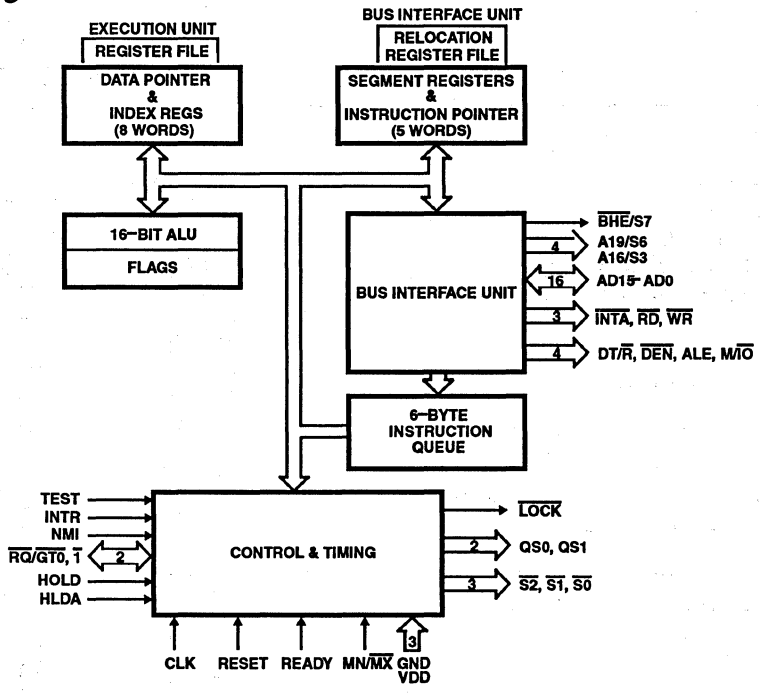
HS-80C86RH 42 LEAD BRAZE SEAL FLATPACK
HARRIS PACKAGE CODE HWN
TOP VIEW

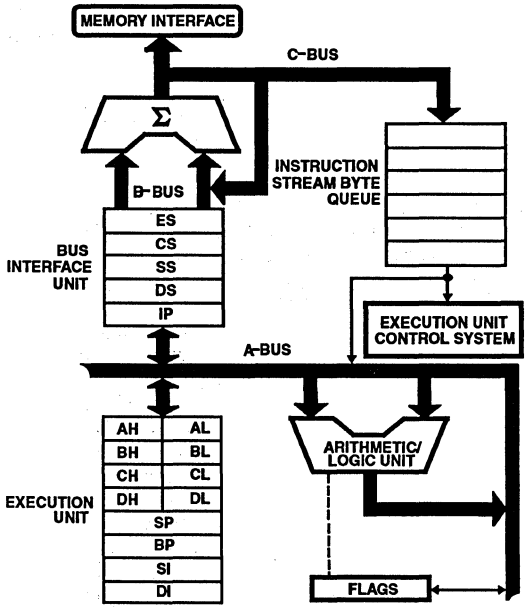
		MAX		MIN
GND	1	42	VDD	
AD14	2	41	AD15	
AD13	3	40	NC	
AD12	4	39	A16/S3	
AD11	5	38	A17/S4	
AD10	6	37	A18/S5	
AD9	7	36	A19/S6	
AD8	8	35	$\overline{BHE}$/S7	
AD7	9	34	MN/$\overline{MX}$	
AD6	10	33	$\overline{RD}$	
AD5	11	32	$\overline{RQ}$/$\overline{GT0}$	(HOLD)
AD4	12	31	$\overline{RQ}$/$\overline{GT1}$	(HLDA)
AD3	13	30	$\overline{LOCK}$	($\overline{WR}$)
AD2	14	29	$\overline{S2}$	(M/$\overline{IO}$)
AD1	15	28	$\overline{S1}$	(DT/$\overline{R}$)
AD0	16	27	$\overline{S0}$	($\overline{DEN}$)
NC	17	26	QS0	(ALE)
NMI	18	25	QS1	($\overline{INTA}$)
INTR	19	24	$\overline{TEST}$	
CLK	20	23	READY	
GND	21	22	RESET	

10 µPROCESSORS

File Number 3035

Functional Diagram





Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
The following pin function descriptions are for HS-80C86RH systems in either minimum or maximum mode. The "Local Bus" in these descriptions is the direct multiplexed bus interface connection to the HS-80C86RH (without regard to additional bus buffers).			
AD15-AD0	2-16, 39	I/O	ADDRESS DATA BUS: These lines constitute the time multiplexed memory/IO address (T1) and data (T2, T3, TW, T4) bus. AO is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D7-D0. It is LOW during T1 when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use AD0 to condition chip select functions (See $\overline{BHE}$). These lines are active HIGH and are held at high impedance to the last valid logic level during interrupt acknowledge and local bus "hold acknowledge" or "grant sequence".
A19/S6 A18/S5 A17/S4 A16/S3	35-38	O	ADDRESS/STATUS: During T1, these are the four most significant address lines for memory operations. During I/O operations these lines are low. During memory and I/O operations, status information is available on these lines during T2, T3, TW, T4. S6 is always zero. The status of the interrupt enable FLAG bit (S5) is updated at the beginning of each CLK cycle. S4 and S3 are encoded. This information indicates which segment register is presently being used for data accessing. These lines are held at high impedance to the last valid logic level during local bus "hold acknowledge" or "grant sequence". **S4 S3** 0 0 Extra Data 0 1 Stack 1 0 Code or None 1 1 Data
$\overline{BHE}$/S7	34	O	BUS HIGH ENABLE/STATUS: During T1 the bus high enable signal ($\overline{BHE}$) should be used to enable data onto the most significant half of the data bus, pins D15-D8. Eight bit oriented devices tied to the upper half of the bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is LOW during T1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. The S7 status information is available during T2, T3 and T4. The signal is active LOW, and is held at high impedance to the last valid logic level during interrupt acknowledge and local bus "hold acknowledge" or "grant sequence"; it is LOW during T1 for the first interrupt acknowledge cycle. **$\overline{BHE}$ A0** 0 0 Whole Word 0 1 Upper Byte from/to Odd Address 1 0 Lower Byte from/to Even Address 1 1 None
$\overline{RD}$	32	O	READ: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the M/$\overline{IO}$ or $\overline{S2}$ pin. This signal is used to read devices which reside on the HS-80C86RH local bus. $\overline{RD}$ is active LOW during T2, T3 and TW of any read cycle, and is guaranteed to remain HIGH in T2 until the 80C86 local bus has floated. This line is held at a high impedance logic one state during "hold acknowledge" or "grant sequence".
READY	22	I	READY: is the acknowledgment from the addressed memory or I/O device that will complete the data transfer. The RDY signal from memory or I/O is synchronized by the HS-82C85RH Clock Generator to form READY. This signal is active HIGH. The HS-80C86RH READY input is not synchronized. Correct operation is not guaranteed if the Setup and Hold Times are not met.
INTR	18	I	INTERRUPT REQUEST: is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. If so, an interrupt service routine is called via an interrupt vector lookup table located in system memory. INTR is internally synchronized and can be internally masked by software resetting the interrupt enable bit. This signal is active HIGH.
$\overline{TEST}$	23	I	TEST: input is examined by the "Wait" instruction. If the $\overline{TEST}$ input is LOW execution continues, otherwise the processor waits in an "Idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
NMI	17	I	NON-MASKABLE INTERRUPT: is an edge triggered input which causes a type 2 interrupt. An interrupt service routine is called via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.

Pin Description (Continued)

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
RESET	21	I	RESET: causes the processor to immediately terminate its present activity. The signal must change from LOW to HIGH and remain active HIGH for at least four clock cycles. It restarts execution, as described in the Instruction Set description, when RESET returns LOW. RESET is internally synchronized.
CLK	19	I	CLOCK: provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
VDD	40		VDD: +5V power supply pin. A 0.1µF capacitor between pins 20 and 40 is recommended for decoupling.
GND	1, 20		GND: Ground. Note: both must be connected. A 0.1µF capacitor between pins 1 and 20 is recommended for decoupling.
MN/$\overline{MX}$	33	I	MINIMUM/MAXIMUM: Indicates what mode the processor is to operate in. The two modes are discussed in the following sections.
The following pin function descriptions are for the HS-80C86RH system in maximum mode (i.e., MN/$\overline{MX}$ = GND). Only the pin functions which are unique to maximum mode are described below.			
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	26-28	O	STATUS: is active during T4, T1 and T2 and is returned to the passive state (1,1,1) during T3 or during TW when READY is HIGH. This status is used by the 82C88 Bus Controller to generate all memory and I/O access control signals. Any change by $\overline{S2}$, $\overline{S1}$, or $\overline{S0}$ during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 or TW is used to indicate the end of a bus cycle. These status lines are encoded. These signals are held at a high impedance logic one state during "grant sequence". $\overline{S2}$ $\overline{S1}$ $\overline{S0}$ 0 0 0 Interrupt Acknowledge 0 0 1 Read I/O Port 0 1 0 Write I/O Port 0 1 1 Halt 1 0 0 Code Access 1 0 1 Read Memory 1 1 0 Write Memory 1 1 1 Passive
$\overline{RQ}/\overline{GT0}$ $\overline{RQ}/\overline{GT1}$	31, 30	I/O	REQUEST/GRANT: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bi-directional with $\overline{RQ}/\overline{GT0}$ having higher priority than $\overline{RQ}/\overline{GT1}$. $\overline{RQ}/\overline{GT}$ has an internal pull-up bus hold device so it may be left unconnected. The request/grant sequence is as follows (see $\overline{RQ}/\overline{GT}$ Sequence Timing) 1. A pulse of 1 CLK wide from another local bus master indicates a local bus request ("hold") to the HS-80C86RH (pulse 1). 2. During a T4 or T1 clock cycle, a pulse 1 CLK wide from the HS-80C86RH to the requesting master (pulse 2) indicates that the HS-80C86RH has allowed the local bus to float and that it will enter the "grant sequence" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "grant sequence". 3. A pulse 1 CLK wide from the requesting master indicates to the HS-80C86RH (pulse 3) that the "hold" request is about to end and that the HS-80C86RH can reclaim the local bus at the next CLK. The CPU then enters T4 (or T1 if no bus cycles pending). Each Master-Master exchange of the local bus is a sequence of 3 pulses. There must be one idle CLK cycle after each bus exchange. Pulses are active low. If the request is made while the CPU is performing a memory cycle, it will release the local bus during T4 of the cycle when all the following conditions are met: 1. Request occurs on or before T2. 2. Current cycle is not the low byte of a word (on an odd address). 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently executing. If the local bus is idle when the request is made the two possible events will follow: 1. Local bus will be released during the next cycle. 2. A memory cycle will start within three clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.

Pin Description (Continued)

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
$\overline{LOCK}$	29	O	LOCK: output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and is held at a HIGH impedance logic one state during "grant sequence". In MAX mode, $\overline{LOCK}$ is automatically generated during T2 of the first $\overline{INTA}$ cycle and removed during T2 of the second $\overline{INTA}$ cycle.
QS1, QS0	24, 25	O	QUEUE STATUS: The queue status is valid during the CLK cycle after which the queue operation is performed. QS1 and QS2 provide status to allow external tracking of the internal HS-80C86RH instruction queue. Note that QS1, QS0 never become high impedance. **QS1 QS0** 0 0 No Operation 0 1 First Byte of Opcode from Queue 1 0 Empty the Queue 1 1 Subsequent Byte from Queue
The following pin function descriptions are for the HS-80C86RH in minimum mode (i.e. MN/$\overline{MX}$ = VDD). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described below.			
M/$\overline{IO}$	28	O	STATUS LINE: logically equivalent to $\overline{S2}$ in the maximum mode. It is used to distinguish a memory access from an I/O access. M/$\overline{IO}$ becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (M = HIGH, IO = LOW). M/$\overline{IO}$ is held to a high impedance logic zero during local bus "hold acknowledge".
$\overline{WR}$	29	O	WRITE: indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/$\overline{IO}$ signal. $\overline{WR}$ is active for T2, T3 and TW of any write cycle. It is active LOW, and is held to high impedance logic one during local bus "hold acknowledge".
$\overline{INTA}$	24	O	INTERRUPT ACKNOWLEDGE: is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T2, T3 and TW of each interrupt acknowledge cycle. Note that $\overline{INTA}$ is never floated.
ALE	25	O	ADDRESS LATCH ENABLE: is provided by the processor to latch the address into the 82C82 latch. It is a HIGH pulse active during clock LOW of TI of any bus cycle. Note that ALE is never floated.
DT/$\overline{R}$	27	O	DATA TRANSMIT/RECEIVE: is needed in a minimum system that desires to use a data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/$\overline{R}$ is equivalent to $\overline{S1}$ in maximum mode, and its timing is the same as for M/$\overline{IO}$ (T = HIGH, R = LOW). DT/$\overline{R}$ is held to a high impedance logic one during local bus "hold acknowledge".
$\overline{DEN}$	26	O	DATA ENABLE: provided as an output enable fora bus transceiver in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access and for $\overline{INTA}$ cycles. For a read or $\overline{INTA}$ cycle it is active from the middle of T2 until the middle of T4, while for a write cycle it is active from the beginning of T2 until the middle of T4. $\overline{DEN}$ is held to a high impedance logic one during local bus "hold acknowledge".
HOLD HLDA	31 30	I O	HOLD: indicates that another master is requesting a local bus "hold". To be a acknowledged, HOLD must be active HIGH. The processor receiving the "hold" will issue a "hold acknowledge" (HLDA) in the middle of a T4 or T1 clock cycle. Simultaneously with the issuance of HLDA, the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will lower HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage
Applied for all Grades ..... VSS-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 12mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	24.2°C/W	8.6°C/W
Braze Seal Flatpack Package	72.1°C/W	9.7°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package 2.05W
Braze Seal Flatpack Package 0.69W
Gate Count ..... 9750 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage Range (VDD) ..... +4.5V to +5.5V
Operating Temperature Range (T_A) ..... -35°C to +125°C
Input Low Voltage (VIL) ..... 0V to +0.8V
Input High Voltage (VIH) ..... 3.5V to VDD
Clock Input Low Voltage (VILC) ..... 0.0V to 0.8V
Clock Input High Voltage (VIHC) ..... VDD - 0.8V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
TTL High Level Output Voltage	VOH1	VDD = 4.5V, IO = -2.5mA VIN = 0V or 4.5V	1, 2, 3	-35°C, +25°C, +125°C	3.0	-	V
CMOS High Level Output Voltage	VOH2	VDD = 4.5V, IO = -100µA VIN = 0V or 4.5V	1, 2, 3	-35°C, +25°C, +125°C	VDD - 0.4V	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, IO = +2.5mA VIN = 0V or 4.5V	1, 2, 3	-35°C, +25°C, +125°C	-	0.4	V
Input Leakage Current	IIH or IIL	VDD = 5.5V VIN = 0V or 5.5V Pins: 17-19, 21-23, 33	1, 2, 3	-35°C, +25°C, +125°C	-1.0	1.0	µA
Output Leakage Current	IOZL or IOZH	VDD = 5.5V VIN = 0V or 5.5V Pins: 2-16, 26-29, 32, 34-39	1, 2, 3	-35°C, +25°C, +125°C	-10	10	µA
Input Current Bus Hold High	IBHH	VDD = 4.5V and 5.5V VIN = 3.0V (Note 1) Pins: 2-16, 26-32, 34-39	1, 2, 3	-35°C, +25°C, +125°C	-600	-40	µA
Input Current Bus Hold Low	IBHL	VDD = 4.5V and 5.5V VIN = 0.8V (Note 2) Pins: 2-16, 34-39	1, 2, 3	-35°C, +25°C, +125°C	40	600	µA
Standby Power Supply Current	IDDSB	VDD = 5.5V, VIN = GND or VDD, IO = 0mA (Note 3)	1, 2, 3	-35°C, +25°C, +125°C	-	500	µA
Operating Power Supply Current	IDDOP	VDD = 5.5V, VIN = GND or VDD, IO = 0mA, f = 1MHz	1, 2, 3	-35°C, +25°C, +125°C	-	12	mA/MHz
Functional Tests	FT	VDD = 4.5V and 5.5V, VIN = GND or VDD, f = 1MHz	7, 8A, 8B	-35°C, +25°C, +125°C	-	-	-
Noise Immunity Functional Tests	FN	VDD = 4.5V and 5.5V, VIN = GND or 3.5V and VDD = 4.5V, VIN = 0.8V or VDD	7, 8A, 8B	-35°C, +25°C, +125°C	-	-	-

NOTES:

1. IBHH should be measured after raising VIN to VDD and then lowering to 3.0V.
2. IBHL should be measured after lowering VIN to VSS and then raising to 0.8V.
3. IDDSB tested during Clock high time after halt instruction executed.

TABLE 2a. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (MIN MODE)

AC's tested at worst case VDD, AC's guaranteed over full operating specifications.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
CLK Cycle Period	TCLCL	VDD = 4.5V VDD = 5.5V	9, 10, 11	-35°C, +25°C, +125°C	200	-	ns
CLK Low Time	TCLCH	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	118	-	ns
CLK High Time	TCHCL	VDD = 4.5V VDD = 5.5V	9, 10, 11	-35°C, +25°C, +125°C	69	-	ns
Data in Setup Time	TDVCL	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	30	-	ns
Data in Hold Time	TCLDX1	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	10	-	ns
Ready Setup Time into 80C86RH	TRYHCH	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	118	-	ns
Ready Hold Time into 80C86RH	TCHRYX	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	30	-	ns
Ready Inactive to CLK (Note 2)	TRYLCL	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	-8	-	ns
Hold Setup Time	THVCH	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	35	-	ns
INTR, NMI, Test/Setup Time	TINVCH	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	30	-	ns
MIN MODE TIMING RESPONSES (CL = 100pF)							
Address Valid Delay	TCLAV	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	10	110	ns
ALE Width	TLHLL	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	TCLCH - 20	-	ns
ALE Active Delay	TCLLH	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	-	80	ns
ALE Inactive Delay	TCHLL	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	-	85	ns
Address Hold Time to ALE Inactive	TLLAX	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	TCHCL - 10	-	ns
Control Active Delay 1	TCVCTV	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	10	110	ns
Control Active Delay 2	TCHCTV	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	10	110	ns
Control Inactive Delay	TCVCTX	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	10	110	ns
$\overline{RD}$ Active Delay	TCLRL	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	10	165	ns
$\overline{RD}$ Inactive Delay	TCLRH	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	10	150	ns
$\overline{RD}$ Inactive to Next Address Active	TRHAV	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	TCLCL - 45	-	ns
HLDA Valid Delay	TCLHAV	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	10	160	ns

TABLE 2a. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (MIN MODE) (Continued)

AC's tested at worst case VDD, AC's guaranteed over full operating specifications.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
$\overline{RD}$ Width	TRLRH	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	2TCLCL - 75	-	ns
$\overline{WR}$ Width	TWLWH	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	2TCLCL - 60	-	ns
Address Valid to ALE Low	TAVLL	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	TCLCH - 60	-	ns
Output Rise Time	TOLOH	VDD = 4.5V From 0.8V to 2.0V	9, 10, 11	-35°C, +25°C, +125°C	-	20	ns
Output Fall Time	TOHOL	VDD = 4.5V From 2.0V to 0.8V	9, 10, 11	-35°C, +25°C, +125°C	-	20	ns

NOTES:

1. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
2. Applies only to T2 State (8ns into T3).

TABLE 2b. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (MAX MODE)

AC's tested at worst case VDD, AC's guaranteed over full operating specifications.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
TIMING REQUIREMENTS							
CLK Cycle Period	TCLCL	VDD = 4.5V VDD = 5.5V	9, 10, 11	-35°C, +25°C, +125°C	200	-	ns
CLK Low Time	TCLCH	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	118	-	ns
CLK High Time	TCHCL	VDD = 4.5V VDD = 5.5V	9, 10, 11	-35°C, +25°C, +125°C	69	-	ns
Data in Setup Time	TDVCL	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	30	-	ns
Data in Hold Time	TCLDX1	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	10	-	ns
Ready Setup Time into 80C86RH	TRYHCH	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	118	-	ns
Ready Hold Time into 80C86RH	TCHRYX	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	30	-	ns
Ready Inactive to CLK (Note 2)	TRYLCL	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	-8	-	ns
INTR, NMI, Test/Setup Time	TINVCH	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	30	-	ns
$\overline{RQ}/\overline{GT}$ Setup Time	TGVCH	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	30	-	ns
$\overline{RQ}$ Hold Time into HS-80C86RH (Note 3)	TCHGX	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	40	TCHCL + 10	ns
MAX MODE TIMING RESPONSES (CL = 100pF)							
Ready Active to Status Passive (Notes 2 and 4)	TRYHSH	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	-	110	ns

TABLE 2b. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (MAX MODE) (Continued)

AC's tested at worst case VDD, AC's guaranteed over full operating specifications.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Status Active Delay	TCHSV	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	10	110	ns
Status Inactive Delay (Note 4)	TCLSH	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	10	130	ns
Address Valid Delay	TCLAV	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	10	110	ns
$\overline{RD}$ Active Delay	TCLRL	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	10	165	ns
$\overline{RD}$ Inactive Delay	TCLRH	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	10	150	ns
$\overline{RD}$ Inactive to Next Address Active	TRHAV	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	TCLCL - 45	-	ns
$\overline{GT}$ Active Delay	TCLGL	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	0	85	ns
$\overline{GT}$ Inactive Delay	TCLGH	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	0	85	ns
$\overline{RD}$ Width	TRLRH	VDD = 4.5V	9, 10, 11	-35°C, +25°C, +125°C	2TCLCL - 75	-	ns
Output Rise Time	TOLOH	VDD = 4.5V From 0.8V to 2.0V	9, 10, 11	-35°C, +25°C, +125°C	-	20	ns
Output Fall Time	TOHOL	VDD = 4.5V From 2.0V to 0.8V	9, 10, 11	-35°C, +25°C, +125°C	-	20	ns

NOTES:

1. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
2. Applies only to T2 State (8ns into T3).
3. The HS-80C86RH actively pulls the RQ/GT pin to a logic one on the following clock low time.
4. Status lines return to their inactive (logic one) state after CLK goes low and READY goes high.

TABLE 3a. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz (Note 1)	T_A = +25°C	-	15	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz (Note 1)	T_A = +25°C	-	15	pF
I/O Capacitance	CI/O	VDD = Open, f = 1MHz (Note 1)	T_A = +25°C	-	20	pF
TIMING REQUIREMENTS						
CLK Rise Time	TCH1CH2	VDD = 4.5V and 5.5V Min and Max Mode from 1.0V to 3.5V	-35°C < T_A < +125°C	-	15	ns
CLK Fall Time	TCL2CL1	VDD = 4.5V and 5.5V Min and Max Mode from 3.5V to 1.0V	-35°C < T_A < +125°C	-	15	ns

TABLE 3a. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Rise Time	TILIH	VDD = 4.5V and 5.5V Min and Max Mode from 0.8V to 2.0V	-35°C < T_A < +125°C	-	25	ns
Input Fall Time	TIHIL	VDD = 4.5V and 5.5V Min and Max Mode from 2.0V to 0.8V	-35°C < T_A < +125°C	-	25	ns
TIMING RESPONSES						
Address Hold Time	TCLAX	VDD = 4.5V and 5.5V Min and Max Mode	-35°C < T_A < +125°C	10	-	ns
Address Float Delay (Note 2)	TCLAZ	VDD = 4.5V and 5.5V Min and Max Mode	-35°C < T_A < +125°C	TCLAX	80	ns
Data Valid Delay	TCLDV	VDD = 4.5V and 5.5V Min and Max Mode	-35°C < T_A < +125°C	10	110	ns
Data Hold Time	TCLDX2	VDD = 4.5V and 5.5V Min and Max Mode	-35°C < T_A < +125°C	10	-	ns
Data Hold Time After WR	TWHDX	VDD = 4.5V and 5.5V Min Mode	-35°C < T_A < +125°C	TCLCL - 30	-	ns
Status Float Delay (Note 2)	TCHSZ	VDD = 4.5V and 5.5V Max Mode	-35°C < T_A < +125°C	-	80	ns
Address Float to Read Active (Note 2)	TAZRL	VDD = 4.5V and 5.5V Min and Max Mode	-35°C < T_A < +125°C	0	-	ns

NOTES:

1. All measurements referenced to device ground.
2. Output drivers disabled. Bus hold circuitry still active.
3. The parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 3b. ELECTRICAL PERFORMANCE CHARACTERISTICS

Timing Signals at HS-82C85RH or 82C88 for Reference Only.

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
RDY Setup Time into HS-82C85RH (Note 1)	TR1VCL	Min and Max Mode	-35°C < T_A < +125°C	35	-	ns
RDY Hold Time into HS-82C85RH (Note 1)	TCLR1X	Min and Max Mode	-35°C < T_A < +125°C	0	-	ns
Command Active Delay	TCLML	Max Mode Only	-35°C < T_A < +125°C	5	35	ns
Command Inactive	TCLMH	Max Mode Only	-35°C < T_A < +125°C	5	35	ns
Status Valid to ALE High	TSVLH	Max Mode Only	-35°C < T_A < +125°C	-	20	ns
Status Valid to MCE High	TSVMCH	Max Mode Only	-35°C < T_A < +125°C	-	30	ns
CLK Low to ALE Valid	TCLLH	Max Mode Only	-35°C < T_A < +125°C	-	20	ns
CLK Low to MCE High	TCLMCH	Max Mode Only	-35°C < T_A < +125°C	-	25	ns
ALE Inactive Delay	TCHLL	Max Mode Only	-35°C < T_A < +125°C	4	18	ns
MCE Inactive Delay	TCLMCL	Max Mode Only	-35°C < T_A < +125°C	-	15	ns
Control Active Delay	TCVNV	Max Mode Only	-35°C < T_A < +125°C	5	45	ns
Control Inactive Delay	TCVNX	Max Mode Only	-35°C < T_A < +125°C	10	45	ns

NOTE:

1. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: See 25°C limits in Table 1 and Table 2 for Post RAD limits (Subgroups 1, 7 and 9).

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Standby Power Supply Current	IDDSB	±100µA
Output Leakage Current	IOZL, IOZH	±2µA
Input Leakage Current	IIH, IIL	±200nA
Low Level Output Voltage	VOL	±80mV
TTL High Level Output Voltage	VOH1	±600mV
CMOS High Level Output Voltage	VOH2	±150mV

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9
Interim Test		100%/5004	1, 7, 9	N/A
PDA		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A
	Others	Samples/5005	1, 7	N/A
Group C		Samples/5005	N/A	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group D, Others		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7, 9	1, 7, 9

Functional Description

Static Operation

All HS-80C86RH circuitry is of static design. Internal registers, counters and latches are static and require no refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction placed on other microprocessors. The CMOS HS-80C86RH can operate from DC to 5MHs. The processor clock may be stopped in either state (HIGH/LOW) and held there indefinitely. This type of operation is especially useful for system debug or power critical applications.

The HS-80C86RH can be single stepped using only the CPU clock. This state can be maintained as long as is necessary. Single step clock operation allows simple interface circuitry to provide critical information for bringing up your system.

Static design also allows very low frequency operation (down to DC). In a power critical situation, this can provide extremely low power operation since HS-80C86RH power dissipation is directly related to operating frequency. As the system frequency is reduced, so is the operating power until, ultimately, at a DC input frequency, the HS-80C86RH power requirement is the standby current, (500µA maximum).

Internal Architecture

The internal functions of the HS-80C86RH processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the CPU functional diagram.

These units can interact directly but for the most part perform as separate asynchronous operational processors. The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocation. This unit also provides the basic bus control. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utilization. Up to 6 bytes of the instruction stream can be queued while waiting for decoding and execution.

The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 2 bytes in the queue, the BIU will attempt a word fetch memory cycle. This greatly reduces "dead-time" on the memory bus. The queue acts as a First-In-First-Out (FIFO) buffer, from which the EU extracts instruction bytes as required. If the queue is empty (following a branch instruction, for example), the first byte into the queue immediately becomes available to the EU.

The execution unit receives pre-fetched instructions from the BIU queue and provides un-relocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage.

Memory Organization

The processor provides a 20-bit address to memory, which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra and stack segments of up to 64K bytes each, with each segment falling on 16-byte boundaries. (See Figure 1).

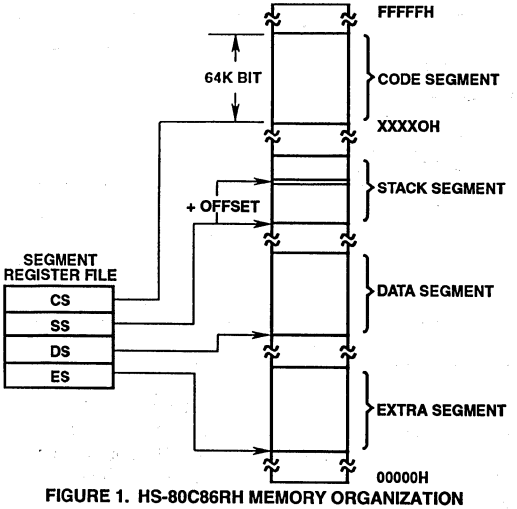


FIGURE 1. HS-80C86RH MEMORY ORGANIZATION

TABLE 7.

TYPE OF MEMORY REFERENCE	DEFAULT SEGMENT BASE	ALTERNATE SEGMENT BASE	OFFSET
Instruction Fetch	CS	None	IP
Stack Operation	SS	None	SP
Variable (except following)	DS	CS, ES, SS	Effective Address
String Source	DS	CS, ES, SS	SI
String Destination	ES	None	DI
BP Used as Base Register	SS	CS, DS, ES	Effective Address

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to the specific rules of Table 7. All information in one segment type share the same logical attributes (e.g. code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster and more structured. (See Table 7).

Word (16-bit) operands can be located on even or odd address boundaries and are thus not constrained to even boundaries as is the case in many 16-bit computers. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU automatically performs the proper number of memory accesses, one if the word operand is on an even byte boundary and two if it is on an odd byte boundary. Except for the performance penalty, this double access is transparent to the software. The performance penalty does not occur for instruction fetches; only word operands.

Physically, the memory is organized as a high bank (D15-D6) and a low bank (D7-D0) of 512K bytes addressed in parallel by the processor's address lines.

Byte data with even addresses is transferred on the D7-D0 bus lines while odd addressed byte data (A0 HIGH) is transferred on the D15-D6 bus lines. The processor provides two enable signals, $\overline{BHE}$ and A0, to selectively allow reading from or writing into either an odd byte location, even byte location, or both. The instruction stream is fetched from memory as words and is addressed internally by the processor at the byte level as necessary.

In referencing word data, the BIU requires one or two memory cycles depending on whether the starting byte of the word is on an even or odd address, respectively. Consequently, in referencing word operands performance can be optimized by locating data on even address boundaries. This is an especially useful technique for using the stack, since odd address references to the stack may adversely affect the context switching time for interrupt processing or task multiplexing.

Certain locations in memory are reserved for specific CPU operations (See Figure 2). Locations from address FFFF0H through FFFFFH are reserved for operations including a jump to the initial program loading routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be located. Locations 00000H through 003FFH are reserved for interrupt operations. Each of the 256 possible interrupt service routines is accessed through its own pair of 16-bit pointers - segment address pointer and offset address pointer. The first pointer, used as the offset address, is loaded into the 1P and the second pointer, which designates the base address is loaded into the CS. At this point program control is transferred to the interrupt routine. The pointer elements are assumed to have been stored at the respective places in reserved memory prior to occurrence of interrupts.

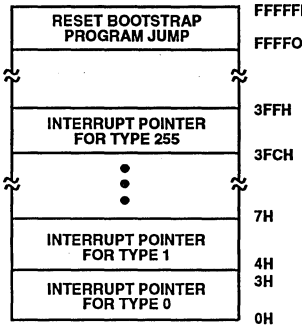


FIGURE 2. RESERVED MEMORY LOCATIONS

Minimum and Maximum Operation Modes

The requirements for supporting minimum and maximum HS-80C86RH systems are sufficiently different that they cannot be met efficiently using 40 uniquely defined pins. Consequently, the HS-80C86RH is equipped with a strap pin (MN/$\overline{MX}$) which defines the system configuration. The definition of a certain subset of the pins changes, dependent on the condition of the strap pin. When the MN/$\overline{MX}$ pin is strapped to GND, the HS-80C86RH defines pins 24 through 31 and 34 in maximum mode. When the MN/$\overline{MX}$ pin is strapped to VDD, the HS-80C86RH generates bus control signals itself on pins 24 through 31 and 34.

Bus Operation

The HS-80C86RH has a combined address and data bus commonly referred to as a time multiplexed bus. This technique provides the most efficient use of pins on the processor while permitting the use of a standard 40-lead package. This "local bus" can be buffered directly and used throughout the system with address latching provided on memory and I/O modules. In addition, the bus can also be demultiplexed at the processor with a single set of 82C82 latches if a standard non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T1 , T2, T3 and T4 (see Figure 3). The address is emitted from the processor during T1 and data transfer occurs on the bus during T3 and T4. T2 is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "Wait" states (TW) are inserted between T3 and T4. Each inserted wait state is the same duration as a CLK cycle. Idle periods occur between HS-80C86RH driven bus cycles whenever the processor performs internal processing.

During T1 of any bus cycle, the ALE (Address Latch Enable) signal is emitted (by either the processor or the 82C88 bus controller, depending on the MN/$\overline{MX}$ strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$ are used by the bus controller, in maximum mode, to identify the type of bus transaction according to Table 8.

TABLE 8.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	CHARACTERISTICS
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Status bits S3 through S7 are time multiplexed with high order address bits and the $\overline{BHE}$ signal, and are therefore valid during T2 through T4. S3 and S4 indicate which segment register (see Instruction Set Description) was used for this bus cycle in forming the address, according to Table 9.

TABLE 9.

S4	S3	CHARACTERISTICS
0 (Low)	0	Alternate Data (extra segment)
0	1	Stack
1 (High)	0	Code or None
1	1	Data

S5 is a reflection of the PSW interrupt enable bit. S6 is always zero and S7 is a spare status bit.

I/O Addressing

In the HS-80C86RH, I/O operations can address up to a maximum of 64K I/O byte registers or 32K I/O word registers. The I/O address appears in the same format as the memory address on bus lines A15-A0. The address lines A19-A16 are zero in I/O operations. The variable I/O instructions which use register DX as a pointer have full address capability while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space.

I/O ports are addressed in the same manner as memory locations. Even addressed bytes are transferred on the D7-D0 bus lines and odd addressed bytes on D15-D8. Care must be taken to ensure that each register within an 8-bit peripheral located on the lower portion of the bus be addressed as even.

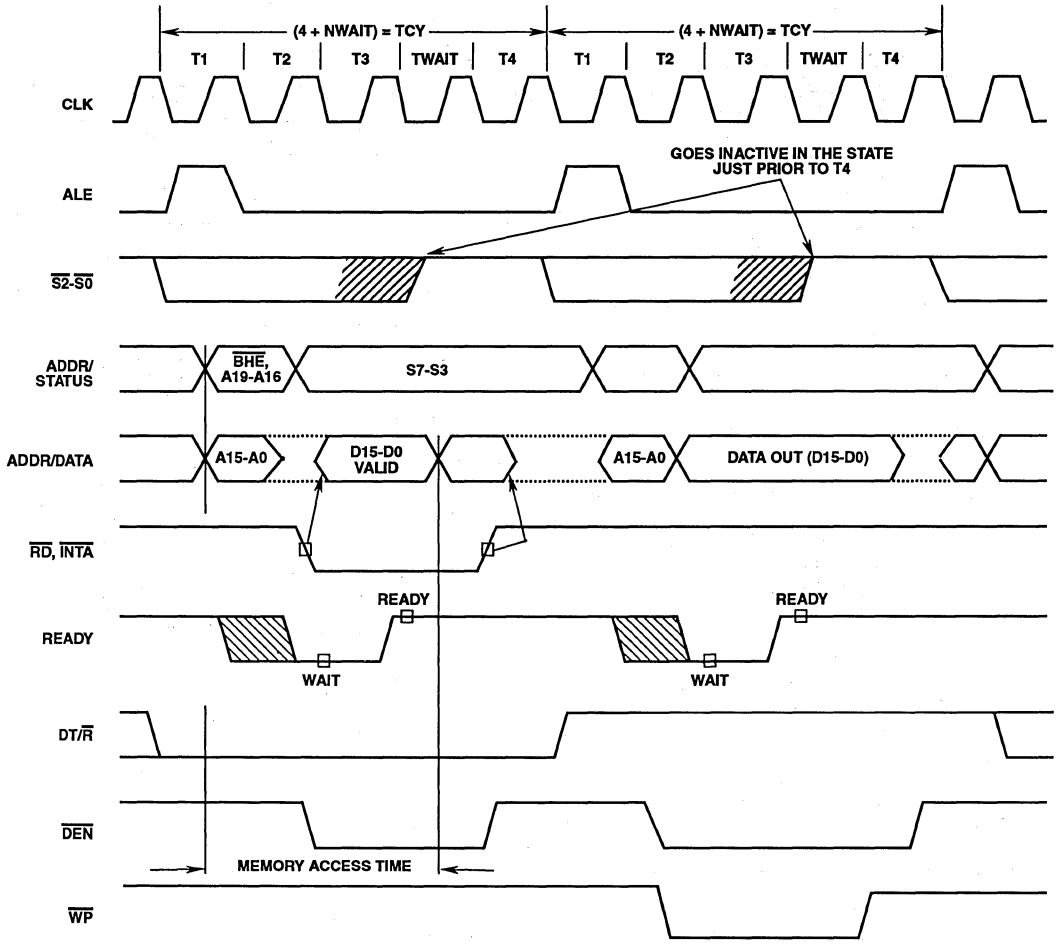


FIGURE 3. BASIC SYSTEM TIMING

External Interface

Processor RESET and Initialization

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The HS-80C86RH RESET is required to be HIGH for greater than 4 CLK cycles. The HS-80C86RH will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence for approximately 7 clock cycles. After this interval, the HS-80C86RH operates normally beginning with the instruction in absolute location FFFFOH. (See Figure 2). The RESET input is internally synchronized to the processor clock. At initialization, the HIGH-to-LOW transition of RESET must occur no sooner than 50µs (or 4 CLK cycles, whichever is greater) after power-up, to allow complete initialization of the HS-80C86RH.

NMI will not be recognized prior to the second CLK cycle following the end of RESET. If NMI is asserted sooner than nine clock cycles after the end of RESET, the processor may execute one instruction before responding to the interrupt.

Bus Hold Circuitry

To avoid high current conditions caused by floating inputs to CMOS devices and to eliminate need for pull- up/down resistors, "bus-hold" circuitry has been used on the HS-80C86RH pins 2-16,26-32 and 34-39. (See Figure 4A and 4B). These circuits will maintain the last valid logic state if no driving source is present (i.e. an unconnected pin or a driving source which goes to a high impedance state). To overdrive the "bus hold" circuits, an external driver must be capable of supplying approximately 400µA minimum sink or source current at valid input voltage levels. Since this "bus hold" circuitry is active and not a "resistive" type element, the associated power supply current is negligible and power dissipation is significantly reduced when compared to the use of passive pull-up resistors.

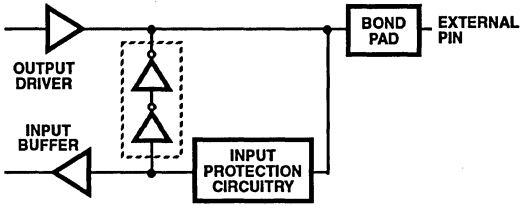


FIGURE 4A. BUS HOLD CIRCUITRY PIN 2-16, 34-39

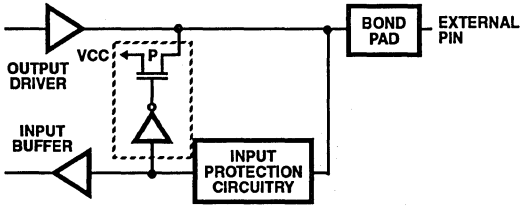


FIGURE 4B. BUS HOLD CIRCUITRY PIN 26-32

Interrupt Operations

Interrupt operations fall into two classes: software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the Instruction Set Description. Hardware interrupts can be classified as non-maskable or maskable.

Interrupts result in a transfer of control to a new program location. A 256-element table containing address pointers to the interrupt service routine locations resides in absolute locations 0 through 3FFH, which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt "type". An interrupting device supplies an 8-bit type number during the interrupt acknowledge sequence, which is used to "vector" through the appropriate element to the interrupt service routine location. All flags and both the Code Segment and Instruction Pointer register are saved as part of the $\overline{\text{INTA}}$ sequence. These are restored upon execution of an Interrupt Return (IRET) instruction.

Non-Maskable Interrupt (NMI)

The processor provides a single non-maskable interrupt pin (NMI) which has higher priority than the maskable interrupt request pin (INTR). A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW-to-HIGH transition. The activation of this pin causes a type 2 interrupt.

NMI is required to have a duration in the HIGH state of greater than two CLK cycles, but is not required to be synchronized to the clock. Any positive transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves of a block-type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during or after the servicing of NMI. Another positive edge triggers another response if it occurs after the start of the NMI procedure. The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

Maskable Interrupt (INTR)

The HS-80C86RH provides a single interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable flag (IF) status bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK. To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block- type instruction. INTR may be removed anytime after the falling edge of the first $\overline{\text{INTA}}$ signal. During the interrupt response sequence further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt or single-step), although the FLAGS register which is automatically pushed onto the stack reflects the state of the processor prior to the interrupt. Until the old FLAGS register is restored the enable bit will be zero unless specifically set by an instruction.

During the response sequence (Figure 5) the processor executes two successive (back-to-back) interrupt acknowledge cycles. The HS-80C86RH emits the $\overline{LOCK}$ signal (Max mode only) from T2 of the first bus cycle until T2 of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle, a byte is supplied to the HS-80C86RH by the HS-82C89ARH Interrupt Controller, which identifies the source (type) of the interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector look-up table. An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. The INTERRUPT RETURN instruction includes a FLAGS pop which returns the status of the original interrupt enable bit when it restores the FLAGS.

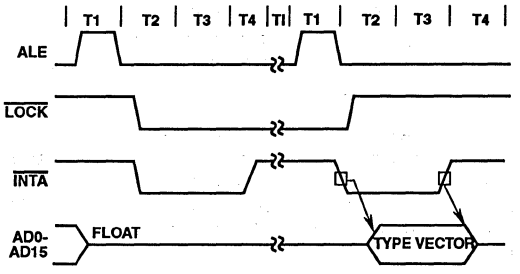


FIGURE 5. INTERRUPT ACKNOWLEDGE SEQUENCE

Halt

When a software "HALT" instruction is executed the pro- cessor indicates that it is entering the "HALT" state in one of two ways depending upon which mode is strapped. In minimum mode, the processor issues one ALE with no qualifying bus control signals. In maximum mode the processor issues appropriate HALT status on $\overline{S2}$, $\overline{S1}$, $\overline{S0}$ and the 82C88 bus controller issues one ALE. The HS-80C86RH will not leave the "HALT" state when a local bus "hold" is entered while in "HALT". In this case, the processor reissues the HALT indicator at the end of the local bus hold. An NMI or interrupt request (when interrupts enabled) or RESET will force the HS-80C86RH out of the "HALT" state.

Read/Modify/Write (Semaphore)

Operations Via Lock

The $\overline{LOCK}$ status information is provided by the processor when consecutive bus cycles are required during the execution of an instruction. This gives the processor the capability of performing read/modify/write operations on memory (via the Exchange Register With Memory instruction, for example) without another system bus master receiving intervening memory cycles. This is useful in multiprocessor system configurations to accomplish "test and set lock" operations. The $\overline{LOCK}$ signal is activated (forced LOW) in the clock cycle following decoding of the software "LOCK" prefix instruction. It is deactivated at the end of the last bus cycle of the instruction following the "LOCK" prefix instruction. While $\overline{LOCK}$ is active a request on a $\overline{RQ/GT}$ pin will be recorded and then honored at the end of the $\overline{LOCK}$.

External Synchronization Via TEST

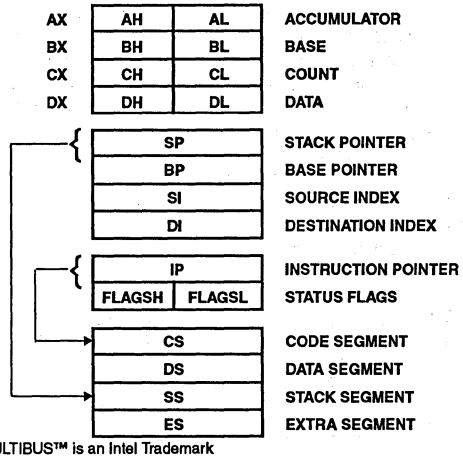
As an alternative to interrupts, the HS-80C86RH provides a single software-testable input pin ($\overline{TEST}$). This input is utilized by executing a WAIT instruction. The single WAIT instruction is repeatedly executed until the $\overline{TEST}$ input goes active (LOW). The execution of WAIT does not consume bus cycles once the queue is full.

If a local bus request occurs during WAIT execution, the HS-80C86RH three-states all output drivers while inputs and I/O pins are held at valid logic levels by internal bus-hold circuits. If interrupts are enabled, the HS-80C86RH will recognize interrupts and process them when it regains control of the bus. The WAIT instruction is then refetched, and reexecuted.

Basic System Timing

Typical system configurations for the processor operating in minimum mode and in maximum mode are shown in Figures 6A and 6B, respectively. In minimum mode, the MN/$\overline{MX}$ pin is strapped to VDD and the processor emits bus control signals (e.g. $\overline{RD}$, $\overline{WR}$, etc.) directly. In maximum mode, the MN/$\overline{MX}$ pin is strapped to GND and the processor emits coded status information which the 82C88 bus controller used to generate MULTIBUS™ compatible bus control signals. Figure 3 shows the signal timing relationships.

TABLE 10. HS-80C86RH REGISTER MODEL



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System Timing - Minimum System

The read cycle begins in T1 with the assertion of the Address Latch Enable (ALE) signal. The trailing (low-going) edge of this signal is used to latch the address information, which is valid on the address/data bus (AD0-AD15) at this time, into the 82C82 latches. The $\overline{BHE}$ and A0 signals address the low, high or both bytes. From T1 to T4 the M/IO signal indicates a memory or I/O operation. At T2, the address is removed from the address/data bus and the bus is held at the last valid logic state by internal bus hold devices. The read control signal is also asserted at T2. The read ($\overline{RD}$) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later, valid data will be available on the bus and the addressed device will

drive the READY line HIGH. When the processor returns the read signal to a HIGH level, the addressed device will three-state its bus drivers. If a transceiver is required to buffer the HS-80C86RH local bus, signals DT/R and DEN are provided by the HS-80C86RH.

A write cycle also begins with the assertion of ALE and the emission of the address. The M/IO signal is again asserted to indicate a memory or I/O write operation. In T2, immediately following the address emission, the processor emits the data to be written into the addressed location. This data remains valid until at least the middle of T4. During T2, T3 and TW, the processor asserts the write control signal.The write ($\overline{WR}$) signal becomes active at the beginning of T2 as opposed to the read which is delayed somewhat into T2 to provide time for output drivers to become inactive.

The BHE and A0 signals are used to select the proper byte(s) of the memory/IO word to be read or written according to Table 11.

TABLE 11.

BHE	A0	CHARACTERISTICS
0	0	Whole word
0	1	Upper byte from/to odd address
1	0	Lower byte from/to even address
1	1	None

I/O ports are addressed in the same manner as memory location. Even addressed bytes are transferred on the D7-D0 bus lines and odd address bytes on D15-D6.

The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge signal ($\overline{INTA}$) is asserted in place of the read ($\overline{RD}$) signal and the address bus is held at the last valid logic state by internal bus hold devices. (See Figure 4). In the second of two successive $\overline{INTA}$ cycles a byte of information is read from the data bus (D7-D0) as supplied by the interrupt system logic (i.e. HS-82CS9ARH Priority Interrupt Controller). This byte identifies the source (type) of the interrupt. It is multiplied by four and used as a pointer into an interrupt vector lookup table, as described earlier.

Bus Timing - Medium and Large Size Systems

For medium complexity systems the MN/$\overline{MX}$ pin is connected to GND and the 82C88 Bus Controller is added to the system as well as three 82C82 latches for latching the system address, and a transceiver to allow for bus loading greater than the HS-80C86RH is capable of handling. Bus control signals are generated by the 82C88 instead of the processor in this configuration, although their timing remains relatively the same. The HS-80C86RH status outputs ($\overline{S2}$, $\overline{S1}$, and $\overline{S0}$) provide type-of-cycle information and become 82C88 inputs. This bus cycle information specifies read (code, data or I/O), write (data or I/O), interrupt acknowledge, or software halt. The 82C88 issues control signals specifying memory read or write, I/O read or write, or interrupt acknowledge. The 82C88 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing as read strobes, and hence, data is not valid at the leading edge of write. The transceiver receives the usual T and 0E inputs from the 82C88 DT/$\overline{R}$ and DEN signals.

For large multiple processor systems, the 82C89 bus arbiter must be added to the system to provide system bus management. In this case, the pointer into the interrupt vector table, which is passed during the second $\overline{INTA}$ cycle, can be derived from an HS-82C59ARH located on either the local bus or the system bus. The processor's $\overline{INTA}$ output should drive the SYSB/$\overline{RESB}$ input of the 82C89 to the proper state when reading the interrupt vector number from the HS-82C59ARH during the interrupt acknowledge sequence and software "poll".

A Note on Radiation Hardened Product Availability

There are no immediate plans to develop the 82C88 Bus Controller or the 82C89 Arbiter as radiation hardened integrated circuits in packaged form. However for systems requiring these circuits, they are available as sort coded LSI macros in the Harris HSC-RH radiation hardened Standard Cell.

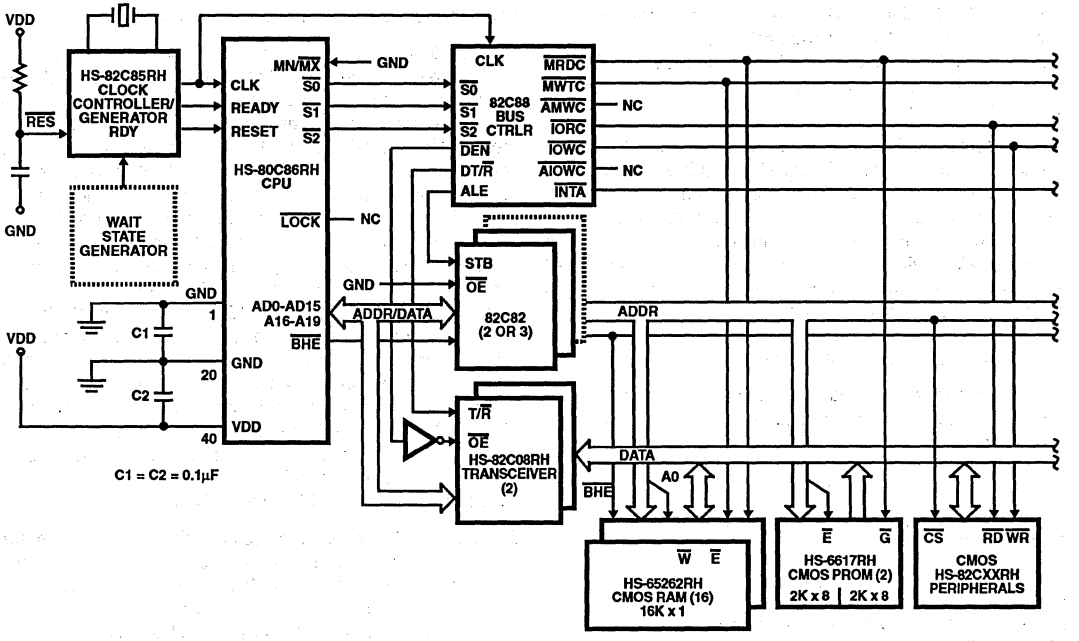


FIGURE 6A. MAXIMUM MODE HS-80C86RH TYPICAL CONFIGURATION

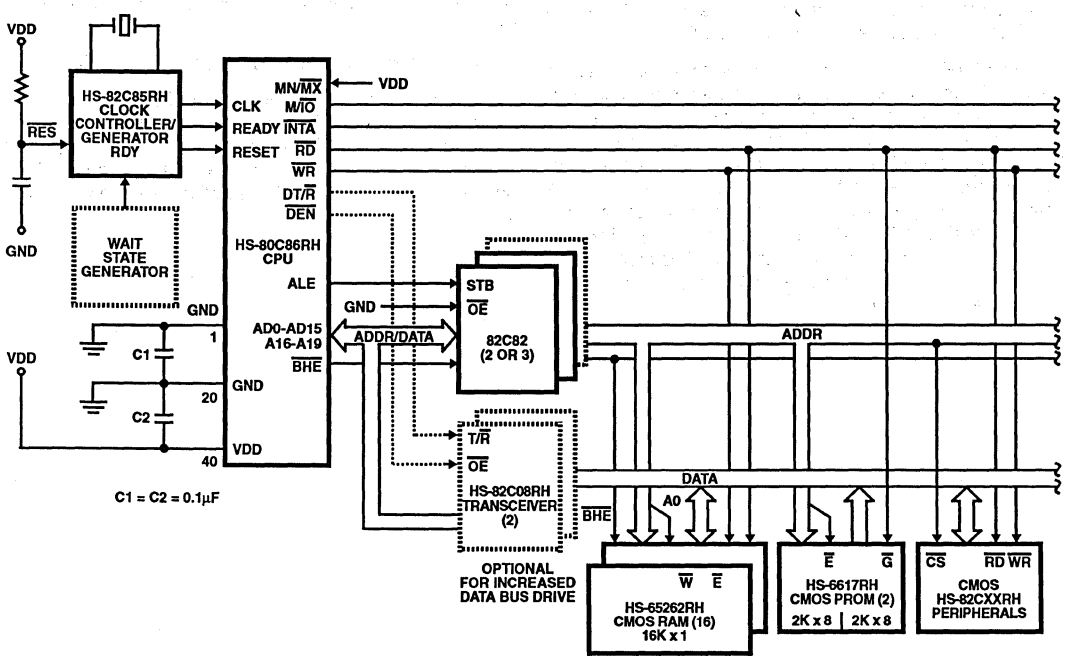
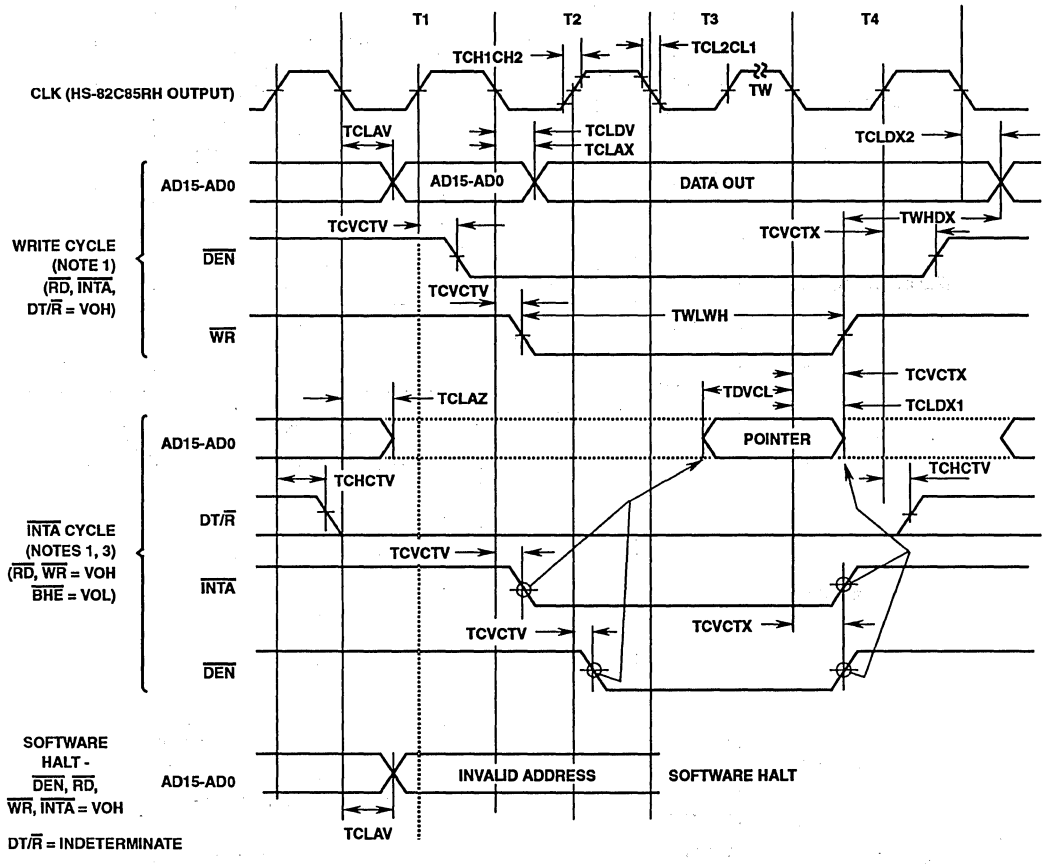


FIGURE 6B. MINIMUM MODE HS-80C86RH TYPICAL CONFIGURATION

Waveforms

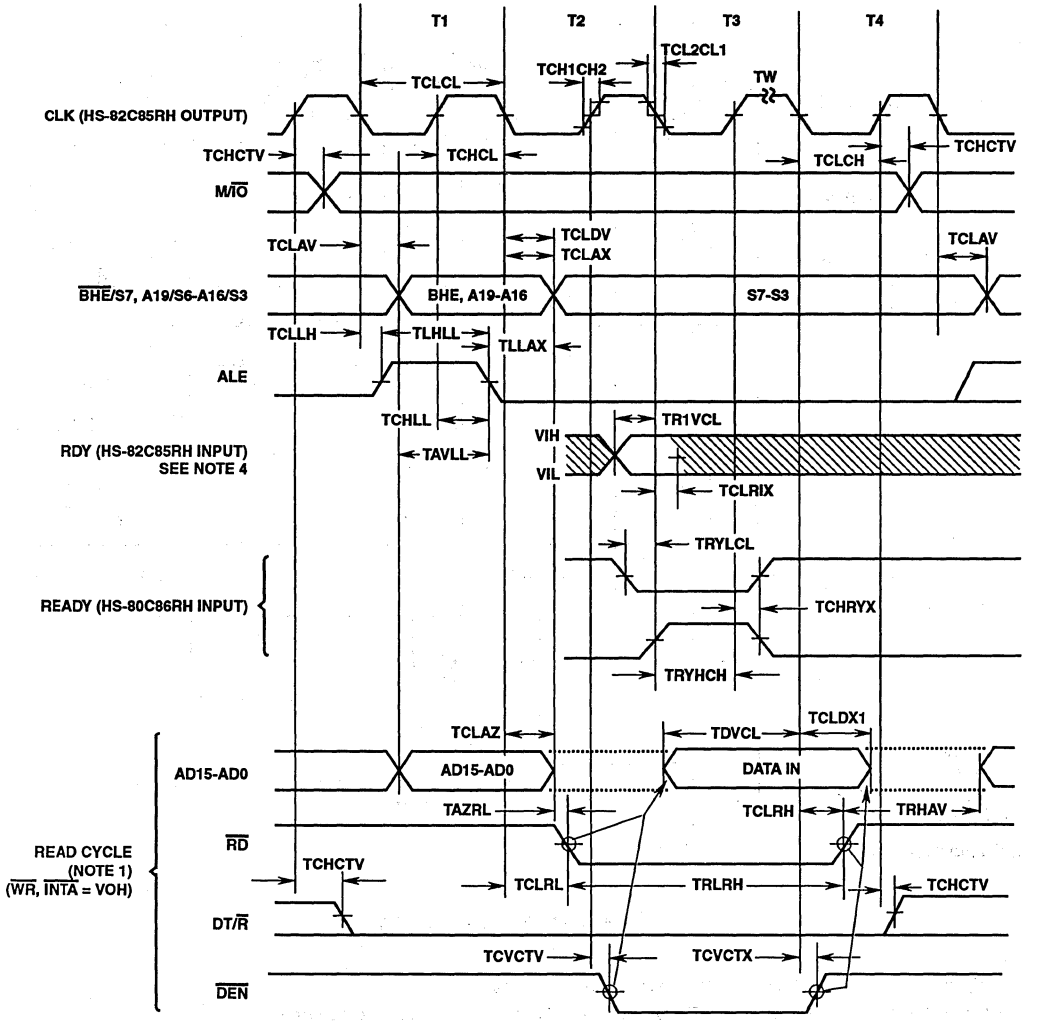


BUS TIMING - MINIMUM MODE SYSTEM

NOTES:

1. All signals switch between VOH and VOL unless otherwise specified.
2. RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted.
3. Two $\overline{\text{INTA}}$ cycles run back-to-back. The HS-80C86RH local ADDR/DATA bus is inactive during both $\overline{\text{INTA}}$ cycles. Control signals are shown for the second $\overline{\text{INTA}}$ cycle.
4. Signals at HS-82C85RH are shown for reference only.
5. All timing measurements are made at 1.5V unless otherwise noted.

Waveforms (Continued)

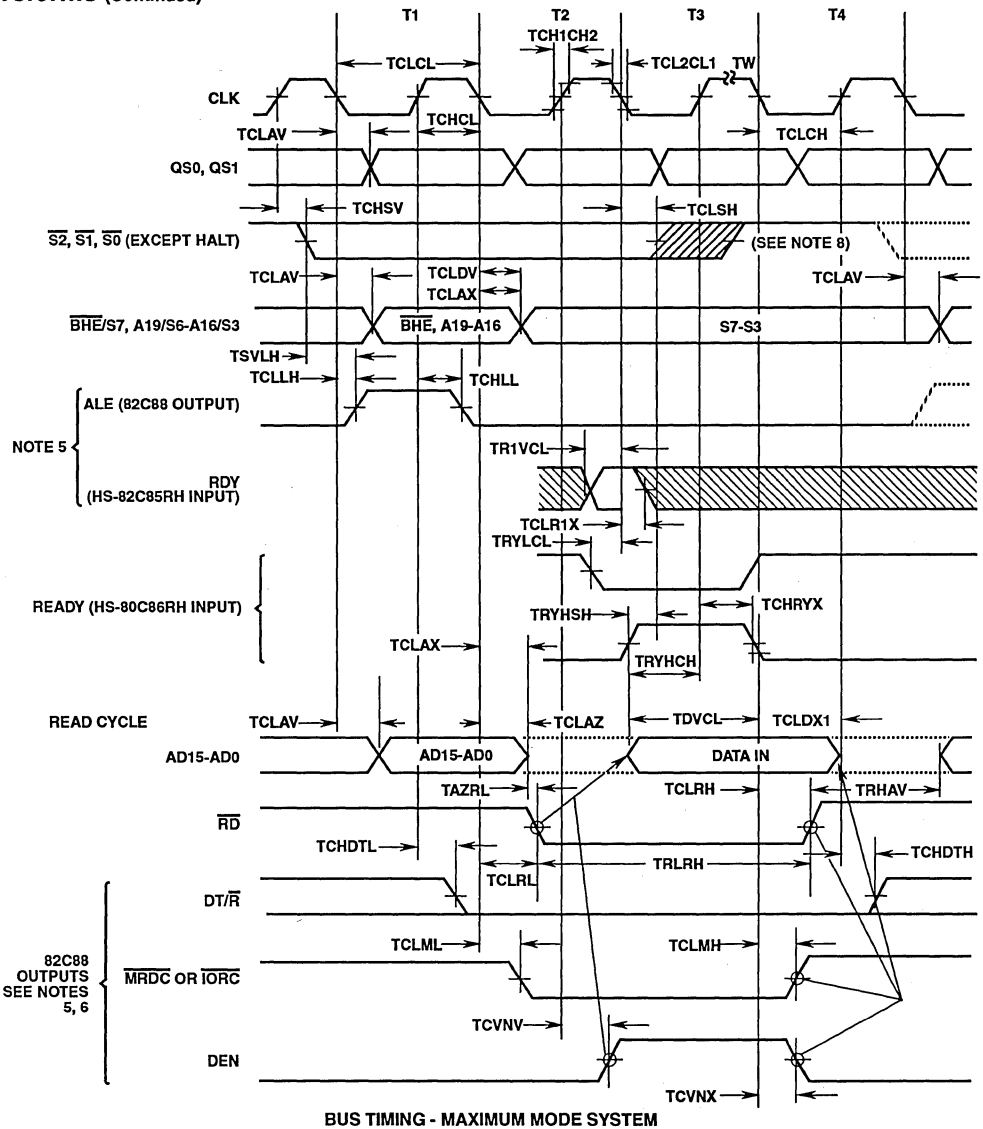


BUS TIMING - MINIMUM MODE SYSTEM

NOTES:

1. All signals switch between VOH and VOL unless otherwise specified.
2. RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted.
3. Two $\overline{\text{INTA}}$ cycles run back-to-back. The HS-80C86RH local ADDR/DATA bus is inactive during both $\overline{\text{INTA}}$ cycles. Control signals are shown for the second $\overline{\text{INTA}}$ cycle.
4. Signals at HS-82C85RH are shown for reference only.
5. All timing measurements are made at 1.5V unless otherwise noted.

Waveforms (Continued)

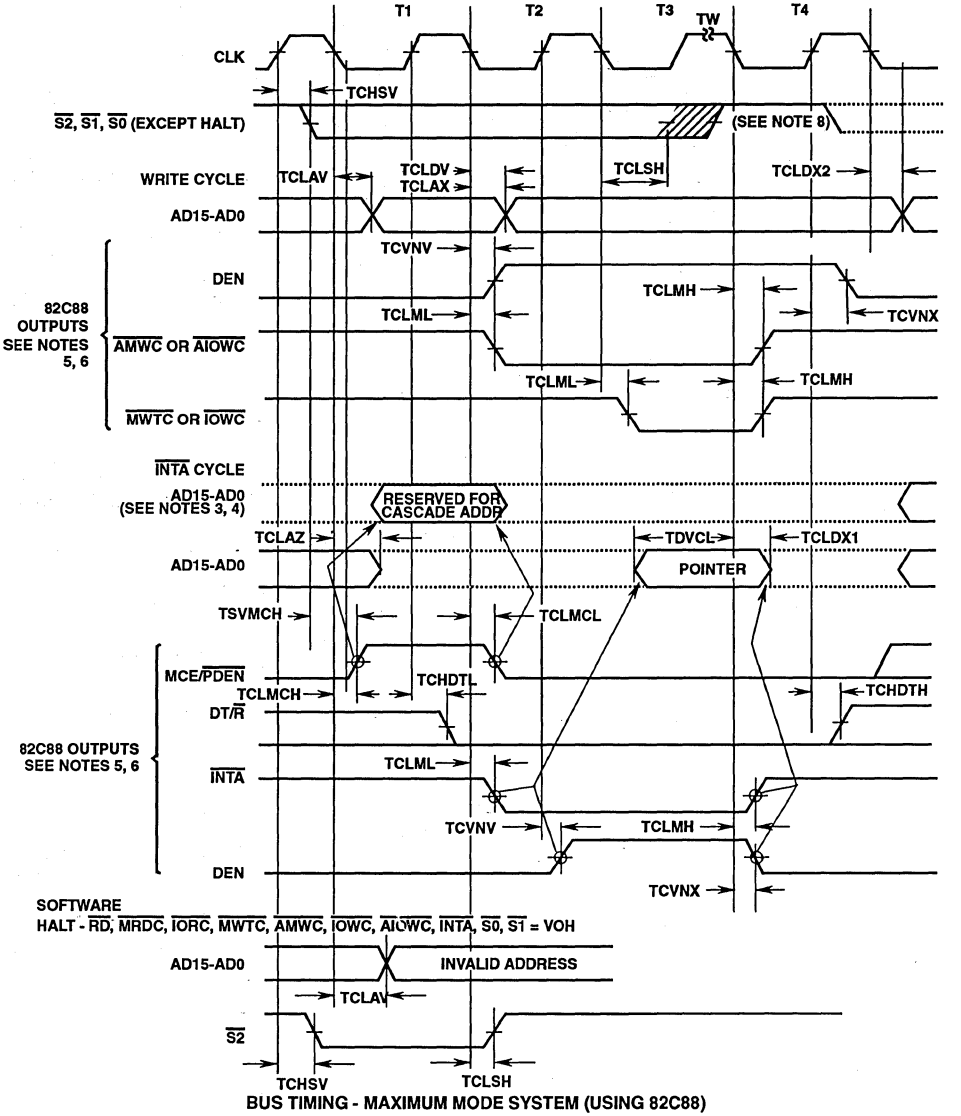


BUS TIMING - MAXIMUM MODE SYSTEM

NOTES:

1. All signals switch between VOH and VOL unless otherwise specified.
2. RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted.
3. Cascade address is valid between first and second $\overline{\text{INTA}}$ cycle.
4. Two $\overline{\text{INTA}}$ cycles run back-to-back. The HS-80C86RH local ADDR/DATA bus is inactive during both $\overline{\text{INTA}}$ cycles. Control for pointer address is shown for the second $\overline{\text{INTA}}$ cycle.
5. Signals at HS-82C85RH or 82C88 are shown for reference only.
6. The issuance of the 82C88 command and control signals ($\overline{\text{MRDC}}$, $\overline{\text{MWTC}}$, $\overline{\text{AMWC}}$, $\overline{\text{IORC}}$, $\overline{\text{IOWC}}$, $\overline{\text{AIOWC}}$, $\overline{\text{INTA}}$ and DEN) lags the active high 82C88 CEN.
7. All timing measurements are made at 1.5V unless otherwise noted.
8. Status inactive in state just prior to T4.

Waveforms (Continued)

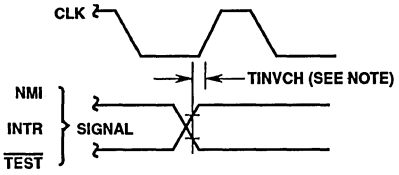


BUS TIMING - MAXIMUM MODE SYSTEM (USING 82C88)

NOTES:

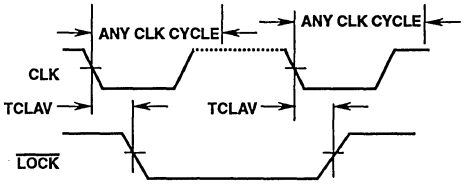
1. All signals switch between VOH and VOL unless otherwise specified.
2. RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted.
3. Cascade address is valid between first and second $\overline{\text{INTA}}$ cycle.
4. Two $\overline{\text{INTA}}$ cycles run back-to-back. The HS-80C86RH local ADDR/DATA bus is inactive during both $\overline{\text{INTA}}$ cycles. Control for pointer address is shown for the second $\overline{\text{INTA}}$ cycle.
5. Signals at HS-82C85RH or 82C88 are shown for reference only.
6. The issuance of the 82C88 command and control signals ($\overline{\text{MRDC}}$, $\overline{\text{MWTC}}$, $\overline{\text{AMWC}}$, $\overline{\text{IORC}}$, $\overline{\text{IOWC}}$, $\overline{\text{AIOWC}}$, $\overline{\text{INTA}}$ and DEN) lags the active high 82C88 CEN.
7. All timing measurements are made at 1.5V unless otherwise noted.
8. Status inactive in state just prior to T4.

Waveforms (Continued)

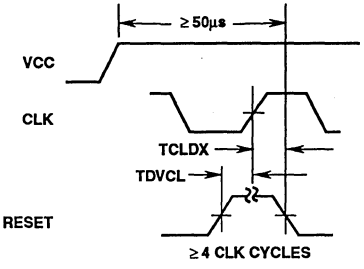


ASYNCHRONOUS SIGNAL RECOGNITION

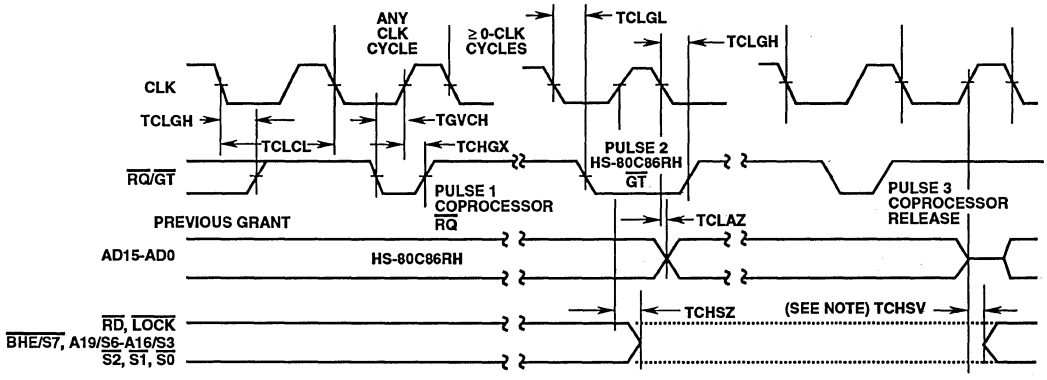
NOTE: Setup Requirements for asynchronous signals only to guarantee recognition at next CLK.



BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)

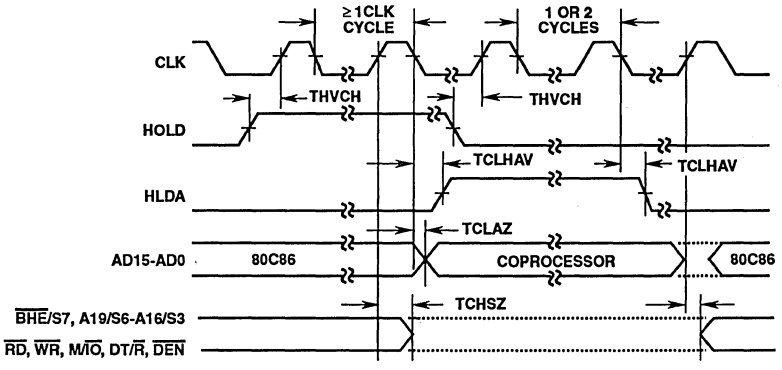


RESET TIMING



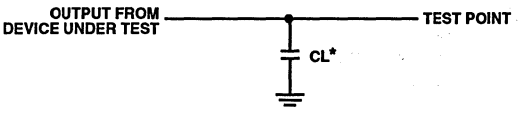
REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)

NOTE: The coprocessor may not drive the busses outside the region shown without risking contention.



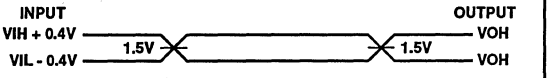
HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)

AC Test Circuits



* Includes stray and jig capacitance.

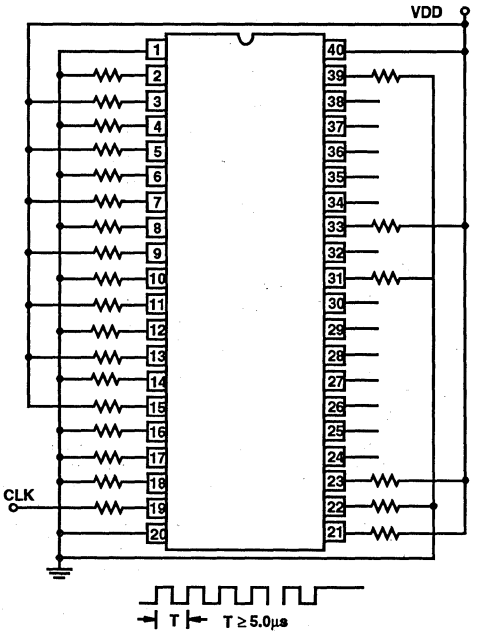
AC Testing Input, Output Waveform



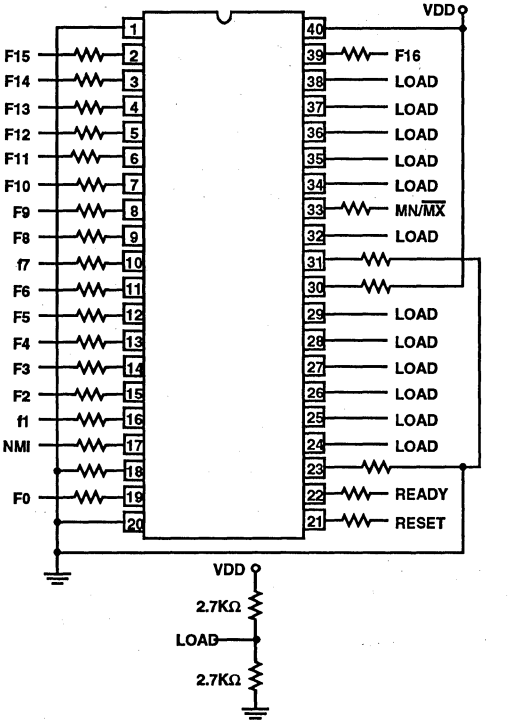
NOTE: All inputs signals (other than CLK) must switch between VIL-max -0.4V and VIHmin +0.4. CLK must switch between 0.4V and 3.9V. TR and TF must be less than or equal to 15ns. CLK TR and TF must be less than or equal to 10ns.

Burn-In Circuits

HS-80C86RH 40 PIN DIP



HS-80C86RH 40 PIN DIP



STATIC

VDD = +6.5V ± 10%
TA = +125°C Minimum
Part is Static Sensitive
Voltages Must Be Ramped
Package: 40 Pin DIP

Resistors:
10kΩ ± 10%
(Pins 17, 18, 21-23, 31, 33)
2.7kΩ ± 5% (Pins 2-16, 39)
1.0kΩ ± 5% 1/10Ω Min (Pin 19)
Minimum of 5 CLK Pulses
After Initial Pulses, CLK is Left High
Pulses are 50% Duty Cycle Square Wave

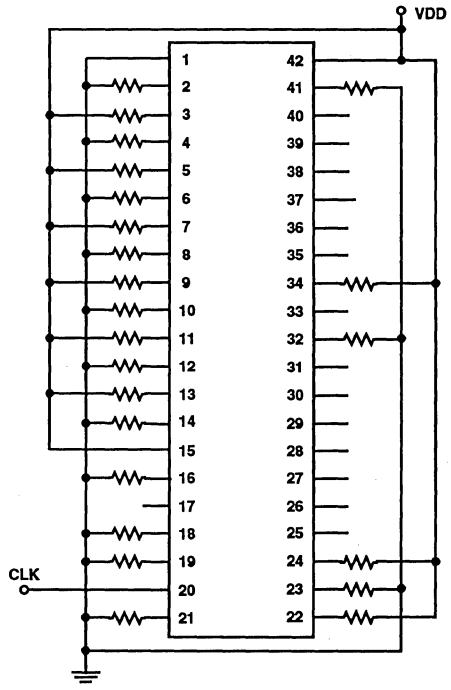
DYNAMIC

VDD = 6.5V ± 5% (Burn-In)
VDD = 6.0V ± 5% (Life Test)
TA = +125°C
Package: 40 Pin DIP
Part is Static Sensitive
Voltage Must Be Ramped

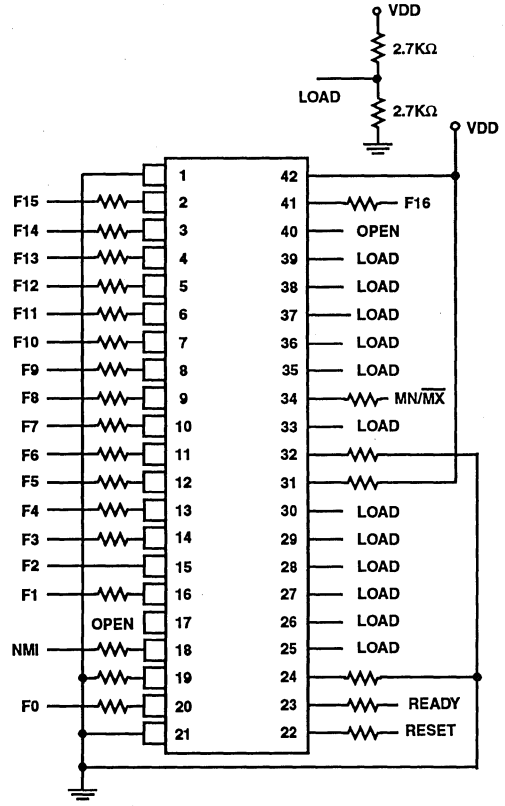
Resistors:
10kΩ (Pins 17, 18, 21, 22, 23, 33)
3.3kΩ (Pins 2-16, 19, 30, 31, 39)
2.7kΩ Loads As Indicated
All Resistors Are At Least 1/8W, ± 10%
F0 = 100kHz, F1 = F0/2, F2 = F1/2 . . .
RESET, NMI low after initialization.
READY pulsed low every 320ms
MN/MX changes state every 5.24s

Burn-In Circuits (Continued)

HS-80C86RH 42 LEAD FLATPACK



HS-80C86RH 42 LEAD FLATPACK



STATIC

VDD = +6.5V ± 10%
TA = +125°C Minimum
Part is Static Sensitive
Voltages Must Be Ramped
Package: 42 Pin Flatpack

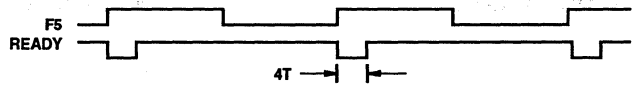
Resistors:
10kΩ ± 10%
(Pins 17, 18, 21-23, 31, 33)
2.7kΩ ± 5% (Pins 2-16, 39)
1.0kΩ ± 5% 1/10Ω Min (Pin 19)
Minimum of 5 CLK Pulses
After Initial Pulses, CLK is Left High
Pulses are 50% Duty Cycle Square Wave

DYNAMIC

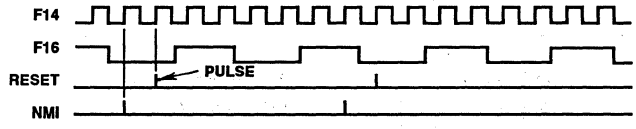
VDD = 6.5V ± 5% (Burn-In)
VDD = 6.0V ± 5% (Life Test)
TA = +125°C
Package: 42 Pin Flatpack
Part is Static Sensitive
Voltage Must Be Ramped

Resistors:
10kΩ (Pins 17, 18, 21, 22, 23, 33)
3.3kΩ (Pins 2-16, 19, 30, 31, 39)
2.7kΩ Loads As Indicated
All Resistors Are At Least 1/8W, ± 10%
F0 = 100kHz, F1 = F0/2, F2 = F1/2 . . .
RESET, NMI low after initialization.
READY pulsed low every 320ms
MN/$\overline{MX}$ changes state every 5.24s

Timing Diagrams



READY TIMING AS COMPARED TO F5



RESET, NMI, AND MN/$\overline{MX}$ TIMING AS COMPARED TO F14 AND F16

F0 = 100kHz, 50% duty cycle square wave.
F1 = F0/2, F2 = F1/2 . . . F16 = F15/2.

READY, RESET, and NMI timing are as shown below:
T = 10µs.

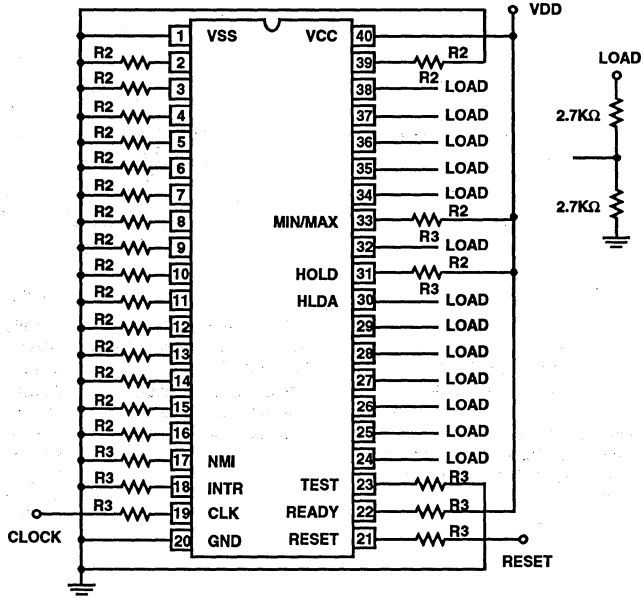
All signals have rise/fall time limits:
100ns < t-rise, t-fall < 500ns

RESET has a pulse width = 8T and occurs every two cycles of F16.

NMI has a pulse width = 4T and occurs every two cycles of F16.

MN/$\overline{MX}$ is a 50% duty cycle square wave and changes every eight cycles of F16.

Irradiation Circuit



NOTE:

1. VDD = 5.0V ± 0.5V
2. R2 = 3.3kΩ, R3 = 47kΩ
3. Pins Tied to Gnd: 1-18, 20, 23, 39
   Pins Tied to VCC: 22, 31, 33, 40
   Pins With Loads: 24-29, 30, 32, 34-38
   Pins Brought Out: 19 (Clock), 21 (Reset)
4. All Group E testing is performed in the sidebrazed DIP
5. Clock and reset should be brought out separately so they can be toggled before irradiation.
6. Group E Sample Size is 2 Die/Wafer.

Harris - Space Level Product Flow -Q (Note 1)

SEM - Traceable to Diffusion Method 2018

Wafer Lot Acceptance Method 5007

Internal Visual Inspection Method 2010, Condition A

Gamma Radiation Assurance Tests Method 1019

Nondestructive Bond Pull Method 2023

Customer Pre-Cap Visual Inspection (Note 2)

Temperature Cycling Method 1010, Condition C

Constant Acceleration Method 2001, Condition E Min, Y1

Particle Impact Noise Detection Method 2020, Condition A

Electrical Tests Harris' Option

Serialization

X-Ray Inspection Method 2012

Electrical Tests Subgroup 1; Read and Record (TO)

Static Burn-In Method 1015, Condition B, 72 Hours, +125°C Minimum

Electrical Tests Subgroup 1; Read and Record (T1)

Burn-In Delta Calculation (T0-T1)

PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ

Dynamic Burn-In Method 1015 Condition D, 240 Hours, +125°C (Note 3)

Electrical Tests Subgroup 1; Read and Record (T2)

Alternate Group A Subgroups 1, 7, 9; Method 5005; Para 3.5.1.1

Burn-In Delta Calculation (TO-T2)

PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ

Electrical Test Subgroup 3; Read and Record

Alternate Group A Subgroups 3, 8B, 11; Method 5005; Para 3.5.1.1

Marking

Electrical Tests Subgroup 2; Read and Record

Alternate Group A Subgroups 2, 8A, 10; Method 5005; Para 3.5.1.1

Gross Leak Method 1014, 100%

Fine Leak Method 1014, 100%

Customer Source Inspection (Note 2)

Group B Inspection Method 5005 (Note 2)
End-Point Electrical Parameters:
B-5/ Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11
B-6; Subgroups 1, 7, 9

Group D Inspection Method 5005 (Notes 2, 4)
End-Point Electrical Parameters: Subgroups 1, 7, 9

External Visual Inspection Method 2009

Data Package Generation (Note 5)

NOTES:

1. The notes of Method 5004, Table 1 Shall apply; unless otherwise specified.
2. These steps are optional and should be listed on the individual purchase order(s), when required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table 1 of Method 1015
4. For group D, subgroup 3 inspection of package configurations which utilize a gold plated lid in its construction; the inspection criteria for illegible markings criteria of Method 1010, paragraph 3.3 and of Method 1004, paragraph 3.8.a shall not apply.
5. Data package contains:
   - Assembly attributes (Post Seal)
   - Test attributes (includes Group A)
   - Shippable serial number list
   - Radiation testing certificate of conformance
   - Wafer lot acceptance report (including SEM report)
   - X-ray report and film
   - Test variables data

Metallization Topology

DIE DIMENSIONS:
6370µm x 7420µm x 485µm

METALLIZATION:
Type: Al/S
Thickness: 11kÅ ± 2kÅ

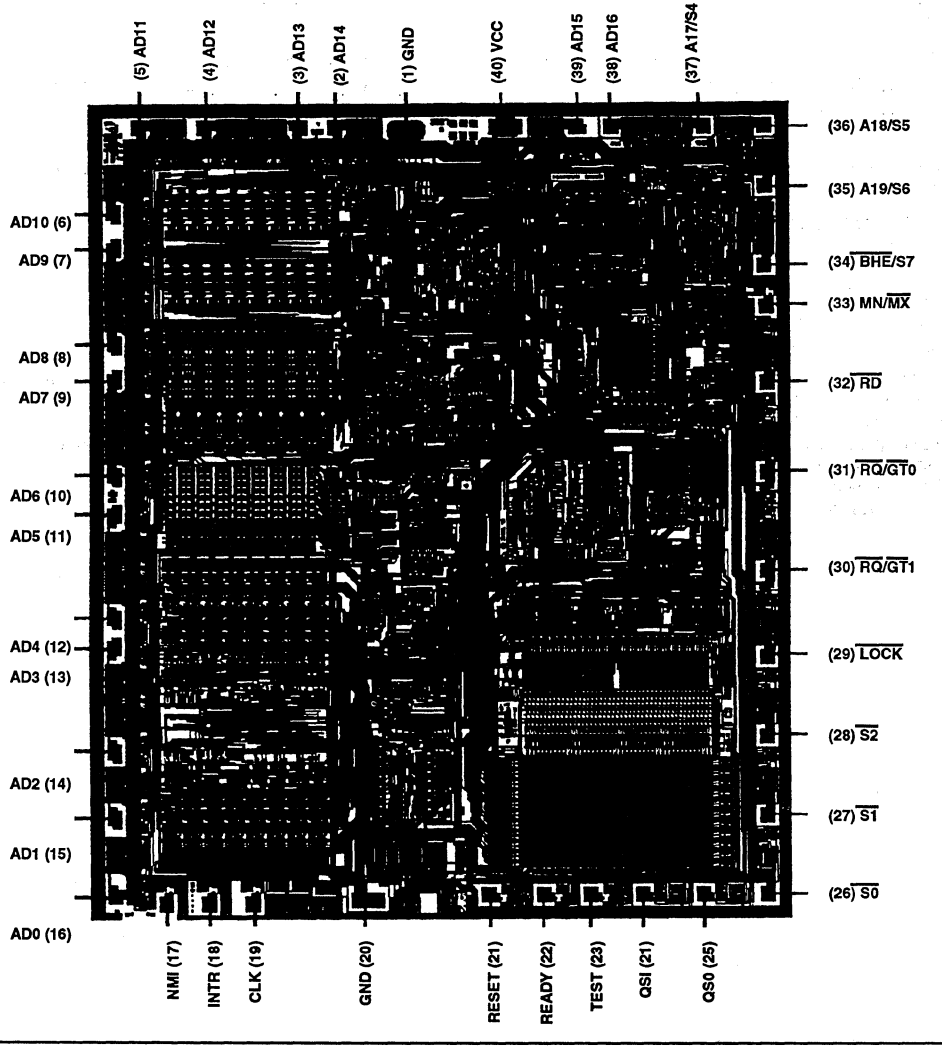
GLASSIVATION:
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold

WORST CASE CURRENT DENSITY:
1.1×10^5 A/cm^2

Metallization Mask Layout

HS-80C86RH



Instruction Set Summary

Mnemonic and Description	Instruction Code			
DATA TRANSFER				
MOV = Move:	76543210	76543210	76543210	76543210
Register/Memory to/from Register	100010dw	mod reg r/m		
Immediate to Register/Memory	1100011w	mod000r/m	data	data if w 1
Immediate to Register	1011w reg	data	data if w 1	
Memory to Accumulator	1010000w	add-low	addr-high	
Accumulator to Memory	1010001w	addr-low	addr-high	
Register/Memory to Segment Register**	10001110	mod 0 reg r/m		
Segment Register to Register/Memory	10001100	mod 0 reg r/m		
PUSH = Push:				
Register/Memory	11111111	mod 1 1 0 r/m		
Register	01010reg			
Segment Register	000reg110			
POP = Pop:				
Register/Memory	10001111	mod000r/m		
Register	01011reg			
Segment Register	000reg111			
XCHG = Exchange:				
Register/Memory with Register	1000011w	mod reg r/m		
Register with Accumulator	10010reg			
IN = Input from:				
Fixed Port	1110010w	port		
Variable Port	1110110w			
OUT = Output to:				
Fixed Port	1110011w	port		
Variable Port	1110111w			
XLAT = Translate Byte to AL	11010111			
LEA = Load EA to Register	10001101	mod reg r/m		
LDS = Load Pointer to DS	11000101	mod reg r/m		
LES = Load Pointer to ES	11000100	mod reg r/m		
LAHF = Load AH with Flags	10011111			
SAHF = Store AH into Flags	10011110			
PUSHF = Push Flags	10011100			
POPF = Pop Flags	10011101			

Instruction Set Summary (Continued)

Mnemonic and Description	Instruction Code			
ARITHMETIC	76543210	76543210	76543210	76543210
ADD = Add:				
Reg./Memory with Register to Either	000000dw	mod reg r/m		
Immediate to Register/Memory	100000sw	mod 000 r/m	data	data if s:w = 01
Immediate to Accumulator	0000010w	data	data if w = 1	
ADC = Add with Carry:				
Reg./Memory with Register to Either	000100dw	mod reg r/m		
Immediate to Register/Memory	100000sw	mod 010 r/m	data	data if s:w = 01
Immediate to Accumulator	0001010w	data	data if w = 1	
INC = Increment:				
Register/Memory	1111111w	mod 000 r/m		
Register	01000reg			
AAA = ASCII Adjust for Add	00110111			
DAA = Decimal Adjust for Add	00100111			
SUB = Subtract:				
Reg./Memory and Register to Either	001010dw	mod reg r/m		
Immediate from Register/Memory	100000sw	mod 101 r/m	data	data if s:w = 01
Immediate from Accumulator	0010110w	data	data if w = 1	
SBB = Subtract with Borrow				
Reg./Memory and Register to Either	000110dw	mod reg r/m		
Immediate from Register/Memory	100000sw	mod 011 r/m	data	data if s:w = 01
Immediate from Accumulator	0001110w	data	data if w = 1	
DEC = Decrement:				
Register/Memory	1111111w	mod 001 r/m		
Register	01001 reg			
NEG = Change Sign	1111011w	mod 011 r/m		
CMP = Compare:				
Register/Memory and Register	001110dw	mod reg r/m		
Immediate with Register/Memory	100000sw	mod 111 r/m	data	data if s:w = 01
Immediate with Accumulator	0011110w	data	data if w = 1	
AAS = ASCII Adjust for Subtract	00111111			
DAS = Decimal Adjust for Subtract	00101111			
MUL = Multiply (Unsigned)	1111011w	mod 100 r/m		
IMUL = Integer Multiply (Signed)	1111011w	mod 101 r/m		
AAM = ASCII Adjust for Multiply	11010100	00001010		
DIV = Divide (Unsigned)	1111011w	mod 110 r/m		
IDIV = Integer Divide (Signed)	1111011w	mod 111 r/m		
AAD = ASCII Adjust for Divide	11010101	00001010		
CBW = Convert Byte to Word	10011000			
CWD = Convert Word to Double Word	10011001			

Instruction Set Summary (Continued)

Mnemonic and Description	Instruction Code			
LOGIC	76543210	76543210	76543210	76543210
NOT = Invert	1111011w	mod 010 r/m		
SHL/SAL = Shift Logical/Arithmetic Left	110100vw	mod 100 r/m		
SHR = Shift Logical Right	110100vw	mod 101 r/m		
SAR = Shift Arithmetic Right	110100vw	mod 111 r/m		
ROL = Rotate Left	110100vw	mod 000 r/m		
ROR = Rotate Right	110100vw	mod 001 r/m		
RCL = Rotate Through Carry Flag Left	110100vw	mod 010 r/m		
RCR = Rotate Through Carry Right	110100vw	mod 011 r/m		
AND = And:				
Reg./Memory and Register to Either	001000dw	mod reg r/m		
Immediate to Register/Memory	1000000w	mod 100 r/m	data	data if w = 1
Immediate to Accumulator	0010010w	data	data if w = 1	
TEST = And Function to Flags, No Result:				
Register/Memory and Register	1000010w	mod reg r/m		
Immediate Data and Register/Memory	1111011w	mod 000 r/m	data	data if w = 1
Immediate Data and Accumulator	1010100w	data	data if w = 1	
OR = Or:				
Reg./Memory and Register to Either	000010dw	mod reg r/m		
Immediate to Register/Memory	1000000w	mod 001 r/m	data	data if w = 1
Immediate to Accumulator	0000110w	data	data if w = 1	
XOR = Exclusive or:				
Reg./Memory and Register to Either	001100dw	mod reg r/m		
Immediate to Register/Memory	1000000w	mod 110 r/m	data	data if w = 1
Immediate to Accumulator	0011010w	data	data if w = 1	
STRING MANIPULATION				
REP = Repeat	1111001z			
MOVS = Move Byte/Word	1010010w			
CMPS = Compare Byte/Word	1010011w			
SCAS = Scan Byte/Word	1010111w			
LODS = Load Byte/Wd to AL/AX	1010110w			
STOS = Stor Byte/Wd from AL/A	1010101w			
CONTROL TRANSFER				
CALL = Call:				
Direct Within Segment	11101000	disp-low	disp-high	
Indirect Within Segment	11111111	mod 010 r/m		
Direct Intersegment	10011010	offset-low	offset-high	
		seg-low	seg-high	
Indirect Intersegment	11111111	mod 011 r/m		

Instruction Set Summary (Continued)

Mnemonic and Description	Instruction Code		
JMP = Unconditional Jump:	76543210	76543210	76543210
Direct Within Segment	11101001	disp-low	disp-high
Direct Within Segment-Short	11101011	disp	
Indirect Within Segment	11111111	mod 100 r/m	
Direct Intersegment	11101010	offset-low	offset-high
		seg-low	seg-high
Indirect Intersegment	11111111	mod 101 r/m	
RET = Return from CALL:			
Within Segment	11000011		
Within Seg Adding Immed to SP	11000010	data-low	data-high
Intersegment	11001011		
Intersegment Adding Immediate to SP	11001010	data-low	data-high
JE/JZ = Jump on Equal/Zero	01110100	disp	
JL/JNGE = Jump on Less/Not Greater or Equal	01111100	disp	
JLE/JNG = Jump on Less or Equal/ Not Greater	01111110	disp	
JB/JNAE = Jump on Below/Not Above or Equal	01110010	disp	
JBE/JNA = Jump on Below or Equal/ Not Above	01110110	disp	
JP/JPE = Jump on Parity/Parity Even	01111010	disp	
JO = Jump on Overflow	01110000	disp	
JS = Jump on Sign	01111000	disp	
JNE/JNZ = Jump on Not Equal/Not Zero	01110101	disp	
JNL/JGE = Jump on Not Less/Greater or Equal	01111101	disp	
JNLE/JG = Jump on Not Less or Equal/ Greater	01111111	disp	
JNB/JAE = Jump on Not Below/Above or Equal	01110011	disp	
JNBE/JA = Jump on Not Below or Equal/Above	01110111	disp	
JNP/JPO = Jump on Not Par/Par Odd	01111011	disp	
JNO = Jump on Not Overflow	01110001	disp	
JNS = Jump on Not Sign	01111001	disp	
LOOP = Loop CX Times	11100010	disp	
LOOPZ/LOOPE = Loop While Zero/Equal	11100001	disp	
LOOPNZ/LOOPNE = Loop While Not Zero/Equal	11100000	disp	
JCXZ = Jump on CX Zero	11100011	disp	
INT = Interrupt			
Type Specified	11001101	type	
Type 3	11001100		
INTO = Interrupt on Overflow	11001110		
IRET = Interrupt Return	11001111		

Instruction Set Summary (Continued)

Mnemonic and Description	Instruction Code	
	76543210	76543210
PROCESSOR CONTROL		
CLC = Clear Carry	11111000	
CMC = Complement Carry	11110101	
STC = Set Carry	11111001	
CLD = Clear Direction	11111100	
STD = Set Direction	11111101	
CLI = Clear Interrupt	11111010	
STI = Set Interrupt	11111011	
HLT = Halt	11110100	
WAIT = Wait	10011011	
ESC = Escape (to External Device)	11011xxx	mod x x x r/m
LOCK = Bus Lock Prefix	11110000	

NOTES:
AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value.
Greater = more positive;
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg
if w = 1 then word instruction; if w = 0 then byte instruction
if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16 bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)
*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.
**MOV CS, REG/MEMORY not allowed.
if s:w = 01 then 16 bits of immediate data form the operand.
if s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand.
if v = 0 then "count" = 1; if v = 1 then "count" in (CL)
x = don't care
z is used for string primitives for comparison with ZF FLAG.

SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:
FLAGS =
X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

RAD HARD 11

MICROPROCESSOR PERIPHERALS

HARRIS SEMICONDUCTOR

HS-3374RH

Radiation Hardened 8-Bit Bidirectional CMOS/TTL Level Converter

December 1992

Features

- Radiation Hardened EPI-CMOS
  - Total Dose 1 x 10^5 RAD(Si)
  - Latch-Up Immune > 1 x 10^{12} RAD(Si)/s*
- Low Propagation Delay Time
  - Typical CMOS to TTL Pre-Rad 40ns
  - Typical CMOS to TTL Post 100K RADs 40ns
  - Typical TTL to CMOS Pre-Rad 50ns
  - Typical TTL to CMOS Post 100K RADs 50ns
- Low Standby Power
- +10V CMOS and +5V TTL Power Supply Inputs
- Eight Non-Inverting Three-State Input/Output Channels
- No External TTL Input Pull-Up Resistors Required
- High TTL Sink Current
- Equivalent to Sandia SA2996
- Military Temperature Range -55°C to +125°C

Description

The Harris HS-3374RH is a radiation hardened 8-bit bidirectional level converter designed to interface CMOS logic levels with TTL logic levels in radiation hardened bus oriented systems. The HS-3374RH is fabricated using a radiation hardened EPI-CMOS process and features eight parallel bidirectional buffer/level converters.

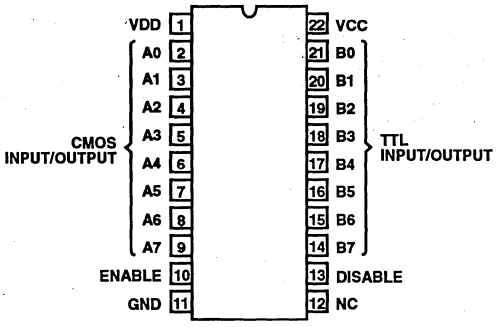
Two control inputs, ENABLE and DISABLE, are used to determine the direction of data flow, and to set both the in puts and outputs in the high impedance state. The control inputs may be driven by either TTL or CMOS logic drivers capable of sinking one standard TTL load.

The HS-3374RH is a non-inverting version of the industry standard CD40116. The non-inverting outputs of the HS-3374RH reduce PC board chip count by eliminating the need to restore data back to a non-inverted format.

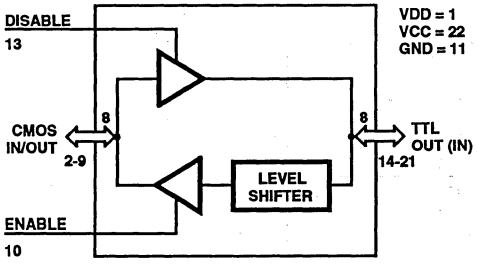
* For operation at 10V and transient levels above 1 x 10^{10} Rad(Si)/s, please refer to Application Note 401.

Pinout

INTERNAL PACKAGE CODE HSX
CASE OUTLINE D7, CONFIGURATION 3
TOP VIEW



Functional Diagram



11 µPROCESSOR PERIPHERALS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3038

Absolute Maximum Ratings

Supply Voltage ..... +11.0V
I/O Voltage Applied ..... GND-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic Dip Package	74.8°C/W	123°C/W

Maximum Package Power Dissipation at +125°C
Ceramic Dip Package ..... .67W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range VDD ..... +9.5V to +10.5V
VCC ..... +4.75V to +5.25V
Operating Temperature Range ..... -55°C to +125°C
Input Voltage Range
Data Inputs (CMOS) ..... .GND-0.3 to VDD+0.3
Data Inputs (TTL) ..... .GND-0.3 to VCC+0.3
Enable, Disable Inputs ..... .GND-0.3 to VDD+0.3

Input Low Voltage (CMOS) ..... GND to 1V
Input High Voltage (CMOS) ..... .VDD-1.0V to VDD
Input Low Voltage (TTL) 0.8V
Input High Voltage (TTL) 2.8V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
ENABLE AND DISABLE IINPUTS							
Input Leakage Current	IIH CMOS	VDD = 10.5V, VCC = 5.25V, VIN = 10.5V, Floating Outputs	1, 2, 3	-55°C, +25°C, +125°C	-	1	µA
TTL INPUT TO CMOS OUTPUTS							
Input Leakage Current	IIL IIH	VDD = 10.5V, VCC = 5.25V, VIN = 0.8V, Other Inputs at 2.8V	1, 2, 3	-55°C, +25°C, +125°C	-1	-	µA
		VDD = 10.5V, VCC = 5.25V, VIN = 2.8V, other Inputs = 0.8V	1, 2, 3	-55°C, +25°C, +125°C	-	1	µA
High Level Output Voltage	VOH	VDD = 9.5V, VCC = 4.75V, VIH = 2.8V, VIL = 0.8V, IOH = -2.0mA	1, 2, 3	-55°C, +25°C, +125°C	3	-	V
Low level output Voltage	VOL	VDD = 10.5V, VCC = 5.25V, VIH = 2.8V, VIL 0.8V, IOL = 2.0mA	1, 2, 3	-55°C, +25°C, +125°C	-	0.4	V
CMOS to TTL OUTPUTS							
High Level Output Voltage	VOH	VDD = 9.5, VCC = 4.75V, VIH = 8.5V, VIL = 1.0V, IOH = -2.0mA	1, 2, 3	-55°C, +25°C, +125°C	9	-	V
Low Level Output Voltage	VOL	VDD = 10.5V, VCC = 5.25V, VIH = 4.5V, VIL = 1.0V, IOL = 11mA	1, 2, 3	-55°C, +25°C, +125°C	-	0.5	V
Output Leakage Current	IOZL	VDD = 10.5V, VCC = 5.25V, VIN = 0V, All other pins high	1, 2, 3	-55°C, +25°C, +125°C	-10	-	µA
	IOZH	VDD = 10.5V, VCC = 5.25V, VIN = 2.8V, All other pins at GND	1, 2, 3	-55°C, +25°C, +125°C	-	10	µA
Functional Tests	FT	CMOS: 1.) VDD = 10.5V, VCC = 5.25V 2.) VDD = 9.5V, VCC = 4.75V, VIH = VDD-1V, VIL = 1V TTL: 1.) VDD = 10.5V, VCC = 5.25V 2.) VDD = 9.5V, VCC = 4.75V, VIH = 2.8V, VIL = 0.8V	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Static Current 1	SIDD1	VDD = 10.5V, VCC = 5.25V, EN = 2.8V, DISABLE = 2.8V, Floating Outputs	1, 2, 3	-55°C, +25°C, +125°C	-	300	µA
Static Current 2	SIDD2	VDD = 10.5V, VCC = 5.25V, EN = 0V, DISABLE = 2.8V, Floating Outputs	1, 2, 3	-55°C, +25°C, +125°C	-	100	µA
Static Current	SICC	VDD = 10.5, VCC = 5.25V, EN = 0V, DISABLE = 2.8V, Floating Output, Measure VCC pin	1, 2, 3	-55°C, +25°C, +125°C	-	5	µA

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Times CMOS/TTL Data In to Data Out	TPHLCT	9, 10, 11	-55°C, +25°C, +125°C	-	40	ns
Propagation Delay Times CMOS Data In to Data Out	TPLHCT	9, 10, 11	-55°C, +25°C, +125°C	-	50	ns
Propagation Delay Times CMOS/TTL Data In to Data Out	TPHLTC	9, 10, 11	-55°C, +25°C, +125°C	-	85	ns
Propagation Delay Time TTL/CMOS Data In to Data Out	TPLHTC	9, 10, 11	-55°C, +25°C, +125°C	-	70	ns
Transition Time CMOS/TTL Input/Output	TTHLCT	9, 10, 11	-55°C, +25°C, +125°C	-	20	ns
Transition Time CMOS/TTL Input/Output	TTLHCT	9, 10, 11	-55°C, +25°C, +125°C	-	70	ns
Transition Time CMOS/TTL Input/Output	TTHLTC	9, 10, 11	-55°C, +25°C, +125°C	-	50	ns
Transition Time CMOS/TTL Input/Output	TTLHTC	9, 10, 11	-55°C, +25°C, +125°C	-	50	ns
Propagation Delay Time TTL/CMOS Enable to CMOS Out	TPHZTC	9, 10, 11	-55°C, +25°C, +125°C	-	90	ns
Propagation Delay Time TTL/CMOS Enable to CMOS Out	TPZHTC	9, 10, 11	-55°C, +25°C, +125°C	-	90	ns
Propagation Delay Time TTL/CMOS Enable to CMOS Out	TPLZTC	9, 10, 11	-55°C, +25°C, +125°C	-	85	ns
Propagation Delay Time TTL/CMOS Enable to CMOS Out	TPZLTC	9, 10, 11	-55°C, +25°C, +125°C	-	85	ns
Propagation Delay Time CMOS/TTL Disable to TTL Out	TPHZCT	9, 10, 11	-55°C, +25°C, +125°C	-	70	ns
Propagation Delay Time CMOS/TTL Disable to TTL Out	TPZHCT	9, 10, 11	-55°C, +25°C, +125°C	-	130	ns
Propagation Delay Time CMOS/TTL Disable to TTL Out	TPLZCT	9, 10, 11	-55°C, +25°C, +125°C	-	120	ns
Propagation Delay Time CMOS/TTL Disable to TTL Out	TPZLCT	9, 10, 11	-55°C, +25°C, +125°C	-	125	ns

NOTE: Timings are measured with the following conditions: CL = 100pF, VDD = 9.5V, VCC = 4.75V, VIH = 8.5V (2.8V), VIL = 1.0V (0.8V).

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input, Output Capacitance	CMOS CI/O	VDD = Open, f = 1MHz, All Measurements Referenced to Device Ground	+25°C	-	13	pF
Input Capacitance	CIN	VDD = Open, f = 1MHz, All Measurements Referenced to Device Ground	+25°C	-	15	pF
Input, Output Capcitance	TTL CI/O	VDD = Open, f = 1MHz, All Measurements Referenced to Device Ground	+25°C	-	17	pF

NOTE: The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The Post Irradiation test conditions and limits are the same as those listed in Table 1 and Table 2.

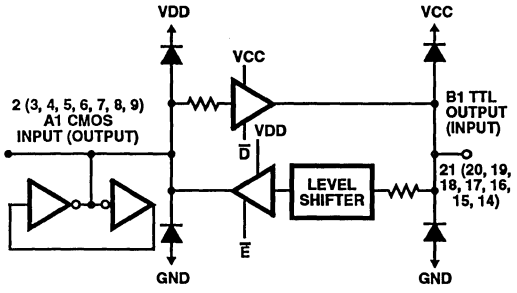
TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Static Current 1	SIDD1	±50µA
Static Current 2	SIDD2	±30µA
Low Input Leakage Current	IIL	±100nA
High Input Leakage Current	IIH	±100nA
Low Output Leakage Current	IOZL	±1µA
High Output Leakage Current	IOZH	±1µA

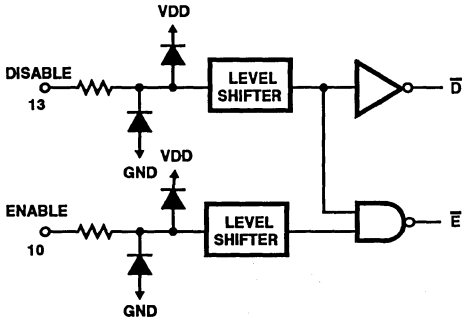
TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	-8 SUBGROUPS
Initial Test	100%/5004	1, 7, 9
PDA	100%/5004	1, 7
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group C	Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group D Others	Samples/5004	1, 7
Group E Subgroup 2	Samples/5004	1, 7, 9

Functional Block Diagram



1 OF 8 IDENTICAL CIRCUITS



NOTES:

1. Enable and disable are TTL type inputs
2. D and E outputs are common to all 8 channels

INPUT (OUTPUT)		OUTPUT (INPUT)	
DATA	TERMINAL NUMBER	DATA	TERMINAL NUMBER
A0	2	B0	21
A1	3	B1	20
A2	4	B2	19
A3	5	B3	18
A4	6	B4	17
A5	7	B5	16
A6	8	B6	15
A7	9	B7	14

TRUTH TABLE

ENABLE	DISABLE	FUNCTION
X	0	Convert CMOS Level to TTL Level
1	1	Convert TTL Level to CMOS Level
0	1	High Impedance (Z)

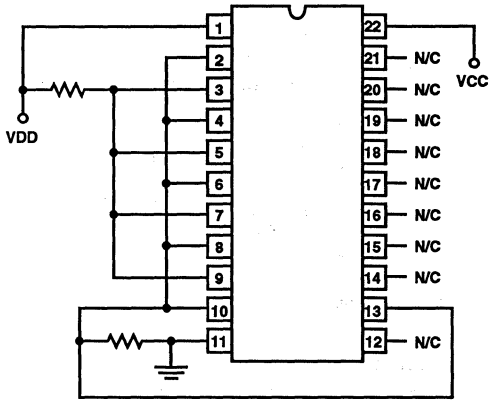
0 = Low Level 1 = High Level X = Don't Care
Z = High Impedance on Both CMOS and TTL sides.

NOTE: An important caveat that is applicable to CMOS devices in general is that unused inputs should never be left floating. This rule applies to inputs connected to a three-state bus. The need for external pull-up resistors during three-state bus conditions is eliminated by the presence of regenerative latches on the following HS-3374RH pins: A0 - 7.

The functional block diagram depicts one of these pins with the regenerative latch. When the CMOS driver assumes the high impedance state, the latch holds the bus in whatever logic state (high or low) it was before the three-state condition. A transient drive current of ±1.5mA at VDD/2 ±0.5V for 10ns is required to switch the latch. Thus, CMOS device inputs connected to the bus are not allowed to float during three-state conditions.

* WARNING: Do not activate the Disable input by hardwiring to any TTL input pins. This is an incorrect mode of operation.

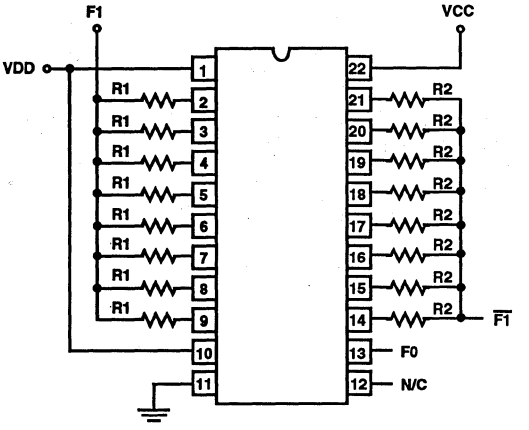
Burn-In Circuits



STATIC CONFIGURATIONS

NOTES:

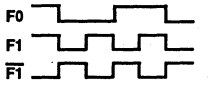
Minimum Temperature +125°C
VCC = 5.0V ±10%
VDD = 10.0V ± 10%
All Resistors R1 = 10K 1/4 watt
Static Sensitive: All Voltages Must be Ramped
ICC = 100µA
IDD = 1mA



DYNAMIC CONFIGURATION

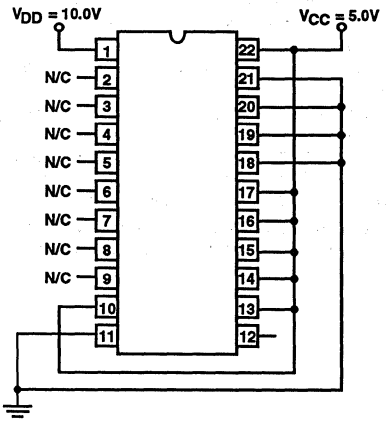
NOTES:

VDD = 10.0 ± 5%
VCC = 5V ± 10%
R1 = 10K, R2 = 2.5K



F0 + F1 are 10V Peak to Peak
F1 = 100KHz 50% Duty cycle
F0 = $\overline{F1}$ = 50KHz 50% Duty Cycle
$\overline{F1}$ is 5V Peak to Peak

Irradiation Circuit



Radiation Screening Procedure

1. A random sample of two dice per wafer is drawn from the wafer lot. Wafer identity is retained.
2. The sample die shall be assembled and tested for functionality, in a ceramic dip.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Ras(Si) +10% from a Gammacell 220 cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with VSUPPLY = +5V. The dose rate shall be between 50 rads/sec and 300 rads/sec.
4. The Irradiation Bias circuit is shown to the left.
5. The sample devices shall be started into test within 1 hour of irradiation and have completed test within 2 hours of irradiation. The wafers are accepted only if the sample, exclusive of non-radiation failures, meets all electrical specifications at room temperature.
6. Radiation screening to a higher total dose is available. Customers should contact their closest Harris Representative for details.

Radiation Effects

The HS-3374RH has been designed to survive in a radiation environment and to meet the electrical characteristics. Latching up free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained when special low temperature processing cycles. On a production basis, Harris performs screens for total dose hardness to a level of 1 x 10^5 Rad(Si). Transient radiation tests have shown the following results:

- Latch-up free to doses ≥ 1 x 10^{12} rads/sec*

* For operation at 10 volts and transient levels above 1 x 10^{10} Rad(Si)/s please refer to Application Note 401.

Harris - Space Level Product Flow (Note 1)

SEM - Traceable to Diffusion - Method 2018

Wafer Lot Acceptance Method 5007

Internal Visual Inspection - Method 2010, Condition A

Gamma Radiation Assurance Tests - Method 1019

Nondestructive Bond Pull - Method 2023

Customer Pre-Cap Visual Inspection (Notes 2)

Temperature Cycling - Method 1010, Condition C

Constant Acceleration - Method 2001, Condition E Min., Y1

Particle Impact Noise Detection - Method 2020, Condition A

Electrical Tests - Harris' Option

Serialization

X-Ray Inspection - Method 2012

Electrical Tests - Subgroup 1; Read and Record (T0)

Static Burn-In - Method 1015, Condition B; 72 Hours, +125°C Minimum

Electrical Tests - Subgroup 1; Read and Record (T1)

Burn-In Delta Calculation (T0-T1)

PDA Calculation 3%: Subgroup 7
5% Subgroups 1, 7, Delta

Dynamic Burn-In, Method 1015, Condition D, 240 Hours, +125°C (Note 3)

Electrical Tests - Subgroup 1; Read and Record (T2)

Alternate Group A - Subgroups 1, 7, 9; Method 5005; Paragraph 3.5.1.1

Burn-In Delta Calculation (T0-T2)

PDA Calculation 3%: Subgroup 7
5% Subgroups 1, 7, Delta

Electrical Tests - Subgroup 3; Read and Record

Alternate Group A - Subgroup 3, 8B, 11; Method 5005; Paragraph 3.5.1.1

Marking

Electrical Tests - Subgroups 2; Read and Record

Alternate Group A - Subgroups 2, 8A, 10; Method 5005; Paragraph 3.5.1.1

Fine and Gross Leak Tests - Method 1014, 100%

Customer Source Inspection (Note 2)

Group B Inspection - Method 5005 (Notes 2)
End-Point Electrical Parameters: B5; Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11

Group D Inspection - Method 5005 (Notes 2, 4)
End-Point Electrical Parameters: B5; Subgroups 1, 7, 9

External Visual Inspection - Method 2009

Data Package Generation (Note 5)

NOTES:

1. The notes of Method 5004, Table I shall apply; unless otherwise specified.
2. These steps are optional, and should be listed on the purchase order if required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table O of Method 1015.
4. For Group D, subgroup 3 inspection of package configurations which utilize a gold plated lid in its construction; the inspection criteria for illegible markings criteria of Method 1010, paragraph 3.3 and of Method 1004, paragraph 3.8.a shall not apply.
5. Data package contains: Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (includes SEM report)
   X-Ray Report and Film
   Test Variables Data

Metallization Topology

DIE DIMENSIONS:
89.4 x 76.0 x 14 ± 1mils

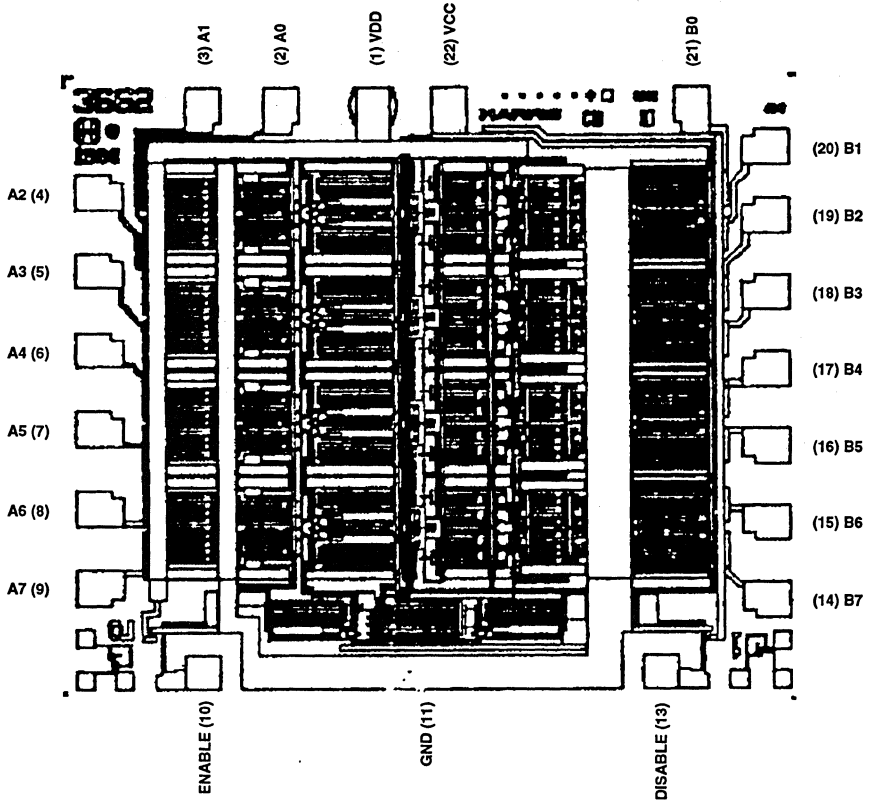
METALLIZATION:
Type: AlSi
Thickness: 8kÅ ± 1kÅ

GLASSIVATION:
Type: SiO2
Thickness: 11kÅ ± 2kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature:Ceramic DIP- 460°C (Max)

Metallization Mask Layout

HS-3374RH



HARRIS SEMICONDUCTOR

HS-54C138RH

Radiation Hardened 3-Line to 8-Line Decoder/Demultiplexer

December 1992

Features

- Radiation Hardened EPI-CMOS
  - Total Dose 1 x 10^5 RAD(Si)
  - Latch-Up Immune > 1 x 10^{12} RAD(Si)/s
- Multiple Input Enable for Easy Expansion
- Single Power Supply +5V
- Outputs Active Low
- Low Standby Power (0.5mW Max at +5V)
- High Noise Immunity
- Equivalent to Sandia SA2995
- Bus Compatible with Harris Rad-Hard 80C85RH
- Full Military Temperature Range -55°C to +125°C

Description

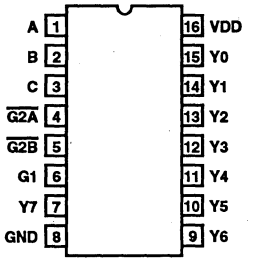
The Harris HS-54C138RH is a radiation hardened 3 to 8 decoder fabricated using a radiation hardened EPI-CMOS process. It features low power consumption, high noise immunity, and high speed. Also featured are pin and function compatibility with the 54LS138 industry standard part. The HS-54C138RH is ideally suited for high speed memory chip select address decoding. It is intended for use with the Harris HS-80C85RH radiation hardened microprocessor, but it can also be utilized as a demultiplexer in any low power rad-hard application.

The HS-54C138RH contains a one of eight binary decoder. A three bit binary input is used to select and activate each of the eight outputs, provided the three chip enable inputs are also present (see truth table).

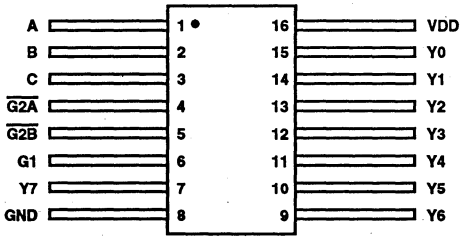
The HS-54C138RH has an on-chip enable gate. The active high (G1) and both active low ($\overline{G2A}$, $\overline{G2B}$) inputs are Anded together to provide a single enable input to the device. The use of both active high and active low inputs minimizes the need for external gates when expanding a system.

Pinouts

16 PIN DIP
CASE OUTLINE D2, CONFIGURATION 3
TOP VIEW



16 PIN FLATPACK
INTERNAL PACKAGE CODE HUV
TOP VIEW



11 µPROCESSOR PERIPHERALS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3037

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
I/O Voltage Applied ..... GND -.3V to VDD +.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	74.5°C/W	12°C/W
Flatpack Package	63.3°C/W	11°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 670mW
Flatpack Package 700mW

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.75V to +5.25V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to 1.0V
Input High Voltage ..... VDD-1.0V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current High	IIH	VDD = 5.25V, VIN = 0V, Pin Under Test = VDD	1, 2, 3	-55°C, +25°C, +125°C	-	1	µA
Input Leakage Current Low	IIL	VDD = 5.25V, VIN = 5.25V, Pin Under Test = 0V	1, 2, 3	-55°C, +25°C	-1	-	µA
High Level Output Voltage	VOH	VDD = 4.75V, IIN = -2mA	1, 2, 3	-55°C, +25°C, +125°C	4.25	-	V
Low Level Output Voltage	VOL	VDD = 5.25V, IIN = 2mA	1, 2, 3	-55°C, +25°C, +125°C	0.5	-	V
Static Current	SIDD	VDD = 5.25V, VIN = GND	1, 2, 3	-55°C, +25°C, +125°C	-	100	µA
Functional Tests	FT	VDD = 5.25V and 4.75V, VIH = VDD - 1.0V, VIL = 1.0V	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-

NOTE: All devices are guaranteed at worst case limits and conditions.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
SELECT TO OUTPUT PROPAGATION DELAY TIME						
Low to high level input, High to low level output	TPHL11	9, 10, 11	-55°C, +25°C, +125°C	-	110	ns
Low to high level input, Low to high level output	TPLH11	9, 10, 11	-55°C, +25°C, +125°C	-	65	ns
High to low level input, Low to high level output	TPLH12	9, 10, 11	-55°C, +25°C, +125°C	-	75	ns
High to low level input, high to low level output	TPHL12	9, 10, 11	-55°C, +25°C, +125°C	-	90	ns
ENABLE TO OUTPUT PROPAGATION DELAY TIME						
Low to high level input, Low to high level output	TPLH21	9, 10, 11	-55°C, +25°C, +125°C	-	70	ns
Low to high level input, High to low level output	TPHL21	9, 10, 11	-55°C, +25°C, +125°C	-	105	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
High to low level input, Low to high level output	TPLH22	9, 10, 11	-55°C, +25°C, +125°C	-	70	ns
High to low level input, High to low level output	TPHL22	9, 10, 11	-55°C, +25°C, +125°C	-	105	ns

NOTE: Output timings are measured with a capacitive load, CL = 100pF, VIH = 3.75V, and VIL = 1.0V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Input Capacitance	CIN	VDD = Open, f = 1MHz, All Measurements Referenced to Device Ground	+25°C	-	10	pF
Output Capcitance	COUT	VDD = Open, f = 1MHz, All Measurements Referenced to Device Ground	+25°C	-	10	pF

NOTE: The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The Post Irradiation test conditions and limits are the same as those listed in Table 1 and Table 2.

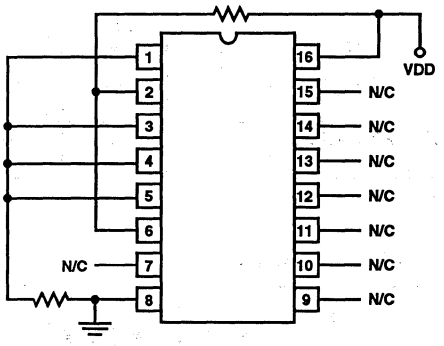
TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Static Current	SIDD	±30µA
Low Input Leakage Current	IIL	±100nA
High Input Leakage Current	IIH	±100nA
Low Level Output Voltage	VOL	±60mV
High Level Output Voltage	VOH	±400mV

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	-8 SUBGROUPS
Initial Test	100%/5004	1, 7, 9
PDA	100%/5004	1, 7
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group C	Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group D Others	Samples/5004	1, 7
Group E Subgroup 2	Samples/5004	1, 7, 9

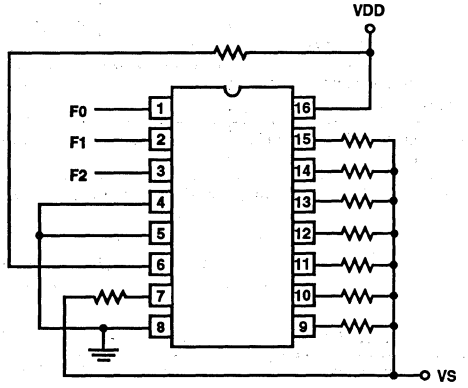
Burn-In Circuits



STATIC CONFIGURATIONS

NOTES:

Minimum Temperature = +125°C, VDD = 10V ± 5%
All Resistors 10KΩ, 1/4W

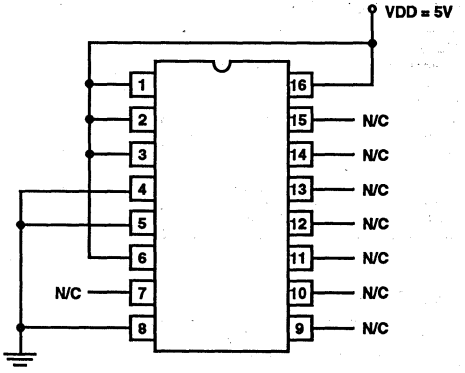


DYNAMIC CONFIGURATION

NOTES:

VDD = 10.0V ± 5%
VS = 5V ± 10%
T_A Min = +125°C
All resistors are 10KΩ ± 10%, 1/4W
F0 = 1MHz, 50% Duty Cycle
F1 = F0/2, F2 = F1/2

Irradiation Circuit



NOTES:

VDD = 5.0V ± 0.5V
Group E Testing Performed in Ceramic DIP
Group E Sample Size is 2 die/wafer

Radiation Screening Procedure

1. A random sample of two dice per wafer is drawn from the wafer lot. Wafer identity is retained.
2. The sample die shall be assembled and tested for functionality, in a ceramic dip.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1 x 105 Ras(Si) +10% from a Gammacell 220 cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with VSUPPLY = +5V. The dose rate shall be between 50 rads/sec and 300 rads/sec.
4. The Irradiation Bias circuit is shown to the left.
5. The sample devices shall be started into test within 1 hour of irradiation and have completed test within 2 hours of irradiation. The wafers are accepted only if the sample, exclusive of non-radiation failures, meets all electrical specifications at room temperature.
6. Radiation screening to a higher total dose is available. Customers should contact their closest Harris Representative for details.

Radiation Effects

The HS-54C138RH has been designed to survive in a radiation environment and to meet the electrical characteristics. Latching up free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained when special low temperature processing cycles. On a production basis, Harris performs screens for total dose hardness to a level of 1 x 10^5 Rad(Si). Transient radiation tests have shown the following results:

- Latch-up free to doses ≥ 1 x 10^{12} rads/sec.
- Upset (loss of stored data) ≥ 1 x 10^8 rads/sec.

Harris - Space Level Product Flow (Note 1)

SEM - Traceable to Diffusion - Method 2018

Wafer Lot Acceptance Method 5007

Internal Visual Inspection - Method 2010, Condition A

Gamma Radiation Assurance Tests - Method 1019

Nondestructive Bond Pull - Method 2023

Customer Pre-Cap Visual Inspection (Notes 2)

Temperature Cycling - Method 1010, Condition C

Constant Acceleration - Method 2001, Condition E Min., Y1

Particle Impact Noise Detection - Method 2020, Condition A

Electrical Tests - Harris' Option

Serialization

X-Ray Inspection - Method 2012

Electrical Tests - Subgroup 1; Read and Record (T0)

Static Burn-In - Method 1015, Condition B, 72 Hours, +125°C Minimum

Electrical Tests - Subgroup 1; Read and Record (T1)

Burn-In Delta Calculation (T0-T1)

PDA Calculation 3%: Subgroup 7
5% Subgroups 1, 7, Delta

Dynamic Burn-In, Method 1015, Condition D, 240 Hours, +125°C (Note 3)

Electrical Tests - Subgroup 1; Read and Record (T2)

Alternate Group A - Subgroups 1, 7, 9; Method 5005; Paragraph 3.5.1.1

Burn-In Delta Calculation (T0-T2)

PDA Calculation 3%: Subgroup 7
5% Subgroups 1, 7, Delta

Electrical Tests - Subgroup 3; Read and Record

Alternate Group A - Subgroups 3, 8B, 11; Method 5005; Paragraph 3.5.1.1

Marking

Electrical Tests - Subgroup 2; Read and Record

Alternate Group A - Subgroups 2, 8A, 10; Method 5005; Paragraph 3.5.1.1

Fine and Gross Leak Tests - Method 1014, 100%

Customer Source Inspection (Note 2)

Group B Inspection - Method 5005 (Notes 2)
End-Point Electrical Parameters: B5; Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11

Group D Inspection - Method 5005 (Notes 2, 4)
End-Point Electrical Parameters: B5; Subgroups 1, 7, 9

External Visual Inspection - Method 2009

Data Package Generation (Note 5)

NOTES:

1. The notes of Method 5004, Table I shall apply; unless otherwise specified.
2. These steps are optional, and should be listed on the purchase order if required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table O of Method 1015.
4. For Group D, subgroup 3 inspection of package configurations which utilize a gold plated lid in its construction; the inspection criteria for illegible markings criteria of Method 1010, paragraph 3.3 and of Method 1004, paragraph 3.8.a shall not apply.
5. Data package contains: Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (includes SEM report)
   X-Ray Report and Film
   Test Variables Data

Metallization Topology

DIE DIMENSIONS:
76 x 63 x 14 ± 1mils

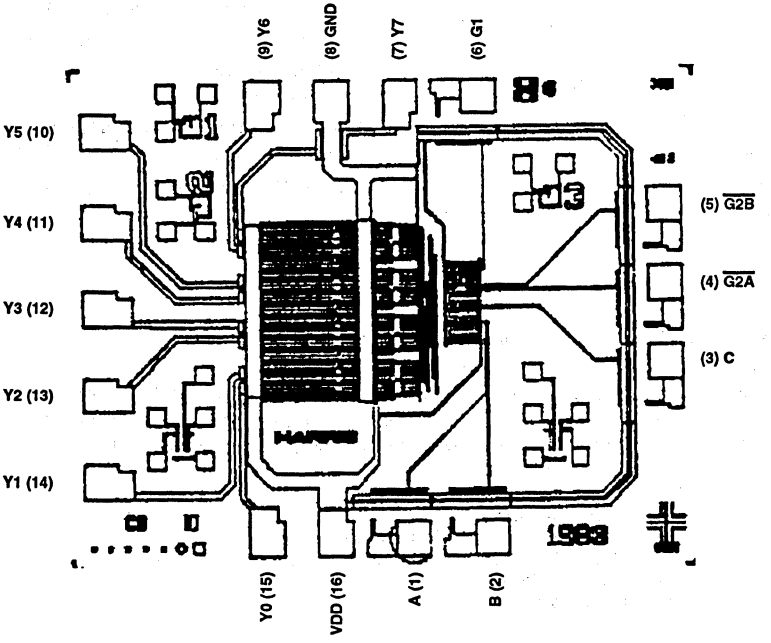
METALLIZATION:
Type: AlSi
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: SiO2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature:Ceramic DIP- 460°C (Max)

Metallization Mask Layout

HS-54C138RH



Typical applications include systems which require multiple input/output ports and memories. When the HS-54C138RH is enabled one of the eight outputs will go low. This output can be used to select a particular device or a group of devices. The HS-54C138RH can also be cascaded to provide an enabling scheme for larger systems and allow one decoder to control eight other decoders as in Figure 1.

Figure 2 shows a configuration that can be used to enable multiple I/O ports or memory devices. Up to 24 memory devices or I/O ports can be controlled using this circuit.

For demultiplexer operation, one of the three enable inputs is used as the data input while the other two inputs are enable. The transmitted data is distributed to the proper output as determined by the 3-line select inputs. See Figure 3.

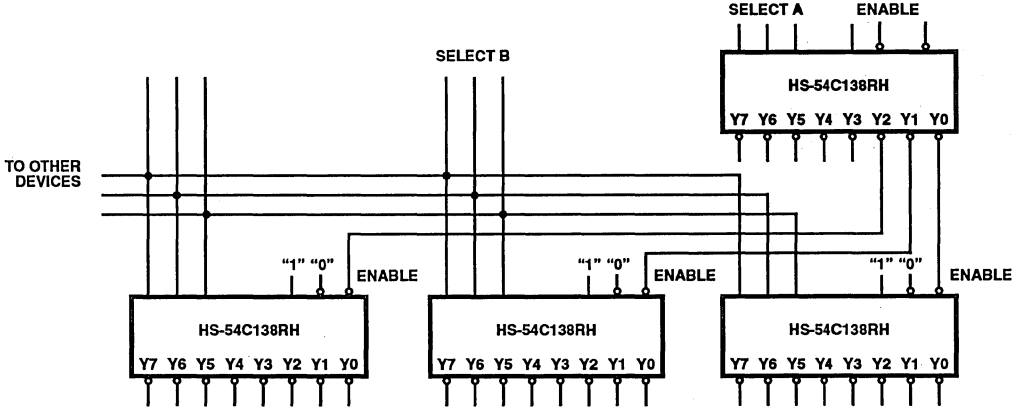


FIGURE 1

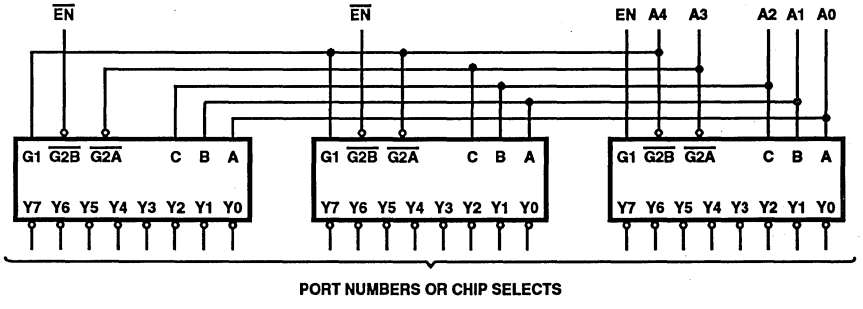


FIGURE 2

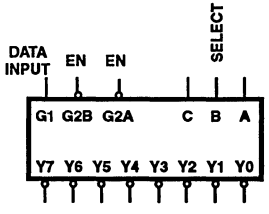


FIGURE 3

HARRIS SEMICONDUCTOR

HS-81C55RH
HS-81C56RH

Radiation Hardened 256 x 8 CMOS RAM

December 1992

Features

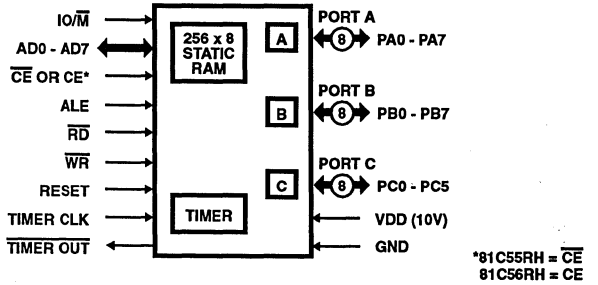
- Radiation Hardened EPI-CMOS
  - Parametrics Guaranteed 1 x 10^5 RAD(Si)
  - Transient Upset > 1 x 10^8 RAD(Si)/s
  - Latch-Up Free > 1 x 10^{12} RAD(Si)/s
- Electrically Equivalent to Sandia SA 3001
- Pin Compatible with Intel 8155/56
- Bus Compatible with HS-80C85RH
- Single 5V Power Supply
- Low Standby Current 200µA Max
- Low Operating Current 2mA/MHz
- Completely Static Design
- Internal Address Latches
- Two Programmable 8-Bit I/O Ports
- One Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter/Timer
- Multiplexed Address and Data Bus
- Self Aligned Junction Isolated (SAJI) Process
- Military Temperature Range -55°C to +125°C

Description

The HS-81C55/56RH are radiation hardened RAM and I/O chips fabricated using the Harris radiation hardened Self-Aligned Junction Isolated (SAJI) silicon gate technology. Latch-up free operation is achieved by the use of epitaxial starting material to eliminate the parasitic SCR effect seen in conventional bulk CMOS devices.

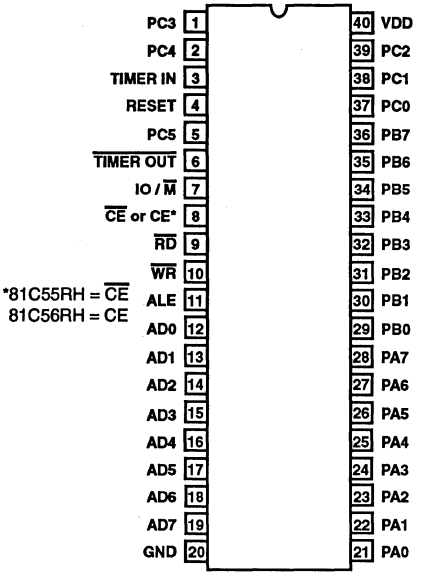
The HS-81C55/56RH is intended for use with the HS-80C85RH radiation hardened microprocessor system. The RAM portion is designed as 2048 static cells organized as 256 x 8. A maximum post irradiation access time of 500ns allows the HS-81C55/56RH to be used with the HS-80C85RH CPU without any wait states. The HS-81C55RH requires an active low chip enable while the HS-81C56RH requires an active high chip enable. These chips are designed for operation utilizing a single 5V power supply.

Functional Diagram

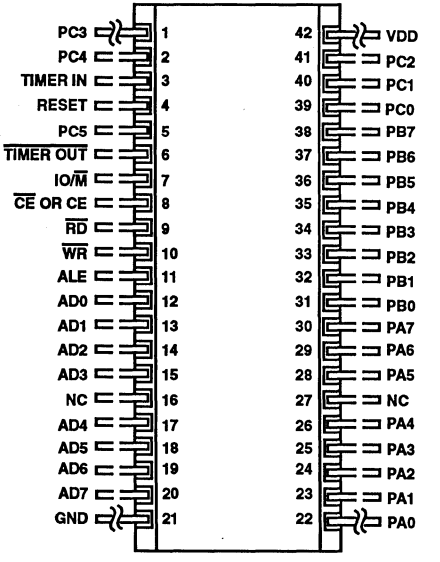


Pinouts

40 PIN CERAMIC DIP
CASE OUTLINE D5, CONFIGURATION 3
TOP VIEW



42 PIN FLATPACK
INTERNAL PACKAGE CODE HWN
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3039

Pin Description

SYMBOL	TYPE	NAME AND FUNCTION
RESET	I	**Reset:** Pulse provided by the HS-80C85RH to initialize the system (connect to HS-80C85RH RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two HS-80C85RH clock cycle times.
AD0 - AD7	I/O	**Address/Data:** Tri-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the HS-81C55 and HS-81C56RH on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/$\overline{M}$ input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{WR}$ or $\overline{RD}$ input signal.
$\overline{CE}$ or CE	I	**Chip Enable:** On the HS-81C55RH, this pin is $\overline{CE}$ and is ACTIVE LOW. On the HS-81C56RH, this pin is CE and is ACTIVE HIGH.
$\overline{RD}$	I	**Read Control:** Input low on this line with the Chip Enable active enables and AD0 - AD7 buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
$\overline{WR}$	I	**Write Control:** Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register, depending on IO/$\overline{M}$.
ALE	I	**Address Latch Enable:** This control signal latches both the address on the AD0 - AD7 lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.
IO/$\overline{M}$	I	**I/O Memory:** Selects memory if low and I/O and command/status registers if high.
PA0 - PA7 (8)	I/O	**Port A:** These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PB0 - PB7 (8)	I/O	**Port B:** These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PC0 - PC7 (8)	I/O	**Port C:** These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC0 - PC5 are used as control signals, they will provide the following: PC0 - A INTR (Port A Interrupt) PC1 - ABF (Port A Buffer Full) PC2 - $\overline{A}$ $\overline{STB}$ (Port A Strobe) PC3 - B INTR (Port B Interrupt) PC4 - B BF (Port B Buffer Full) PC5 - $\overline{B}$ $\overline{STB}$ (Port B Strobe)
TIMER IN	I	**Timer Input:** Input to the counter-timer.
$\overline{TIMER\ OUT}$	O	**Timer Output:** This output can be either a square wave or a pulse, depending on the timer mode.
VDD	I	**Voltage:** +5V.
GND	I	**Ground:** Ground reference.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage ..... GND-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 2mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	25.8°C/W	9.9°C/W
Braze Seal Flatpack Package	36.1°C/W	9.9°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package 1.94W
Braze Seal Flatpack Package 1.39W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.75V to +5.25V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... VDD -0.5V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Input Leakage Current	IIH	VDD = 5.25V, VIN = 0V, Pin under test = VDD	1, 2, 3	-55°C, +25°C, +125°C	-	1	µA
Low Input Leakage Current	IIL	VDD = 5.25V, VIN = 5.25V, Pin under test = 0V	1, 2, 3	-55°C, +25°C, +125°C	-1	-	µA
Low Output Voltage	VOL	VDD = 5.25V, IOL = 2mA	1, 2, 3	-55°C, +25°C, +125°C	-	0.5	V
High Output Voltage	VOH	VDD = 4.75V, IOH = 2mA	1, 2, 3	-55°C, +25°C, +125°C	4.25	-	V
Static Current	IDDSB	VDD = 5.25V	1, 2, 3	-55°C, +25°C, +125°C	-	200	µA
Dynamic Current	IDDOP	VDD = 5.25V, f = 1MHz	1, 2, 3	-55°C, +25°C, +125°C	-	2	mA
Functional Tests	FT	VDD = 4.75V and 5.25V, VIH = VDD-0.5V, VIL = 0.8V	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-

NOTE: All devices are guaranteed at worst case limits and over radiation. Dynamic current is proportional to operating frequency (2mA/MHz).

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Latch Setup Time	TAL	Notes 1, 4	9, 10, 11	$-55°C \le T_A \le +125°C$	60	-	ns
Address Hold Time After Latch	TLA	Notes 1, 4	9, 10, 11	$-55°C \le T_A \le +125°C$	60	-	ns
Latch to READ/WRITE Control	TLC	Notes 1, 4	9, 10, 11	$-55°C \le T_A \le +125°C$	200	-	ns
Valid Data Out From Read Control	TRD	Notes 1, 4	9, 10, 11	$-55°C \le T_A \le +125°C$	-	250	ns
Address Stable to Data Out Valid	TAD	Notes 1, 4	9, 10, 11	$-55°C \le T_A \le +125°C$	-	500	ns
Latch Enable Width	TLL	Notes 1, 4	9, 10, 11	$-55°C \le T_A \le +125°C$	200	-	ns
READ/WRITE Control to Latch Enable	TCL	Notes 1, 4,7	9, 10, 11	$-55°C \le T_A \le +125°C$	20	-	ns
READ/WRITE Control Width	TCC	Notes 1, 4	9, 10, 11	$-55°C \le T_A \le +125°C$	250	-	ns
Data In to WRITE Setup Time	TDW	Notes 1, 4	9, 10, 11	$-55°C \le T_A \le +125°C$	200	-	ns
Data In Hold Time After WRITE	TWD	Notes 1, 4	9, 10, 11	$-55°C \le T_A \le +125°C$	25	-	ns
WRITE to Port Output	TWP	Notes 1, 4	9, 10, 11	$-55°C \le T_A \le +125°C$	-	300	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Port Input Setup Time	TPR	Notes 1, 4	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	50	-	ns
Port Input Hold Time	TRP	Notes 1, 4	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	15	-	ns
Strobe to Buffer Full	TSBF	Notes 1, 4	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	300	ns
Strobe Width	TSS	Notes 1, 4	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	150	-	ns
READ to Buffer Empty	TRBE	Notes 1, 4	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	300	ns
Strobe to INTR Off	TSI	Notes 1, 4	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	300	ns
READ to INTR Off	TRDI	Notes 1, 4	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$		360	ns
Port Setup Time to Strobe	TPSS	Notes 1, 4, 5	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	100	-	ns
Post Hold Time After Strobe	TPHS	Notes 1, 4	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	100	-	ns
Strobe to Buffer Empty	TSBE	Notes 1, 4	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	300	ns
WRITE to Buffer full	TWBF	Notes 1, 4	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	300	ns
WRITE to INTR Off	TWI	Notes 1, 4	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	340	ns
TIMER-IN to TIMER OUT Low	TTL	Notes 1, 4	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	300	ns
TIMER-IN to TIMER-OUT High	TTH	Notes 1, 4	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	300	ns
Data Bus Enable from READ Control	TRDE	Notes 1, 4	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	120	-	ns
TIMER-IN Low Time	T1	Notes 1, 4, 6	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	40	-	ns
TIMER-IN High Time	T2	Notes 1, 4	9, 10, 11	$-55^{\circ}C \le T_A \le +125^{\circ}C$	115	-	ns

NOTES:

1. All devices guaranteed at worst case limits and over radiation.
2. Operating supply current (IDDOP) is proportional to operating frequency.
3. Output timings are measured with purely capacitive load.
4. For design purposes the limits are given as shown. For compatibility with the 80C85RH microprocessor, the AC parameters are tested as maximums.
5. Parameter tested as part of the functional test. No read and record data available.
6. At low temperature, T1 is measured down to 10ns. If the reading is less than 10ns, the parameter will read 10ns.
7. Read and Record data available on failing data only.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz, All measurements referenced to device ground	$T_A = +25^{\circ}C$	-	10	pF
I/O Capacitance	CI/O	VDD = Open, f = 1MHz, All measurements referenced to device ground	$T_A = +25^{\circ}C$	-	12	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz, All measurements referenced to device ground	$T_A = +25^{\circ}C$	-	10	pF
Data Bus Float After READ	TRDF	VDD = 4.75V	$-55^{\circ}C$, $+25^{\circ}C$, $+125^{\circ}C$	10	100	ns
Recovery Time Between Controls	TRV	VDD = 4.75V	$-55^{\circ}C$, $+25^{\circ}C$, $+125^{\circ}C$	-	220	ns

NOTE: The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The Post Irradiation test conditions and limits are the same as those listed in Table 1 and Table 2.

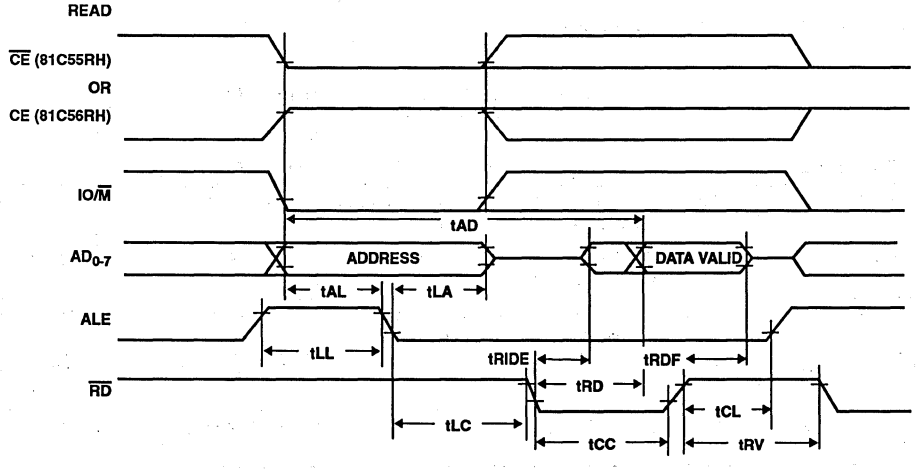
TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Static Current	IDDSB	±40µA
Low Input Leakage Current	IIL	±100nA
High Input Leakage Current	IIH	±100nA
Low Level Output Voltage	VOL	±60mV
High Level Output Voltage	VOH	±400mV

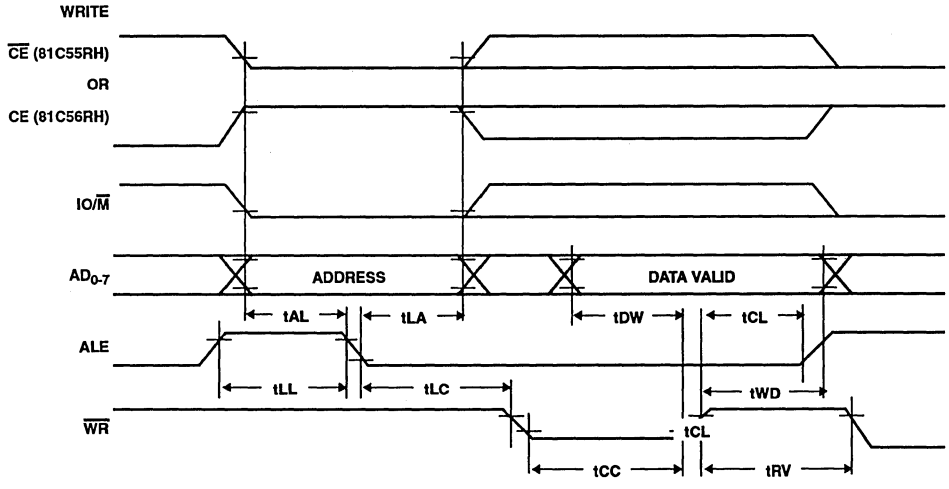
TABLE 6. APPLICABLE SUBGROUPS

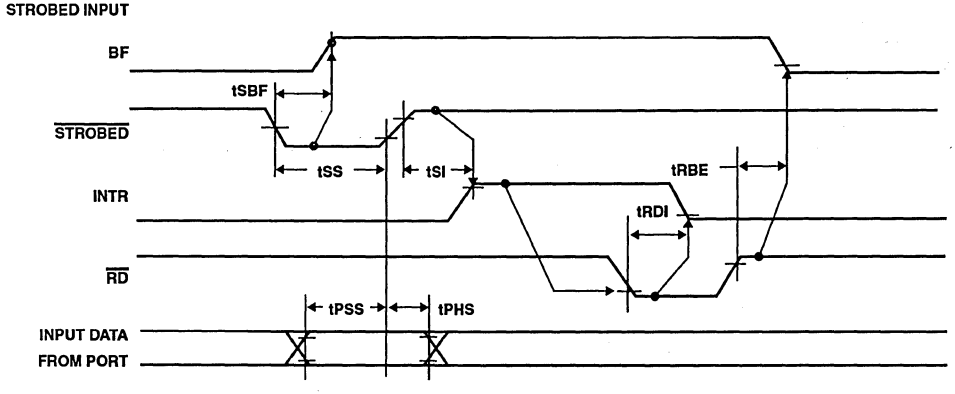
CONFORMANCE GROUPS	METHOD	-8 SUBGROUPS
Initial Test	100%/5004	1, 7, 9
PDA	100%/5004	1, 7
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group C	Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group D Others	Samples/5004	1, 7
Group E Subgroup 2	Samples/5004	1, 7, 9

Waveforms



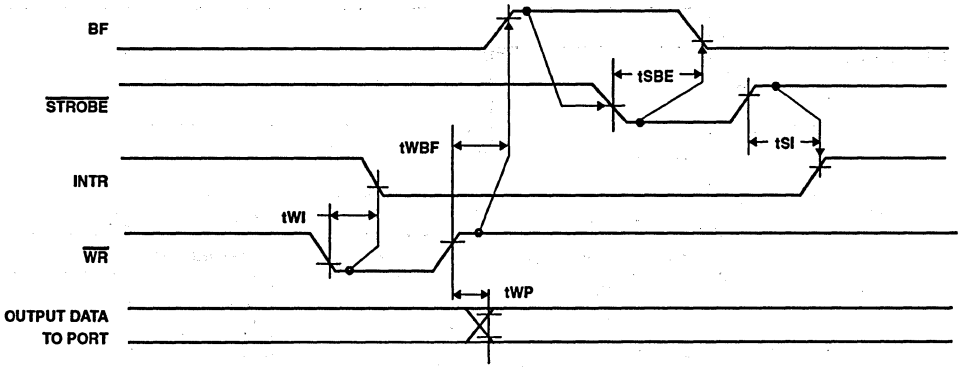
Waveforms (Continued)



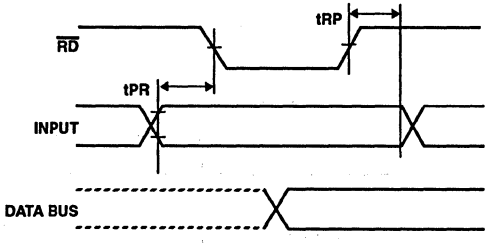


Waveforms (Continued)

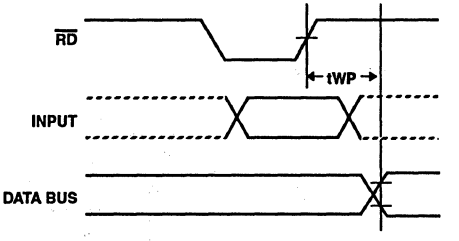
STROBED OUTPUT



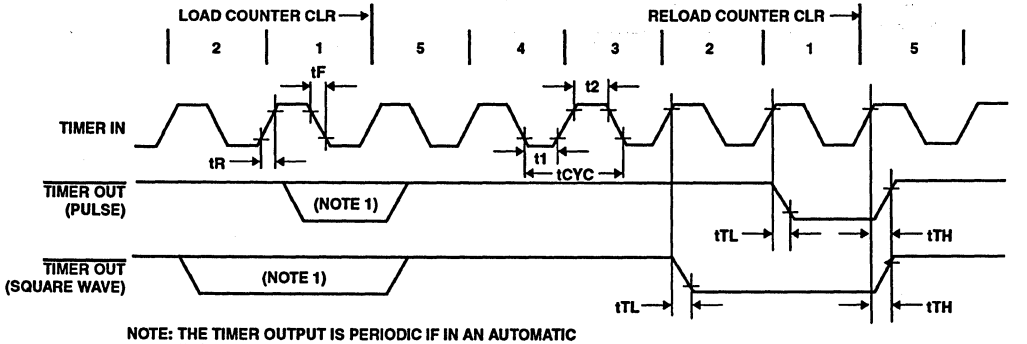
BASIC INPUT



BASIC INPUT



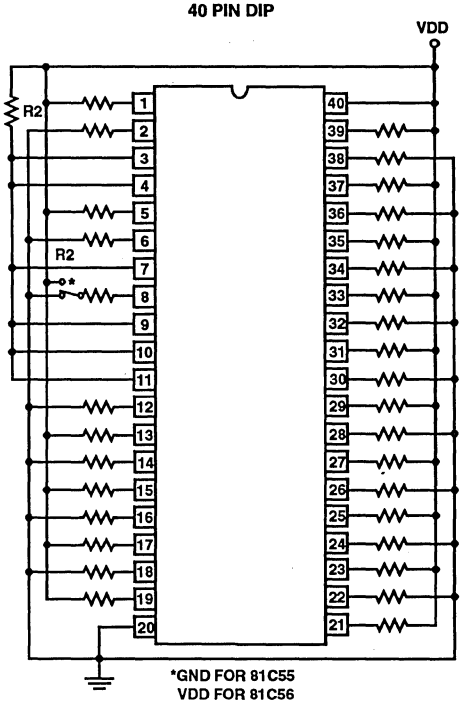
TIMER OUTPUT COUNTDOWN FROM 5 TO 1



NOTE: THE TIMER OUTPUT IS PERIODIC IF IN AN AUTOMATIC RELOAD MODE (M, MODE BIT = 1)

Burn-In Circuits

40 PIN DIP

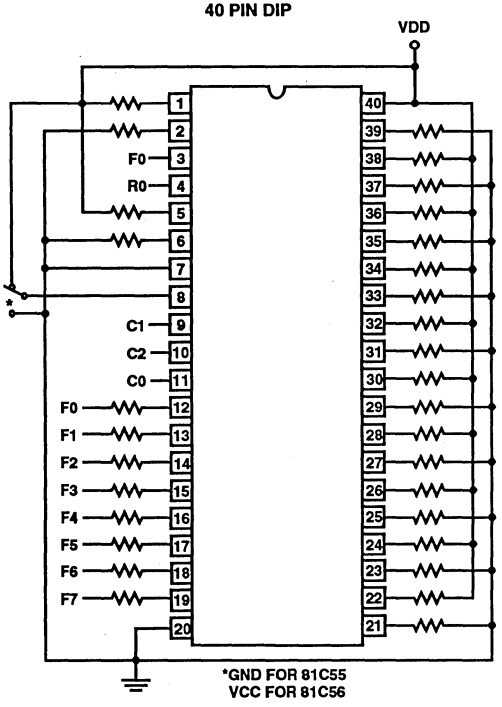


STATIC CONFIGURATION

NOTES:

VDD = 10V ± 10%
All resistors R1 = 100kΩ unless otherwise marked: R2 = 50K
Pin 8 tied through a resistor to two position switch.
Label ground side "81C55" and VDD side "81C56".

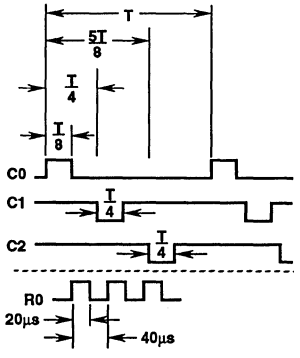
40 PIN DIP



DYNAMIC CONFIGURATION

NOTES:

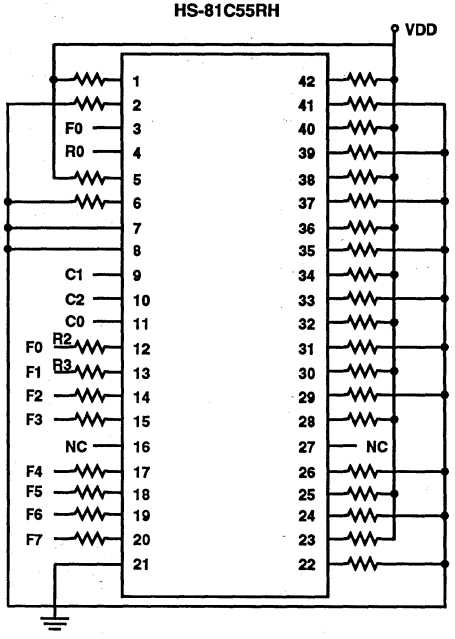
Minimum Temperature +125°C
All resistors 100kΩ 1/4 Watt. VDD = 10V ± 10%.
Pin 8 tied to two position switch. Label ground side "81C55" and VDD side "81C56".
Period of C0 = C1 = C2 = T = 10µs
C0 active HIGH, C1 and C2 active LOW.
C0, C1, C2 cannot overlap each other.
R0 shall have at least 3 pulses on power up as indicated below.
Pulses shall stop and R0 shall go to 0V no more than 60 seconds after power-up.



SIGNAL NAME	FREQUENCY	DUTY CYCLE
F0	50KHz	50%
F1	F0/2	50%
F2	F1/2	50%
F3	F2/2	50%
F4	F3/2	50%
F5	F4/2	50%
F6	F5/2	50%
F7	F6/2	50%

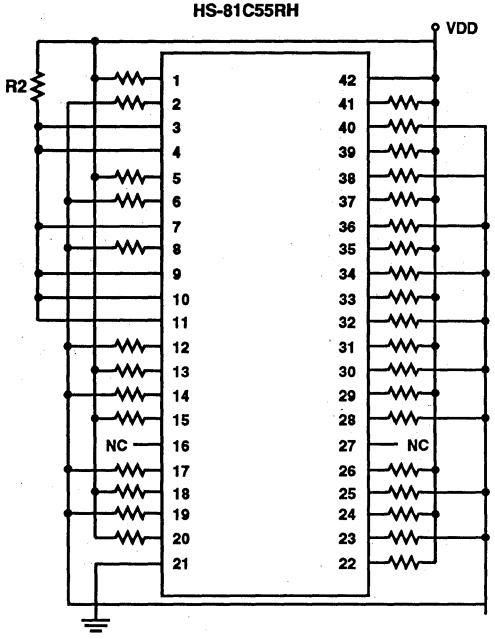
Burn-In Circuits (Continued)

42 PIN FLATPACK
HS-81C55RH



STATIC CONFIGURATION

42 PIN FLATPACK
HS-81C55RH



DYNAMIC CONFIGURATION

Radiation Screening Procedure

1. A random sample of two dice per wafer is drawn from the wafer lot. Wafer identity is retained.
2. The sample die shall be assembled and tested for functionality, in a ceramic dip.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1 x 105 Ras(Si) +10% from a Gamma-cell 220 cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with VSUPPLY = +5V. The dose rate shall be between 50 rads/sec and 300 rads/sec.
4. The Irradiation Bias circuit is shown.
5. The sample devices shall bestarted into test within 1 hour of irradiation and have completed test within 2 hours of irradiation. The wafers are accepted only if the sample, exclusive of non-radiation failures, meets all electrical specifications at room temperature.
6. Radiation screening to a higher total dose is available. Customers should contact their closest Harris Representative for details.

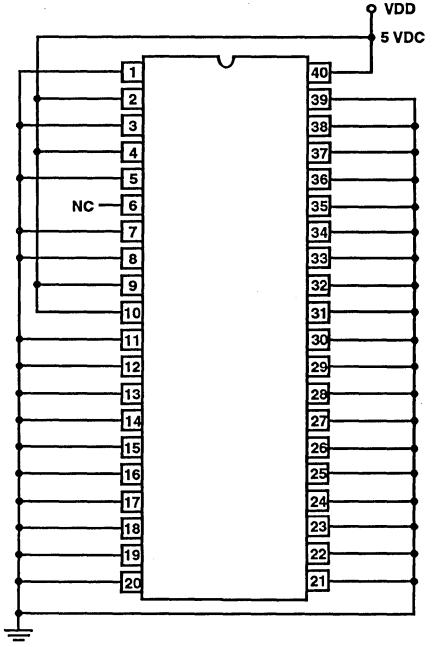
Radiation Effects

The HS-81C55RH and HS-81C56RH has been designed to survive in a radiation environment and to meet the electrical characteristics. Latching up free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained when special low temperature processing cycles. On a production basis, Harris performs screens for total dose hardness to a level of 1 x 10^5 Rad(Si). Transient radiation tests have shown the following results:

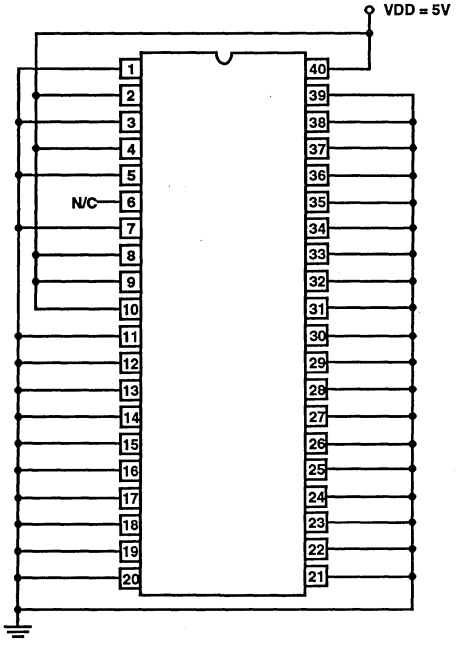
- Latch-up free to doses ≥ 1 x 10^{12} rads/sec.
- Upset (loss of stored data) ≥ 1 x 10^8 rads/sec.

Irradiation Circuits

HS-81C55RH



HS-81C56RH



Harris - Space Level Product Flow (Note 1)

SEM - Traceable to Diffusion - Method 2018

Wafer Lot Acceptance Method 5007

Internal Visual Inspection - Method 2010, Condition A

Gamma Radiation Assurance Tests - Method 1019

Nondestructive Bond Pull - Method 2023

Customer Pre-Cap Visual Inspection (Notes 2)

Temperature Cycling - Method 1010, Condition C

Constant Acceleration - Method 2001, Condition E Min., Y1

Particle Impact Noise Detection - Method 2020, Condition A

Electrical Tests - Harris' Option

Serialization

X-Ray Inspection - Method 2012

Electrical Tests - Subgroup 1; Read and Record (T0)

Static Burn-In - Method 1015, Condition B, 72 Hours, +125°C Minimum

Electrical Tests - Subgroup 1; Read and Record (T1)

Burn-In Delta Calculation (T0-T1)

PDA Calculation 3%: Subgroup 7
5% Subgroups 1, 7, Delta

Dynamic Burn-In, Method 1015, Condition D, 240 Hours, +125°C (Note 3)

Electrical Tests - Subgroup 1; Read and Record (T2)

Alternate Group A - Subgroups 1, 7, 9; Method 5005; Paragraph 3.5.1.1

Burn-In Delta Calculation (T0-T2)

PDA Calculation 3%: Subgroup 7
5% Subgroups 1, 7, Delta

Electrical Tests - Subgroup 3; Read and Record

Alternate Group A - Subgroups 3, 8B, 11; Method 5005; Paragraph 3.5.1.1

Marking

Electrical Tests - Subgroup 2; Read and Record

Alternate Group A - Subgroups 2, 8A, 10; Method 5005; Paragraph 3.5.1.1

Fine and Gross Leak Tests - Method 1014, 100%

Customer Source Inspection (Note 2)

Group B Inspection - Method 5005 (Notes 2)
End-Point Electrical Parameters: B5; Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11

Group D Inspection - Method 5005 (Notes 2, 4)
End-Point Electrical Parameters: B5; Subgroups 1, 7, 9

External Visual Inspection - Method 2009

Data Package Generation (Note 5)

NOTES:

1. The notes of Method 5004, Table I shall apply; unless otherwise specified.
2. These steps are optional, and should be listed on the purchase order if required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table O of Method 1015.
4. For Group D, subgroup 3 inspection of package configurations which utilize a gold plated lid in its construction; the inspection criteria for illegible markings criteria of Method 1010, paragraph 3.3 and of Method 1004, paragraph 3.8.a shall not apply.
5. Data package contains: Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (includes SEM report)
   X-Ray Report and Film
   Test Variables Data

Metallization Topology

DIE DIMENSIONS:
76 x 63 x 14 ± 1mils

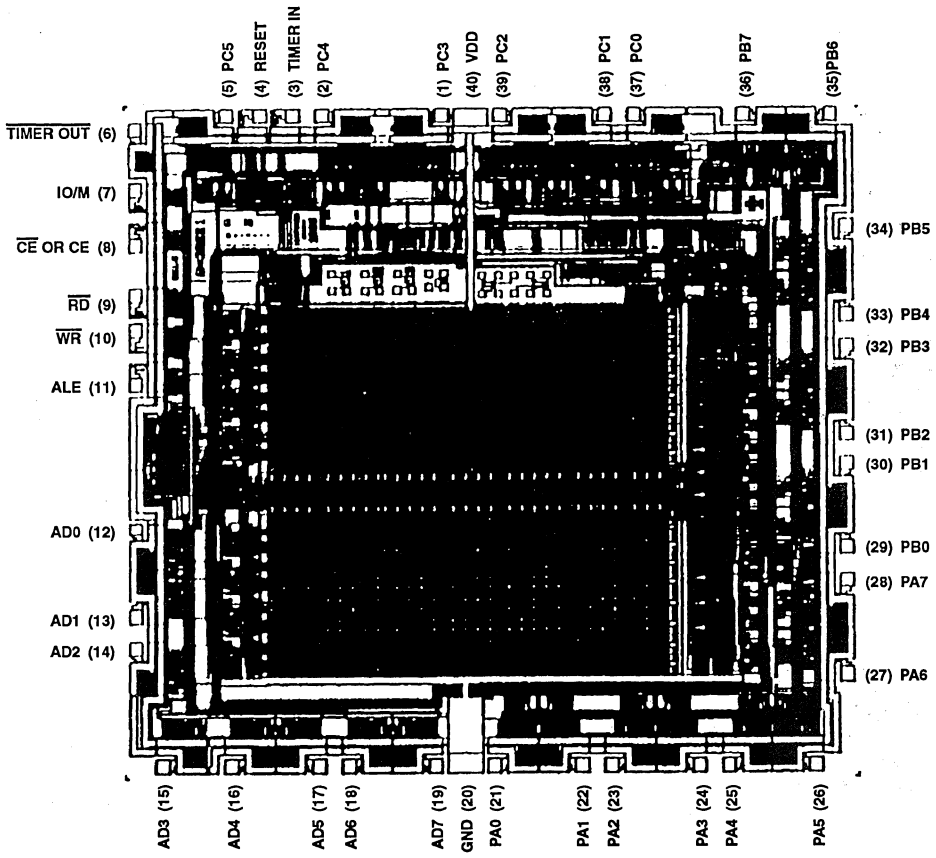
METALLIZATION:
Type: AlSi
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: SiO2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature:Ceramic DIP- 460°C (Max)

Metallization Mask Layout

HS-81C55RH, HS-81C56RH



Functional Description

The HS-81C55RH and 81C56RH contains the following:

- 2K Bit Static RAM Organized as 256 x 8
- Two 8-Bit I/O Ports (PA and PB) and One 6-Bit I/O Port (PC)
- 14-Bit Timer-Counter

The IO/$\overline{M}$ (IO/Memory Select) pin selects either the five register (Command, Status, PA0 - PA7, PB0 - PB7, PC0 - PC5) or the memory (RAM) portion.

The 8-bit address on the Address/Data lines, Chip Enable input $\overline{CE}$ or CE and IO/$\overline{M}$ are all latched on-chip at the falling edge of ALE.

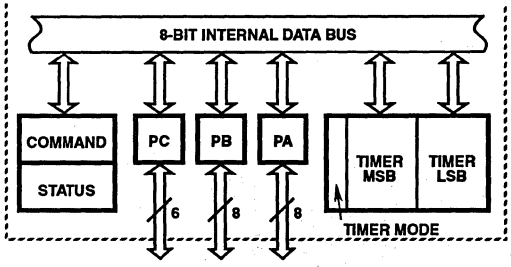


FIGURE 1. INTERNAL REGISTERS

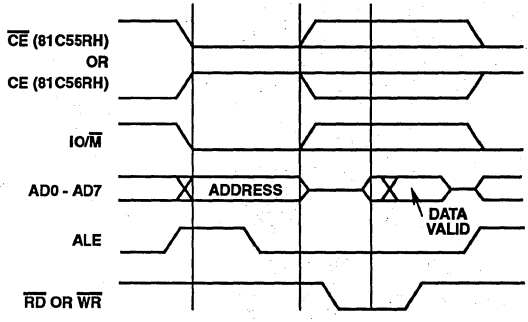


FIGURE 2. ON-BOARD MEMORY READ/WRITE CYCLE

Programming of the Command Register

The command register consists of eight latches. Four bits (0-3) define the mode of the ports, two bit (4-5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6-7) are for the timer.

The command register contents can be altered at anytime by using the I/O address XXXXX000 during a WRITE operation with the Chip Enable active and IO/$\overline{M}$ = 1. The meaning of each bit of the command byte is defined in Figure 3. The contents of the command register may never be read.

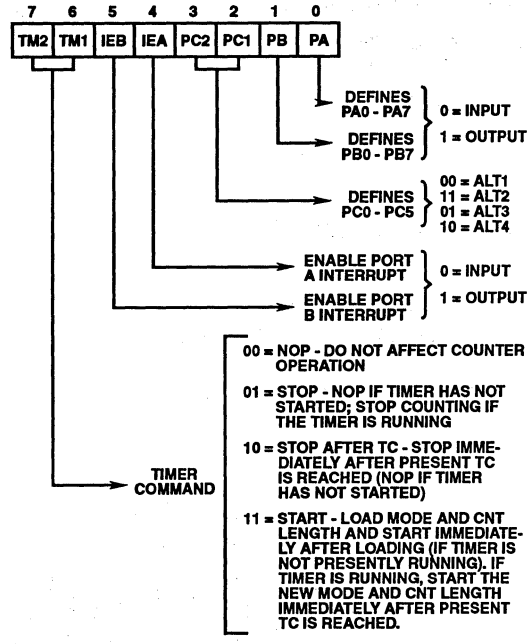


FIGURE 3. COMMAND REGISTER BIT ASSIGNMENT

Reading the Status Register

The status register consists of seven latches, one for each bit six (0-5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the Status Register (Address XXXXX000). Status word format is shown in Figure 4. Note that you may never write to the status register since the command register shares the same I/O address and the command register is selected when a write to that address is issued.

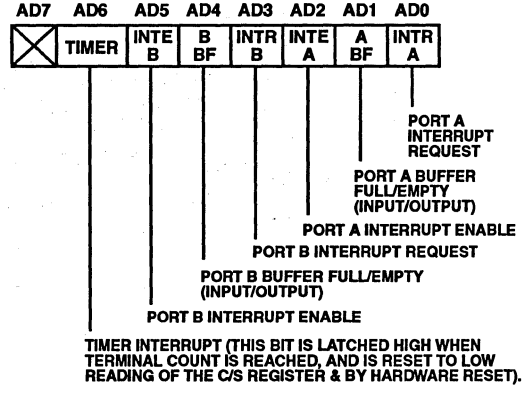


FIGURE 4. STATUS REGISTER BIT ASSIGNMENT

Input/Output Section

The I/O section of the HS-81C55RH and HS-81C56RH consists of five registers: (See Figure 5)

- **Command/Status Register (C/S)** - Both register are assigned the address XXXXX000. The C/S address serves the dual prupose.

  When the C/S registers are selected during WRITE operation, a command is written into the command register. The contents of this register are not accessible through the pins.

  When the C/S (XXXXX000) is selected during a READ operation, the status information of the I/O ports and the timer becomes available on the AD0 - AD7 lines.

- **PA Register** - This register can be programmed to be either input or output ports depending on the status of the contents of the C/S Register. also depending on the command, this port can operate in either the basic mode or the strobed mode (See timing diagram). the I/O pins assigned in relation to this register are PA0 - PA7. The address of this register is XXXXX001.

- **PB Register** - This register functions the same as PA Register. the I/O pins assigned are PB0 - PB7. The address of this register is XXXXX010

- **PC Register** - This register has the address XXXXX011 and contains only 6 bits. The 6 bits can be programmed to be either input ports, output ports or as control signals for PA and PB by properly programming the AD2 and AD3 bits of the C/S register.

  When PC0 - PC5 is used as a control port, 3 bits are assigned for Port A and 3 for Port B. The first bit is an Interrupt that the HS-81C55RH and HS-81C56RH sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode. (See Table 1).

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and Pb are initialized as follows: :

CONTROL	INPUT MODE	OUTPUT MODE
BF	Low	Low
INTR	Low	High
STB	Input Control	Input Control

I/O ADDRESS†								
A7	A6	A5	A4	A3	A2	A1	A0	SELECTION
X	X	X	X	X	0	0	0	Interval Command/ Status Register
X	X	X	X	X	0	0	1	General Purpose I/O Port A
X	X	X	X	X	0	1	0	General Purpose I/O Port B
X	X	X	X	X	0	1	1	General Purpose I/O or Control Port C
X	X	X	X	X	1	0	0	Low-Order 8 Bits of Timer Count
X	X	X	X	X	1	0	1	High 6 Bits of Timer Count and 2 Bits of Timer Mode

† I/O Address must be qualified by CE = 1(81C56RH) or $\overline{CE}$ = 0(81C55RH) and IO/$\overline{M}$ = 1 in order to select the appropriate register.
X = Don't Care

FIGURE 5. I/O PORT AND TIMER ADDRESSING SCHEME

Figure 6 shows how I/O Ports A and B are structured within the HS-81C55RH and HS-81C56RH.

Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

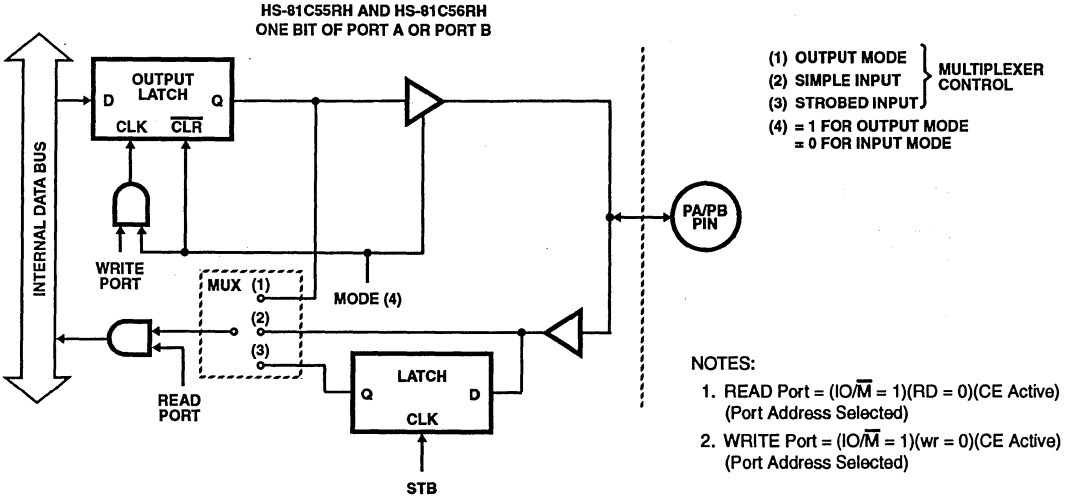


FIGURE 6. HS-81C55RH AND HS-81C56RH PORT FUNCTION

The outputs of the HS-81C55/56RH are "glitch-free" meaning that you can write a "1" to a bit position that was previously "1" and the level at the output pin will not change.

Note also that the output latch is cleared when the port enters the input mode. the output latch cannot be loaded by writing to the port if the port is in theinput mode. The result is that each time a port mode is changed from input to output, the output pins will go low. When the HS-81C55/56RH is RESET, the output latches are all cleared and all 3 ports enter the input mode.

When in the ALT1 or ALT2 modes, the bits of Port C are structured like the diagram above in the simple input or output mode, respectively.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

Figure 7 shows how the HS-81C55/56RH I/O ports might be configured in a typical system.

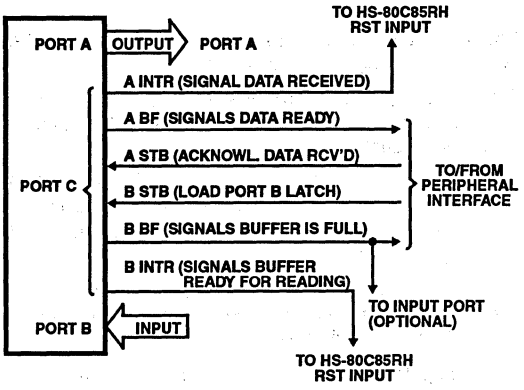


FIGURE 7. EXAMPLE: COMMAND REGISTER = 00111001

Timer Section

The timer is a 14 bit down counter that counts the TIMER IN pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register. (See Figure 5).

To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits 0-13 of the high order count register will specify the length of the next count and bits 14-15 of the high order register will specify the timer output mode (see Figure 8). The value loaded into the count length register can have any value from 2H through 3FFH in Bits 0-13.

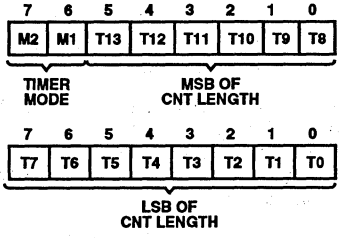


FIGURE 8. TIMER FORMAT

TABLE 1. PORT CONTROL ASSIGNMENT

PIN	ALT1	ALT2	ALT3	ALT4
PC0	Input Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
PC1	Input Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
PC2	Input Port	Output Port	A STB (Port A Strobe)	A STB (Port A Strobe)
PC3	Input Port	Output Port	Output Port	B INTR (Port B Interrupt)
PC4	Input Port	Output Port	Output Port	B BF (Port B Buffer Full)
PC5	Input Port	Output Port	Output Port	B STB (Port B Strobe)

There are four modes to choose from: M2 and M1 define the timer mode, as shown in Figure 9.

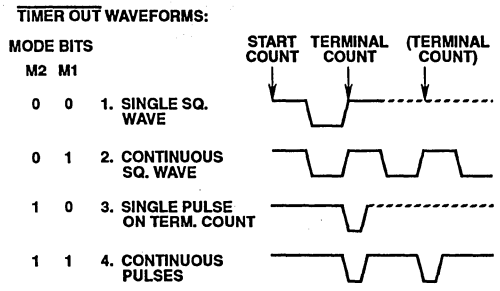


FIGURE 9. TIMER MODES

Bits 6-7 (TM2 and TM1) of command register contents are used to start and stop the counter. there are four commands to choose from:

TM2	TM1	
0	0	NOP - Do not affect counter operation
0	1	STOP-NOP - If timer has not started; stop counting if the timer is running
1	0	STOP AFTER TC - Stop immediately after present TC is reached (NOP if timer has not started)
1	1	START - Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached.

Note that while the counter is counting, you may load a new count and mode into the count length registers. Before the new count and mode will be used by the counter, you *must* issue a START command to the counter. This applies even thought you may only want to change the count and use the previous mode.

In case of an odd-numbered count, the first half-cycle of the squarewave output, which is high, is one count longer than the second (low) half-cycle, as shown in Figure 10.

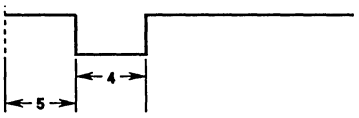


FIGURE 10. ASYMMETRICAL SQUARE-WAVE OUTPUT RESULTING FROM COUNT OF 9

The counter in the HS-81C55/56RH is not initialized to any particular mode or count when hardware RESET occurs, but RESET does stop the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

Please note that the timer circuit on the HS-81C55/56RH chip is designed to be a square-wave timer, not an event counter. To achieve this, it counts down by twos twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulses received. You cannot load an initial value of 1 into the count register and cause the timer to operate, as its terminal count value is 10 (binary) or 2 (decimal). (For the detection of single pulses, it is suggested that one of the hardware interrupt pins on the HS-80C85RH be used.) After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulses required to complete the timer cycle if desired. To obtain the remaining count, perform the following operations in order:

1. Stop the count
2. Read in the 16 bit value from the count length registers
3. Reset the upper two mode bits
4. Reset the carry and rotate right one position all 16 bits through carry
5. If carry is set, add 1/2 of the full original count (1/2 full count - 1 if full count is odd).

NOTE: If you started with an odd count and you read the count length register before the third count pulse occurs, you will not be able to discern whether one or two counts has occurred. Regardless of this, the HS-81C55/56RH always counts out the right number of pulses in generating the TIMER OUT waveforms.

HARRIS SEMICONDUCTOR

HS-82C08RH

Radiation Hardened 8-Bit Bus Transceiver

December 1992

Features

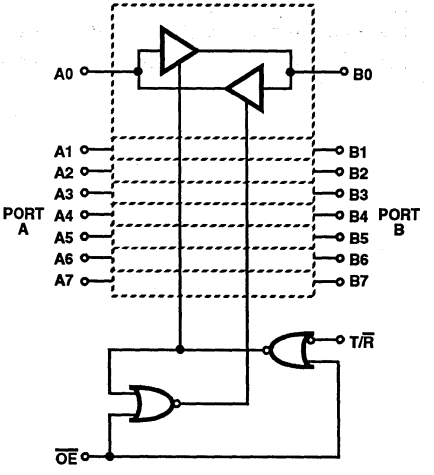
- Radiation Hardened
  - Total Dose 1 x 10^5 RAD(Si)
  - Latch-Up Immune EPI-CMOS > 1 x 10^{12} RAD(Si)/s
- Bidirectional Three-State Input/Outputs
- Low Propagation Delay Time
- Low Power Consumption
- Single Power Supply +5V
- Electrically Equivalent to Sandia SA2997
- Military Temperature Range -55°C to +125°C

Description

The Harris HS-82C08RH is a radiation-hardened octal bus transceiver with three-state outputs. It is manufactured using a self-aligned, junction isolated CMOS process and is designed for use with the HS-80C08RH radiation-hardened microprocessor. The HS-82C08RH allows asynchronous two-way communication between data buses. The direction of data flow is determined by the logic level on the transmit/receive ($T/\overline{R}$) input. A logic high on the $T/\overline{R}$ input specifies data flow from Port A to Port B of the device. Conversely, a logic low on the $T/\overline{R}$ input specifies data flow from Port B to Port A. The Output Enable input disables both ports by placing them in the high impedance state.

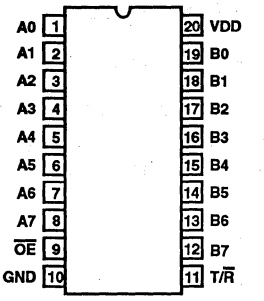
The HS-82C08RH is ideally suited for a wide variety of buffering applications in radiation-hardened microcomputer systems.

Functional Diagram

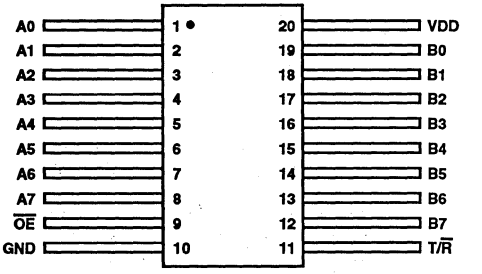


Pinouts

20 PIN CERAMIC DIP
CASE OUTLINE D8, CONFIGURATION 3
TOP VIEW



20 PIN FLATPACK
CASE OUTLINE F-9A, CONFIGURATION 2
TOP VIEW

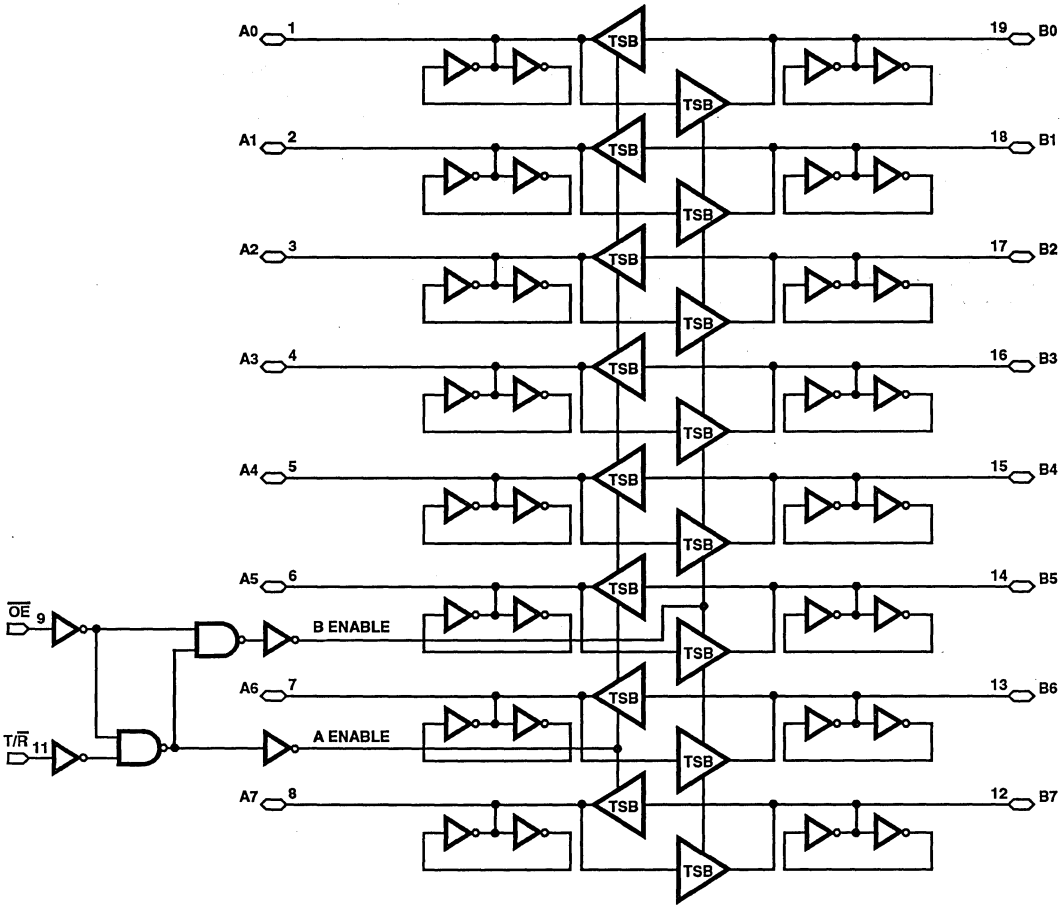


PIN	DESCRIPTION
A0-A7	Local Bus Data I/O Pins
B0-B7	System Bus Data I/O Pins
$T/\overline{R}$	Transmit/Receive Input
$\overline{OE}$	Active Low Output Enable

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3040**

Logic Diagram



NOTE: An Important caveat that is applicable to CMOS devices in general is that unused inputs should never be left floating. This rule applies to inputs connected to a three-state bus. The need for external pull-up resistors during three-state bus conditions is eliminated by the presence of regenerative latches on the following HS-82C08RH pins. A0-7 and B0-7 The functional block diagram depicts one of these pins with the regenerative latch. When the CMOS driver assumes the high impedance state, the latch holds the bus in whatever logic state (high or low) it was before the three-state condition. A transient drive current of ±1.5mA at VDD/2 ±0.5V for 10ns is required to switch the latch. Thus, CMOS device inputs connected to the bus are not allowed to float during three-state conditions.

TRUTH TABLE

INPUTS		OPERATION	
OUTPUT ENABLE	TRANSMIT/RECEIVE	PORT A	PORT B
0	0	Out	In
0	1	In	Out
1	X	High Z	High Z

X = Don't Care

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage ..... GND-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	78°C/W	12°C/W
Braze Seal FP Package	70°C/W	11°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package 0.64W
Braze Seal FP Package 0.71W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.75V to +5.25V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +1V
Input High Voltage ..... VDD -1V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

All Devices Guaranteed at Worst Case Limits and Conditions.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current	IIL	VDD = 5.25V, VIN = VDD Pin Under Test = 0V	1, 2, 3	-55°C, +25°C, +125°C	-1.0	-	µA
	IIH	VDD = 5.25V, VIN = 0V Pin Under Test = 5.25V	1, 2, 3	-55°C, +25°C, +125°C	-	1.0	µA
High Level Output Voltage	VOH	VDD = 4.75V, IOH = -2.0mA	1, 2, 3	-55°C, +25°C, +125°C	4.25	-	V
Low Level Output Voltage	VOL	VDD = 5.25V, IOL = 2.0mA	1, 2, 3	-55°C, +25°C, +125°C	-	0.5	V
Static Current	SIDD	VDD = 5.25V, VIN = GND	1, 2, 3	-55°C, +25°C, +125°C	-	100	µA
Functional Test	FT	VDD = 4.75V to 5.25V VIH = VDD -1.0V, VIL = 1.0V	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
PORT DATA/MODE SPECIFICATIONS						
Propagation Delay to Logical "1" from Port A, B to Port B, A	TPDLH	9, 10, 11	-55°C, +25°C, +125°C	-	65	ns
Propagation Delay to Logical "0" from Port A, B to Port B, A	TPDHL	9, 10, 11	-55°C, +25°C, +125°C	-	80	ns
Propagation Delay from High-Impedance to Logical "1" from T/$\overline{R}$ to Port	TPRTH	9, 10, 11	-55°C, +25°C, +125°C	-	75	ns
Propagation Delay from High-Impedance to Logical "0" from T/$\overline{R}$ to Port	TPRTL	9, 10, 11	-55°C, +25°C, +125°C	-	130	ns
Propagation Delay from High-Impedance to Logical "1" from $\overline{OE}$ to Port	TPZH	9, 10, 11	-55°C, +25°C, +125°C	-	70	ns
Propagation Delay from High-Impedance to Logical "0" from $\overline{OE}$ to Port	TPZL	9, 10, 11	-55°C, +25°C, +125°C	-	130	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE) CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
In/Out Capacitance	CI/O	VDD = Open, f = 1MHz All Measurements Referenced to GND.	+25°C	-	10	pF
TRANSMIT/RECEIVE MODE SPECIFICATIONS (AC Parameters)						
Propagation Delay from Logical "1" to High-Impedance from T/$\overline{R}$ to Port	TPHZTR		+25°C	-	35	ns
Propagation Delay from Logical "0" to High-Impedance from T/$\overline{R}$ to Port	TPLZTR		+25°C	-	35	ns
Propagation Delay from Logical "1" to High-Impedance from $\overline{OE}$ to Port	TPHZ		+25°C	-	35	ns
Propagation Delay from Logical "0" to High-Impedance from $\overline{OE}$ to Port	TPLZ		+25°C	-	35	ns

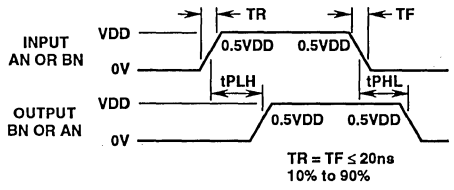
NOTE:

1. The parameters listed are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which could affect these characteristics.

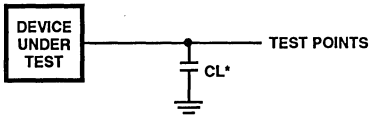
TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The Post Irradiation test conditions and limits are the same as those listed in Table 1 and Table 2.

Switching Time Waveforms

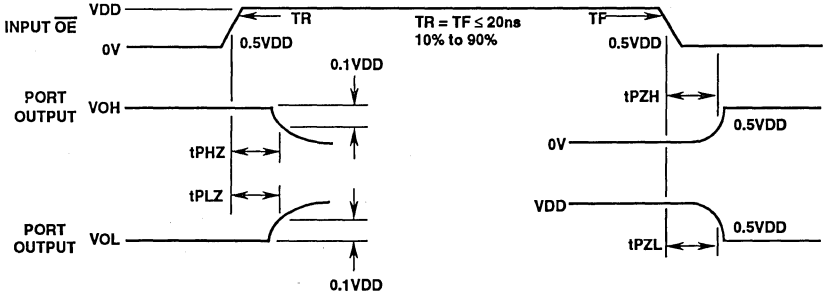


PORT TO PORT



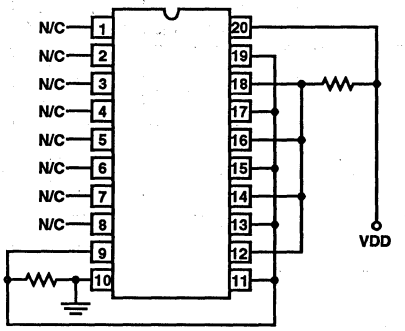
*CL INCLUDES STRAY AND JIG CAPACITANCE

AC TESTING LOAD CIRCUIT



$\overline{OE}$ TO HIGH-IMPEDANCE, $\overline{OE}$ TO PORT OUTPUT

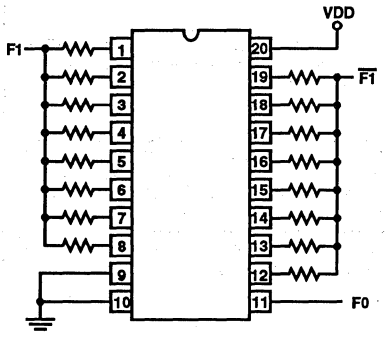
Burn-In Circuits



STATIC CONFIGURATION

NOTE:

Minimum Temperature = +125°C
VDD = 10V ± 5%
All resistors = 10kΩ, 1/4 Watt

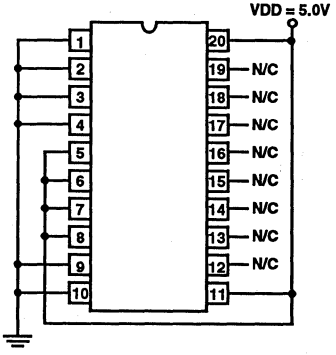


DYNAMIC CONFIGURATION

NOTE:

Minimum Temperature = +125°C, VDD = 10V ± 5%
All resistors = 10kΩ, 1/4 Watt
F1 = 100kHz, 50% Duty Cycle
F0 = F1/2, F1 = Complement of F1

Irradiation Circuits



Radiation Screening Procedure

1. A random sample of two dice per wafer is drawn from the wafer lot. Wafer identity is retained.
2. The sample die shall be assembled and tested for functionality, in a ceramic DIP.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad-Si (±10%) from a Gammacell 220 Cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with VSUPPLY = +5V. The dose rate shall be between 50 rads/sec and 300 rads/sec.
4. The Irradiation Bias circuit is shown.
5. The samples shall be started into test within 1 hour of irradiation and have completed test within 2 hours of irradiation. The wafers are accepted only if the sample, exclusive of non-radiation failures, meets all electrical specifications at room temperature.
6. Radiation screening to a higher total dose is available. Customers should contact their closest Harris Representative for details.

Radiation Effects

The HS-82C08RH has been designed to survive in a radiation environment and to meet the electrical characteristics. Latch-up free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained with special low temperature processing cycles. On a production basis, Harris performs screens for total dose hardness to a level of 1 x 10^5 Rad-Si. Transient radiation tests have shown the following results:

Latch-up free to doses ≥ 1 x 10^{12} rads/sec.

Harris - Space Level Product Flow (Note 1)

SEM - Traceable to Diffusi

on - Method 2018

Wafer Lot Acceptance Method 5007

Internal Visual Inspection - Method 2010, Condition A

Gamma Radiation Assurance Tests - Method 1019

Nondestructive Bond Pull - Method 2023

Customer Pre-Cap Visual Inspection (Notes 2)

Temperature Cycling - Method 1010, Condition C

Constant Acceleration - Method 2001, Condition E Min., Y1

Particle Impact Noise Detection - Method 2020, Condition A

Electrical Tests - Harris' Option

Serialization

X-Ray Inspection - Method 2012

Electrical Tests - Subgroup 1; Read and Record (T0)

Static Burn-In - Method 1015, Condition B, 72 Hours, +125°C Minimum

Electrical Tests - Subgroup 1; Read and Record (T1)

Burn-In Delta Calculation (T0-T1)

PDA Calculation 3%: Subgroup 7
5% Subgroups 1, 7, Delta

Dynamic Burn-In, Method 1015, Condition D, 240 Hours, +125°C (Note 3)

Electrical Tests - Subgroup 1; Read and Record (T2)

Alternate Group A - Subgroups 1, 7, 9; Method 5005; Paragraph 3.5.1.1

Burn-In Delta Calculation (T0-T2)

PDA Calculation 3%: Subgroup 7
5% Subgroups 1, 7, Delta

Electrical Tests - Subgroup 3; Read and Record

Alternate Group A - Subgroups 3, 8B, 11; Method 5005; Paragraph 3.5.1.1

Marking

Electrical Tests - Subgroup 2; Read and Record

Alternate Group A - Subgroups 2, 8A, 10; Method 5005; Paragraph 3.5.1.1

Fine and Gross Leak Tests - Method 1014, 100%

Customer Source Inspection (Note 2)

Group B Inspection - Method 5005 (Notes 2)
End-Point Electrical Parameters: B5; Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11

Group D Inspection - Method 5005 (Notes 2, 4)
End-Point Electrical Parameters: B5; Subgroups 1, 7, 9

External Visual Inspection - Method 2009

Data Package Generation (Note 5)

NOTES:

1. The notes of Method 5004, Table I shall apply; unless otherwise specified.
2. These steps are optional, and should be listed on the purchase order if required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table O of Method 1015.
4. For Group D, subgroup 3 inspection of package configurations which utilize a gold plated lid in its construction; the inspection criteria for illegible markings criteria of Method 1010, paragraph 3.3 and of Method 1004, paragraph 3.8.a shall not apply.
5. Data package contains: Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (includes SEM report)
   X-Ray Report and Film
   Test Variables Data

Metallization Topology

DIE DIMENSIONS:
76.0 x 89.4 x 14 ± 1mils

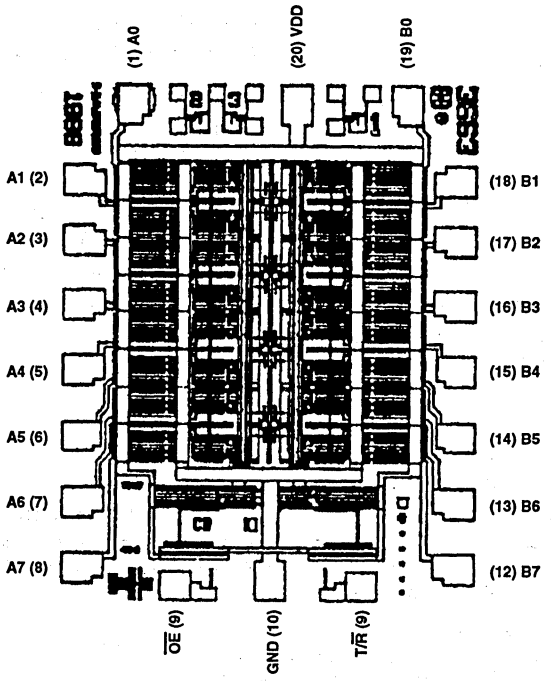
METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature:Ceramic DIP - 460°C (Max)

Metallization Mask Layout

HS-82C08RH



HARRIS SEMICONDUCTOR

HS-82C12RH

Radiation Hardened 8-Bit Input/Output Port

December 1992

Features

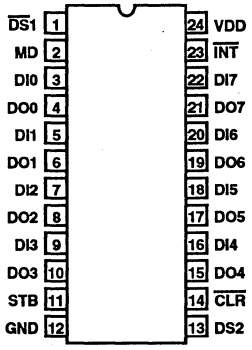
- Radiation Hardened CMOS Process
  - Total Dose 1 x 10^5 RAD(Si)
  - Transient Upset > 1 x 10^8 RAD(Si)/s
  - Latch-Up Immune EPI-CMOS > 1 x 10^{12} RAD(Si)/s
- Low Power Dissipation
- High Noise Immunity
- Single Power Supply +5V
- Low Input Load Current
- 8-Bit Data Register and Buffer
- Asynchronous Register Clear
- Service Request Flip-Flop for Interrupt Generation
- Three-State Outputs
- Bus-Compatible with HS-80C85RH CPU
- Electrically Equivalent to Sandia SA3026
- Military Temperature Range -55°C to +125°C

Description

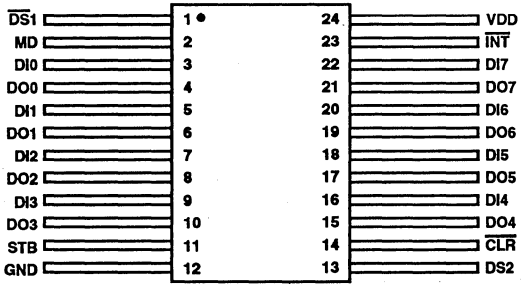
The Harris HS-82C12RH is a radiation hardened 8-bit input/output port designed for use with the HS-80C85RH radiation hardened microprocessor. It is manufactured using a self-aligned, junction-isolated EPI-CMOS process and features three-state output buffers and device selection and control logic. A service request flip-flop is included for the generation and control of interrupts to the microprocessor. The device can be used in implement many of the peripheral and input/output functions of a microcomputer system. The HS-82C12RH is pinout- and function- compatible with industry-standard 8212 devices.

Pinouts

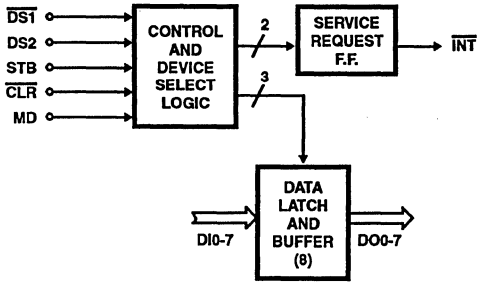
24 PIN DIP
CASE OUTLINE D3, CONFIGURATION 3
TOP VIEW



24 PIN FLATPACK
INTERNAL PACKAGE CODE HWL
TOP VIEW



Functional Diagram



DI0-DI7	Data In
DO0-DO7	Data Out
$\overline{DS1}$, DS2	Device Select
MD	Mode
STB	Strobe
$\overline{INT}$	Interrupt
$\overline{CLR}$	Clear

11 µPROCESSOR PERIPHERALS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3041

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage ..... GND-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	61.6°C/W	15.1°C/W
Flatpack Package	55°C/W	10°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 0.81W
Flatpack Package 0.91W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.75V to +5.25V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +1.0V
Input High Voltage ..... VDD -1V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Input Leakage Current	IIH	VDD = 5.25V, VIN = 0V, Pin under test = 5.25V	1, 2, 3	-55°C, +25°C, +125°C	-	1	µA
Low Input Leakage Current	IIL	VDD = 5.25V, VIN = 5.25V, Pin under test = 0V	1, 2, 3	-55°C, +25°C, +125°C	-1	-	µA
Low Output Voltage	VOL	VDD = 5.25V, IOL = 2mA	1, 2, 3	-55°C, +25°C, +125°C	-	0.5	V
High Output Voltage	VOH	VDD = 4.75V, IOH = -2mA	1, 2, 3	-55°C, +25°C, +125°C	4.25	-	V
Static Current	SIDD	VDD = 5.25V, VIN = GND	1, 2, 3	-55°C, +25°C, +125°C	-	100	µA
Functional Tests	FT	VDD = 4.75V and 5.25V, VIH = VDD-1.0V, VIL = 1.0V	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-

NOTE: All devices are guaranteed at worst case limits and over radiation.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Data to Output Delay	TPD	9, 10, 11	-55°C, +25°C, +125°C	-	105	ns
Write Enable to Output Delay	TWE	9, 10, 11	-55°C, +25°C, +125°C	-	200	ns
Reset to Output Delay	TR	9, 10, 11	-55°C, +25°C, +125°C	-	145	ns
Set to Output Delay	TS	9, 10, 11	-55°C, +25°C, +125°C	-	100	ns
Clear to Output Delay	TC	9, 10, 11	-55°C, +25°C, +125°C	-	135	ns
Output Enable Time	TE	9, 10, 11	-55°C, +25°C, +125°C	-	125	ns
Output Disable Time	TD	9, 10, 11	-55°C, +25°C, +125°C	-	85	ns

NOTE:

1. Output Timings are measured with the following conditions: CL = 100pF, VIH = 3.75V, and VIL = 1.0V

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz, All measurements referenced to device ground		T_A = +25°C	-	8	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz, All measurements referenced to device ground		T_A = +25°C	-	8	pF
Pulse Width	TPW	VDD = 4.75, VIH = 3.75, VIL = 1.0	9, 10, 11	-55°C, +25°C, +125°C	-	50	ns
Data Set Up Time	TSET	VDD = 4.75, VIH = 3.75, VIL = 1.0	9, 10, 11	-55°C, +25°C, +125°C	-	30	ns
Data Hold Time	TH	VDD = 4.75, VIH = 3.75, VIL = 1.0	9, 10, 11	-55°C, +25°C, +125°C	-	40	ns

NOTE: The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The Post Irradiation test conditions and limits are the same as those listed in Table 1 and Table 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C) GROUP B, SUBGROUP 5

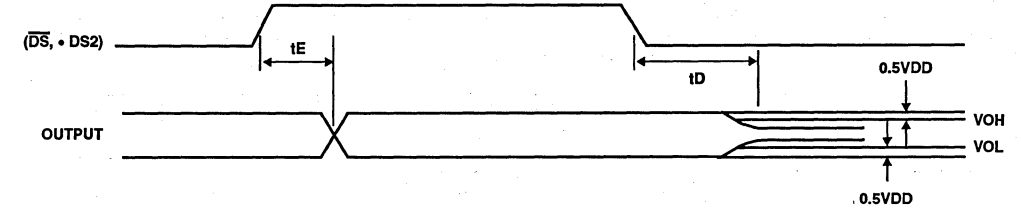
PARAMETER	SYMBOL	DELTA LIMITS
Static Current	SIDD	±30µA
Low Input Leakage Current	IIL	±100nA
High Input Leakage Current	IIH	±100nA
Low Level Output Voltage	VOL	±60mV
High Level Output Voltage	VOH	±400mV

TABLE 6. APPLICABLE SUBGROUPS

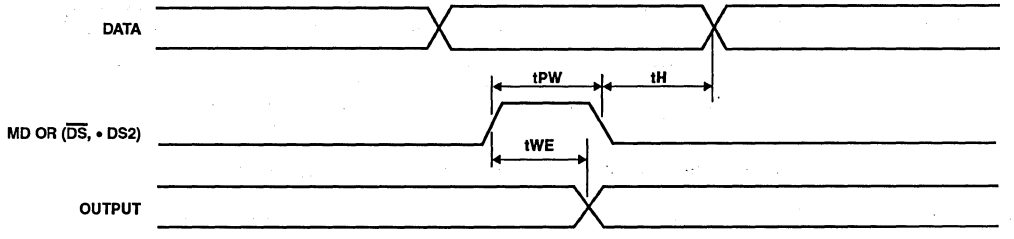
CONFORMANCE GROUPS	METHOD	-8 SUBGROUPS
Initial Test	100%/5004	1, 7, 9
PDA	100%/5004	1, 7
Final Test	100%/5004	2, 3, 8A, 8B, 9, 10, 11
Group A	Samples/5004	1, 2, 3, 8A, 8B, 9, 10, 11
Group C	Samples/5004	1, 2, 3, 8A, 8B, 9, 10, 11
Group D Others	Samples/5004	1, 7
Group E Subgroup 2	Samples/5004	1, 7, 9

Timing Waveforms

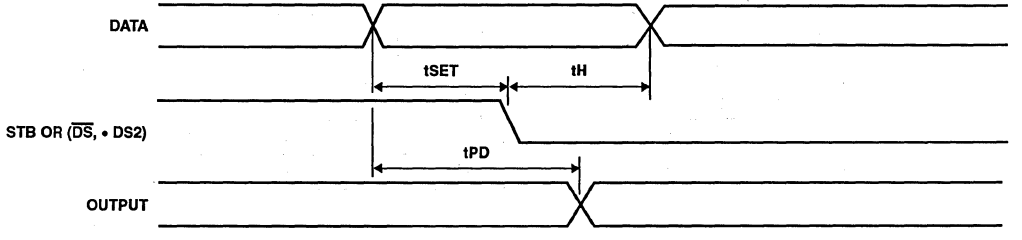
READ TIMING



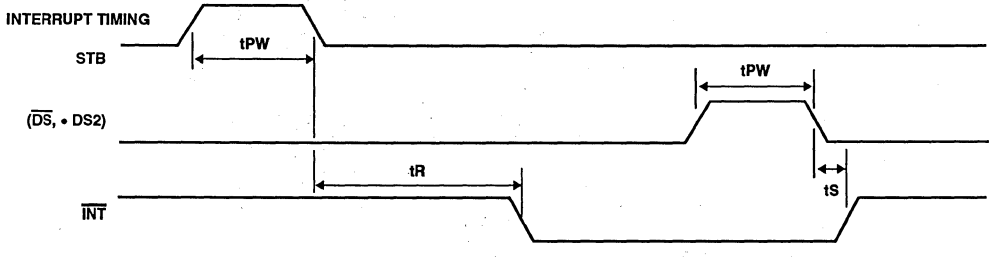
WRITE TIMING



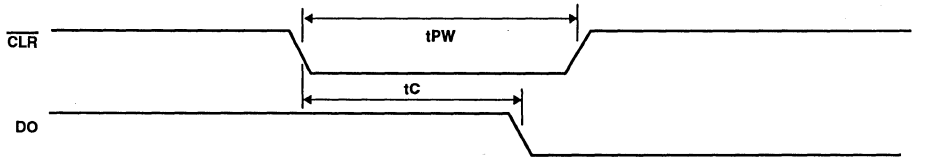
DATA SETUP, HOLD, PROPAGATION DELAY TIMING



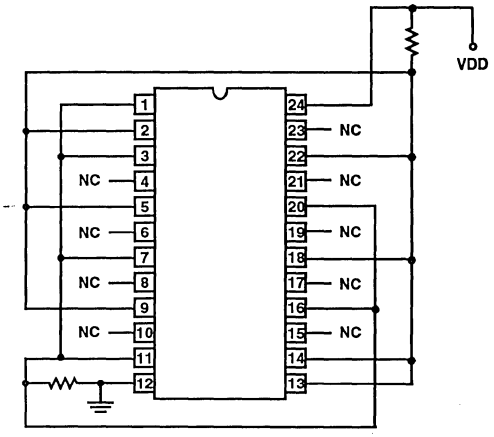
INTERRUPT TIMING



CLEAR TIMING



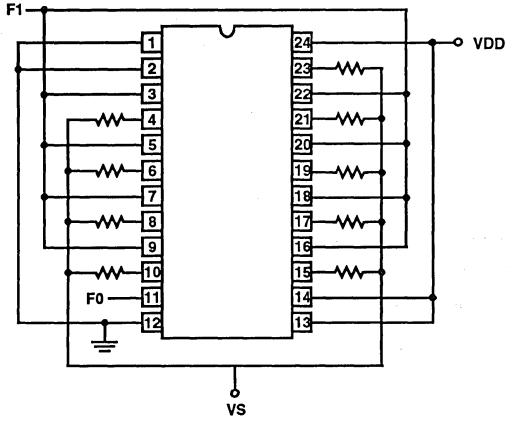
Burn-In Circuits



STATIC CONFIGURATION

NOTES:

VDD = 10V ± 10%
All resistors 10K
Voltage must be ramped up



DYNAMIC CONFIGURATION

NOTES:

VDD = 10V ± 10%, VS = 5V ± 10%, T_A Min = +125°C
All resistors 10kΩ ± 10%, 1/4W
Part is Static Sensitive, Voltage Must be Ramped

Radiation Screening Procedure

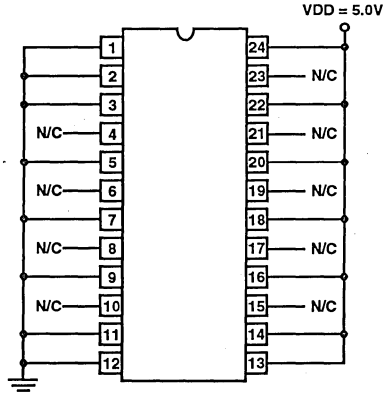
1. A random sample of two dice per wafer is drawn from the wafer lot. Wafer identity is retained.
2. The sample die shall be assembled and tested for functionality, in a ceramic DIP.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1 x 105 Rad-Si (±10%) from a Gamma-cell 220 Cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with VSUPPLY = +5V. The dose rate shall be between 50 rads/sec and 300 rads/sec.
4. The Irradiation Bias circuit is shown.
5. The samples shall be started into test within 1 hour of irradiation and have completed test within 2 hours of irradiation. The wafers are accepted only if the sample, exclusive of non-radiation failures, meets all electrical specifications at room temperature.
6. Radiation screening to a higher total dose is available. Customers should contact their closest Harris Representative for details.

Radiation Effects

The HS-82C08RH has been designed to survive in a radiation environment and to meet the electrical characteristics. Latch-up free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained with special low temperature processing cycles. On a production basis, Harris performs screens for total dose hardness to a level of 1 x 10^5 Rad-Si. Transient radiation tests have shown the following results:

Latch-up free to doses ≥ 1 x 10^{12} rads/sec.

Irradiation Circuit



NOTES:

VDD = 5.0 ± 0.5V
Group E Testing is performed in Ceramic DIP
Group E Sample Size is 2 die/wafer

Harris - Space Level Product Flow (Note 1)

SEM - Traceable to Diffusion - Method 2018

Wafer Lot Acceptance Method 5007

Internal Visual Inspection - Method 2010, Condition A

Gamma Radiation Assurance Tests - Method 1019

Nondestructive Bond Pull - Method 2023

Customer Pre-Cap Visual Inspection (Notes 2)

Temperature Cycling - Method 1010, Condition C

Constant Acceleration - Method 2001, Condition E Min., Y1

Particle Impact Noise Detection - Method 2020, Condition A

Electrical Tests - Harris' Option

Serialization

X-Ray Inspection - Method 2012

Electrical Tests - Subgroup 1; Read and Record (T0)

Static Burn-In - Method 1015, Condition B, 72 Hours, +125°C Minimum

Electrical Tests - Subgroup 1; Read and Record (T1)

Burn-In Delta Calculation (T0-T1)

PDA Calculation 3%: Subgroup 7
5% Subgroups 1, 7, Delta

Dynamic Burn-In, Method 1015, Condition D, 240 Hours, +125°C (Note 3)

Electrical Tests - Subgroup 1; Read and Record (T2)

Alternate Group A - Subgroups 1, 7, 9; Method 5005; Paragraph 3.5.1.1

Burn-In Delta Calculation (T0-T2)

PDA Calculation 3%: Subgroup 7
5% Subgroups 1, 7, Delta

Electrical Tests - Subgroup 3; Read and Record

Alternate Group A - Subgroups 3, 8B, 11; Method 5005; Paragraph 3.5.1.1

Marking

Electrical Tests - Subgroup 2; Read and Record

Alternate Group A - Subgroups 2, 8A, 10; Method 5005; Paragraph 3.5.1.1

Fine and Gross Leak Tests - Method 1014, 100%

Customer Source Inspection (Note 2)

Group B Inspection - Method 5005 (Notes 2)
End-Point Electrical Parameters: B5; Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11

Group D Inspection - Method 5005 (Notes 2, 4)
End-Point Electrical Parameters: B5; Subgroups 1, 7, 9

External Visual Inspection - Method 2009

Data Package Generation (Note 5)

NOTES:

1. The notes of Method 5004, Table I shall apply; unless otherwise specified.
2. These steps are optional, and should be listed on the purchase order if required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table O of Method 1015.
4. For Group D, subgroup 3 inspection of package configurations which utilize a gold plated lid in its construction; the inspection criteria for illegible markings criteria of Method 1010, paragraph 3.3 and of Method 1004, paragraph 3.8.a shall not apply.
5. Data package contains: Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (includes SEM report)
   X-Ray Report and Film
   Test Variables Data

Metallization Topology

DIE DIMENSIONS:
90 x 76 x 14 ± 1mils

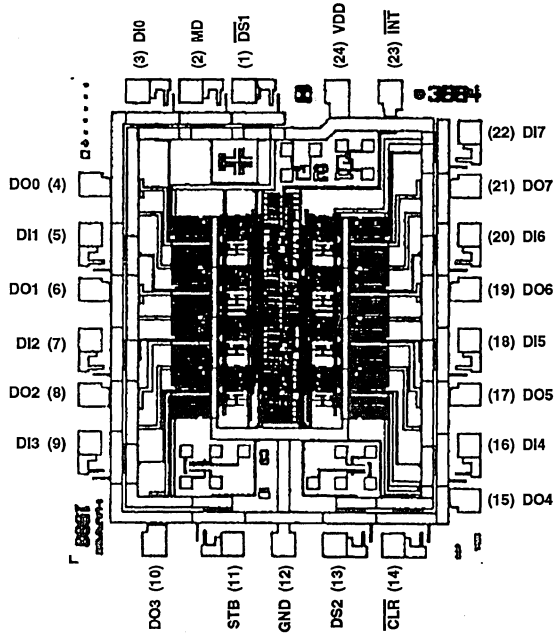
METALLIZATION:
Type: AlSi
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: SiO2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature:Ceramic DIP - 460°C (Max)

Metallization Mask Layout

HS-82C12RH



Functional Description

Data Latch

The data latch is comprised of eight "D" type flip-flops. The output of each flip-flop will follow the corresponding data input (DI0 - DI7) when the clock (C) is high. The clock input is level sensitive and the data becomes latched when the clock returns low.

An asynchronous reset ($\overline{CLR}$) is used to clear the latched data. Since the clock (C) overrides the reset ($\overline{CLR}$), the data must be in the latched state in order to clear the flip-flops. If the data is not latched (i.e. clock is high) when $\overline{CLR}$ goes low, then the Q outputs of the data latch will continue to follow the data input, overriding the reset signal.

Output Buffer

Three-state buffers are used to provide output drive for the data latch. A high level on the "output buffer enable" control line enables the buffer outputs. When "output buffer enable" is low the buffer outputs are forced to the high-impedance state.

Device Select Logic

The inputs $\overline{DS1}$ and DS2 are used for device selection. When $\overline{DS1}$ is low and DS2 is high, the device is selected. The output buffers are enabled and the service request flip-flop is asynchronously cleared when the device is selected.

Mode

the mode input (MD) is used to control the state of the output buffer and to determine the source of the data latch clock (C). When MD is high, the output buffers are enabled and the source of the data latch clock (C) is the device select logic ($\overline{DS1} \bullet DS2$).

When MD is low, the state of the output buffer is controlled by the device select logic ($\overline{DS1} \bullet DS2$) and the source of the data latch clock is the strobe (STB) input.

Strobe

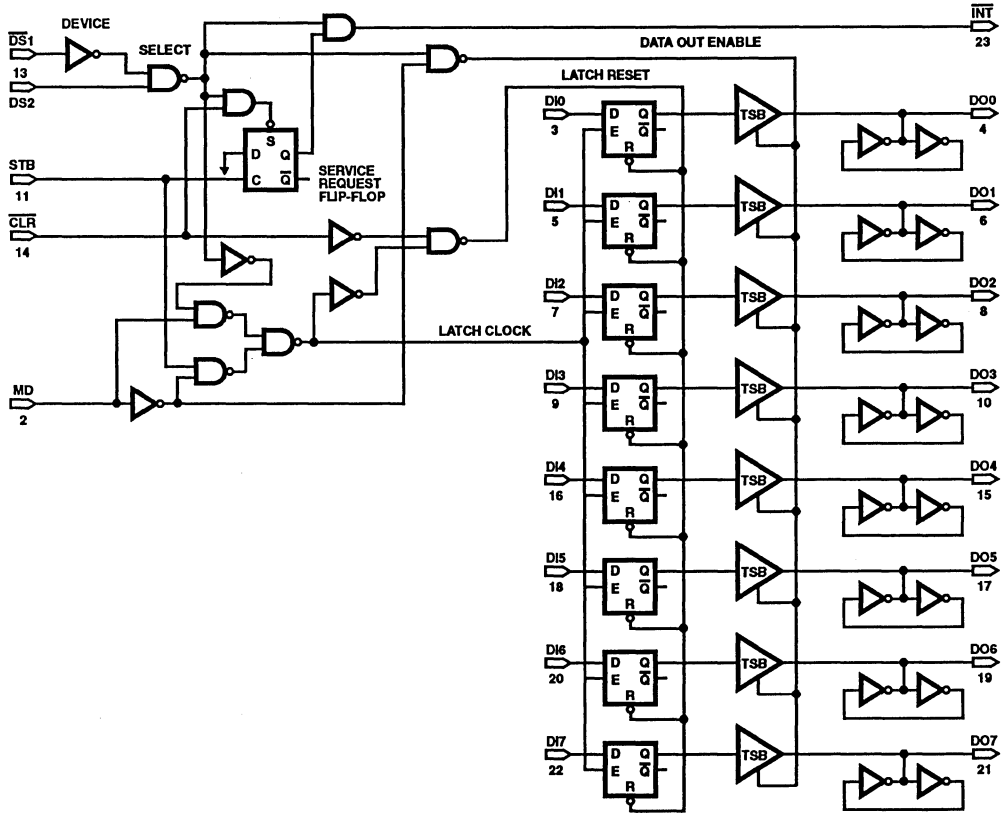
The strobe input (STB) is used as the data latch clock (C) when the mode input (MD) is low. The service request flip-flop is synchronously set on the negative going edge of STB.

Service Request Flip-Flop

The service request flip-flop is to generate interrupts to microcomputer systems. It is negative edge triggered and asynchronously cleared (reset).

The output of the service request flip-flop is AND-gated with the device select logic ($\overline{DS1} \bullet DS2$). The output of the AND gate is the active low interrupt ($\overline{INT}$) signal.

Logic Diagram



TRUTH TABLE 1. DATA OUT

STB	MD	$\overline{DS1} \cdot DS2$	DATA OUT EQUALS
0	0	0	High Z State
1	0	0	High Z State
0	1	0	Data Latch
1	1	0	Data Latch
0	0	1	Data Latch
1	0	1	Data In
0	1	1	Data In
1	1	1	Data In

TRUTH TABLE 2. $\overline{INT}$

$\overline{CLR}$	$\overline{DS1} \cdot DS2$	STB	Q*	$\overline{INT}$
0 RESET	0	0	0	1
1	0	0	0	1
1	0	⌐	1	0
1	1 RESET	0	0	0
1	0	0	0	1

* Internal Service Request Flip-Flop

HARRIS SEMICONDUCTOR

HS-82C37ARH

Radiation Hardened CMOS High Performance Programmable DMA Controller

December 1992

Features

- Radiation Hardened
  - Total Dose >10^5 RAD(Si)
  - Transient Upset > 10^8 RAD(Si)/s
  - Latch Up Free EPI-CMOS
  - Functional After Total Dose 10^6 RAD(Si)
- Low Power Consumption
  - IDDSB = 50μA Maximum
  - IDDOP = 4.0mA/MHz Maximum
- Pin Compatible with NMOS 8237A and the Harris 82C37A
- High Speed Data Transfers Up To 2.5 MBPS With 5MHz Clock
- Four Independent Maskable Channels With Autoinitialization Capability
- Expandable to Any Number of Channels
- Memory-to-Memory Transfer Capability
- CMOS Compatible
- Hardened Field, Self-Aligned, Junction Isolated CMOS Process
- Single 5V Supply
- Military Temperature Range -55°C to +125°C

Description

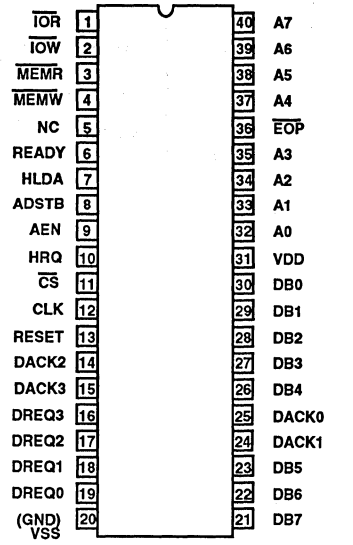
The Harris HS-82C37ARH is an enhanced, radiation hardened CMOS ver sion of the industry standard 8237A Direct Memory Access (DMA) controller, fabricated using the Harris hardened field, self-aligned silicon gate CMOS process. The HS-82C37ARH offers increased functionality, improved performance, and dramatically reduced power consumption for the radiation environment. The high speed, radiation hardness, and industry standard configuration of the HS-82C37ARH make it compatible with radiation hardened microprocessors such as the HS-80C85RH and the HS-80C86RH.

The HS-82C37ARH can improve system performance by allowing external devices to transfer data directly to or from system memory. Memory-to-memory transfer capability is also provided, along with a memory block initialization feature. DMA requests may be generated by either hardware or software, and each channel is independently programmable with a variety of features for flexible operation.

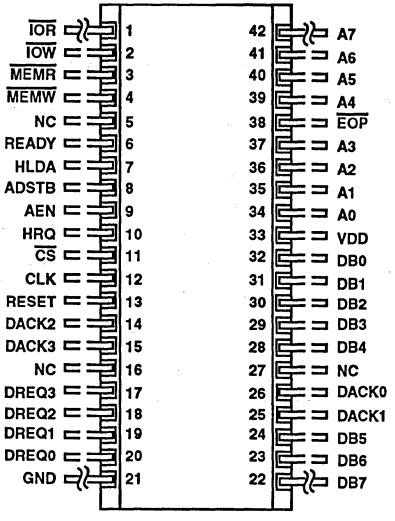
Static CMOS circuit design insures low operating power and allows gated clock operation for an even further reduction of power. Multimode programmability allows the user to select from three basic types of DMA services, and reconfiguration under program control is possible even with the clock to the controller stopped. Each channel has a full 64K address and word count range, and may be programmed to autoinitialize these registers following DMA termination (end of process). The Harris hardened field CMOS process results in performance equal to or greater than existing radiation resistant products at a fraction of the power.

Pinouts

40 DIP
38510 OUTLINE D5, CONFIGURATION 3
TOP VIEW



42 PIN FLATPACK
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3042

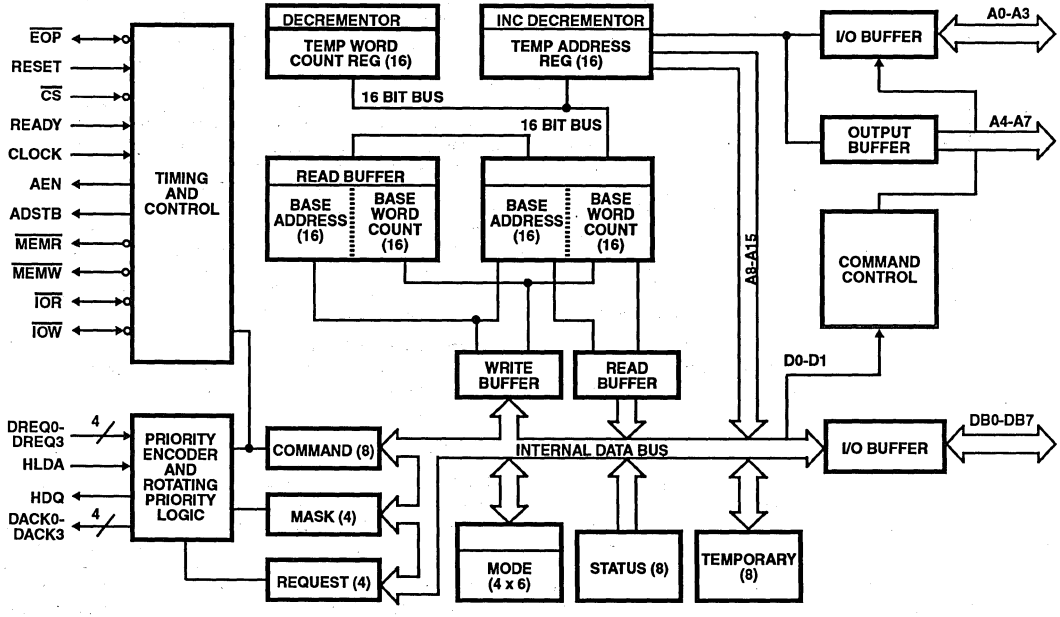
Pin Descriptions

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
VDD	31		VDD: is the +5V power supply pin. A 0.1µF capacitor between pins 31 and 20 is recommended for decoupling.
GND	20		Ground
CLK	12	I	CLOCK INPUT: The Clock Input is used to generate the timing signals which control HS-82C37ARH operations. This input may be driven from DC to 5MHz and may be stopped in either high or low state for standby operation.
$\overline{CS}$	11	I	CHIP SELECT: Chip Select is an active low input used to enable the controller onto the data bus for CPU communications.
RESET	13	I	RESET: This is an active high input which clears the Command, Status, Request and Temporary Registers, the First/Last Flip-Flop, and the Mode Register Counter. The Mask Register is Set to ignore requests. Following a Reset, the controller is in an idle cycle.
READY	6	I	READY: This signal can be sued to extend the memory read and write pulses from the HS-82C37ARH to accommodate slow memories or I/O devices. Ready must not make transitions during its specified set-up and hold times. Ready is ignored in Verify Transfer mode.
HLDA	7	I	HOLD ACKNOWLEDGE: The active high Hold Acknowledge from the CPU indicates that is has relinquished control of the system busses.
DREQ0-DREQ3	16-19	I	DMA REQUEST: The DMA Request (DREQ) lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In Fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ is programmable. Reset initializes these lines to active. DREQ will not be recognized while the clock is stopped. Unused DREQ inputs should be pulled High or Low (inactive) and the corresponding mask bit set.
DB0-DB7	21-23 26-30	I/O	DATA BUS: The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled in the Program Condition during the I/O Read to output the contents of a register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the HS-82C37ARH Control Registers. During DMA cycles, the most significant 8 bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In Memory-to-Memory operations, data from the memory enters the HS-82C37ARH on the data bus during the read-from-memory transfer, then during the write-to-memory transfer, the data bus outputs write the data into the new memory location.
$\overline{IOR}$	1	I/O	I/O READ: I/O Read is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to read the internal registers. In the Active cycle, it is an output control signal used by the HS-82C37ARH to access data from a peripheral during a DMA Write transfer.
$\overline{IOW}$	2	I/O	I/O WRITE: I/O Write is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to load information into the HS-82C37ARH. In the Active cycle, it is an output control signal used by the HS-82C37ARH to load data to the peripheral during a DMA Read transfer.
$\overline{EOP}$	36	I/O	END OF PROCESS: End of Process ($\overline{EOP}$) is an active low bidirectional signal. Information concerning the completion of DMA services is available at the bidirectional $\overline{EOP}$ pin. The HS-82C37ARH allows an external signal to terminate an active DMA service by pulling the $\overline{EOP}$ pin low. A pulse is generated by the HS-82C37ARH when terminal count (TC) for any channel is reached, except for channel 0 in Memory-to-Memory mode. During Memory-to-Memory transfers, EOP will be output when the TC for channel 1 occurs. The $\overline{EOP}$ pin is driven by an open drain transistor on-chip, and requires an external pull-up resistor. When an EOP pulse occurs, whether internally or externally generated, the HS-82C37ARH will terminate the service, and if Autoinitialize is enabled, the base registers will be written to the current registers of that channel. The mask bit and TC bit in the Status Register will be set for the currently active channel by $\overline{EOP}$ unless the channel is programmed for Autoinitialize. In that case, the mask bit remains clear.
A0-A3	32-35	I/O	Address: The four least significant address lines are bidirectional three-state signals. In the Idle cycle, they are inputs and are used by the HS-80C86RH to address the internal registers to be loaded or read. In the Active cycle, they are outputs and provide the lower 4 bits of the output address.

Pin Descriptions (Continued)

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
A4-A7	37-40	O	Address: The four most significant address lines are three-state outputs and provide 4 bits of address. These lines are enabled only during the Active cycle.
HRQ	10	O	Hold Request: The Hold Request (HRQ) output is used to request control of the system bus. When a DREQ occurs and the corresponding mask bit is clear, or a software DMA request is made, the HS-82C37ARH issues HRQ. The HLDA signal then informs the controller when access to the system busses is permitted. For stand-alone operation where the HS-82C37ARH always controls the busses, HRQ may be tied to HLDA. This will result in one S0 state before the transfer.
DACK0-DACK3	14,15,24, 25	O	DMA Acknowledge: DMA acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. Reset initializes them to active low.
AEN	9	O	Address Enable: Address Enable enables the 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers. AEN is active HIGH.
ADSTB	8	O	Address Strobe: This is an active high signal used to control latching of the upper address byte. It will drive directly the strobe input of external transparent octal latches, such as the 82C82. During block operations, ADSTB will only be issued when the upper address byte must be updated, thus speeding operation through elimination of S1 states. (See Note 2).
$\overline{\text{MEMR}}$	3	O	Memory Read: The Memory Read signal is an active low three-state output used to access data from the selected memory location during a DMA Read or a Memory-to-Memory transfer.
$\overline{\text{MEMW}}$	4	O	Memory Write: The Memory Write is an active low three-state output used to write data to the selected memory location during a DMA Write or a Memory-to-Memory transfer.
NC	5		No connect. Pin 5 is open and should not be tested for continuity.

Functional Diagram



Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied ..... VSS - 0.3V to VDD + 0.3V for All Grades
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C
Junction Temperature ..... +175°C
Typical Derating Factor ..... 4mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	24.2°C/W	9.5°C/W
Braze Seal Flatpack Package	72.1°C/W	9.7°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package 1.98W
Braze Seal Flatpack Package ..... 0.69 W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage Range (VDD) ..... +4.5V to +5.5V
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... VDD -1.5V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
TTL Output High Voltage	VOH1	VDD = 4.5V, IO = -2.5mA, VIN = 0V or 4.0V	1, 2, 3	+25°C, +125°C, -55°C	3.0	-	V
CMOS Output High Voltage	VOH2	VDD = 4.5V, IO = -100µA, VIN = 0V or 4.0V	1, 2, 3	+25°C, +125°C, -55°C	VDD-0.4	-	V
Output Low Voltage	VOL1	VDD = 4.5V, IO = +2.5mA, VIN = 0V or 4.0V	1, 2, 3	+25°C, +125°C, -55°C	-	0.4	V
Input Leakage Current	IIL or IIH	VDD = 5.5V, VIN = 0V or 5.5V Pins: 6, 7, 11-13, 16-19	1, 2, 3	+25°C, +125°C, -55°C	-1.0	1.0	µA
Output Leakage Current	IOZL or IOZH	VDD = 5.5V, VIN = 0V or 5.5V Pins: 1-4, 21-23, 26-30, 32-40	1, 2, 3	+25°C, +125°C, -55°C	-10	10	µA
Standby Power Supply Current	IDDSB	VDD = 5.5V, IO = 0mA, VIN = GND or VDD	1, 2, 3	+25°C, +125°C, -55°C	-	+50	µA
Operating Power Supply Current	IDDOP	VDD = 5.5V, IO = 0mA, VIN = GND or VDD, f = 5MHz	1, 2, 3	+25°C, +125°C, -55°C	-	20	mA
Functional Tests	FT	VDD = 4.5V and 5.5V, VIN = GND or VDD, f = 1MHz	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-
Noise Immunity Functional Test	FN	VDD = 4.5V and 5.5V, VIN = GND or VDD - 1.5V and VDD = 4.5V, VIN = 0.8V or VDD	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

VCC = +5V ±10%, GND = 0V, AC's Tested at Worst Case VDD, Guaranteed Over Full Operating Range.

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	SUBGROUP	LIMITS MIN	LIMITS MAX	UNITS
DMA (MASTER) MODE							
AEN HIGH from CLK LOW (S1) Delay Time	TCLAEH	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11		175	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

VCC = +5V ±10%, GND = 0V, AC's Tested at Worst Case VDD, Guaranteed Over Full Operating Range.

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	SUBGROUP	LIMITS MIN	LIMITS MAX	UNITS
DMA (MASTER) MODE (Continued)							
AEN LOW from CLK HIGH (SI) Delay Time	TCHAEL	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	-	130	ns
ADR from $\overline{\text{READ}}$ HIGH Hold Time	TRHAX	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	TCLCL-100	-	ns
DB from ADSTB LOW Hold Time	TSLDZ	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	TCLCH-18	-	ns
ADR from $\overline{\text{WRITE}}$ HIGH Hold Time	TWHAX	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	TCLCL-50	-	ns
DACK Valid from CLK LOW Delay Time	TCLDAV	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	-	170	ns
$\overline{\text{EOP}}$ HIGH from CLK HIGH Delay Time	TCHIPH	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	-	170	ns
$\overline{\text{EOP}}$ LOW from CLK HIGH Delay Time	TCHIPL	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	-	100	ns
ADR Stable from CLK HIGH	TCHAV	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	-	110	ns
DB to ADSTB LOW Setup Time	TDVSL	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	TCHCL +10	-	ns
Clock HIGH Time (Transitions 10ns)	TCHCL	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	70	-	ns
Clock LOW Time (Transitions 10ns)	TCLCH	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	50	-	ns
CLK Cycle Time	TCLCL	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	200	-	ns
CLK HIGH to $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ LOW Delay	TCHRWL	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	-	190	ns
$\overline{\text{READ}}$ HIGH from CLK HIGH (S4) Delay Time	TCHRH	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	-	190	ns
$\overline{\text{WRITE}}$ HIGH from CLK HIGH (S4) Delay Time	TCHWH	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	-	130	ns
HRQ Valid from CLK HIGH Delay Time	TCHRQV	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	-	120	ns
$\overline{\text{EOP}}$ LOW to CLK LOW Setup Time	TEPLCL	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	40	-	ns
$\overline{\text{EOP}}$ Pulse Width	TEPLEPH	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	220	-	ns
$\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ Active from CLK HIGH	TCHRWV	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	-	150	ns
DB Float to Active Delay from CLK HIGH	TCHDV	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	-	110	ns
HLDA Valid to CLK HIGH Setup Time	TRAVCH	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	75	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

VCC = +5V ±10%, GND = 0V, AC's Tested at Worst Case VDD, Guaranteed Over Full Operating Range.

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	SUBGROUP	LIMITS		UNITS
					MIN	MAX	
DMA (MASTER) MODE (Continued)							
Input Data from $\overline{MEMR}$ HIGH Hold Time	TMRHDX	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	0		ns
Input Data to $\overline{MEMR}$ HIGH Setup Time	TDVMRH	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	155		ns
Output Data from $\overline{MEMW}$ HIGH HOLD Time	TMWHDZ	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	15		ns
Output Data Valid to $\overline{MEMW}$ HIGH	TDVMWH	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	TCLCL-35	-	ns
DREQ to CLK LOW (SI, S4) Setup Time	TDQVCL	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	0	-	ns
CLK LOW to READY Hold Time	TCLRYX	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	20	-	ns
READY to CLK LOW Setup Time	TRYVCL	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	60	-	ns
ADSTB HIGH from CLK LOW Delay Time	TCLSH	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	-	80	ns
ADSTB LOW from CLK LOW Delay Time	TCLSL	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	-	120	ns
$\overline{READ}$ HIGH Delay from $\overline{WRITE}$ HIGH	TWHRH	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	0	-	ns
$\overline{READ}$ Pulse Width, Normal Timing	TRLRH1	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	2TCLCL -50	-	ns
ADSTB Pulse Width	TSHSL	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	TCLCL - 80	-	ns
Extended $\overline{WRITE}$ Pulse Width	TWLWH1	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	2TCLCL -100	-	ns
$\overline{WRITE}$ Pulse Width	TWLWH2	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	TCLCL - 100	-	ns
$\overline{READ}$ Pulse Width, Compressed	TRLRH2	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	TCLCL - 50	-	ns
PERIPHERAL (SLAVE) MODE							
ADR Valid or $\overline{CS}$ LOW to $\overline{IOR}$ LOW	TAVIRL	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	10	-	ns
ADR Valid or $\overline{CS}$ LOW to $\overline{IOW}$ LOW Setup Time 0	TAVIWL	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	0	-	ns
Data Valid to $\overline{IOW}$ HIGH Setup Time	TDVIWH	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	150	-	ns
ADR or $\overline{CS}$ Hold from $\overline{IOR}$ HIGH	TIRHAX	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	0	-	ns
Data Access from $\overline{IOR}$	TIRLDV	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	-	150	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

VCC = +5V ±10%, GND = 0V, AC's Tested at Worst Case VDD, Guaranteed Over Full Operating Range.

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	SUBGROUP	LIMITS MIN	LIMITS MAX	UNITS
PERIPHERAL (SLAVE) MODE (Continued)							
RESET to First $\overline{IOW}$ or $\overline{IOR}$	TRSLIRWL	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	2TCLCL	-	ns
RESET Pulse Width	TRSHRSL	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	300	-	
$\overline{IOR}$ Width	TIRLIRH	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	200	-	ns
ADR or $\overline{CS}$ HIGH from $\overline{IOW}$ HIGH Hold Time	TIWHAX	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	0	-	ns
Data from $\overline{IOW}$ HIGH Hold Time	TIWHDX	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	10	-	ns
$\overline{IOW}$ Width	TIWLIWH	VDD = 4.5V	+25°C, +125°C, -55°C	9, 10, 11	150	-	ns

NOTE:

1. $\overline{READ}$ refers to both $\overline{IOR}$ and $\overline{MEMR}$, and WRITE refers to both $\overline{IOW}$ and $\overline{MEMW}$, during memory to I/O and I/O to memory transfers
2. AC's Tested at Worst Case VDD But Guaranteed Over Full Operating Range

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz, All measurements referenced to device ground.	T_A = +25°C	-	15	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz, All measurements referenced to device ground.	T_A = +25°C	-	15	pF
I/O Capacitance	CI/O	VDD = Open, f = 1MHz, All measurements referenced to device ground.	T_A = +25°C	-	20	pF
ADR Active to Float Delay from CLK HIGH	TCHAZ	VDD = 4.5V and 5.5V	-55°C < T_A < +125°C	-	90	ns
READ or WRITE Float Delay from CLK HIGH	TCHRWZ	VDD = 4.5V and 5.5V	-55°C < T_A < +125°C	-	120	ns
DB Active to Float Delay from CLK HIGH	TCHDZ	VDD = 4.5V and 5.5V	-55°C < T_A < +125°C	-	170	ns
DB Float Delay from IOR HIGH	TIRHDZ	VDD = 4.5V and 5.5V	-55°C < T_A < +125°C	10	85	ns
Power Supply HIGH to RESET LOW Setup Time	TPHRSL	VDD = 4.5V and 5.5V	-55°C < T_A < +125°C	500	-	ns

NOTE: The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: See +25°C limits in Table 1 and Table 2 for Post RAD limits (Subgroups 1, 7 and 9).

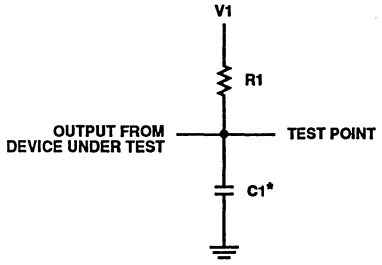
TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Standby Power Supply Current	IDDSB	± 20µA
Output Leakage Current	IOZL, IOZH	± 2µA
Input Leakage Current	IIH, IIL	± 200nA
Output Low Voltage	VOL	± 80mV
TTL Output High Voltage	VOH1	± 600mV
CMOS Output High Voltage	VOH2	± 150mV

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9
Interim Test		100%/5004	1, 7, 9	N/A
PDA		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B	B5	Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A
	Others	Samples/5004	1, 7	N/A
Group C		Samples/5004	N/A	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group D		Samples/5004	1, 7	1, 7
Group E	Subgroup 2	Samples/5004	1, 7, 9	1, 7, 9

AC Test Circuit

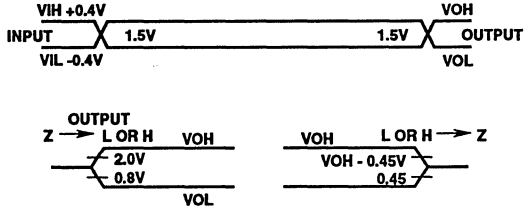


*Includes Stray and Jig Capacitance

TEST CONDITION DEFINITION TABLE

PINS	V1	R1	C1
All Output Except $\overline{EOP}$	1.7V	510Ω	100pF
$\overline{EOP}$	VDD	1.6KΩ	50pF

AC Testing Input, Output Waveforms



Waveforms

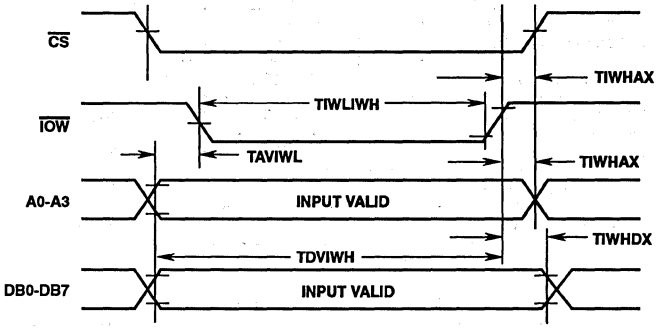


FIGURE 1. SLAVE MODE TIMING

NOTE: Host system must allow at least TCLCL as recovery time between successive write accesses

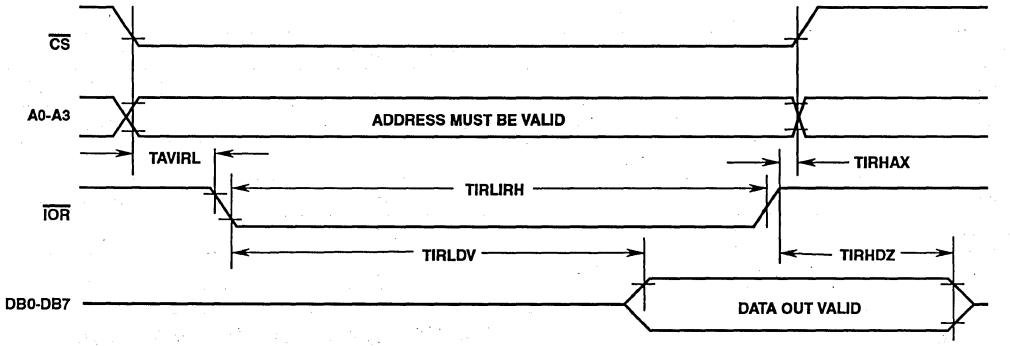


FIGURE 2. SLAVE MODE READ

NOTE: Host system must allow at least TCLCL as recovery time between successive write accesses

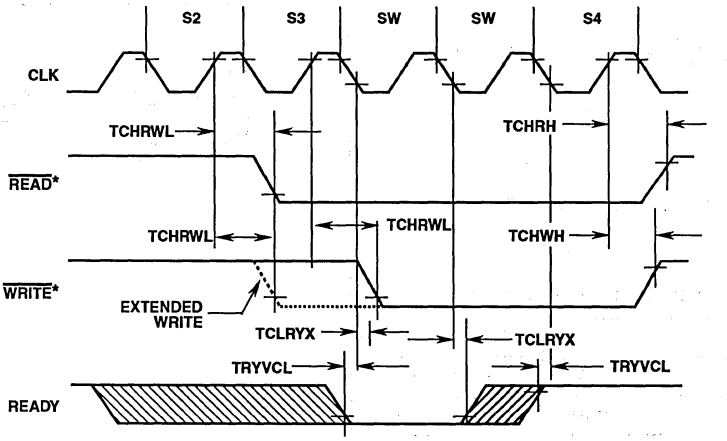


FIGURE 3. READY

* $\overline{\text{READ}}$ refers to both $\overline{\text{IOR}}$ and $\overline{\text{MEMR}}$ outputs. $\overline{\text{WRITE}}$ refers to both $\overline{\text{IOW}}$ and $\overline{\text{MEMW}}$ outputs

Waveforms (Continued)

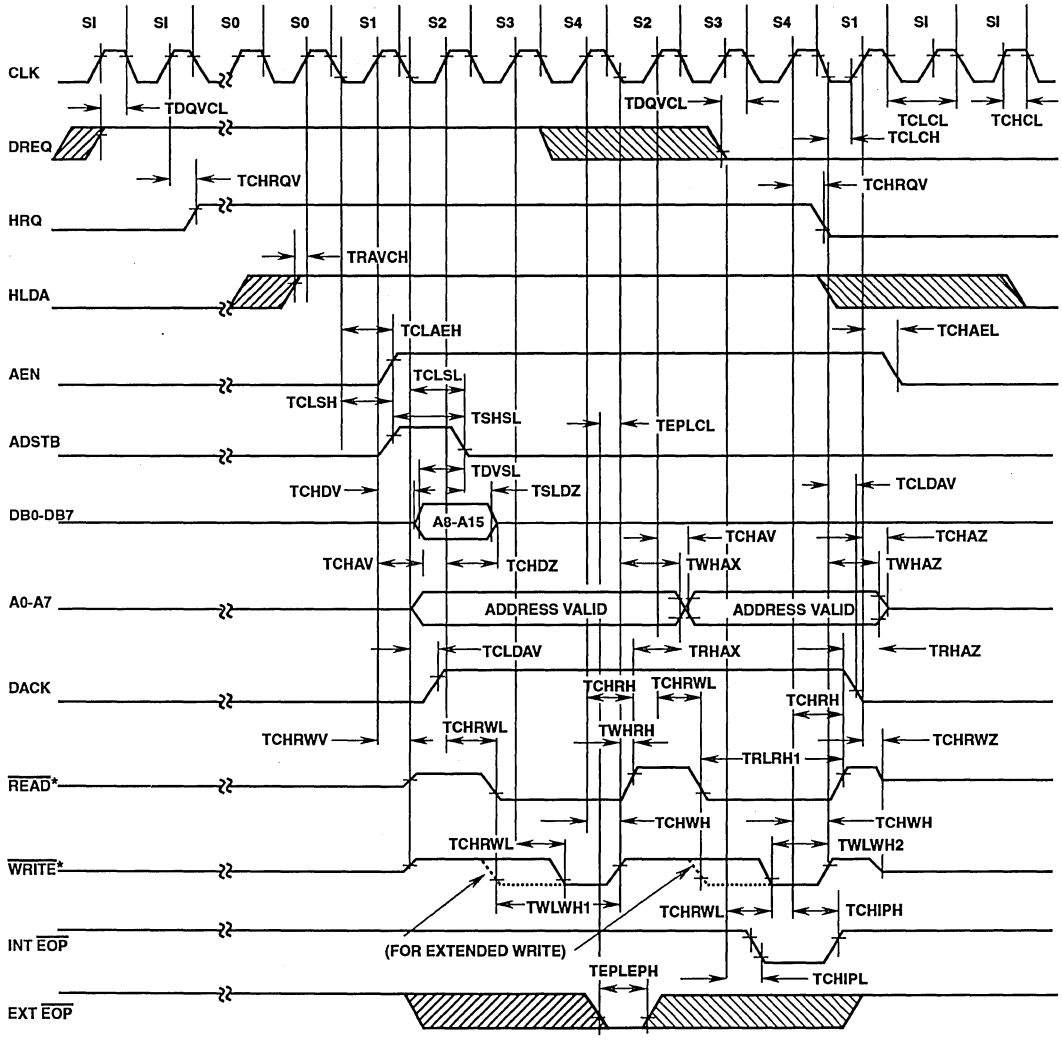


FIGURE 4. DMA TRANSFER

* READ refers to both IOR and MEMR outputs. WRITE refers to both IOW and MEMW outputs

Waveforms (Continued)

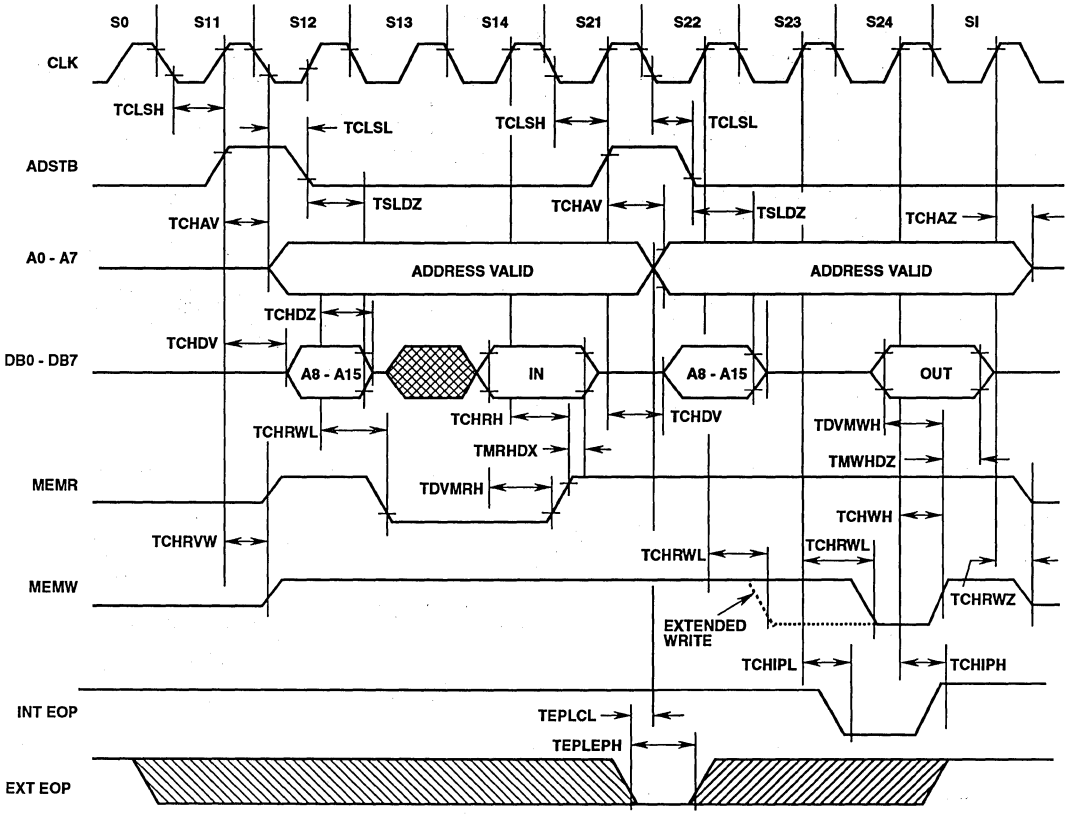


FIGURE 5. MEMORY-TO-MEMORY TRANSFER

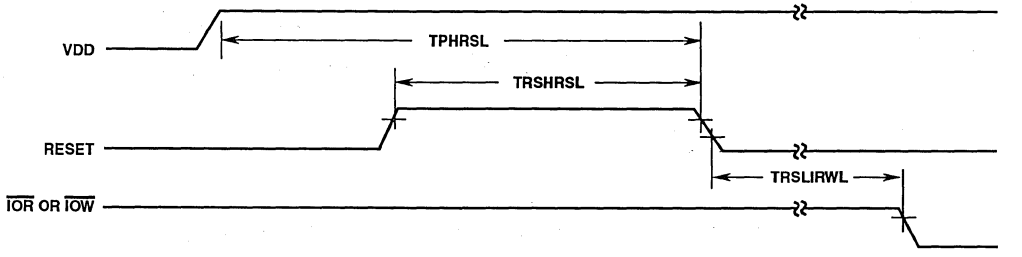


FIGURE 6. RESET

Waveforms (Continued)

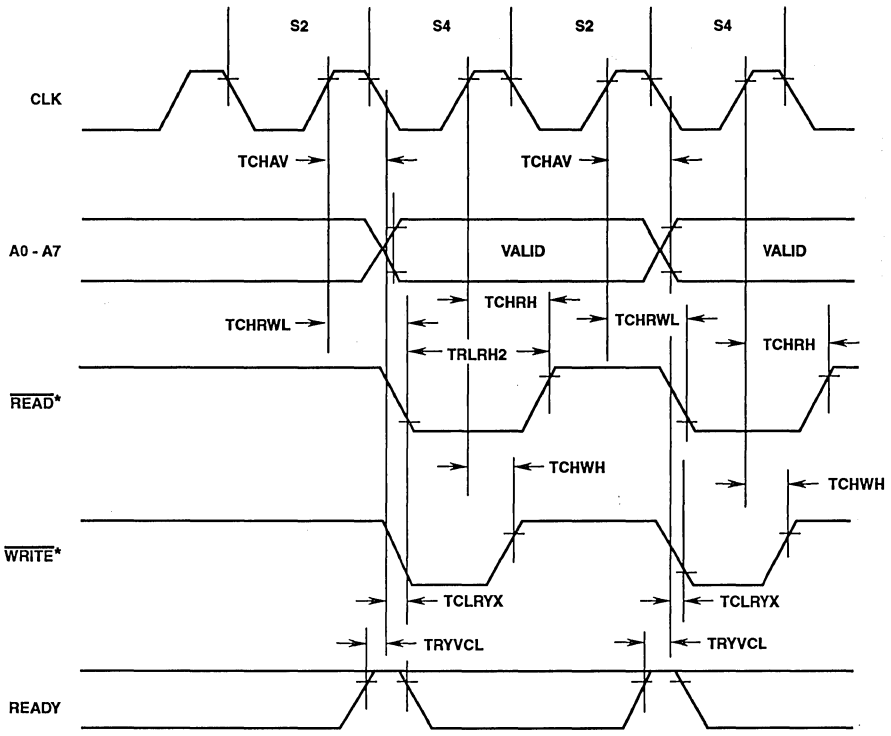
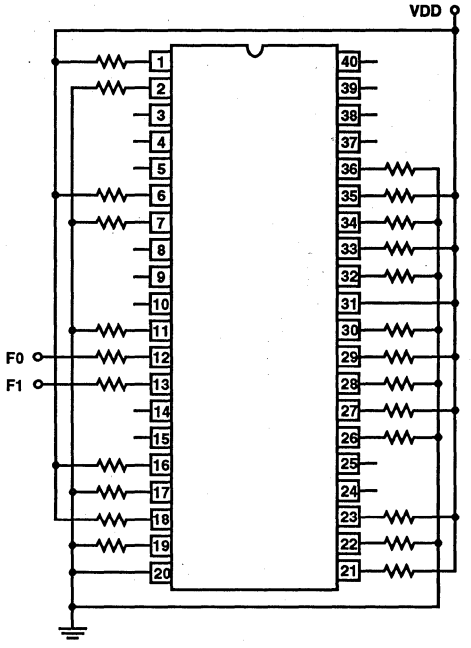


FIGURE 7. COMPRESSED TRANSFER

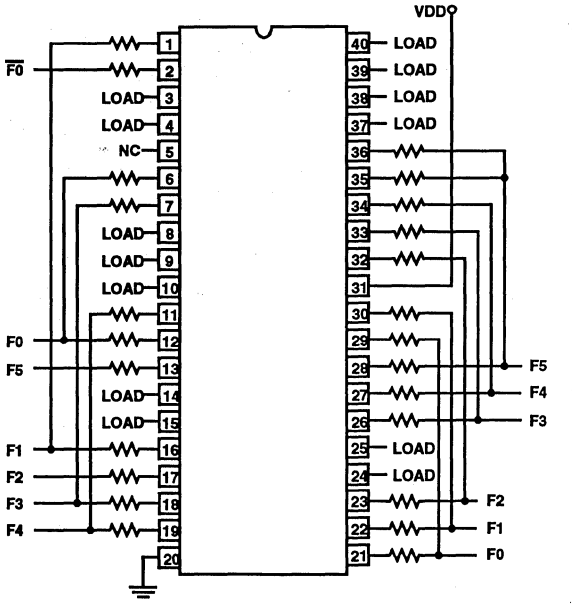
* $\overline{\text{READ}}$ refers to both $\overline{\text{IOR}}$ and $\overline{\text{MEMR}}$ outputs. $\overline{\text{WRITE}}$ refers to both $\overline{\text{IOW}}$ and $\overline{\text{MEMW}}$ outputs

Burn-In Circuits

HS-82C37ARH 40 PIN DIP



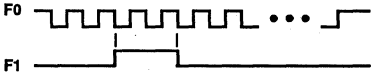
HS-82C37ARH 40 PIN DIP



STATIC CONFIGURATION

VDD = +6.0V ± 5%
T_A = +125°C Minimum
Resistors:
R1 = 10kΩ ± 10% (Pins 6, 7, 11-13, 16-19)
R2 = 2.7kΩ ± 5% (Pins 1, 2, 21-23, 26-30, 32-36)

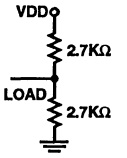
Part is Static Sensitive
Voltage Must be Ramped



START-UP TIMING

F0 is 50% duty cycle square wave pulse burst.
1.0kHz ≤ F0 ≤ 100kHz
10 cycles ≤ F0 Pulse Burst ≤ 1.0s
F1 = Single pulse with width equal to 2 cycles of F0
F1 is left Low after pulse burst
NOTE: F1 pulse occurs after start of F0 and ends before F0.
Input levels: 0.9VDD ≤ VIH ≤ VDD, -0.3V ≤ VIL ≤ 0.7V

F0 is left High after pulse burst

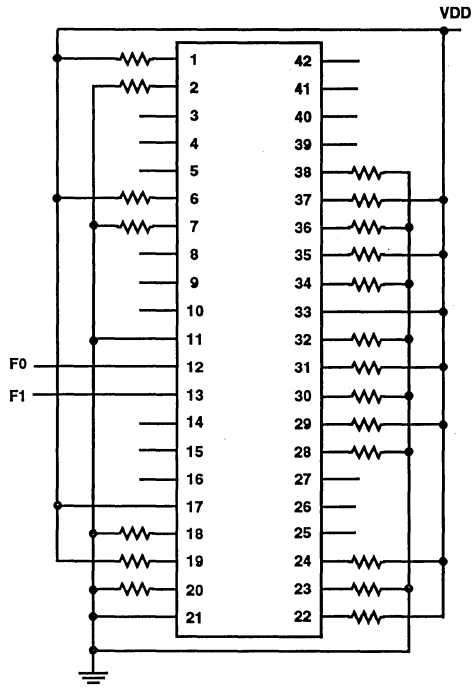


DYNAMIC CONFIGURATION

VDD = 6.5V ± 5% (Burn-In)
VDD = 6.0V ± 5% (Life Test)
T_A = +125°C Minimum
Part is Static Sensitive, Voltage Must be Ramped
Resistors:
R1 = 10kΩ ± 10% (Pins 6, 7, 11-13, 16-19)
R2 = 2.7kΩ ± 10% (Pins 1, 2, 21-23, 26-30, 32-36, and LOADS)

Burn-In Circuits (Continued)

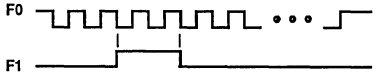
HS-82C37ARH 42 PIN FLATPACK



STATIC CONFIGURATION

VDD = +6.0V ± 5%
T_A = +125°C Minimum
Resistors:
R1 = 10kΩ ± 10% (Pins 6, 7, 11-13, 16-19)
R2 = 2.7kΩ ± 5% (Pins 1, 2, 21-23, 26-30, 32-36)

Part is Static Sensitive
Voltage Must be Ramped

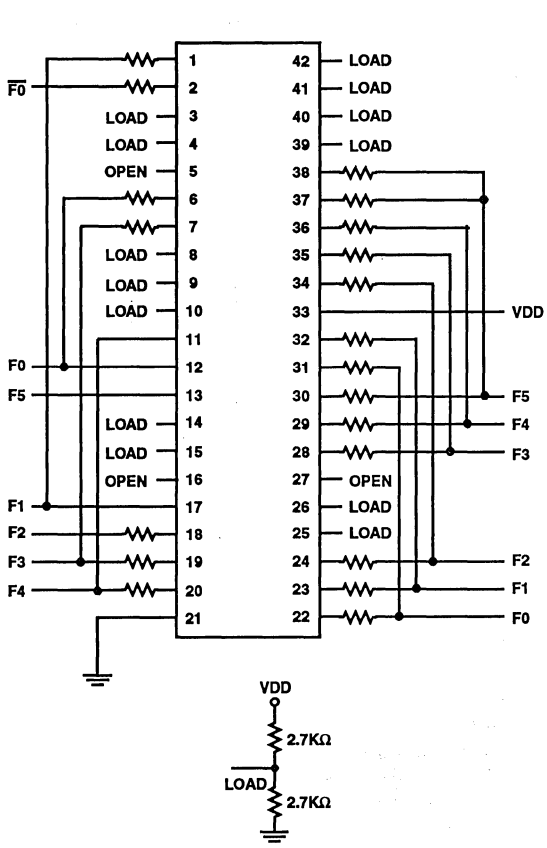


START-UP TIMING

F0 is 50% duty cycle square wave pulse burst.
1.0kHz ≤ F0 ≤ 100kHz
10 cycles ≤ F0 Pulse Burst ≤ 1.0s
F1 = Single pulse with width equal to 2 cycles of F0
F1 is left Low after pulse burst
NOTE: F1 pulse occurs after start of F0 and ends before F0.
Input levels: 0.9VDD ≤ VIH ≤ VDD, -0.3V ≤ VIL ≤ 0.7V

F0 is left High after pulse burst

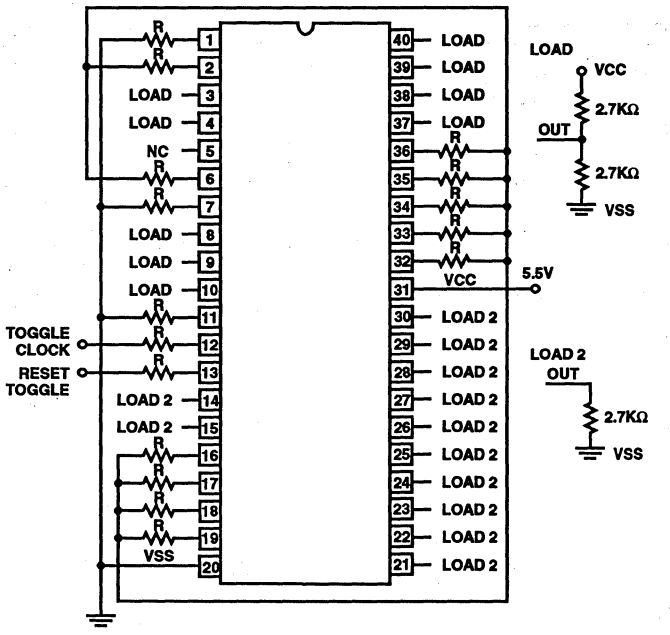
HS-82C37ARH 42 PIN FLATPACK



DYNAMIC CONFIGURATION

VDD = 6.5V ± 5% (Burn-In)
VDD = 6.0V ± 5% (Life Test)
T_A = +125°C Minimum
Part is Static Sensitive, Voltage Must be Ramped
Resistors:
R1 = 10kΩ ± 10% (Pins 6, 7, 11-13, 16-19)
R2 = 2.7kΩ ± 10% (Pins 1, 2, 21-23, 26-30, 32-36, and LOADS)

Irradiation Circuit



NOTE:

1. R = 47kΩ
2. Pins with Load: 3, 4, 8, 9, 10, 37-40
   Pins with Load2: 14, 15, 21-30
   Pins Brought Out: 12 (Clock), 13 (Reset)
3. VDD = 5.5V ± 0.5V
4. All Group E testing is performed in the Sidebrazed Ceramic DIP
5. Group E sample size is 2 dice per wafer

Harris - Space Level '-Q' Flow

SEM - Traceable to Diffusion Method 2018
Wafer Lot Acceptance Method 5007
Internal Visual Inspection
Gamma Radiation Assurance Tests Method 1019
100% Nondestructive Bond Pull Method 2023
Customer Pre-Cap Visual Inspection (Note 1)
Temperature Cycling Method 1010 Condition C
Constant Acceleration Method 2001 Y1 30KG
Particle Impact Noise Detection Method 2020, Condition A 20G
Serialization
X-Ray Inspection Method 2012 (Two Views)
Initial Electrical Tests (T0)
Static Burn-In 72 Hour, +125°C, Method 1015 Condition A
+25°C Interim Electrical Tests Subgroups 1, 7, 9 (T1)
Burn-In Delta Calculation (T0 - T1)
PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ
Dynamic Burn-In 240 Hours, +125°C Method 1015 Condition D
+25°C Electrical Tests (T2) Subgroups 1, 7, 9 (T2)
Burn-In Delta Calculation (T0 - T2)
PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ
Electrical Tests +125°C, -55°C
Group A Inspection Method 5005. 5% PDA (Note 3)
Fine and Gross Leak Tests Method 1014
Brand
Customer Source Inspection (Note 1)
Group B Inspection Method 5005 (Notes 1, 2)
Group D Inspection Method 5005 (Notes 1, 2)
External Visual Inspection Method 2009
Data Package Generation (Note 4)

NOTES:
1. These steps are optional, and if desired, should be indicated on the purchase order.
2. Group B and D data package contains Attributes Data plus Variables Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable.
4. '-Q' Data Pack Contains:
   Cover Sheet
   a) Purchase Order Number
   b) Customer Part Number
   c) Lot Date Code
   d) Harris Part Number
   e) Lot Number
   f) Quantity
   Certificate of Conformance (as found on shipper).
   Shippable serial number list.
   Test Attributes (including Group A) for all test temperatures.
5. Test Variables data for all read/record and delta operations.
   +25°C Initial Test (T0)
   +25°C Interim Test (T1)
   +25°C Final Test (T2)
   All +25°C Delta's (T1-T0, T2-T0)
   +125°C Final Test
   -55°C Final Test
   Wafer Lot Acceptance Report (includes SEM).
   X-Ray Report and Film.
   Radiation Testing Certificate of Conformance.
   Assembly Attributes (Post seal).

Harris - '-8' Flow

Internal Visual Inspection
Gamma Radiation Assurance Tests Method 1019
Customer Pre-Cap Visual Inspection (Note 1)
Temperature Cycling Method 1010 Condition C
Fine and Gross Leak Tests Method 1014
Constant Acceleration Method 2001 Y1 30KG
Initial Electrical Tests
Dynamic Burn-In 160 Hours, +125°C Method 1015 Condition D
+25°C Electrical Tests Subgroups 1, 7, 9
PDA Calculation: 5% Subgroups 1, 7
Electrical Tests +125°C, -55°C
Group A Inspection Method 5005. 5% PDA (Note 3)
Brand
Customer Source Inspection (Note 1)
Group C Inspection Method 5005 (Notes 1, 2)
Group D Inspection Method 5005 (Notes 1, 2)
External Visual Inspection Method 2009
Data Package Generation (Note 4)

NOTES:
1. These steps are optional, and if desired, should be indicated on the purchase.
2. Group B and D data package contains Attributes Data plus Variables Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable.
4. '-8' Data Pack Contains:
   Assembly Attributes (Post Seal).
   Test Attributes (Including Group A).
   Radiation Testing Certificate of Conformance.
   Certificate of Conformance (as found on shipper).

Metallization Topology

DIE DIMENSIONS:
215 x 232 mils x 19 ± 1 mil

METALLIZATION:
Type: Al/Si
Thickness: 11kÅ ± 2kÅ

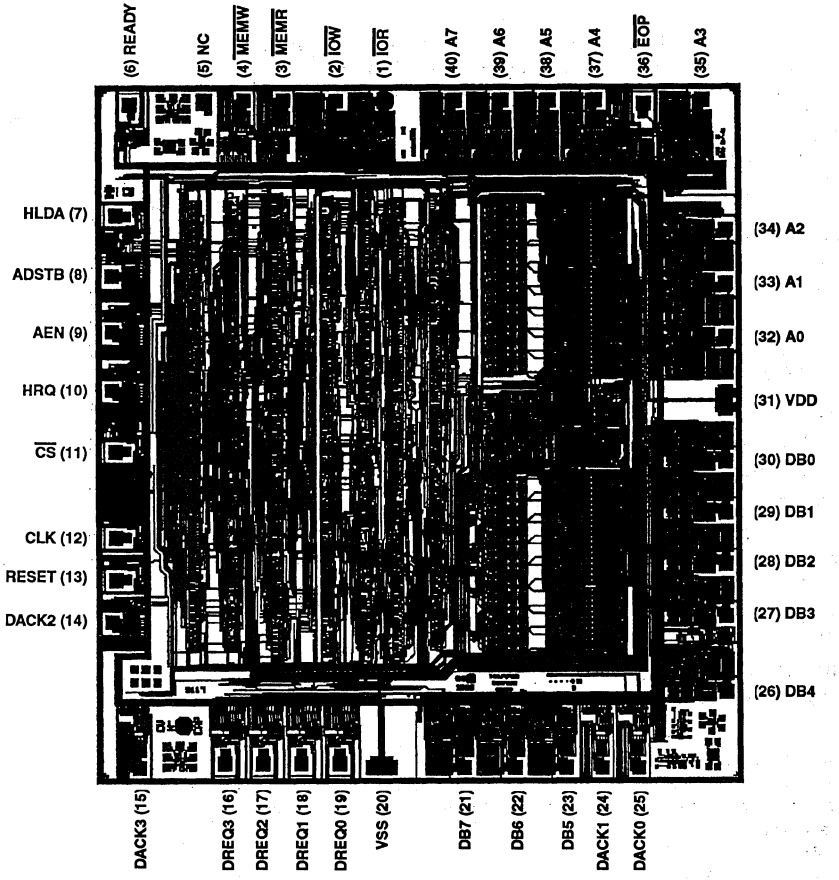
GLASSIVATION:
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold

WORST CASE CURRENT DENSITY:
7.9×10^4 A/cm^2

Metallization Mask Layout

HS-82C37ARH



Functional Description

The HS-82C37ARH Direct Memory Access Controller is designed to improve the data transfer rate in systems which must transfer data from an I/O device to memory, or move a block of memory to an I/O device. It will also perform memory-to-memory block moves, or fill a block of memory with data from a single location. Operating modes are provided to handle single byte transfers as well as discontinuous data streams, which allows the HS-82C37ARH to control data movement with software transparency.

The DMA controller is a state-driven address and control signal generator, which permits data to be transferred directly from an I/O device to memory or vice versa without ever being stored in a temporary register. This can greatly increase the data transfer rate for sequential operations, compared with processor moves or repeated string instructions. Memory-to-Memory operations require temporary internal storage of the data byte between generation of the source and destination addresses, so Memory-to-Memory transfers take place at less than half the rate of I/O operations, but still much faster than with central processor techniques. The maximum data transfer rate obtainable with the HS-82C37ARH is approximately 2.5 Mbytes/second, for an I/O operation using the compressed timing option and 5MHz clock.

The block diagram of the HS-82C37ARH is shown on page 2. The Timing and Control Block, Priority Block, and internal registers are the main components. Figure 8 lists the name and size of the internal registers. The Timing and Control Block derives internal timing from the CLOCK input, and generates external control signals. The Priority Encoder Block resolves priority contention between DMA channels requesting service simultaneously.

NAME	SIZE	NUMBER
Base Address Registers	16 Bits	4
Base Word Count Registers	16 Bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Registers	4 bits	1
Request Register	4 bits	1

FIGURE 1. HS-82C37ARH INTERNAL REGISTERS

DMA Operation

In a system, the HS-82C37ARH address and control outputs and data bus pins are basically connected in parallel with the system busses. An external latch is required for the upper address byte. While inactive, the controller's outputs are in a high impedance state. When activated by a DMA request and bus control is relinquished by the host, the HS-82C37ARH drives the busses and generates the control signals to perform the data transfer. The operation performed by activating one of the four DMA request inputs has previously been programmed into the controller via the Command, Mode, Address, and Word Count Registers.

For example, if a block of data is to be transferred from RAM to an I/O device, the starting address of the data is loaded into the HS-82C37ARH Current and Base Address Registers for a particular channel, and the length of the block is loaded into that channel's Word Count Register. The corresponding Mode Register is programmed for a Memory-to-I/O operation (read transfer), and various options are selected by the Command Register and other Mode Register bits. The channel's mask bit is cleared to enable recognition of a DMA request (DREQ). The DREQ can either be a hardware signal or a software command.

Once initiated, the block DMA transfer will proceed as the controller outputs the data address, simultaneous $\overline{\text{MEMR}}$ and $\overline{\text{IOW}}$ pulses, and selects an I/O device via the DMA acknowledge (DACK) outputs. The data byte flows directly from the RAM to the I/O device. After each byte is transferred, the address is automatically incremented (or decremented) and the word count is decremented. The operation is then repeated for the next byte. The controller stops transferring data when the Word Count Register underflows, or an external $\overline{\text{EOP}}$ is applied.

To further understand HS-82C37ARH operation, the states generated by each clock cycle must be considered. The DMA controller operates in two major cycles, Active and Idle. After being programmed, the controller is normally Idle until a DMA request occurs on an unmasked channel, or a software request is given. The HS-82C37ARH will then request control of the system busses and enter the Active cycle. The Active cycle is composed of several internal states, depending on what options have been selected and what type of operation has been requested.

The HS-82C37ARH can assume seven separate states, each composed of one full clock period. State I (SI) is the Idle state. It is entered when the HS-82C37ARH has no valid DMA requests pending, at the end of a transfer sequence, or when a Reset or Master Clear has occurred. While in SI, the DMA controller is inactive but may be in the Program Condition (being programmed by the processor.)

State 0 (S0) is the first state of a DMA service. The HS-82C37ARH has requested a hold but the processor has not yet returned an acknowledge. The HS-82C37ARH may still be programmed until it has received HLDA from the CPU. An acknowledge from the CPU will signal that DMA transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted between S2 or S3 and S4 by the use of the Ready line on the HS-82C37ARH.

Note that the data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active at the same time. The data is not read into or driven out of the HS-82C37ARH in I/O-to-memory or memory-to-I/O DMA transfers.

Memory-to-Memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two-digit numbers for identification. Eight states are required for a single transfer. The first four states (S11, S12, S13, S14 are used for the read-from-memory half and the last four states (S21, S22, S23, S24) for the write-to-memory half of the transfer.

Idle Cycle

When no channel is requesting service, the HS-82C37ARH will enter the Idle cycle and perform "SI" states. In this cycle, the HS-82C37ARH will sample the DREQ lines on the falling edge of every clock cycle to determine if any channel is requesting a DMA service.

Note that for standby operation where the clock has been stopped, DMA requests will be ignored. The device will respond to $\overline{CS}$ (chip select), in case of an attempt by the microprocessor to write or read the internal registers of the HS-82C37ARH. When $\overline{CS}$ is low and HLDA is low, the HS-82C37ARH enters the Program Condition. The CPU can now establish, change or inspect the internal definition of the part by reading from or writing to the internal registers.

The HS-82C37ARH may be programmed with the clock stopped, provided that HLDA is low and at least one rising clock edge has occurred after HLDA was driven low, so the controller is in an SI state. Address lines A0-A3 are inputs to the device and select which registers will be read or written. The $\overline{IOR}$ and $\overline{IOW}$ lines are used to select and time the read or write operations. Due to the number and size of the internal registers, an internal flip-flop is used to generate an additional bit of address. The bit is used to determine the upper or lower byte of the 16-bit Address and Word Count Registers. The flip-flop is reset by Master Clear or Reset. Separate software commands can also set or reset this flip-flop.

Special software commands can be executed by the HS-82C37ARH in the Program Condition. These commands are decoded as sets of addresses with $\overline{CS}$, $\overline{IOR}$, and $\overline{IOW}$. The commands do not make use of the data bus. Instructions include Set and Clear First/Last Flip-Flop, Master Clear, Clear Mode Register Counter, and Clear Mask Register.

Active Cycle

When the HS-82C37ARH is in the Idle cycle, and a software request or an unmasked channel requests a DMA service, the device will output an HRQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode - In Single Transfer mode, the device is programmed to make one transfer only. The word count will be decremented and the address decremented or incremented following each transfer. When the word count "rolls over" from zero to FFFFH, a terminal count (TC) bit in the Status Register is set, an $\overline{EOP}$ pulse is generated, and the channel will Autoinitialize if this option has been selected. If not programmed to Autoinitialize, the mask bit will be set, along with the TC bit and $\overline{EOP}$ pulse.

DREQ must be held active until DACK becomes active. If DREQ is held active throughout the single transfer (there-by triggering a second transfer), HRQ will still go inactive and release the bus to the system. Then it will again go active and, upon receipt of a new HLDA, another single transfer will be performed, unless a higher priority channel takes over. In HS-80C85RH or HS-80C86RH systems, this will ensure one full machine cycle execution between DMA transfers. Details of timing between the HS-82C37ARH and other bus control protocols will depend upon the characteristics of the microprocessor involved.

Block Transfer Mode - In Block Transfer Mode, the device is activated by DREQ or software request and continues making transfers during the service until a TC, caused by word count going to FFFFH, or an external End of Process ($\overline{EOP}$) is encountered. DREQ need only beheld active until DACK becomes active. Again, an Autoinitialization will occur at the end of the service if the channel has been programmed for that option.

Demand Transfer Mode - In Demand Transfer Mode the device continues making transfers until a TC or external $\overline{EOP}$ is encountered, or until DREQ goes inactive. Thus, transfers may continue until the I/O device has exhaust edits data capacity. After the I/O device has had a chance to catch up, the DMA service is reestablished by means of a DREQ. During the time between services when the micro-processor is allowed to operate, the intermediate values of address and word count are stored in the HS-82C37ARH Current Address and Current Word Count Registers. Higher priority channels may intervene in the demand process, once DREQ has gone inactive. Only an EOP can cause an Autoinitialization at the end of the service. EOP is generated either by TC or by an external signal.

Cascade Mode - This mode is used to cascade more than one HS-82C37ARH for simple system expansion. The HRQ and HLDA signals from the additional HS-82C37ARH are connected to the DREQ and DACK signals respectively of a channel for the initial HS-82C37ARH. This allows the DMA requests of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests. Since the cascade channel of the initial HS-82C37ARH is used only for prioritizing the additional device, it does not output an address or control signals of its own so that there is no conflict with the cascaded device. The HS-82C37ARH will respond to DREQ and generate DACK but all other outputs except HRQ will be disabled. An external $\overline{EOP}$ will be ignored by the initial device, but will have the usual effect on the added device.

Figure 9 shows two additional devices cascaded with an initial device using two of the previous channels. This forms a two-level DMA system. More HS-82C37ARHs could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices, forming a third level.

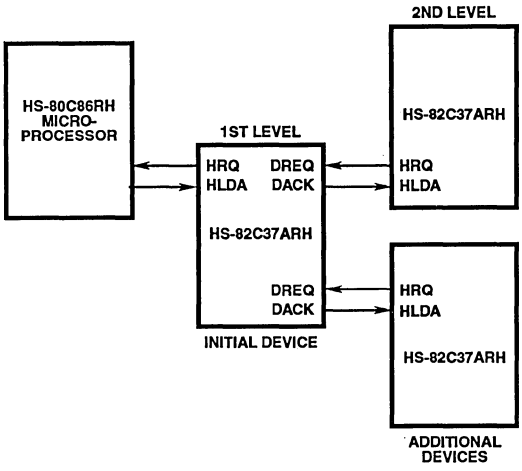


FIGURE 9. CASCADED HS-82C37ARHs

When programming cascaded controllers, start with the first level (closest to the microprocessor). After RESET, the DACK outputs are programmed to be active low and are held in the high state. If they are used to drive HLDA directly, the second level device(s) cannot be programmed until DACK polarity is selected as active high on the initial device. Also, the initial device's mask bits function normally on cascaded channels, so they may be used to inhibit second-level services.

Transfer Types

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from an I/O device to the memory by activating $\overline{MEMW}$ and $\overline{IOR}$. Read transfers move data from memory to an I/O device by activating $\overline{MEMR}$ and $\overline{IOW}$.

Verify transfers are pseudo-transfers. The HS-82C37ARH operates as in Read or Write transfers generating addresses and responding to $\overline{EOP}$, etc., however the memory and I/O control lines all remain inactive. Verify mode is not permitted for Memory-to-Memory operation. Ready is ignored during Verify transfers.

Autoinitialize - By programming a bit in the Mode Register, a channel may be set up as an Autoinitialize channel. During Autoinitialization, the original values of the Current Address and Current Word Count Registers are automatically restored from the Base Address and Base Word Count Registers of that channel following $\overline{EOP}$. The base registers are loaded simultaneously with the current registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in Autoinitialize. Following Autoinitialization, the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected, or software request made.

Memory-to-Memory - To perform block moves of data from one memory address space to another with minimum of program effort and time, the HS-82C37ARH includes a Memory-to-Memory transfer feature. Programming a bit in the Command Register selects channels 0 and 1 to operate as Memory-to-Memory transfer channels.

The transfer is initiated by setting the software or hardware DREQ for channel 0. The HS-82C37ARH requests a DMA service in the normal manner. After HLDA is true, the device, using four-state transfers in Block Transfer Mode, reads data from the memory. The channel 0 Current Address Register is the source for the address used and is decremented or incremented in the normal manner. The data byte read from the memory is stored in the HS-82C37ARH internal Temporary Register. Another four-state transfer moves the data to memory using the address in channel 1's Current Address Register and incrementing or decrementing it in the normal manner. The channel 1 Current Word Count Register is decremented.

When the word count of channel 1 goes to FFFFH, a TC is generated causing an $\overline{EOP}$ output terminating the service. Channel 0 word count decrementing to FFFFH will not set the channel 0 TC bit in the Status Register or generate an $\overline{EOP}$ in this mode. It will cause an Autoinitialization of channel 0, if that option has been selected.

If full Autoinitialization for a Memory-to-Memory operation is desired, the channel 0 and channel 1 word counts must be set equal before the transfer begins. Otherwise, if channel 0 underflows before channel 1, it will Autoinitialize and set the data source address back to the beginning of the block. If the channel 1 word count underflows before channel 0, the Memory-to-Memory DMA service will terminate, and channel 1 will Autoinitialize but channel 0 will not.

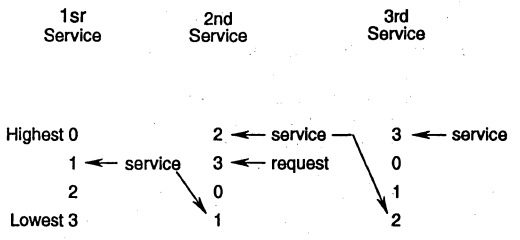
In Memory-to-Memory Mode, Channel 0 may be programmed to retain the same address for all transfers. This allows a single byte to be written to a block of memory. This channel 0 address hold feature is selected by bit 1 in the Command Register.

The HS-82C37ARH will respond to external $\overline{EOP}$ signals during Memory-to-Memory transfers, but will only relinquish the system busses after the transfer is complete (i.e., after an S24 state). Data comparators in block search schemes may use this input to terminate the service when a match is found. The timing of Memory-to-Memory transfers is found in Figure 5. Memory-to-Memory operations can be detected as an active AEN with no DACK outputs.

Priority - The HS-82C37ARH has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their numbers. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0. After the recognition of any one channel for service, the other channels are prevented from interfering with the service until it is completed.

The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly. The next lower channel from the channel serviced has highest priority on the following request: Priority rotates every time control of the system busses is returned to the processor.

Rotating Priority



With Rotating Priority in a single chip DMA system, any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. This prevents any one channel from monopolizing the system.

Regardless of which priority scheme is chosen, priority is evaluated every time a HLDA is returned to the HS-82C37ARH.

Compressed Timing - In order to achieve even greater throughput where system characteristics permit, the HS-82C37ARH can compress the transfer time to two clock cycles. From Figure 4 it can be seen that state S3 is used to extend the access time of the read pulse. By removing state S3, the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 states will still occur when A8-A15 need updating (see Address Generation). Timing for compressed transfers is found in Figure 7. $\overline{EOP}$ will be output in S2 if compressed timing is selected. Compressed Timing is not allowed for Memory-to-Memory transfers.

Address Generation - In order to reduce pin count, the HS-82C37ARH multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a three-state enable. The lower order address bits are output by the HS-82C37ARH directly. Lines A0-A7 should be connected to the address bus. Figure 4 shows the time relationships between CLK, AEN, ADSTB, DB0-DB7 and A0-A7.

During Block and Demand Transfer Mode service, which include multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A7 to A8 takes place in the normal sequence of addresses. To save time and speed transfers, the HS-82C37ARH executes S1 states only when updating of A8-A15 in the latch is necessary. This means for long services, S1 states and Address Strobes may occur only once every 256 transfers, a savings of 255 clock cycles for each 256 transfers.

Programming

The HS-82C37ARH will accept programming from the host processor anytime that HLDA is inactive, and at least one rising clock edge has occurred after HLDA went low. It is the responsibility of the host to assure that programming and HLDA are mutually exclusive.

Note that a problem can occur if a DMA request occurs on an unmasked channel while the HS-82C37ARH is being programmed. For instance, the CPU may be starting to reprogram the two byte Address Register of channel 1 when channel 1 receives a DMA request. If the HS-82C37ARH is enabled (bit 2 in the command register is 0), and channel 1 is unmasked, a DMA service will occur after only one byte of the Address Register has been reprogrammed. This condition can be avoided by disabling the controller (setting bit 2 in the Command Register) or masking the channel before programming any of its registers. Once the programming is complete, the controller can be enabled/unmasked.

After power-up it is suggested that all internal locations be loaded with some known value, even if some channels are unused. This will aid in debugging.

Register Description

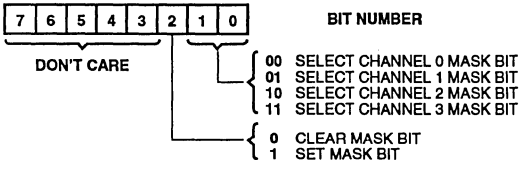
Current Address Register - Each channel has a 16-bit Current Address Register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the values of the address are stored in the Current Address Register during the transfer. This register is written or read by the microprocessor in successive 8-bit bytes. It may also be reinitialized by an Autoinitialize back to its original value. Autoinitialize takes place only after an $\overline{EOP}$. In Memory-to-Memory Mode, the channel 0 Current Address Register can be prevented from incrementing or decrementing by setting the address hold bit in the Command Register.

Current Word Register - Each channel has a 16-Bit Current Word Count Register. This register determines the number of transfers to be performed. The actual number of transfers will be one more than the number programmed in the Current Word Count Register (i.e., programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer. When the value in the register goes from zero to FFFFH, a TC will be generated. This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition. Following the end of a DMA service it may also be reinitialized by an Autoinitialization back to its original value. Autoinitialization can occur only when an $\overline{EOP}$ occurs. If it is not Autoinitialized, this register will have a count of FFFFH after TC.

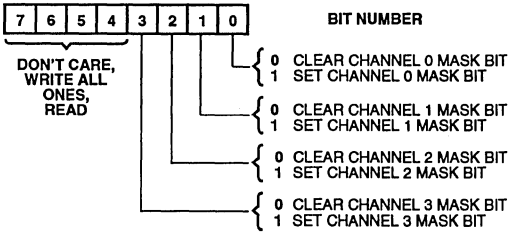
Base Address and Base Word Count Registers - Each channel has a pair of Base Address and Base Word Count Registers. These 16-bit registers store the original value of their associated current registers. During Autoinitialization, these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes in the Program Condition by the microprocessor. These registers cannot be read by the microprocessor.

Mask Register - Each channel has associated with it a mask bit which can be set to disable an incoming DREQ. Each mask bit is set when its associated channel produces an $\overline{EOP}$ if the channel is not programmed to Autoinitialize. Each bit of the 4-bit Mask Register may also be set or cleared separately or simultaneously under soft-ware control. The entire register is also set by a Reset or Master Clear. This disables all hardware DMA requests until a clear Mask Register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request Register. Refer to the following table and Figure 10 for details. When reading the Mask Register, bits 4-7 will always read as logical ones, and bits 0-3 will display the mask bits of channel 0-3, respectively. The 4 bits of the Mask Register may be cleared simultaneously by using the Clear Mask Register command (see software commands section).

Mask Register

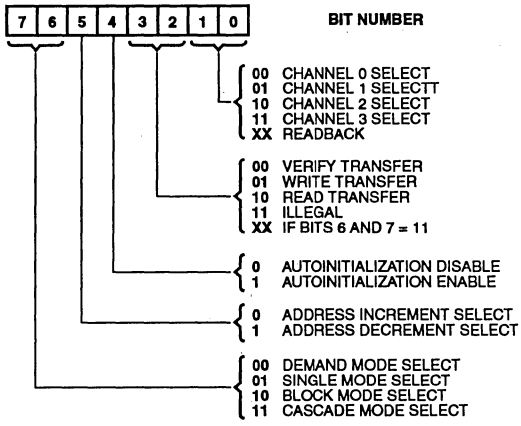


All four bits of the Mask Register may also be written with a single command.



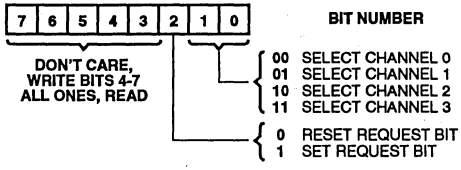
Mode Register - Each channel has a 6-bit Mode Register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode Register is to be written. When the processor reads a Mode Register, bits 0 and 1 will both be ones. See the adjacent table and Figure 10 for Mode Register functions and addresses.

Mode Register



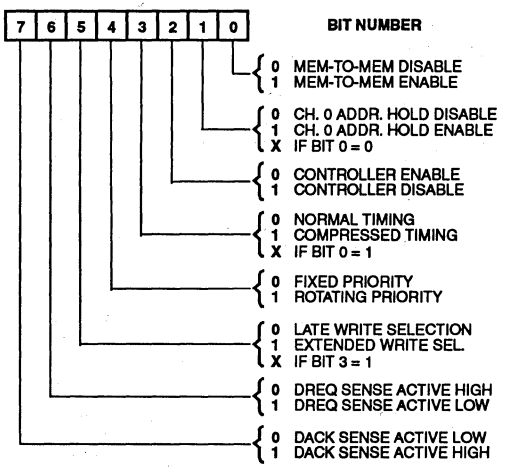
Request Register - The HS-82C37ARH can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request Register. These are non-maskable and subject to prioritization by the Priority Encoder network. Each register bit is set or reset separately under software control. The entire register is cleared by a Reset. To set or reset a bit, the software loads the proper form of the data word. See Figure 10 for register address coding, and the following table for Request Register format. A software request for DMA operation can be made in Block or Single Modes. For Memory-to-Memory transfers, the software request for channel 0 should be set. When reading the Request Register, bits 4-7 will always read as ones, and bits 0-3 will display the request bits of channels 0-3 respectively.

Request Register



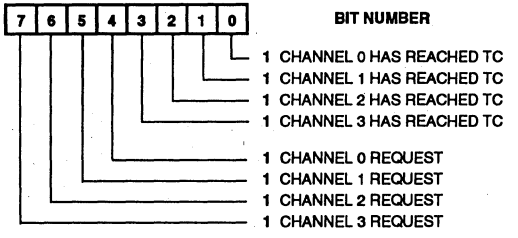
Command Register - This 8-bit register controls the operation of the HS-82C37ARH. It is programmed by the microprocessor and is cleared by Reset or a Master Clear instruction. The adjacent table lists the function of the command bits. See Figure 10 for Read and Write addresses.

Command Register



Status Register - The Status Register contains information about the present status of the HS-82C37ARH and can be read by the microprocessor. This information includes which channels have reached a terminal count and which channels have pending DMA requests. Bits 0-3 are set every time a TC is reached by that channel or an external $\overline{EOP}$ is applied. These bits are cleared upon Reset, Master Clear, and on each Status Read. Bits 4-7 are set whenever their corresponding channel is requesting service, regardless of the mask bit state. If the mask bits are set, software can poll the Status Register to determine which channels have DREQs, and selectively clear a mask bit, thus allowing user defined service priority. Status bits 4-7 are updated while the clock is high, and latched on the falling edge. Status Bits 4-7 are cleared upon Reset or Master Clear.

Status Register



Temporary Register - The Temporary Register is used to hold data during Memory-to-Memory transfers. Following the completion of the transfer, the last word moved can be read by the microprocessor by accessing this register. The Temporary Register always contains the last byte transferred in the previous Memory-to-Memory operation, unless cleared by a Reset or Master Clear.

OPERATION	A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$
Read Status Register	1	0	0	0	0	1
Write Command Register	1	0	0	0	1	0
Read Request Register	1	0	0	1	0	1
Write Request Register	1	0	0	1	1	0
Read Command Register	1	0	1	0	0	1
Write Single Mask Bit	1	0	1	0	1	0
Read Mode Register	1	0	1	1	0	1
Write Mode Register	1	0	1	1	1	0
Set Byte Pointer F/F	1	1	0	0	0	1
Clear Byte Pointer F/F	1	1	0	0	1	0
Read Temporary Register	1	1	0	1	0	1
Master Clear	1	1	0	1	1	0
Clear Mode Reg. Counter	1	1	1	0	0	1
Clear Mask Register	1	1	1	0	1	0
Read All Mask Bits	1	1	1	1	0	1
Write All Mask Bits	1	1	1	1	1	0

FIGURE 10. SOFTWARE COMMAND CODES AND REGISTER CODES

Software Commands

There are special software commands which can be executed by reading or writing to the HS-82C37ARH. These commands do not depend on the specific data pattern on the data bus, but are activated by the I/O operation itself. On read type commands, the data value is not guaranteed. These commands are:

Clear First/Last Flip-Flop: This command is executed prior to writing or reading new address or word count information to the HS-82C37ARH. This initializes the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

Set First/Last Flip-Flop: This command will set the flip-flop to select the high byte first on read and write operations to Address and Word Count registers.

Master Clear: This software instruction has the same effect as the hardware Reset. The Command, Status, Request, and Temporary Registers, and Internal First/Last Flip-Flop and Mode Register Counter are cleared and the Mask Register is set. The HS-82C37ARH will enter the Idle cycle.

Clear Mask Register: This command clears the mask bits of all four channels, enabling them to accept DMA requests.

Clear Mode Register Counter: Since only one address location is available for reading the Mode Registers, an internal two-bit counter has been included to select Mode Registers during read operations. To read the Mode Registers, first execute the Clear Mode Register Counter command, then do consecutive reads until the desired channel is read. Read order is channel 0 first, channel 3 last. The lower two bits on all Mode Registers will read as ones.

External $\overline{EOP}$ Operation

The $\overline{EOP}$ pin is a bidirectional, open drain pin which may be driven by external signals to terminate DMA operation. Because $\overline{EOP}$ is an open drain pin an external pull-up resistor is required. The value of the external pull-up resistor used should guarantee a rise time of less than 125ns. It is important to note that the HS-82C37ARH will not accept external $\overline{EOP}$ signals when it is in an SI (Idle)state. The controller must be active to latch EXT $\overline{EOP}$. Once latched, the EXT $\overline{EOP}$ will be acted upon during the next S2 state, unless the HS-82C37ARH enters an Idle state first. In the latter case the latched $\overline{EOP}$ is cleared. External $\overline{EOP}$ pulses occurring between active DMA transfers in demand mode will not be recognized, since the HS-82C37ARH is in an SI state.

CHANNEL	REGISTER	OPERATION	SIGNALS							INTERNAL FLIP-FLOP	DATA BUS DB0-DB7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0		
0	Base and Current Address	Write	0 0	1 1	0 0	0 0	0 0	0 0	0 0	0 1	A0-A7 A8-A15
	Current Address	Read	0 0	0 0	1 1	0 0	0 0	0 0	0 0	0 1	A0-A7 A8-A15
	Base and Current Word Count	Write	0 0	1 1	0 0	0 0	0 0	0 0	1 1	0 1	W0-W7 W8-W15
	Current Word Count	Read	0 0	0 0	1 1	0 0	0 0	0 0	1 1	0 1	W0-W7 W8-W15
1	Base and Current Address	Write	0 0	1 1	0 0	0 0	0 0	1 1	0 0	0 1	A0-A7 A8-A15
	Current Address	Read	0 0	0 0	1 1	0 0	0 0	1 1	0 0	0 1	A0-A7 A8-A15
	Base and Current Word Count	Write	0 0	1 1	0 0	0 0	0 0	1 1	1 1	0 1	W0-W7 W8-W15
	Current Word Count	Read	0 0	0 0	1 1	0 0	0 0	1 1	1 1	0 1	W0-W7 W8-W15
2	Base and Current Address	Write	0 0	1 1	0 0	0 0	1 1	0 0	0 0	0 1	A0-A7 A8-A15
	Current Address	Read	0 0	0 0	1 1	0 0	1 1	0 0	0 0	0 1	A0-A7 A8-A15
	Base and Current Word Count	Write	0 0	1 1	0 0	0 0	1 1	0 0	1 1	0 1	W0-W7 W8-W15
	Current Word Count	Read	0 0	0 0	1 1	0 0	1 1	0 0	1 1	0 1	W0-W7 W8-W15
3	Base and Current Address	Write	0 0	1 1	0 0	0 0	1 1	1 1	0 0	0 1	A0-A7 A8-A15
	Current Address	Read	0 0	0 0	1 1	0 0	1 1	1 1	0 0	0 1	A0-A7 A8-A15
	Base and Current Word Count	Write	0 0	1 1	0 0	0 0	1 1	1 1	1 1	0 1	W0-W7 W8-W15
	Current Word Count	Read	0 0	0 0	1 1	0 0	1 1	1 1	1 1	0 1	W0-W7 W8-W15

FIGURE 11. WORD COUNT AND ADDRESS REGISTER COMMAND CODES

Application Information

Figure 12 shows an application for a DMA system utilizing the HS-82C37ARH DMA controller and the HS-80C86RH Microprocessor. In this application, the HS-82C37ARH DMA controller is used to improve system performance by allowing an I/O device to transfer data directly to or from system memory.

Components

The system clock is generated by the HS-82C85RH clock controllers generator and is inverted to meet the clock high and low times required by the HS-82C37ARH DMA controller. The four OR gates are used to support the HS-80C86RH Microprocessor in minimum mode by producing the control signals used by the processor to access memory or I/O. A decoder is used to generate chip select for the DMA controller and memory. The HS-82C37ARH multiplexes the most significant bits of the address on its data outputs (DB0 - 7), so the 82C82 octal latch is used to demultiplex the address. A three-state inverter is used to generate the $\overline{BHE}$ signal using the A0 output of the HS-82C37ARH. Hold Acknowledge (HLDA) and Address Enable (AEN) are "ORed" together and used to deactivate the microprocessors 82C82 transceiver to insure that the DMA controller does not have bus contention with the microprocessor.

Operation

A DMA request (DREQ) is generated by the I/O device. After receiving the DMA request, the DMA controller will issue a Hold Request (HRQ) to the processor. The system busses are not released to the DMA controller until a Hold Acknowledge (HLDA) signal is returned to the DMA controller from the HS-80C86RH processor. After the Hold Acknowledge has been received, addresses and control signals are generated by the DMA controller to accomplish the DMA transfers. Data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active. Note that data is not read into or driven out of the DMA controller in I/O-to-Memory or Memory-to-I/O data transfers.

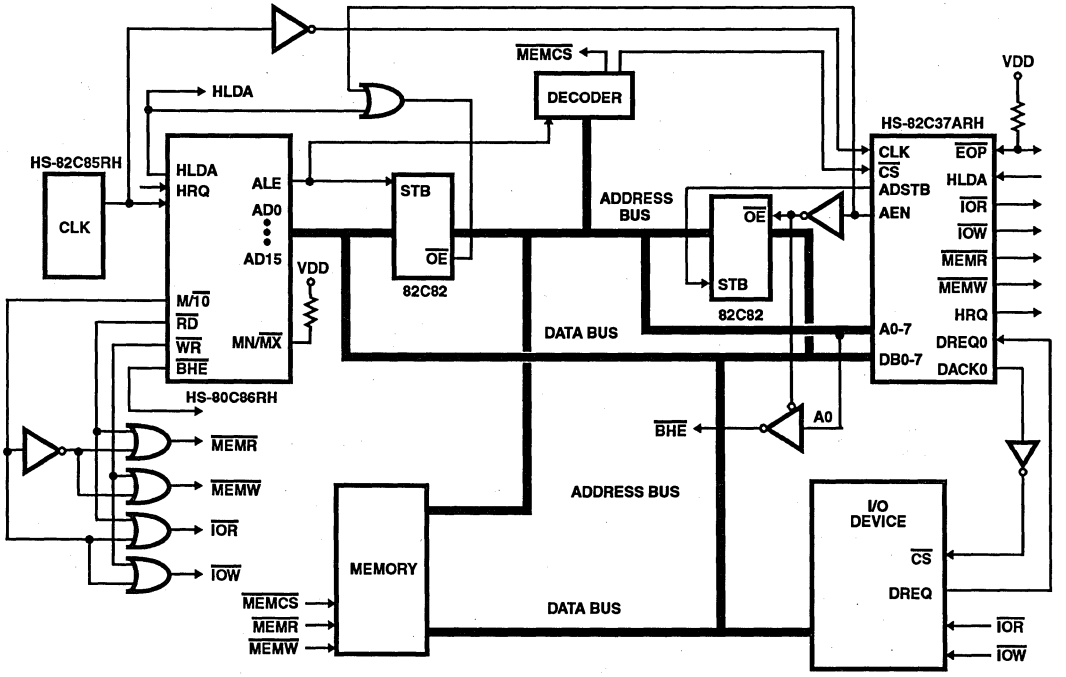


FIGURE 12. APPLICATION FOR DMA SYSTEM

HARRIS SEMICONDUCTOR

HS-82C54RH

Radiation Hardened CMOS Programmable Interval Timer

December 1992

Features

- Radiation Hardened
  - Total Dose > 10^5 RAD(Si)
  - Transient Upset > 10^8 RAD(Si)/sec
  - Latch Up Free EPI-CMOS
  - Functional After Total Dose 1 x 10^6 RAD(Si)
- Low Power Consumption
  - IDDSB = 20μA
  - IDDOP = 12mA
- Pin Compatible with NMOS 8254 and the Harris 82C54
- High Speed, "No Wait State" Operation with 5MHz HS-80C86RH
- Three Independent 16-Bit Counters
- Six Programmable Counter Modes
- Binary or BCD Counting
- Status Read Back Command
- Hardened Field, Self-Aligned, Junction Isolated CMOS Process
- Single 5V Supply
- Military Temperature Range -55°C to +125°C

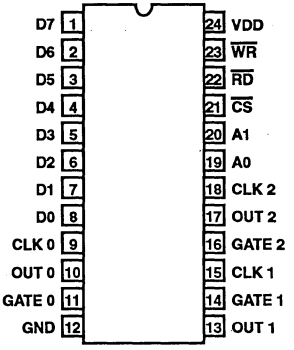
Description

The Harris HS-82C54RH is a high performance, radiation hardened CMOS version of the industry standard 8254 and is manufactured using a hardened field, self-aligned silicon gate CMOS process. It has three independently programmable and functional 16-bit counters, each capable of handling clock input frequencies of up to 5MHz. Six programmable timer modes allow the HS-82C54RH to be used as an event counter, elapsed time indicator, a programmable one-shot, or for any other timing application. The high performance, radiation hardness, and industry standard configuration of the HS-82C54RH make it compatible with the HS-80C86RH radiation hardened microprocessor.

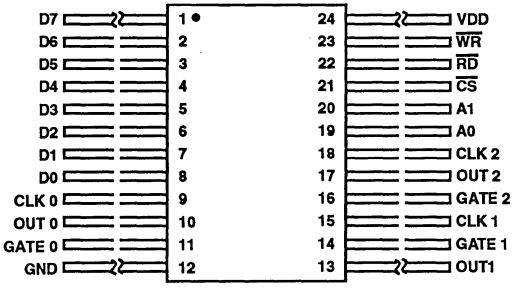
Static CMOS circuit design insures low operating power. The Harris hardened field CMOS process results in performance equal to or greater than existing radiation resistant products at a fraction of the power.

Pinouts

24 PIN BRAZED SEAL DIP
CASE OUTLINE D3, CONFIGURATION 3
TOP VIEW



24 PIN BRAZED SEAL FLATPACK
CASE OUTLINE F6A, CONFIGURATION 2
TOP VIEW



11 μPROCESSOR PERIPHERALS

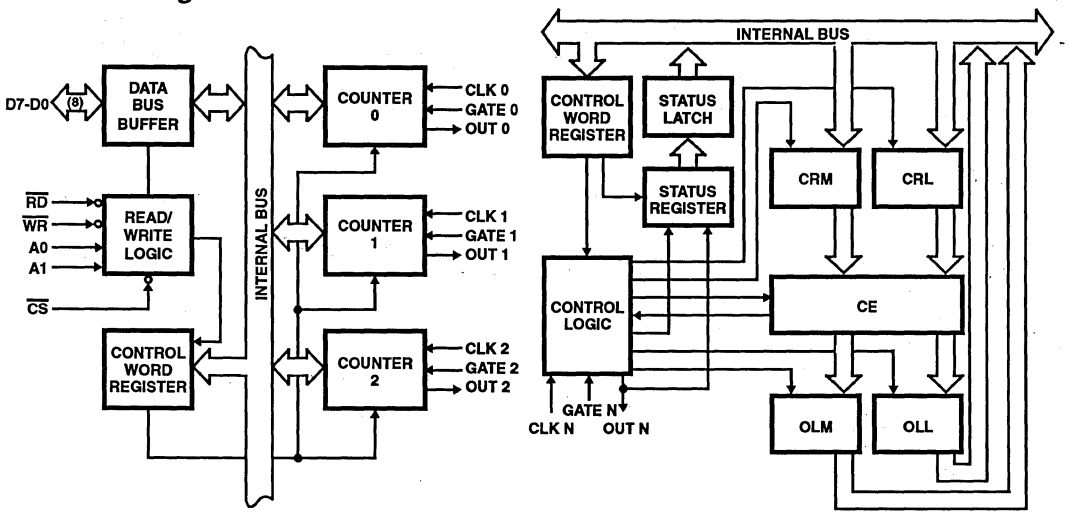
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3043

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
D7-D0	1-8	I/O	DATA: Bi-directional three state data bus lines, connected to system data bus.
CLK 0	9	I	CLOCK 0: Clock input of Counter 0.
OUT 0	10	O	OUT 0: Output of Counter 0.
GATE 0	11	I	GATE 0: Gate input of Counter 0.
GND	12		GROUND: Power supply connection.
OUT 1	13	O	OUT 1: Output of Counter 1.
GATE 1	14	I	GATE 1: Gate input of Counter 1.
CLK 1	15	I	CLOCK 1: Clock input of Counter 1.
GATE 2	16	I	GATE 2: Gate input of Counter 2.
OUT 2	17	O	OUT 2: Output of Counter 2.
CLK 2	18	I	CLOCK 2: Clock input of Counter 2.
A0, A1	19-20	I	ADDRESS: Select inputs for one of the three counters or Control Word Register for read/write operations. Normally connected to the system address bus. **A1 A0 Selects** 0 0 Counter 0 0 1 Counter 1 1 0 Counter 2 1 1 Control Word Register
$\overline{CS}$	21	I	CHIP SELECT: A low on this input enables the HS-82C54RH to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
$\overline{RD}$	22	I	READ: This input is low during CPU read operations.
$\overline{WR}$	23	I	WRITE: This input is low during CPU write operations.
VDD	24		VDD: The +5V power supply pin. A 0.1µF capacitor between pins 12 and 24 is recommended for decoupling.

Functional Diagram



Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage
Applied for all Grades ..... VSS-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 2.4mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Brazed Seal DIP Package	58.5°C/W	12.9°C/W
Brazed Seal Flatpack Package	72.7°C/W	10.2°C/W

Maximum Package Power Dissipation at +125°C
Brazed Seal DIP Package 0.86W
Brazed Seal Flatpack Package 0.64W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0V to +0.8V
Input High Voltage (VIH) ..... VDD -1.5V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
TTL Output High Current	IOH1	VDD = 4.5V, VO = 3.0V, VIN = 0V or 4.5V	1, 2, 3	-55°C, +25°C, +125°C	-2.5	-	mA
CMOST Output High Current	IOH2	VDD = 4.5V, VO = 4.1V, VIN = 0V or 4.5V	1, 2, 3	-55°C, +25°C, +125°C	-100	-	µA
Output Low Current	IOL	VDD = 4.5V, VO = 0.4V, VIN = 0V or 4.5V	1, 2, 3	-55°C, +25°C, +125°C	2.5	-	mA
Input Leakage Current	IIL or IIH	VDD = 5.5V, VIN = 0V or 5.5V Pins: 9, 11, 14-16, 18-23	1, 2, 3	-55°C, +25°C, +125°C	-1.0	1.0	µA
Output Leakage Current	IOZL or IOZH	VDD = 5.5V, VIN = 0V or 5.5V Pins: 1-8	1, 2, 3	-55°C, +25°C, +125°C	-10	10	µA
Standby Power Supply Current	IDDSB	VDD = 5.5V, VIN = GND or VDD IO = 0mA, Counters Programmed	1, 2, 3	-55°C, +25°C, +125°C	-	20.0	µA
Operating Power Supply Current	IDDOP	VDD = 5.5V, VIN = GND or VDD IO = 0mA, CLK1 = CLK2 = CLK3 = 5MHz	1, 2, 3	-55°C, +25°C, +125°C	-	12.0	mA
Functional Tests	FT	VDD = 4.5V and 5.5V, VIN = GND or VDD, f = 1MHz	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-
Noise Immunity Functional Test	FN	VDD = 5.5V, VIN = GND or VDD - 1.5 and VDD = 4.5V, VIN = 0.8V or VDD	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

AC's Tested at Worst Case VDD (s), Guaranteed Over Full Operating Range.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Stable Before $\overline{RD}$	TAVRL	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	75	-	ns
$\overline{CS}$ Stable Before $\overline{RD}$	TSLRL	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
Address Hold Time After $\overline{RD}$	TRHAX	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
$\overline{RD}$ Pulse Width	TRLRH	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	240	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

AC's Tested at Worst Case VDD (s), Guaranteed Over Full Operating Range.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Data Delay from $\overline{RD}$	TRLDV	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	200	ns
Command Recovery Time	TRHRL	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	320	-	ns
WRITE CYCLE							
Address Stable Before $\overline{WR}$	TAVWL	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
$\overline{CS}$ Stable Before $\overline{WR}$	TSLWL	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
Address Hold Time After $\overline{WR}$	TWHAX	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
$\overline{WR}$ Pulse Width	TWLWH	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	240	-	ns
Data Setup Time Before $\overline{WR}$	TDVWH	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	225	-	ns
Data Hold Time After $\overline{WR}$	TWHDX	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	35	-	ns
Command Recovery Time	TWHWL	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	320	-	ns
CLOCK AND GATE							
Clock Period	TCLCL	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	200	-	ns
High Pulse Width	TCHCL	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	100	-	ns
Low Pulse Width	TCLCH	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	100	-	ns
Gate Width High	TGHGL	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	80	-	ns
Gate Width Low	TGLGH	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	80	-	ns
Gate Setup Time to CLK	TGVCH	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	80	-	ns
Gate Hold Time After CLK	TCHGX	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	80	-	ns
Output Delay from CLK	TCLOV	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	240	ns
Output Delay from Gate	TGLOV	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	200	ns
Data Delay from Address Read	TAVAV	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	275	ns
Output Delay from $\overline{WR}$ High	TWHOV	VDD = 4.5V + 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	260	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz, All measurements referenced to device ground.	T_A = +25°C	-	15	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz, All measurements referenced to device ground.	T_A = +25°C	-	15	pF
I/O Capacitance	COUT	VDD = Open, f = 1MHz, All measurements referenced to device ground.	T_A = +25°C	-	20	pF
TIMING REQUIREMENTS						
$\overline{RD}$/ to Data Float	TRHDZ	VDD = 4.5V and 5.5V	-55°C < T_A < +125°C	8	145	ns
TIMING RESPONSES						
Clock Rise Time	TCH1CH2	VDD = 4.5V and 5.5V, 1.0V to 3.5V	-55°C < T_A < +125°C	-	25	ns
Clock Fall Time	TCL1CL2	VDD = 4.5V and 5.5V, 3.5V to 1.0V	-55°C < T_A < +125°C	-	25	ns

NOTE: The parameters listed are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: See +25°C limits in Table 1 and Table 2 for Post RAD limits (Sub Groups 1, 7 and 9).

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

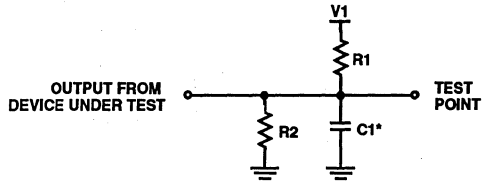
PARAMETER	SYMBOL	DELTA LIMITS
Standby Power Supply Current	IDDSB	±2µA
Output Leakage Current	IOZL, IOZH	±2µA
Input Leakage Current	IIH, IIL	±200nA
Output Low Current	IOL	±500µA or 10% of BBI Reading*
TTL Output High Current	IOH TTL	±500µA or 10% of BBI Reading*
CMOS Output High Current	IOH CMOS	±20µA or 10% of BBI Reading*

* Which ever is greater.

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9
Interim Test		100%/5004	1, 7, 9	N/A
PDA		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	N/A
	Others	Samples/5005	1, 7	N/A
Group C		Samples/5005	N/A	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group D, Others		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7, 9	1, 7, 9

AC Test Circuits

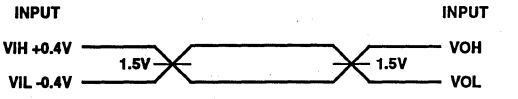


* Includes stray and jig capacitance

TEST CONDITION DEFINITION TABLE

TEST CONDITION	V1	R1	R2	C1
1	1.7V	510	OPEN	150pF

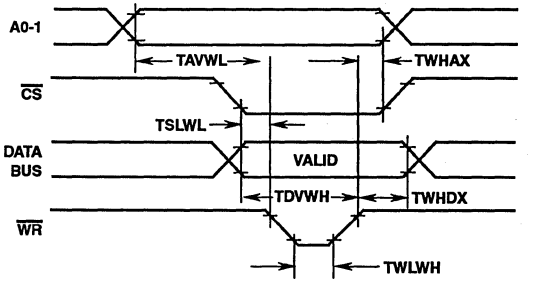
AC Testing Input, Output Waveform



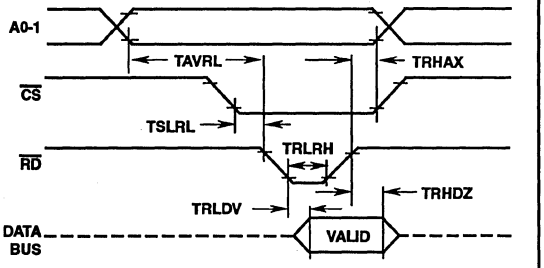
NOTE: AC Testing: All input signals must switch between VIL -0.4V and VIH +0.4V. Input rise and fall times are driven at 1ns/V.

Waveforms

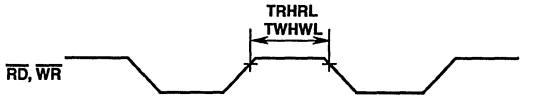
WRITE



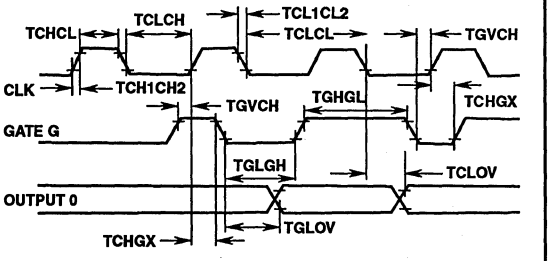
READ



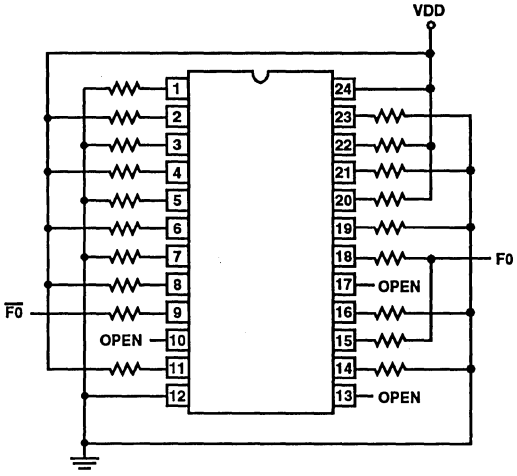
RECOVERY



CLOCK AND GATE



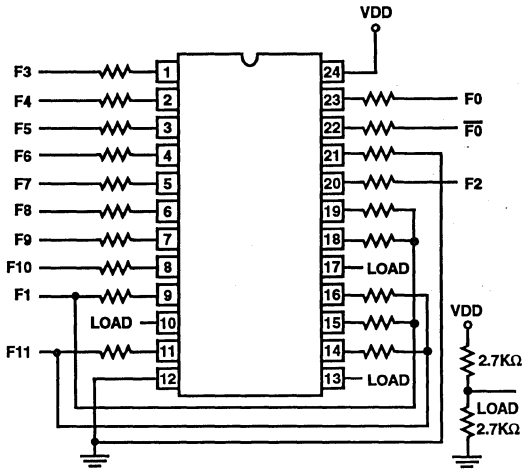
Burn-In Circuits



STATIC CONFIGURATION FOR BOTH FLATPACKS & DIPS

NOTES:

VDD = 6.5V ± 5%
T_A = +125°C Minimum
Resistors = 10kΩ
IDD < 100μA
AC: $\overline{F0}$ is compliment of F0
F0 is a 50% duty cycle pulse burst
F0 is left high after pulse burst

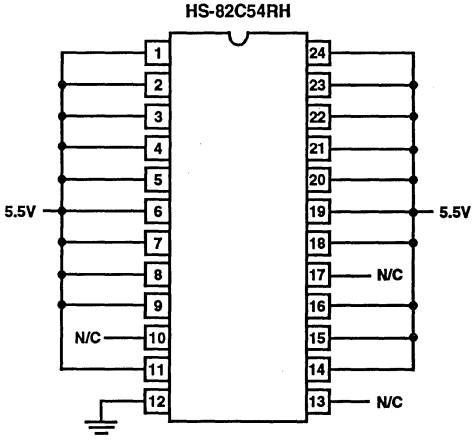


DYNAMIC CONFIGURATION FOR BOTH FLATPACKS & DIPS

NOTES:

VDD = 6.5V ± 5%(Burn-In)
VDD = 6.0V ± 5%(Life Test)
T_A = +125°C Minimum
IDD < 20mA
Resistors = 10KΩ, except for loads = 2.7kΩ
-0.3V ≤ VIL ≤ 0.8V
VDD -1.0V ≤ VIH ≤ 0.8V
AC: $\overline{F0}$ is compliment of F0
F0 = 50kHz ±10%m 50% Duty Cycle
F1 = F0/2, F2 = F1/2 . . . F10 = F9/2

Irradiation Circuits



NOTES:

VDD = 5.5V ± 10%, T_A = +25°C
Group E Testing is performed in Sidebrazed DIP
Group E Sample Size is 2 die/wafer

Harris - Space Level '-Q' Flow

SEM - Traceable to Diffusion Method 2018
Wafer Lot Acceptance Method 5007
Internal Visual Inspection
Gamma Radiation Assurance Tests Method 1019
100% Nondestructive Bond Pull Method 2023
Customer Pre-Cap Visual Inspection (Note 1)
Temperature Cycling Method 1010 Condition C
Constant Acceleration Method 2001 Y1 30KG
Particle Impact Noise Detection Method 2020, Condition A 20G
Serialization
X-Ray Inspection Method 2012 (Two Views)
Initial Electrical Tests (T0)
Static Burn-In 72 Hour, +125°C, Method 1015 Condition A
+25°C Interim Electrical Tests Subgroups 1, 7, 9 (T1)
Burn-In Delta Calculation (T0 - T1)
PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ
Dynamic Burn-In 240 Hours, +125°C Method 1015 Condition D
+25°C Electrical Tests (T2) Subgroups 1, 7, 9 (T2)
Burn-In Delta Calculation (T0 - T2)
PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ
Electrical Test +125°C, -55°C
Group A Inspection Method 5005. 5% PDA (Note 3)
Fine and Gross Leak Tests Method 1014
Brand
Customer Source Inspection (Note 1)
Group B Inspection Method 5005 (Notes 1, 2)
Group D Inspection Method 5005 (Notes 1, 2)
External Visual Inspection Method 2009
Data Package Generation (Note 4)

NOTES:
1. These steps are optional, and must be negotiated as part of the order.
2. Group B and D data package contains Attributes Data plus Variables Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable.
4. '-Q' Data Pack Contains:
   - Cover Sheet:
     a) Purchase Order Number
     b) Customer Part Number
     c) Lot Date Code
     d) Harris Part Number
     e) Lot Number
     f) Quantity
   - Certificate of Conformance (as found on shipper).
   - Shippable serial number list.
   - Test Attributes (including Group A) for all test temperatures.
   - Test Variables data for all read/record and delta operations.
     +25°C Initial Test (T0)
     +25°C Interim Test (T1)
     +25°C Final Test (T2)
     All +25°C Delta's (T1-T0, T2-T0)
     +125°C Final Test
     -35°C Final Test
   - Wafer Lot Acceptance Report (includes SEM).
   - X-Ray report and Film.
   - Radiation Testing Certificate of Conformance.
   - Assembly Attributes (Post seal).

Harris - '-8' Flow

Internal Visual Inspection
Gamma Radiation Assurance Tests Method 1019
Customer Pre-Cap Visual Inspection (Note 1)
Temperature Cycling Method 1010 Condition C
Fine and Gross Leak Tests Method 1014
Constant Acceleration Method 2001 Y1 30KG
Initial Electrical Tests
Dynamic Burn-In 160 Hours, +125°C Method 1015 Condition D
+25°C Electrical Tests Subgroups 1, 7, 9
PDA Calculation: 5% Subgroups 1, 7
Electrical Test +125°C, -55°C
Group A Inspection Method 5005. 5% PDA (Note 3)
Brand
Customer Source Inspection (Note 1)
Group C Inspection Method 5005 (Notes 1, 2)
Group D Inspection Method 5005 (Notes 1, 2)
External Visual Inspection Method 2009
Data Package Generation (Note 4)

NOTES:
1. These steps are optional, and must be negotiated as part of the order.
2. Group B and D data package contains Attributes Data plus Variables Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable.
4. '-8' Data Pack Contains:
   - Assembly Attributes (Post Seal).
   - Test Attributes (Including Group A).
   - Radiation Testing Certificate of Conformance.
   - Certificate of Conformance (as found on shipper).

Metallization Topology

DIE DIMENSIONS:
4700 x 5510µm x 485µm ± 25.4µm

METALLIZATION:
Type: Al/Si
Thickness: 11kÅ ± 2kÅ

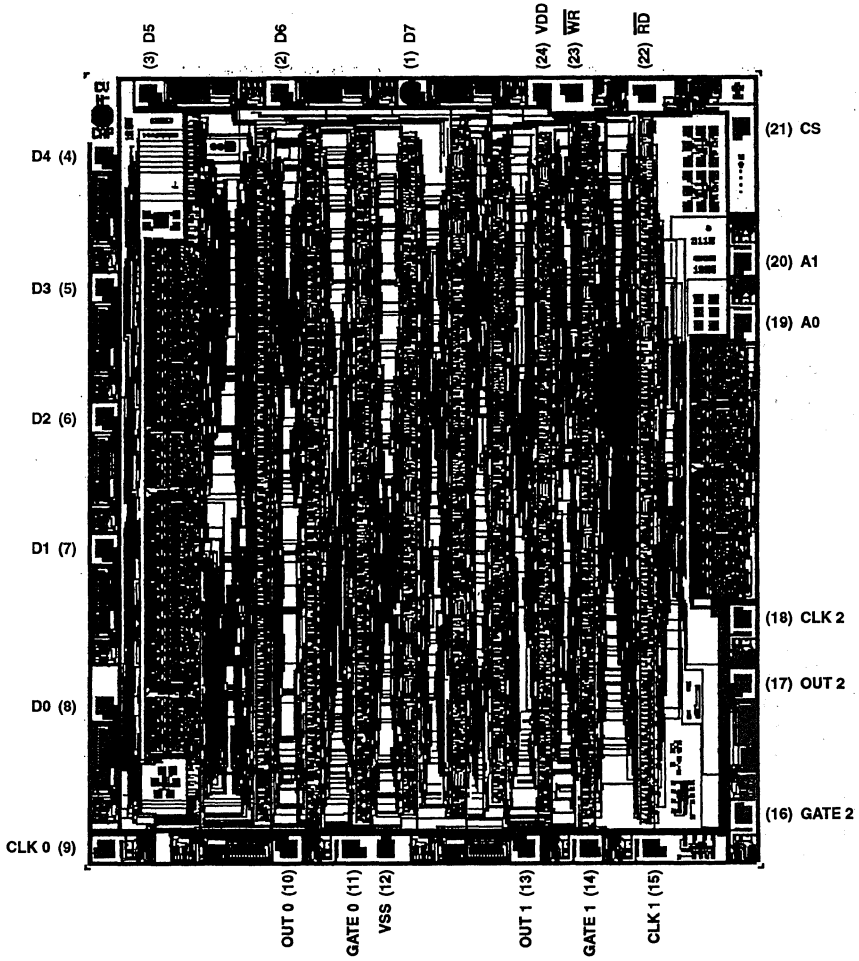
GLASSIVATION:
Type: SiO2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy

WORST CASE CURRENT DENSITY:
7.9×10^4 A/cm^2

Metallization Mask Layout

HS-82C54RH



Functional Description

General

The HS-82C54RH is a programmable interval timer/counter designed for use with microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The HS-82C54RH solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the HS-82C54RH to match his requirements and programs one of the counters for the desired delay. After the desired delay, the HS-82C54RH will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other timer functions common to micro-computers which can be implemented with the HS-82C54RH are:

- Real time clock
- Event counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Data Bus Buffer

This three-state, bi-directional, 8-bit buffer is used to interface the HS-82C54RH to the system bus (see Figure 1).

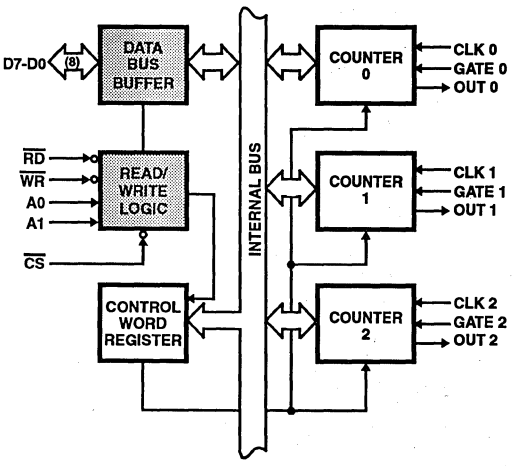


FIGURE 1. DATA BUS BUFFER AND READ/WRITE LOGIC FUNCTION

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the HS-82C54RH. A1 and A0 select one of the three counters or the Control Word Register to be read from/written into. A "low" on the $\overline{RD}$ input tells the HS-82C54RH that the CPU is reading one of the counters. A "low" on the $\overline{WR}$ input tells the HS-82C54RH that the CPU is writing either a Control Word or an initial count. Both $\overline{RD}$ and $\overline{WR}$ are qualified by $\overline{CS}$; $\overline{RD}$ and $\overline{WR}$ are ignored unless the HS-82C54RH has been selected by holding $\overline{CS}$ low.

Control Word Register

The Control Word Register (Figure 2) is selected by the Read/Write Logic when A1, A0 = 11. If the CPU then does a write operation to the HS-82C54RH, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the Counter operation.

The Control Word Register can only be written to; status information is available with the Read-Back Command.

Counter 0, Counter 1, Counter 2

These three functional clocks are identical in operation, so only a single Counter will be described. The internal block diagram of a single counter is shown in Figure 3. The counters are fully independent. Each Counter may operate in a different Mode.

The Control Word Register is shown in the figure; it is not part of the Counter itself, but its contents determine how the Counter operates.

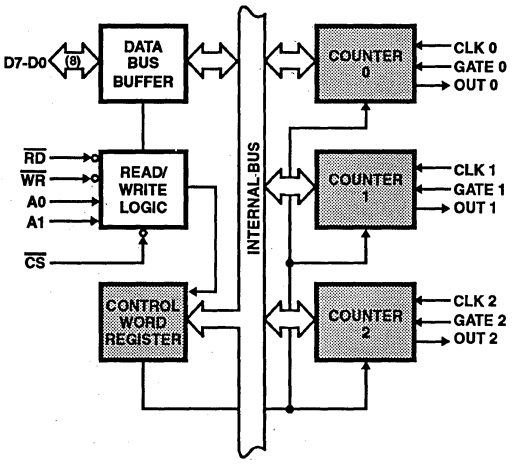


FIGURE 2. CONTROL WORD REGISTER AND COUNTER FUNCTIONS

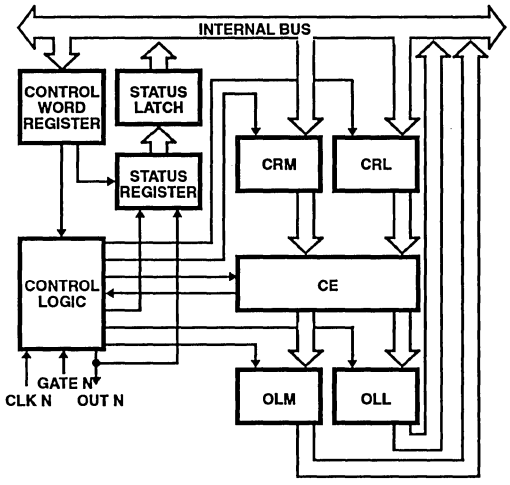


FIGURE 3. COUNTER INTERNAL BLOCK DIAGRAM

The Status Register, shown in the figure, when latched, contains the current contents of the Control Word Register and status of the output and null count flag. (See detailed explanation of the Read-Back Command.)

The actual counter is labeled CE for "Counting Element". It is a 16-bit presettable synchronous down counter.

OLM and OLL are two 8-bit latches. OL stands for "Output Latch", subscripts M and L for "Most significant byte" and "Least significant byte", respectively. Both are normally referred to as one unit and called just OL. These latches normally "follow" the CE, but if a suitable Counter Latch Command is sent to the HS-82C54RH, the OL latches the present count until read by the CPU and then returns to "following" the CE. One latch at a time is enabled by the counter's Control Logic to drive the internal bus. This is how the 16-bit Counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Similarly, there are two 8-bit registers called CRM and CRL (for "Count Register"). Both are normally referred to as one unit and called just CR. When a new count is written to the Counter, the count is stored in the CR and later transferred to the CE. The Control Logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously. CRM and CRL are cleared when the Counter is programmed for one byte counts (either most significant byte only or least significant byte only) the other byte will be zero. Note that the CE cannot be written into; whenever a count is written, it is written into the CR.

The Control Logic is also shown in the diagram. CLKn, GATEn, and OUTn are all connected to the outside world through the Control Logic.

HS-82C54RH System Interface

The HS-82C54RH is treated by the system software as an array of peripheral I/O ports; three are Counters and the fourth is a Control Word Register for MODE programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The $\overline{CS}$ can be derived directly from the address bus using a linear select method or it can be connected to the output of a decoder, such as a Harris HD-6440 for larger systems.

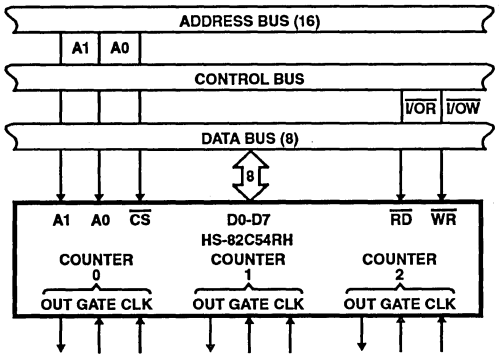


FIGURE 4. HS-82C54RH SYSTEM INTERFACE

Operational Description

General

After power-up, the state of the HS-82C54RH is undefined. The Mode, count value, and output of all Counters are undefined.

How each Counter operates is determined when it is programmed. Each Counter must be programmed before it can be used. Unused Counters need not be programmed.

Programming The HS-82C54RH

Counters are programmed by writing a Control Word and then an initial count.

All Control Words are written into the Control Word Register, which is selected when A1, A0 = 11. The Control Word specifies which Counter is being programmed.

By contrast, initial counts are written into the Counters, not the Control Word Register. The A1, A0 inputs are used to select the Counter to be written into. The format of the initial count is determined by the Control Word used.

Write Operations

The programming procedure for the HS-82C54RH is very flexible. Only two conventions need to be remembered:

1. For each Counter, the Control Word must be written before the initial count is written.
2. The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the Control Word Register and the three Counter shave separate addresses (selected by the A1, A0 inputs), and each Control Word specifies the Counter it applies to (SC0, SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions above is acceptable.

Control Word Format

A1, A0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC2	RW1	RW0	M2	M1	M0	BCD

SC - Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See Read Operations)

RW - Read/Write

RW1	RW0	
0	0	Counter Latch Command (See Read Operations)
0	1	Read/Write least significant byte only.
1	0	Read/Write most significant byte only.
1	1	Read/Write least significant byte first, then most significant byte.

M - Mode:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD - Binary Coded Decimal:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE: Don't Care bits (X) should be 0 to insure compatibility with future products.

FIGURE 5. CONTROL WORD FORMAT

	A1	A0
Control Word - Counter 0	1	1
LSB of count - Counter 0	0	0
MSB of count - Counter 0	0	0
Control Word - Counter 1	1	1
LSB of count - Counter 1	0	1
MSB of count - Counter 1	0	1
Control Word - Counter 2	1	1
LSB of count - Counter 2	1	0
MSB of count - Counter 2	1	0

	A1	A0
Control Word - Counter 2	1	1
Control Word - Counter 1	1	1
Control Word - Counter 0	1	1
LSB of count - Counter 2	1	0
MSB of count - Counter 2	1	0
LSB of count - Counter 1	0	1
MSB of count - Counter 1	0	1
LSB of count - Counter 0	0	0
MSB of count - Counter 0	0	0

	A1	A0
Control Word - Counter 0	1	1
Control Word - Counter 1	1	1
Control Word - Counter 2	1	1
LSB of count - Counter 2	1	0
LSB of count - Counter 1	0	1
LSB of count - Counter 0	0	0
MSB of count - Counter 0	0	0
MSB of count - Counter 1	0	1
MSB of count - Counter 2	1	0

	A1	A0
Control Word - Counter 1	1	1
Control Word - Counter 0	1	1
LSB of count - Counter 1	0	1
Control Word - Counter 2	1	1
LSB of count - Counter 0	0	0
MSB of count - Counter 1	0	1
LSB of count - Counter 2	1	0
MSB of count - Counter 0	0	0
MSB of count - Counter 2	1	0

NOTE: In all four examples, all counters are programmed to Read/Write two-byte counts. These are only four of many possible programming sequences.

FIGURE 6. A FEW POSSIBLE PROGRAMMING SEQUENCES

A new initial count may be written to a Counter at any time without affecting the Counter's programmed Mode in anyway. Counting will be affected as described in the Mode definitions. The new count must follow the programmed count format.

If a Counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same Counter. Otherwise, the Counter will be loaded with an incorrect count.

Read Operations

It is often desirable to read the value of a Counter without disturbing the count in progress. This is easily done in the HS-82C54RH.

There are three possible methods for reading the Counters. The first is through the Read-Back Command, which is explained later. The second is a simple read operation of the Counter, which is selected with the A1, A0 inputs. The only requirement is that the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in process of changing when it is read, giving an undefined result.

Counter Latch Command

The other method for reading the Counters involves a special software command called the "Counter Latch Command". Like a Control Word, this command is written to the Control Word Register, which is selected when A1, A0 = 11. Also, like a Control Word, the SC0, SC1 bits select one of the three Counters, but two other bits, D5 and D4, distinguish this command from a Control Word.

A1, A0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

SC1, SC0 - specify counter to be latched

SC1	SC1	Counter
0	0	0
0	0	1
1	1	2
1	1	Read-Back Command

D5, D4 = 00 designates Counter Latch Command
X = Don't Care

NOTE: Don't Care bits (X) should be 0 to Insure compatibility with future products.

FIGURE 7. COUNTER LATCH COMMAND FORMAT

The selected Counter's Output Latch (OL) latches the count when the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed). The count is then unlatched automatically and the OL returns to "following" the Counting Element (CE). This allows reading the contents of the Counters "on the fly" without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one Counter. Each latched Counter's OL holds its count until read. Counter Latch Commands do not affect the programmed Mode of the Counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.

With either method, the count must be read according to the programmed format; specifically, if the Counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or programming operations of other Counters may be inserted between them.

Another feature of the HS-82C54RH is that reads and writes of the same Counter may be interleaved; for example, if the Counter is programmed for two byte counts, the following sequence is valid.

1. Read least significant byte.
2. Write new least significant byte.
3. Read most significant byte.
4. Write new most significant byte.

If a Counter is programmed to read or write two-byte counts, the following precaution applies: A program MUST NOT transfer control between reading the first and second byte to another routine which also reads from that same Counter. Otherwise, an incorrect count will be read.

Read-Back Command

The Read-Back Command allows the user to check the count value, programmed Mode, and current state of the OUT pin and Null Count flag of the selected Counter(s).

The command is written into the Control Word Register and has the format shown in Figure 8. The command applies to the Counters selected by setting their corresponding bits D3, D2, D1 = 1.

A0, A1 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
1	1	$\overline{COUNT}$	$\overline{STATUS}$	CNT 2	CNT 1	CNT 0	0

D5: 0 = Latch count of selected Counters(s)
D4: 0 = Latch status of selected Counters(s)
D3: 1 = Select Counter 2
D2: 1 = Select Counter 1
D1: 1 = Select Counter 0
D0: Reserved for future expansion; Must be 0

FIGURE 8. READ-BACK COMMAND FORMAT

The Read-Back Command may be used to latch multiple Counter Output Latches (OL) by setting the COUNT bit D5 = 0 and selecting the desired Counter(s). This single command is functionally equivalent to several Counter Latch

Commands, one for each Counter latched. Each Counter's latched count is held until it is read (or the Counter is reprogrammed). That Counter is automatically unlatched when read, but other Counters remain latched until they are read. If multiple count Read-Back Commands are issued to the same Counter without reading the count, all but the first are ignored; i.e., the count which will be read is the count at the time the first Read-Back Command was issued.

The Read-Back Command may also be used to latch status information of selected Counter(s) by setting STATUS bit D4 = 0. Status must be latched to be read; status of a Counter is accessed by a read from that Counter.

The Counter status format is shown in Figure 9. Bits D5 through D0 contain the Counter's programmed Mode exactly as written in the last Mode Control Word. OUTPUT bit D7 contains the current state of the OUT pin. This allows the user to monitor the Counter's output via software, possibly eliminating some hardware from a system.

D7	D6	D5	D4	D3	D2	D1	D0
OUT PUT	NULL COUNT	RW1	RW0	M2	M1	M0	BCD

D7 1 = Out Pin is 1
0 = Out pin is 0
D6 1 = Null count
0 = Count available for reading
D5-D0 = Counter programmed mode (See Figure 5)

FIGURE 9. STATUS BYTE

NULL COUNT bit D6 indicates when the last count written to the Counter Register (CR) has been loaded into the Counting Element (CE). The exact time this happens depends on the Mode of the Counter and is described in the Mode Definitions, but until the count is loaded into the Counting Element (CE), it can't be read from the Counter. If the count is latched or read before this time, the count value will not reflect the new count just written. The operation of Null Count is shown in Figure 10.

THIS ACTION:	CAUSES:
A. Write to the Control Word Register: (Note 1)	Null Count = 1
B. Write to the Count Register (CR): (Note 2)	Null Count = 1
C. New count is loaded into CE (CR → CE):	Null Count = 0

NOTES:

1. Only the Counter specified by the Control Word will have its Null Count set to 1. Null Count bits of other Counters are unaffected.
2. If the Counter is programmed for two-byte counts (least significant byte then most significant byte) Null Count goes to 1 when the second byte is written.

FIGURE 10. NULL COUNT OPERATION

If multiple status latch operations of the Counter(s) are performed without reading the status, all but the first are ignored; i.e., the status that will be read is the status of the Counter at the time the first status Read-Back Command was issued.

Both count and status of the selected Counter(s) may be latched simultaneously by setting both COUNT and STATUS bits D5, D4 = 0. This is functionally the same as issuing two separate Read-Back Commands at once, and the above discussions apply here also. Specifically, if multiple count and/or status Read-Back Commands are issued to the same Counter(s) without any intervening reads, all but the first are ignored. This is illustrated in Figure 11.

If both count and status of a Counter are latched, the first read operation of that Counter will return latched status, regardless of which was latched first. The next one or two reads (depending on whether the Counter is programmed for one or two byte counts) return latched count. Subsequent reads return unlatched count.

COMMAND								DESCRIPTION	RESULT
D7	D6	D5	D4	D3	D2	D1	D0		
1	1	0	0	0	0	1	0	Read back count and status of Counter 0	Count and status latched for Counter 0
1	1	1	0	0	1	0	0	Read-back status of Counter 1	Status latched for Counter 1
1	1	1	0	1	1	0	0	Read-back status of Counters 2, 1	Status latched for Counter 2, but not Counter 1
1	1	0	1	1	0	0	0	Read-back count of Counter 2	Count latched for Counter 2
1	1	0	0	0	1	0	0	Read-back count and status of Counter 1	Count latched for Counter 1, but not status
1	1	1	0	0	1	0	0	Read-back status of Counter 1	Command ignored, status already latched for Counter 1

FIGURE 11. READ-BACK COMMAND EXAMPLE

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (Three-State)
1	X	X	X	X	No-Operation (Three-State)
0	1	1	X	X	No-Operation (Three-State)

FIGURE 12. READ/WRITE OPERATIONS SUMMARY

Mode Definitions

The following are defined for use in describing the operation of the HS-82C54RH.

CLK PULSE:

A rising edge, then a falling edge, in that order, of a Counter's CLK input.

TRIGGER:

A rising edge of a Counter's Gate input.

COUNTER LOADING:

The transfer of a count from the CR to the CE (See "Functional Description")

Mode 0: Interrupt on Terminal Count

Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written to the Counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

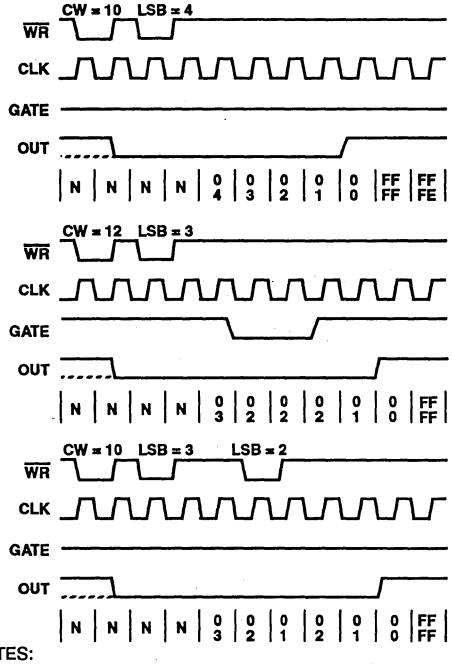
After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N + 1 CLK pulses after the initial count is written.

If a new count is written to the Counter it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1. Writing the first byte disables counting. OUT is set low immediately (no clock pulse required).
2. Writing the second byte allows the new count to be loaded on next CLK pulse.

This allows the counting sequence to be synchronized by software. Again OUT does not go high until N + 1 CLK pulses after the new count of N is written.

If an initial count is written while GATE = 0, it will still beloaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the Counter as this has already been done.



NOTES:

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The Counter is always selected ($\overline{CS}$ always low).
3. CW stands for "Control Word"; CW = 10 means a Control Word of 10, Hex is written to the Counter.
4. LSB stands for "Least significant byte" of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the Counter is programmed to read/write LSB only, the most significant byte cannot be read.
6. N stands for an undefined count.
7. Vertical lines show transitions between count values.

FIGURE 13. MODE 0

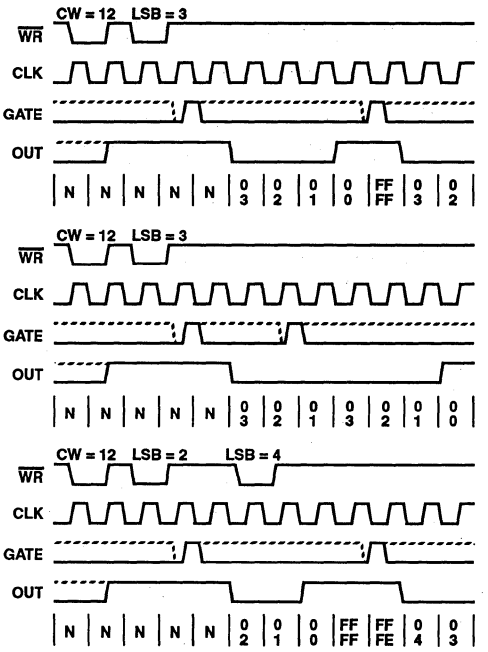
Mode 1: Hardware Retriggerable One-Shot

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse N CLK cycles in duration. The one-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the Counter. GATE has no effect on OUT.

If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the Counter is retriggered. In that case, the Counter is loaded with the new count and the one-shot pulse continues until

the new count expires.



NOTES:

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The Counter is always selected ($\overline{CS}$ always low).
3. CW stands for "Control Word"; CW = 10 means a Control Word of 10, Hex is written to the Counter.
4. LSB stands for "Least significant byte" of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the Counter is programmed to read/write LSB only, the most significant byte cannot be read.
6. N stands for an undefined count.
7. Vertical lines show transitions between count values.

FIGURE 14. MODE 1

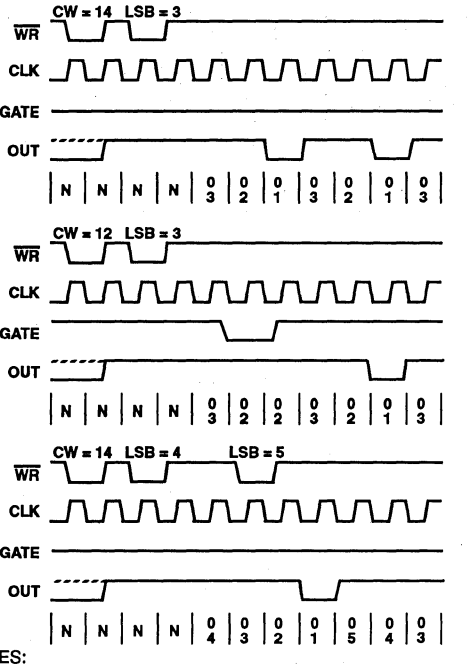
Mode 2: Rate Generator

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK pulses after the initial count is written. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle.



NOTES:

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The Counter is always selected ($\overline{CS}$ always low).
3. CW stands for "Control Word"; CW = 10 means a Control Word of 10, Hex is written to the Counter.
4. LSB stands for "Least significant byte" of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the Counter is programmed to read/write LSB only, the most significant byte cannot be read.
6. N stands for an undefined count.
7. Vertical lines show transitions between count values.

FIGURE 15. MODE 2

Mode 3: Square Wave Mode

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If

GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

EVEN COUNTS: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires, OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

ODD COUNTS: OUT is initially high. The initial count is loaded on one CLK pulse, decremented by one on the next CLK pulse, and then decremented by two on succeeding CLK pulses. When the count expires, OUT goes low and the Counter is reloaded with the initial count. The count is decremented by three on the next CLK pulse, and then by two on succeeding CLK pulses.When the count expires, OUT goes high again and the Counter is reloaded with the initial count. The above process is repeated indefinitely. So for odd counts, OUT will be high for (N + 1)/2 counts and low for (N-1)/2 counts.

Mode 4: Software Triggered Mode

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse then go high again.The counting sequence is "Triggered" by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1. Writing the first byte has no effect on counting.
2. Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be "retriggered" by software. OUT strobes low N + 1 CLK pulses after the new count of N is written.

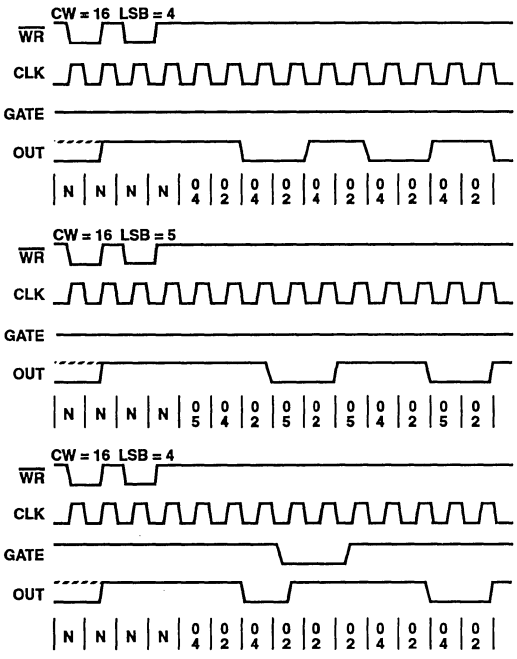
Mode 5: Hardware Triggered Strobe (Retriggerable)

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

After writing the Control Word and initial count, the Counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after trigger.

A trigger results in the Counter being loaded with the initial count on the next CLK pulse. This allows the counting sequence to be regretted. OUT strobes low N + 1 CLK pulses after any new trigger. GATE has no effect on the state of OUT.

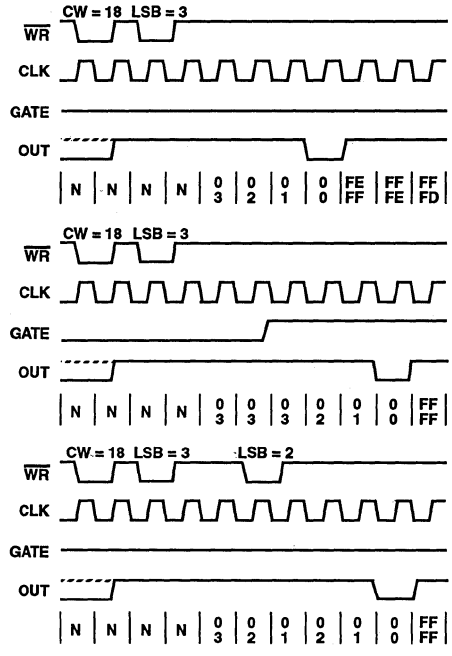
If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.



NOTES:

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The Counter is always selected ($\overline{CS}$ always low).
3. CW stands for "Control Word"; CW = 10 means a Control Word of 10, Hex is written to the Counter.
4. LSB stands for "Least significant byte" of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the Counter is programmed to read/write LSB only, the most significant byte cannot be read.
6. N stands for an undefined count.
7. Vertical lines show transitions between count values.

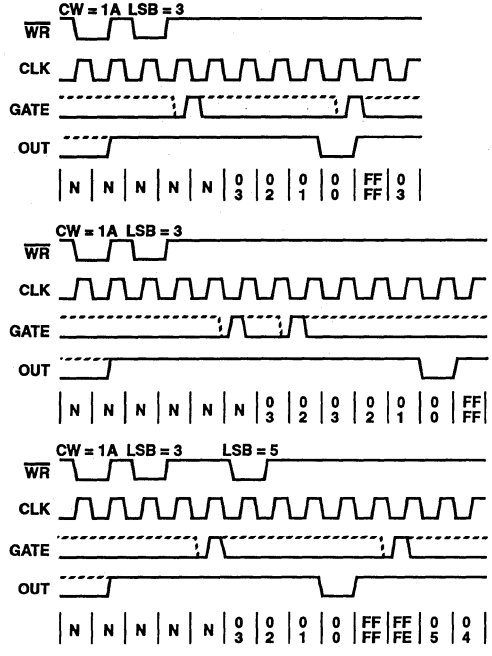
FIGURE 16. MODE 3



NOTES:

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The Counter is always selected ($\overline{CS}$ always low).
3. CW stands for "Control Word"; CW = 10 means a Control Word of 10, Hex is written to the Counter.
4. LSB stands for "Least significant byte" of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the Counter is programmed to read/write LSB only, the most significant byte cannot be read.
6. N stands for an undefined count.
7. Vertical lines show transitions between count values.

FIGURE 17. MODE 4



NOTES:

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The Counter is always selected ($\overline{CS}$ always low).
3. CW stands for "Control Word"; CW = 10 means a Control Word of 10, Hex is written to the Counter.
4. LSB stands for "Least significant byte" of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the Counter is programmed to read/write LSB only, the most significant byte cannot be read.
6. N stands for an undefined count.
7. Vertical lines show transitions between count values.

FIGURE 18. MODE 5

Operation Common to All Modes

Programming

When a Control Word is written to a Counter, all Control Logic is immediately reset and OUT goes to a known initial state; no CLK pulses are required for this.

Gate

The GATE input is always sampled on the rising edge of CLK. In Modes 0, 2, 3 and 4 the GATE input is level sensitive, and logic level is sampled on the rising edge of CLK. In modes 1, 2, 3 and 5 the GATE input is rising-edge sensitive. In these Modes, a rising edge of Gate (trigger) sets an edge-sensitive flip-flop in the Counter. This flip-flop is then sampled on the next rising edge of CLK. The flip-flop is reset immediately after it is sampled. In this way, a trigger will be detected no matter when it occurs - a high logic level does not have to be maintained until the next rising edge of CLK. Note that in Modes 2 and 3, the GATE input is both edge-and level-sensitive.

Counter

New counts are loaded and Counters are decremented on the falling edge of CLK.

The largest possible initial count is 0; this is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

The Counter does not stop when it reaches zero. In Modes 0, 1, 4 and 5 the Counter "wraps around" to the highest count, either FFFF hex for binary counting or 9999 for BCD counting, and continues counting. Modes 2 and 3 are periodic; the Counter reloads itself with the initial count and continues counting from there.

GATE PIN OPERATIONS SUMMARY

SIGNAL STATUS MODES	LOW OR GOING LOW	RISING	HIGH
0	Disables counting	-	Enables counting
1	-	1) Initiates counting 2) Resets output after next clock	-
2	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	1) Disables counting	-	Enables counting
5	-	Initiates counting	-

MINIMUM AND MAXIMUM INITIAL COUNTS

MODE	MIN COUNT	MAX COUNT
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0
5	1	0

NOTE: 0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

HARRIS SEMICONDUCTOR

HS-82C55ARH

Radiation Hardened CMOS Programmable Peripheral Interface

December 1992

Features

- Radiation Hardened
  - Total Dose >10^5 RAD(Si)
  - Transient Upset <10^8 RAD(Si)/s
  - Functional After Total Dose 1 x 10^6RAD(Si)
  - Latch Up Free EPI-CMOS
- Low Power Consumption
  - IDDSB = 20μA
- Pin Compatible with NMOS 8255A and the Harris 82C55A
- High Speed, No "Wait State" Operation with 5MHz HS-80C86RH
- 24 Programmable I/O Pins
- Bus-Hold Circuitry on All I/O Ports Elimnates Pull-Up Resistors
- Direct Bit Set/Reset Capability
- Enhanced Control Word Read Capability
- Hardened Field, Self-Aligned, Junction Isolated CMOS Process
- Single 5V Supply
- 2.0mA Drive Capability on All I/O Port Outputs
- Military Temperature range -55°C to +125°C

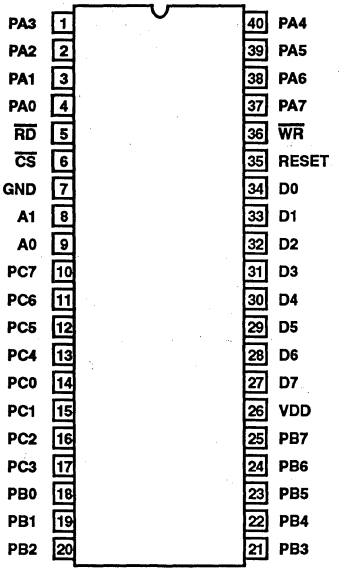
Description

The Harris HS-82C55ARH is a high performance, radiation hardened CMOS version of the industry standard 8255A and is manufactured using a hardened field, self-aligned silicon-gate CMOS process. It is a general purpose programmable I/O device which may be used with many different microprocessors. There are 24 I/O pins which are organized into two 8-bit and two 4-bit ports. Each port may be programmed to function as either an input or an output. Additionally, one of the 8-bit ports may be programmed for bi-directional operation,and the two 4-bit ports can be programmed to provide handshaking capabilities. The high performance, radiation hardness, and industry standard configuration of the HS-82C55ARH make it compatible with the HS-80C86RH radiation hardened microprocessor.

Static CMOS circuit design insures low operating power. Bus hold circuitry eliminates the need for pull-up resistors. The Harris hardened field CMOS process results in performance equal to or greater than existing radiation resistant products at a fraction of the power.

Pinout

40 PIN DIP
CASE OUTLINE D-5, CONFIGURATION 3
TOP VIEW



PIN	DESCRIPTION
D7 - D0	Data Bus (Bi-Directional
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A0 - A1	Port Address
PA7 - PA0	Port A (Bit)
PB& - PB0	Port B (Bit)
PC7 - PC0	Port C (Bit)
VDD	+5 volts
GND	0 volts

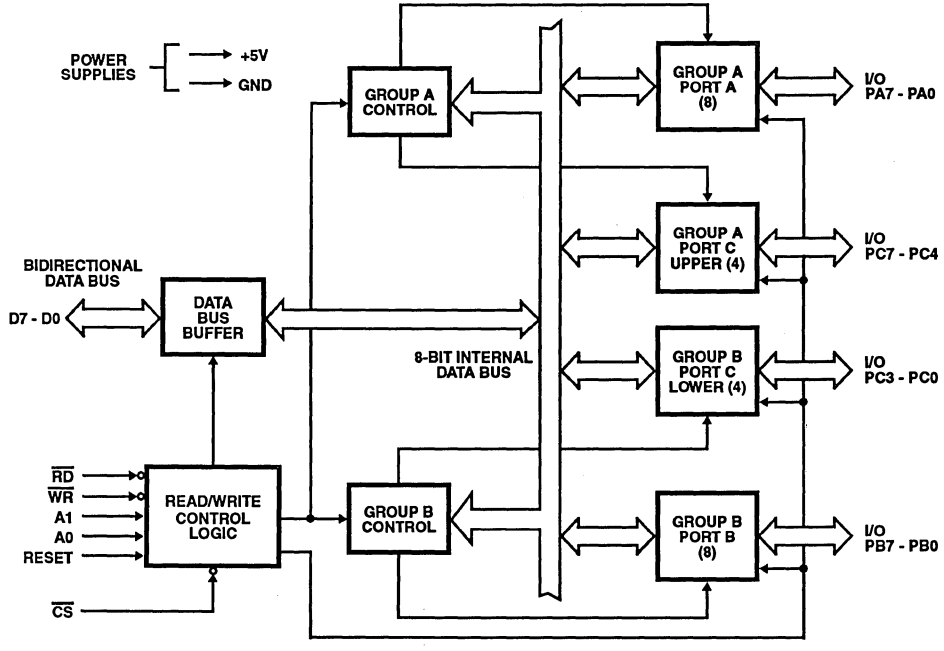
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3191**

Pin Description

SYMBOL	PIN NUMBERS	TYPE	DESCRIPTION
PA0-7	1-4, 37-40	I/O	**Port A:** General purpose I/O Port. Data direction and mode is determined by the contents of the Control Word.
PB0-7	18-25	I/O	**Port B:** General purpose I/O port. See Port A.
PC0-3	14-17	I/O	**Port C (Lower):** Combination I/O port and control port associated with Port B. See Port A.
PC4-7	10-13	I/O	**Port C (Upper):** Combination I/O Port and control port associated with Port A. See Port A.
D0-7	27-34	I/O	**Bidirectional Data Bus:** Three-State data bus enabled as an input when $\overline{CS}$ and $\overline{WR}$ are low and as an output when $\overline{CS}$ and $\overline{RD}$ are low.
VDD	26	I	**VDD:** The +5V power supply pin. A 0.1µF capacitor between pins 26 and 7 is recommended for decoupling.
GND	7	I	**Ground.**
CS	6	I	**Chip Select:** A "low" on this input pin enables the communication between the HS-82C55ARH and the CPU.
RD	5	I	**Read:** A "low" on this input pin enables the HS-82C55ARH to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the HS-82C55ARH.
WR	36	I	**Write:** A "low" on this input pin enables the CPU to write data or control words into the HS-82C55ARH.
A0 and A1	8, 9	I	**Port Select 0 and Port Select 1:** These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the Least Significant Bits of the address bus (A0 and A1).
Reset	35	I	**Reset:** A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode. "Bus hold" devices internal to the HS-82C55ARH will hold the I/O port inputs to a logic "1" state with a maximum hold current of 400µA.

Functional Diagram



Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage ..... VSS-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Brazed Seal DIP Package	26.7°C/W	10.7°C/W
Brazed Seal Flatpacke Package	61.1°C/W	13.6°C/W

Maximum Package Power Dissipation at +125°C
Brazed Seal DIP Package 1.87W
Brazed Seal Flatpack Package 0.82W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... VDD -1.5V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
TTL Output High Voltage	VOH1	VDD = 4.5V, IO = -2.5mA, VIN = 0V, 4.5V	1, 2, 3	-55°C, +25°C, +125°C	3.0	-	V
CMOS Output High Voltage	VOH2	VDD = 4.5V, IO = -100µA, VIN = 0V, 4.5V	1, 2, 3	-55°C, +25°C, +125°C	VDD-0.4	-	V
Output Low Voltage	VOL	VDD = 4.5V, IO = 2.5mA, VIN = 0V, 4.5V	1, 2, 3	-55°C, +25°C, +125°C	-	0.4	V
Input Leakage Current	IIL or IIH	VDD = 5.5V, VIN = 0V, 5.5V	1, 2, 3	-55°C, +25°C, +125°C	-1.0	1.0	µA
Output Leakage Current	IOZL or IOZH	VDD = 5.5V, VIN = 0V, 5.5V	1, 2, 3	-55°C, +25°C, +125°C	-10	10	µA
Input Current Bus Hold High	IBHH	VDD = 4.5V or 5.5V, VIN = 3.0V (See Note 1) Ports A, B, C	1, 2, 3	-55°C, +25°C, +125°C	-800	-60	µA
Input Current Bus Hold Low	IBHL	VDD = 4.5V or 5.5V, VIN = 1.0V (See Note 2) Port A	1, 2, 3	-55°C, +25°C, +125°C	60	800	µA
Standby Power Supply Current	IDDSB	VDD = 5.5V, IO = 0mA, VIN =GND or VDD	1, 2, 3	-55°C, +25°C, +125°C	-	20	µA
Darlington Drive Voltage	VDAR	VDD = 4.5V, IO = -2.0mA, VIN = GND or VDD	1, 2, 3	-55°C, +25°C, +125°C	3.9	-	V
Functional Tests	FT	VDD = 4.5V and 5.5V, VIN = GND or VDD, f = 1MHz	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-
Noise Immunity Functional Test (Note 4)	FN	VDD = 5.5V, VIN = GND or VDD - 1.5V and VDD = 4.5V, VIN = 0.8V or VDD	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-

NOTES:

1. IBHH should be measured after raising VIN and then lowering to 3.0V.
2. IBHL should be measured after lowering VIN to VSS and then raising to 0.8V.
3. No internal current limiting exists on the Port Outputs. A resistor must be added externally to limit the current.
4. For VIH (VDD = 5.5V) and VIL (VDD = 4.5V) each of the following groups is tested separately with all other inputs using VIH = 2.6V, VIL = 0.4V: PA, PB, PC, Control Pins (Pins 5, 6, 8, 9, 35, 36).

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS T_A = -55°C to +125°C

PARAMETERS	SYMBOL	CONDITIONS	SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
READ							
Address Stable Before $\overline{RD}$	TAVRL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
Address Stable After $\overline{RD}$	TRHAX	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
$\overline{RD}$ Pulse Width	TRLRH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	250	-	ns
Data Valid From $\overline{RD}$	TRLDV	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	200	ns
Data Float After $\overline{RD}$	TRHDX	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	10	-	ns
Time Between $\overline{RD}$s and/or $\overline{WR}$s	TRWHRWL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	300	-	ns
WRITE							
Address Stable Before $\overline{WR}$	TAVWL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
Address Stable After $\overline{WR}$	TWHAX	VDD = 4.5, 5.5V, Ports A and B	9, 10, 11	-55°C, +25°C, +125°C	20	-	ns
		VDD = 4.5, 5.5V, Port C	9, 10, 11	-55°C, +25°C, +125°C	100	-	ns
$\overline{WR}$ Pulse Width	TWLWH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	100	-	ns
Data Valid to $\overline{WR}$ High	TDVWH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	100	-	ns
Data Valid After $\overline{WR}$ High	TWHDX	VDD = 4.5, 5.5V, Ports A and B	9, 10, 11	-55°C, +25°C, +125°C	30	-	ns
		VDD = 4.5, 5.5V, Port C	9, 10, 11	-55°C, +25°C, +125°C	100	-	
OTHER TIMINGS							
$\overline{WR}$ = 1 to Output	TWHPV	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	350	ns
Peripheral Data Before $\overline{RD}$	TPVRL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
Peripheral Data After $\overline{RD}$	TRHPX	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
$\overline{ACK}$ Pulse Width	TKLKH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	200	-	ns
$\overline{STB}$ Pulse Width	TSLSH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	100	-	ns
Peripheral Data Before $\overline{STB}$ High	TPVSH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	20	-	ns
Peripheral Data After $\overline{STB}$ High	TSHPX	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	50	-	ns
$\overline{ACK}$ = 0 to Output	TKLPV	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	175	ns
$\overline{ACK}$ = 1 to output Float	TKHPZ	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	10	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS T_A = -55°C to +125°C (Continued)

PARAMETERS	SYMBOL	CONDITIONS	SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
$\overline{WR}$ = 1 to $\overline{OBF}$ = 0	TWHOL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	150	ns
$\overline{ACK}$ = 0 to $\overline{OBF}$ = 1	TKLOH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	150	ns
$\overline{STB}$ = 0 to IBF = 1	TSLIH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	150	ns
$\overline{RD}$ = 1 to IBF = 0	TRHIL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	150	ns
$\overline{RD}$ = 0 to INTR = 1	TRLNL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	200	ns
$\overline{STB}$ = 1 t INTR = 1	TSHNH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	150	ns
$\overline{ACK}$ = 1 to INTR = 1	TKHNH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	150	ns
$\overline{WR}$ = 0 to INTR = 0	TWLNL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	200	ns
RESET Pulse Width	TRSHRSL	VDD = 4.5, 5.5V (Note 2)	9, 10, 11	-55°C, +25°C, +125°C	500	-	ns

NOTES:

1. AC's tested at worst case VDD, guaranteed over full operating range.
2. Period of initial RESET pulse after power-on must be at least 50µs. Subsequenct RESET pulses may be 500ns minimum.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz, All measurements referenced to device ground	T_A = +25°C	-	10	pF
I/O Capacitance	CI/O	VDD = Open, f = 1MHz, All measurements referenced to device ground	T_A = +25°C	-	20	pF
Data Float After $\overline{RD}$	TRHDX	VDD = 4.5V and 5.5V	-55°C < T_A < +125°C	-	75	ns
$\overline{ACK}$ = 1 to Output Float	TKHPZ	VDD = 4.5V and 5.5V	-55°C < T_A < +125°C	-	250	ns

NOTE: The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics

TALBE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

See +25°C limits in Table 1 and Table 2 for Post RAD limits (Subgroups 1, 7, 9)

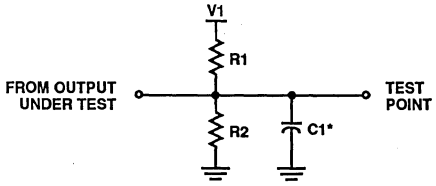
TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Static Current	IDDSB	±10µA
Input Leakage Current	IIL, IIH	±200nA
Output Leakage Current	IOZL, IOZH	±2µA
Low Level Output Voltage	VOL	±80mV
TTL Output High Voltage	VOH1	±600mV
CMOS Output High Voltage	VOH2	±150mV

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9
Interim Test		100%/5004	1, 7, 9	-
PDA		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B	B5	Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11	-
	Others	Samples/5004	1, 7	-
Group C		Samples/5004	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group D		Samples/5004	1, 7	1, 7
Group E, Subgroup 2		Samples/5004	1, 7, 9	1, 7, 9

AC Test Circuit

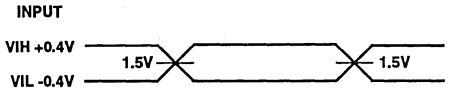


* Includes stray and jig capacitance

TEST CONDITIONS DEFINITION TABLE

V1	R1	R2	C1
1.7V	523Ω	Open	150pF

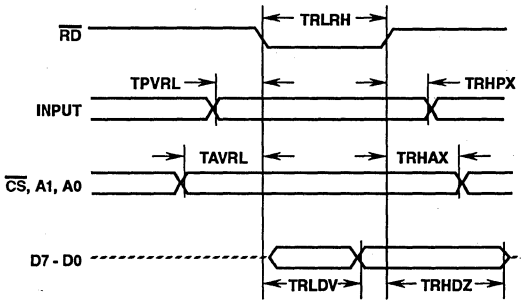
AC Testing Input, Output Waveforms



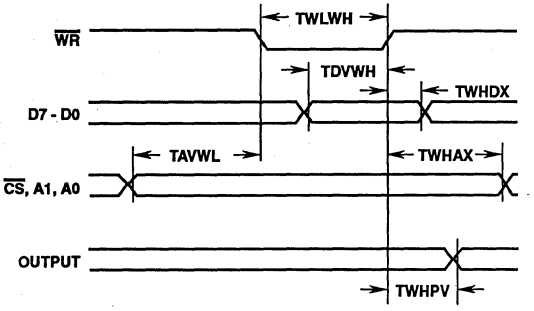
NOTE: AC Testing: All parameters tested as per test circuits. Input rise and fall times are driven at 1ns/V.

Waveforms

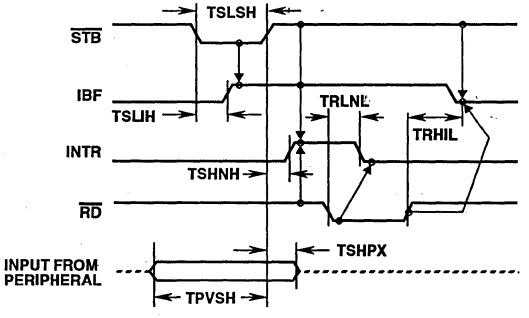
MODE 0 (BASIC INPUT)



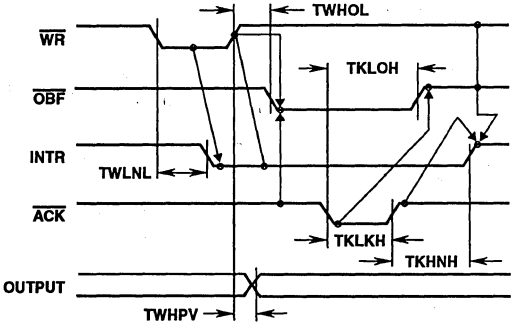
MODE 0 (BASIC OUTPUT)



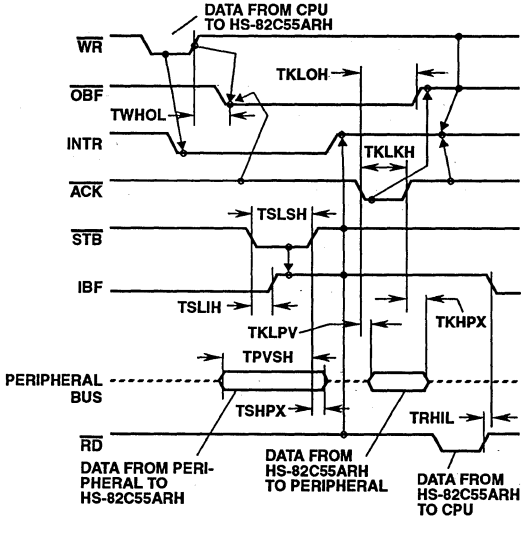
MODE 1 (STROBED INPUT)



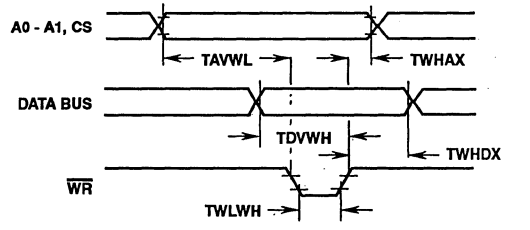
MODE 1 (STROBED OUTPUT)



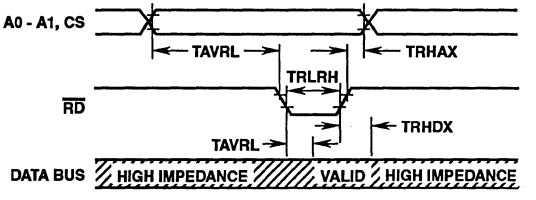
MODE 2 (BIDIRECTIONAL)



WRITE TIMING



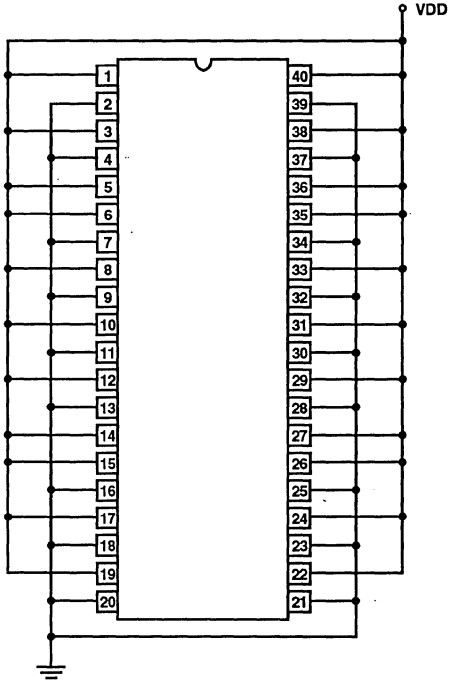
READ TIMING



NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.

Burn-In Circuits

PROGRAMMABLE PERIPHERAL INTERFACE

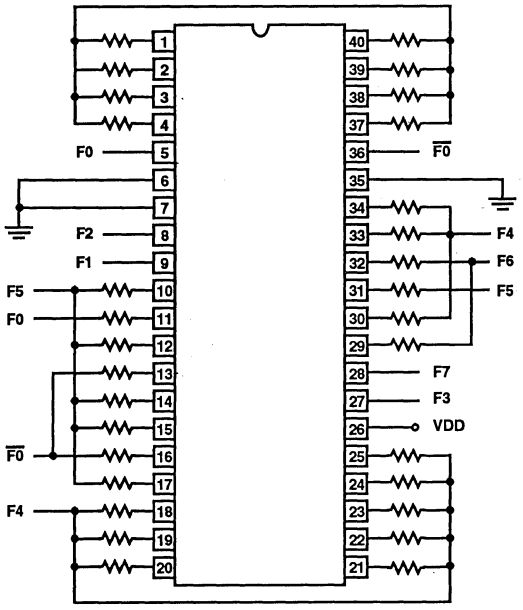


STATIC CONFIGURATION

NOTES:

VDD = 6.0V ± 0. 5%
IDD <500µA
T_A Min = +125°C

PROGRAMMABLE PERIPHERAL INTERFACE



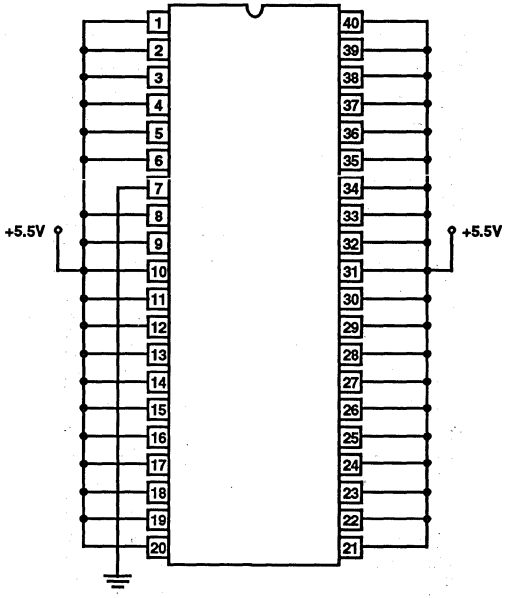
DYNAMIC CONFIGURATION

NOTES:

VDD = 6.0V ± 5% for Burn-In
VDD = 5.0V ± 5% for Life Test
All resistors are 10KΩ ± 5%
-0.3V ≤ VIL ≤ 0.8V
VDD - 1.0V ≤ VIH ≤ VDD
IDD < 5mA
F0 = 10KHz, 50% Duty cycle
F1 = F0/2; F2 = F1/2; F3 = F2/2; F4 = F3/2 . . . F7 = F6/2
T_A Min = +125°C

Irradiation Circuit

CMOS PROGRAMMABLE PERIPHERAL INTERFACE



NOTES:

VDD = 5.5V
All Group E Testing is performed in a ceramic side brazed DIP
Group E Sample Size is 2 die/wafer

Harris - Space Level '-Q' Flow

SEM - Traceable to Diffusion Method 2018
Wafer Lot Acceptance Method 5007
Internal Visual Inspection
Gamma Radiation Assurance Tests Method 1019
100% Nondestructive Bond Pull Method 2023
Customer Pre-Cap Visual Inspection (Note 1)
Temperature Cycling Method 1010 Condition C
Constant Acceleration Method 2001 Y1 30KG
Particle Impact Noise Detection Method 2020, Condition A 20G
Serialization
X-Ray Inspection Method 2012 (Two Views)
Initial Electrical Tests (T0)
Static Burn-In 72 Hour, +125°C, Method 1015 Condition A
+25°C Interim Electrical Tests Subgroups 1, 7, 9 (T1)
Burn-In Delta Calculation (T0 - T1)
PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ
Dynamic Burn-In 240 Hours, +125°C Method 1015 Condition D
+25°C Electrical Tests (T2) Subgroups 1, 7, 9 (T2)
Burn-In Delta Calculation (T0 - T2)
PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ
Electrical Test +125°C, -55°C
Group A Inspection Method 5005. 5% PDA (Note 3)
Fine and Gross Leak Tests Method 1014
Brand
Customer Source Inspection (Note 1)
Group B Inspection Method 5005 (Notes 1, 2)
Group D Inspection Method 5005 (Notes 1, 2)
External Visual Inspection Method 2009
Data Package Generation (Note 4)

NOTES:
1. These steps are optional, and must be negotiated as part of the order.
2. Group B and D data package contains Attributes Data plus Variables Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable.
4. '-Q' Data Pack Contains:
   Cover Sheet:
   a) Purchase Order Number
   b) Customer Part Number
   c) Lot Date Code
   d) Harris Part Number
   e) Lot Number
   f) Quantity
   Certificate of Conformance (as found on shipper).
   Shippable serial number list.
   Test Attributes (including Group A) for all test temperatures.
5. Test Variables data for all read/record and delta operations.
   +25°C Initial Test (T0)
   +25°C Interim Test (T1)
   +25°C Final Test (T2)
   All +25°C Delta's (T1-T0, T2-T0)
   +125°C Final Test
   -55°C Final Test
   Wafer Lot Acceptance Report (includes SEM).
   X-Ray report and Film.
   Radiation Testing Certificate of Conformance.
   Assembly Attributes (Post seal).

Harris - '-8' Flow

Internal Visual Inspection
Gamma Radiation Assurance Tests Method 1019
Customer Pre-Cap Visual Inspection (Note 1)
Temperature Cycling Method 1010 Condition C
Fine and Gross Leak Tests Method 1014
Constant Acceleration Method 2001 Y1 30KG
Initial Electrical Tests
Dynamic Burn-In 160 Hours, +125°C Method 1015 Condition D
+25°C Electrical Tests Subgroups 1, 7, 9
PDA Calculation: 5% Subgroups 1, 7
Electrical Test +125°C, -55°C
Group A Inspection Method 5005. 5% PDA (Note 3)
Brand
Customer Source Inspection (Note 1)
Group C Inspection Method 5005 (Notes 1, 2)
Group D Inspection Method 5005 (Notes 1, 2)
External Visual Inspection Method 2009
Data Package Generation (Note 4)

NOTES:
1. These steps are optional, and must be negotiated as part of the order.
2. Group B and D data package contains Attributes Data plus Variables Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable.
4. '-8' Data Pack Contains:
   Assembly Attributes (Post Seal).
   Test Attributes (Including Group A).
   Radiation Testing Certificate of Conformance.
   Certificate of Conformance (as found on shipper).

Metallization Topology

DIE DIMENSIONS:
3420µm x 4350µm x 485µm ± 25µm

METALLIZATION:
Type: Al/Si
Thickness: 11kÅ ± 2kÅ

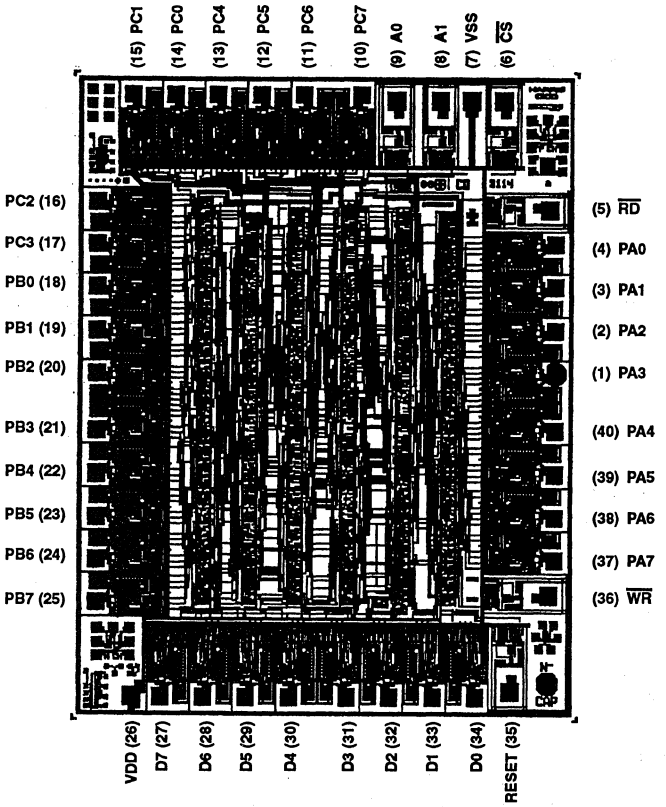
GLASSIVATION:
Type: SiO2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy

WORST CASE CURRENT DENSITY:
7.7×10^4 A/cm^2

Metallization Mask Layout

HS-82C55ARH



Functional Description

The HS-82C55ARH is a programmable peripheral interface designed to allow microcomputer systems to control and interface with all types of peripheral devices.It has the ability to generate and respond to all asynchronous handshaking signals necessary to transfer data to and from peripheral devices, and it can also interrupt the processor when a peripheral needs servicing. These capabilities allow the HS-82C55ARH to be used in an unlimited number of applications including EXTERNAL SYSTEM CONTROL, ASYNCHRONOUS DATA TRANSFER, and SYSTEMS MONITORING.

Data Bus Buffer

This tri-state bidirectional 8-bit buffer is used to interface the HS-82C55ARH to the system data bus (see Figure 1). Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

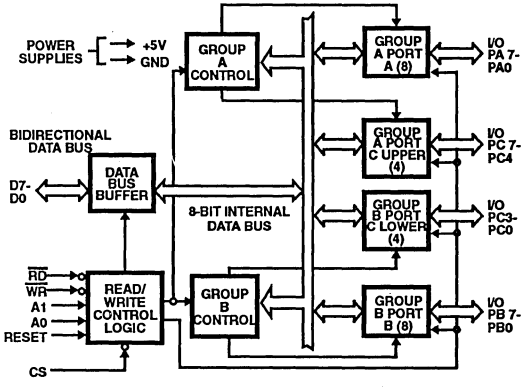


FIGURE 1. BLOCK DIAGRAM DATA BUS BUFFER, READ/WRITE, GROUP A AND B CONTROL LOGIC FUNCTIONS

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfer of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU writes a control word to the HS-82C55ARH. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the HS-82C55ARH.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group - Port A and Port C upper (C7 - C4)

Control Group - Port B and Port C lower (C3 - C0).

Ports A, B, C

The HS-82C55ARH contains three 8-bit ports (A, B and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the HS-82C55ARH.

Port A One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-down" bus hold devices are present on Port A. See Figure 2A.

Port B One 8-bit data input/output latch/buffer and one 8-bit data input buffer. See Figure 2B.

Port C One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and can be used for the control signal outputs and status signal inputs in conjunction with Ports A and B. See Figure 2B.

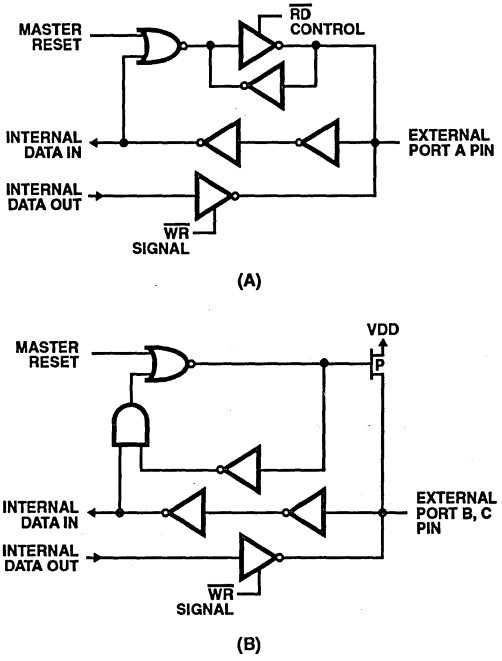


FIGURE 2. I/O PORT CONFIGURATION

Operational Description

Control Word

The data direction and mode of Ports A, B and C are determined by the contents of the Control Word. See Figure 4. The Control Word can be both written and read as shown in Table 1 and 2. During write operations, the function of the Control Word being written is determined by data bit D7. If D7 is low, the data on D0 - D3 will set or reset one of the bits of Port C. See Figure 5. During read Operations, the Control

Word will always be in the format illustrated in Figure 4 with Bit D7 high to indicate Control Word Mode Information.

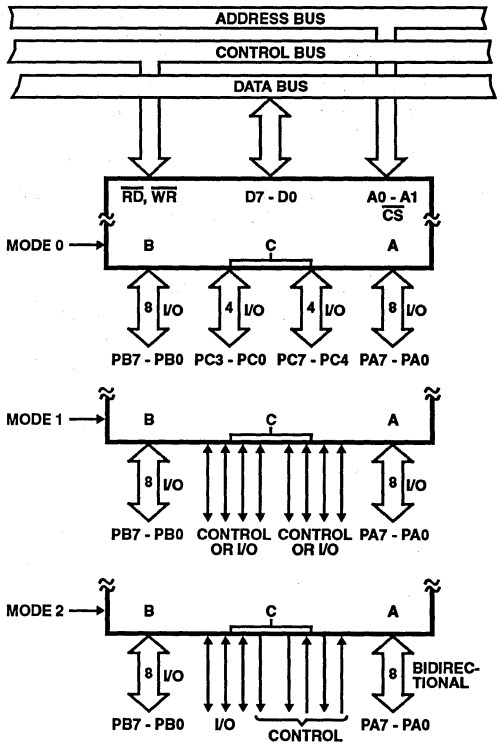


FIGURE 3. BASIC MODE DEFINITIONS & BUS INTERFACE

TABLE 1.

A1	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	Port A - Data Bus
0	1	0	1	0	Port B - Data Bus
1	0	0	1	0	Port C - Data Bus
1	1	0	1	0	Control Word - Data Bus

TABLE 2.

A1	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	OUTPUT OPERATION (WRITE)
0	0	1	0	0	Data Bus - Port A
0	1	1	0	0	Data Bus - Port B
1	0	1	0	0	Data Bus - Port C
1	1	1	0	0	Data Bus - Control Word

TABLE 3.

A1	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	DISABLE FUNCTION
X	X	X	X	1	Data Bus - 3-State
X	X	1	1	0	Data Bus - 3-State

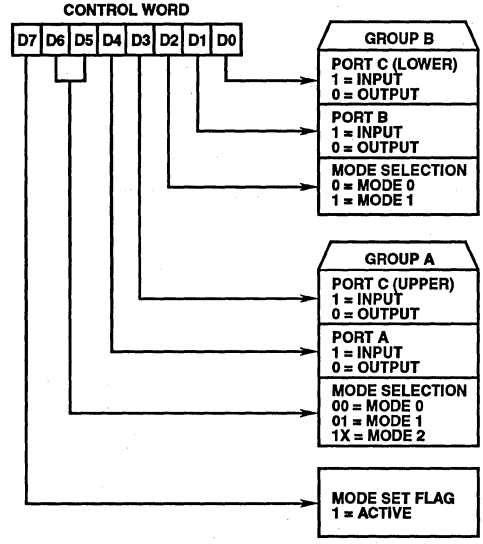


FIGURE 4. MODE SET CONTROL WORD FORMAT

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 - Basic Input/Output

Mode 1 - Strobed Input/Output

Mode 2 - Bidirectional Bus

When the RESET input goes "high", all ports will be set to the input mode with all 24 port lines held at the logic "one" level by internal bus hold devices. After reset, the HS-82C55ARH can remain in the input mode with no additional initialization required. This eliminates the need for pullup or pulldown resistors in all CMOS designs. During the execution of the system program, any of the other modes may be selected using a single output instruction. This allows a single HS-82C55ARH to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status register, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance: Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape recorder on an interrupt-driven basis.

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the HS-82C55ARH has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

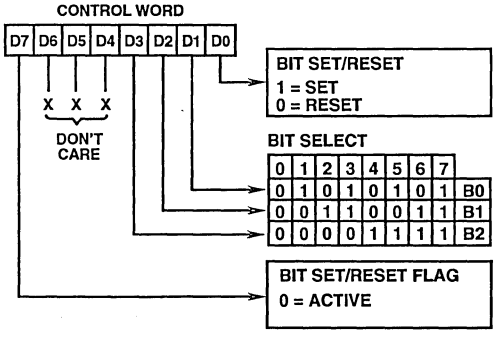


FIGURE 5. BIT SET/RESET CONTROL WORD FORMAT

Single Bit/Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. See Figure 5. This feature reduces software requirements in control-based applications.

Interrupt Control Functions

When the HS-82C55ARH is programmed to operate in Mode 1 or Mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from Port C, can be inhibited or enable by setting or resetting the associated INTE flip-flop, using the Bit Set/Reset function of Port C.

This function allows the programmer to enable or disable a CPU interrupt by a specific I/O device without affecting any other device in the interrupt structure.

INTE Flip-Flop Definition:

(BIT-SET) - INTE is SET - Interrupt enable.

(BIT-RESET) - INTE is RESET - Interrupt disable.

NOTE: All mask flip-flops are automatically reset during mode selection and device Reset.

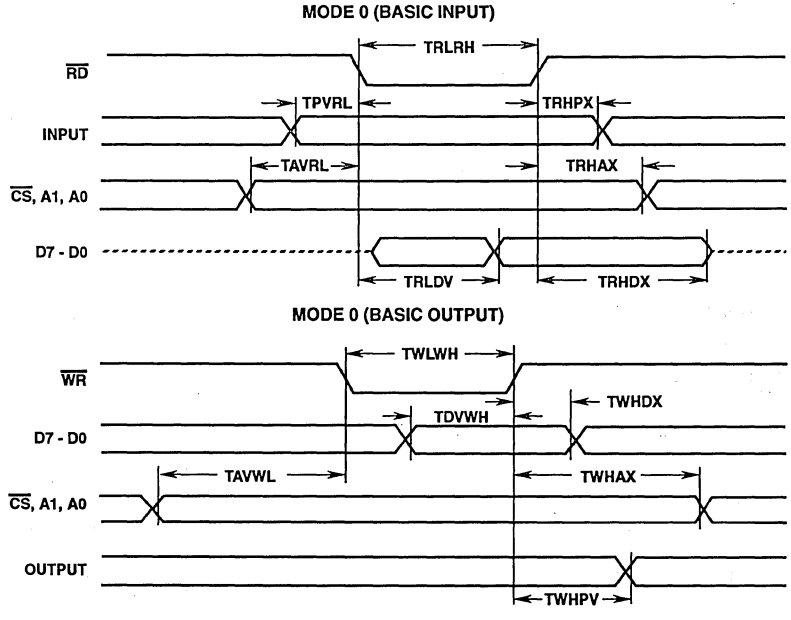
Operating Modes

Mode 0 (Basic Input/Output)

This functional configuration provides simple input and output operations for each of the three ports. No handshaking it required, data is simply written to or read from a specific port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports
- Any port can be input or output
- Outputs are latched
- Inputs are not latched
- 16 different Input/Output configurations possible

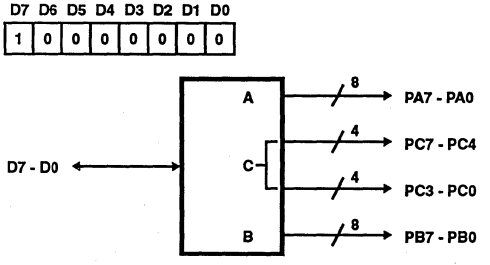


Mode 0 Port Definition

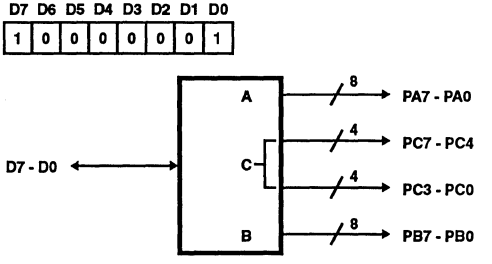
A		B		GROUP A			GROUP B	
D4	D3	D1	D0	PORT A	PORT C (UPPER)	NO.	PORT B	PORT C (LOWER)
0	0	0	0	Output	Output	0	Output	Output
0	0	0	1	Output	Output	1	Output	Input
0	0	1	0	Output	Output	2	Input	Output
0	0	1	1	Output	Output	3	Input	Input
0	1	0	0	Output	Input	4	Output	Output
0	1	0	1	Output	Input	5	Output	Input
0	1	1	0	Output	Input	6	Input	Output
0	1	1	1	Output	Input	7	Input	Input
1	0	0	0	Input	Output	8	Output	Output
1	0	0	1	Input	Output	9	Output	Input
1	0	1	0	Input	Output	10	Input	Output
1	0	1	1	Input	Output	11	Input	Input
1	1	0	0	Input	Input	12	Output	Output
1	1	0	1	Input	Input	13	Output	Input
1	1	1	0	Input	Input	14	Input	Output
1	1	1	1	Input	Input	15	Input	Input

Mode 0 Configurations

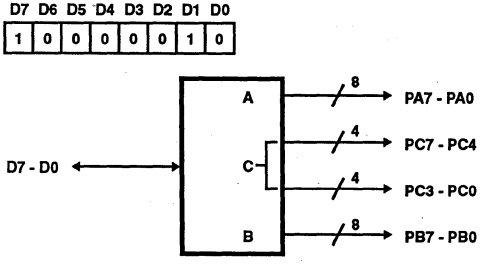
CONTROL WORD #0



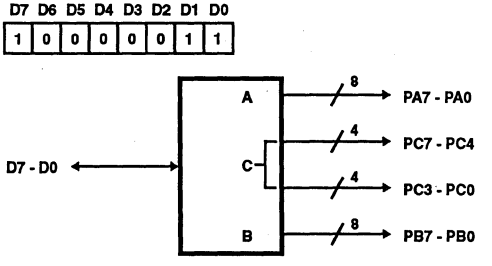
CONTROL WORD #1



CONTROL WORD #2



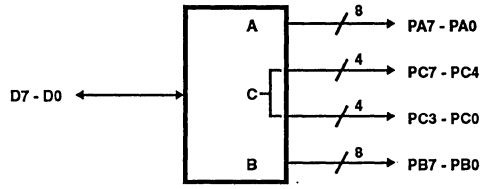
CONTROL WORD #3



Mode 0 Configurations (Continued)

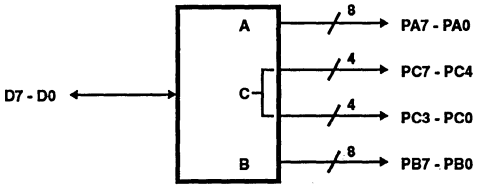
CONTROL WORD #4

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	0



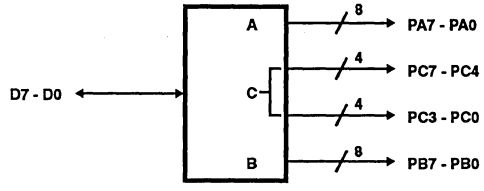
CONTROL WORD #5

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	0	1



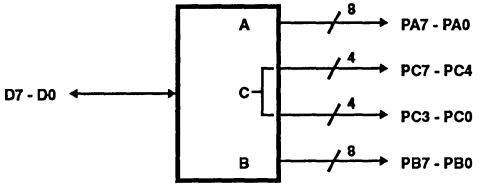
CONTROL WORD #6

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	0



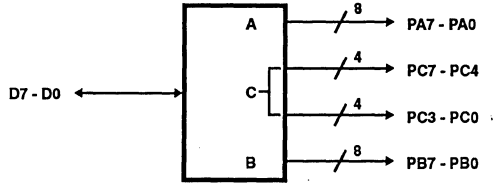
CONTROL WORD #7

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	1



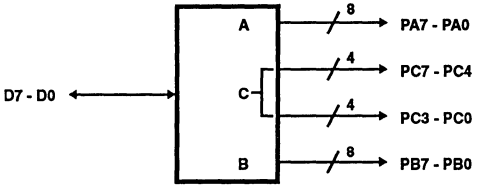
CONTROL WORD #8

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	0



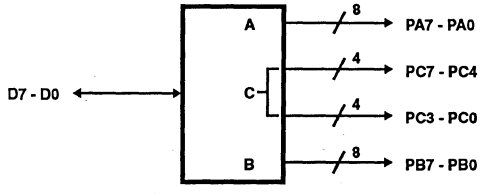
CONTROL WORD #9

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	1



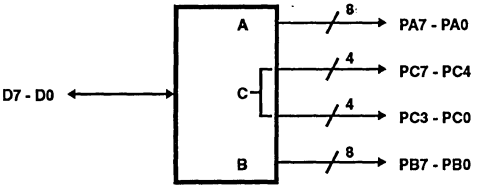
CONTROL WORD #10

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	1	0



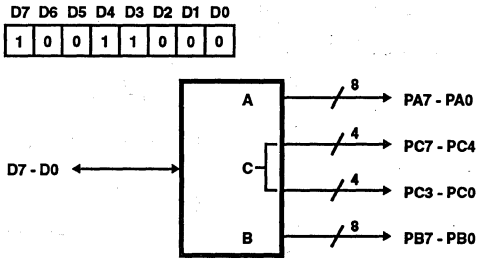
CONTROL WORD #11

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	1	1

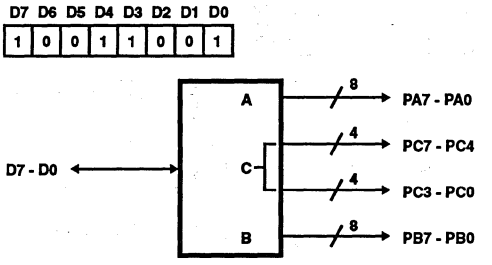


Mode 0 Configurations (Continued)

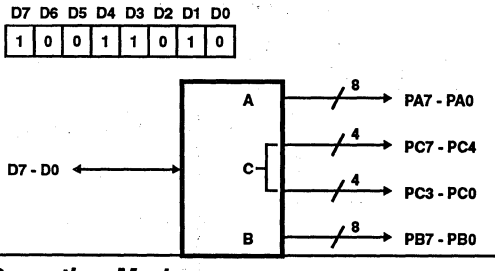
CONTROL WORD #12



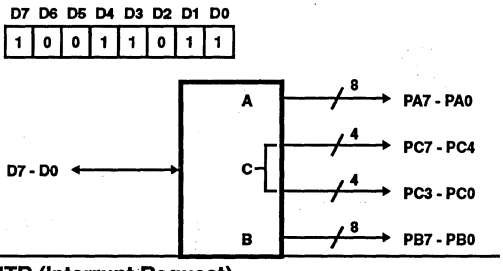
CONTROL WORD #13



CONTROL WORD #14



CONTROL WORD #15



Operating Modes

Mode 1 (Strobed Input/Output)

This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In Mode 1, Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit port.

Input Control Signal Definition

$\overline{STB}$ (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgment. IBF is set by $\overline{STB}$ input being low and is reset by the rising edge of the $\overline{RD}$ input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the rising edge of $\overline{STB}$ and reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by Bit Set/Reset of PC4.

INTE B

Controlled by Bit Set/Reset of PC2.

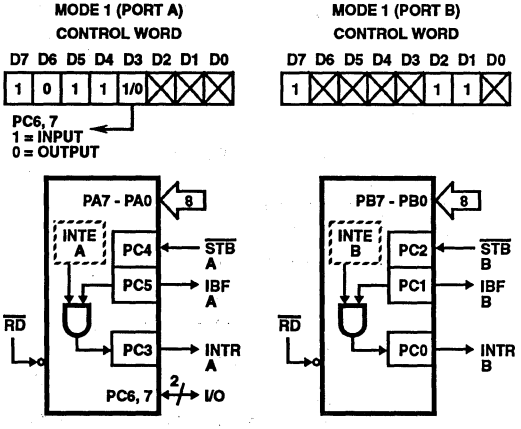


FIGURE 6. MODE 1 INPUT

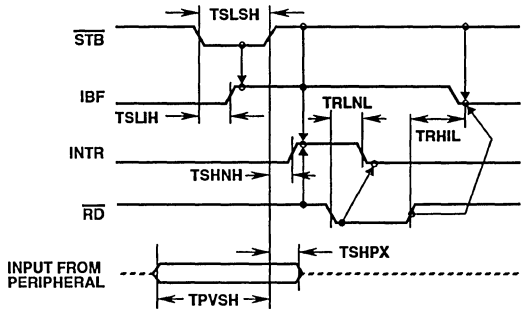


FIGURE 7. MODE 1 (STROBED INPUT)

Output Control Signal Definition

OBF (Output Buffer Full F/F)

The OBF output will go "low" to indicate that the CPU has written data out to the specified port. This does not mean valid data is sent out of the port at this time since OBF can go true before data is available. Data is guaranteed valid at the rising edge of OBF. See Note 1. The OBF F/F will be set by the rising edge of the WR input and reset by ACK input being low.

ACK (Acknowledge Input)

A "low" on this input informs the HS-82C55ARH that the data from Port A or Port B is ready to be accepted. In essence, a response from the peripheral device indicating that it is ready to accept data. See Note 1.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set by the rising edge of ACK and reset by the falling edge of WR.

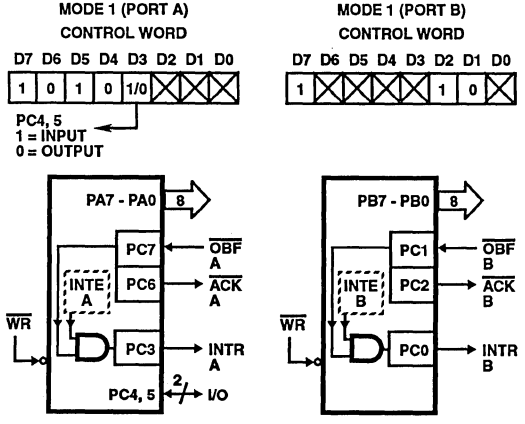


FIGURE 8. MODE 1 OUTPUT

INTE A

Controlled by Bit Set/Reset of PC6.

INTE B

Controlled by Bit Set/Reset of PC2.

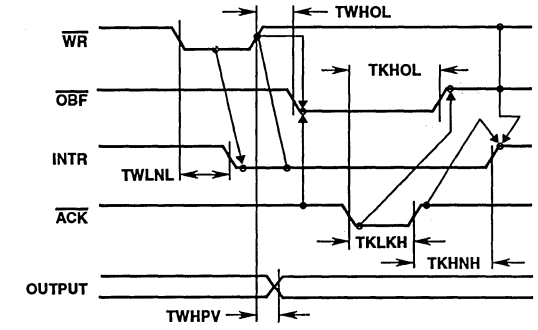


FIGURE 9. MODE 1 (STROBED OUTPUT)

NOTE:

1. To strobe data into the peripheral device, the user must operate the strobe line in a hand shaking mode. The user needs to send $\overline{OBF}$ to the peripheral device, generate an $\overline{ACK}$ from the peripheral device and then latch data into the peripheral device on the rising edge of $\overline{OBF}$.

Combinations of Mode 1: Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

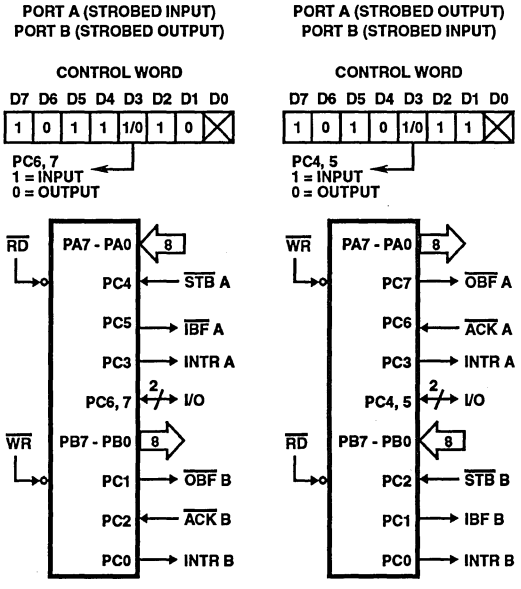


FIGURE 10. COMBINATIONS OF MODE 1

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O)

The functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline similar to MODE 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bidirectional bus port (Port A) and a 5-bit control port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bidirectional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request)

A high on this output can be used to interrupt the CPU for both input or output operations. INTR will be set either by the rising edge of $\overline{ACK}$ (INTE1 = 1) or the rising edge of $\overline{STB}$ (INTE2 = 1). INTR will be reset by the falling edge of $\overline{WR}$ (if previously set by the rising edge or $\overline{ACK}$), the falling edge of $\overline{RD}$ (if previously set by the rising edge of $\overline{STB}$), or the falling edge of $\overline{WR}$ when immediately following a low $\overline{RD}$ pulse or the falling edge of $\overline{RD}$ when immediately following a low $\overline{WR}$ pulse (if previously set by the rising edges of both $\overline{ACK}$ and $\overline{STB}$).

Output Operations

$\overline{OBF}$ (Output Buffer Full)

The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to Port A.

$\overline{ACK}$ (Acknowledge)

A "low" on this input enables the tri-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with $\overline{OBF}$)

Controlled by Bit Set/Reset of PC6.

Input Operations

$\overline{STB}$ (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF)

Controlled by Bit Set/Reset of PC4.

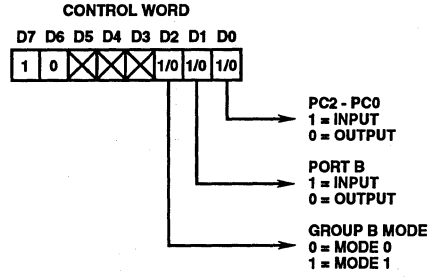


FIGURE 11. MODE CONTROL WORD

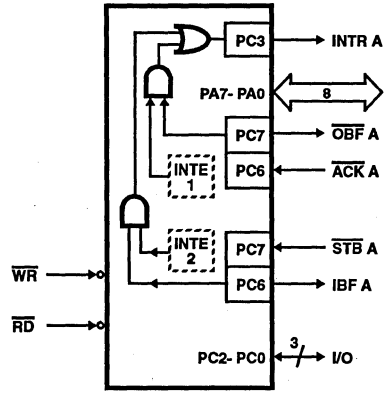
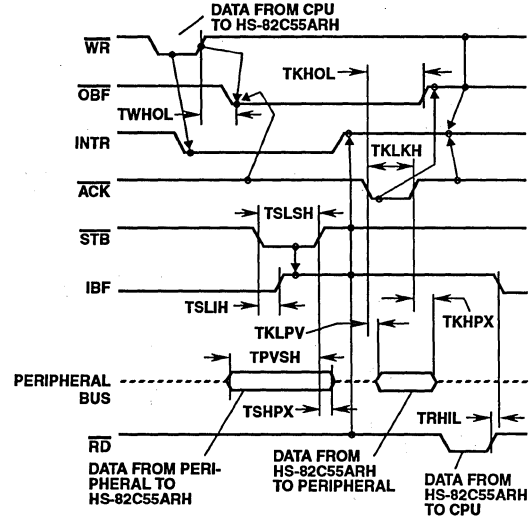


FIGURE 12. MODE 2 (BIDIRECTIONAL)



NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.

FIGURE 13. MODE 2 (BIDIRECTIONAL)

MODE DEFINITION SUMMARY

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA0	In	Out	In	Out	← →	
AP1	In	Out	In	Out	← →	
PA2	In	Out	In	Out	← →	
PA3	In	Out	In	Out	← →	
PA4	In	Out	In	Out	← →	
PA5	In	Out	In	Out	← →	
PA6	In	Out	In	Out	← →	
PA7	In	Out	In	Out	← →	
PB0	In	Out	In	Out	-	Mode 0 or Mode 1 Only
PB1	In	Out	In	Out	-	
PB2	In	Out	In	Out	-	
PB3	In	Out	In	Out	-	
PB4	In	Out	In	Out	-	
PB5	In	Out	In	Out	-	
PB6	In	Out	In	Out	-	
PB7	In	Out	In	Out	-	
PC0	In	Out	INTR B	INTR B	I/O	
PC1	In	Out	$\overline{IBF}$ B	$\overline{OBF}$ B	I/O	
PC2	In	Out	$\overline{STB}$ B	$\overline{ACK}$ B	I/O	
PC3	In	Out	INTR A	INTR A	INTR A	
PC4	In	Out	$\overline{STB}$ A	I/O	$\overline{STB}$ A	
PC5	In	Out	IBF A	I/O	IBF A	
PC6	In	Out	I/O	$\overline{ACK}$ A	$\overline{ACK}$ A	
PC7	In	Out	I/O	$\overline{OBF}$ A	$\overline{OBF}$ A	

Special Mode Combination Considerations

There are several combinations of modes possible. For any combination, some or all of Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a "Set Mode" command.

During a read of Port C, the state of all the Port C lines, except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus. In place of the ACK and STB line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 17.

Through a "Write Port C" command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a "Write Port C" command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in a Mode 1 group or to change an interrupt enable flag, the "Set/Reset Port C Bit" command must be used.

With a "Set/Reset Port C Bit" command, any Port C line programmed as an output (including IBF and $\overline{OBF}$) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, associated with Port C fare not affected by a "Set/Reset Port C Bit" command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the "Set/Reset Port C Bit" command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 17.

INPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
I/O	I/O	IBFA	INTEA	INTRA	INTEB	IBFB	INTRB
GROUP A					GROUP B		

OUTPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
$\overline{OBF}$A	INTEA	I/O	I/O	INTRA	INTEB	$\overline{OBF}$B	INTRB
GROUP A					GROUP B		

FIGURE 15. MODE 1 STATUS WORD FORMAT

D7	D6	D5	D4	D3	D2	D1	D0
$\overline{OBF}$A	INTE1	IBFA	INTE2	INTRA	X	X	X
GROUP A					GROUP B		

NOTE: (Defined by Mode 0 or Mode 1 Selection)

FIGURE 16. MODE 2 STATUS WORD FORMAT

Current Drive Capability

Any output on Port A, B or C can sink or source 2.5mA. This feature allows the 82C55A to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status (Figures 15 and 16)

In Mode 0, Port C transfers data to or from the peripheral device. When the 82C55A is programmed to function in Modes 1 or 2, Port C generates or accepts "hand shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

INTERRUPT ENABLE FLAG*	POSITION	ALTERNATE PORT C PIN SIGNAL (MODE)
INTE B	PC2	$\overline{ACK}$B (Output Mode 1) or STBB (Input Mode 1)
INTE A2	PC4	$\overline{STB}$A (Input Mode 1 or Mode 2)
INTE A1	PC6	$\overline{ACK}$A (Output Mode 1 or Mode 2)

FIGURE 17. INTERRUPT ENABLE FLAGS IN MODES 1 AND 2

HARRIS SEMICONDUCTOR

HS-82C85RH

Radiation Hardened CMOS Static Clock Controller/Generator

December 1992

Features

- Radiation Hardened
  - Total Dose > 10^5 RAD(Si)
  - Transient Upset > 10^8 RAD(Si)/s
  - Latch Up Free EPI-CMOS
  - Functional After Total Dose 1 x 10^6 RAD(Si)
- Very Low Power Consumption
- Pin Compatible with NMOS 8285 and Harris 82C85
- Generates System Clocks for Microprocessors and Peripherals
- Complete Control Over System Clock Operation for Very Low System Power
  - Stop-Oscillator
  - Stop-Clock
  - Low Frequency (Slo) Mode
  - Full Speed Operation
- DC to 15MHz Operation (DC to 5MHz System Clock)
- Generates Both 50% and 33% Duty Cycle Clocks (Synchronized)
- Uses Either Parallel Mode Crystal Circuit or External Frequency Source
- Hardened Field, Self-Aligned, Junction Isolated CMOS Process
- Single 5V Supply
- Military Temperature Range -55°C to +125°C

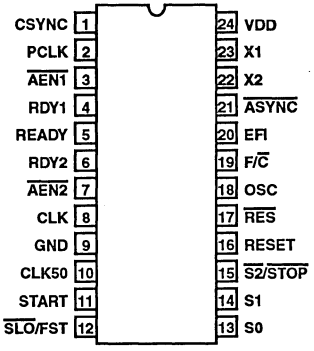
Description

The Harris HS-82C85RH is a high performance, radiation hardened CMOS Clock Controller/Generator designed to support systems utilizing radiation hardened static CMOS microprocessors such as the HS-80C86RH. The HS-82C85RH contains a crystal controlled oscillator, reset pulse conditioning, halt/restart logic, and divide-by-256 circuitry. These features provide the means to stop the system clock, stop the clock oscillator, or run the system at a low frequency (CLK/256), enhancing control of static system power dissipation and allowing system shut-down during periods of external stress.

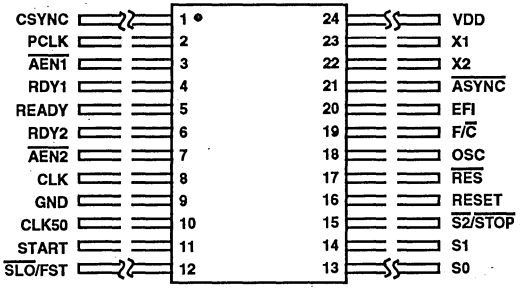
Static CMOS circuit design insures low operating power and permits operation with an external frequency source from DC to 15MHz. Crystal controlled operation to 15MHz is guaranteed with the use of a parallel, fundamental mode crystal and two small load capacitors. Outputs are guaranteed compatible with both CMOS and TTL specifications. The Harris hardened field CMOS process results in performance equal to or greater than existing radiation resistant products at a fraction of the power.

Pinout

24 PIN DIP
CASE OUTLINE D-3, CONFIGURATION 3
TOP VIEW



24 PIN FLATPACK
CASE OUTLINE F-6A, CONFIGURATION 2
TOP VIEW



11 µPROCESSOR PERIPHERALS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3044

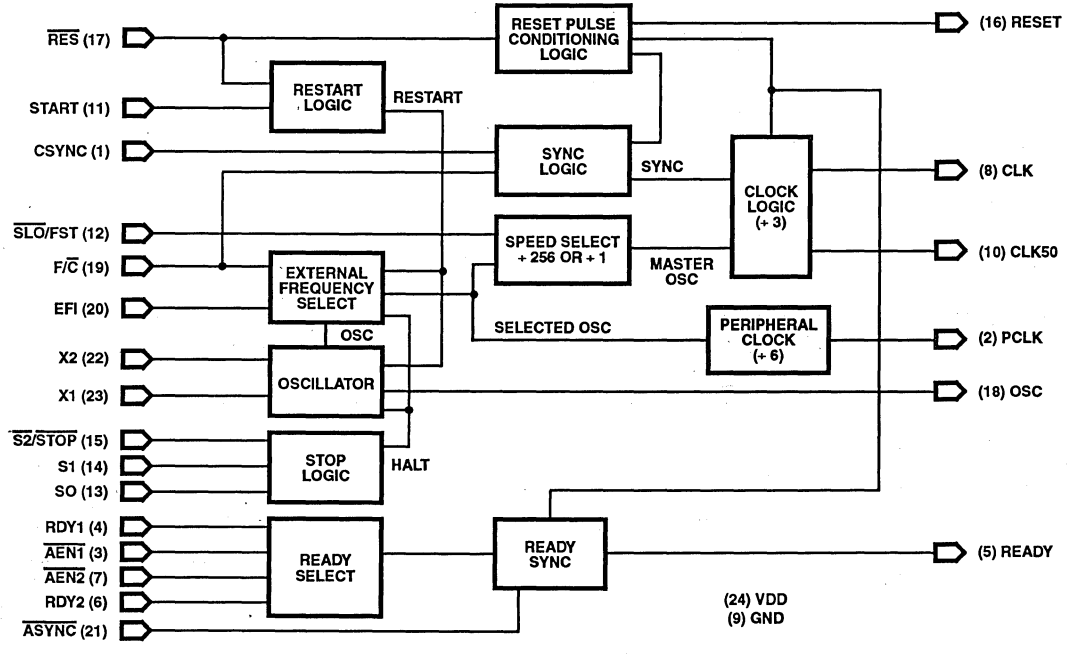
Pin Description

PIN	PIN NUMBER	TYPE	DESCRIPTION
X1 X2	23 22	I O	CRYSTAL CONNECTIONS: X1 and X2 are the crystal oscillator connections. The crystal frequency must be three times the maximum desired processor clock frequency. X1 is the oscillator circuit input and X2 is the output of the oscillator circuit.
EFI	20	I	EXTERNAL FREQUENCY IN: When F/$\overline{C}$ is HIGH, CLK is generated from the EFI input signal. This input signal should be a square wave with a frequency of three times the maximum desired CLK output frequency.
F/$\overline{C}$	19	I	FREQUENCY/CRYSTAL SELECT: F/$\overline{C}$ selects either the crystal oscillator or the EFI input as the main frequency source. When F/$\overline{C}$ is LOW, the HS-82C85RH clocks are derived from the crystal oscillator circuit. When F/$\overline{C}$ is HIGH, CLK is generated from the EFI input. F/$\overline{C}$ cannot be dynamically switched during normal operation.
START	11	I	A low-to-high transition on START will restart the CLK, CLK50 and PCLK outputs after the appropriate restart sequence is completed. When in the crystal mode (F/$\overline{C}$ LOW) with the oscillator stopped, the oscillator will be restarted when a Start command is received. The CLK, CLK50 and PCLK outputs will start after the oscillator input signal (X1) reaches the Schmitt trigger input threshold and an 8K internal counter reaches terminal count. If F/$\overline{C}$ is HIGH (EFI mode), CLK, CLK50 and PCLK will restart within 3 EFI cycles after START is recognized. The HS-82C85RH will restart in the same mode ($\overline{SLO}$/FST) in which it stopped. A high level on START disables the STOP mode.
S0 S1 $\overline{S2}$/$\overline{STOP}$	13 14 15	I I I	$\overline{S2}$/$\overline{STOP}$, S1, S0 are used to stop the HS-82C85RH clock outputs (CLK, CLK50, PCLK) and are sampled by the rising edge of CLK. CLK, CLK50 and PCLK are stopped by $\overline{S2}$/$\overline{STOP}$,S1, S0 being in the LHH state on the low-to-high transition of CLK. This LHH state must follow a passive HHH state occurring on the previous low-to-high CLK transition. CLK and CLK50 stop in the high state. PCLK stops in it's current state (high or low). When in the crystal mode (F/$\overline{C}$) low and a STOP command is issued, the HS-82C85RH oscillator will stop along with the CLK, CLK50 and PCLK outputs. When in the EFI mode, only the CLK, CLK50 and PCLK outputs will be halted. The oscillator circuit if operational, will continue to run. The oscillator and/or clock is restarted by the START input signal going true (HIGH) or the reset input ($\overline{RES}$) going low.
$\overline{SLO}$/FST	12	I	$\overline{SLO}$/FST is a level-triggered input. When HIGH, the CLK and CLK50 outputs run at the maximum frequency (crystal or EFI frequency divided by 3). When LOW, CLK and CLK50 frequencies are equal to the crystal or EFI frequency divided by 768. $\overline{SLO}$/FST mode changes are internally synchronized to eliminate glitches on the CLK and CLK50. START and STOP control of the oscillator or EFI is available in either the SLOW or FAST frequency modes. The $\overline{SLO}$/FST input must be held LOW for at least 195 OSC/EFI clock cycles before it will be recognized. This eliminates unwanted frequency changes which could be caused by glitches or noise transients. The $\overline{SLO}$/FST input must be held HIGH for at least 6 OSC/EFI clock pulses to guarantee a transition to FAST mode operation.
CLK	8	O	PROCESSOR CLOCK: CLK is the clock output used by the HS-80C86RH processor and other peripheral devices. When $\overline{SLO}$/FST is high, CLK has an output frequency which is equal to the crystal or EFI input frequency divided by three. When $\overline{SLO}$/FST is low, CLK has an output frequency which is equal to the crystal or EFI input frequency divide by 768. CLK has a 33% duty cycle.
CLK50	10	O	50% DUTY CYCLE CLOCK: CLK50 is an auxiliary clock with a 50% duty cycle and is synchronized to the falling edge of CLK. When $\overline{SLO}$/FST is high, CLK50 has an output frequency which is equal to the crystal or EFI input frequency divided by 3. When $\overline{SLO}$/FST is low, CLK50 has an output frequency equal to the crystal or EFI input frequency divided by 768.
PCLK	2	O	PERIPHERAL CLOCK: PCLK is a peripheral clock signal whose output frequency is equal to the crystal or EFI input frequency divided by six and has a 50% duty cycle. PCLK frequency is unaffected by the state of the $\overline{SLO}$/FST input.
OSC	18	O	OSCILLATOR OUTPUT: OSC is the output of the internal oscillator circuitry. Its frequency is equal to that of the crystal oscillator circuit. OSC is unaffected by the state of the $\overline{SLO}$/FST input. When the HS-82C85RH is in the crystal mode (F/$\overline{C}$ LOW) and a STOP command is issued, the OSC output will stop in the HIGH state. When the HS-82C85RH is in the EFI mode (F/$\overline{C}$ HIGH), the oscillator (if operational) will continue to run when a STOP command is issued and OSC remains active.

Pin Description (Continued)

PIN	PIN NUMBER	TYPE	DESCRIPTION
$\overline{RES}$	17	I	RESET IN: $\overline{RES}$ is an active LOW signal which is used to generate RESET. The HS-82C85RH provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration. $\overline{RES}$ starts crystal oscillator operation.
RESET	16	O	RESET: RESET is an active HIGH signal which is used to reset the HS-80C86RH processor. Its timing characteristics are determined by $\overline{RES}$. RESET is guaranteed to be HIGH for a minimum of 16 CLK pulses after the rising edge of $\overline{RES}$.
CSYNC	1	I	CLOCK SYNCHRONIZATION: CSYNC is an active HIGH signal which allows multiple HS-82C85RHs to be synchronized to provide multiple in-phase clock signals. When CSYNC is HIGH, the internal counters are reset and force CLK, CLK50 and PCLK into a HIGH state. When CSYNC is LOW, the internal counters are allowed to count and the CLK,CLK50 and PCLK outputs are active. CSYNC must be externally synchronized to EFI.
$\overline{AEN1}$ $\overline{AEN2}$	3 7	I I	ADDRESS ENABLE: $\overline{AEN}$ is an active LOW signal. $\overline{AEN}$ serves to qualify its respective Bus Ready Signal (RDY1 or RDY2). $\overline{AEN1}$ validates RDY1 while $\overline{AEN2}$ validates RDY2. Two $\overline{AEN}$ signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Buses.
RDY1 RDY2	4 6	I I	BUS READY: (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by $\overline{AEN1}$ while RDY2 is qualified by $\overline{AEN2}$.
$\overline{ASYNC}$	21	I	READY SYNCHRONIZATION SELECT: $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is LOW, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open or HIGH a single stage of READY synchronization is provided.
READY	5	O	READY: READY is an active HIGH signal which is used to inform the HS-80C86RH that it may conclude a pending data transfer.
GND	9	I	Ground
VDD	24	I	+5V power supply

Functional Diagram



Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage ..... VSS-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 5.33mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Brazed Seal DIP Package	61.1°C/W	14.7°C/W
Brazed Seal Flatpack Package	61.1°C/W	14.7°C/W

Maximum Package Power Dissipation at +125°C
Brazed Seal DIP Package 0.82W
Brazed Seal Flatpack Package 0.82W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
RESET Input High Voltage ..... 3.5V to VDD
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... 3.5V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CLK or CLK50 Output High Voltage	VOH	VDD = 4.5V, IO = -5.0mA, VIN = 0V or 4.5V	1, 2, 3	-55°C, +25°C, +125°C	VDD-0.4	-	V
Output High Voltage	VOH	VDD = 4.5V, IO = -2.5mA, VIN = 0V or 4.5V	1, 2, 3	-55°C, +25°C, +125°C	VDD-0.4	-	V
Output Low Voltage	VOL	VDD = 4.5V, IO = 5.0mA, VIN = 0V or 4.5V	1, 2, 3	-55°C, +25°C, +125°C	-	0.4	V
Input Leakage Current	IIL or IIH	VDD = 5.5V, VIN = 0V or 5.5V, Input Pins except: 11 to 15, 21, 23	1, 2, 3	-55°C, +25°C, +125°C	-1.0	1.0	µA
Bus Hold High Leakage Current (Note 1)	IBHH	VDD = 4.5V, 5.5V, VIN = 3.0V, Pins: 11 to 15, 21	1, 2, 3	-55°C, +25°C, +125°C	-200	-20	µA
Standby Power Supply Current	IDDSB	VDD = 5.5V, VIN = GND or VDD, IO = 0mA	1, 2, 3	-55°C, +25°C, +125°C	-	100	µA
Operating Power Supply Current	IDDOP	VDD = 5.5V, VIN = GND or VDD, IO = 0mA, Crystal Frequency = 15MHz	1, 2, 3	-55°C, +25°C, +125°C	-	80	mA
Functional Tests	FT	VDD = 4.5V and 5.5V, VIN = GND or VDD, f = 1MHz	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-
Noise Immunity Functional Test	FN	VDD = 5.5V, VIN = GND or 3.5V and VDD = 4.5V, VIN = 0.8V or VDD	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-

NOTE:

1. IBHH should be measured after raising VIN to VDD and then lowering to 3.0V

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS VDD = 4.5V, T_A = -55°C to +125°C

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
TIMING REQUIREMENTS							
External Frequency High Time	TEHEL	90% - 90% VIN	9, 10, 11	-55°C, +25°C, +125°C	25	-	ns
External Frequency Low Time	TELEH	10% - 10% VIN	9, 10, 11	-55°C, +25°C, +125°C	25	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS VDD = 4.5V, T_A = -55°C to +125°C (Continued)

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
EFI or Crystal Period	TELEL		9, 10, 11	-55°C, +25°C, +125°C	65	-	ns
External Frequency Input Duty Cycle	TEFIDC		9, 10, 11	-55°C, +25°C, +125°C	45	55	%
Crystal Frequency	FX		9, 10, 11	-55°C, +25°C, +125°C	2.4	15	MHz
RDY1, RDY2 Active Setup to CLK	TR1VCL	$\overline{ASYNC}$ = High	9, 10, 11	-55°C, +25°C, +125°C	55	-	ns
RDY1, RDY2 Active Setup to CLK	TR1VCH	$\overline{ASYNC}$ = Low	9, 10, 11	-55°C, +25°C, +125°C	55	-	ns
RDY1, RDY2 Inactive Setup to CLK	TR1VCL		9, 10, 11	-55°C, +25°C, +125°C	55	-	ns
RDY1, RDY2 Hold to CLK	TCLR1X		9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
$\overline{ASYNC}$ Setup to CLK	TAYVCL		9, 10, 11	-55°C, +25°C, +125°C	84	-	ns
$\overline{ASYNC}$ Hold to CLK	TCLAYX		9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
$\overline{AEN1}$, $\overline{AEN2}$ Setup to RDY1, RDY2	TA1VR1V		9, 10, 11	-55°C, +25°C, +125°C	25	-	ns
$\overline{AEN1}$, $\overline{AEN2}$ Hold to CLK	TCLA1X		9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
CSYNC Setup to EFI	TYHEH		9, 10, 11	-55°C, +25°C, +125°C	17	-	ns
CSYNC Hold to EFI	TEHYL		9, 10, 11	-55°C, +25°C, +125°C	17	-	ns
CSYNC Pulse Width	TYHYL		9, 10, 11	-55°C, +25°C, +125°C	2TELEL	-	ns
$\overline{RES}$ Setup to CLK	TI1HCL	Note 3	9, 10, 11	-55°C, +25°C, +125°C	105	-	ns
S0, S1, $\overline{S2}$/$\overline{STOP}$ Setup to CLK	TSVCH		9, 10, 11	-55°C, +25°C, +125°C	55	-	ns
S0, S1, $\overline{S2}$/$\overline{STOP}$ Hold to CLK	TCHSX		9, 10, 11	-55°C, +25°C, +125°C	55	-	ns
$\overline{RES}$, START Setup to CLK	TRSVCH	Note 3	9, 10, 11	-55°C, +25°C, +125°C	105	-	ns
$\overline{RES}$ (Low) or START (High) Pulse Width	TSHSL		9, 10, 11	-55°C, +25°C, +125°C	2/3 TCLCL	-	ns
$\overline{SLO}$/FST Setup to PCLK	TSFPC	Note 3	9, 10, 11	-55°C, +25°C, +125°C	TEHEL+170	-	ns
TIMING RESPONSES							
CLK/CLK50 Cycle Period	TCLCL		9, 10, 11	-55°C, +25°C, +125°C	200	-	ns
CLK HIGH Time	TCHCL		9, 10, 11	-55°C, +25°C, +125°C	(1/3 TCLCL)+3	-	ns
CLK LOW	TCLCH		9, 10, 11	-55°C, +25°C, +125°C	(2/3 TCLCL)-15	-	ns
CLK50 HIGH Time	T5CHCL		9, 10, 11	-55°C, +25°C, +125°C	(1/2 TCLCL)-7.5	-	ns
CLK50 LOW Time	T5CLCH		9, 10, 11	-55°C, +25°C, +125°C	(1/2 TCLCL)-7.5	-	ns
PCLK HIGH Time	TPHPL		9, 10, 11	-55°C, +25°C, +125°C	TCLCL-20	-	ns
PCLK LOW Time	TPLPH		9, 10, 11	-55°C, +25°C, +125°C	TCLCL-20	-	ns
Ready Inactive to CLK	TRYLCL	Note 4	9, 10, 11	-55°C, +25°C, +125°C	-8	-	ns
Ready Active to CLK	TRYHCH	Note 3	9, 10, 11	-55°C, +25°C, +125°C	2/3(TCLCL)-15	-	ns
CLK to Reset Delay	TCLIL		9, 10, 11	-55°C, +25°C, +125°C	-	65	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS VDD = 4.5V, T_A = -55°C to +125°C **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CLK to PCLK HIGH Delay	TCLPH		9, 10, 11	-55°C, +25°C, +125°C	-	40	ns
CLK to PCLK LOW Delay	TCLPL		9, 10, 11	-55°C, +25°C, +125°C	-	40	ns
OSC to CLK HIGH Delay	TOHCH		9, 10, 11	-55°C, +25°C, +125°C	-5	60	ns
OSC to CLK LOW Delay	TOHCL		9, 10, 11	-55°C, +25°C, +125°C	2	70	ns
OSC LOW to CLK50 HIGH Delay	TOLCH		9, 10, 11	-55°C, +25°C, +125°C	-5	60	ns
CLK LOW to CLK50 LOW Skew	TCLC50L		9, 10, 11	-55°C, +25°C, +125°C	-	10	ns

NOTES:

1. ACs tested at worst case VDD, guaranteed over full operating range
2. Setup and hold necessary only to guarantee recognition at next clock
3. Applies only to T3, TW states
4. Applies only to T2 states
5. All timing delays are measured at 1.5V, unless otherwise noted
6. Timing measurements made with EFI duty cycle = 50%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz, Note 2	T_A = +25°C	-	5	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz, Note 2	T_A = +25°C	-	15	pF
RESET Input Hysteresis	(+)VT - (-)VT	VDD = 4.5V and 5.5V	-55°C < T_A < +125°C	0.25	-	V
TIMING REQUIREMENTS						
$\overline{RES}$ or START Valid to CLK Low	TSTART	VDD = 4.5V and 5.5V	-55°C < T_A < +125°C	2TELEL+3	-	ns
$\overline{STOP}$ Command Valid to CLK High	TSTOP	VDD = 4.5V and 5.5V	-55°C < T_A < +125°C	TCLCL + TCLCH	3TCHCH +55	ns
TIMING RESPONSES						
CLK/CLK50 Rise Time	TCH1CH2	VDD = 4.5V and 5.5V, 1.0V to 3.5V	-55°C < T_A < +125°C	-	15	ns
CLK/CLK50 Fall Time	TCL1CL2	VDD = 4.5V and 5.5V, 3.5V to 1.0V	-55°C < T_A < +125°C	-	15	ns
Output Rise Time (Except CLK)	TOLOH	VDD = 4.5V and 5.5V, 0.8V to 2.0V	-55°C < T_A < +125°C	-	25	ns
Output Fall Time (Except CLK)	TOHOL	VDD = 4.5V and 5.5V, 2.0V to 0.8V	-55°C < T_A < +125°C	-	25	ns
Start/Reset Valid to CLK Low	TOST	VDD = 4.5V and 5.5V (TYP) Note 3	-55°C < T_A < +125°C	-	3	ms
RESET Output Time High	TRST	VDD = 4.5V and 5.5V	-55°C < T_A < +125°C	16(TCLCL)	-	ms

NOTES:

1. The parameters listed in table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. All measurements referenced to device ground.
3. Oscillator start-up time depends on several factors including crystal frequency, crystal manufacturer, capacitive load, temperature, power supply voltage, etc. This parameter is given for information only.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

See +25°C limits in Table 1 and Table 2 for Post RAD limits (Subgroups 1, 7, 9)

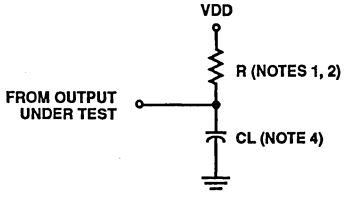
TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Static Current	IDDSB	±20µA
Input Leakage Current	IIL, IIH	±200nA
Output Leakage Current	IOZL, IOZH	±2µA
Low Level Output Voltage	VOL	±80mV
High Level Output Voltage	VOH	±150mV

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9
Interim Test		100%/5004	1, 7, 9	-
PDA		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B	B5	Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11	-
	Others	Samples/5004	1, 7	-
Group C		Samples/5004	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group D		Samples/5004	1, 7	1, 7
Group E, Subgroup 2		Samples/5004	1, 7, 9	1, 7, 9

AC Test Circuit

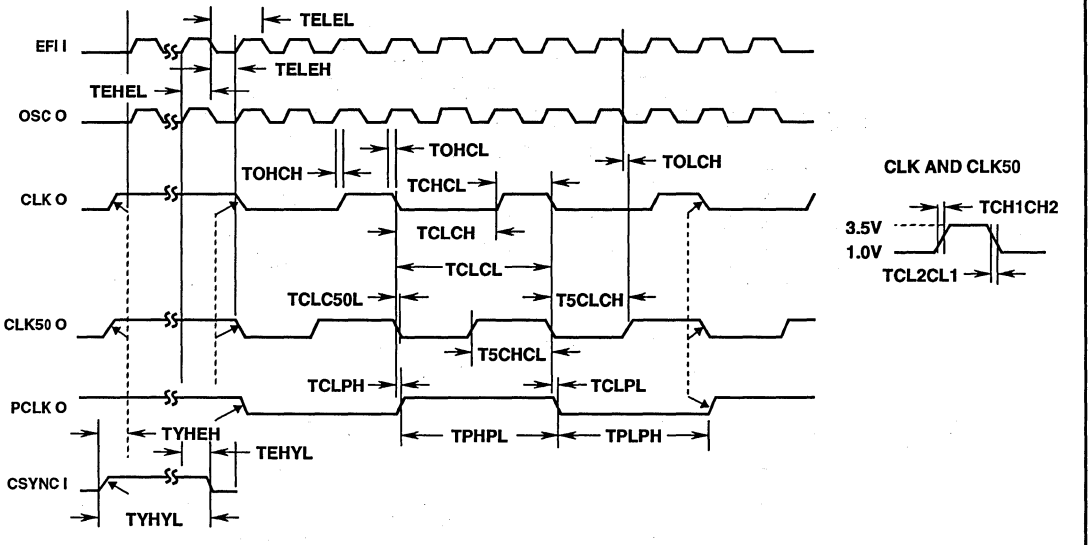


NOTES:

1. R = 370Ω at V = 2.25 for CLK and CLK50 outputs.
2. R = 494Ω at V = 2.87 for all other outputs.
3. CL = 50pF.
4. CL Includes probe and jig capacitance.

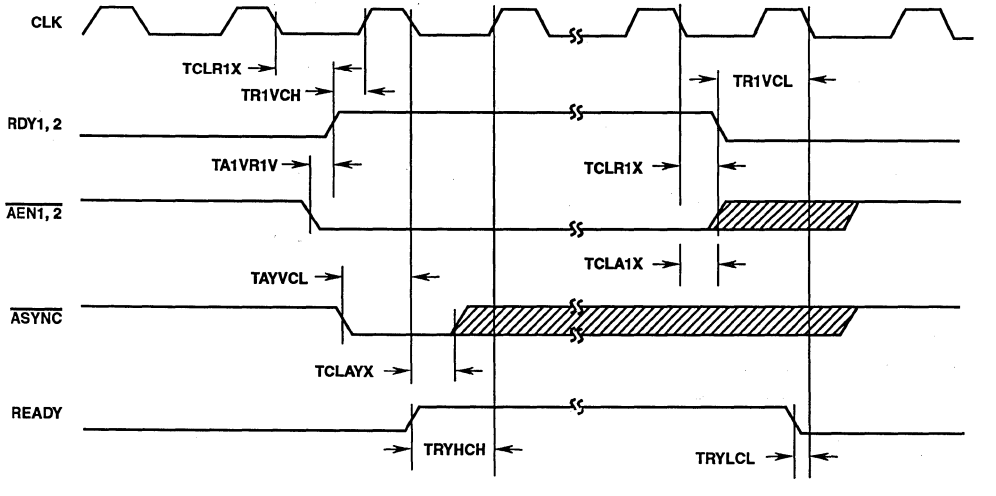
Waveforms

WAVEFORMS FOR CLOCKS



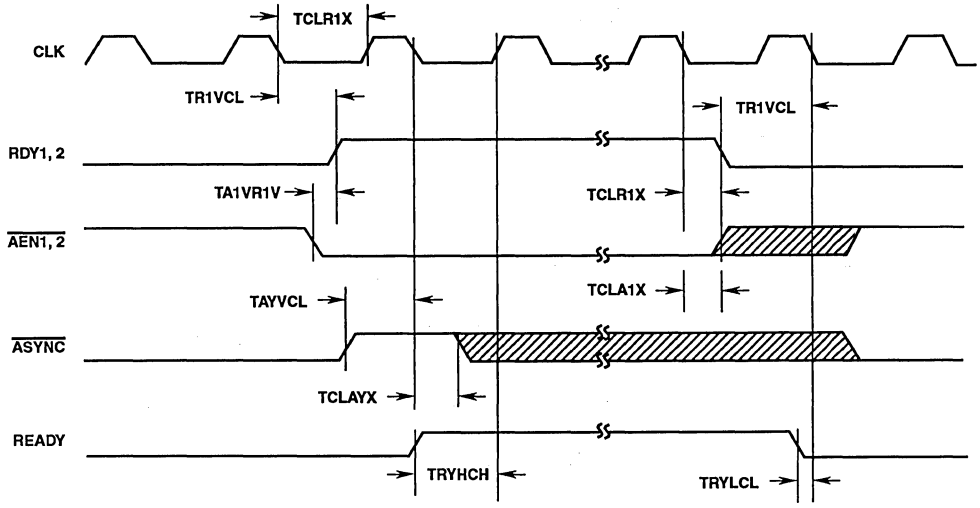
NOTE: All timing measurements are made at 1.5V, unless otherwise noted

WAVEFORMS FOR READY SIGNALS (FOR ASYNCHRONOUS DEVICES

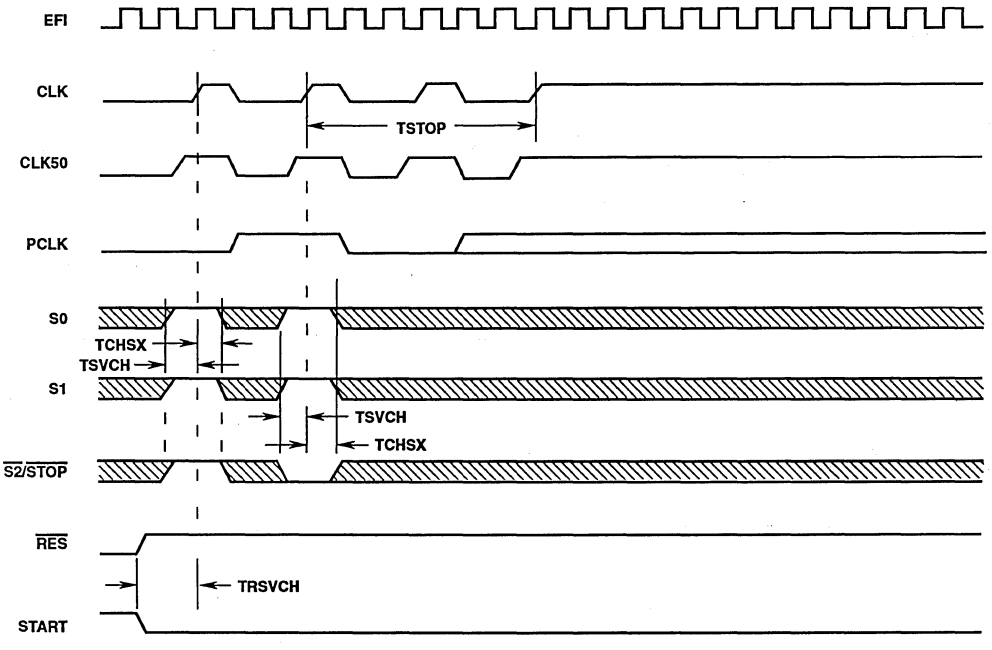


Waveforms (Continued)

WAVEFORMS FOR READY SIGNALS (FOR SYNCHRONOUS DEVICES)

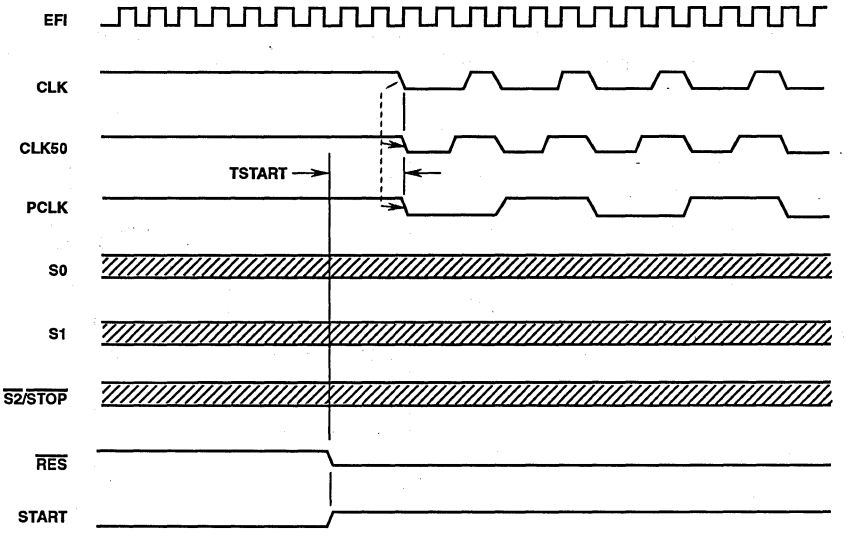


CLOCK STOP (F/$\overline{C}$ HIGH OR F/$\overline{C}$ LOW)

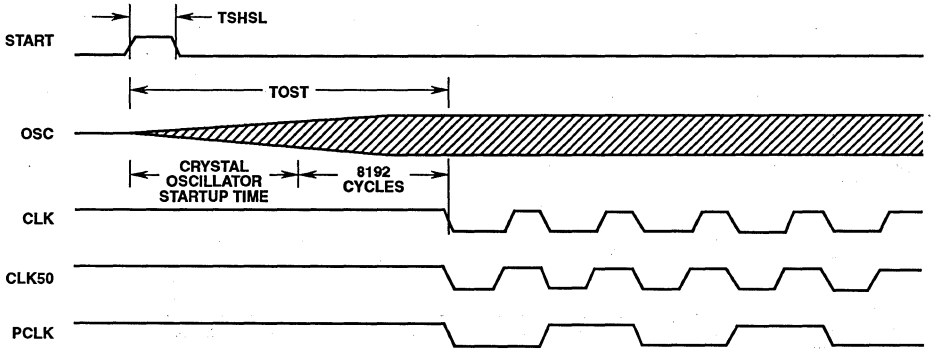


Waveforms (Continued)

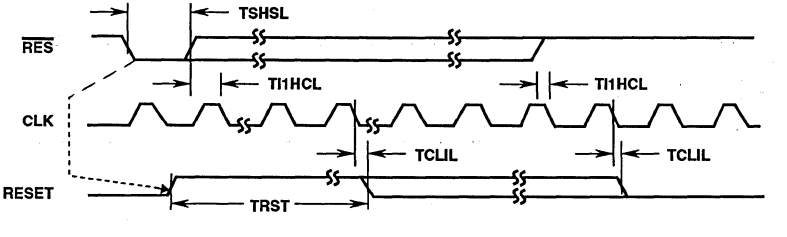
CLOCK START (F/$\overline{C}$ HIGH)



CLOCK START (F/$\overline{C}$ LOW)

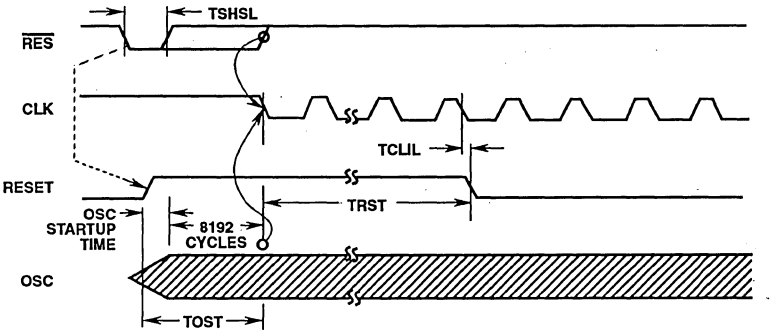


RESET TIMING (CLK RUNNING WITH F/$\overline{C}$ LOW - OSC MODE; CLK RUNNING - OR STOPPED WITH F/$\overline{C}$ HIGH EFI MODE



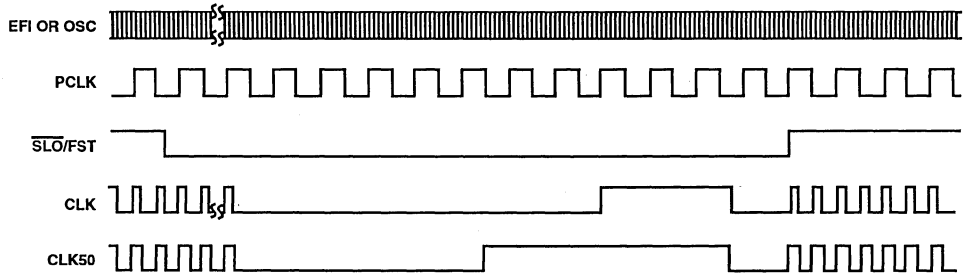
Waveforms (Continued)

RESET TIMING OSCILLATOR STOPPED (F/$\overline{C}$ LOW)

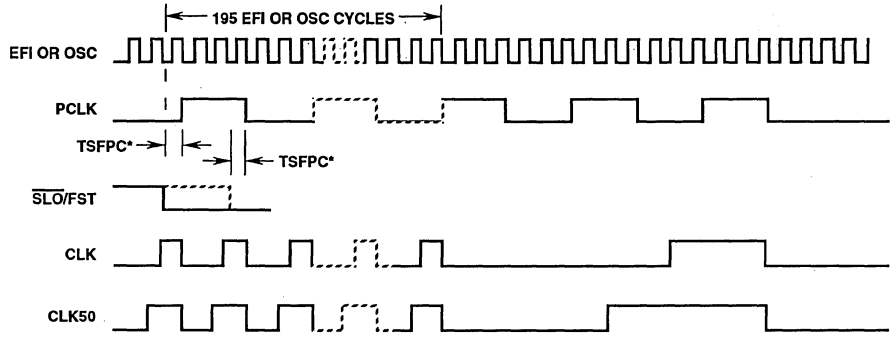


NOTE: CLK, CLK50, PCLK remain in the high state until $\overline{RES}$ goes high and 8192 valid oscillator cycles have been registered by the HS-82C85RH internal counter TOST time period). After $\overline{RES}$ goes high and CLK, CLK50, PCLK become active, the RESET output will remain high for a minimum of 16 CLK cycles (TRST).

SLO/FST TIMING OVERVIEW

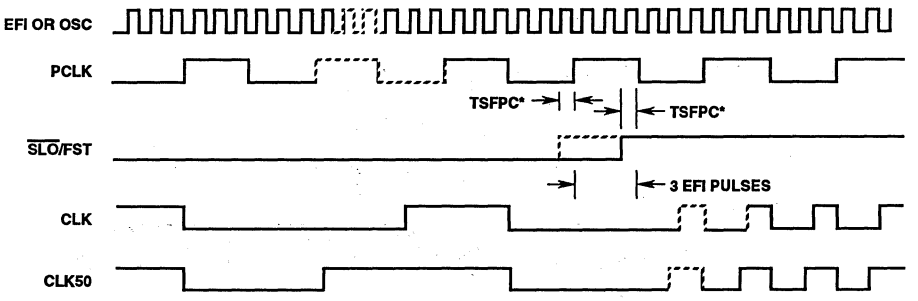


FAST TO SLOW CLOCK MODE TRANSITION



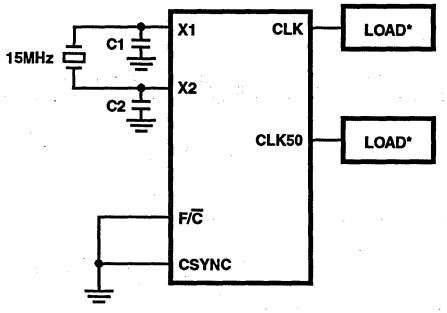
Waveforms (Continued)

SLOW TO FAST CLOCK MODE TRANSITION

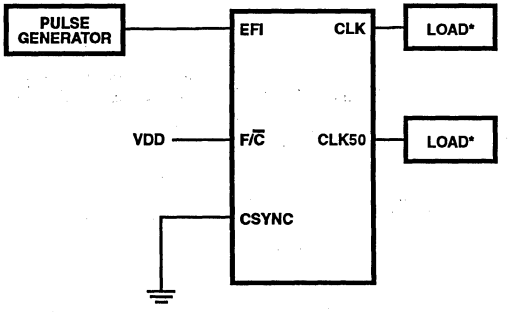


* If TSFPC is not met on one edge of PCLK, SLO/FST will be recognized on the next edge of PCLK.

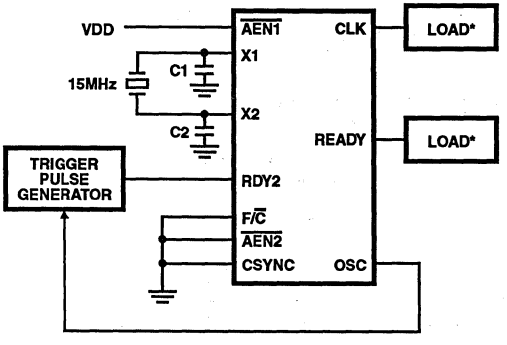
CLOCK HIGH AND LOW TIME (USING X1, X2)



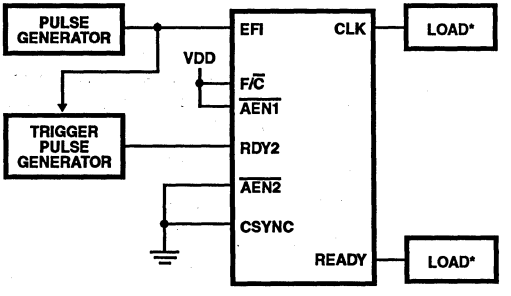
CLOCK HIGH AND LOW TIME (USING EFI)



READY TO CLOCK (USING X1, X2)

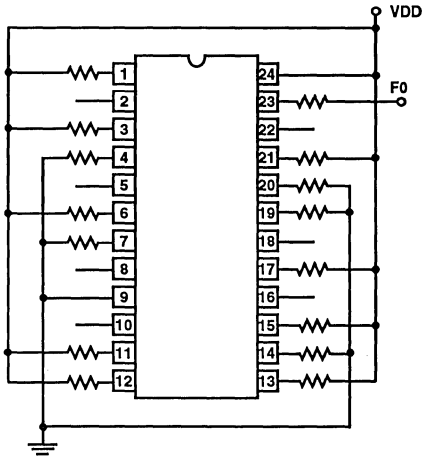


READY TO CLOCK (USING EFI)



* CL = 50pF

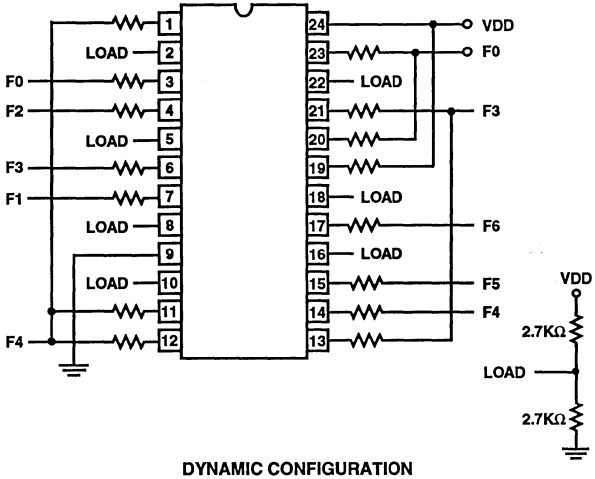
Burn-In Circuits



STATIC CONFIGURATION

NOTES:

R = 10kΩ
VDD = 6.0V ± 5%
T_A = +125°C Min
Package Code: SZ (24 Lead DIP)
F0 is 50% duty cycle square wave pulse burst. F0 is left low after pulse burst

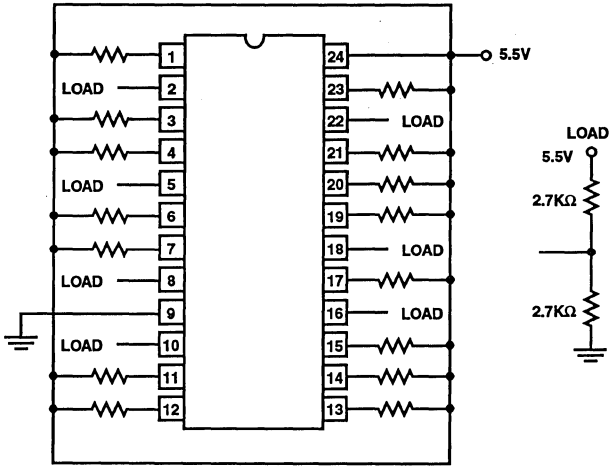


DYNAMIC CONFIGURATION

NOTES:

R = 10kΩ
VDD = 6.5V ± 5% (Burn-In); VDD = 6.0V ± 5% (Life Test)
T_A = +125°C Min
Package Code: SZ (24 Lead DIP)
F0 = 10kHz, 50% duty cycle
F1 = F0/2; F2 = F1/2; F3 = F2/2, F4 = F3/2; F5 = F4/2

Irradiation Circuit



NOTES:

R = 47kΩ
Pins tied to VSS (0V): Pin 9
Pins with loads: 2, 5, 8, 10, 16, 18, 22
Pins tied to VDD: 1, 3, 4, 6, 7, 11 - 15, 17, 19 - 21, 23, 24
VDD = 5.5V ± 0.5V
All Group E Testing is performed in the side brazed DIP
Group E Sample Size is 2 die/wafer

Harris - Space Level '-Q' Flow

SEM - Traceable to Diffusion Method 2018
Wafer Lot Acceptance Method 5007
Internal Visual Inspection
Gamma Radiation Assurance Tests Method 1019
100% Nondestructive Bond Pull Method 2023
Customer Pre-Cap Visual Inspection (Note 1)
Temperature Cycling Method 1010 Condition C
Constant Acceleration Method 2001 Y1 30KG
Particle Impact Noise Detection Method 2020, Condition A 20G
Serialization
X-Ray Inspection Method 2012 (Two Views)
Initial Electrical Tests (T0)
Static Burn-In 72 Hour, +125°C, Method 1015 Condition A
+25°C Interim Electrical Tests Subgroups 1, 7, 9 (T1)
Burn-In Delta Calculation (T0 - T1)
PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ
Dynamic Burn-In 240 Hours, +125°C Method 1015 Condition D
+25°C Electrical Tests (T2) Subgroups 1, 7, 9 (T2)
Burn-In Delta Calculation (T0 - T2)
PDA Calculation 3% Functional
5% Subgroups 1, 7, Δ
Electrical Test +125°C, -55°C
Group A Inspection Method 5005. 5% PDA (Note 3)
Fine and Gross Leak Tests Method 1014
Brand
Customer Source Inspection (Note 1)
Group B Inspection Method 5005 (Notes 1, 2)
Group D Inspection Method 5005 (Notes 1, 2)
External Visual Inspection Method 2009
Data Package Generation (Note 4)

NOTES:
1. These steps are optional, and must be negotiated as part of the order.
2. Group B and D data package contains Attributes Data plus Variables Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable.
4. '-Q' Data Pack Contains:
   Cover Sheet:
   a) Purchase Order Number
   b) Customer Part Number
   c) Lot Date Code
   d) Harris Part Number
   e) Lot Number
   f) Quantity
   Certificate of Conformance (as found on shipper).
   Shippable serial number list.
   Test Attributes (including Group A) for all test temperatures.
   Test Variables data for all read/record and delta operations.
   +25°C Initial Test (T0)
   +25°C Interim Test (T1)
   +25°C Final Test (T2)
   All +25°C Delta's (T1-T0, T2-T0)
   +125°C Final Test
   -55°C Final Test
   Wafer Lot Acceptance Report (includes SEM).
   X-Ray report and Film.
   Radiation Testing Certificate of Conformance.
   Assembly Attributes (Post seal).

Harris - '-8' Flow

Internal Visual Inspection
Gamma Radiation Assurance Tests Method 1019
Customer Pre-Cap Visual Inspection (Note 1)
Temperature Cycling Method 1010 Condition C
Fine and Gross Leak Tests Method 1014
Constant Acceleration Method 2001 Y1 30KG
Initial Electrical Tests
Dynamic Burn-In 160 Hours, +125°C Method 1015 Condition D
+25°C Electrical Tests Subgroups 1, 7, 9
PDA Calculation: 5% Subgroups 1, 7
Electrical Test +125°C, -55°C
Group A Inspection Method 5005. 5% PDA (Note 3)
Brand
Customer Source Inspection (Note 1)
Group C Inspection Method 5005 (Notes 1, 2)
Group D Inspection Method 5005 (Notes 1, 2)
External Visual Inspection Method 2009
Data Package Generation (Note 4)

NOTES:
1. These steps are optional, and must be negotiated as part of the order.
2. Group B and D data package contains Attributes Data plus Variables Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable.
4. '-8' Data Pack Contains:
   Assembly Attributes (Post Seal).
   Test Attributes (Including Group A).
   Radiation Testing Certificate of Conformance.
   Certificate of Conformance (as found on shipper).

Metallization Topology

DIE DIMENSIONS:
2770µm x 3130µm x 483µm ± 25µm

METALLIZATION:
Type: Al/Si
Thickness: 11kÅ ± 2kÅ

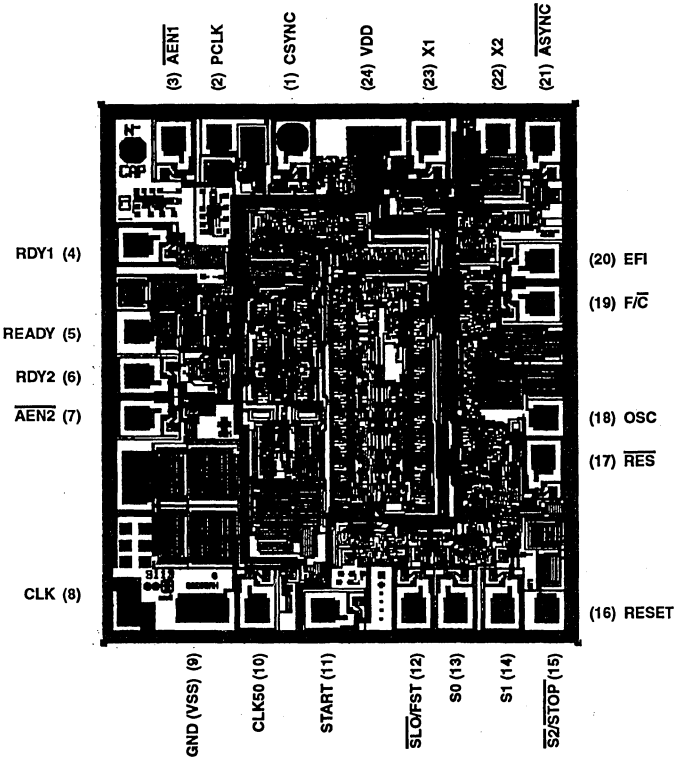
GLASSIVATION:
Type: SiO2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP- 460°C (Max)

WORST CASE CURRENT DENSITY:
1.6×10^4 A/cm^2

Metallization Mask Layout

HS-82C85RH



Functional Description

The HS-82C85RH Static Clock Controller/Generator provides simple and complete control of static CMOS system operating modes. The HS-82C85RH can operate with either an external crystal or an external frequency source and can support full speed, slow, stop-clock and stop-oscillator operation. While it is directly compatible with the Harris HS-80C86RH CMOS 16-bit static microprocessor, the HS-82C85RH can also be used for general purpose system clock control.

Separate signals are provided on the HS-82C85RH for stop and start control of the crystal oscillator and clock outputs. A single control line determines fast (crystal/EFI frequency divided by 3) or slow (crystal/EFI frequency divided by 768) mode operation. A clock synchronization input is provided to allow the use of multiple HS-82C85RHs in the same system. The HS-82C85RH generates the proper HS-80C86RH reset pulse, and it also handles all data transfer timing by generating the HS-80C86RH ready signal.

Automatic maximum mode HS-80C86RH software HALT instruction decode logic is present to ease the design of software-based clock control systems and provides complete software control of STOP mode operation.Automatic minimum mode software HALT instruction decoding can be easily implemented with a single 74HC74 device. Restart logic insures valid clock start-up and complete synchronization of CLK, CLK50 and PCLK.

Static Operating Modes

The HS-82C85RH Static Clock Controller can be dynamically set to operate in any one of four modes at anyone time: FAST, SLOW, STOP-CLOCK and STOP-OSCILLATOR. Each mode has distinct power and performance characteristics which can be matched to the needs of a particular system at a specific time (See Table 1).

Keep in mind that a single system may require all of these operating modes at one time or another during normal operation. A design need not be limited to a single operating mode or a specific combination of modes. The appropriate operating mode can be matched to the power-performance level needed at a specific time or in a particular circumstance.

Reset Logic

The HS-82C85RH reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate there set timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the HS-82C85RH.When in the crystal oscillator (F/$\overline{C}$ = LOW) or the EFI (F/$\overline{C}$ = HIGH) mode, a LOW state on the $\overline{RES}$ input will set the RESET output to the HIGH state. It will also restart the oscillator circuit if it is in the idle state. The RESET output is guaranteed to stay in the HIGH state for a minimum of 16 CLK cycles after a low-to-high transition of the RES input.

An oscillator restart count sequence will not be disturbed by RESET if this count is already in progress. After the restart counter expires, the RESET output will stay HIGH at least for 16 periods of CLK before going LOW. RESET can be kept high beyond this time by a continuing low input on the $\overline{RES}$ input.

If F/C is low (crystal oscillator mode), a low state on $\overline{RES}$ starts the crystal oscillator circuit. The stopped outputs remain inactive, until the oscillator signal amplitude reaches the X1 Schmitt trigger input threshold voltage and 8192 cycles of the crystal oscillator output are counted by an internal counter. After this count is complete, the stopped outputs (CLK, CLK50, PCLK) start cleanly with the proper phase relationships.

This 8192 count requirement insures that the CLK, CLK50 and PCLK outputs will meet minimum clock requirements and will not be affected by unstable oscillator characteristics which may exist during the oscillator start-up sequence. This sequence is also followed when a START command is issued while the HS-82C85RH oscillator is stopped.

Oscillator/Clock Start Control

Once the oscillator is stopped (or committed to stop) or at power-on, the restart sequence is initiated by a HIGH state on START or LOW state on $\overline{RES}$. If F/$\overline{C}$ is HIGH, then restart occurs immediately after the START or $\overline{RES}$ input is synchronized internally. This insures that stopped outputs (CLK, PCLK, OSC and CLK50) start cleanly with the proper phase relationship.

TABLE 1. STATIC SYSTEM OPERATING MODE CHARACTERISTICS

OPERATING MODE	DESCRIPTION	POWER LEVEL	PERFORMANCE
Stop-Oscillator	All system clocks and main clock oscillator are stopped	Maximum savings	Slowest response due to oscillator restart time
Stop-Clock	System CPU and peripherals clocks stop but main clock oscillator continues to run at rated frequency	Reduced system power	Fast restart - no oscillator restart time
Slow	System CPU clocks are slowed while peripheral clock and main clock oscillator run at rated frequency	Power dissipation slightly higher than Stop-Clock	Continuous operation at low frequency
Fast	All clocks and oscillators run at rated frequency	Highest power	Fastest response

If F/$\overline{C}$ is low (crystal oscillator mode), a HIGH state on the START input or a low state on $\overline{RES}$ causes the crystal oscillator to be restarted. The stopped outputs remain stopped, until the oscillator signal amplitude reaches the X1 Schmitt trigger input threshold voltage and 8192 cycles of the crystal oscillator output are counted by an internal counter. After this count is complete, the stopped outputs (CLK, CLK50, PCLK) start cleanly with the proper phase relationships.

Typically, any input signal which meets the START input timing requirements can be used to start the HS-82C85RH. In many cases, this would be the INT output from an HS-82C59A CMOS Priority Interrupt Controller (See Figure 1). This output, which is active high, can be connected to both the HS-82C85RH START pin and to the INTR input on the microprocessor.

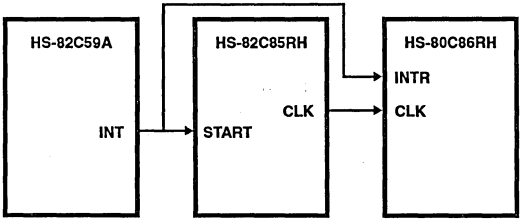


FIGURE 1. START CONTROL USING HS-82C59ARH INTERRUPT CONTROLLER

When the INT output becomes active (as a result of a "restart" IRQ or a system reset), the oscillator/clock circuit on the HS-82C85RH will restart. Upon completion of the appropriate restart sequence, the CLK signal to the CPU will become active. The CPU can then respond to the still-pending interrupt request.

Oscillator/Clock Stop Control

The S0, S1, and $\overline{S2}/\overline{STOP}$ control lines determine when the HS-82C85RH clock outputs or oscillator will stop. These three lines are designed to connect directly to the MAXimum mode HS-80C86RH status lines as shown in Figure 2.

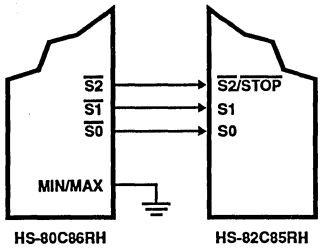


FIGURE 2. STOP CONTROL USING HS-80C86RH MAXIMUM MODE STATUS LINES

When used in this configuration, the HS-82C85RH will automatically recognize a software HALT command from the HS-80C86RH and stop the system clocks or oscillator.This allows complete software control of the STOP function.

If the HS-80C86RH is used in the MINimum mode, the HS-82C85RH can be controlled using the $\overline{S2}/\overline{STOP}$ input (with S0 and S1 held high). This can be done using the circuit shown in Figure 3. Since the HS-80C86RH, when executing a halt instruction in minimum mode, issues a single ALE pulse with no corresponding bus signals ($\overline{DEN}$ remains high), the ALE pulse will be clocked through the 74HC74 and put the HS-82C85RH into stop mode.

The HS-82C85RH status inputs $\overline{S2}/\overline{STOP}$, S1, S0 are sampled on the rising edge of CLK. The oscillator (F/$\overline{C}$ LOW only) and clock outputs are stopped by $\overline{S2}/\overline{STOP}$, S1, S0 being in the LHH state on a low-to-high transition of CLK. This LHH state must follow a passive HHH state occurring on the previous low-to-high CLK transition.CLK and CLK50 will stop in the logic HIGH state after two additional complete cycles of CLK. PCLK stops in its current state (HIGH or LOW). This is true for both SLOW and FAST mode operation.

Stop-Oscillator Mode

When the HS-82C85RH is stopped while in the crystal mode (F/C LOW), the oscillator, in addition to all system clock signals (CLK, CLK50 and PCLK), are stopped. CLK and

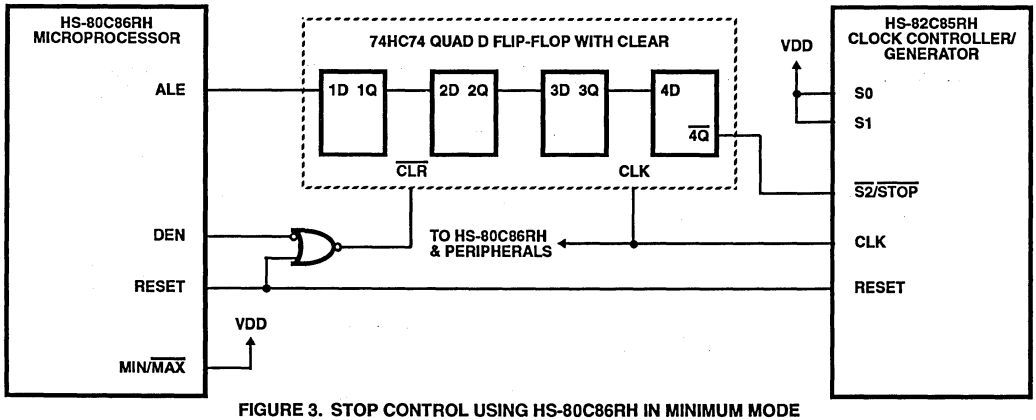


FIGURE 3. STOP CONTROL USING HS-80C86RH IN MINIMUM MODE

CLK50 stop in the high state. PCLK stops in its current state (high or low).

With the oscillator stopped, HS-82C85RH power drops to its lowest level. All clocks and oscillators are stopped. All devices in the system which are driven by the HS-82C85RH go into the lowest power standby mode.The HS-82C85RH also goes into standby and requires a power supply current of less than 100mA.

Stop-Clock Mode

When the HS-82C85RH is in the EFI mode (F/$\overline{C}$ HIGH) and a STOP command is issued, all system clock signals (CLK, CLK50 and PCLK) are stopped. CLK and CLK50 stop in the high state. PCLK stops in its current state (high or low).

The HS-82C85RH can also provide its own EFI source simply by connecting the OSC output to the EFI input and pulling the F/$\overline{C}$ input HIGH. This puts the HS-82C85RH into the External Frequency Mode using its own oscillator as an external source signal (See Figure 4). In this configuration, when the HS-82C85RH is stopped in the EFI mode, the oscillator continues to run. Only the clocks to the CPU and peripherals (CLK, CLK50 and PCLK) are stopped.

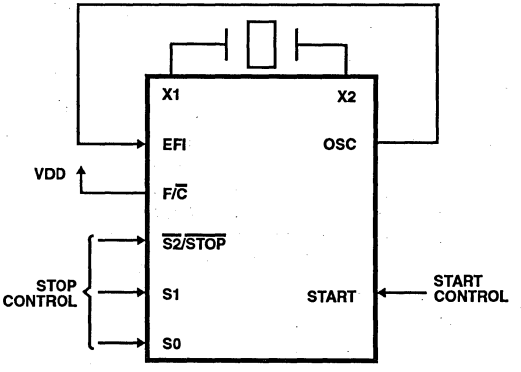


FIGURE 4. STOP-CLOCK MODE IN EFI MODE WITH OSCILLATOR AS FREQUENCY SOURCE

Clock Slow/Fast Operation

The $\overline{SLO}$/FST input determines whether the CLK and CLK50 outputs run at full speed (crystal or EFI frequency divided by 3) or at slow speed (crystal or EFI frequency divided by 768) (See Figure 5). When in the SLOW mode,HS-82C85RH stop-clock and stop-oscillator functions operate in the same manner as in the FAST mode, and the frequency of PCLK is unaffected.

The SLOW mode allows the CPU and the system to operate at a reduced rate which, in turn, reduces system power. For example, the operating power for the HS-80C86RH CPU is 10mA/MHz of clock frequency. When the SLOW mode is used in a typical 5MHz system, CLK and CLK50 run at approximately 20kHz. At this reduced frequency, the average operating current of the CPU drops to 200mA. Adding the HS-80C86RH 500mA standby current brings the total current to 700mA.

While the CPU and peripherals run slower and the HS-82C85RH CLK and CLK50 outputs switch at a reduced frequency, the main HS-82C85RH oscillator is still running at the maximum frequency (determined by the crystal or EFI input frequency.) Since CMOS power is directly related to operating frequency, HS-82C85RH power supply current will typically be reduced by 25% - 35%.

Internal logic requires that the $\overline{SLO}$/FST pin be held low for at least 195 oscillator or EFI clock pulses before the SLOW mode command is recognized. This requirement eliminates unwanted FAST-to-SLOW mode frequency changes which could be caused by glitches or noise spikes.

To guarantee FAST mode recognition, the $\overline{SLO}$/FST pin must be held high for at least 3 OSC or EFI pulses. The HS-82C85RH will begin FAST mode operation on the next PCLK edge after FAST command recognition. Proper CLK and CLK50 phase relationships are maintained and minimum pulse width specifications are met.

FAST-to-SLOW or SLOW-to-FAST mode changes will occur on the next rising or falling edge of PCLK. It is important to remember that the transition time for operating frequency changes, which are dependent upon PCLK, will vary with the HS-82C85RH oscillator or EFI frequency.

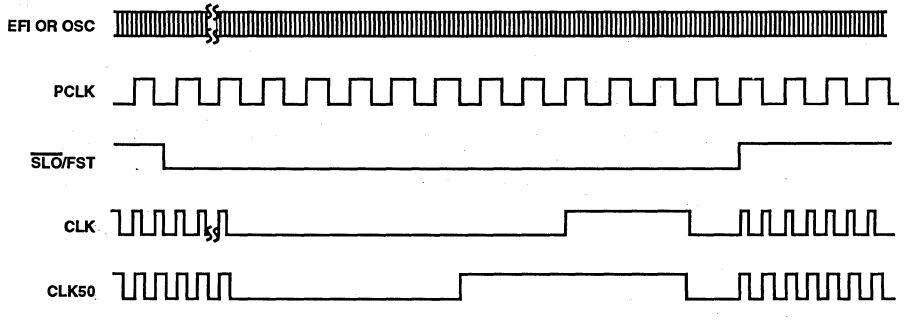


FIGURE 5. SLOW/FAST TIMING OVERVIEW

Slow/Fast Mode Control

The HS-82C55ARH programmable peripheral interface can be used to provide slow/fast mode control by connecting one of the port pins directly to the $\overline{SLO}$/FST pin (See Figure 6). With the port pin configured as an output, software control of the $\overline{SLO}$/FST pin is provided by simply writing a logical one (FAST mode) or logical zero (SLOW Mode) to the corresponding port. PORT C is well-suited for this function due to its bit set and reset capabilities.

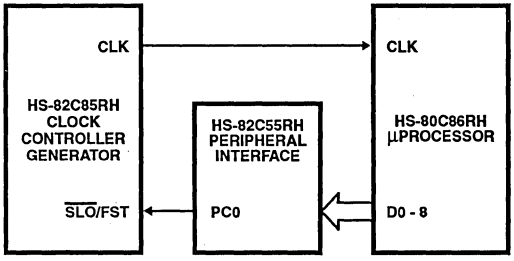


FIGURE 6. SLOW/FAST MODE CONTROL USING HS-82C55RH PERIPHERAL INTERFACE

Alternate Operating Modes

Using alternate modes of operation (slow, stop-clock, stop-oscillator) will reduce the average system operating power dissipation in a static CMOS system (See Table 2). This does not mean that system speed or throughput must be reduced. When used appropriately, the slow, stop-clock, stop-oscillator modes can make your design more power-efficient while maintaining maximum system performance.

TABLE 2. TYPICAL SYSTEM POWER SUPPLY CURRENT FOR STATIC CMOS OPERATING MODES

	FAST	SLOW	STOP-CLOCK	STOP-OSC
CPU Frequency	5MHz	20KHz	DC	DC
XTAL Frequency	15MHz	15MHz	15MHz	DC
IDD				
HS-80C86RH	50mA	2.5mA	250µA	250µA
HS-82C85RH	24.7mA	16.9mA	14.1mA	24.4µA
HS-82C08RH	1.0mA	10.0µA	1.0µA	1.0µA
82C82	1.7mA	6.5mA	1.0µA	1.0µA
HS-82C54RH	943.0µA	915.0µA	1.0µA	1.0µA
HS-82C55ARH	3.2µA	1.2µA	1.0µA	1.0µA
74HCXX + Other	2.9mA	110.0µA	90.0µA	90.0µA
HS-65262RH	4.0mA	50.0µA	10.0µA	10.0µA
HS-6617RH	6.3mA	52.5µA	12.0µA	12.0µA

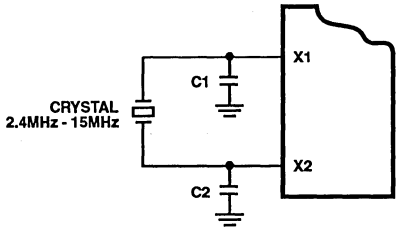
NOTE: All measurements taken at room temperature, VDD = +5.0V. Power supply current levels will be dependent upon system configuration and frequency of operation.

Oscillator

The oscillator circuit of the HS-82C85RH is designed primarily for use with an external parallel resonant, fundamental mode crystal from which the basic operating frequency is derived. The crystal frequency must be three times the required CPU clock. X1 and X2 are the two crystal input connections. The output of the oscillator is buffered and available at the OSC output (pin 18) for generation of other system timing signals.

For the most stable operation of the oscillator (OSC) output circuit, two capacitors (C1 = C2) are recommended. Capacitors C1 and C2 are chosen such that their combined capacitance matches the load capacitance as specified by the crystal manufacturer. This insures operation within the frequency tolerance specified by the crystal manufacturer.

The crystal/capacitor configuration and the formula used to determine the capacitor values are shown in Figure 7. Crystal Specifications are shown in Table 3. For additional information on crystal operation, see Harris publication Tech Brief 47.



$$CT = \frac{C1 \bullet C2}{C1 + C2}$$ (Including stray capacitance)

FIGURE 7. CRYSTAL CONNECTION

TABLE 3. CRYSTAL SPECIFICATIONS

PARAMETER	TYPICAL CRYSTAL SPECIFICATION
Frequency	2.4MHz to 15MHz
Type of Operation	Parallel Resonant, Fund. Mode
Load Capacitance	20pF or 32pF
R SERIES (Max)	56Ω (f = 15MHz, CL = 32pF), 105Ω (f = 15MHz, CL = 20pF)

Frequency Source Selection

The F/$\overline{C}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the source frequency for clock generation. If the EFI input is selected as the source, the oscillator section (OSC output) can be used independently for another clock source. If a crystal is not used, then crystal input X1 (pin 23) must be tied to VDD or GND and X2 (pin 22) should be left open. If the EFI mode is not used, then EFI (pin 20) should be tied to VDD or GND.

Clock Generator

The clock generator consists of two synchronous divide-by-three counters with special clear inputs that inhibit the counting. One counter generates a 33% duty cycle waveform (CLK) and the other generates a 50% duty cycle waveform (CLK50). These two counters are negative-edge synchronized, with the low-going transitions of both waveforms occurring on the same oscillator transition.The CLK and CLK50 output frequencies are one-third of the base input frequency when $\overline{SLO}$/FST is high and are equal to the base input frequency divided by 768 when $\overline{SLO}$/FST is low.

The CLK output is a 33% duty cycle clock signal designed to drive the HS-80C86RH microprocessor directly. CLK50 has a 50% duty cycle output synchronous with CLK, designed to drive coprocessors and peripherals requiring a 50% duty cycle clock.

PCLK is a peripheral clock signal with an output frequency equal to the oscillator or EFI frequency divided by 6. PCLK has a 50% duty cycle. PCLK is unaffected by $\overline{SLO}$/FST. When the HS-82C85RH is placed in the STOP mode, PCLK will remain in its current state (logic high or logic low) until a $\overline{RES}$ or START command restarts the HS-82C85RH clock circuitry. PCLK is negative-edge synchronized with CLK and CLK50.

Since PCLK continues to run at the same frequency regardless of the state of the $\overline{SLO}$/FST pin, it can be used by other devices in the system which need a fixed high frequency clock. For example, PCLK could be used to clock an HS-82C54RH programmable interval timer to produce a real-time clock for the system or as a baud rate generator to maintain serial data communications during SLOW mode operation.

Clock Synchronization

The clock synchronization (CSYNC) input allows the output clocks to be synchronized with an external event (such as another HS-82C85RH clock signal). CSYNC going active causes all clocks (CLK, CLK50 and PCLK) to stop in the HIGH state.

It is necessary to synchronize the CSYNC input to the EFI clock using two flip-flops as shown in Figure 8. Multiple external flip-flops are necessary to minimize the occurrence of metastable (or indeterminate) states.

Ready Synchronization

Two RDY inputs (RDY1, RDY2) are provided to accommodate two system buses. Each RDY input is qualified by its corresponding $\overline{AEN}$ input ($\overline{AEN1}$, $\overline{AEN2}$). Reception of a valid RDY signal causes the HS-82C85RH to output READY high, informing the HS-80C86RH that the pending data transfer may be concluded. (See HS-80C86RH data sheet system timing).

Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY set up and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

The $\overline{ASYNC}$ input defines two modes of RDY synchronization operation. When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active RDY input signals. Positive-going asynchronous RDY inputs will first be synchronized to flip-flop one at the rising edge of CLK (requiring a setup time TR1VCH) and then synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go HIGH.

Negative-going asynchronous RDY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the RDY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing (TR1VCL) on each bus cycle.

When $\overline{ASYNC}$ is high or left open, the first RDY flip-flop is bypassed in the RDY synchronization logic. RDY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time. $\overline{ASYNC}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

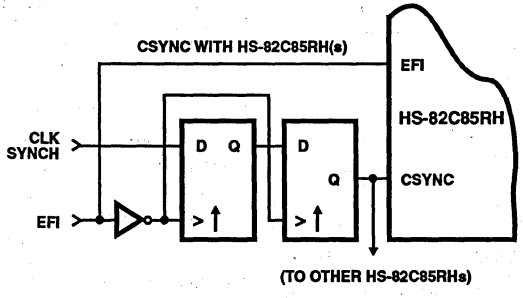


FIGURE 8. CSYNC SYNCHRONIZATION METHODS

HARRIS SEMICONDUCTOR

HS-83C55RH

Radiation Hardened 16K Bit CMOS ROM

December 1992

Features

- Radiation Hardened EPI-CMOS
  - Total Dose 1 x 10^5 RAD(Si)
  - Transient Upset > 1 x 10^8 RAD(Si)/s (Ports and DDR)
  - Latch-Up Free > 1 x 10^{12} RAD(Si)/s
- 2048 Words x 8 Bits ROM
- Electrically Equivalent to Sandia SA3002
- Pin Compatible with Intel 8355
- Bus Compatible with HS-80C85RH
- Single 5 Volt Power Supply
- Low Standby Current 100µA Max
- Low Operating Current 2mA/MHz
- Completely Static Design
- Internal Address Latches
- Two General Purpose 8-Bit I/O Ports
- Multiplexed Address and Data Bus
- Self Aligned Junction Isolated (SAJI) Process
- Military Temperature Range -55°C to +125°C

Description

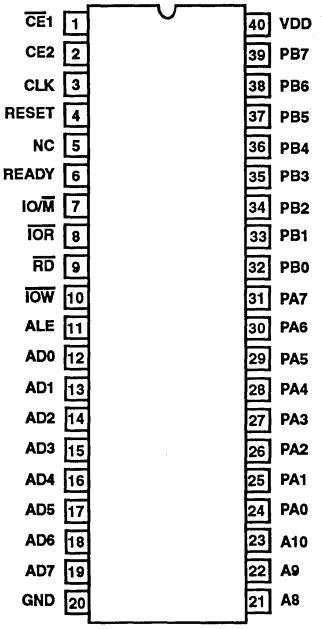
The HS-83C55RH is a radiation hardened ROM and I/O chip fabricated using the Harris radiation hardened Self-Aligned Junction Isolated (SAJI) silicon gate technology. Latch-up free operation is achieved by the use of epitaxial starting material to eliminate the parasitic SCR effect seen in conventional bulk CMOS devices.

The HS-83C55RH is intended for use with the HS-80C85RH radiation hardened microprocessor system.

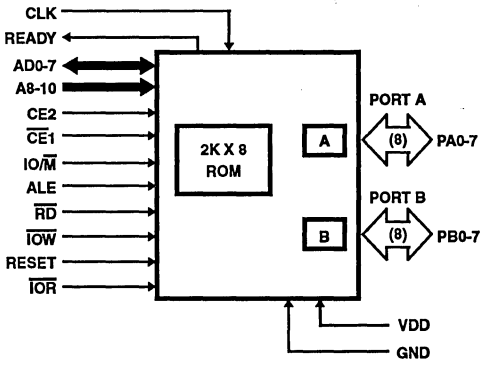
The ROM portion is designed as 16,384 mask programmable cells organized in a 2048 word x 8-bit format. A maximum post irradiation access time of 340ns allows the HS-83C55RH to be used with the HS-80C85RH CPU without any wait states. This ROM is designed for operation utilizing a single 5 volt power supply.

Pinout

HS-83C55RH 40 LEAD BRAZE SEAL DIP
COMPLIANT OUTLINE D5, CONFIGURATION 3
TOP VIEW



Block Diagram



11 µPROCESSOR PERIPHERALS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3045

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
ALE	11	I	Address Latch Enable: When high, AD0-7, IO/$\overline{M}$, A8-0, CE2, and $\overline{CE1}$, enter the address latches. The signals (AD, IO/$\overline{M}$, A8-10, CE2, CE1) are latched in at the trailing edge of ALE.*
AD0-7	12-19	I	Address/Data Bus (Bidirectional): The lower 8-bits of the ROM or I/O address are applied to the bus lines when ALE is high. During an I/O cycle, Port A or B is selected based on the latched value of AD0. If $\overline{RD}$ or $\overline{IOR}$ is low when the latched chip enables are active, the output buffers present data on the bus.
A8-10	21, 22, 23	I	Address Bus: High order bits of the ROM address. They do not affect I/O operations.
$\overline{CE1}$,CE2	1, 2	I	Chip Enable Inputs: $\overline{CE1}$ is active low and CE2 is active high.The HS-83C55RH can be accessed only when BOTH Chip Enables are active at the time the ALE signal latches them In. If either Chip Enable input is not active, the AD0-7 and READY outputs will be in a high impedance state.
IO/$\overline{M}$	7	I	I/O Memory: If the latched IO/$\overline{M}$ is high when $\overline{RD}$ is low, the output data comes from an I/O port. If it is low, the output data comes from the ROM.
$\overline{RD}$	9	I	Read: If the latched Chip Enables are active when $\overline{RD}$ goes low, the AD0-7 output buffers are enabled and output either the selected ROM location or I/O port. When both $\overline{RD}$ and $\overline{IOR}$ are high, the AD0-7 output buffers are 3-stated.
$\overline{IOW}$	10	I	I/O Write: If the latched Chip Enables are active, a low on $\overline{IOW}$ causes the output port pointed to by the latched value of AD0 to be written with the data on AD0-7. The state of IO/$\overline{M}$ is ignored.
CLK	3	I	Clock: Used to force the READY into its high impedance state after it has been forced low by $\overline{CE1}$, low, CE2 high and ALE high.
READY	6	O	READY: A 3-state output controlled by $\overline{CE1}$, CE2, ALE and CLK. READY is forced low when the Chip Enables are active during the time ALE is high, and remains low until the rising edge of the next CLK.
PA0-7	24-31	I/O	Port A: General purpose I/O pins. Their input/output direction is determined by the contents of the Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active and $\overline{IOW}$ is low and a 0 was previously latched from AD0, AD1. Read operation is selected by either $\overline{IOR}$ low and active Chip Enables and AD0 and AD1 low, or IO/$\overline{M}$ high, RD low, active chip enables, and AD0 and AD1, LOW.
PB0-7	32-39	I/O	Port B: This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD0 and a 0 from AD1.
RESET	4	I	Reset: An input high causes all pins in Port A and B to assume input-mode. (Clear DDR Register.)
$\overline{IOR}$	8	I	I/O Read: When the Chip Enables are active, a low on $\overline{IOR}$ will output the selected I/O port onto the AD bus. $\overline{IOR}$ low performs the same function as the combination IO/$\overline{M}$ high and $\overline{RD}$ low. When $\overline{IOR}$ is not used in a system, $\overline{IOR}$ should be tied to VCC.
VDD	40	I	Voltage: +5 Volt
GND	20	I	Ground: Ground Reference.

* ALE must be clocked once after power up.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage ..... GND-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 1.5mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	25.8°C/W	9.9°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package 1.94W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.75V to +5.25V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... VDD -0.5V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

All Devices are Guaranteed at Worst Case Limits and Over Radiation. Dynamic Current is Proportional to Operating Frequency.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current	IIH	VDD = 5.25V, VIN = 0V Pin Under Test = VDD	1, 2, 3	-55°C, +25°C, or +125°C	-	1.0	µA
	IIL	VDD = 5.25V, VIN = 5.25V Pin Under Test = 0V	1, 2, 3	-55°C, +25°C, or +125°C	-1.0	-	µA
High Level Output Voltage	VOH	VDD = 4.75V, IOH = -2.0mA	1, 2, 3	-55°C, +25°C, or +125°C	4.25	-	V
Low Level Output Voltage	VOL	VDD = 5.25V, IOL = 2.0mA,	1, 2, 3	-55°C, +25°C, or +125°C	-	0.5	V
Output Leakage Current	IOZL	VDD = 5.25V, VIN = 0V	1, 2, 3	-55°C, +25°C, or +125°C	-10	-	µA
	IOZH	VDD = 5.25V, VIN = 5.25V	1, 2, 3	-55°C, +25°C, or +125°C	-	10	µA
Static Current	IDDSB	VDD = 5.25V	1, 2, 3	-55°C, +25°C, or +125°C	-	100	µA
Dynamic Current	IDDOP	VDD = 5.25V, f = 1MHz	1, 2, 3	-55°C, +25°C, or +125°C	-	5.0	mA/MHz
Functional Tests	FT	VDD = 4.75V and 5.25V, VIH = VDD - 0.5, VIL = 0.8V	7, 8A, 8B	-55°C, +25°C, or +125°C	-	-	-

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

AC Tests are Guaranteed Through Functional Testing with the Clock Period Equal to 500ns. TRDE + TRDF are the Only Read and Record Parameters. Output Timings are Measured with a Capacitive Load CL = 170pF, VIH = 4.25, and VIL = 0.8V

PARAMETERS	SYMBOL	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Data Bus Float After Read	TRDF	9, 10, 11	-55°C, +25°C, +125°C	0	110	ns
Read Control to Data Bus Enable	TRDE	9, 10, 11	-55°C, +25°C, +125°C	10	-	ns
Clock Pulse Width Low	T1	9, 10, 11	-55°C, +25°C, +125°C	40	-	ns
Clock Pulse Width High	T2	9, 10, 11	-55°C, +25°C, +125°C	70	-	ns
Clock Rise and Fall Times	TR, TF	9, 10, 11	-55°C, +25°C, +125°C	-	100	ns
Address to Latch Setup Time	TAL	9, 10, 11	-55°C, +25°C, +125°C	60	-	ns
Address Hold Time After Latch	TLA	9, 10, 11	-55°C, +25°C, +125°C	60	-	ns
Latch to Read/Write Control	TLC	9, 10, 11	-55°C, +25°C, +125°C	140	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

AC Tests are Guaranteed Through Functional Testing with the Clock Period Equal to 500ns. TRDE + TRDF are the Only Read and Record Parameters. Output Timings are Measured with a Capacitive Load CL = 170pF, VIH = 4.25, and VIL = 0.8V

PARAMETERS	SYMBOL	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Valid Out Delay from Read Control (Note 1)	TRD	9, 10, 11	-55°C, +25°C, +125°C	-	140	ns
Address Stable to Data Out Valid (Note 2)	TAD	9, 10, 11	-55°C, +25°C, +125°C	-	340	ns
Latch Enable Width	TLL	9, 10, 11	-55°C, +25°C, +125°C	120	-	ns
Read/Write Control of Latch Enable	TCL	9, 10, 11	-55°C, +25°C, +125°C	40	-	ns
Read/Write Control Width	TCC	9, 10, 11	-55°C, +25°C, +125°C	200	-	ns
Data In to Write Setup Time	TDW	9, 10, 11	-55°C, +25°C, +125°C	150	-	ns
Data In Hold Time After Write	TWD	9, 10, 11	-55°C, +25°C, +125°C	10	-	ns
Write to Port Output	TWP	9, 10, 11	-55°C, +25°C, +125°C	-	300	ns
Port Input Setup Time	TPR	9, 10, 11	-55°C, +25°C, +125°C	50	-	ns
Port Input Hold Time	TRP	9, 10, 11	-55°C, +25°C, +125°C	50	-	ns
Ready Hold Time	TRYH	9, 10, 11	-55°C, +25°C, +125°C	0	160	ns
Address CE to Ready	TARY	9, 10, 11	-55°C, +25°C, +125°C	-	160	ns
Recovery Time Between Controls	TRV	9, 10, 11	-55°C, +25°C, +125°C	300	-	ns

NOTES:

1. Or TAD - (TAL + TLC), whichever is greater.
2. Defines ALE to Data Out Valid in conjunction with TAL.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Input Capacitance	CIN	VDD = Open, f = 1MHz	T_A = +25°C	-	10	pF
I/O Capacitance	CI/O	VDD = Open, f = 1MHz	T_A = +25°C	-	12	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz	T_A = +25°C	-	10	pF

NOTE:

1. All measurements referenced to device ground.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

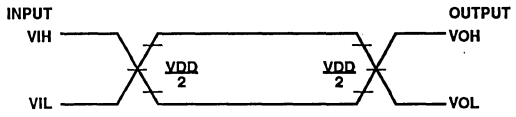
NOTE: The post irradiation test conditions and limits are the same as those listed in Table 1 and 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

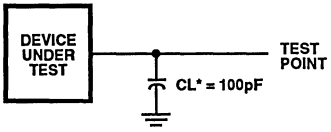
PARAMETER	SYMBOL	DELTA LIMITS
Output Low Voltage	VOL	± 60mV
Output High Voltage	VOH	± 400mV
Input Leakage Current	IIL	± 100nA
Input Leakage Current	IIH	± 100nA
Static Current	IDDSB	±30µA

A.C. Testing Input, Output Waveform

INPUT/OUTPUT



A.C. Testing Load Circuit (Note 1)



A.C. TESTING: All input signals must switch between VIL max and VIH min, tr and tf must be less than or equal to 15ns.

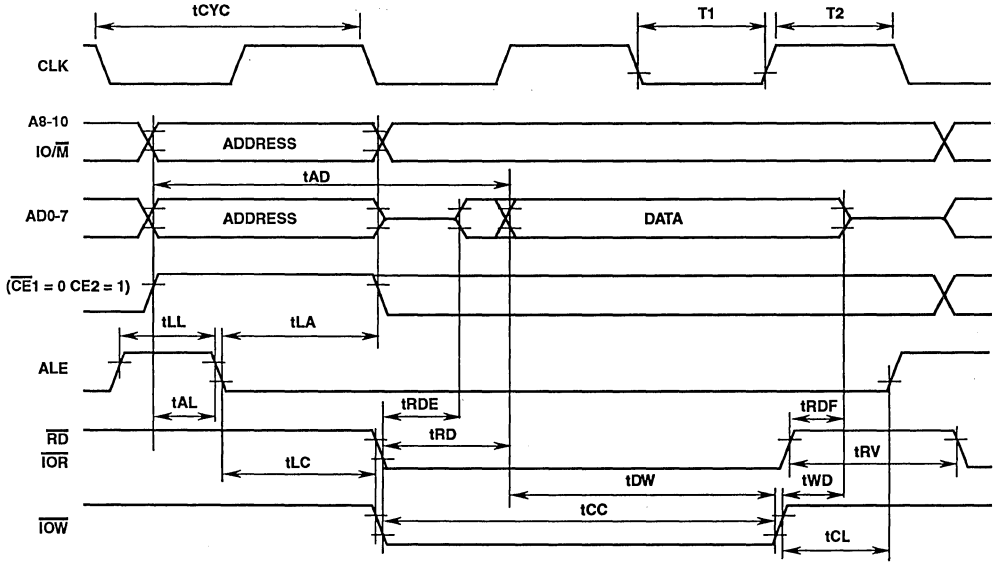
* CL includes stray and jig capacitance.

NOTES:

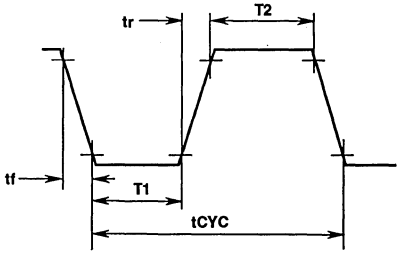
1. Output timings are measured with purely capacitive load.
2. Devices screened to more rigorous electrical specifiecations are available. Contact your nearest Harris representative for details.

Waveforms

ROM READ AND I/O READ AND WRITE

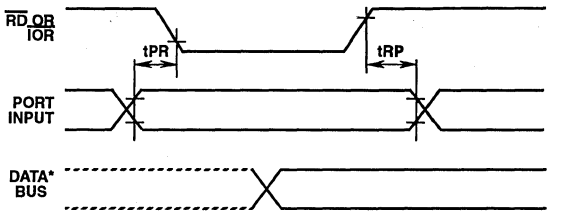


83C55RH CLOCK SPECIFICATIONS



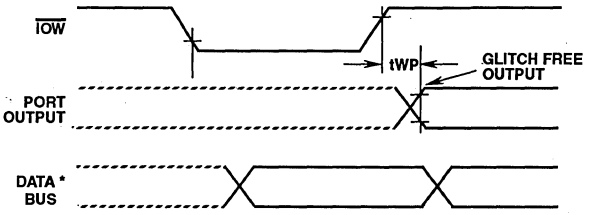
Waveforms (Continued)

INPUT MODE



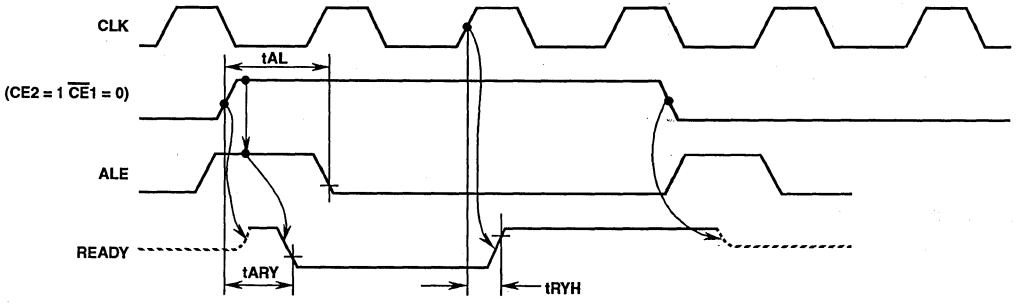
* DATA BUS TIMING IS SHOWN IN FIGURE 4.

OUTPUT MODE



* DATA BUS TIMING IS SHOWN IN FIGURE 4.

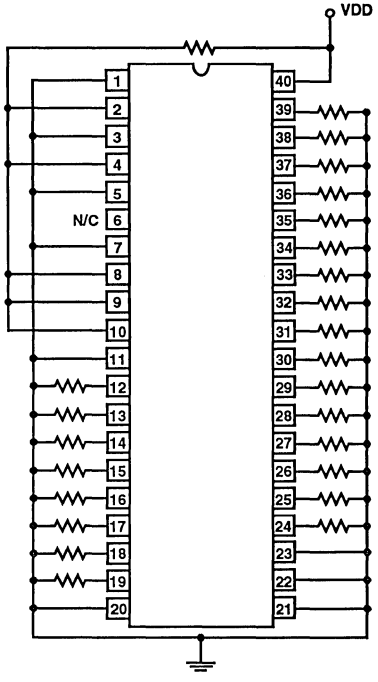
WAIT STATE



NOTE: READY = 0

Burn-In Circuits

HS-83C55RH 40 PIN DIP

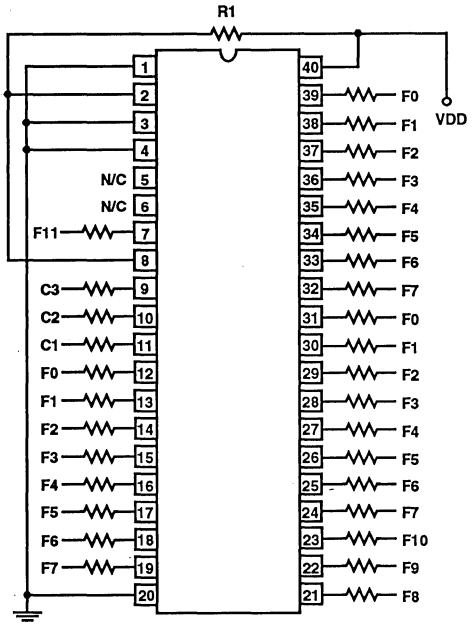


STATIC

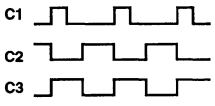
NOTES:

VDD = 10V ± 10%
16K ROM
T_A Min = 125°C
All Resistors are 10kΩ ± 10%, 1.4 Watt
Part is static sensitive. Voltage must be ramped.

HS-83C55RH 40 PIN DIP



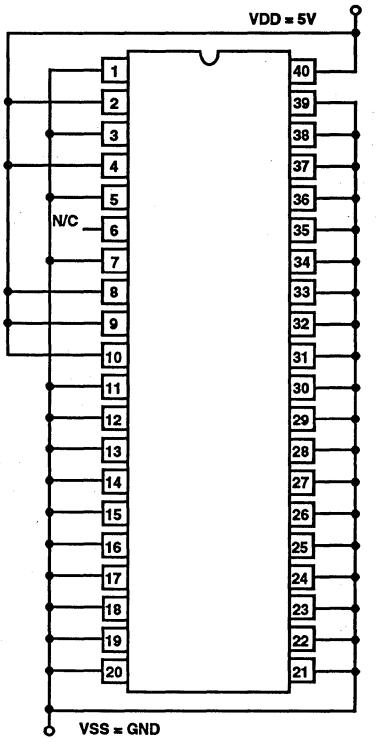
DYNAMIC



NOTES:

VDD = 10V ± 10%
16K ROM
$T_A = \overline{125}$°C
C2 = $\overline{C3}$
R1 = 100KΩ ± 10%, 1/4 Watt.
All other resistors 10KΩ ± 10%, 1/4 Watt.
Part is static sensitive. Voltage must be ramped.
C2 thru C3 = 200kHz and have 50% duty cycles.
C1 = 200kHz and have 20% duty cycle.
F0 = 100kHz, F1 = F0/2, F2 = F1/2 . . . F11 = F10/2
Frequencies Fn defined by: Fn = F(n-1)/2 where F0 = 100kHz e.g. F1 = 50kHz, F2 = 25kHz . . . All Fn's have 50% duty cycle.
Part is static sensitive.

Irradiation Circuit



Radiation Screening Procedure

1. A random sample of two dice per wafer is drawn from the wafer lot. Wafer identity is retained.
2. The sample die shall be assembled and tested for functionality in a ceramic DIP.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1×10^5 Rad(Si) +10% from a Gammacell 220 cobalt 60 source or equivalent. The devices will be powered with VSUPPLY = +5V. The dose rate shall be between 50 rads/sec and 300 rads/sec.
4. The Irradiation Circuit is shown on a previous page.
5. The sample devices shall be started into test within 1 hour of irradiation and have completed test within 2 hours of irradiation. The wafers are accepted only if the sample, exclusive of non-radiation failures, meets all electrical specifications at room temperature.
6. Radiation screening to a higher total dose is available. Customers should contact their closest Harris Representative for details.

Radiation Effects

The HS-83C55RH has been designed to survive in a radiation environment and to meet the electrical characteristics. Latch-up free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained with special low temperature processing cycles. On a production basis, Harris performs screens for total dose hardness to a level of 1×10^5 Rad-Si. Transient radiation tests have shown the following results:

1. Latch-up free to doses $\geq 1 \times 10^{12}$ rads/sec.
2. Upset (loss of stored data $\geq 1 \times 10^8$ rads/sec.

Harris - Space Level Product Flow -Q (Note 1)

SEM - Traceable to Diffusion Method 2018

Wafer Lot Acceptance Method 5007

Internal Visual Inspection Method 2010, Condition A

Gamma Radiation Assurance Tests Method 1019

Nondestructive Bond Pull Method 2023

Customer Pre-Cap Visual Inspection (Note 2)

Temperature Cycling Method 1010, Condition C

Constant Acceleration Method 2001, Condition E Min, Y1

Particle Impact Noise Detection Method 2020, Condition A

Electrical Tests Harris' Option

Serialization

X-Ray Inspection Method 2012

Electrical Tests Subgroup 1; Read and Record (TO)

Static Burn-In Method 1015, Condition B, 72 Hours, +125°C Minimum

Electrical Tests Subgroup 1; Read and Record (T1)

Burn-In Delta Calculation (T0-T1)

PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ

Dynamic Burn-In Method 1015 Condition D, 240 Hours, +125°C (Note 3)

Electrical Tests Subgroup 1; Read and Record (T2)

Alternate Group A Subgroups 1, 7, 9; Method 5005; Para 3.5.1.1

Burn-In Delta Calculation (TO-T2)

PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ

Electrical Test Subgroup 3; Read and Record

Alternate Group A Subgroups 3, 8B, 11; Method 5005; Para 3.5.1.1

Marking

Electrical Tests Subgroup 2; Read and Record

Alternate Group A Subgroups 2, 8A, 10; Method 5005; Para 3.5.1.1

Gross Leak Method 1014, 100%

Fine Leak Method 1014, 100%

Customer Source Inspection (Note 2)

Group B Inspection Method 5005 (Note 2)
End-Point Electrical Parameters:
B-5/ Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11

B-6; Subgroups 1, 7, 9

Group D Inspection Method 5005 (Notes 2, 4)
End-Point Electrical Parameters: Subgroups 1, 7, 9

External Visual Inspection Method 2009

Data Package Generation (Note 5)

NOTES:

1. The notes of Method 5004, Table 1 Shall apply; unless otherwise specified.
2. These steps are optional and should be listed on the individual purchase order(s), when required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table 1 of Method 1015
4. For group D, subgroup 3 inspection of package configurations which utilize a gold plated lid in its construction; the inspection criteria for illegible markings criteria of Method 1010, paragraph 3.3 and of Method 1004, paragraph 3.8.a shall not apply.
5. Data package contains:
   Assembly attributes (Post Seal)
   Test attributes (includes Group A)
   Shippable serial number list
   Radiation testing certificate of conformance
   Wafer lot acceptance report (including SEM report)
   X-ray report and film
   Test variables data

Metallization Topology

DIE DIMENSIONS:
179.1 x 189.0 x 14 ± 1mils

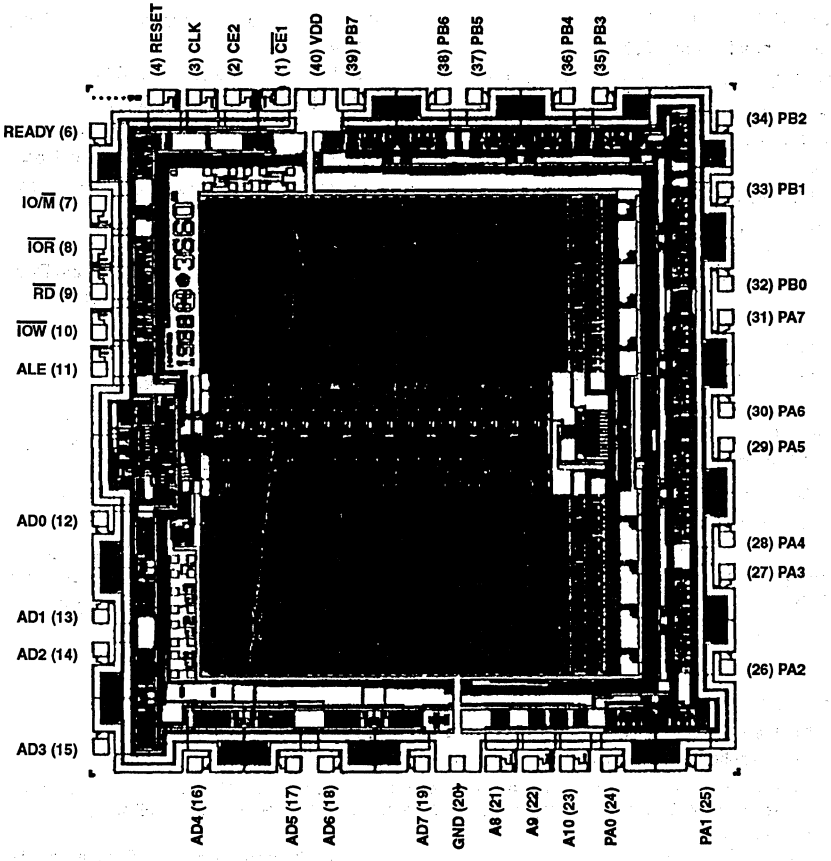
METALLIZATION:
Type: Si Al
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP - 460°C (Max)

Metallization Mask Layout

HS-83C55RH



Functional Description

ROM Section

The HS-83C55RH contains an 8-bit address latch which allows it to interface directly to the HS-80C85RH Microprocessor without additional hardware.

The ROM section of the Chip is addressed by an 11-bit address and the Chip Enables. The address and levels on the Chip Enable pins are latched into the address latches on the falling edge of ALE. If the latched Chip Enables are active and IO/$\overline{M}$ is low when $\overline{RD}$ goes low, the contents of the ROM location addressed by the latched address are put out through AD0-7 output buffers.

I/O Section

The I/O section of the chip is addressed by the latched value of AD0-1. Two 8-bit Data Direction Registers (DDR) in the HS-83C55RH determine the input/output status of each pin in the corresponding ports. A "0" in a particular bit position of a DDR signifies that the corresponding I/O port bit is in the input mode. A "1" in a particular bit position signifies that the corresponding I/O port bit is in the output mode. In this manner the I/O ports of the HS-83C55RH are bit-by-bit programmable as inputs or outputs. The table summarizes port and DDR designation. DDR's Cannot be read.

AD1	AD0	Selection
0	0	Port A
0	1	Port B
1	0	Port A Data Direction Register (DDR A)
1	1	Port B Data Direction Register (DDR B)

When $\overline{IOW}$ goes low and the Chip Enables are active, the data on the AD0-7 is written into the I/O port selected by the latched value of AD0-1. During this operation all I/O bits of selected port are affected, regardless of their I/O mode and the state of IO/$\overline{M}$. The actual output level does not change until $\overline{IOW}$ returns high (glitch free output). A port can be read out when the latched Chip Enables are active and either $\overline{RD}$ goes low with IO/$\overline{M}$ high, or $\overline{IOR}$ goes low. Both input and output mode bits of a selected port will appear on lines AD0-7.

To clarify the function of the I/O ports and Data Direction Registers, Figure 1 shows the configuration of one bit of PORT A and DDR A. The same logic applies to PORT B and DDR B.

Note that hardware RESET or writing a zero to the DDR latch will cause the output latch's output buffer to be disabled, preventing the data in the output latch from being passed through to the pin. This is equivalent to putting the port in the input mode. Note also that the data can be written to the Output Latch even though the Output Buffer has been disabled. This enables a port to be initialized with a value prior to enabling the output.

Figure 1 also shows that the contents of PORT A and PORT B can be read even when the ports are configured as outputs.

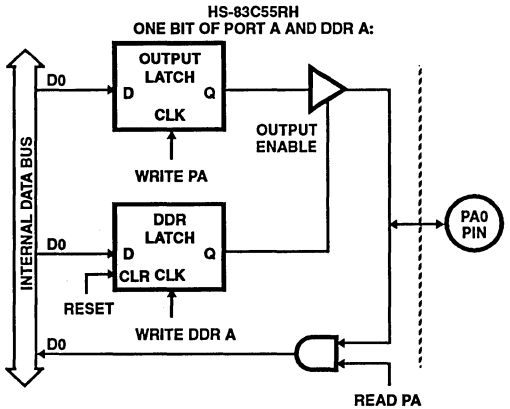
System Interface with HS-8OC85RH

A system using the HS-83C55RH can use either one of the two I/O Interface techniques:

- Standard I/O
- Memory Mapped I/O

If a standard I/O technique is used, the system can use the feature of both CE2 and $\overline{CE}$1. By using a combination of unused address lines A11-15 and the Chip Enable inputs, the system can use up to 5 each HS-83C55RHs without requiring a CE decoder. See Figure 3.

If a memory mapped I/O approach is used the HS-83C55RH will be selected by the combination of both the Chip Enables and IO/M using AD8-15 address lines. See Figure 2.



Write PA = ($\overline{IOW}$ = 0) (Chip Enables Active) (Port A Address Selected)
Write DDR A = ($\overline{IOW}$ = 0) (Chip Enables Active) (DDR A Address Selected)
Read PA = [[(IO/$\overline{M}$ = 1) ($\overline{RD}$ = 0)] + ($\overline{IOR}$ = 0)] (Chip Enables Active) (Port A Address Selected)

NOTE: Write PA is not qualified by IO/$\overline{M}$.

FIGURE 1. HS-83C55RH ONE BIT OF PORT A AND DDR A

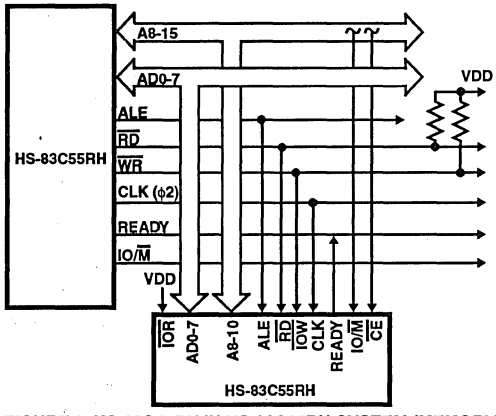
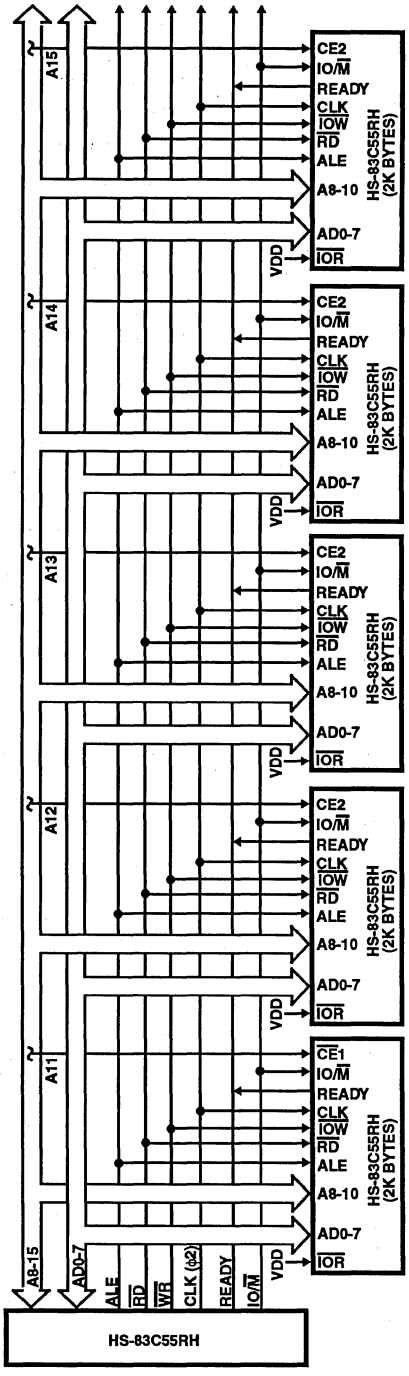


FIGURE 2. HS-83C55RH IN HS-80C85RH SYSTEM (MEMORY\-MAPPED I/O)



NOTE: Use $\overline{CE}1$, for the first HS-83C55RH in the system, and CE2 for the other HS-83C55RH's. Permits up Is 5 HS-83C55RH's in a system without CE decoder.

FIGURE 3. HS-83C55RH IN HS-8OC85RH SYSTEM (STANDARD I/O)

RAD HARD 12

TRANSISTORS

TRANSISTORS (Continued)

Radiation Hardened MOSFET Nomenclature System

FR X XXXX X X

HARRIS RADIATION HARDENED POWER MOSFET

PACKAGE DESIGNATION

M - TO-204AA (TO-3 with 40 mil diameter leads)
K - TO-204AE (TO-3 with 60 mil diameter leads)
L - TO-205AF (TO-39)
F - TO-254AA
S - TO-257AA
E - TO-258AA

DIE DESIGNATION

All Numeric Characters
N-Channel (Three Digits) - XXX
P-Channel (Four Digits) - 9XXX

RADIATION (TOTAL DOSE) ASSURANCE LEVEL

D - 10kRAD (Si)
R - 100kRAD (Si)
H - 1000kRAD (Si)

RELIABILITY SCREENING LEVEL

1 - Non-TX (Commerical)
2 - TX Equivalent of MIL-S-19500
3 - TXV Equivalent of MIL-S-19500
4 - Space Equivalent of MIL-S-19500

Tactical and Strategic Level Selections*

Radiation Hardened MOSFETs (N-Channel)

DIE FAMILY	TO-3		TO-39		TO-254		TO-257		TO-258	
	INTERIM	FINAL	INTERIM	FINAL	INTERIM	FINAL	INTERIM	FINAL	INTERIM	FINAL
17631	FRM130D FRM130R FRM130H	2N7271	FRL130D FRL130R FRL130H	2N7272	- - -	-	FRS130D FRS130R FRS130H	2N7273	- - -	-
17632	FRM230D FRM230R FRM230H	2N7274	FRL230D FRL230R FRL230H	2N7275	- - -	-	FRS230D FRS230R FRS230H	2N7276	- - -	-
17633	FRM234D FRM234R FRM234H	2N7277	FRL234D FRL234R FRL234H	2N7278	- - -	-	FRS234D FRS234R FRS234H	2N7279	- - -	-
17635	FRM430D FRM430R FRM430H	2N7280	FRL430D FRL430R FRL430H	2N7281	- - -	-	FRS430D FRS430R FRS430H	2N7282	- - -	-
17641	FRM140D FRM140R FRM140H	2N7283	- - -	-	- - -	-	FRS140D FRS140R FRS140H	2N7284	- - -	-
17642	FRM240D FRM240R FRM240H	2N7285	- - -	-	- - -	-	FRS240D FRS240R FRS240H	2N7286	- - -	-
17643	FRM244D FRM244R FRM244H	2N7287	- - -	-	- - -	-	FRS244D FRS244R FRS244H	2N7288	- - -	-
17645	FRM440D FRM440R FRM440H	2N7289	- - -	-	- - -	-	FRS440D FRS440R FRS440H	2N7290	- - -	-
17651	FRK150D FRK150R FRK150H	2N7291	- - -	-	FRF150D FRF150R FRF150H	2N7292	- - -	-	- - -	-
17652	FRK250D FRK250R FRK250H	2N7293	- - -	-	FRF250D FRF250R FRF250H	2N7294	- - -	-	- - -	-
17653	FRK254D FRK254R FRK254H	2N7295	- - -	-	FRF254D FRF254R FRF254H	2N7296	- - -	-	- - -	-
17655	FRM450D FRM450R FRM450H	2N7297	- - -	-	FRF450D FRF450R FRF450H	2N7298	- - -	-	- - -	-
17661	FRK160D FRK160R FRK160H	2N7299	- - -	-	- - -	-	- - -	-	FRE160D FRE160R FRE160H	2N7300
17662	FRK260D FRK260R FRK260H	2N7301	- - -	-	- - -	-	- - -	-	FRE260D FRE260R FRE260H	2N7302
17663	FRK264D FRK264R FRK264H	2N7303	- - -	-	- - -	-	- - -	-	FRE264D FRE264R FRE264H	2N7304
17665	FRK460D FRK460R FRK460H	2N7305	- - -	-	- - -	-	- - -	-	FRE460D FRE460R FRE460H	2N7306

* The reliability screening code has been omitted for convenience.

Radiation Hardened MOSFETs (P-Channel)

DIE FAMILY	TO-3		TO-39		TO-254		TO-257		TO-258	
	INTERIM	FINAL	INTERIM	FINAL	INTERIM	FINAL	INTERIM	FINAL	INTERIM	FINAL
17731	FRM9130D FRM9130R FRM9130H	2N7307	FRL9130D FRL9130R FRL9130H	2N7308	- - -	-	FRS9130D FRS9130R FRS9130H	2N7309	- - -	-
17732	FRM9230D FRM9230R FRM9230H	2N7310	FRL9230D FRL9230R FRL9230H	2N7311	- - -	-	FRS9230D FRS9230R FRS9230H	2N7312	- - -	-
17741	FRM9140D FRM9140R FRM9140H	2N7316	- - -	-	- - -	-	FRS9140D FRS9140R FRS9140H	2N7317	- - -	-
17742	FRM9240D FRM9240R FRM9240H	2N7318	- - -	-	- - -	-	FRS9240D FRS9240R FRS9240H	2N7319	- - -	-
17751	FRK9150D FRK9150R FRK9150H	2N7322	- - -	-	FRF9150D FRF9150R FRF9150H	2N7323	- - -	-	- - -	-
17752	FRM9250D FRM9250R FRM9250H	2N7324	- - -	-	FRF9250D FRF9250R FRF9250H	2N7325	- - -	-	- - -	-
17761	FRK9160D FRK9160R FRK9160H	2N7328	- - -	-	-	-	- - -	-	FRE9160D FRE9160R FRE9160H	2N7329
17762	FRK9260D FRK9260R FRK9260H	2N7330	- - -	-	-	-	- - -	-	FRE9260D FRE9260R FRE9260H	2N7331

* The reliability screening code has been omitted for convenience.

Radiation Hardened Power MOSFETs

N-Channel

RATED BVDSS	TYPE NUMBER	PACKAGE OUTLINE (TO-)	INITIAL RATINGS			POST 10K RAD OR POST 100K RAD (SI) RATINGS			POST 1M RAD (SI) RATINGS		
			Id (A)	RDS(on) (Ω)	VGS(th) (V)	BVDSS (V)	RDS(on) (Ω)	VGS(th) (V)	BVDSS (V)	RDS(on) (Ω)	VGS(th) (V)
100	2N7271	204AA	14	0.180	2 - 4	100	0.180	2 - 4	95	0.270	1.5 - 4.5
	2N7272	205AF	8	0.180	2 - 4	100	0.180	2 - 4	95	0.270	1.5 - 4.5
	2N7273	257AA	12	0.195	2 - 4	100	0.195	2 - 4	95	0.293	1.5 - 4.5
	2N7283	204AA	23	0.130	2 - 4	100	0.130	2 - 4	95	0.200	1.5 - 4.5
	2N7284	257AA	17	0.145	2 - 4	100	0.145	2 - 4	95	0.218	1.5 - 4.5
	2N7291	204AE	40	0.055	2 - 4	100	0.055	2 - 4	95	0.083	1.5 - 4.5
	2N7292	254AA	25	0.070	2 - 4	100	0.070	2 - 4	95	0.105	1.5 - 4.5
	2N7299	204AE	50	0.040	2 - 4	100	0.040	2 - 4	95	0.060	1.5 - 4.5
	2N7300	258	41	0.050	2 - 4	100	0.050	2 - 4	95	0.075	1.5 - 4.5
200	2N7274	204AA	8	0.500	2 - 4	200	0.500	2 - 4	190	0.750	1.5 - 4.5
	2N7275	205AF	5	0.500	2 - 4	200	0.500	2 - 4	190	0.750	1.5 - 4.5
	2N7276	257AA	7	0.515	2 - 4	200	0.515	2 - 4	190	0.773	1.5 - 4.5
	2N7285	204AA	16	0.240	2 - 4	200	0.240	2 - 4	190	0.360	1.5 - 4.5
	2N7286	257AA	12	0.255	2 - 4	200	0.255	2 - 4	190	0.383	1.5 - 4.5
	2N7293	204AE	27	0.100	2 - 4	200	0.100	2 - 4	190	0.140	1.5 - 4.5
	2N7294	254AA	23	0.115	2 - 4	200	0.115	2 - 4	190	0.161	1.5 - 4.5
	2N7301	204AE	46	0.070	2 - 4	200	0.070	2 - 4	190	0.105	1.5 - 4.5
	2N7302	258	31	0.080	2 - 4	200	0.080	2 - 4	190	0.120	1.5 - 4.5
250	2N7277	204AA	7	0.700	2 - 4	250	0.700	2 - 4	238	1.000	1.5 - 4.5
	2N7278	205AF	4	0.700	2 - 4	250	0.700	2 - 4	238	1.000	1.5 - 4.5
	2N7279	257AA	5	0.715	2 - 4	250	0.715	2 - 4	238	1.070	1.5 - 4.5
	2N7287	204AA	12	0.400	2 - 4	250	0.400	2 - 4	238	0.600	1.5 - 4.5
	2N7288	257AA	9	0.415	2 - 4	250	0.415	2 - 4	238	0.623	1.5 - 4.5
	2N7295	204AE	20	0.170	2 - 4	250	0.170	2 - 4	238	0.215	1.5 - 4.5
	2N7296	254AA	17	0.185	2 - 4	250	0.185	2 - 4	238	0.234	1.5 - 4.5
	2N7303	204AE	34	0.120	2 - 4	250	0.120	2 - 4	238	0.180	1.5 - 4.5
	2N7304	258	23	0.130	2 - 4	250	0.130	2 - 4	238	0.195	1.5 - 4.5
500	2N7280	204AA	3	2.500	2 - 4	500	2.500	2 - 4	475	3.750	1.5 - 4.5
	2N7281	205AF	2	2.500	2 - 4	500	2.500	2 - 4	475	3.750	1.5 - 4.5
	2N7282	257AA	3	2.520	2 - 4	500	2.520	2 - 4	475	3.780	1.5 - 4.5
	2N7289	204AA	6	1.400	2 - 4	500	1.400	2 - 4	475	2.100	1.5 - 4.5
	2N7290	257AA	5	1.420	2 - 4	500	1.420	2 - 4	475	2.130	1.5 - 4.5
	2N7297	204AA	10	0.600	2 - 4	500	0.600	2 - 4	475	0.860	1.5 - 4.5
	2N7298	254AA	9	0.615	2 - 4	500	0.615	2 - 4	475	0.879	1.5 - 4.5
	2N7305	204AE	17	0.400	2 - 4	500	0.400	2 - 4	475	0.600	1.5 - 4.5
	2N7306	258	12	0.410	2 - 4	500	0.410	2 - 4	475	0.615	1.5 - 4.5

Radiation Hardened Power MOSFETs

P-Channel

RATED BVDSS	TYPE NUMBER	PACKAGE OUTLINE (TO-)	INITIAL RATINGS			POST 10K RAD OR POST 100K RAD (Si) RATINGS			POST 1M RAD (Si) RATINGS		
			Id (A)	RDS(on) (W)	VGS(th) (V)	BVDSS (V)	RDS(on) (W)	VGS(th) (V)	BVDSS (V)	RDS(on) (W)	VGS(th) (V)
100	2N7307	204AA	6	0.550	2 - 4	100	0.550	2 - 4	95	0.830	2 - 6
	2N7308	205AF	5	0.550	2 - 4	100	0.550	2 - 4	95	0.830	2 - 6
	2N7309	257AA	6	0.565	2 - 4	100	0.565	2 - 4	95	0.848	2 - 6
	2N7316	204AA	11	0.300	2 - 4	100	0.300	2 - 4	95	0.450	2 - 6
	2N7317	257AA	11	0.315	2 - 4	100	0.315	2 - 4	95	0.473	2 - 6
	2N7322	204AE	26	0.125	2 - 4	100	0.125	2 - 4	95	0.188	2 - 6
	2N7323	254AA	23	0.140	2 - 4	100	0.140	2 - 4	95	0.210	2 - 6
	2N7328	204AE	40	0.085	2 - 4	100	0.085	2 - 4	95	0.128	2 - 6
	2N7329	258	30	0.095	2 - 4	100	0.095	2 - 4	95	0.143	2 - 6
200	2N7310	204AA	4	1.300	2 - 4	200	1.300	2 - 4	190	1.950	2 - 6
	2N7311	205AF	3	1.300	2 - 4	200	1.300	2 - 4	190	1.950	2 - 6
	2N7312	257AA	4	1.320	2 - 4	200	1.320	2 - 4	190	1.980	2 - 6
	2N7318	204AA	7	0.720	2 - 4	200	0.720	2 - 4	190	1.080	2 - 6
	2N7319	257AA	7	0.735	2 - 4	200	0.735	2 - 4	190	1.100	2 - 6
	2N7324	204AA	16	0.300	2 - 4	200	0.300	2 - 4	190	0.450	2 - 6
	2N7325	254AA	14	0.315	2 - 4	200	0.315	2 - 4	190	0.473	2 - 6
	2N7330	204AE	26	0.200	2 - 4	200	0.200	2 - 4	190	0.300	2 - 6
	2N7331	258	19	0.210	2 - 4	200	0.210	2 - 4	190	0.315	2 - 6

HARRIS SEMICONDUCTOR

2N7271D, 2N7271R 2N7271H

REGISTRATION PENDING
Currently Available as FRM130 (D, R, H)
December 1992

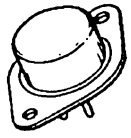
Radiation Hardened N-Channel Power MOSFETs

Features

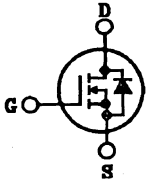
- 14A, 100V, RDS(on) = 0.180Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 1.5nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E13 Neutrons/cm^2
  - Usable to 3E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Package

TO-204AA



Symbol



Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7271D, R, H	UNITS
Drain-Source Voltage	VDS	100	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	100	V
Continuous Drain Current			
TC = +25°C	ID	14	A
TC = +100°C	ID	9	A
Pulsed Drain Current	IDM	42	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	75	W
TC = +100°C	PT	30	W
Derated Above +25°C		0.60	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	42	A
Continuous Source Current (Body Diode)	IS	14	A
Pulsed Source Current (Body Diode)	ISM	42	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3217**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	100	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 100V, VGS = 0 VDS = 80V, VGS = 0 VDS = 80V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	42	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 14A	-	2.65	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 9A	-	.18	Ω
Turn-On Delay Time	td(on)	VDD = 50V, ID = 14A	-	30	ns
Rise Time	tr	Pulse Width = 3µs	-	218	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	156	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	144	
Gate-Charge Threshold	QG(th)	VDD = 50V, ID = 14A IGS1 = IGS2 0 ≤ VGS ≤ 20	1	4	nc
Gate-Charge On State	QG(on)		18	74	
Gate-Charge Total	QGM		36	146	
Plateau Voltage	VGP		3	14	V
Gate-Charge Source	QGS		3	14	nc
Gate-Charge Drain	QGD		9	36	
Diode Forward Voltage	VSD	ID = 14A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 14A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	Rθjc		-	1.67	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	60	

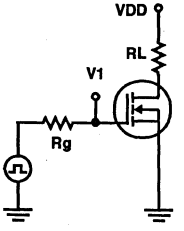


FIGURE 1. SWITCHING TIME TESTING

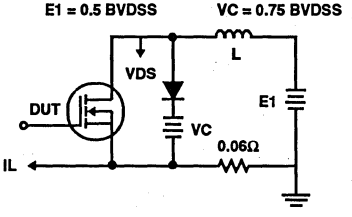


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

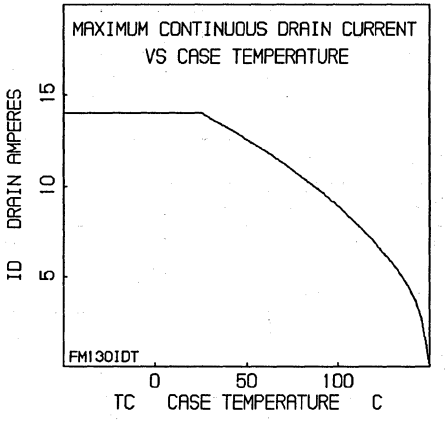
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

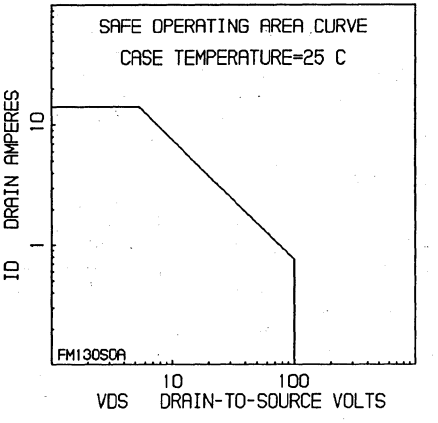
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7271D, R	VGS = 0, ID = 1mA	100	-	V
	(Note 5, 6)	BVDSS	2N7271H	VGS = 0, ID = 1mA	95	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7271D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7271H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7271D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7271H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7271D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7271H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7271D, R	VGS = 0, VDS = 80V	-	25	μA
	(Note 5, 6)	IDSS	2N7271H	VGS = 0, VDS = 80V	-	100	μA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7271D, R	VGS = 10V, ID = 14A	-	2.65	V
	(Note 1, 5, 6)	VDS(on)	2N7271H	VGS = 16V, ID = 14A	-	3.97	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7271D, R	VGS = 10V, ID = 9A	-	0.180	Ω
	(Note 1, 5, 6)	RDS(on)	2N7271H	VGS = 14V, ID = 9A	-	0.270	Ω

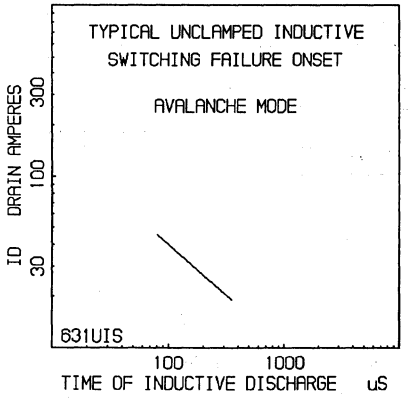
NOTES:

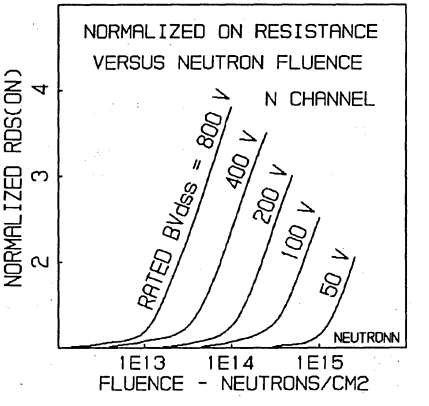
1. Pulse test, 300μs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 3E13
5. Gamma = 1000KRAD(Si). Neutron = 3E13
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 4/17/90 on TA 17631 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

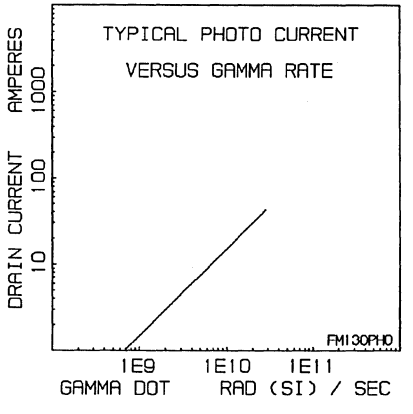
Typical Performance Characteristics

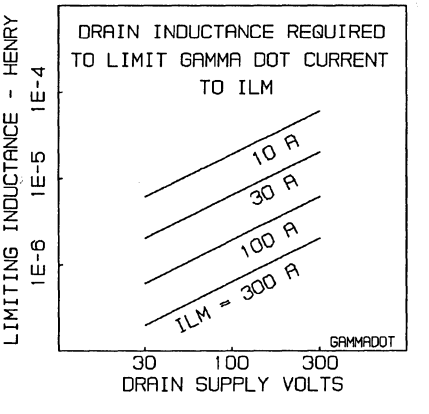












HARRIS SEMICONDUCTOR

2N7272D, 2N7272R 2N7272H

REGISTRATION PENDING
Currently Available as FRL130 (D, R, H)
December 1992

Radiation Hardened N-Channel Power MOSFETs

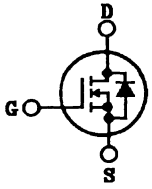
Features

- 8A, 100V, RDS(on) = 0.180Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 1.5nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E13 Neutrons/cm^2
  - Usable to 3E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Package

TO-205AF

Symbol



Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7272D, R, H	UNITS
Drain-Source Voltage	VDS	100	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	100	V
Continuous Drain Current			
TC = +25°C	ID	8	A
TC = +100°C	ID	5	A
Pulsed Drain Current	IDM	24	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	25	W
TC = +100°C	PT	10	W
Derated Above +25°C		0.20	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	24	A
Continuous Source Current (Body Diode)	IS	8	A
Pulsed Source Current (Body Diode)	ISM	24	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3218**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	100	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 100V, VGS = 0 VDS = 80V, VGS = 0 VDS = 80V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	24	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 8A	-	1.51	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 5A	-	.180	Ω
Turn-On Delay Time	td(on)	VDD = 50V, ID = 8A	-	35	ns
Rise Time	tr	Pulse Width = 3µs	-	210	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	200	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	145	
Gate-Charge Threshold	QG(th)	VDD = 50V, ID = 8A IGS1 = IGS2 0 ≤ VGS ≤ 20	1	4	nc
Gate-Charge On State	QG(on)		19	76	
Gate-Charge Total	QGM		35	142	
Plateau Voltage	VGP		3	12	V
Gate-Charge Source	QGS		3	13	nc
Gate-Charge Drain	QGD		9	38	
Diode Forward Voltage	VSD	ID = 8A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 8A; di/dt = 100A/µs	-	450	ns
Junction-To-Case	Rθjc		-	5.0	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	175	

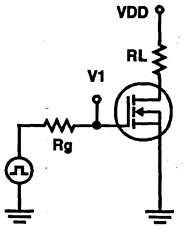


FIGURE 1. SWITCHING TIME TESTING

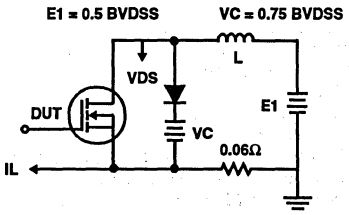


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

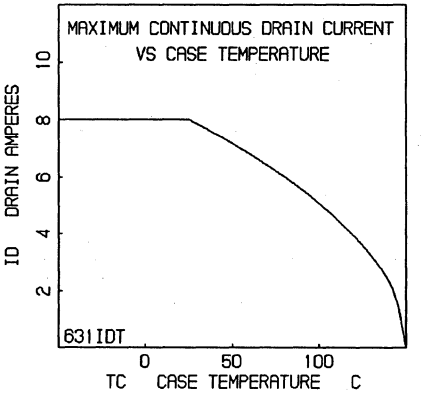
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

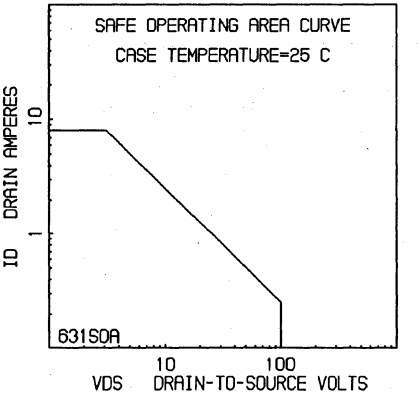
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7272D, R	VGS = 0, ID = 1mA	100	-	V
	(Note 5, 6)	BVDSS	2N7272H	VGS = 0, ID = 1mA	95	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7272D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7272H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7272D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7272H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7272D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7272H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7272D, R	VGS = 0, VDS = 80V	-	25	µA
	(Note 5, 6)	IDSS	2N7272H	VGS = 0, VDS = 80V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7272D, R	VGS = 10V, ID = 8A	-	1.51	V
	(Note 1, 5, 6)	VDS(on)	2N7272H	VGS = 16V, ID = 8A	-	2.27	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7272D, R	VGS = 10V, ID = 5A	-	0.180	Ω
	(Note 1, 5, 6)	RDS(on)	2N7272H	VGS = 14V, ID = 5A	-	0.270	Ω

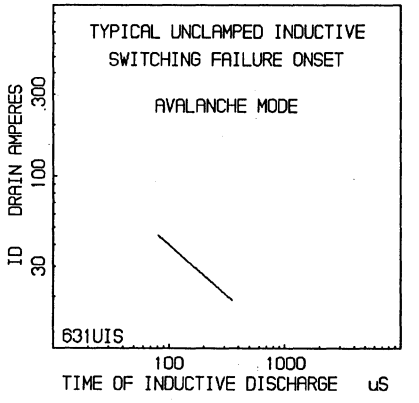
NOTES:

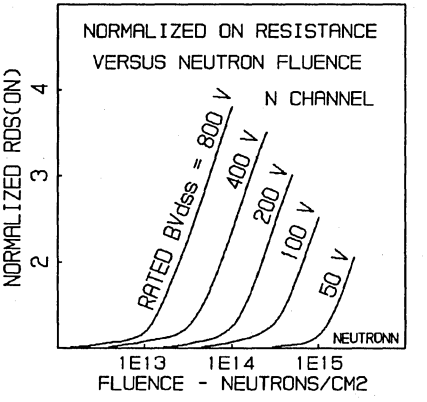
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 3E13
5. Gamma = 1000KRAD(Si). Neutron = 3E13
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 4/19/90 on TA 17631 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

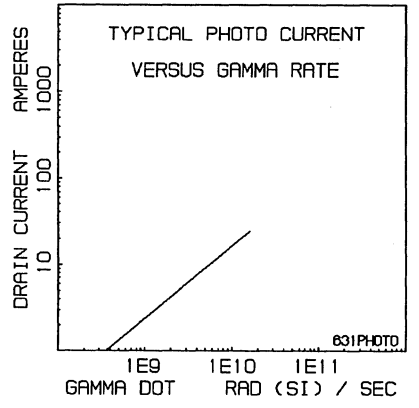
Typical Performance Characteristics

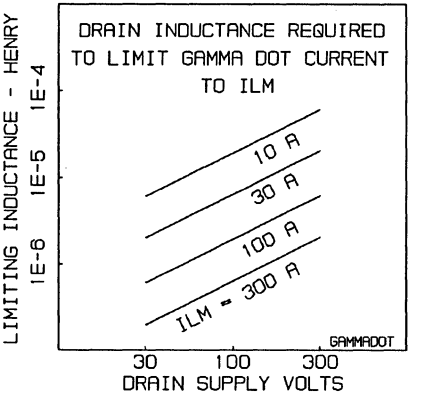












HARRIS SEMICONDUCTOR

2N7273D, 2N7273R 2N7273H

REGISTRATION PENDING
Currently Available as FRS130 (D, R, H)
January 1993

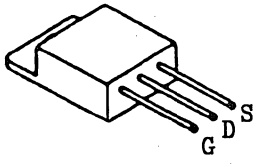
Radiation Hardened N-Channel Power MOSFETs

Features

- 12A, 100V, RDS(on) = 0.195Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 1.5nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E13 Neutrons/cm^2
  - Usable to 3E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Package

TO-257AA



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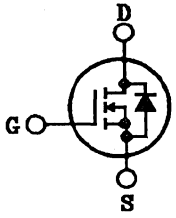


Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7273D, R, H	UNITS
Drain-Source Voltage	VDS	100	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	100	V
Continuous Drain Current			
TC = +25°C	ID	12	A
TC = +100°C	ID	7	A
Pulsed Drain Current	IDM	36	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	50	W
TC = +100°C	PT	20	W
Derated Above +25°C		0.40	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	36	A
Continuous Source Current (Body Diode)	IS	12	A
Pulsed Source Current (Body Diode)	ISM	36	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3219**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	100	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 100V, VGS = 0 VDS = 80V, VGS = 0 VDS = 80V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	36	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 12A	-	2.46	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 7A	-	0.195	Ω
Turn-On Delay Time	td(on)	VDD = 50V, ID = 12A	-	44	ns
Rise Time	tr	Pulse Width = 3µs	-	428	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	128	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	108	
Gate-Charge Threshold	QG(th)		1	4	nc
Gate-Charge On State	QG(on)		18	72	
Gate-Charge Total	QGM	VDD = 50V, ID = 12A	33	134	
Plateau Voltage	VGP	IGS1 = IGS2 0 ≤ VGS ≤ 20	3	14	V
Gate-Charge Source	QGS		3	14	nc
Gate-Charge Drain	QGD		9	38	
Diode Forward Voltage	VSD	ID = 12A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 12A; di/dt = 100A/µs	-	600	ns
Junction-To-Case	Rθjc		-	2.5	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	60	

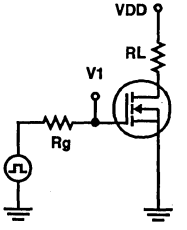


FIGURE 1. SWITCHING TIME TESTING

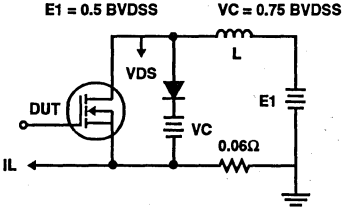


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

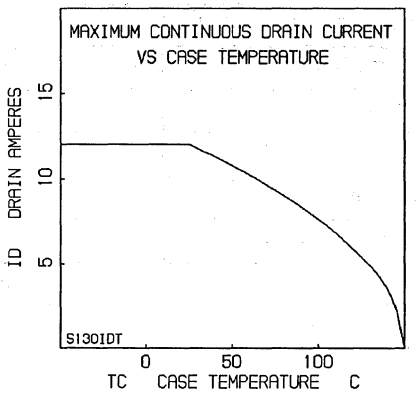
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

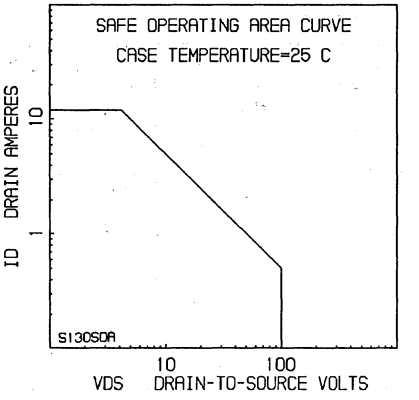
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7273D, R	VGS = 0, ID = 1mA	100	-	V
	(Note 5, 6)	BVDSS	2N7273H	VGS = 0, ID = 1mA	95	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7273D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7273H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7273D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7273H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7273D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7273H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7273D, R	VGS = 0, VDS = 80V	-	25	μA
	(Note 5, 6)	IDSS	2N7273H	VGS = 0, VDS = 80V	-	100	μA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7273D, R	VGS = 10V, ID = 12A	-	2.46	V
	(Note 1, 5, 6)	VDS(on)	2N7273H	VGS = 16V, ID = 12A	-	3.69	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7273D, R	VGS = 10V, ID = 7A	-	0.195	Ω
	(Note 1, 5, 6)	RDS(on)	2N7273H	VGS = 14V, ID = 7A	-	0.293	Ω

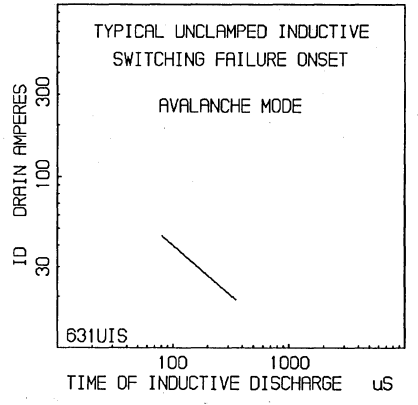
NOTES:

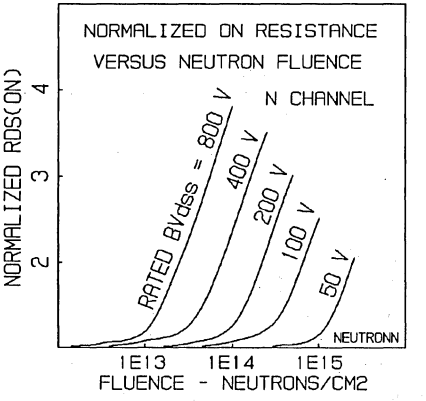
1. Pulse test, 300μs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 3E13
5. Gamma = 1000KRAD(Si). Neutron = 3E13
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 4/17/90 on TA 17631 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

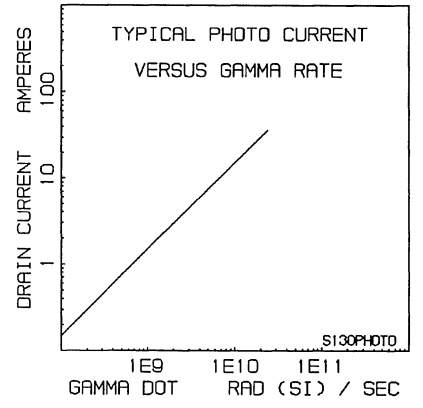
Typical Performance Characteristics

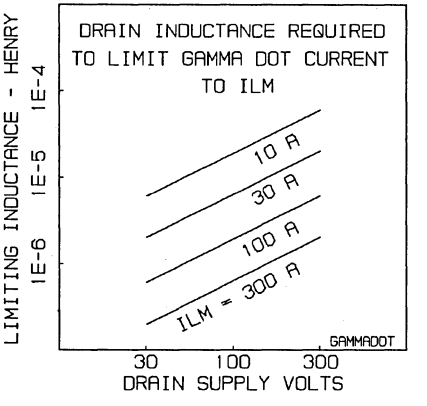












HARRIS SEMICONDUCTOR

2N7274D, 2N7274R 2N7274H

REGISTRATION PENDING
Currently Available as FRM230 (D, R, H)
December 1992

Radiation Hardened N-Channel Power MOSFETs

Features

- 8A, 200V, RDS(on) = 0.50Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 3.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

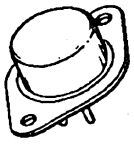
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

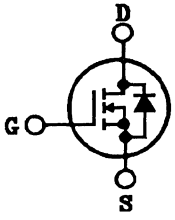
This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-204AA



Symbol



Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7274D, R, H	UNITS
Drain-Source Voltage	VDS	200	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	200	V
Continuous Drain Current			
TC = +25°C	ID	8	A
TC = +100°C	ID	5	A
Pulsed Drain Current	IDM	24	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	75	W
TC = +100°C	PT	30	W
Derated Above +25°C		0.60	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	24	A
Continuous Source Current (Body Diode)	IS	8	A
Pulsed Source Current (Body Diode)	ISM	24	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3249**

HARRIS SEMICONDUCTOR

2N7275D, 2N7275R 2N7275H

REGISTRATION PENDING
Currently Available as FRL230 (D, R, H)
December 1992

Radiation Hardened N-Channel Power MOSFETs

Features

- 5A, 200V, RDS(on) = 0.500Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 3.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

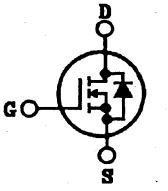
This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-205AF

Symbol



Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7275D, R, H	UNITS
Drain-Source Voltage	VDS	200	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	200	V
Continuous Drain Current			
TC = +25°C	ID	5	A
TC = +100°C	ID	3	A
Pulsed Drain Current	IDM	15	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	25	W
TC = +100°C	PT	10	W
Derated Above +25°C		0.20	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	15	A
Continuous Source Current (Body Diode)	IS	5	A
Pulsed Source Current (Body Diode)	ISM	15	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3223**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	200	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 200V, VGS = 0 VDS = 160V, VGS = 0 VDS = 160V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	15	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 5A	-	2.63	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 3A	-	0.500	Ω
Turn-On Delay Time	td(on)	VDD = 100V, ID = 5A	-	34	ns
Rise Time	tr	Pulse Width = 3µs	-	140	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	172	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	80	
Gate-Charge Threshold	QG(th)	VDD = 100V, ID = 5A IGS1 = IGS2 0 ≤ VGS ≤ 20	1	3	nc
Gate-Charge On State	QG(on)		15	60	
Gate-Charge Total	QGM		30	120	
Plateau Voltage	VGP		3	13	V
Gate-Charge Source	QGS		3	12	nc
Gate-Charge Drain	QGD		7	29	
Diode Forward Voltage	VSD	ID = 5A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 5A; di/dt = 100A/µs	-	600	ns
Junction-To-Case	Rθjc		-	5.0	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	175	

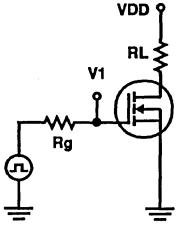


FIGURE 1. SWITCHING TIME TESTING

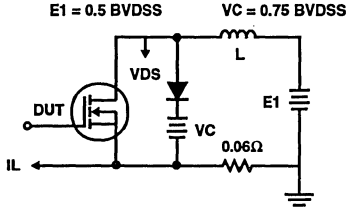


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

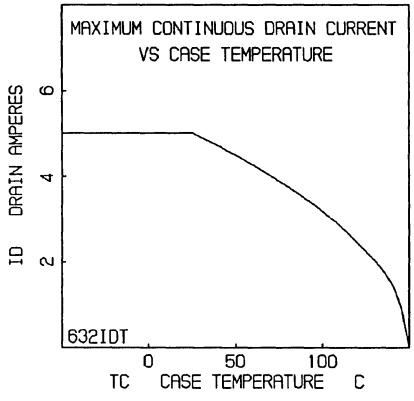
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

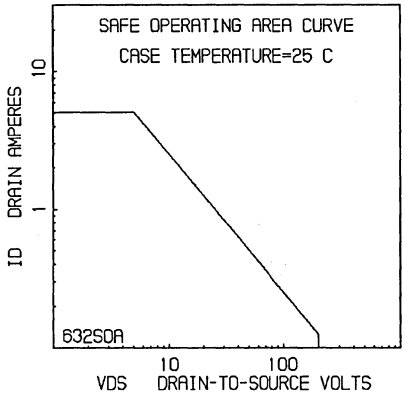
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7275D, R	VGS = 0, ID = 1mA	200	-	V
	(Note 5, 6)	BVDSS	2N7275H	VGS = 0, ID = 1mA	190	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7275D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7275H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7275D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7275H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7275D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7275H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7275D, R	VGS = 0, VDS = 160V	-	25	µA
	(Note 5, 6)	IDSS	2N7275H	VGS = 0, VDS = 160V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7275D, R	VGS = 10V, ID = 5A	-	2.63	V
	(Note 1, 5, 6)	VDS(on)	2N7275H	VGS = 16V, ID = 5A	-	3.94	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7275D, R	VGS = 10V, ID = 3A	-	0.500	Ω
	(Note 1, 5, 6)	RDS(on)	2N7275H	VGS = 14V, ID = 3A	-	0.750	Ω

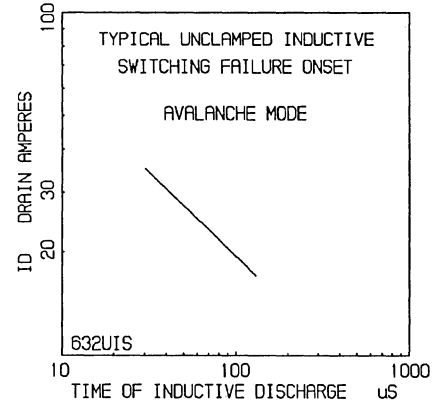
NOTES:

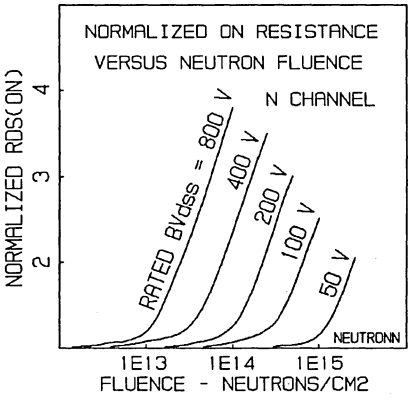
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 1E13
5. Gamma = 1000KRAD(Si). Neutron = 1E13
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 3/03/90 on TA 17632 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

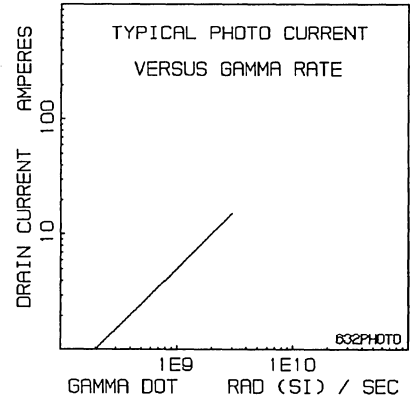
Typical Performance Characteristics

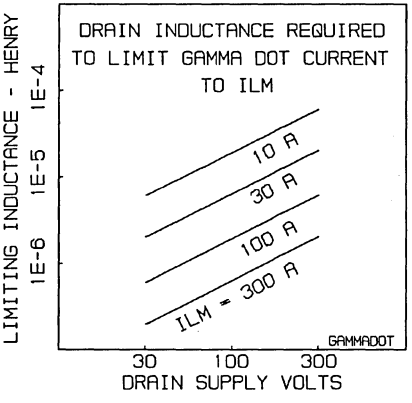












HARRIS SEMICONDUCTOR

2N7276D, 2N7276R 2N7276H

REGISTRATION PENDING
Currently Available as FRS230(D, R, H)

December 1992

Radiation Hardened N-Channel Power MOSFETs

Features

- 7A, 200V, RDS(on) = 0.515Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 3.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

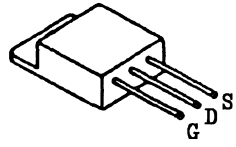
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n^0) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

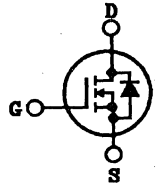
This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-257AA



Symbol



Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7276D, R, H	UNITS
Drain-Source Voltage	VDS	200	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	200	V
Continuous Drain Current			
TC = +25°C	ID	7	A
TC = +100°C	ID	4	A
Pulsed Drain Current	IDM	21	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	50	W
TC = +100°C	PT	20	W
Derated Above +25°C		0.40	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	21	A
Continuous Source Current (Body Diode)	IS	7	A
Pulsed Source Current (Body Diode)	ISM	21	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3224**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	200	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 200V, VGS = 0 VDS = 160V, VGS = 0 VDS = 160V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	21	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 7A	-	3.79	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 4A	-	0.515	Ω
Turn-On Delay Time	td(on)	VDD = 100V, ID = 7A	-	42	ns
Rise Time	tr	Pulse Width = 3µs	-	214	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	152	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	66	
Gate-Charge Threshold	QG(th)	VDD = 100V, ID = 7A IGS1 = IGS2 0 ≤ VGS ≤ 20	1	4	nc
Gate-Charge On State	QG(on)		17	68	
Gate-Charge Total	QGM		30	122	
Plateau Voltage	VGP		3	13	V
Gate-Charge Source	QGS		3	13	nc
Gate-Charge Drain	QGD		8	34	
Diode Forward Voltage	VSD	ID = 7A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 7A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	Rθjc		-	2.5	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	60	

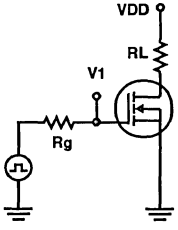


FIGURE 1. SWITCHING TIME TESTING

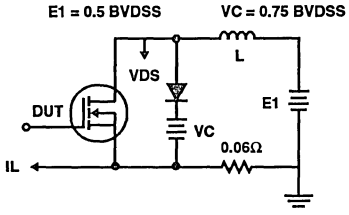


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

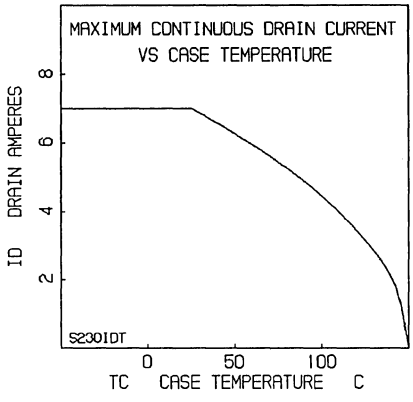
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

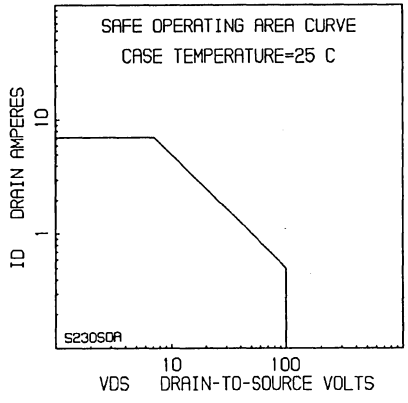
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7276D, R	VGS = 0, ID = 1mA	200	-	V
	(Note 5, 6)	BVDSS	2N7276H	VGS = 0, ID = 1mA	190	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7276D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7276H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7276D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7276H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7276D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7276H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7276D, R	VGS = 0, VDS = 160V	-	25	µA
	(Note 5, 6)	IDSS	2N7276H	VGS = 0, VDS = 160V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7276D, R	VGS = 10V, ID = 7A	-	3.79	V
	(Note 1, 5, 6)	VDS(on)	2N7276H	VGS = 16V, ID = 7A	-	5.69	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7276D, R	VGS = 10V, ID = 4A	-	0.515	Ω
	(Note 1, 5, 6)	RDS(on)	2N7276H	VGS = 14V, ID = 4A	-	0.773	Ω

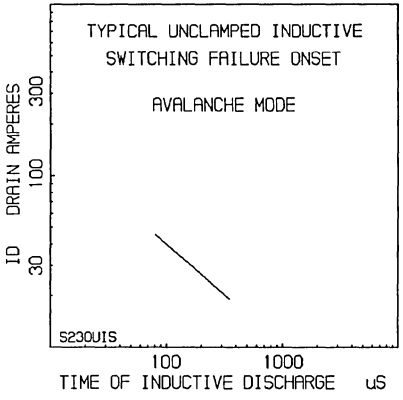
NOTES:

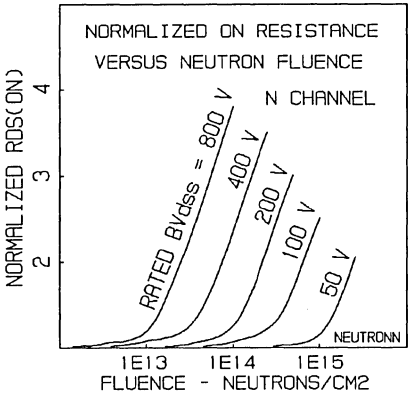
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 1E13
5. Gamma = 1000KRAD(Si). Neutron = 1E13
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 3/03/90 on TA 17632 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

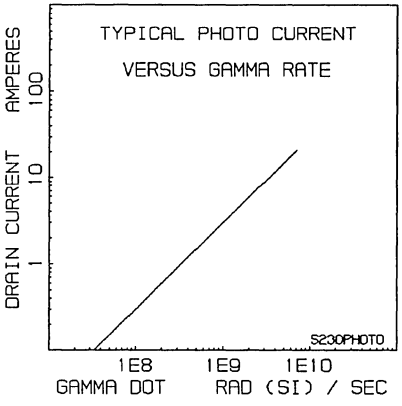
Typical Performance Characteristics

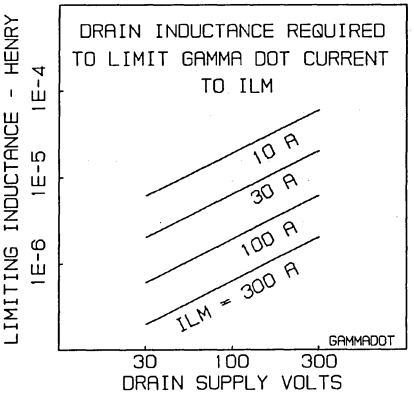












HARRIS SEMICONDUCTOR

2N7277D, 2N7277R 2N7277H

REGISTRATION PENDING
Currently Available as FRM234(D, R, H)
December 1992

Radiation Hardened N-Channel Power MOSFETs

Features

- 7A, 250V, RDS(on) = 0.70Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 4.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

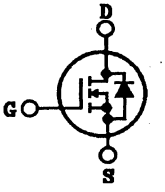
This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-204AA

Symbol



Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7277D, R, H	UNITS
Drain-Source Voltage	VDS	250	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	250	V
Continuous Drain Current			
TC = +25°C	ID	7	A
TC = +100°C	ID	4	A
Pulsed Drain Current	IDM	21	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	75	W
TC = +100°C	PT	30	W
Derated Above +25°C		0.60	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	21	A
Continuous Source Current (Body Diode)	IS	7	A
Pulsed Source Current (Body Diode)	ISM	21	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3250**

HARRIS SEMICONDUCTOR

2N7278D, 2N7278R 2N7278H

REGISTRATION PENDING
Currently Available as FRL234(D, R, H)
December 1992

Radiation Hardened N-Channel Power MOSFETs

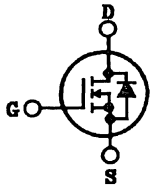
Features

- 4A, 250V, RDS(on) = 0.700Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 4.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Package

TO-205AF

Symbol



Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7278D, R, H	UNITS
Drain-Source Voltage	VDS	250	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	250	V
Continuous Drain Current			
TC = +25°C	ID	4	A
TC = +100°C	ID	2	A
Pulsed Drain Current	IDM	12	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	25	W
TC = +100°C	PT	10	W
Derated Above +25°C		0.20	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	12	A
Continuous Source Current (Body Diode)	IS	4	A
Pulsed Source Current (Body Diode)	ISM	12	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3229**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	250	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 250V, VGS = 0 VDS = 200V, VGS = 0 VDS = 200V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	12	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 4A	-	2.94	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 2A	-	0.70	Ω
Turn-On Delay Time	td(on)	VDD = 125V, ID = 4A	-	35	ns
Rise Time	tr	Pulse Width = 3µs	-	85	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	195	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	75	
Gate-Charge Threshold	QG(th)		1	4	nc
Gate-Charge On State	QG(on)		15	62	
Gate-Charge Total	QGM	VDD = 125V, ID = 4A	30	120	
Plateau Voltage	VGP	IGS1 = IGS2	3	12	V
Gate-Charge Source	QGS	0 ≤ VGS ≤ 20	3	12	nc
Gate-Charge Drain	QGD		7	30	
Diode Forward Voltage	VSD	ID = 4A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 4A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	Rθjc		-	5.0	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	175	

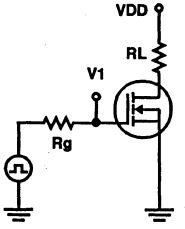


FIGURE 1. SWITCHING TIME TESTING

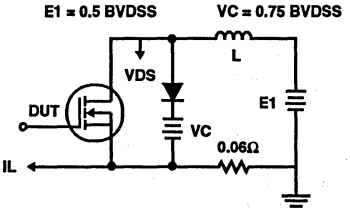


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

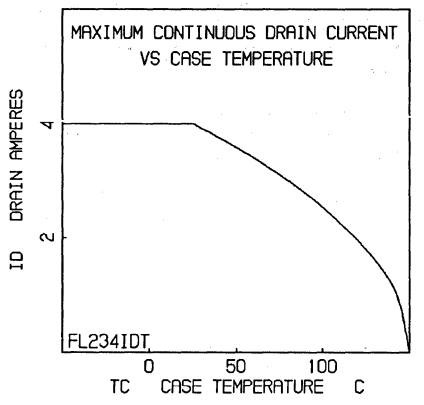
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

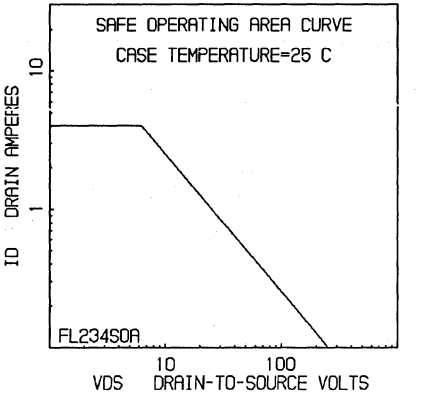
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7278D, R	VGS = 0, ID = 1mA	250	-	V
	(Note 5, 6)	BVDSS	2N7278H	VGS = 0, ID = 1mA	238	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7278D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7278H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7278D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7278H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7278D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7278H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7278D, R	VGS = 0, VDS = 200V	-	25	µA
	(Note 5, 6)	IDSS	2N7278H	VGS = 0, VDS = 200V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7278D, R	VGS = 10V, ID = 4A	-	2.94	V
	(Note 1, 5, 6)	VDS(on)	2N7278H	VGS = 16V, ID = 4A	-	4.20	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7278D, R	VGS = 10V, ID = 2A	-	0.700	Ω
	(Note 1, 5, 6)	RDS(on)	2N7278H	VGS = 14V, ID = 2A	-	1.0	Ω

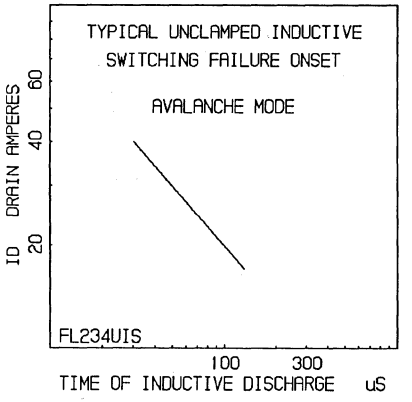
NOTES:

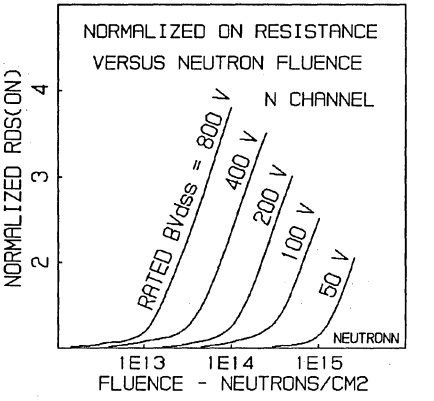
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 1E13
5. Gamma = 1000KRAD(Si). Neutron = 1E13
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 1/19/90 on TA 17633 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

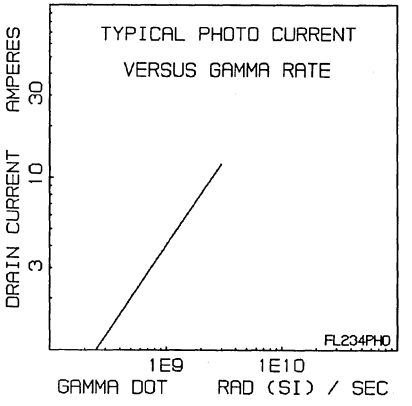
Typical Performance Characteristics

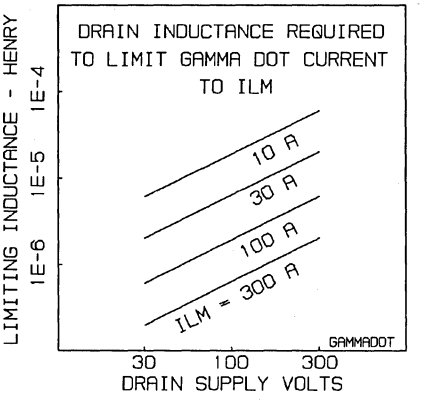












HARRIS SEMICONDUCTOR

2N7279D, 2N7279R 2N7279H

REGISTRATION PENDING
Currently Available as FRS234 (D, R, H)
December 1992

Radiation Hardened N-Channel Power MOSFETs

Features

- 5A, 250V, RDS(on) = 0.715Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 4.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

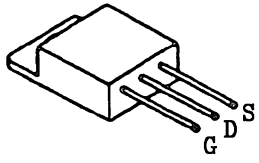
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-257AA



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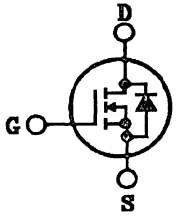


Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7279D, R, H	UNITS
Drain-Source Voltage	VDS	250	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	250	V
Continuous Drain Current			
TC = +25°C	ID	5	A
TC = +100°C	ID	3	A
Pulsed Drain Current	IDM	15	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	50	W
TC = +100°C	PT	20	W
Derated Above +25°C		0.40	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	15	A
Continuous Source Current (Body Diode)	IS	5	A
Pulsed Source Current (Body Diode)	ISM	15	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3251**

HARRIS SEMICONDUCTOR

2N7280D, 2N7280R 2N7280H

REGISTRATION PENDING
Currently Available as FRM430 (D, R, H)
December 1992

Radiation Hardened N-Channel Power MOSFETs

Features

- 3A, 500V, RDS(on) = 2.50Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 8.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E12 Neutrons/cm^2
  - Usable to 3E13 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25MΩ Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

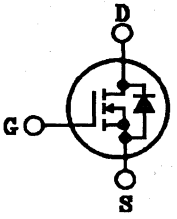
This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-204AA

Symbol



Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7280D, R, H	UNITS
Drain-Source Voltage	VDS	500	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	500	V
Continuous Drain Current			
TC = +25°C	ID	3	A
TC = +100°C	ID	2	A
Pulsed Drain Current	IDM	9	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	75	W
TC = +100°C	PT	30	W
Derated Above +25°C		0.60	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	9	A
Continuous Source Current (Body Diode)	IS	3	A
Pulsed Source Current (Body Diode)	ISM	9	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3252**

HARRIS SEMICONDUCTOR

2N7281D, 2N7281R 2N7281H

REGISTRATION PENDING
Currently Available as FRL430(D, R, H)
December 1992

Radiation Hardened N-Channel Power MOSFETs

Features

- 2A, 500V, RDS(on) = 2.50Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 8.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E12 Neutrons/cm^2
  - Usable to 3E13 Neutrons/cm^2
- Single Event - Typically Survives 1E5ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

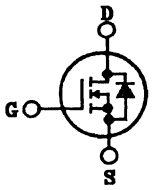
This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-205AF

Symbol



Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7281D, R, H	UNITS
Drain-Source Voltage	VDS	500	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	500	V
Continuous Drain Current			
TC = +25°C	ID	2	A
TC = +100°C	ID	1	A
Pulsed Drain Current	IDM	6	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	25	W
TC = +100°C	PT	10	W
Derated Above +25°C		0.20	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	6	A
Continuous Source Current (Body Diode)	IS	2	A
Pulsed Source Current (Body Diode)	ISM	6	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3234**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	500	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 500V, VGS = 0 VDS = 400V, VGS = 0 VDS = 400V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	6	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 2A	-	5.25	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 1A	-	2.50	Ω
Turn-On Delay Time	td(on)	VDD = 250V, ID = 2A	-	46	ns
Rise Time	tr	Pulse Width = 3µs	-	58	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	208	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	54	
Gate-Charge Threshold	QG(th)	VDD = 250V, ID = 2A IGS1 = IGS2 0 ≤ VGS ≤ 20	1	4	nc
Gate-Charge On State	QG(on)		15	64	
Gate-Charge Total	QGM		32	130	
Plateau Voltage	VGP		3	14	V
Gate-Charge Source	QGS		3	12	nc
Gate-Charge Drain	QGD		8	32	
Diode Forward Voltage	VSD	ID = 2A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 2A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	RθJC		-	5.0	°C/W
Junction-To-Ambient	RθJA	Free Air Operation	-	175	

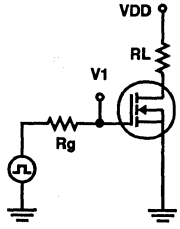


FIGURE 1. SWITCHING TIME TESTING

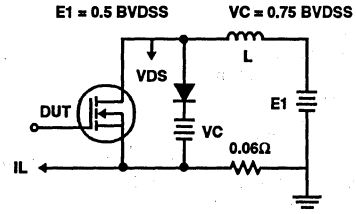


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

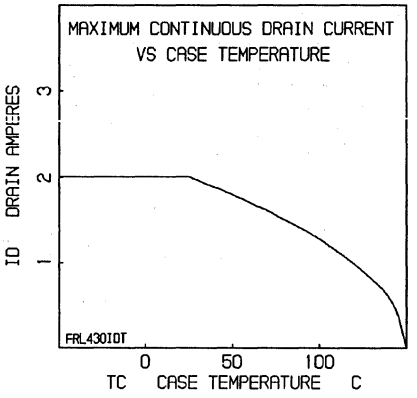
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

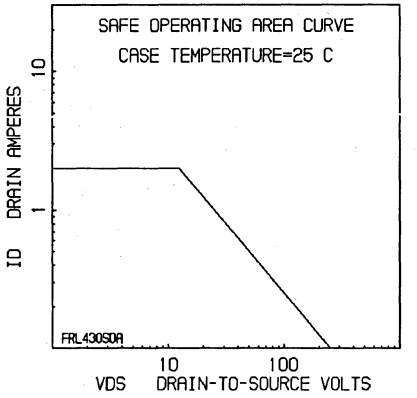
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7281D, R	VGS = 0, ID = 1mA	500	-	V
	(Note 5, 6)	BVDSS	2N7281H	VGS = 0, ID = 1mA	475	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7281D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7281H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7281D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7281H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7281D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7281H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7281D, R	VGS = 0, VDS = 400V	-	25	µA
	(Note 5, 6)	IDSS	2N7281H	VGS = 0, VDS = 400V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7281D, R	VGS = 10V, ID = 2A	-	5.25	V
	(Note 1, 5, 6)	VDS(on)	2N7281H	VGS = 16V, ID = 2A	-	7.88	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7281D, R	VGS = 10V, ID = 1A	-	2.50	Ω
	(Note 1, 5, 6)	RDS(on)	2N7281H	VGS = 14V, ID = 1A	-	3.75	Ω

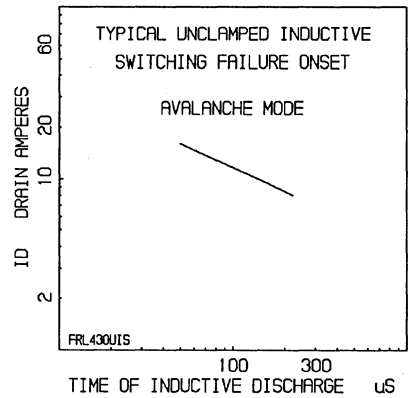
NOTES:

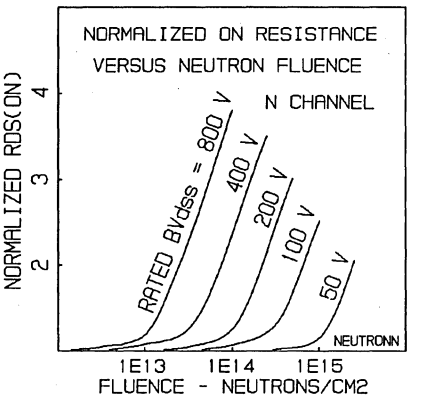
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 3E12
5. Gamma = 1000KRAD(Si). Neutron = 3E12
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 10/29/90 on TA 17635 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

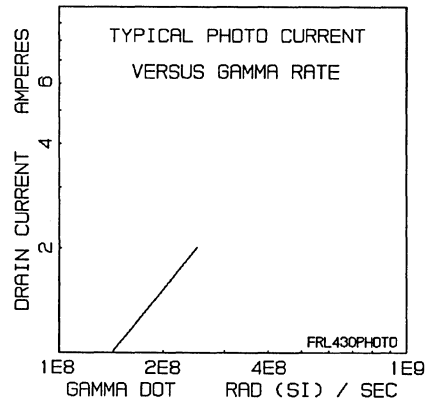
Typical Performance Characteristics

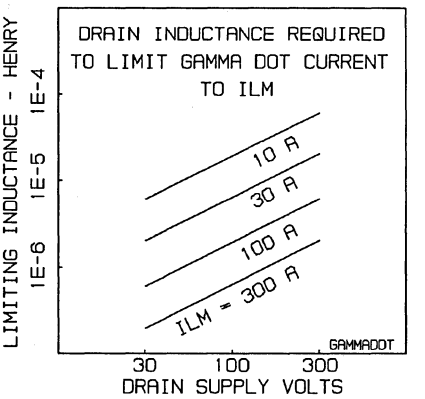












HARRIS SEMICONDUCTOR

2N7282D, 2N7282R 2N7282H

REGISTRATION PENDING
Currently Available as FRS430 (D, R, H)
December 1992

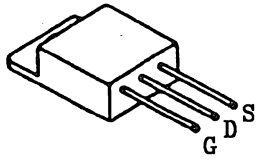
Radiation Hardened N-Channel Power MOSFETs

Features

- 3A, 500V, RDS(on) = 2.52Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 8.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E12 Neutrons/cm^2
  - Usable to 3E13 Neutrons/cm^2
- Single Event - Typically Survives 1E5ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Package

TO-257AA



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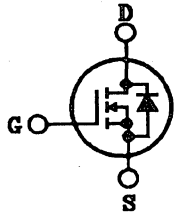


Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7282D, R, H	UNITS
Drain-Source Voltage	VDS	500	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	500	V
Continuous Drain Current			
TC = +25°C	ID	3	A
TC = +100°C	ID	2	A
Pulsed Drain Current	IDM	9	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	50	W
TC = +100°C	PT	20	W
Derated Above +25°C		0.40	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	9	A
Continuous Source Current (Body Diode)	IS	3	A
Pulsed Source Current (Body Diode)	ISM	9	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3253

HARRIS SEMICONDUCTOR

2N7283D, 2N7283R 2N7283H

REGISTRATION PENDING
Currently Available as FRM140 (D, R, H)
December 1992

Radiation Hardened N-Channel Power MOSFETs

Features

- 23A, 100V, RDS(on) = 0.130Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 3.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E13 Neutrons/cm^2
  - Usable to 3E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

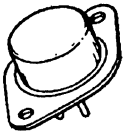
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n^0) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-204AA



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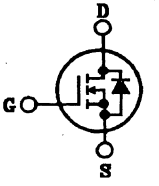


Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7283D, R, H	UNITS
Drain-Source Voltage	VDS	100	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	100	V
Continuous Drain Current			
TC = +25°C	ID	23	A
TC = +100°C	ID	15	A
Pulsed Drain Current	IDM	69	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	125	W
TC = +100°C	PT	50	W
Derated Above +25°C		1.00	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	69	A
Continuous Source Current (Body Diode)	IS	23	A
Pulsed Source Current (Body Diode)	ISM	69	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3220**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	100	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 100V, VGS = 0 VDS = 80V, VGS = 0 VDS = 80V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	69	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 23A	-	3.14	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 15A	-	0.13	Ω
Turn-On Delay Time	td(on)	VDD = 50V, ID = 23A	-	50	ns
Rise Time	tr	Pulse Width = 3µs	-	500	ns
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	160	ns
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	200	ns
Gate-Charge Threshold	QG(th)	VDD = 50V, ID = 23A IGS1 = IGS2 0 ≤ VGS ≤ 20	2	8	nc
Gate-Charge On State	QG(on)		30	122	nc
Gate-Charge Total	QGM		57	228	nc
Plateau Voltage	VGP		3	12	V
Gate-Charge Source	QGS		6	24	nc
Gate-Charge Drain	QGD		13	54	nc
Diode Forward Voltage	VSD	ID = 23A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 23A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	Rθjc		-	1.0	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	30	°C/W

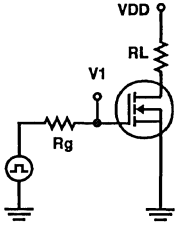


FIGURE 1. SWITCHING TIME TESTING

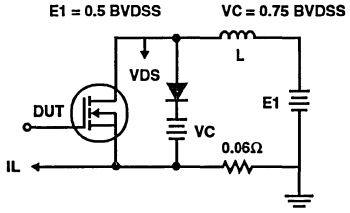


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

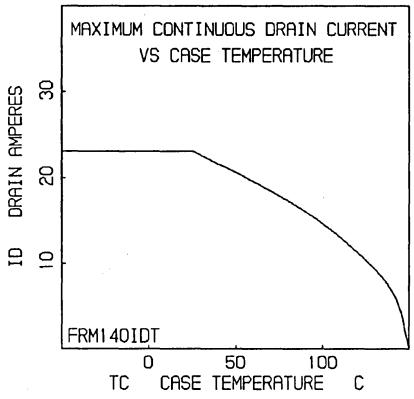
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

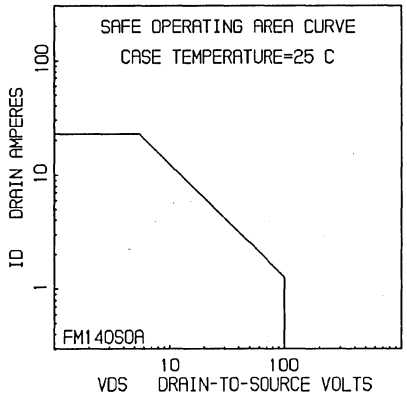
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS		UNITS
					MIN	MAX	
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7283D, R	VGS = 0, ID = 1mA	100	-	V
	(Note 5, 6)	BVDSS	2N7283H	VGS = 0, ID = 1mA	95	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7283D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7283H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7283D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7283H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7283D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7283H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7283D, R	VGS = 0, VDS = 80V	-	25	µA
	(Note 5, 6)	IDSS	2N7283H	VGS = 0, VDS = 80V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7283D, R	VGS = 10V, ID = 23A	-	3.14	V
	(Note 1, 5, 6)	VDS(on)	2N7283H	VGS = 16V, ID = 23A	-	4.83	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7283D, R	VGS = 10V, ID = 15A	-	0.130	Ω
	(Note 1, 5, 6)	RDS(on)	2N7283H	VGS = 14V, ID = 15A	-	0.200	Ω

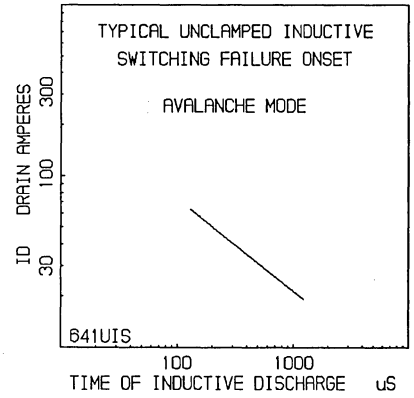
NOTES:

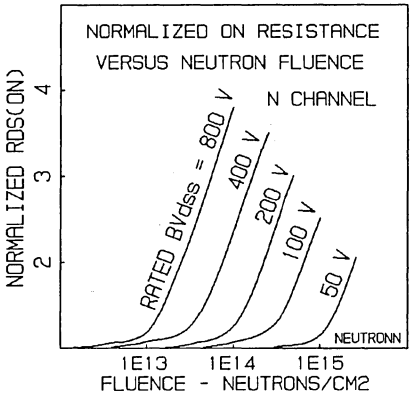
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 3E13
5. Gamma = 1000KRAD(Si). Neutron = 3E13
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 6/25/90 on TA 17641 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

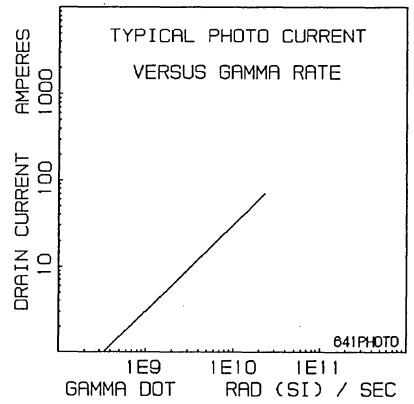
Typical Performance Characteristics

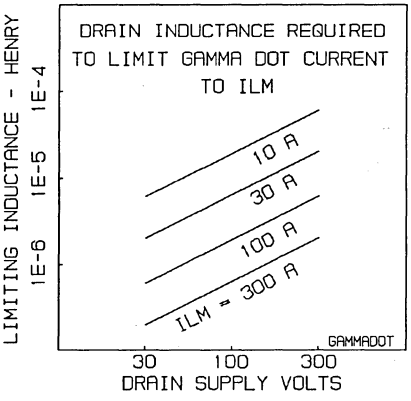












HARRIS SEMICONDUCTOR

2N7284D, 2N7284R 2N7284H

REGISTRATION PENDING
Currently Available as FRS140 (D, R, H)
December 1992

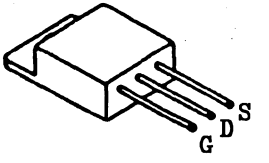
Radiation Hardened N-Channel Power MOSFETs

Features

- 17A, 100V, RDS(on) = 0.145Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 3.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E13 Neutrons/cm^2
  - Usable to 3E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Package

TO-257AA



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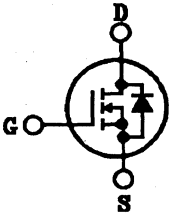


Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n^o) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7284D, R, H	UNITS
Drain-Source Voltage	VDS	100	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	100	V
Continuous Drain Current			
TC = +25°C	ID	17	A
TC = +100°C	ID	11	A
Pulsed Drain Current	IDM	51	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	75	W
TC = +100°C	PT	30	W
Derated Above +25°C		0.60	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	51	A
Continuous Source Current (Body Diode)	IS	17	A
Pulsed Source Current (Body Diode)	ISM	51	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3254**

HARRIS SEMICONDUCTOR

2N7285D, 2N7285R 2N7285H

REGISTRATION PENDING
Currently Available as FRM240(D, R, H)
December 1992

Radiation Hardened N-Channel Power MOSFETs

Features

- 16A, 200V, RDS(on) = 0.24Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 5.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

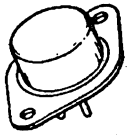
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-204AA



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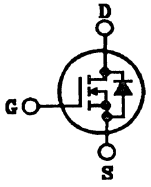


Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7285D, R, H	UNITS
Drain-Source Voltage	VDS	200	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	200	V
Continuous Drain Current			
TC = +25°C	ID	16	A
TC = +100°C	ID	10	A
Pulsed Drain Current	IDM	48	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	125	W
TC = +100°C	PT	50	W
Derated Above +25°C		1.00	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	48	A
Continuous Source Current (Body Diode)	IS	16	A
Pulsed Source Current (Body Diode)	ISM	48	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3225**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	200	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 200V, VGS = 0 VDS = 160V, VGS = 0 VDS = 160V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	48	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 16A	-	4.03	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 10A	-	0.240	Ω
Turn-On Delay Time	td(on)	VDD = 100V, ID = 16A	-	52	ns
Rise Time	tr	Pulse Width = 3µs	-	264	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	280	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	148	
Gate-Charge Threshold	QG(th)	VDD = 100V, ID = 16A IGS1 = IGS2 0 ≤ VGS ≤ 20	1.5	8	nc
Gate-Charge On State	QG(on)		29	116	
Gate-Charge Total	QGM		57	228	
Plateau Voltage	VGP		3	16	V
Gate-Charge Source	QGS		7	28	nc
Gate-Charge Drain	QGD		15	60	
Diode Forward Voltage	VSD	ID = 16A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 16A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	Rθjc		-	1.0	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	30	

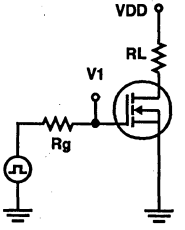


FIGURE 1. SWITCHING TIME TESTING

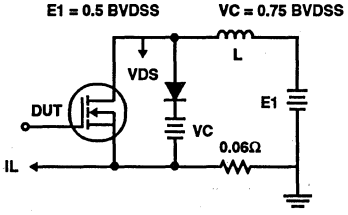


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

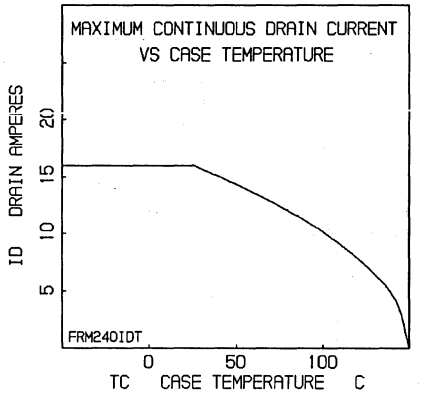
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

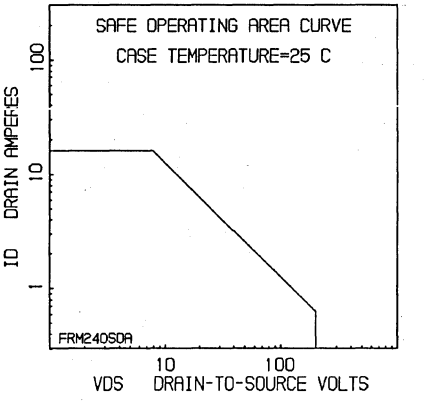
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7285D, R	VGS = 0, ID = 1mA	200	-	V
	(Note 5, 6)	BVDSS	2N7285H	VGS = 0, ID = 1mA	190	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7285D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7285H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7285D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7285H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7285D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7285H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7285D, R	VGS = 0, VDS = 160V	-	25	μA
	(Note 5, 6)	IDSS	2N7285H	VGS = 0, VDS = 160V	-	100	μA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7285D, R	VGS = 10V, ID = 16A	-	4.03	V
	(Note 1, 5, 6)	VDS(on)	2N7285H	VGS = 16V, ID = 16A	-	6.05	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7285D, R	VGS = 10V, ID = 10A	-	0.240	Ω
	(Note 1, 5, 6)	RDS(on)	2N7285H	VGS = 14V, ID = 10A	-	0.360	Ω

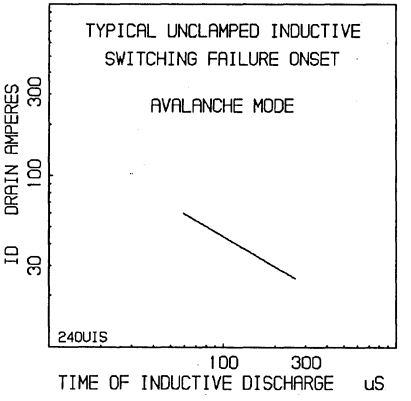
NOTES:

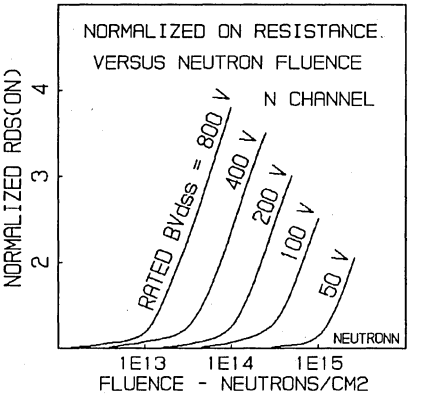
1. Pulse test, 300μs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 1E13
5. Gamma = 1000KRAD(Si). Neutron = 1E13
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 7/9/90 on TA 17642 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

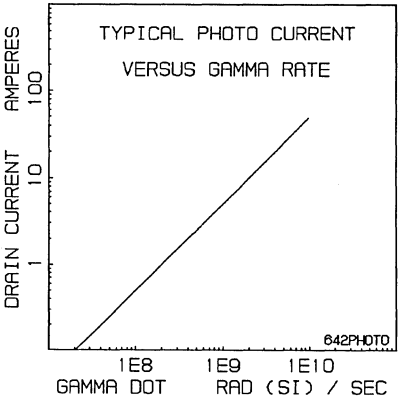
Typical Performance Characteristics

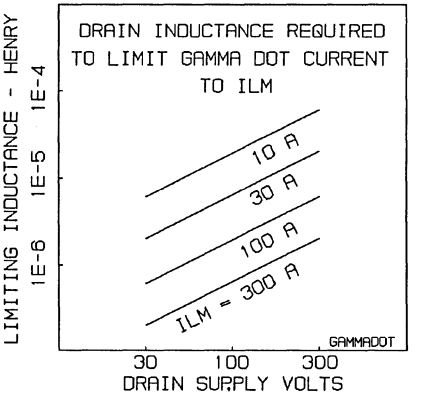












HARRIS SEMICONDUCTOR

2N7286D, 2N7286R 2N7286H

REGISTRATION PENDING
Currently Available as FRS240 (D, R, H)
December 1992

Radiation Hardened N-Channel Power MOSFETs

Features

- 12A, 200V, RDS(on) = 0.255Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 5.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

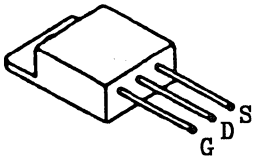
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-257AA



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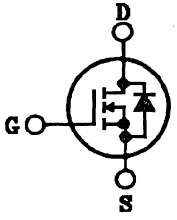


Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7286D, R, H	UNITS
Drain-Source Voltage	VDS	200	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	200	V
Continuous Drain Current			
TC = +25°C	ID	12	A
TC = +100°C	ID	7	A
Pulsed Drain Current	IDM	36	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	75	W
TC = +100°C	PT	30	W
Derated Above +25°C		0.60	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	36	A
Continuous Source Current (Body Diode)	IS	12	A
Pulsed Source Current (Body Diode)	ISM	36	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3255**

HARRIS SEMICONDUCTOR

2N7287D, 2N7287R 2N7287H

REGISTRATION PENDING
Currently Available as FRM244(D, R, H)
December 1992

Radiation Hardened N-Channel Power MOSFETs

Features

- 12A, 250V, RDS(on) = 0.400Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 7.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

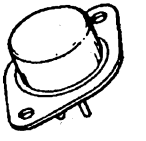
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-204AA



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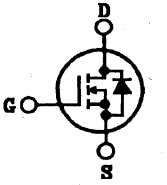


Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7287D, R, H	UNITS
Drain-Source Voltage	VDS	250	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	250	V
Continuous Drain Current			
TC = +25°C	ID	12	A
TC = +100°C	ID	7	A
Pulsed Drain Current	IDM	36	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	125	W
TC = +100°C	PT	50	W
Derated Above +25°C		1.00	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	36	A
Continuous Source Current (Body Diode)	IS	12	A
Pulsed Source Current (Body Diode)	ISM	36	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3230**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	250	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 250V, VGS = 0 VDS = 200V, VGS = 0 VDS = 200V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	36	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 12A	-	5.04	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 7A	-	0.400	Ω
Turn-On Delay Time	td(on)	VDD = 125V, ID = 12A	-	62	ns
Rise Time	tr	Pulse Width = 3µs	-	258	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	228	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	110	
Gate-Charge Threshold	QG(th)	VDD = 125V, ID = 12A IGS1 = IGS2 0 ≤ VGS ≤ 20	2	8	nc
Gate-Charge On State	QG(on)		25	102	
Gate-Charge Total	QGM		49	198	
Plateau Voltage	VGP		4	16	V
Gate-Charge Source	QGS		7	30	nc
Gate-Charge Drain	QGD		13	54	
Diode Forward Voltage	VSD	ID = 12A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 12A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	Rθjc		-	1.0	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	30	

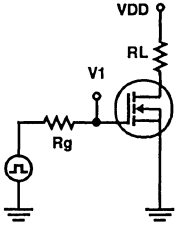


FIGURE 1. SWITCHING TIME TESTING

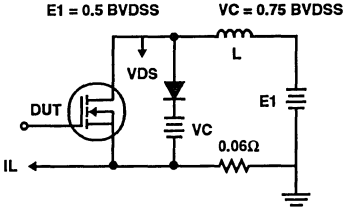


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

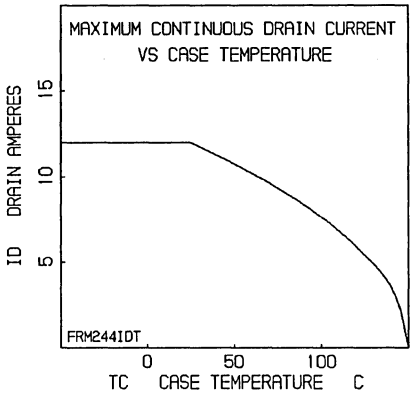
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

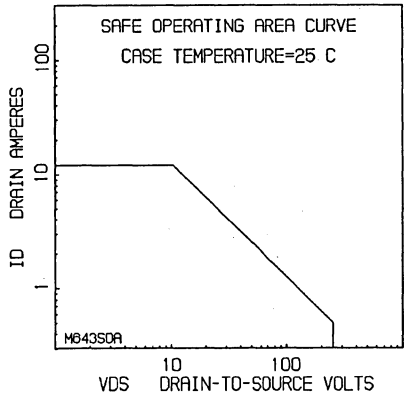
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7287D, R	VGS = 0, ID = 1mA	250	-	V
	(Note 5, 6)	BVDSS	2N7287H	VGS = 0, ID = 1mA	238	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7287D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7287H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7287D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7287H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7287D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7287H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7287D, R	VGS = 0, VDS = 200V	-	25	µA
	(Note 5, 6)	IDSS	2N7287H	VGS = 0, VDS = 200V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7287D, R	VGS = 10V, ID = 12A	-	5.04	V
	(Note 1, 5, 6)	VDS(on)	2N7287H	VGS = 16V, ID = 12A	-	7.56	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7287D, R	VGS = 10V, ID = 7A	-	0.400	Ω
	(Note 1, 5, 6)	RDS(on)	2N7287H	VGS = 14V, ID = 7A	-	0.600	Ω

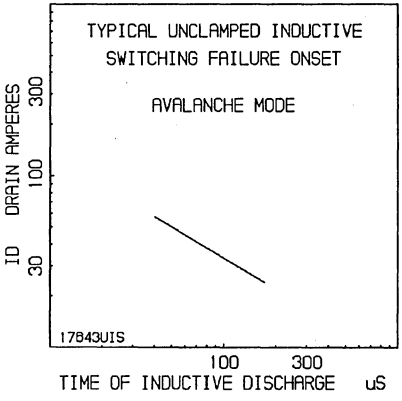
NOTES:

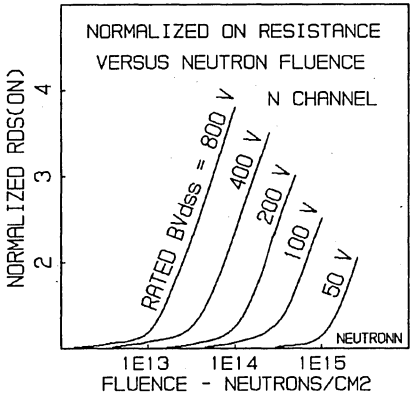
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 1E13
5. Gamma = 1000KRAD(Si). Neutron = 1E13
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 1/30/90 on TA 17643 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

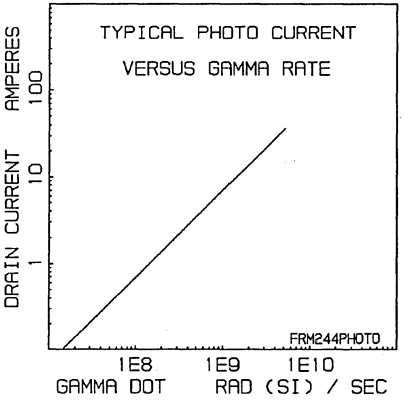
Typical Performance Characteristics

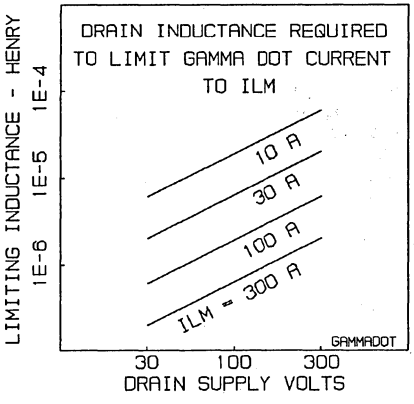












HARRIS SEMICONDUCTOR

2N7288D, 2N7288R 2N7288H

Radiation Hardened N-Channel Power MOSFETs

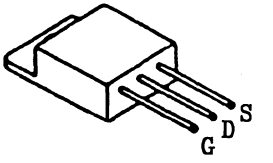
REGISTRATION PENDING
Currently Available as FRS244 (D, R, H)
December 1992

Features

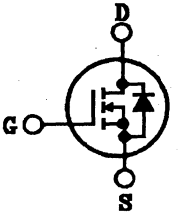
- 9A, 250V, RDS(on) = 0.415Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 7.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Package

TO-257AA



Symbol



Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7288D, R, H	UNITS
Drain-Source Voltage	VDS	250	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	250	V
Continuous Drain Current			
TC = +25°C	ID	9	A
TC = +100°C	ID	6	A
Pulsed Drain Current	IDM	27	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	75	W
TC = +100°C	PT	30	W
Derated Above +25°C		0.60	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	27	A
Continuous Source Current (Body Diode)	IS	9	A
Pulsed Source Current (Body Diode)	ISM	27	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3256**

HARRIS SEMICONDUCTOR

2N7289D, 2N7289R 2N7289H

REGISTRATION PENDING
Currently Available as FRM440(D, R, H)
December 1992

Radiation Hardened N-Channel Power MOSFETs

Features

- 6A, 500V, RDS(on) = 1.40Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current
  - 12.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E12 Neutrons/cm^2
  - Usable to 3E13 Neutrons/cm^2
- Single Event
  - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

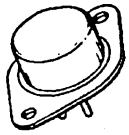
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm$_2$ for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

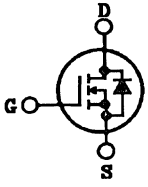
This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-204AA



Symbol



Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7289D, R, H	UNITS
Drain-Source Voltage	VDS	500	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	500	V
Continuous Drain Current			
TC = +25°C	ID	6	A
TC = +100°C	ID	4	A
Pulsed Drain Current	IDM	18	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	125	W
TC = +100°C	PT	50	W
Derated Above +25°C		1.00	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	18	A
Continuous Source Current (Body Diode)	IS	6	A
Pulsed Source Current (Body Diode)	ISM	18	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3235**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	500	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 500V, VGS = 0 VDS = 400V, VGS = 0 VDS = 400V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	18	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 6A	-	8.82	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 4A	-	1.40	Ω
Turn-On Delay Time	td(on)	VDD = 250V, ID = 6A	-	60	ns
Rise Time	tr	Pulse Width = 3µs	-	84	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	476	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	116	
Gate-Charge Threshold	QG(th)	VDD = 250V, ID = 6A IGS1 = IGS2 0 ≤ VGS ≤ 20	2	8	nc
Gate-Charge On State	QG(on)		32	128	
Gate-Charge Total	QGM		65	250	
Plateau Voltage	VGP		3	12	V
Gate-Charge Source	QGS		6	24	nc
Gate-Charge Drain	QGD		11	46	
Diode Forward Voltage	VSD	ID = 6A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 6A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	Rθjc		-	1.0	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	30	

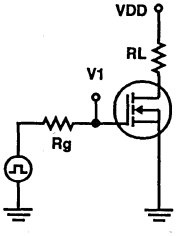


FIGURE 1. SWITCHING TIME TESTING

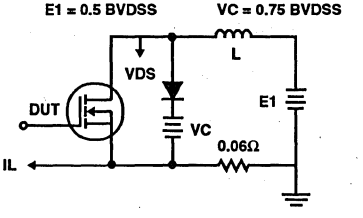


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

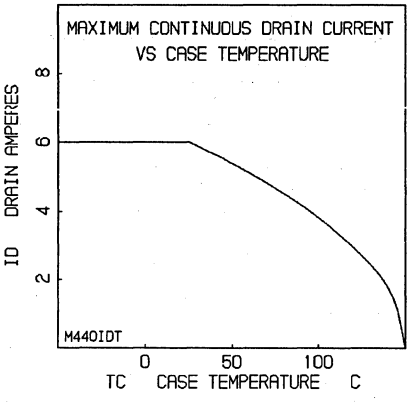
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

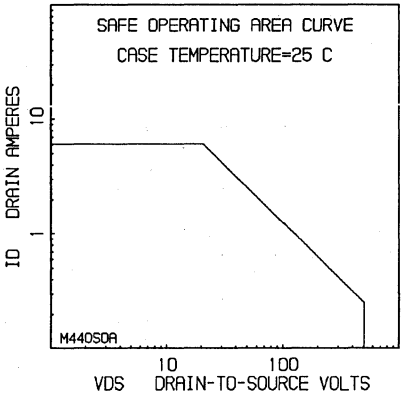
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7289D, R	VGS = 0, ID = 1mA	500	-	V
	(Note 5, 6)	BVDSS	2N7289H	VGS = 0, ID = 1mA	475	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7289D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7289H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7289D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7289H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7289D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7289H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7289D, R	VGS = 0, VDS = 400V	-	25	µA
	(Note 5, 6)	IDSS	2N7289H	VGS = 0, VDS = 400V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7289D, R	VGS = 10V, ID = 6A	-	8.82	V
	(Note 1, 5, 6)	VDS(on)	2N7289H	VGS = 16V, ID = 6A	-	13.20	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7289D, R	VGS = 10V, ID = 4A	-	1.40	Ω
	(Note 1, 5, 6)	RDS(on)	2N7289H	VGS = 14V, ID = 4A	-	2.10	Ω

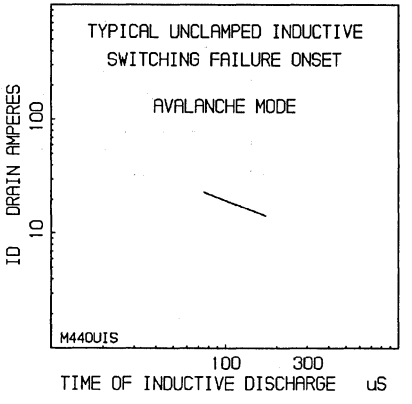
NOTES:

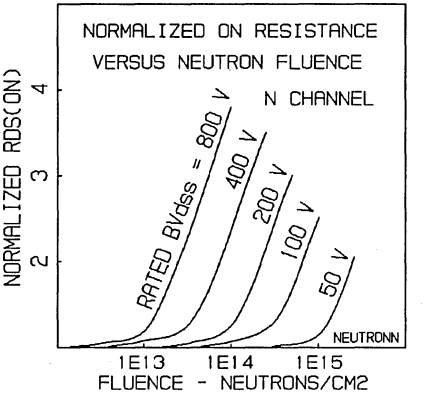
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 3E12
5. Gamma = 1000KRAD(Si). Neutron = 3E12
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 3/15/90 on TA 17645 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

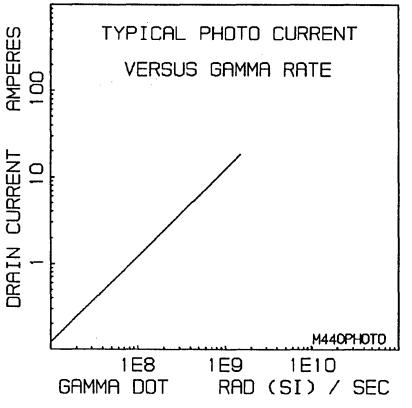
Typical Performance Characteristics

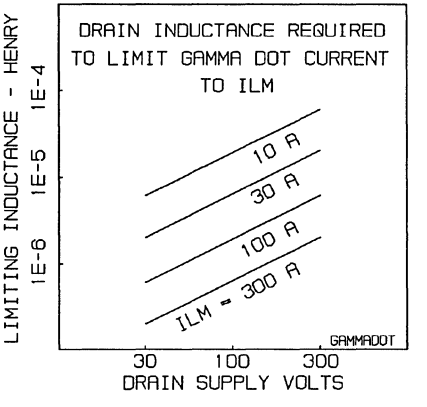












HARRIS SEMICONDUCTOR

2N7290D, 2N7290R 2N7290H

REGISTRATION PENDING
Currently Available as FRS440 (D, R, H)
December 1992

Radiation Hardened N-Channel Power MOSFETs

Features

- 5A, 500V, RDS(on) = 1.42Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 12.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E12 Neutrons/cm^2
  - Usable to 3E13 Neutrons/cm^2
- Single Event - Typically Survives 1E5ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

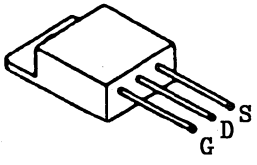
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

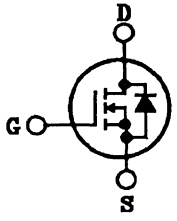
This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-257AA



Symbol



Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7290D, R, H	UNITS
Drain-Source Voltage	VDS	500	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	500	V
Continuous Drain Current			
TC = +25°C	ID	5	A
TC = +100°C	ID	3	A
Pulsed Drain Current	IDM	15	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	75	W
TC = +100°C	PT	30	W
Derated Above +25°C		0.60	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	15	A
Continuous Source Current (Body Diode)	IS	5	A
Pulsed Source Current (Body Diode)	ISM	15	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3257**

HARRIS SEMICONDUCTOR

2N7291D, 2N7291R 2N7291H

REGISTRATION PENDING
Currently Available as FRK150(D, R, H)
December 1992

Radiation Hardened N-Channel Power MOSFETs

Features

- 40A, 100V, RDS(on) = 0.055Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 7.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E13 Neutrons/cm^2
  - Usable to 3E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

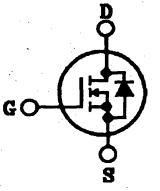
This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n^0) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-204AE

Symbol



Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7291D, R, H	UNITS
Drain-Source Voltage	VDS	100	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	100	V
Continuous Drain Current			
TC = +25°C	ID	40	A
TC = +100°C	ID	25	A
Pulsed Drain Current	IDM	100	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	150	W
TC = +100°C	PT	60	W
Derated Above +25°C		1.20	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	100	A
Continuous Source Current (Body Diode)	IS	40	A
Pulsed Source Current (Body Diode)	ISM	100	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3221**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	100	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 100V, VGS = 0 VDS = 80V, VGS = 0 VDS = 80V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	100	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 40A	-	2.32	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 25A	-	0.055	Ω
Turn-On Delay Time	td(on)	VDD = 50V, ID = 40A	-	170	ns
Rise Time	tr	Pulse Width = 3µs	-	1120	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	420	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	380	
Gate-Charge Threshold	QG(th)	VDD = 50V, ID = 40A IGS1 = IGS2 0 ≤ VGS ≤ 20	3.5	15	nc
Gate-Charge On State	QG(on)		58	230	
Gate-Charge Total	QGM		140	560	
Plateau Voltage	VGP		4	16	V
Gate-Charge Source	QGS		15	63	nc
Gate-Charge Drain	QGD		30	123	
Diode Forward Voltage	VSD	ID = 40A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 40A; di/dt = 100A/µs	-	1400	ns
Junction-To-Case	Rθjc		-	0.83	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	30	

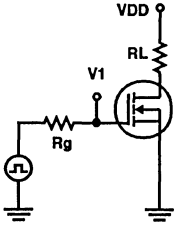


FIGURE 1. SWITCHING TIME TESTING

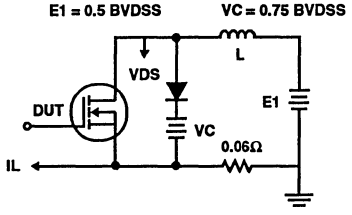


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

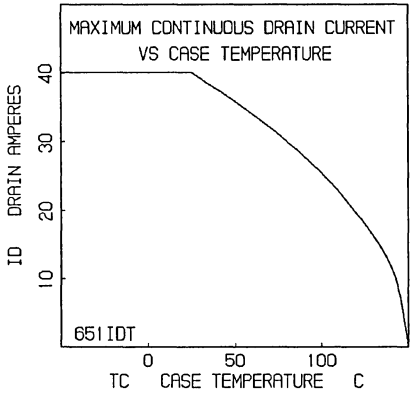
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

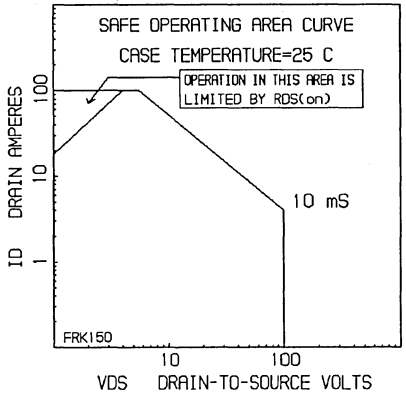
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7291D, R	VGS = 0, ID = 1mA	100	-	V
	(Note 5, 6)	BVDSS	2N7291H	VGS = 0, ID = 1mA	95	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7291D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7291H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7291D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7291H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7291D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7291H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7291D, R	VGS = 0, VDS = 80V	-	25	µA
	(Note 5, 6)	IDSS	2N7291H	VGS = 0, VDS = 80V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7291D, R	VGS = 10V, ID = 40A	-	2.31	V
	(Note 1, 5, 6)	VDS(on)	2N7291H	VGS = 16V, ID = 40A	-	3.47	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7291D, R	VGS = 10V, ID = 25A	-	0.055	Ω
	(Note 1, 5, 6)	RDS(on)	2N7291H	VGS = 14V, ID = 25A	-	0.083	Ω

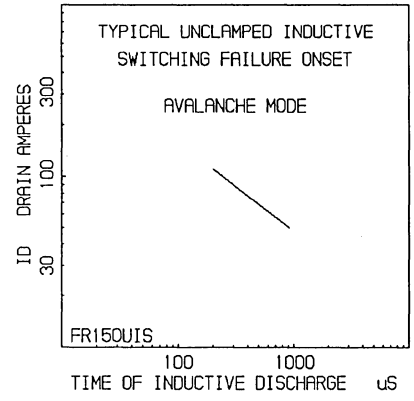
NOTES:

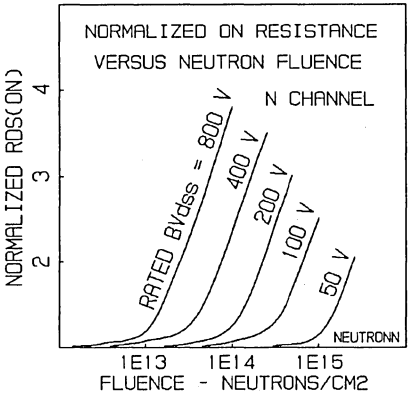
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 3E13
5. Gamma = 1000KRAD(Si). Neutron = 3E13
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 11/6/89 on TA 17651 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

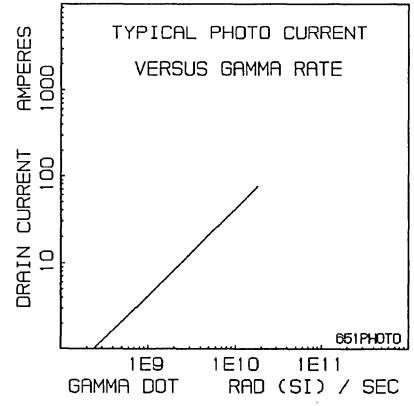
Typical Performance Characteristics

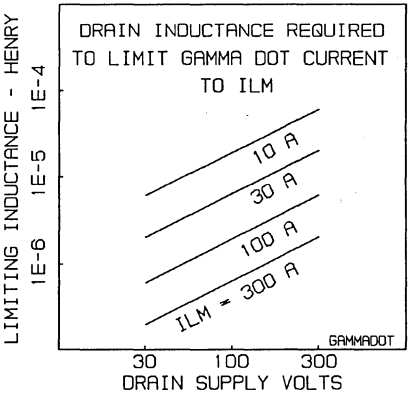












HARRIS SEMICONDUCTOR

2N7292D, 2N7292R 2N7292H

REGISTRATION PENDING
Currently Available as FRF150(D, R, H)
December 1992

Radiation Hardened N-Channel Power MOSFETs

Features

- 25A, 100V, RDS(on) = 0.07Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 7.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E13 Neutrons/cm^2
  - Usable to 3E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

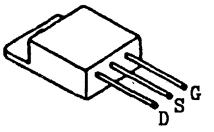
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-254AA



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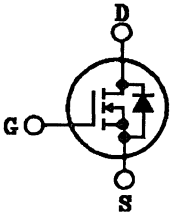


Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7292D, R, H	UNITS
Drain-Source Voltage	VDS	100	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	100	V
Continuous Drain Current			
TC = +25°C	ID	25	A
TC = +100°C	ID	20	A
Pulsed Drain Current	IDM	75	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	125	W
TC = +100°C	PT	50	W
Derated Above +25°C		1.00	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	75	A
Continuous Source Current (Body Diode)	IS	25	A
Pulsed Source Current (Body Diode)	ISM	75	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3215**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	100	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 100V, VGS = 0 VDS = 80V, VGS = 0 VDS = 80V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	75	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 25A	-	1.84	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 20A	-	.07	Ω
Turn-On Delay Time	td(on)	VDD = 50V, ID = 25A	-	134	ns
Rise Time	tr	Pulse Width = 3µs	-	628	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	642	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	490	
Gate-Charge Threshold	QG(th)	VDD = 50V, ID = 25A IGS1 = IGS2 0 ≤ VGS ≤ 20	4	17	nc
Gate-Charge On State	QG(on)		79	314	
Gate-Charge Total	QGM		138	552	
Plateau Voltage	VGP		2	12	V
Gate-Charge Source	QGS		11	46	nc
Gate-Charge Drain	QGD		40	164	
Diode Forward Voltage	VSD	ID = 25A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 25A; di/dt = 100A/µs	-	1400	ns
Junction-To-Case	RΘjc		-	1.0	°C/W
Junction-To-Ambient	RΘja	Free Air Operation	-	48	

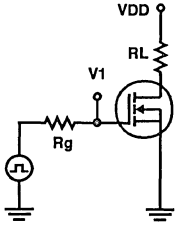


FIGURE 1. SWITCHING TIME TESTING

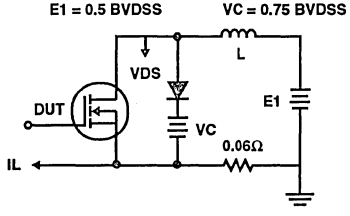


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

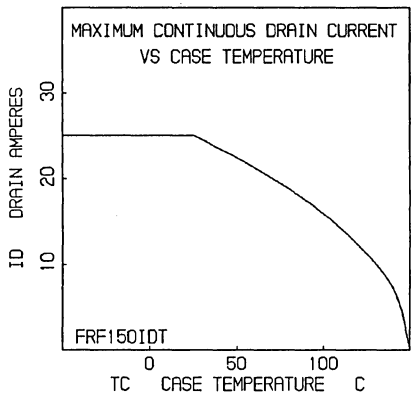
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

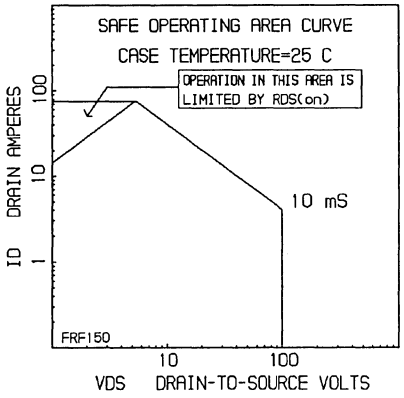
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7292D, R	VGS = 0, ID = 1mA	100	-	V
	(Note 5, 6)	BVDSS	2N7292H	VGS = 0, ID = 1mA	95	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7292D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7292H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7292D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7292H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7292D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7292H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7292D, R	VGS = 0, VDS = 80V	-	25	µA
	(Note 5, 6)	IDSS	2N7292H	VGS = 0, VDS = 80V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7292D, R	VGS = 10V, ID = 25A	-	1.84	V
	(Note 1, 5, 6)	VDS(on)	2N7292H	VGS = 16V, ID = 25A	-	2.76	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7292D, R	VGS = 10V, ID = 20A	-	0.07	Ω
	(Note 1, 5, 6)	RDS(on)	2N7292H	VGS = 14V, ID = 20A	-	0.105	Ω

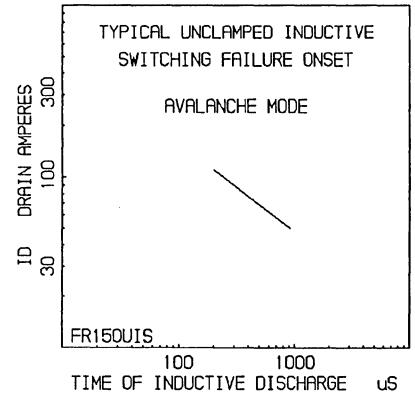
NOTES:

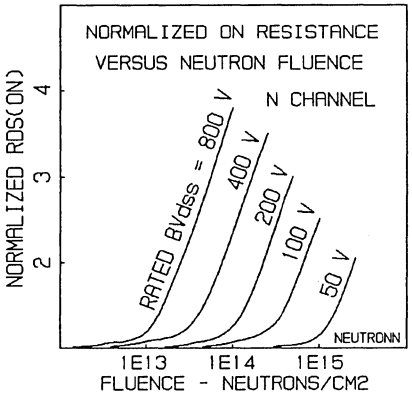
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 3E13
5. Gamma = 1000KRAD(Si). Neutron = 3E13
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 11/16/89 on TA 17651 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

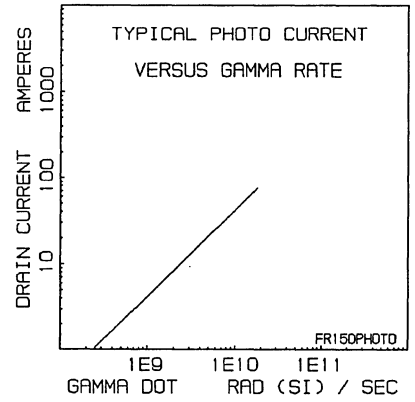
Typical Performance Characteristics

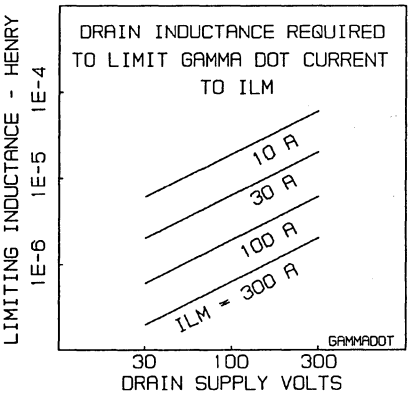












HARRIS SEMICONDUCTOR

2N7293D, 2N7293R 2N7293H

REGISTRATION PENDING
Currently Available as FRK250(D, R, H)
December 1992

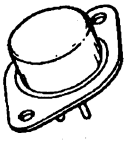
Radiation Hardened N-Channel Power MOSFETs

Features

- 27A, 200V, RDS(on) = 0.100Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 12.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Package

TO-204AE



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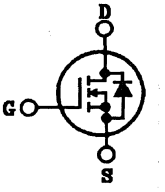


Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7293D, R, H	UNITS
Drain-Source Voltage	VDS	200	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	200	V
Continuous Drain Current			
TC = +25°C	ID	27	A
TC = +100°C	ID	17	A
Pulsed Drain Current	IDM	81	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	150	W
TC = +100°C	PT	60	W
Derated Above +25°C		1.20	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	81	A
Continuous Source Current (Body Diode)	IS	27	A
Pulsed Source Current (Body Diode)	ISM	81	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3226**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	200	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 200V, VGS = 0 VDS = 160V, VGS = 0 VDS = 160V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	81	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 27A	-	2.7	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 17A	-	0.100	Ω
Turn-On Delay Time	td(on)	VDD = 100V, ID = 27A	-	170	ns
Rise Time	tr	Pulse Width = 3µs	-	600	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	580	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	300	
Gate-Charge Threshold	QG(th)	VDD = 100V, ID = 27A IGS1 = IGS2 0 ≤ VGS ≤ 20	3.5	15	nc
Gate-Charge On State	QG(on)		61	244	
Gate-Charge Total	QGM		120	485	
Plateau Voltage	VGP		3	14	V
Gate-Charge Source	QGS		13	53	nc
Gate-Charge Drain	QGD		31	125	
Diode Forward Voltage	VSD	ID = 27A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 27A; di/dt = 100A/µs	-	1700	ns
Junction-To-Case	Rθjc		-	0.83	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	30	

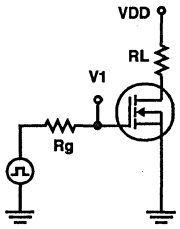


FIGURE 1. SWITCHING TIME TESTING

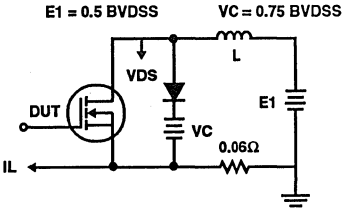


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

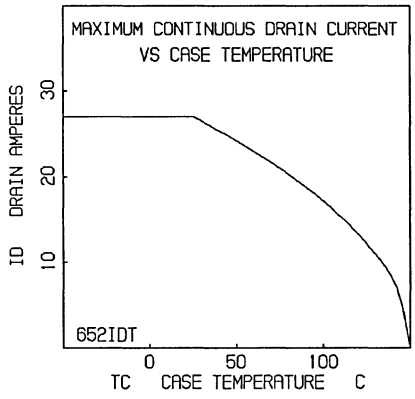
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

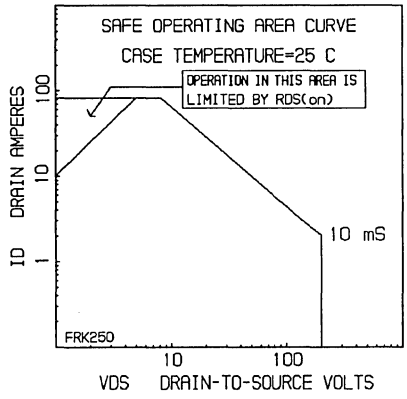
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7293D, R	VGS = 0, ID = 1mA	200	-	V
	(Note 5, 6)	BVDSS	2N7293H	VGS = 0, ID = 1mA	190	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7293D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7293H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7293D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7293H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7293D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7293H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7293D, R	VGS = 0, VDS = 160V	-	25	μA
	(Note 5, 6)	IDSS	2N7293H	VGS = 0, VDS = 160V	-	100	μA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7293D, R	VGS = 10V, ID = 27A	-	2.7	V
	(Note 1, 5, 6)	VDS(on)	2N7293H	VGS = 16V, ID = 27A	-	3.78	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7293D, R	VGS = 10V, ID = 17A	-	0.100	Ω
	(Note 1, 5, 6)	RDS(on)	2N7293H	VGS = 14V, ID = 17A	-	0.140	Ω

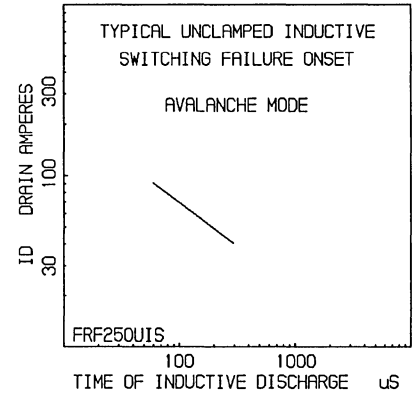
NOTES:

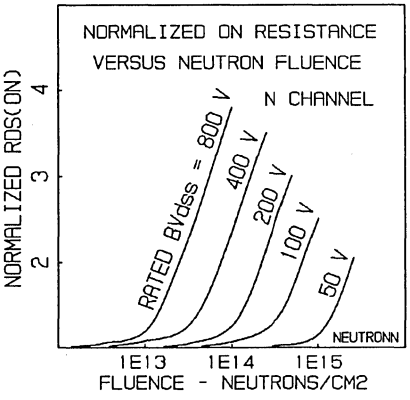
1. Pulse test, 300μs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 1E13
5. Gamma = 1000KRAD(Si). Neutron = 1E13
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 11/15/89 on TA 17652 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

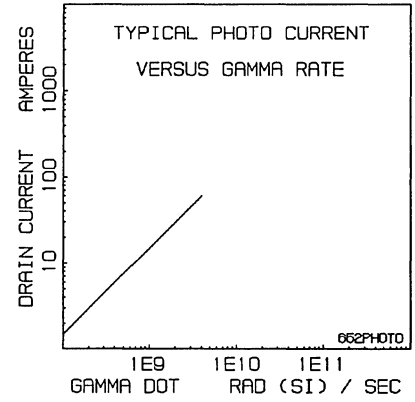
Typical Performance Characteristics

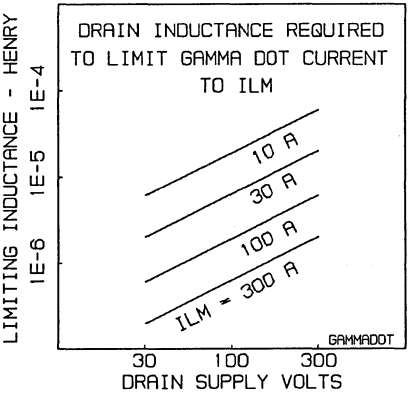












HARRIS SEMICONDUCTOR

2N7294D, 2N7294R 2N7294H

REGISTRATION PENDING
Currently Available as FRF250(D, R, H)
December 1992

Radiation Hardened N-Channel Power MOSFETs

Features

- 23A, 200V, RDS(on) = 0.115Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 12.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

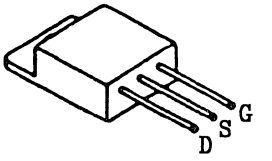
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-254AA



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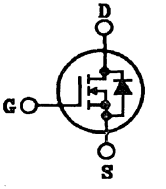


Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7294D, R, H	UNITS
Drain-Source Voltage	VDS	200	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	200	V
Continuous Drain Current			
TC = +25°C	ID	23	A
TC = +100°C	ID	15	A
Pulsed Drain Current	IDM	69	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	125	W
TC = +100°C	PT	50	W
Derated Above +25°C		1.00	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	69	A
Continuous Source Current (Body Diode)	IS	23	A
Pulsed Source Current (Body Diode)	ISM	69	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3227**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	200	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 200V, VGS = 0 VDS = 160V, VGS = 0 VDS = 160V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	69	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 23A	-	2.78	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 15A	-	0.115	Ω
Turn-On Delay Time	td(on)	VDD = 100V, ID = 23A	-	156	ns
Rise Time	tr	Pulse Width = 3µs	-	510	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	574	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	280	
Gate-Charge Threshold	QG(th)	VDD = 100V, ID = 23A IGS1 = IGS2 0 ≤ VGS ≤ 20	5	20	nc
Gate-Charge On State	QG(on)		75	298	
Gate-Charge Total	QGM		140	558	
Plateau Voltage	VGP		3	14	V
Gate-Charge Source	QGS		16	66	nc
Gate-Charge Drain	QGD		36	144	
Diode Forward Voltage	VSD	ID = 23A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 23A; di/dt = 100A/µs	-	1700	ns
Junction-To-Case	Rθjc		-	1.0	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	48	

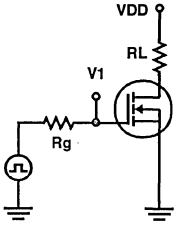


FIGURE 1. SWITCHING TIME TESTING

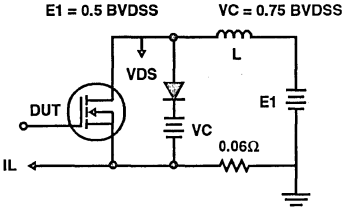


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

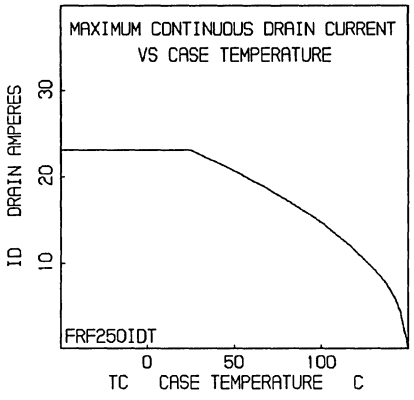
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

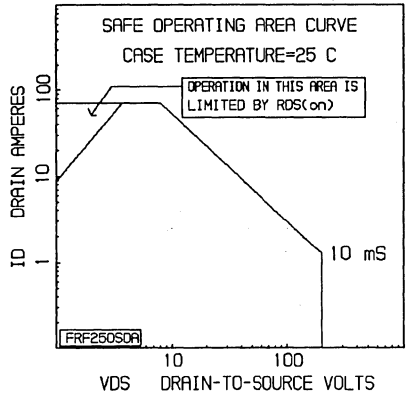
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS		UNITS
					MIN	MAX	
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7294D, R	VGS = 0, ID = 1mA	200	-	V
	(Note 5, 6)	BVDSS	2N7294H	VGS = 0, ID = 1mA	190	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7294D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7294H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7294D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7294H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7294D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7294H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7294D, R	VGS = 0, VDS = 160V	-	25	μA
	(Note 5, 6)	IDSS	2N7294H	VGS = 0, VDS = 160V	-	100	μA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7294D, R	VGS = 10V, ID = 23A	-	2.78	V
	(Note 1, 5, 6)	VDS(on)	2N7294H	VGS = 16V, ID = 23A	-	3.89	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7294D, R	VGS = 10V, ID = 15A	-	0.115	Ω
	(Note 1, 5, 6)	RDS(on)	2N7294H	VGS = 14V, ID = 15A	-	0.161	Ω

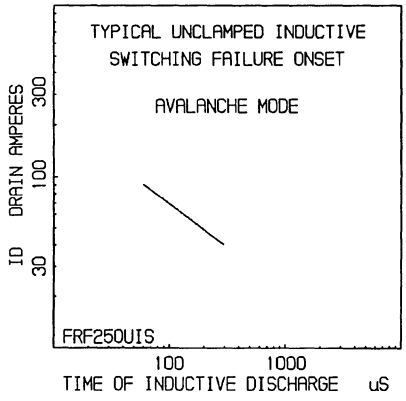
NOTES:

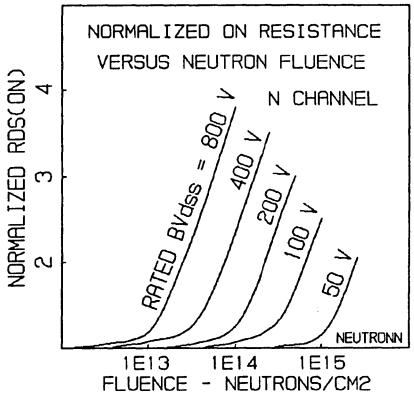
1. Pulse test, 300μs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 1E13
5. Gamma = 1000KRAD(Si). Neutron = 1E13
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 11/15/89 on TA 17652 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

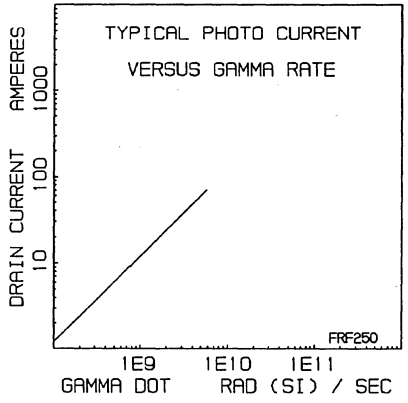
Typical Performance Characteristics

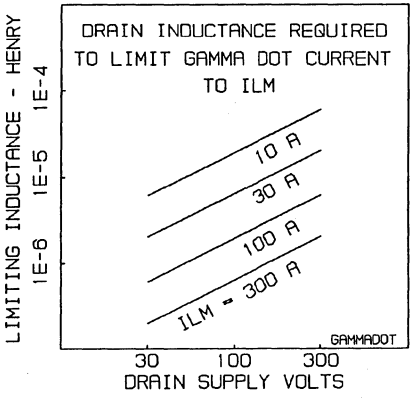












HARRIS SEMICONDUCTOR

2N7295D, 2N7295R 2N7295H

REGISTRATION PENDING
Currently Available as FRK254(D, R, H)
December 1992

Radiation Hardened N-Channel Power MOSFETs

Features

- 20A, 250V, RDS(on) = 0.170Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically if Current Limited to IDM
- Photo Current - 15.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

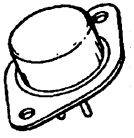
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n^0) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-204AE



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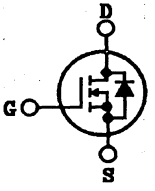


Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7295D, R, H	UNITS
Drain-Source Voltage	VDS	250	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	250	V
Continuous Drain Current			
TC = +25°C	ID	20	A
TC = +100°C	ID	12	A
Pulsed Drain Current	IDM	60	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	150	W
TC = +100°C	PT	60	W
Derated Above +25°C		1.20	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	60	A
Continuous Source Current (Body Diode)	IS	20	A
Pulsed Source Current (Body Diode)	ISM	60	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3231**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	250	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 250V, VGS = 0 VDS = 200V, VGS = 0 VDS = 200V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	60	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 20A	-	3.58	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 12A	-	0.170	Ω
Turn-On Delay Time	td(on)	VDD = 125V, ID = 20A	-	150	ns
Rise Time	tr	Pulse Width = 3µs	-	450	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	650	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	260	
Gate-Charge Threshold	QG(th)	VDD = 125V, ID = 20A IGS1 = IGS2 0 ≤ VGS ≤ 20	3.5	15	nc
Gate-Charge On State	QG(on)		63	252	
Gate-Charge Total	QGM		127	510	
Plateau Voltage	VGP		3	14	V
Gate-Charge Source	QGS		12	48	nc
Gate-Charge Drain	QGD		32	126	
Diode Forward Voltage	VSD	ID = 20A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 20A; di/dt = 100A/µs	-	2000	ns
Junction-To-Case	Rθjc		-	0.83	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	30	

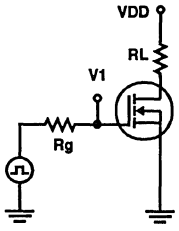


FIGURE 1. SWITCHING TIME TESTING

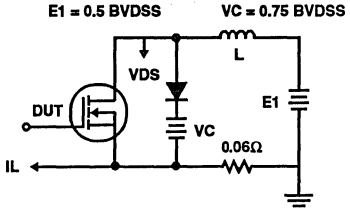


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

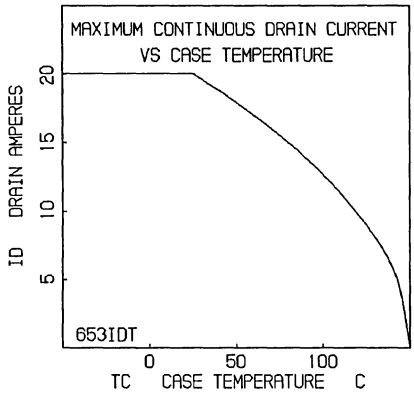
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

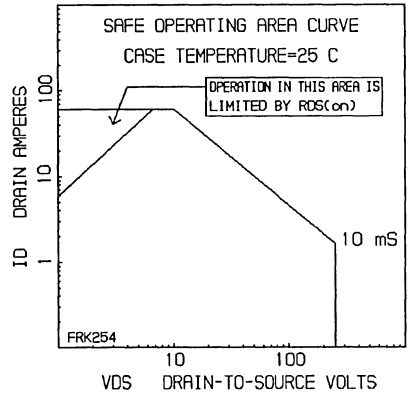
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7295D, R	VGS = 0, ID = 1mA	250	-	V
	(Note 5, 6)	BVDSS	2N7295H	VGS = 0, ID = 1mA	238	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7295D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7295H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7295D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7295H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7295D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7295H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7295D, R	VGS = 0, VDS = 200V	-	25	μA
	(Note 5, 6)	IDSS	2N7295H	VGS = 0, VDS = 200V	-	100	μA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7295D, R	VGS = 10V, ID = 20A	-	3.58	V
	(Note 1, 5, 6)	VDS(on)	2N7295H	VGS = 16V, ID = 20A	-	4.53	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7295D, R	VGS = 10V, ID = 12A	-	0.170	Ω
	(Note 1, 5, 6)	RDS(on)	2N7295H	VGS = 14V, ID = 12A	-	0.215	Ω

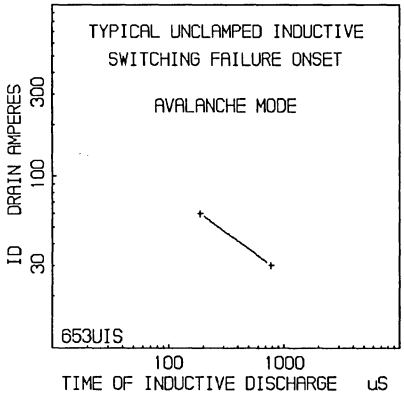
NOTES:

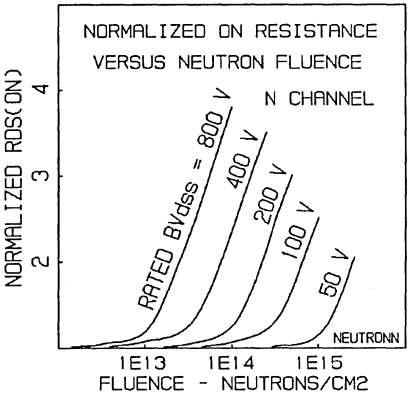
1. Pulse test, 300μs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 1E13
5. Gamma = 1000KRAD(Si). Neutron = 1E13
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 11/1/89 on TA 17653 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

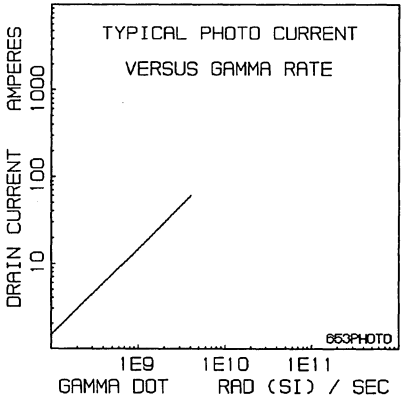
Typical Performance Characteristics

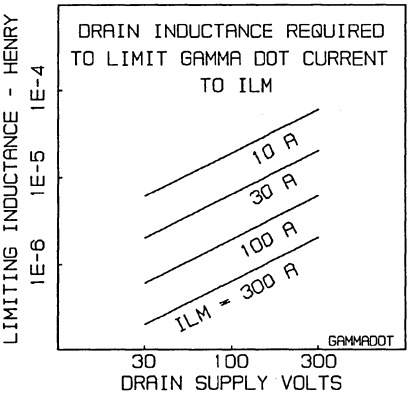












HARRIS SEMICONDUCTOR

2N7296D, 2N7296R 2N7296H

REGISTRATION PENDING
Currently Available as FRF254(D, R, H)
December 1992

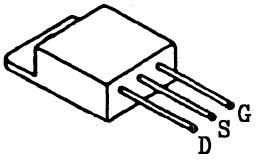
Radiation Hardened N-Channel Power MOSFETs

Features

- 17A, 250V, RDS(on) = 0.185Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 15.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Package

TO-254AA



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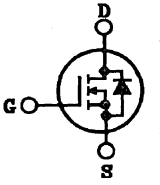


Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7296D, R, H	UNITS
Drain-Source Voltage	VDS	250	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	250	V
Continuous Drain Current			
TC = +25°C	ID	17	A
TC = +100°C	ID	11	A
Pulsed Drain Current	IDM	51	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	125	W
TC = +100°C	PT	50	W
Derated Above +25°C		1.00	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	51	A
Continuous Source Current (Body Diode)	IS	17	A
Pulsed Source Current (Body Diode)	ISM	51	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3232**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	250	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 250V, VGS = 0 VDS = 200V, VGS = 0 VDS = 200V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	51	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 17A	-	3.30	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 11A	-	0.185	Ω
Turn-On Delay Time	td(on)	VDD = 125V, ID = 17A	-	114	ns
Rise Time	tr	Pulse Width = 3µs	-	162	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	990	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	256	
Gate-Charge Threshold	QG(th)	VDD = 125V, ID = 17A IGS1 = IGS2 0 ≤ VGS ≤ 20	4	18	nc
Gate-Charge On State	QG(on)		66	264	
Gate-Charge Total	QGM		125	500	
Plateau Voltage	VGP		3	12	V
Gate-Charge Source	QGS		12	48	nc
Gate-Charge Drain	QGD		31	124	
Diode Forward Voltage	VSD	ID = 17A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 17A; di/dt = 100A/µs	-	2000	ns
Junction-To-Case	Rθjc		-	1.0	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	48	

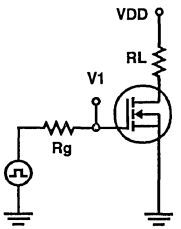


FIGURE 1. SWITCHING TIME TESTING

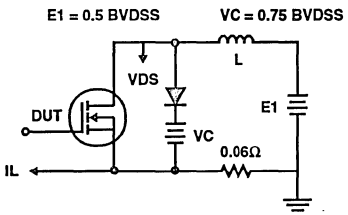


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

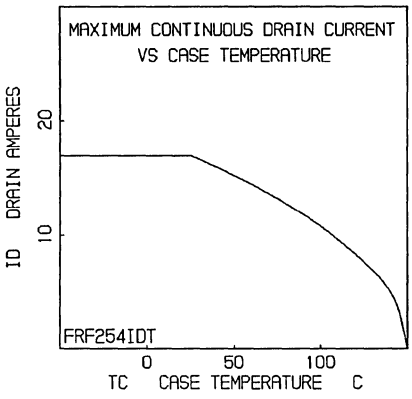
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

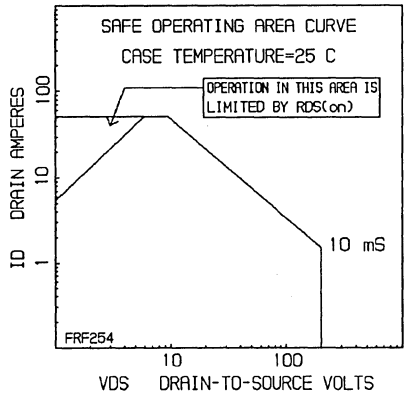
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7296D, R	VGS = 0, ID = 1mA	250	-	V
	(Note 5, 6)	BVDSS	2N7296H	VGS = 0, ID = 1mA	238	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7296D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7296H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7296D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7296H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7296D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7296H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7296D, R	VGS = 0, VDS = 200V	-	25	µA
	(Note 5, 6)	IDSS	2N7296H	VGS = 0, VDS = 200V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7296D, R	VGS = 10V, ID = 17A	-	3.30	V
	(Note 1, 5, 6)	VDS(on)	2N7296H	VGS = 16V, ID = 17A	-	4.18	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7296D, R	VGS = 10V, ID = 11A	-	0.185	Ω
	(Note 1, 5, 6)	RDS(on)	2N7296H	VGS = 14V, ID = 11A	-	0.234	Ω

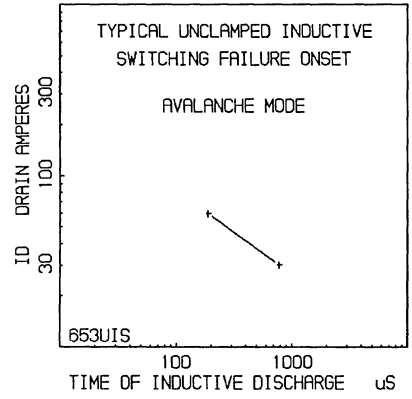
NOTES:

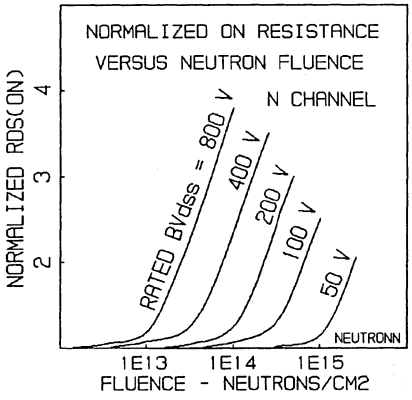
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 1E13
5. Gamma = 1000KRAD(Si). Neutron = 1E13
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 11/1/89 on TA 17653 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

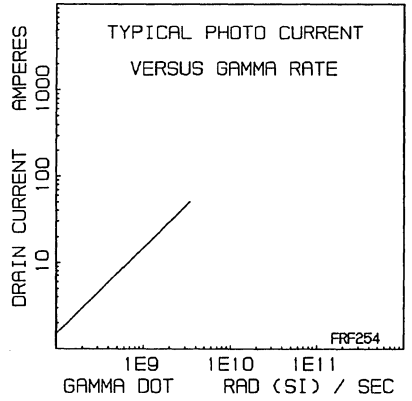
Typical Performance Characteristics

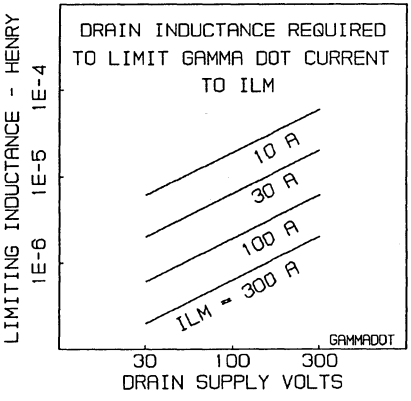












HARRIS SEMICONDUCTOR

2N7297D, 2N7297R 2N7297H

REGISTRATION PENDING
Currently Available as FRM450(D, R, H)
December 1992

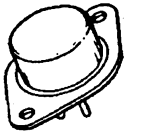
Radiation Hardened N-Channel Power MOSFETs

Features

- 10A, 500V, RDS(on) = 0.600Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 30nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E12 Neutrons/cm^2
  - Usable to 3E13 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Package

TO-204AA



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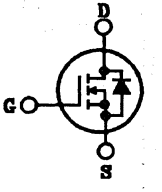


Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7297D, R, H	UNITS
Drain-Source Voltage	VDS	500	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	500	V
Continuous Drain Current			
TC = +25°C	ID	10	A
TC = +100°C	ID	6	A
Pulsed Drain Current	IDM	30	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	150	W
TC = +100°C	PT	60	W
Derated Above +25°C		1.20	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	30	A
Continuous Source Current (Body Diode)	IS	10	A
Pulsed Source Current (Body Diode)	ISM	30	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3236**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	500	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 500V, VGS = 0 VDS = 400V, VGS = 0 VDS = 400V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	30	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 10A	-	6.30	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 6A	-	0.600	Ω
Turn-On Delay Time	td(on)	VDD = 250V, ID = 10A	-	160	ns
Rise Time	tr	Pulse Width = 3µs	-	260	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	750	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	180	
Gate-Charge Threshold	QG(th)	VDD =250V, ID = 10A IGS1 = IGS2 0 ≤ VGS ≤ 20	4	18	nc
Gate-Charge On State	QG(on)		64	258	
Gate-Charge Total	QGM		125	502	
Plateau Voltage	VGP		3	14	V
Gate-Charge Source	QGS		8	34	nc
Gate-Charge Drain	QGD		30	123	
Diode Forward Voltage	VSD	ID = 10A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 10A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	Rθjc		-	0.83	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	30	

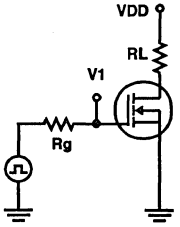


FIGURE 1. SWITCHING TIME TESTING

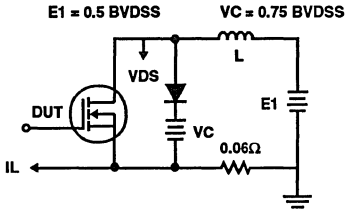


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

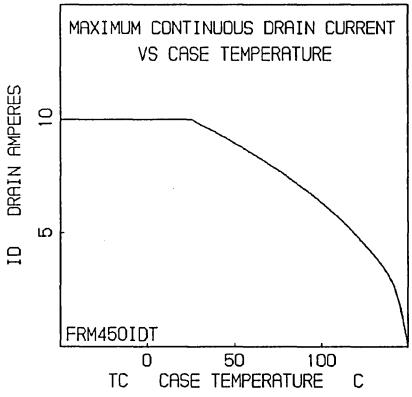
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

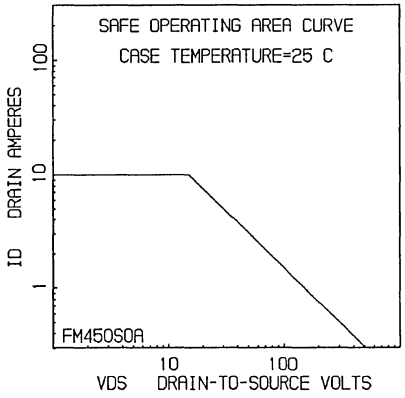
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS		UNITS
					MIN	MAX	
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7297D, R	VGS = 0, ID = 1mA	500	-	V
	(Note 5, 6)	BVDSS	2N7297H	VGS = 0, ID = 1mA	475	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7297D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7297H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7297D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7297H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7297D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7297H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7297D, R	VGS = 0, VDS = 400V	-	25	µA
	(Note 5, 6)	IDSS	2N7297H	VGS = 0, VDS = 400V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7297D, R	VGS = 10V, ID = 10A	-	6.3	V
	(Note 1, 5, 6)	VDS(on)	2N7297H	VGS = 16V, ID = 10A	-	9.0	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7297D, R	VGS = 10V, ID = 6A	-	0.600	Ω
	(Note 1, 5, 6)	RDS(on)	2N7297H	VGS = 14V, ID = 6A	-	0.860	Ω

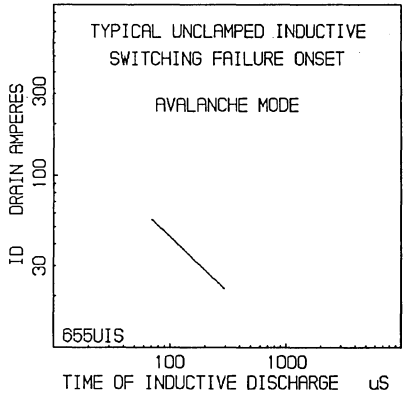
NOTES:

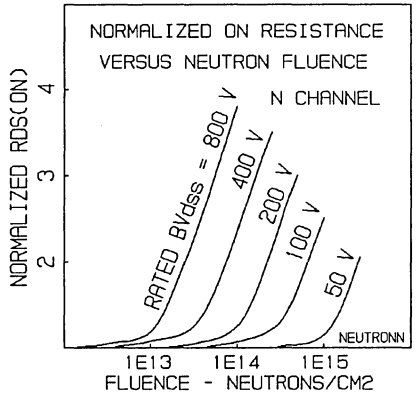
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 3E12
5. Gamma = 1000KRAD(Si). Neutron = 3E12
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 12/18/89 on TA 17655 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

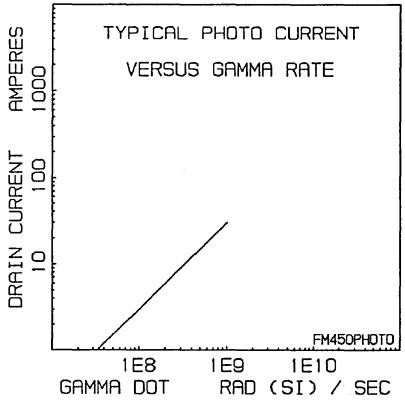
Typical Performance Characteristics

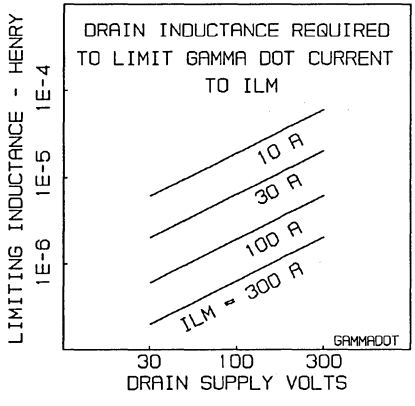












HARRIS SEMICONDUCTOR

2N7298D, 2N7298R 2N7298H

REGISTRATION PENDING
Currently Available as FRF450(D, R, H)
December 1992

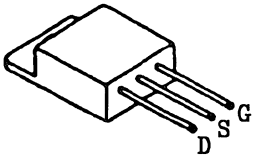
Radiation Hardened N-Channel Power MOSFETs

Features

- 9A, 500V, RDS(on) = 0.615Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 30.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E12 Neutrons/cm^2
  - Usable to 3E13 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Package

TO-254AA



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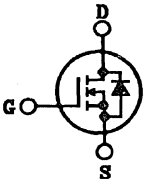


Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm$_2$ for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n^0) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7298D, R, H	UNITS
Drain-Source Voltage	VDS	500	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	500	V
Continuous Drain Current			
TC = +25°C	ID	9	A
TC = +100°C	ID	6	A
Pulsed Drain Current	IDM	27	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	125	W
TC = +100°C	PT	50	W
Derated Above +25°C		1.00	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	27	A
Continuous Source Current (Body Diode)	IS	9	A
Pulsed Source Current (Body Diode)	ISM	27	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3237**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	500	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 500V, VGS = 0 VDS = 400V, VGS = 0 VDS = 400V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	27	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 9A	-	5.81	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 6A	-	0.615	Ω
Turn-On Delay Time	td(on)	VDD = 250V, ID = 9A	-	148	ns
Rise Time	tr	Pulse Width = 3µs	-	196	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	800	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	180	
Gate-Charge Threshold	QG(th)	VDD = 250V, ID = 9A IGS1 = IGS2 0 ≤ VGS ≤ 20	4	16	nc
Gate-Charge On State	QG(on)		66	264	
Gate-Charge Total	QGM		121	486	
Plateau Voltage	VGP		3	12	V
Gate-Charge Source	QGS		14	56	nc
Gate-Charge Drain	QGD		31	126	
Diode Forward Voltage	VSD	ID = 9A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 9A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	Rθjc		-	1.0	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	48	

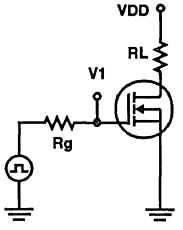


FIGURE 1. SWITCHING TIME TESTING

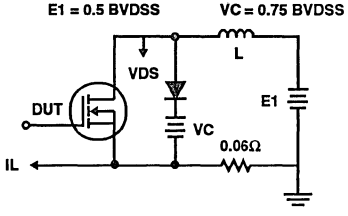


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

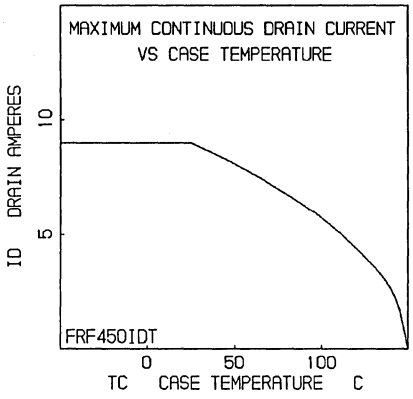
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

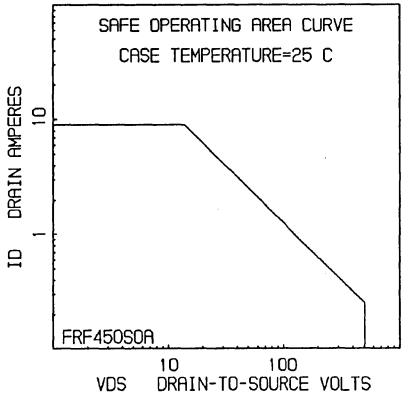
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7298D, R	VGS = 0, ID = 1mA	500	-	V
	(Note 5, 6)	BVDSS	2N7298H	VGS = 0, ID = 1mA	475	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7298D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7298H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7298D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7298H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7298D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7298H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7298D, R	VGS = 0, VDS = 400V	-	25	μA
	(Note 5, 6)	IDSS	2N7298H	VGS = 0, VDS = 400V	-	100	μA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7298D, R	VGS = 10V, ID = 9A	-	5.81	V
	(Note 1, 5, 6)	VDS(on)	2N7298H	VGS = 16V, ID = 9A	-	8.30	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7298D, R	VGS = 10V, ID = 6A	-	0.615	Ω
	(Note 1, 5, 6)	RDS(on)	2N7298H	VGS = 14V, ID = 6A	-	0.879	Ω

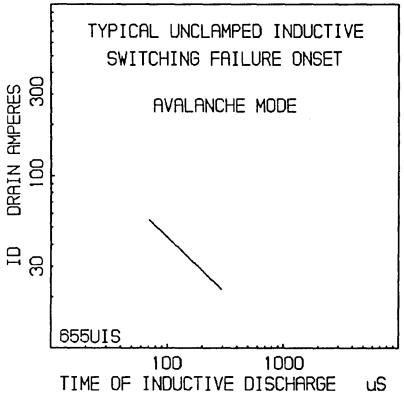
NOTES:

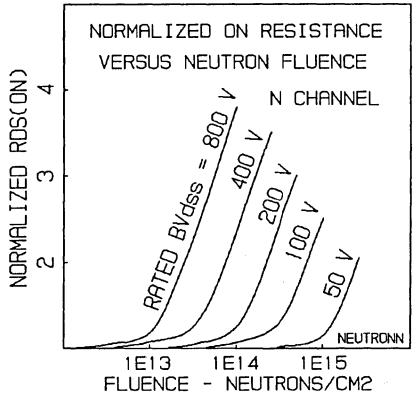
1. Pulse test, 300μs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 3E12
5. Gamma = 1000KRAD(Si). Neutron = 3E12
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 12/18/89 on TA 17655 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

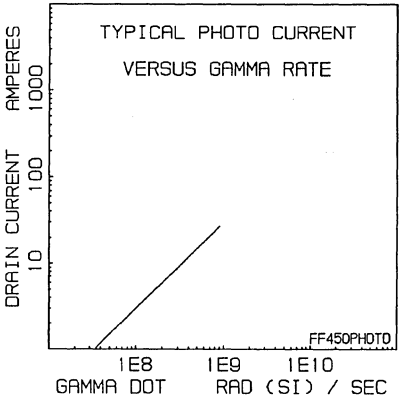
Typical Performance Characteristics

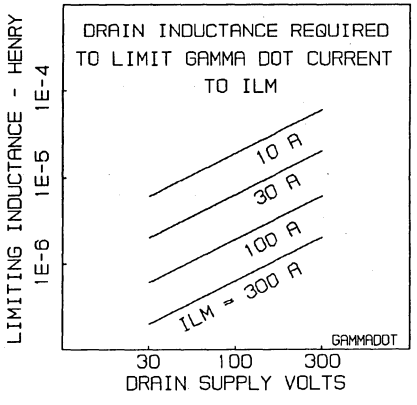












HARRIS SEMICONDUCTOR

2N7299D, 2N7299R 2N7299H

REGISTRATION PENDING
Currently Available as FRK160(D, R, H)
December 1992

Radiation Hardened N-Channel Power MOSFETs

Features

- 50A, 100V, RDS(on) = 0.040Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 10.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E13 Neutrons/cm^2
  - Usable to 3E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

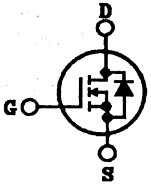
This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-204AE

Symbol



Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7299D, R, H	UNITS
Drain-Source Voltage	VDS	100	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	100	V
Continuous Drain Current			
TC = +25°C	ID	50	A
TC = +100°C	ID	42	A
Pulsed Drain Current	IDM	100	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	300	W
TC = +100°C	PT	120	W
Derated Above +25°C		2.40	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	100	A
Continuous Source Current (Body Diode)	IS	50	A
Pulsed Source Current (Body Diode)	ISM	100	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3222**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	100	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 100V, VGS = 0 VDS = 80V, VGS = 0 VDS = 80V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	100	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 50A	-	2.10	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 42A	-	0.040	Ω
Turn-On Delay Time	td(on)	VDD = 50V, ID = 50A	-	150	ns
Rise Time	tr	Pulse Width = 3µs	-	900	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 10Ω	-	700	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	500	
Gate-Charge Threshold	QG(th)	VDD = 50V, ID = 50A IGS1 = IGS2 0 ≤ VGS ≤ 20	6	24	nc
Gate-Charge On State	QG(on)		82	330	
Gate-Charge Total	QGM		176	704	
Plateau Voltage	VGP		4	18	V
Gate-Charge Source	QGS		27	108	nc
Gate-Charge Drain	QGD		44	176	
Diode Forward Voltage	VSD	ID = 50A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 50A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	Rθjc		-	0.42	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	30	

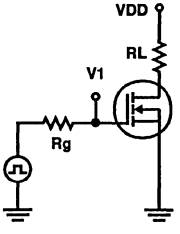


FIGURE 1. SWITCHING TIME TESTING

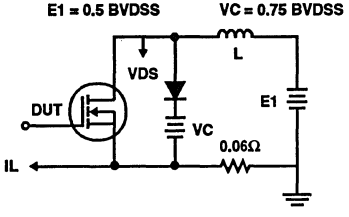


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

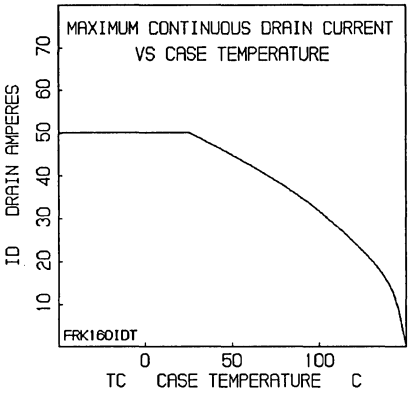
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

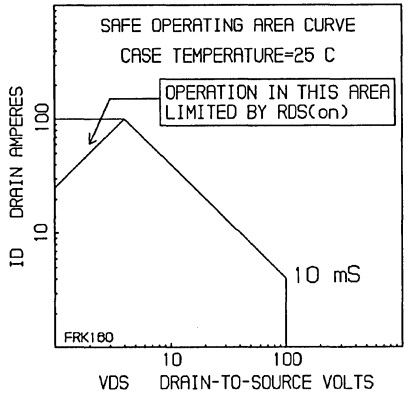
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS		UNITS
					MIN	MAX	
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7299D, R	VGS = 0, ID = 1mA	100	-	V
	(Note 5, 6)	BVDSS	2N7299H	VGS = 0, ID = 1mA	95	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7299D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7299H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7299D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7299H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7299D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7299H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7299D, R	VGS = 0, VDS = 80V	-	25	µA
	(Note 5, 6)	IDSS	2N7299H	VGS = 0, VDS = 80V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7299D, R	VGS = 10V, ID = 50A	-	2.10	V
	(Note 1, 5, 6)	VDS(on)	2N7299H	VGS = 16V, ID = 50A	-	3.15	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7299D, R	VGS = 10V, ID = 42A	-	0.040	Ω
	(Note 1, 5, 6)	RDS(on)	2N7299H	VGS = 14V, ID = 42A	-	0.060	Ω

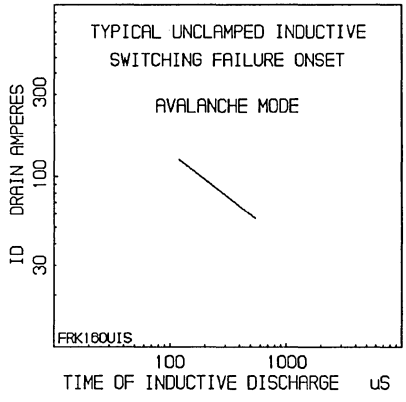
NOTES:

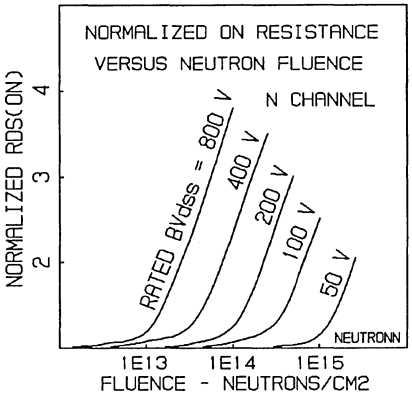
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 3E13
5. Gamma = 1000KRAD(Si). Neutron = 3E13
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 6/11/89 on TA 17661 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

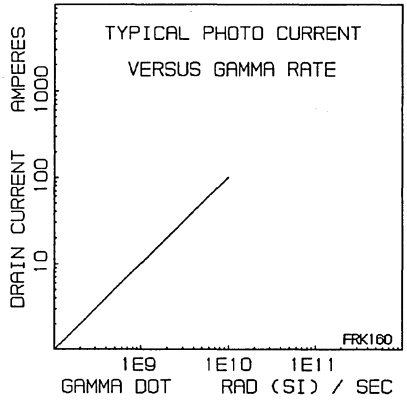
Typical Performance Characteristics

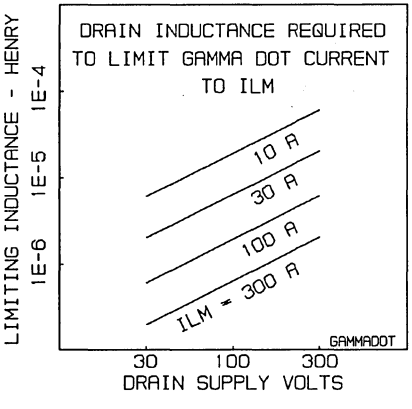












HARRIS SEMICONDUCTOR

2N7300D, 2N7300R 2N7300H

PRELIMINARY REGISTRATION PENDING
Currently Available as FRE160(D, R, H)

January 1993

Radiation Hardened N-Channel Power MOSFETs

Features

- 41A, 100V, RDS(on) = 0.050Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 10nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E13 Neutrons/cm^2
  - Usable to 3E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

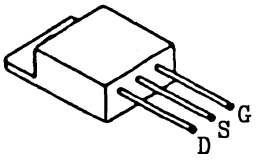
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-258



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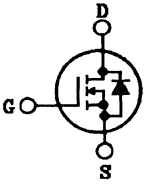


Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7300D, R, H	UNITS
Drain-Source Voltage	VDS	100	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	100	V
Continuous Drain Current			
TC = +25°C	ID	41	A
TC = +100°C	ID	26	A
Pulsed Drain Current	IDM	100	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	150	W
TC = +100°C	PT	60	W
Derated Above +25°C		1.20	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	100	A
Continuous Source Current (Body Diode)	IS	41	A
Pulsed Source Current (Body Diode)	ISM	100	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3258**

HARRIS SEMICONDUCTOR

2N7301D, 2N7301R 2N7301H

REGISTRATION PENDING
Currently Available as FRK260(D, R, H)
December 1992

Radiation Hardened N-Channel Power MOSFETs

Features

- 46A, 200V, RDS(on) = 0.070Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 18.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

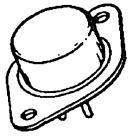
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness.(GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-204AE



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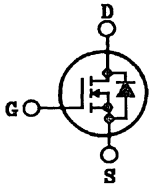


Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7301D, R, H	UNITS
Drain-Source Voltage	VDS	200	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	200	V
Continuous Drain Current			
TC = +25°C	ID	46	A
TC = +100°C	ID	29	A
Pulsed Drain Current	IDM	100	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	300	W
TC = +100°C	PT	120	W
Derated Above +25°C		2.40	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	100	A
Continuous Source Current (Body Diode)	IS	46	A
Pulsed Source Current (Body Diode)	ISM	100	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3228**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	200	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 200V, VGS = 0 VDS = 160V, VGS = 0 VDS = 160V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	100	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 46A	-	3.38	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 29A	-	0.070	Ω
Turn-On Delay Time	td(on)	VDD = 100V, ID = 46A	-	150	ns
Rise Time	tr	Pulse Width = 3µs	-	800	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 10Ω	-	700	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	500	
Gate-Charge Threshold	QG(th)	VDD = 100V, ID = 46A IGS1 = IGS2 0 ≤ VGS ≤ 20	6	24	nc
Gate-Charge On State	QG(on)		88	352	
Gate-Charge Total	QGM		171	686	
Plateau Voltage	VGP		3	14	V
Gate-Charge Source	QGS		21	84	nc
Gate-Charge Drain	QGD		43	172	
Diode Forward Voltage	VSD	ID =46A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 46A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	Rθjc		-	0.42	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	30	

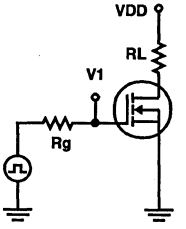


FIGURE 1. SWITCHING TIME TESTING

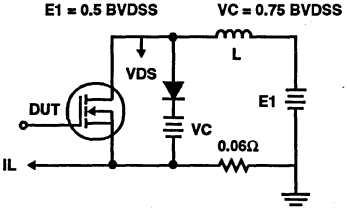


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

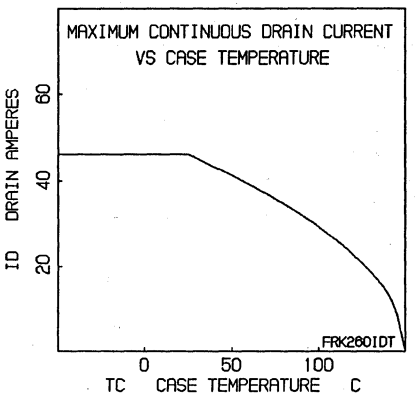
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

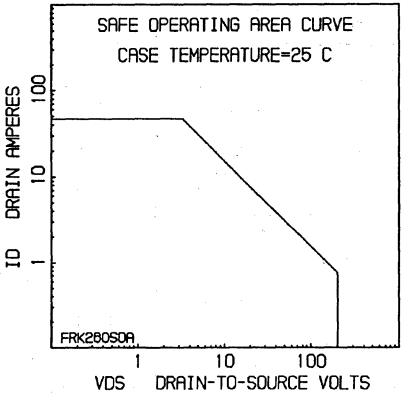
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7301D, R	VGS = 0, ID = 1mA	200	-	V
	(Note 5, 6)	BVDSS	2N7301H	VGS = 0, ID = 1mA	190	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7301D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7301H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7301D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7301H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7301D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7301H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7301D, R	VGS = 0, VDS = 160V	-	25	µA
	(Note 5, 6)	IDSS	2N7301H	VGS = 0, VDS = 160V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7301D, R	VGS = 10V, ID = 46A	-	3.38	V
	(Note 1, 5, 6)	VDS(on)	2N7301H	VGS = 16V, ID = 46A	-	5.07	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7301D, R	VGS = 10V, ID = 29A	-	0.070	Ω
	(Note 1, 5, 6)	RDS(on)	2N7301H	VGS = 14V, ID = 29A	-	0.105	Ω

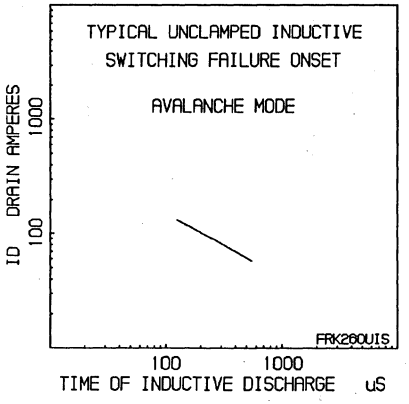
NOTES:

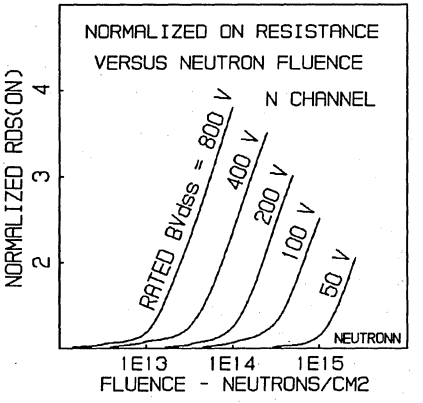
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 1E13
5. Gamma = 1000KRAD(Si). Neutron = 1E13
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 11/2/90 on TA 17662 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

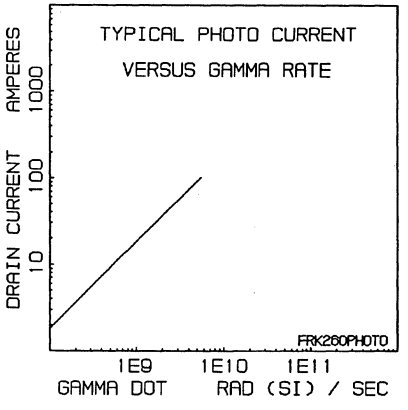
Typical Performance Characteristics

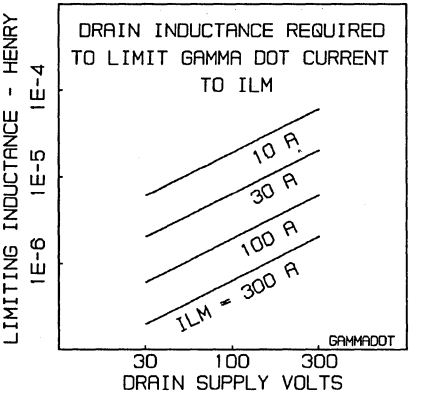












HARRIS SEMICONDUCTOR

2N7302D, 2N7302R 2N7302H

PRELIMINARY REGISTRATION PENDING
Currently Available as FRE260(D, R, H)
January 1993

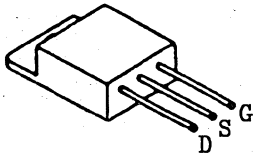
Radiation Hardened N-Channel Power MOSFETs

Features

- 31A, 200V, RDS(on) = 0.080Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 18.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Package

TO-258



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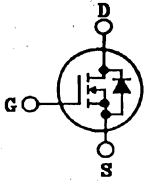


Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7302D, R, H	UNITS
Drain-Source Voltage	VDS	200	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	200	V
Continuous Drain Current			
TC = +25°C	ID	31	A
TC = +100°C	ID	19	A
Pulsed Drain Current	IDM	93	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	150	W
TC = +100°C	PT	60	W
Derated Above +25°C		1.20	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	93	A
Continuous Source Current (Body Diode)	IS	31	A
Pulsed Source Current (Body Diode)	ISM	93	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3259**

HARRIS SEMICONDUCTOR

2N7303D, 2N7303R 2N7303H

Radiation Hardened N-Channel Power MOSFETs

REGISTRATION PENDING
Currently Available as FRK264(D, R, H)
December 1992

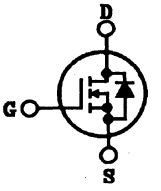
Features

- 34A, 250V, RDS(on) = 0.120Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 22.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Package

TO-204AE

Symbol



Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7303D, R, H	UNITS
Drain-Source Voltage	VDS	250	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	250	V
Continuous Drain Current			
TC = +25°C	ID	34	A
TC = +100°C	ID	21	A
Pulsed Drain Current	IDM	100	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	300	W
TC = +100°C	PT	120	W
Derated Above +25°C		2.40	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	100	A
Continuous Source Current (Body Diode)	IS	34	A
Pulsed Source Current (Body Diode)	ISM	100	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3233**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	250	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 250V, VGS = 0 VDS = 200V, VGS = 0 VDS = 200V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	100	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 34A	-	4.28	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 21A	-	0.120	Ω
Turn-On Delay Time	td(on)	VDD = 125V, ID = 34A	-	150	ns
Rise Time	tr	Pulse Width = 3µs	-	800	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 10Ω	-	700	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	500	
Gate-Charge Threshold	QG(th)	VDD = 125V, ID = 34A IGS1 = IGS2 0 ≤ VGS ≤ 20	6	28	nc
Gate-Charge On State	QG(on)		93	372	
Gate-Charge Total	QGM		188	754	
Plateau Voltage	VGP		3	16	V
Gate-Charge Source	QGS		27	110	nc
Gate-Charge Drain	QGD		44	178	
Diode Forward Voltage	VSD	ID = 34A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 34A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	Rθjc		-	0.42	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	30	

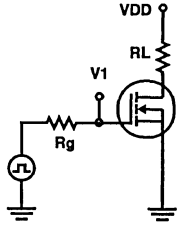


FIGURE 1. SWITCHING TIME TESTING

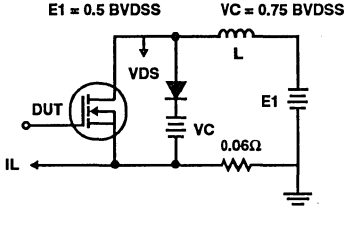


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

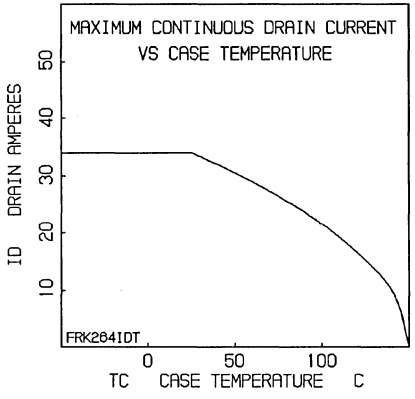
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

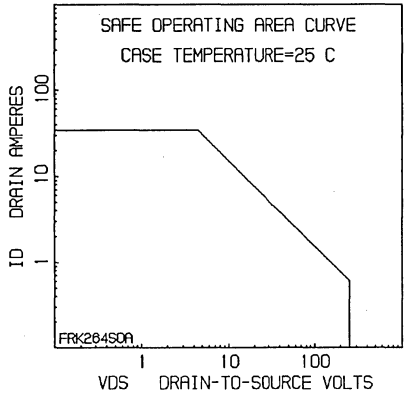
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7303D, R	VGS = 0, ID = 1mA	250	-	V
	(Note 5, 6)	BVDSS	2N7303H	VGS = 0, ID = 1mA	238	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7303D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7303H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7303D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7303H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7303D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7303H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7303D, R	VGS = 0, VDS = 200V	-	25	µA
	(Note 5, 6)	IDSS	2N7303H	VGS = 0, VDS = 200V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7303D, R	VGS = 10V, ID = 34A	-	4.28	V
	(Note 1, 5, 6)	VDS(on)	2N7303H	VGS = 16V, ID = 34A	-	6.43	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7303D, R	VGS = 10V, ID = 21A	-	0.120	Ω
	(Note 1, 5, 6)	RDS(on)	2N7303H	VGS = 14V, ID = 21A	-	0.180	Ω

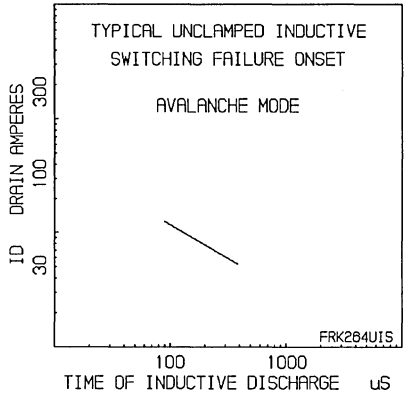
NOTES:

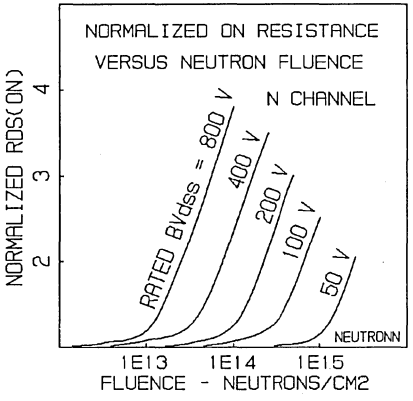
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 1E13
5. Gamma = 1000KRAD(Si). Neutron = 1E13
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 6/15/90 on TA 17663 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

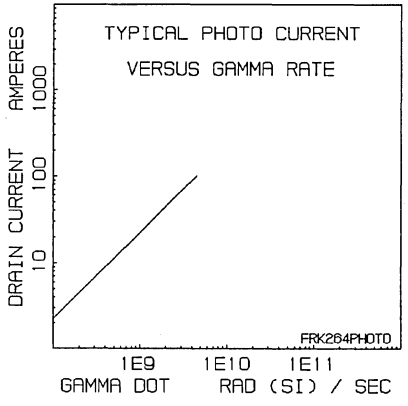
Typical Performance Characteristics

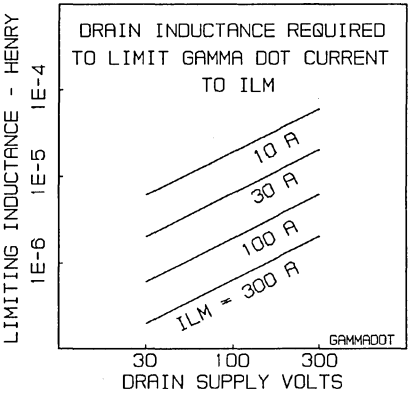












HARRIS SEMICONDUCTOR

2N7304D, 2N7304R 2N7304H

PRELIMINARY REGISTRATION PENDING
Currently Available as FRE264(D, R, H)

January 1993

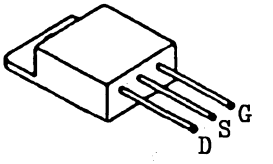
Radiation Hardened N-Channel Power MOSFETs

Features

- 23A, 250V, RDS(on) = 0.130Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 22.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Package

TO-258



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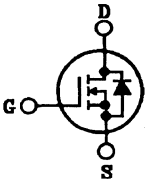


Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n^0) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7304D, R, H	UNITS
Drain-Source Voltage	VDS	250	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	250	V
Continuous Drain Current			
TC = +25°C	ID	23	A
TC = +100°C	ID	15	A
Pulsed Drain Current	IDM	69	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	150	W
TC = +100°C	PT	60	W
Derated Above +25°C		1.20	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	69	A
Continuous Source Current (Body Diode)	IS	23	A
Pulsed Source Current (Body Diode)	ISM	69	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3260

HARRIS SEMICONDUCTOR

2N7305D, 2N7305R 2N7305H

REGISTRATION PENDING
Currently Available as FRK460(D, R, H)
December 1992

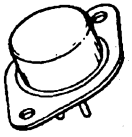
Radiation Hardened N-Channel Power MOSFETs

Features

- 17A, 500V, RDS(on) = 0.400Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 45.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E12 Neutrons/cm^2
  - Usable to 3E13 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Package

TO-204AE



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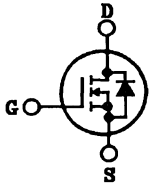


Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n^0) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7305D, R, H	UNITS
Drain-Source Voltage	VDS	500	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	500	V
Continuous Drain Current			
TC = +25°C	ID	17	A
TC = +100°C	ID	11	A
Pulsed Drain Current	IDM	51	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	300	W
TC = +100°C	PT	120	W
Derated Above +25°C		2.40	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	51	A
Continuous Source Current (Body Diode)	IS	17	A
Pulsed Source Current (Body Diode)	ISM	51	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3238**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	500	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 500V, VGS = 0 VDS = 400V, VGS = 0 VDS = 400V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	51	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 17A	-	7.14	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 11A	-	0.400	Ω
Turn-On Delay Time	td(on)	VDD = 250V, ID = 17A	-	150	ns
Rise Time	tr	Pulse Width = 3µs	-	800	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 10Ω	-	700	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	500	
Gate-Charge Threshold	QG(th)	VDD = 250V, ID = 17A IGS1 = IGS2 0 ≤ VGS ≤ 20	6	26	nc
Gate-Charge On State	QG(on)		97	390	
Gate-Charge Total	QGM		189	758	
Plateau Voltage	VGP		3	14	V
Gate-Charge Source	QGS		23	92	nc
Gate-Charge Drain	QGD		47	188	
Diode Forward Voltage	VSD	ID = 17A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 17A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	Rθjc		-	0.42	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	30	

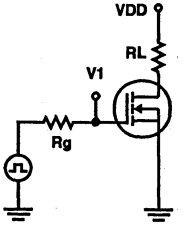


FIGURE 1. SWITCHING TIME TESTING

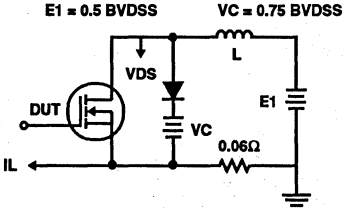


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

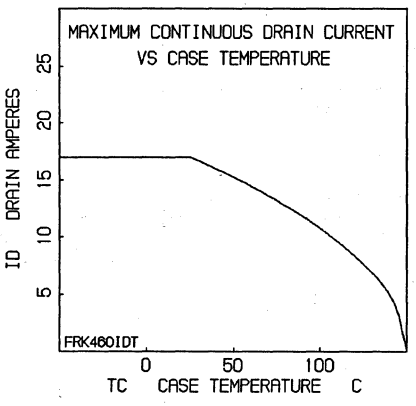
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

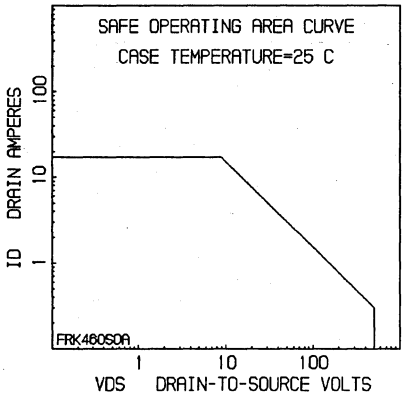
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7305D, R	VGS = 0, ID = 1mA	500	-	V
	(Note 5, 6)	BVDSS	2N7305H	VGS = 0, ID = 1mA	475	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7305D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7305H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7305D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7305H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7305D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7305H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7305D, R	VGS = 0, VDS = 400V	-	25	µA
	(Note 5, 6)	IDSS	2N7305H	VGS = 0, VDS = 400V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7305D, R	VGS = 10V, ID = 17A	-	7.14	V
	(Note 1, 5, 6)	VDS(on)	2N7305H	VGS = 16V, ID = 17A	-	10.71	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7305D, R	VGS = 10V, ID = 11A	-	0.400	Ω
	(Note 1, 5, 6)	RDS(on)	2N7305H	VGS = 14V, ID = 11A	-	0.600	Ω

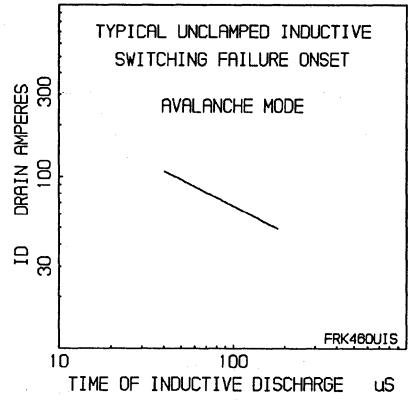
NOTES:

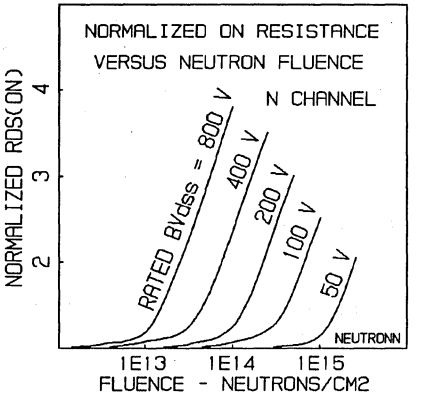
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 3E12
5. Gamma = 1000KRAD(Si). Neutron = 3E12
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 11/14/90 on TA 17665 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

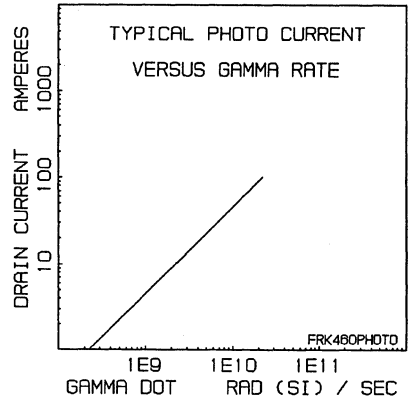
Typical Performance Characteristics

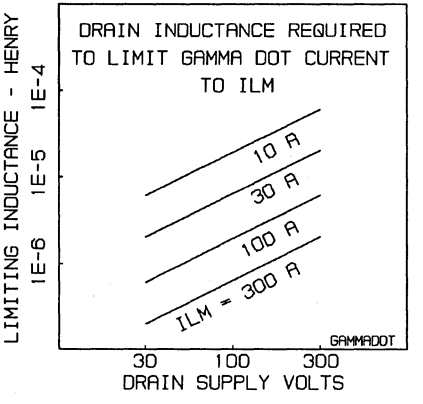












HARRIS SEMICONDUCTOR

2N7306D, 2N7306R 2N7306H

PRELIMINARY REGISTRATION PENDING
Currently Available as FRE460(D, R, H)

January 1993

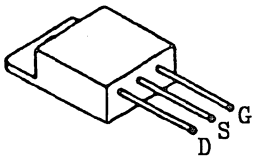
Radiation Hardened N-Channel Power MOSFETs

Features

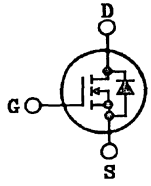
- 12A, 500V, RDS(on) = 0.410Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 45.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E12 Neutrons/cm^2
  - Usable to 3E13 Neutrons/cm^2
- Single Event - Typically Survives 1E5ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Package

TO-258



Symbol



Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7306D, R, H	UNITS
Drain-Source Voltage	VDS	500	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	500	V
Continuous Drain Current			
TC = +25°C	ID	12	A
TC = +100°C	ID	7	A
Pulsed Drain Current	IDM	36	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	150	W
TC = +100°C	PT	60	W
Derated Above +25°C		1.20	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	36	A
Continuous Source Current (Body Diode)	IS	12	A
Pulsed Source Current (Body Diode)	ISM	36	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3261**

HARRIS SEMICONDUCTOR

2N7307D, 2N7307R 2N7307H

REGISTRATION PENDING
Currently Available as FRM9130 (D, R, H)
December 1992

Radiation Hardened P-Channel Power MOSFETs

Features

- 6A, -100V, RDS(on) = 0.550Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 1.50nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E13 Neutrons/cm^2
  - Usable to 3E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

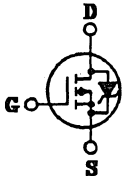
This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-204AA

Symbol



Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7307D, R, H	UNITS
Drain-Source Voltage	VDS	-100	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	-100	V
Continuous Drain Current			
TC = +25°C	ID	6	A
TC = +100°C	ID	4	A
Pulsed Drain Current	IDM	18	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	75	W
TC = +100°C	PT	30	W
Derated Above +25°C		0.60	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	18	A
Continuous Source Current (Body Diode)	IS	6	A
Pulsed Source Current (Body Diode)	ISM	18	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3262**

HARRIS SEMICONDUCTOR

2N7308D, 2N7308R 2N7308H

Radiation Hardened P-Channel Power MOSFETs

REGISTRATION PENDING
Currently Available as FRL9130(D, R, H)
December 1992

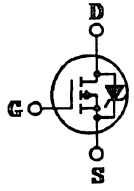
Features

- 5A, -100V, RDS(on) = 0.550Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 1.50nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E13 Neutrons/cm^2
  - Usable to 3E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Package

TO-205AF

Symbol



Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7308D, R, H	UNITS
Drain-Source Voltage	VDS	-100	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	-100	V
Continuous Drain Current			
TC = +25°C	ID	5	A
TC = +100°C	ID	3	A
Pulsed Drain Current	IDM	15	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	25	W
TC = +100°C	PT	10	W
Derated Above +25°C		0.20	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	15	A
Continuous Source Current (Body Diode)	IS	5	A
Pulsed Source Current (Body Diode)	ISM	15	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3239

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	-100	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	-2.0	-4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = -20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = +20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = -100V, VGS = 0 VDS = -80V, VGS = 0 VDS = -80V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	15	A
Drain-Source On-State Volts	VDS(on)	VGS = -10V, ID = 5A	-	-2.89	V
Drain-Source On Resistance	RDS(on)	VGS = -10V, ID =3A	-	0.55	Ω
Turn-On Delay Time	td(on)	VDD = -50V, ID = 5A	-	56	ns
Rise Time	tr	Pulse Width = 3µs	-	124	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	126	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	78	
Gate-Charge Threshold	QG(th)	VDD = -50V, ID = 5A IGS1 = IGS2 0 ≤ VGS ≤ 20	1	4	nc
Gate-Charge On State	QG(on)		15	60	
Gate-Charge Total	QGM		31	124	
Plateau Voltage	VGP		-3	-12	V
Gate-Charge Source	QGS		3	15	nc
Gate-Charge Drain	QGD		5	22	
Diode Forward Voltage	VSD	ID =5A, VGD = 0	-0.6	-1.8	V
Reverse Recovery Time	TT	I = 5A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	Rθjc		-	5.0	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	175	

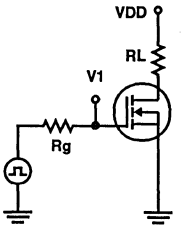


FIGURE 1. SWITCHING TIME TESTING

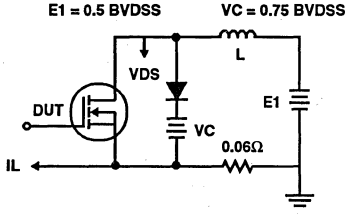


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

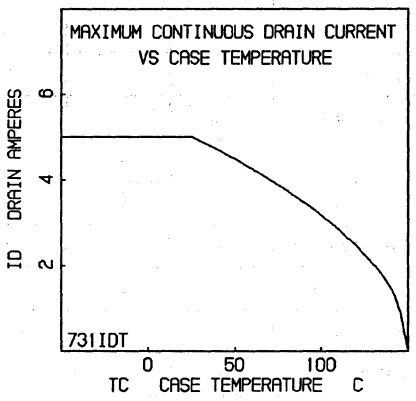
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

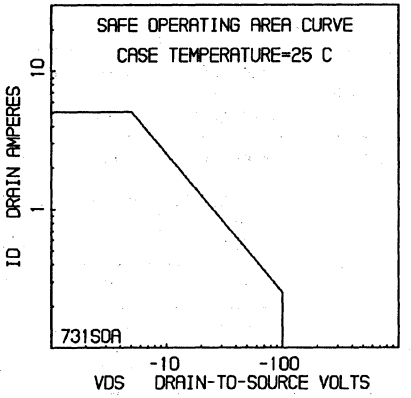
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7308D, R	VGS = 0, ID = 1mA	-100	-	V
	(Note 5, 6)	BVDSS	2N7308H	VGS = 0, ID = 1mA	-95	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7308D, R	VGS = VDS, ID = 1mA	-2.0	-4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7308H	VGS = VDS, ID = 1mA	-2.0	-6.0	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7308D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7308H	VGS = -20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7308D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7308H	VGS = 20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7308D, R	VGS = 0, VDS = -80V	-	25	µA
	(Note 5, 6)	IDSS	2N7308H	VGS = 0, VDS = -80V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7308D, R	VGS = -10V, ID = 5A	-	-2.89	V
	(Note 1, 5, 6)	VDS(on)	2N7308H	VGS = -16V, ID = 5A	-	-4.34	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7308D, R	VGS = -10V, ID = 3A	-	0.550	Ω
	(Note 1, 5, 6)	RDS(on)	2N7308H	VGS = -14V, ID = 3A	-	0.830	Ω

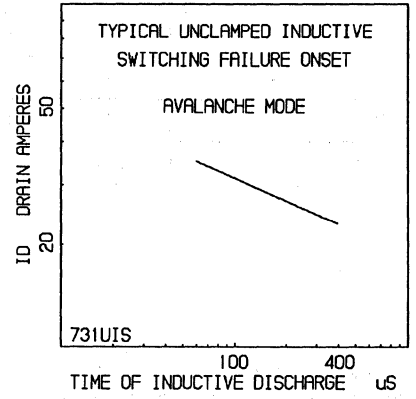
NOTES:

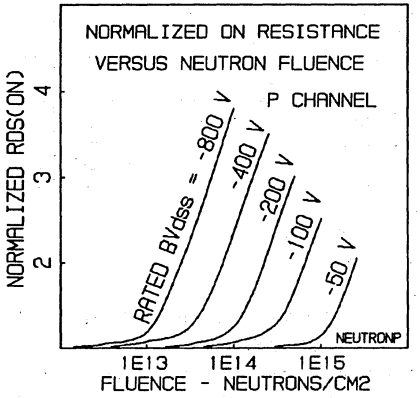
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 3E13
5. Gamma = 1000KRAD(Si). Neutron = 3E13
6. Insitu Gamma bias must be sampled for both VGS = -10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 12/19/89 on TA 17731 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

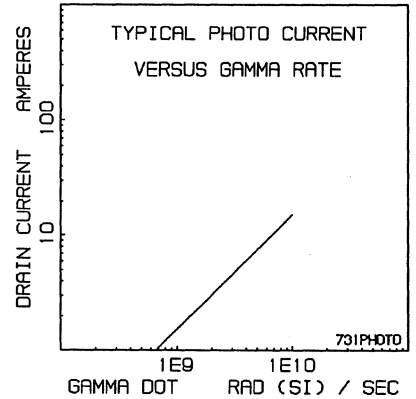
Typical Performance Characteristics

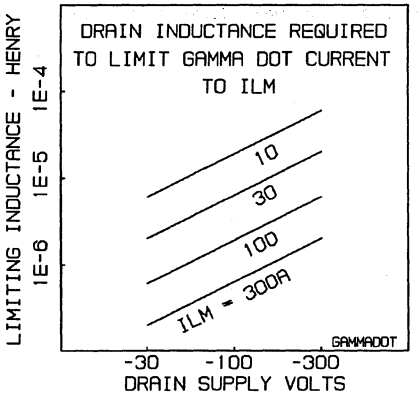












HARRIS SEMICONDUCTOR

2N7309D, 2N7309R 2N7309H

REGISTRATION PENDING
Currently Available as FRS9130(D, R, H)
December 1992

Radiation Hardened P-Channel Power MOSFETs

Features

- 6A, -100V, RDS(on) = 0.565Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 1.50nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E13 Neutrons/cm^2
  - Usable to 3E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

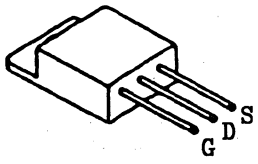
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

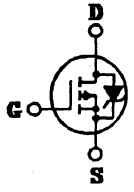
This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-257AA



Symbol



Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7309D, R, H	UNITS
Drain-Source Voltage	VDS	-100	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	-100	V
Continuous Drain Current			
TC = +25°C	ID	6	A
TC = +100°C	ID	4	A
Pulsed Drain Current	IDM	18	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	50	W
TC = +100°C	PT	20	W
Derated Above +25°C		0.40	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	18	A
Continuous Source Current (Body Diode)	IS	6	A
Pulsed Source Current (Body Diode)	ISM	18	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3240**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	-100	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	-2.0	-4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = -20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = +20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = -100V, VGS = 0 VDS = -80V, VGS = 0 VDS = -80V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	18	A
Drain-Source On-State Volts	VDS(on)	VGS = -10V, ID = 6A	-	-3.56	V
Drain-Source On Resistance	RDS(on)	VGS = -10V, ID = 4A	-	0.565	Ω
Turn-On Delay Time	td(on)	VDD = -50V, ID = 6A	-	38	ns
Rise Time	tr	Pulse Width = 3µs	-	176	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	126	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	74	
Gate-Charge Threshold	QG(th)	VDD = -50V, ID = 6A IGS1 = IGS2 0 ≤ VGS ≤ 20	1	4	nc
Gate-Charge On State	QG(on)		16	66	
Gate-Charge Total	QGM		33	132	
Plateau Voltage	VGP		-3	-12	V
Gate-Charge Source	QGS		3	13	nc
Gate-Charge Drain	QGD		6	26	
Diode Forward Voltage	VSD	ID =6A, VGD = 0	-0.6	-1.8	V
Reverse Recovery Time	TT	I = 6A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	RθJC		-	2.5	°C/W
Junction-To-Ambient	RθJA	Free Air Operation	-	60	

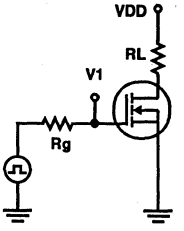


FIGURE 1. SWITCHING TIME TESTING

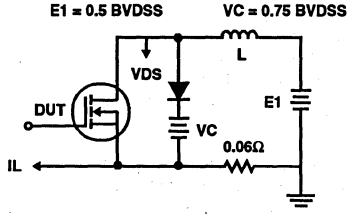


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

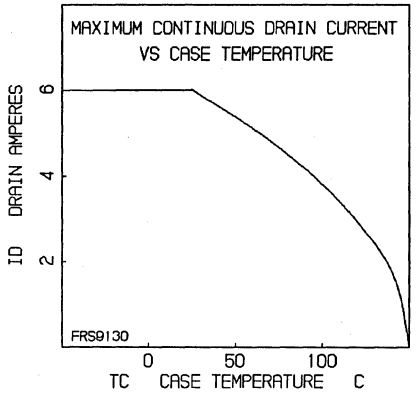
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

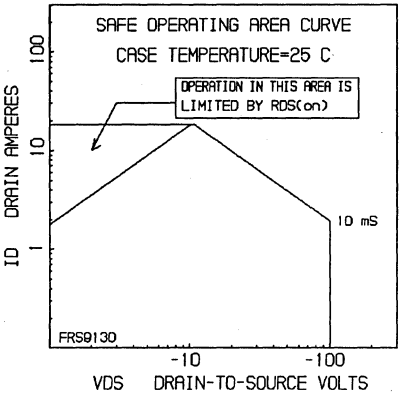
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7309D, R	VGS = 0, ID = 1mA	-100	-	V
	(Note 5, 6)	BVDSS	2N7309H	VGS = 0, ID = 1mA	-95	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7309D, R	VGS = VDS, ID = 1mA	-2.0	-4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7309H	VGS = VDS, ID = 1mA	-2.0	-6.0	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7309D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7309H	VGS = -20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7309D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7309H	VGS = 20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7309D, R	VGS = 0, VDS = -80V	-	25	µA
	(Note 5, 6)	IDSS	2N7309H	VGS = 0, VDS = -80V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7309D, R	VGS = -10V, ID = 6A	-	-3.56	V
	(Note 1, 5, 6)	VDS(on)	2N7309H	VGS = -16V, ID = 6A	-	-5.34	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7309D, R	VGS = -10V, ID = 4A	-	0.565	Ω
	(Note 1, 5, 6)	RDS(on)	2N7309H	VGS = -14V, ID = 4A	-	0.848	Ω

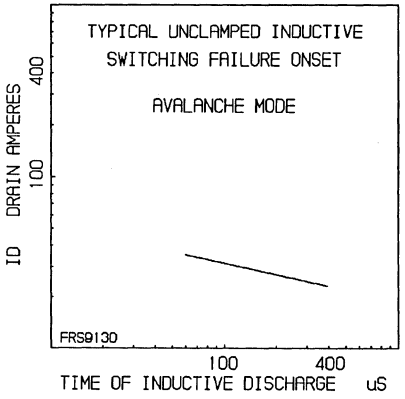
NOTES:

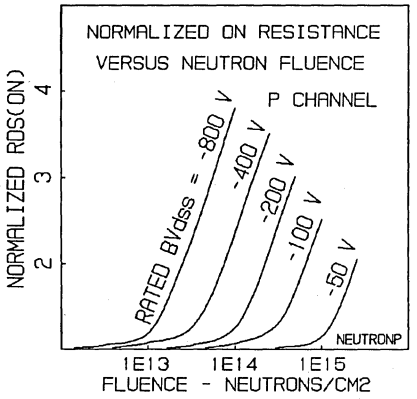
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 3E13
5. Gamma = 1000KRAD(Si). Neutron = 3E13
6. Insitu Gamma bias must be sampled for both VGS = -10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 12/19/89 on TA 17731 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

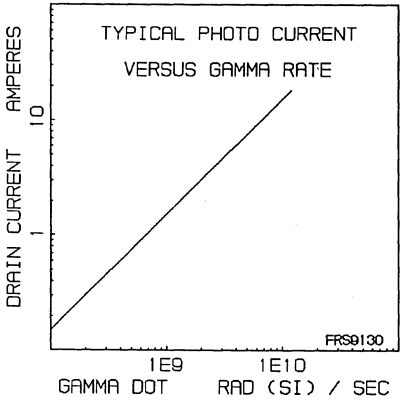
Typical Performance Characteristics

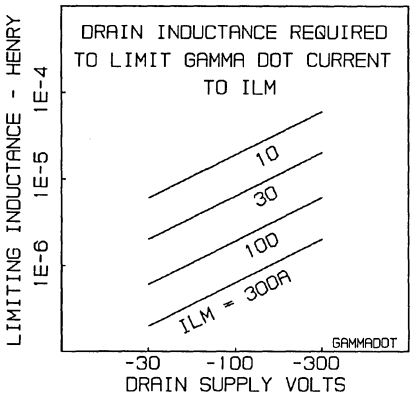












HARRIS SEMICONDUCTOR

2N7310D, 2N7310R 2N7310H

REGISTRATION PENDING
Currently Available as FRM9230 (D, R, H)
December 1992

Radiation Hardened P-Channel Power MOSFETs

Features

- 4A, -200V, RDS(on) = 1.30Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current
  - 3nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event
  - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

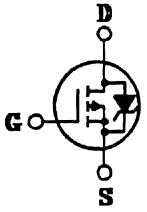
This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-204AA

Symbol



Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7310D, R, H	UNITS
Drain-Source Voltage	VDS	-200	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	-200	V
Continuous Drain Current			
TC = +25°C	ID	4	A
TC = +100°C	ID	2	A
Pulsed Drain Current	IDM	12	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	75	W
TC = +100°C	PT	30	W
Derated Above +25°C		0.60	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	12	A
Continuous Source Current (Body Diode)	IS	4	A
Pulsed Source Current (Body Diode)	ISM	12	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3263

HARRIS SEMICONDUCTOR

2N7311D, 2N7311R 2N7311H

REGISTRATION PENDING
Currently Available as FRL9230(D, R, H)
December 1992

Radiation Hardened P-Channel Power MOSFETs

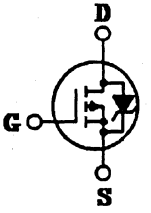
Features

- 3A, -200V, RDS(on) = 1.30Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 3.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Package

TO-205AF

Symbol



Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n^0) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7311D, R, H	UNITS
Drain-Source Voltage	VDS	-200	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	-200	V
Continuous Drain Current			
TC = +25°C	ID	3	A
TC = +100°C	ID	2	A
Pulsed Drain Current	IDM	9	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	25	W
TC = +100°C	PT	10	W
Derated Above +25°C		0.20	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	9	A
Continuous Source Current (Body Diode)	IS	3	A
Pulsed Source Current (Body Diode)	ISM	9	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3245**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	-200	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	-2.0	-4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = -20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = +20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = -200V, VGS = 0 VDS = -160V, VGS = 0 VDS = -160V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	9	A
Drain-Source On-State Volts	VDS(on)	VGS = -10V, ID = 3A	-	-4.1	V
Drain-Source On Resistance	RDS(on)	VGS = -10V, ID = 2A	-	1.3	Ω
Turn-On Delay Time	td(on)	VDD = -100V, ID = 3A	-	58	ns
Rise Time	tr	Pulse Width = 3µs	-	76	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	48	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	54	
Gate-Charge Threshold	QG(th)	VDD = -100V, ID = 3A IGS1 = IGS2 0 ≤ VGS ≤ 20	1	4	nc
Gate-Charge On State	QG(on)		13	52	
Gate-Charge Total	QGM		28	114	
Plateau Voltage	VGP		-3	-12	V
Gate-Charge Source	QGS		4	16	nc
Gate-Charge Drain	QGD		4	16	
Diode Forward Voltage	VSD	ID = 3A, VGD = 0	-0.6	-1.8	V
Reverse Recovery Time	TT	I = 3A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	Rθjc		-	5.0	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	175	

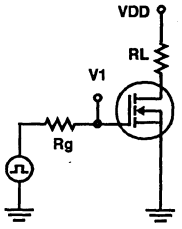


FIGURE 1. SWITCHING TIME TESTING

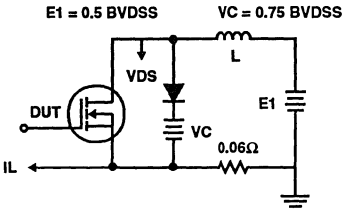


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

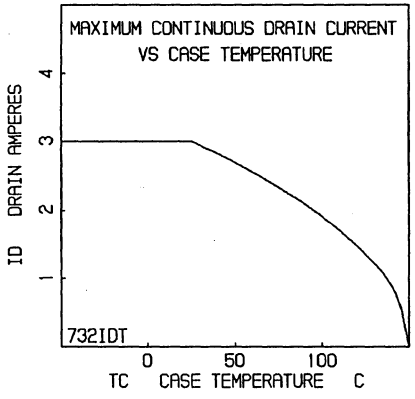
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

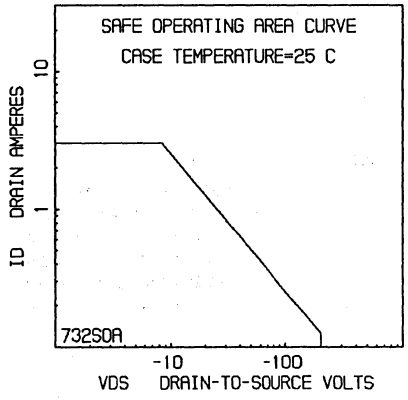
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7311D, R	VGS = 0, ID = 1mA	-200	-	V
	(Note 5, 6)	BVDSS	2N7311H	VGS = 0, ID = 1mA	-190	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7311D, R	VGS = VDS, ID = 1mA	-2.0	-4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7311H	VGS = VDS, ID = 1mA	-2.0	-6.0	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7311D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7311H	VGS = -20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7311D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7311H	VGS = 20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7311D, R	VGS = 0, VDS = -160V	-	25	µA
	(Note 5, 6)	IDSS	2N7311H	VGS = 0, VDS = -160V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7311D, R	VGS = -10V, ID = 3A	-	-4.1	V
	(Note 1, 5, 6)	VDS(on)	2N7311H	VGS = -16V, ID = 3A	-	-6.15	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7311D, R	VGS = -10V, ID = 2A	-	1.30	Ω
	(Note 1, 5, 6)	RDS(on)	2N7311H	VGS = -14V, ID = 2A	-	1.95	Ω

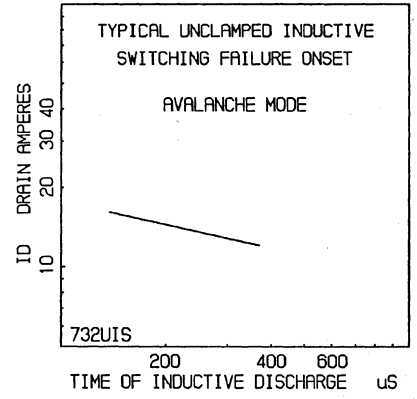
NOTES:

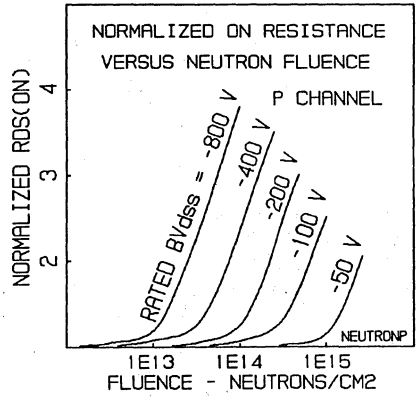
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 1E13
5. Gamma = 1000KRAD(Si). Neutron = 1E13
6. Insitu Gamma bias must be sampled for both VGS = -10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 2/19/90 on TA 17732 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

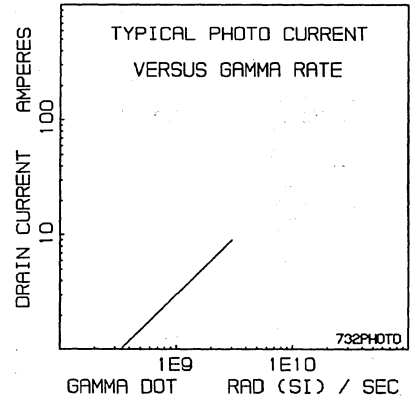
Typical Performance Characteristics

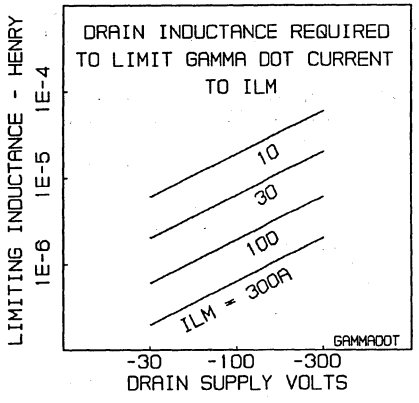












HARRIS SEMICONDUCTOR

2N7312D, 2N7312R 2N7312H

REGISTRATION PENDING
Currently Available as FRS9230(D, R, H)
December 1992

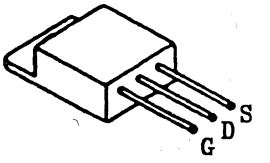
Radiation Hardened P-Channel Power MOSFETs

Features

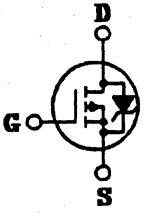
- 4A, -200V, RDS(on) = 1.32Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 3.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Package

TO-257AA



Symbol



Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7312D, R, H	UNITS
Drain-Source Voltage	VDS	-200	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	-200	V
Continuous Drain Current			
TC = +25°C	ID	4	A
TC = +100°C	ID	2	A
Pulsed Drain Current	IDM	12	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	50	W
TC = +100°C	PT	20	W
Derated Above +25°C		0.40	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	12	A
Continuous Source Current (Body Diode)	IS	4	A
Pulsed Source Current (Body Diode)	ISM	12	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3246**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	-200	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	-2.0	-4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = -20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = +20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = -200V, VGS = 0 VDS = -160V, VGS = 0 VDS = -160V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	12	A
Drain-Source On-State Volts	VDS(on)	VGS = -10V, ID = 4A	-	-5.54	V
Drain-Source On Resistance	RDS(on)	VGS = -10V, ID = 2A	-	1.32	Ω
Turn-On Delay Time	td(on)	VDD = -100V, ID = 4A	-	48	ns
Rise Time	tr	Pulse Width = 3µs	-	158	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	111	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	52	
Gate-Charge Threshold	QG(th)	VDD = -100V, ID = 4A IGS1 = IGS2 0 ≤ VGS ≤ 20	1	4	nc
Gate-Charge On State	QG(on)		15	60	
Gate-Charge Total	QGM		31	124	
Plateau Voltage	VGP		-3	-13	V
Gate-Charge Source	QGS		4	16	nc
Gate-Charge Drain	QGD		5	22	
Diode Forward Voltage	VSD	ID = 4A, VGD = 0	-0.6	-1.8	V
Reverse Recovery Time	TT	I = 4A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	Rθjc		-	2.5	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	60	

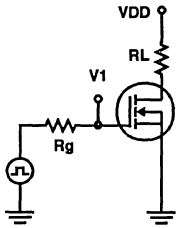


FIGURE 1. SWITCHING TIME TESTING

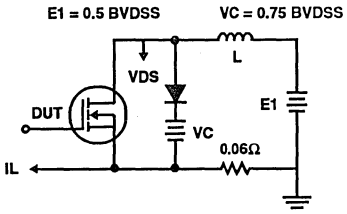


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

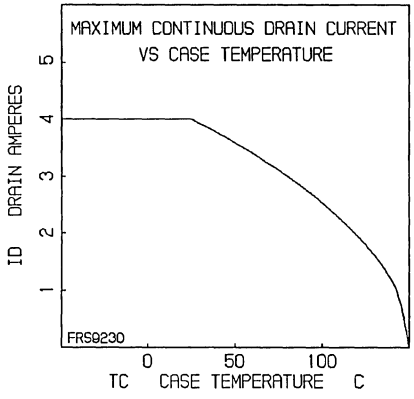
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

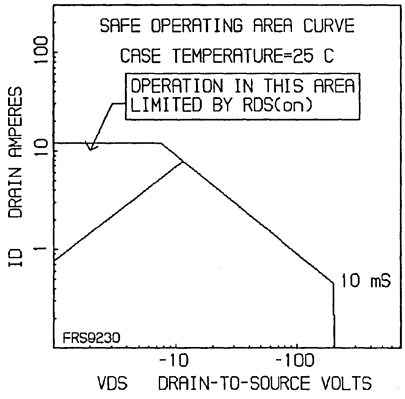
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS		UNITS
					MIN	MAX	
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7312D, R	VGS = 0, ID = 1mA	-200	-	V
	(Note 5, 6)	BVDSS	2N7312H	VGS = 0, ID = 1mA	-190	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7312D, R	VGS = VDS, ID = 1mA	-2.0	-4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7312H	VGS = VDS, ID = 1mA	-2.0	-6.0	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7312D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7312H	VGS = -20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7312D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7312H	VGS = 20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7312D, R	VGS = 0, VDS = -160V	-	25	μA
	(Note 5, 6)	IDSS	2N7312H	VGS = 0, VDS = -160V	-	100	μA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7312D, R	VGS = -10V, ID = 4A	-	-5.54	V
	(Note 1, 5, 6)	VDS(on)	2N7312H	VGS = -16V, ID = 4A	-	-8.31	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7312D, R	VGS = -10V, ID = 2A	-	1.32	Ω
	(Note 1, 5, 6)	RDS(on)	2N7312H	VGS = -14V, ID = 2A	-	1.98	Ω

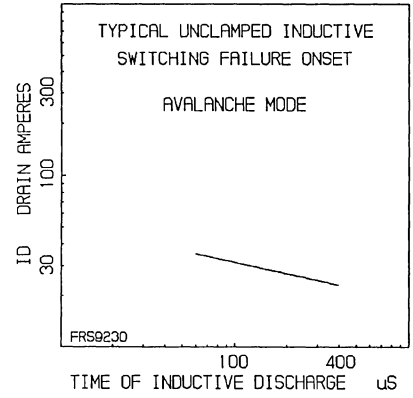
NOTES:

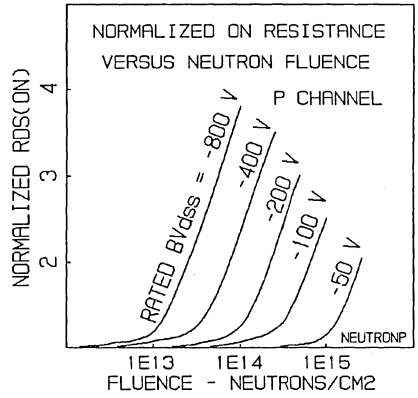
1. Pulse test, 300μs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 1E13
5. Gamma = 1000KRAD(Si). Neutron = 1E13
6. Insitu Gamma bias must be sampled for both VGS = -10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 2/19/90 on TA 17732 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

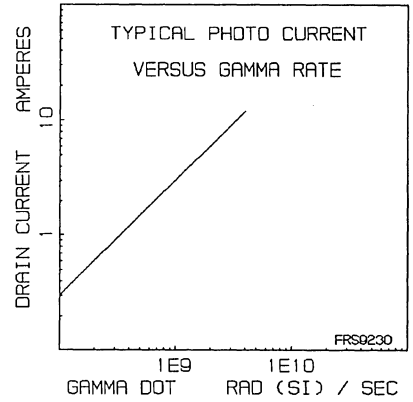
Typical Performance Characteristics

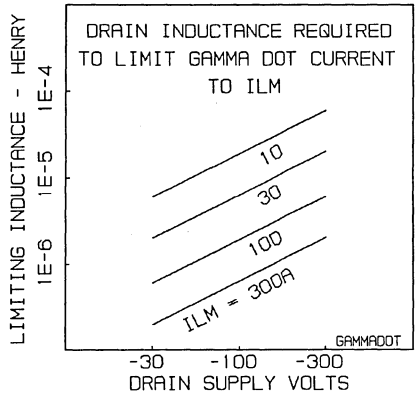












HARRIS SEMICONDUCTOR

2N7316D, 2N7316R 2N7316H

REGISTRATION PENDING
Currently Available as FRM9140(D, R, H)
December 1992

Radiation Hardened P-Channel Power MOSFETs

Features

- 11A, -100V, RDS(on) = 0.300Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 3.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E13 Neutrons/cm^2
  - Usable to 3E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

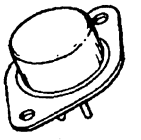
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-204AA



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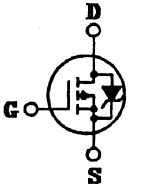


Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7316D, R, H	UNITS
Drain-Source Voltage	VDS	-100	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	-100	V
Continuous Drain Current			
TC = +25°C	ID	11	A
TC = +100°C	ID	7	A
Pulsed Drain Current	IDM	33	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	125	W
TC = +100°C	PT	50	W
Derated Above +25°C		1.0	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	33	A
Continuous Source Current (Body Diode)	IS	11	A
Pulsed Source Current (Body Diode)	ISM	33	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3241**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	-100	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	-2.0	-4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = -20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = +20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = -100V, VGS = 0 VDS = -80V, VGS = 0 VDS = -80V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	33	A
Drain-Source On-State Volts	VDS(on)	VGS = -10V, ID = 11A	-	-3.47	V
Drain-Source On Resistance	RDS(on)	VGS = -10V, ID = 7A	-	0.300	Ω
Turn-On Delay Time	td(on)	VDD = -50V, ID = 11A	-	64	ns
Rise Time	tr	Pulse Width = 3µs	-	236	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	232	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	132	
Gate-Charge Threshold	QG(th)	VDD = -50V, ID = 11A IGS1 = IGS2 0 ≤ VGS ≤ 20	2	10	nc
Gate-Charge On State	QG(on)		26	104	
Gate-Charge Total	QGM		53	214	
Plateau Voltage	VGP		-3	-12	V
Gate-Charge Source	QGS		7	30	nc
Gate-Charge Drain	QGD		9	36	
Diode Forward Voltage	VSD	ID =11A, VGD = 0	-0.6	-1.8	V
Reverse Recovery Time	TT	I = 11A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	Rθjc		-	1.0	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	30	

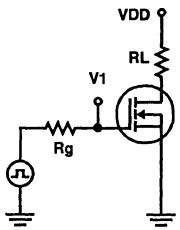


FIGURE 1. SWITCHING TIME TESTING

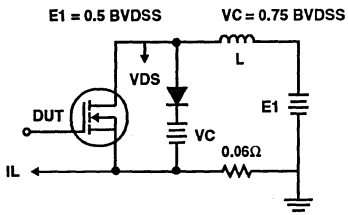


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

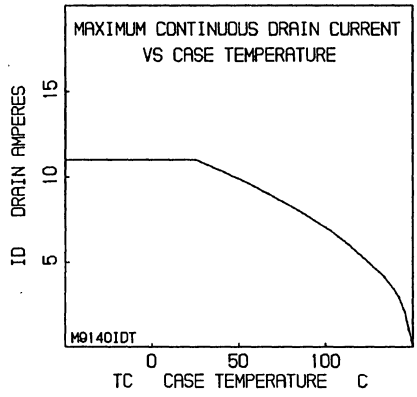
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

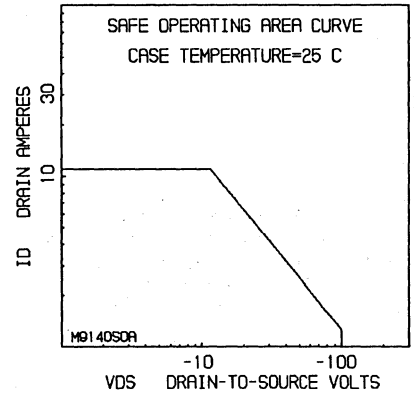
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7316D, R	VGS = 0, ID = 1mA	-100	-	V
	(Note 5, 6)	BVDSS	2N7316H	VGS = 0, ID = 1mA	-95	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7316D, R	VGS = VDS, ID = 1mA	-2.0	-4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7316H	VGS = VDS, ID = 1mA	-2.0	-6.0	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7316D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7316H	VGS = -20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7316D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7316H	VGS = 20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7316D, R	VGS = 0, VDS = -80V	-	25	µA
	(Note 5, 6)	IDSS	2N7316H	VGS = 0, VDS = -80V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7316D, R	VGS = -10V, ID = 11A	-	-3.47	V
	(Note 1, 5, 6)	VDS(on)	2N7316H	VGS = -16V, ID = 11A	-	-5.21	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7316D, R	VGS = -10V, ID = 7A	-	0.300	Ω
	(Note 1, 5, 6)	RDS(on)	2N7316H	VGS = -14V, ID = 7A	-	0.450	Ω

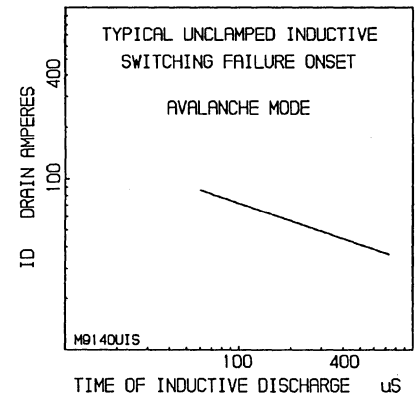
NOTES:

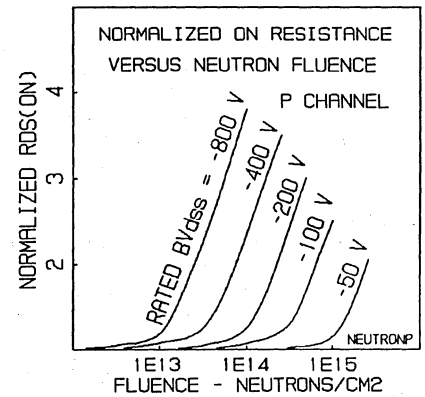
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 3E13
5. Gamma = 1000KRAD(Si). Neutron = 3E13
6. Insitu Gamma bias must be sampled for both VGS = -10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 5/19/90 on TA 17741 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

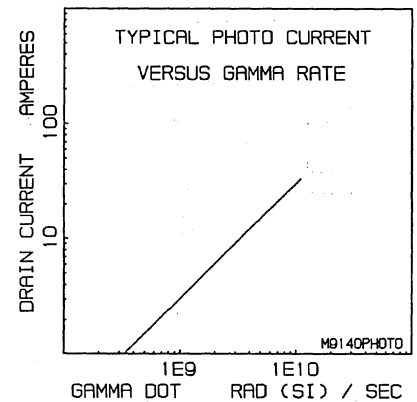
Typical Performance Characteristics

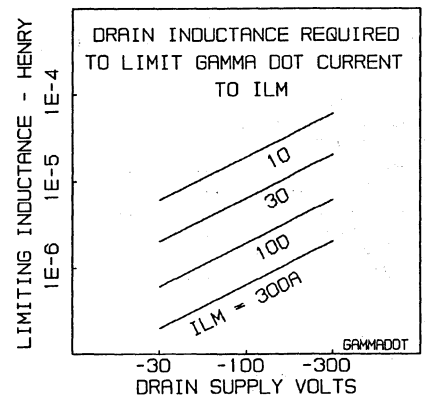












HARRIS SEMICONDUCTOR

2N7317D, 2N7317R 2N7317H

REGISTRATION PENDING
Currently Available as FRS9140 (D, R, H)
December 1992

Radiation Hardened P-Channel Power MOSFETs

Features

- 11A, -100V, RDS(on) = 0.315Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 3.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E13 Neutrons/cm^2
  - Usable to 3E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

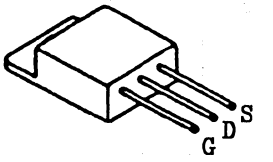
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-257AA



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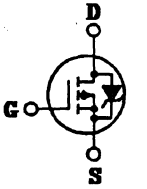


Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7317D, R, H	UNITS
Drain-Source Voltage	VDS	-100	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	-100	V
Continuous Drain Current			
TC = +25°C	ID	11	A
TC = +100°C	ID	7	A
Pulsed Drain Current	IDM	33	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	75	W
TC = +100°C	PT	30	W
Derated Above +25°C		0.60	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	33	A
Continuous Source Current (Body Diode)	IS	11	A
Pulsed Source Current (Body Diode)	ISM	33	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3264**

HARRIS SEMICONDUCTOR

2N7318D, 2N7318R 2N7318H

REGISTRATION PENDING
Currently Available as FRM9240(D, R, H)

December 1992

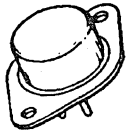
Radiation Hardened P-Channel Power MOSFETs

Features

- 7A, -200V, RDS(on) = 0.720Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 5.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Package

TO-204AA



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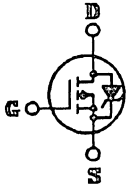


Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7318D, R, H	UNITS
Drain-Source Voltage	VDS	-200	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	-200	V
Continuous Drain Current			
TC = +25°C	ID	7	A
TC = +100°C	ID	4	A
Pulsed Drain Current	IDM	21	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	125	W
TC = +100°C	PT	50	W
Derated Above +25°C		1.0	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	21	A
Continuous Source Current (Body Diode)	IS	7	A
Pulsed Source Current (Body Diode)	ISM	21	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3242**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	-200	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	-2.0	-4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = -20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = +20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = -200V, VGS = 0 VDS = -160V, VGS = 0 VDS = -160V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	21	A
Drain-Source On-State Volts	VDS(on)	VGS = -10V, ID = 7A	-	-5.29	V
Drain-Source On Resistance	RDS(on)	VGS = -10V, ID = 4A	-	0.720	Ω
Turn-On Delay Time	td(on)	VDD = -100V, ID = 7A	-	60	ns
Rise Time	tr	Pulse Width = 3µs	-	132	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	268	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	114	
Gate-Charge Threshold	QG(th)	VDD = -100V, ID = 7A IGS1 = IGS2 0 ≤ VGS ≤ 20	2	8	nc
Gate-Charge On State	QG(on)		26	106	
Gate-Charge Total	QGM		43	216	
Plateau Voltage	VGP		-3	-12	V
Gate-Charge Source	QGS		5	22	nc
Gate-Charge Drain	QGD		9	36	
Diode Forward Voltage	VSD	ID =7A, VGD = 0	-0.6	-1.8	V
Reverse Recovery Time	TT	I = 7A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	Rθjc		-	1.0	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	30	

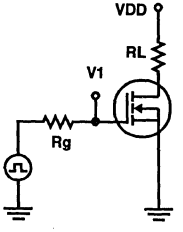


FIGURE 1. SWITCHING TIME TESTING

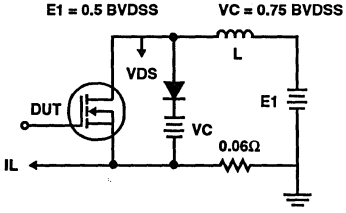


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

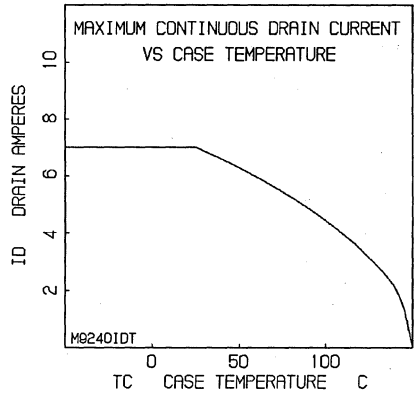
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

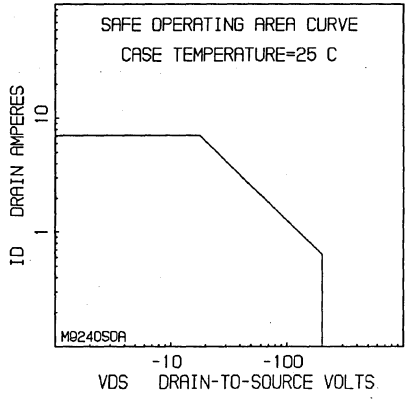
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7318D, R	VGS = 0, ID = 1mA	-200	-	V
	(Note 5, 6)	BVDSS	2N7318H	VGS = 0, ID = 1mA	-190	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7318D, R	VGS = VDS, ID = 1mA	-2.0	-4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7318H	VGS = VDS, ID = 1mA	-2.0	-6.0	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7318D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7318H	VGS = -20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7318D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7318H	VGS = 20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7318D, R	VGS = 0, VDS = -160V	-	25	μA
	(Note 5, 6)	IDSS	2N7318H	VGS = 0, VDS = -160V	-	100	μA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7318D, R	VGS = -10V, ID = 7A	-	-5.29	V
	(Note 1, 5, 6)	VDS(on)	2N7318H	VGS = -16V, ID = 7A	-	-7.94	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7318D, R	VGS = -10V, ID = 4A	-	0.720	Ω
	(Note 1, 5, 6)	RDS(on)	2N7318H	VGS = -14V, ID = 4A	-	1.08	Ω

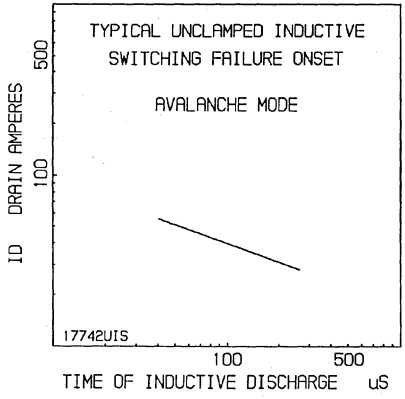
NOTES:

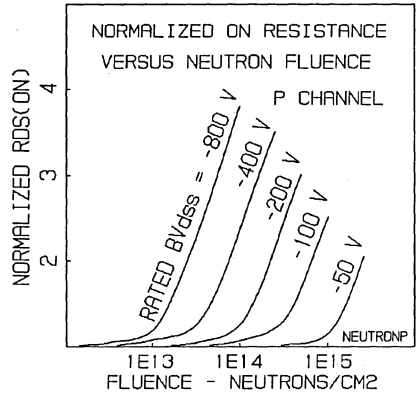
1. Pulse test, 300μs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 1E13
5. Gamma = 1000KRAD(Si). Neutron = 1E13
6. Insitu Gamma bias must be sampled for both VGS = -10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 7/13/90 on TA 17742 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

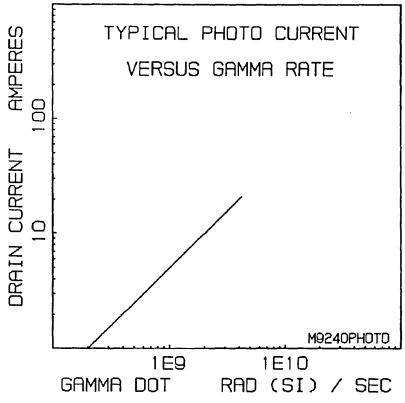
Typical Performance Characteristics

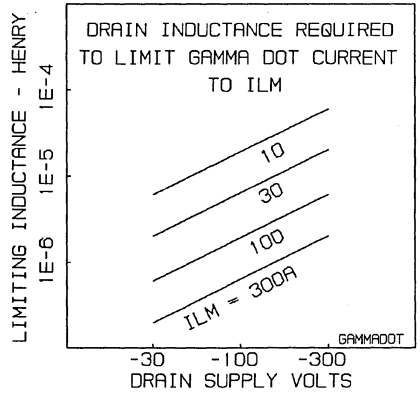












HARRIS SEMICONDUCTOR

2N7319D, 2N7319R 2N7319H

REGISTRATION PENDING
Currently Available as FRS9240 (D, R, H)

December 1992

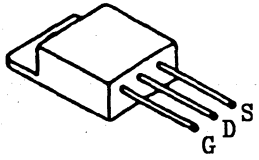
Radiation Hardened P-Channel Power MOSFETs

Features

- 7A, -200V, RDS(on) = 0.735Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 5.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Package

TO-257AA



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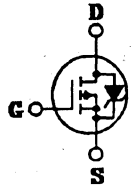


Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n^o) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7319D, R, H	UNITS
Drain-Source Voltage	VDS	-200	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	-200	V
Continuous Drain Current			
TC = +25°C	ID	7	A
TC = +100°C	ID	4	A
Pulsed Drain Current	IDM	21	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	75	W
TC = +100°C	PT	30	W
Derated Above +25°C		0.60	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	21	A
Continuous Source Current (Body Diode)	IS	7	A
Pulsed Source Current (Body Diode)	ISM	21	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3265**

HARRIS SEMICONDUCTOR

2N7322D, 2N7322R 2N7322H

REGISTRATION PENDING
Currently Available as FRK9150 (D, R, H)
December 1992

Radiation Hardened P-Channel Power MOSFETs

Features

- 26A, -100V, RDS(on) = 0.125Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 7.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E13 Neutrons/cm^2
  - Usable to 3E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

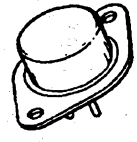
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25MΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm2 for 500V product to 1E14n/cm2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-204AE



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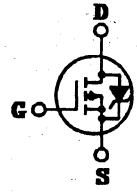


Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7322D, R, H	UNITS
Drain-Source Voltage	VDS	-100	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	-100	V
Continuous Drain Current			
TC = +25°C	ID	26	A
TC = +100°C	ID	17	A
Pulsed Drain Current	IDM	78	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	300	W
TC = +100°C	PT	120	W
Derated Above +25°C		2.40	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	78	A
Continuous Source Current (Body Diode)	IS	26	A
Pulsed Source Current (Body Diode)	ISM	78	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3266

HARRIS SEMICONDUCTOR

2N7323D, 2N7323R 2N7323H

REGISTRATION PENDING
Currently Available as FRF9150(D, R, H)

December 1992

Radiation Hardened P-Channel Power MOSFETs

Features

- 23A, -100V, RDS(on) = 0.140Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 7.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E13 Neutrons/cm^2
  - Usable to 3E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

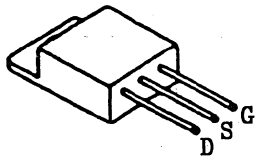
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-254AA



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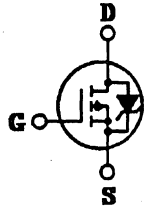


Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7323D, R, H	UNITS
Drain-Source Voltage	VDS	-100	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	-100	V
Continuous Drain Current			
TC = +25°C	ID	23	A
TC = +100°C	ID	15	A
Pulsed Drain Current	IDM	69	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	125	W
TC = +100°C	PT	50	W
Derated Above +25°C		1.00	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	69	A
Continuous Source Current (Body Diode)	IS	23	A
Pulsed Source Current (Body Diode)	ISM	69	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3243**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	-100	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	-2.0	-4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = -20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = +20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = -100V, VGS = 0 VDS = -80V, VGS = 0 VDS = -80V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	69	A
Drain-Source On-State Volts	VDS(on)	VGS = -10V, ID = 23A	-	-3.38	V
Drain-Source On Resistance	RDS(on)	VGS = -10V, ID = 15A	-	0.140	Ω
Turn-On Delay Time	td(on)	VDD = -50V, ID = 23A	-	170	ns
Rise Time	tr	Pulse Width = 3µs	-	620	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	158	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	242	
Gate-Charge Threshold	QG(th)	VDD = -50V, ID = 23A IGS1 = IGS2 0 ≤ VGS ≤ 20	4	16	nc
Gate-Charge On State	QG(on)		60	240	
Gate-Charge Total	QGM		126	504	
Plateau Voltage	VGP		3	14	V
Gate-Charge Source	QGS		17	68	nc
Gate-Charge Drain	QGD		21	86	
Diode Forward Voltage	VSD	ID = 23A, VGD = 0	-0.6	-1.8	V
Reverse Recovery Time	TT	I = 23A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	Rθjc		-	1.0	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	48	

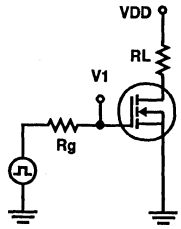


FIGURE 1. SWITCHING TIME TESTING

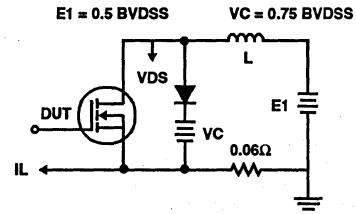


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

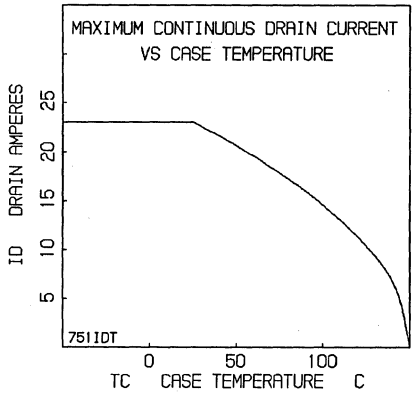
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

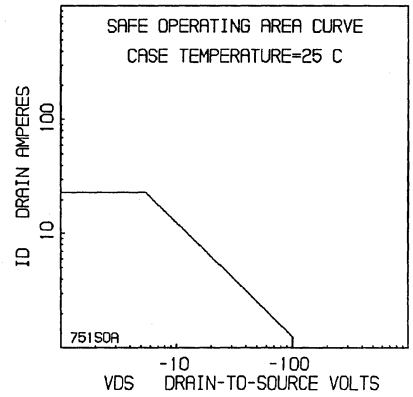
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7323D, R	VGS = 0, ID = 1mA	-100	-	V
	(Note 5, 6)	BVDSS	2N7323H	VGS = 0, ID = 1mA	-95	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7323D, R	VGS = VDS, ID = 1mA	-2.0	-4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7323H	VGS = VDS, ID = 1mA	-2.0	-6.0	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7323D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7323H	VGS = -20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7323D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7323H	VGS = 20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7323D, R	VGS = 0, VDS = -80V	-	25	µA
	(Note 5, 6)	IDSS	2N7323H	VGS = 0, VDS = -80V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7323D, R	VGS = -10V, ID = 23A	-	-3.38	V
	(Note 1, 5, 6)	VDS(on)	2N7323H	VGS = -16V, ID = 23A	-	-5.07	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7323D, R	VGS = -10V, ID = 15A	-	0.140	Ω
	(Note 1, 5, 6)	RDS(on)	2N7323H	VGS = -14V, ID = 15A	-	0.210	Ω

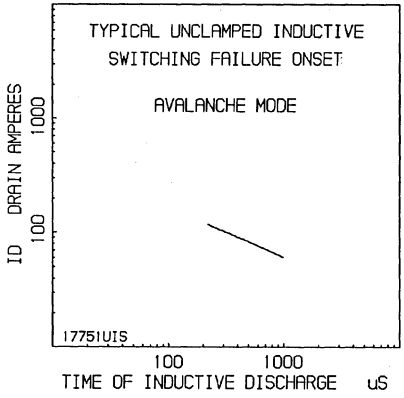
NOTES:

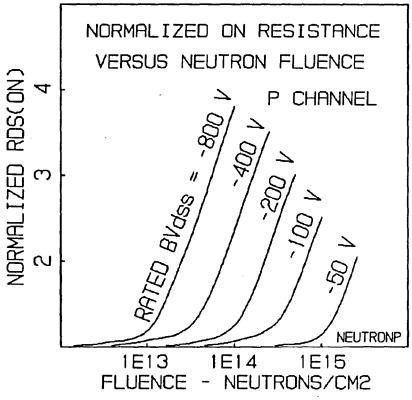
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 3E13
5. Gamma = 1000KRAD(Si). Neutron = 3E13
6. Insitu Gamma bias must be sampled for both VGS = -10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 1/18/91 on TA 17751 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

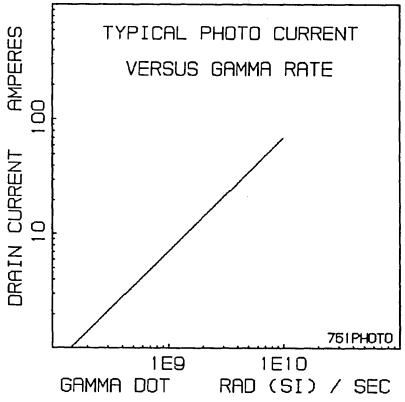
Typical Performance Characteristics

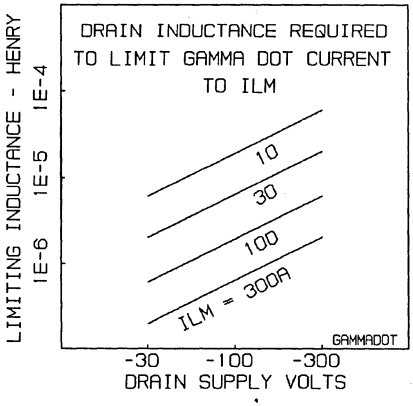












HARRIS SEMICONDUCTOR

2N7324D, 2N7324R 2N7324H

REGISTRATION PENDING
Currently Available as FRM9250 (D, R, H)
December 1992

Radiation Hardened P-Channel Power MOSFETs

Features

- 16A, -200V, RDS(on) = 0.300Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 12nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

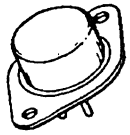
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

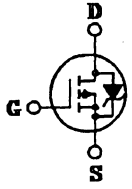
This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-204AA



Symbol



Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7324D, R, H	UNITS
Drain-Source Voltage	VDS	-200	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	-200	V
Continuous Drain Current			
TC = +25°C	ID	16	A
TC = +100°C	ID	10	A
Pulsed Drain Current	IDM	48	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	300	W
TC = +100°C	PT	120	W
Derated Above +25°C		2.40	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	48	A
Continuous Source Current (Body Diode)	IS	16	A
Pulsed Source Current (Body Diode)	ISM	48	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3267**

HARRIS SEMICONDUCTOR

2N7325D, 2N7325R 2N7325H

REGISTRATION PENDING
Currently Available as FRF9250(D, R, H)
December 1992

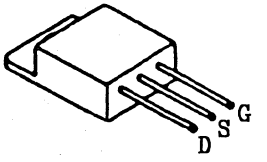
Radiation Hardened P-Channel Power MOSFETs

Features

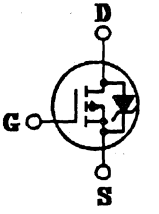
- **14A, -200V, RDS(on) = 0.315Ω**
- **Second Generation Rad Hard MOSFET Results From New Design Concepts**
- Gamma
  - **Meets Pre-Rad Specifications to 100KRAD(Si)**
  - **Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)**
  - **Performance Permits Limited Use to 3000KRAD(Si)**
- Gamma Dot
  - **Survives 3E9RAD(Si)/sec at 80% BVDSS Typically**
  - **Survives 2E12 Typically If Current Limited to IDM**
- Photo Current - **12.0nA Per-RAD(Si)/sec Typically**
- Neutron
  - **Pre-RAD Specifications for 1E13 Neutrons/cm^2**
  - **Usable to 1E14 Neutrons/cm^2**
- Single Event - **Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS**

Package

TO-254AA



Symbol



Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n^0) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7325D, R, H	UNITS
Drain-Source Voltage	VDS	-200	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	-200	V
Continuous Drain Current			
TC = +25°C	ID	14	A
TC = +100°C	ID	9	A
Pulsed Drain Current	IDM	42	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	125	W
TC = +100°C	PT	50	W
Derated Above +25°C		1.00	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	42	A
Continuous Source Current (Body Diode)	IS	14	A
Pulsed Source Current (Body Diode)	ISM	42	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max.	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3247**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	-200	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	-2.0	-4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = -20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = +20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = -200V, VGS = 0 VDS = -160V, VGS = 0 VDS = -160V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	42	A
Drain-Source On-State Volts	VDS(on)	VGS = -10V, ID = 14A	-	-4.63	V
Drain-Source On Resistance	RDS(on)	VGS = -10V, ID = 9A	-	0.315	Ω
Turn-On Delay Time	td(on)	VDD = -100V, ID = 14A	-	102	ns
Rise Time	tr	Pulse Width = 3µs	-	242	ns
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 25Ω	-	658	ns
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	278	ns
Gate-Charge Threshold	QG(th)	VDD = -100V, ID = 14A IGS1 = IGS2 0 ≤ VGS ≤ 20	3	12	nc
Gate-Charge On State	QG(on)		62	248	nc
Gate-Charge Total	QGM		125	502	nc
Plateau Voltage	VGP		2	10	V
Gate-Charge Source	QGS		10	42	nc
Gate-Charge Drain	QGD		21	86	nc
Diode Forward Voltage	VSD	ID = 14A, VGD = 0	-0.6	-1.8	V
Reverse Recovery Time	TT	I = 14A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	Rθjc		-	1.0	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	48	°C/W

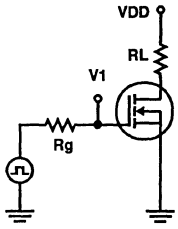


FIGURE 1. SWITCHING TIME TESTING

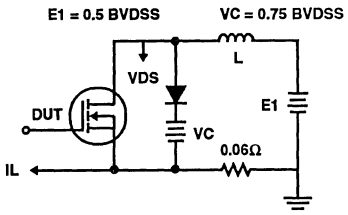


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

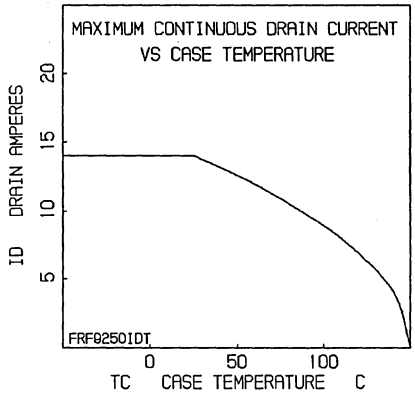
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

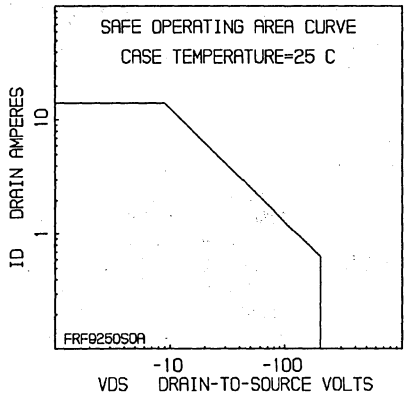
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7325D, R	VGS = 0, ID = 1mA	-200	-	V
	(Note 5, 6)	BVDSS	2N7325H	VGS = 0, ID = 1mA	-190	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7325D, R	VGS = VDS, ID = 1mA	-2.0	-4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7325H	VGS = VDS, ID = 1mA	-2.0	-6.0	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7325D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7325H	VGS = -20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7325D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7325H	VGS = 20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7325D, R	VGS = 0, VDS = -160V	-	25	µA
	(Note 5, 6)	IDSS	2N7325H	VGS = 0, VDS = -160V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7325D, R	VGS = -10V, ID = 14A	-	-4.63	V
	(Note 1, 5, 6)	VDS(on)	2N7325H	VGS = -16V, ID = 14A	-	-6.95	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7325D, R	VGS = -10V, ID = 9A	-	0.315	Ω
	(Note 1, 5, 6)	RDS(on)	2N7325H	VGS = -14V, ID = 9A	-	0.473	Ω

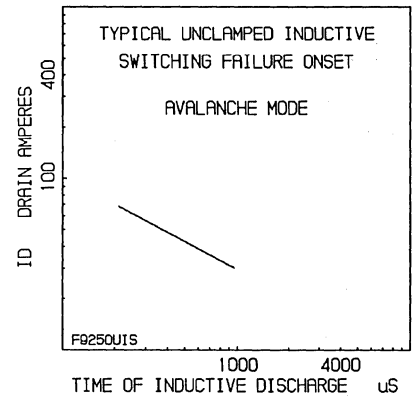
NOTES:

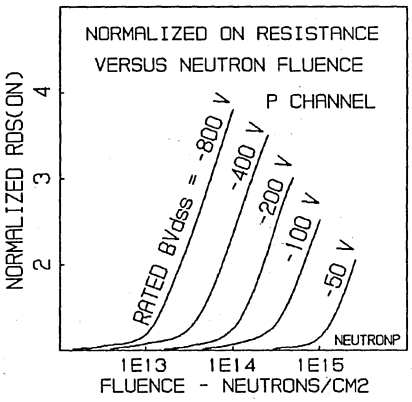
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 1E13
5. Gamma = 1000KRAD(Si). Neutron = 1E13
6. Insitu Gamma bias must be sampled for both VGS = -10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 7/21/90 on TA 17752 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

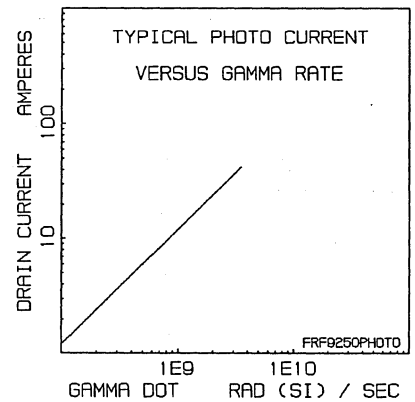
Typical Performance Characteristics

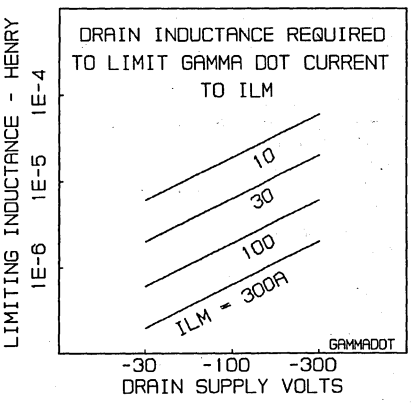












HARRIS SEMICONDUCTOR

2N7328D, 2N7328R 2N7328H

REGISTRATION PENDING
Currently Available as FRK9160(D, R, H)
December 1992

Radiation Hardened P-Channel Power MOSFETs

Features

- 40A, -100V, RDS(on) = 0.085Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 10.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E13 Neutrons/cm^2
  - Usable to 3E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

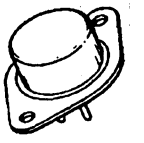
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n^0) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-204AE



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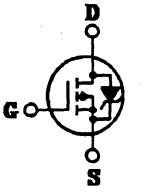


Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7328D, R, H	UNITS
Drain-Source Voltage	VDS	-100	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	-100	V
Continuous Drain Current			
TC = +25°C	ID	40	A
TC = +100°C	ID	26	A
Pulsed Drain Current	IDM	100	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	300	W
TC = +100°C	PT	120	W
Derated Above +25°C		2.40	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	100	A
Continuous Source Current (Body Diode)	IS	40	A
Pulsed Source Current (Body Diode)	ISM	100	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3244**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	-100	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	-2.0	-4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = -20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = +20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = -100V, VGS = 0 VDS = -80V, VGS = 0 VDS = -80V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	100	A
Drain-Source On-State Volts	VDS(on)	VGS = -10V, ID = 40A	-	-3.57	V
Drain-Source On Resistance	RDS(on)	VGS = -10V, ID = 26A	-	0.085	Ω
Turn-On Delay Time	td(on)	VDD = -50V, ID = 40A	-	150	ns
Rise Time	tr	Pulse Width = 3µs	-	900	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 10Ω	-	700	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	500	
Gate-Charge Threshold	QG(th)	VDD = -50V, ID = 40A IGS1 = IGS2 0 ≤ VGS ≤ 20	7	28	nc
Gate-Charge On State	QG(on)		86	346	
Gate-Charge Total	QGM		158	632	
Plateau Voltage	VGP		-2	-11	V
Gate-Charge Source	QGS		19	78	nc
Gate-Charge Drain	QGD		34	138	
Diode Forward Voltage	VSD	ID = 40A, VGD = 0	-0.6	-1.8	V
Reverse Recovery Time	TT	I = 40A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	Rθjc		-	0.42	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	30	

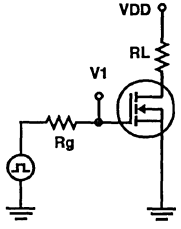


FIGURE 1. SWITCHING TIME TESTING

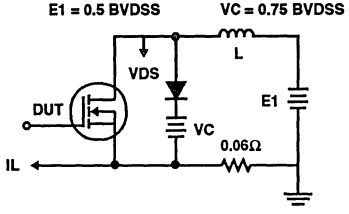


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

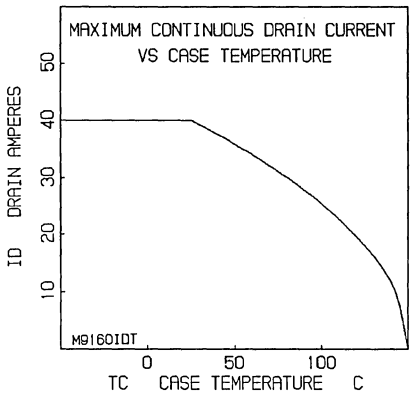
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

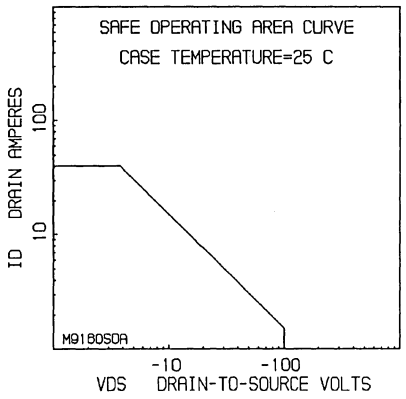
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7328D, R	VGS = 0, ID = 1mA	-100	-	V
	(Note 5, 6)	BVDSS	2N7328H	VGS = 0, ID = 1mA	-95	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7328D, R	VGS = VDS, ID = 1mA	-2.0	-4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7328H	VGS = VDS, ID = 1mA	-2.0	-6.0	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7328D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7328H	VGS = -20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7328D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7328H	VGS = 20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7328D, R	VGS = 0, VDS = -80V	-	25	µA
	(Note 5, 6)	IDSS	2N7328H	VGS = 0, VDS = -80V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7328D, R	VGS = -10V, ID = 40A	-	-3.57	V
	(Note 1, 5, 6)	VDS(on)	2N7328H	VGS = -16V, ID = 40A	-	-5.36	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7328D, R	VGS = -10V, ID = 26A	-	0.85	Ω
	(Note 1, 5, 6)	RDS(on)	2N7328H	VGS = -14V, ID = 26A	-	0.128	Ω

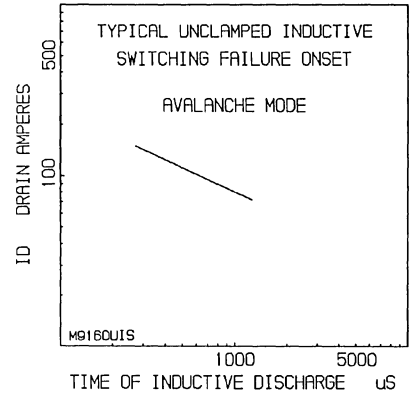
NOTES:

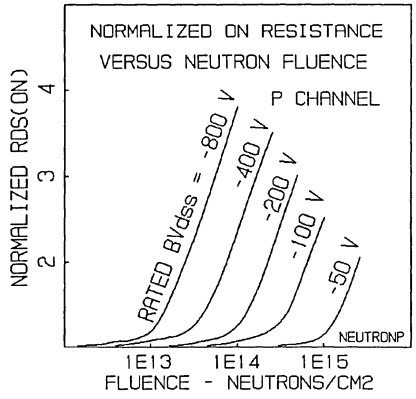
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 3E13
5. Gamma = 1000KRAD(Si). Neutron = 3E13
6. Insitu Gamma bias must be sampled for both VGS = -10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 6/8/90 on TA 17761 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

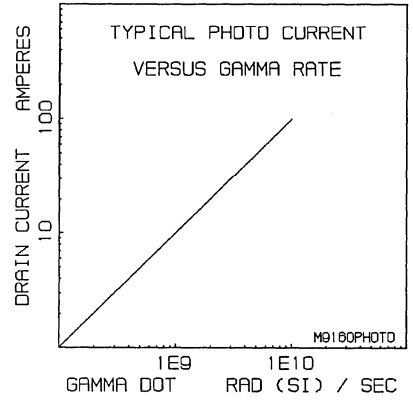
Typical Performance Characteristics

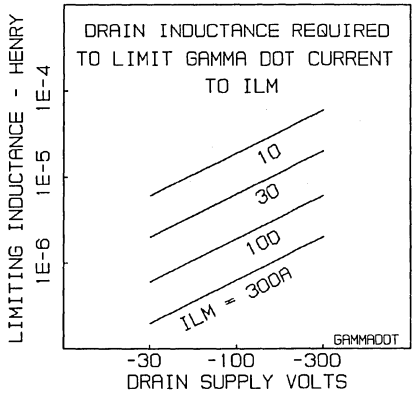












HARRIS SEMICONDUCTOR

2N7329D, 2N7329R 2N7329H

PRELIMINARY REGISTRATION PENDING
Currently Available as FRE9160(D, R, H)

January 1993

Radiation Hardened P-Channel Power MOSFETs

Features

- 30A, -100V, RDS(on) = 0.095Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 10.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E13 Neutrons/cm^2
  - Usable to 3E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

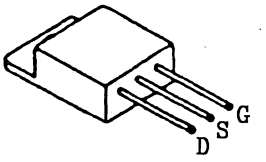
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n^0) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-258



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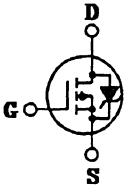


Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7329D, R, H	UNITS
Drain-Source Voltage	VDS	-100	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	-100	V
Continuous Drain Current			
TC = +25°C	ID	30	A
TC = +100°C	ID	19	A
Pulsed Drain Current	IDM	90	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	150	W
TC = +100°C	PT	60	W
Derated Above +25°C		1.20	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	90	A
Continuous Source Current (Body Diode)	IS	30	A
Pulsed Source Current (Body Diode)	ISM	90	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3268**

HARRIS SEMICONDUCTOR

2N7330D, 2N7330R 2N7330H

REGISTRATION PENDING
Currently Available as FRK9260(D, R, H)
December 1992

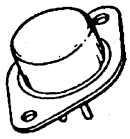
Radiation Hardened P-Channel Power MOSFETs

Features

- 26A, -200V, RDS(on) = 0.200Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 18.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Package

TO-204AE



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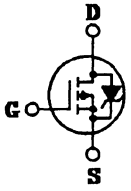


Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7330D, R, H	UNITS
Drain-Source Voltage	VDS	-200	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	-200	V
Continuous Drain Current			
TC = +25°C	ID	26	A
TC = +100°C	ID	17	A
Pulsed Drain Current	IDM	78	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	300	W
TC = +100°C	PT	120	W
Derated Above +25°C		2.40	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	78	A
Continuous Source Current (Body Diode)	IS	26	A
Pulsed Source Current (Body Diode)	ISM	78	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3248**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	-200	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	-2.0	-4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = -20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = +20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = -200V, VGS = 0 VDS = -160V, VGS = 0 VDS = -160V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	78	A
Drain-Source On-State Volts	VDS(on)	VGS = -10V, ID = 26A	-	-5.46	V
Drain-Source On Resistance	RDS(on)	VGS = -10V, ID = 17A	-	0.200	Ω
Turn-On Delay Time	td(on)	VDD = -100V, ID = 26A	-	150	ns
Rise Time	tr	Pulse Width = 3µs	-	800	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 10Ω	-	700	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	500	
Gate-Charge Threshold	QG(th)	VDD = -100V, ID = 26A IGS1 = IGS2 0 ≤ VGS ≤ 20	6	26	nc
Gate-Charge On State	QG(on)		97	388	
Gate-Charge Total	QGM		185	740	
Plateau Voltage	VGP		-2	-10	V
Gate-Charge Source	QGS		15	60	nc
Gate-Charge Drain	QGD		33	132	
Diode Forward Voltage	VSD	ID = 26A, VGD = 0	-0.6	-1.8	V
Reverse Recovery Time	TT	I = 26A; di/dt = 100A/µs	-	TBD	ns
Junction-To-Case	Rθjc		-	0.42	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	30	

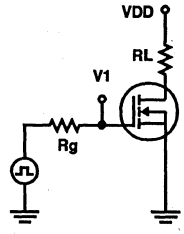


FIGURE 1. SWITCHING TIME TESTING

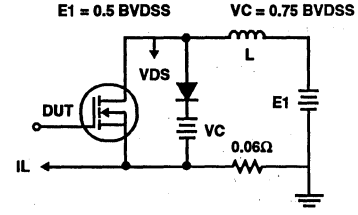


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

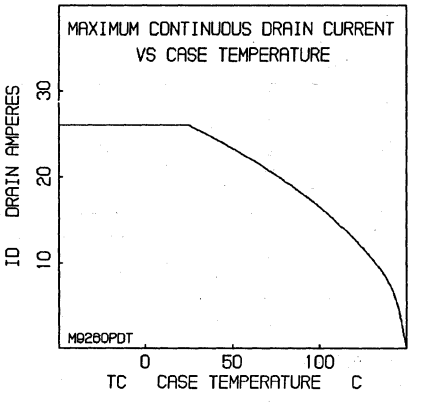
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

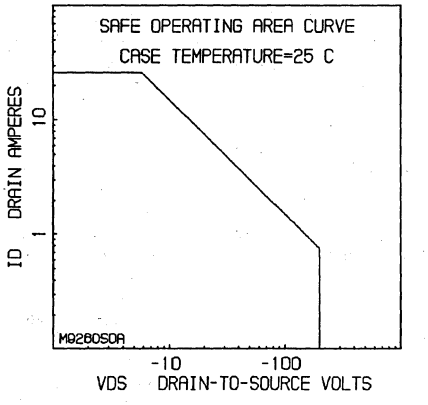
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7330D, R	VGS = 0, ID = 1mA	-200	-	V
	(Note 5, 6)	BVDSS	2N7330H	VGS = 0, ID = 1mA	-190	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7330D, R	VGS = VDS, ID = 1mA	-2.0	-4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7330H	VGS = VDS, ID = 1mA	-2.0	-6.0	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7330D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7330H	VGS = -20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7330D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7330H	VGS = 20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7330D, R	VGS = 0, VDS = -160V	-	25	μA
	(Note 5, 6)	IDSS	2N7330H	VGS = 0, VDS = -160V	-	100	μA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	2N7330D, R	VGS = -10V, ID = 26A	-	-5.46	V
	(Note 1, 5, 6)	VDS(on)	2N7330H	VGS = -16V, ID = 26A	-	-8.19	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7330D, R	VGS = -10V, ID = 17A	-	0.200	Ω
	(Note 1, 5, 6)	RDS(on)	2N7330H	VGS = -14V, ID = 17A	-	0.300	Ω

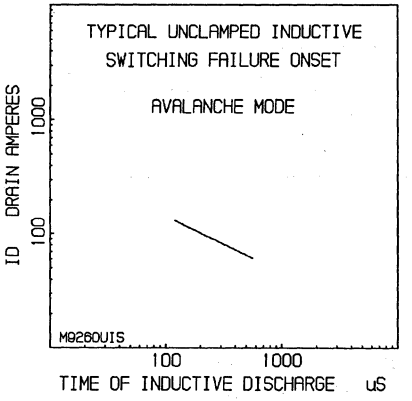
NOTES:

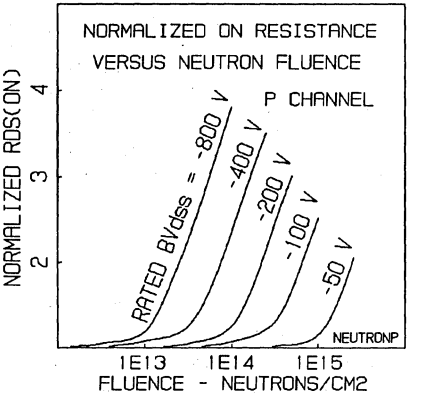
1. Pulse test, 300μs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 1E13
5. Gamma = 1000KRAD(Si). Neutron = 1E13
6. Insitu Gamma bias must be sampled for both VGS = -10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 6/12/90 on TA 17762 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

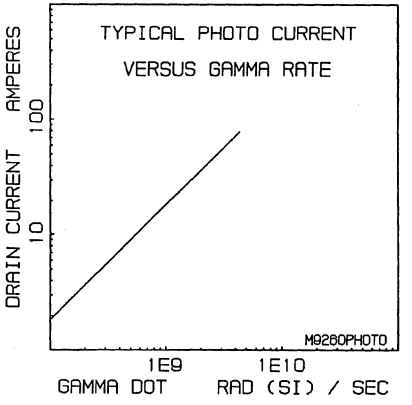
Typical Performance Characteristics

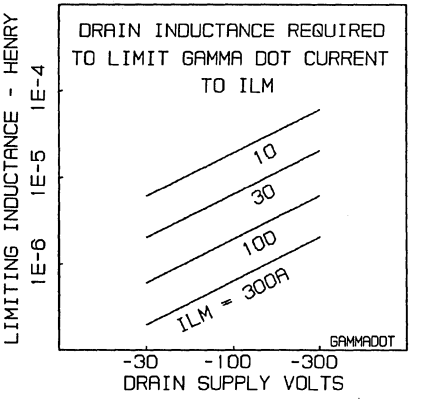












HARRIS SEMICONDUCTOR

2N7331D, 2N7331R 2N7331H

PRELIMINARY REGISTRATION PENDING
Currently Available as FRE9260 (D, R, H)
January 1993

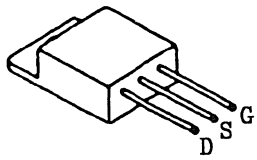
Radiation Hardened P-Channel Power MOSFETs

Features

- 19A, -200V, RDS(on) = 0.210Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 18.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm^2
  - Usable to 1E14 Neutrons/cm^2
- Single Event - Typically Survives 1E5ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Package

TO-258



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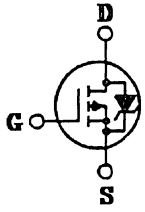


Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		2N7331D, R, H	UNITS
Drain-Source Voltage	VDS	-200	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	-200	V
Continuous Drain Current			
TC = +25°C	ID	19	A
TC = +100°C	ID	12	A
Pulsed Drain Current	IDM	57	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	150	W
TC = +100°C	PT	60	W
Derated Above +25°C		1.20	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	57	A
Continuous Source Current (Body Diode)	IS	19	A
Pulsed Source Current (Body Diode)	ISM	57	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3269**

RAD HARD 13

APPLICATION NOTES

No. 9011 June 1992

SYNCHRONOUS OPERATION OF HARRIS RAD HARD SOS 64K ASYNCHRONOUS SRAMs

Author: Steve Rivet

The Harris SOS 64K SRAMs provide excellent single event and total dose hardness, and fast access and cycle times. The HS-65643RH and HS-65647RH were designed as standard pinout asysnchronous circuits; they can, however, be used in systems that require their speed and radiation resistance, but have been designed for synchronous memories. The addition of two HCS373 or HCTS373 to latch the address location on the falling edge of the chip enable signal will make the HS-65643RH and HS-65647RH appear as synchronous memories to the system. The only difference in signal wiring need to use the asynchronous circuits it to route the address lines through the 373's and connect the $\overline{E}$ or $\overline{E1}$ signal to the 373's $\overline{LE}$ pin as shown in Figure 1.

The HCS373 and HCTS373 are both fabricated with SOS technology; each circuit is available hardened to 200K RADs or 1M RADs, and has excellent single event immunity. The addition of the latches will delay the address inputs to the SRAMs by a maximum of 39ns (over temperature, VDD, and 1M RAD total dose), so system timing should be analyzed accordingly. Even with the additional delay of the latches, address access time is a maximum of 89ns (for a 50ns SRAM access time).

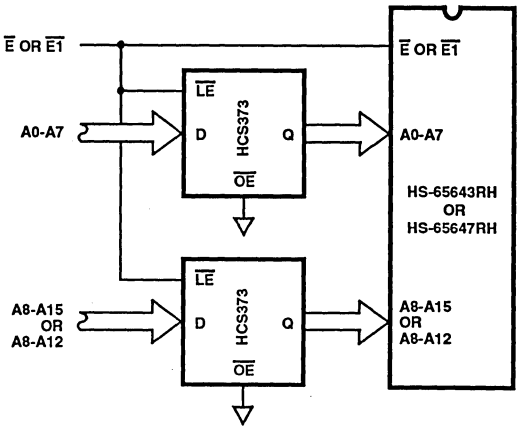
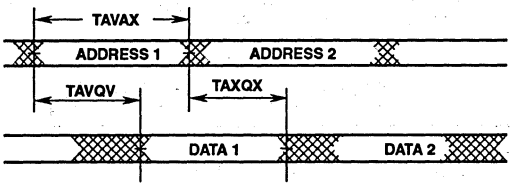


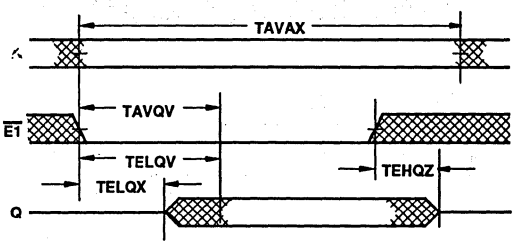
FIGURE 1.

HS-65643RH, HS-65647RH Asynchronous Read Cycles

READ CYCLE I: $\overline{W}$ HIGH; $\overline{G}$, $\overline{E1}$ LOW

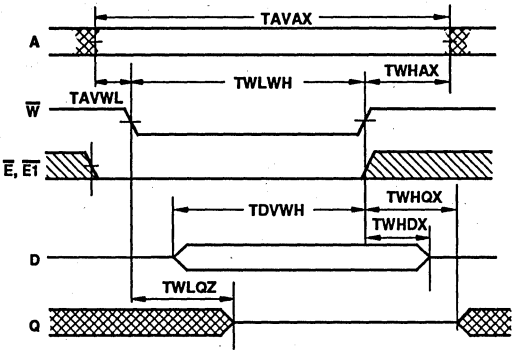


READ CYCLE II: $\overline{W}$ HIGH

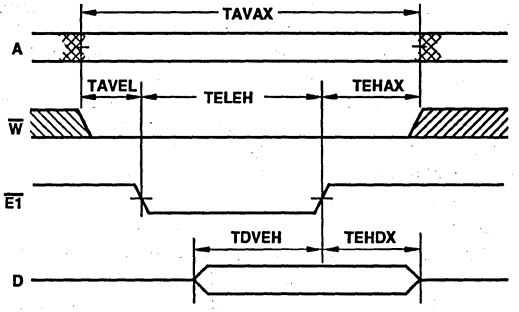


HS-65643RH, HS-6547RH Asynchronous Write Cycles

WRITE CYCLE I: LATE WRITE

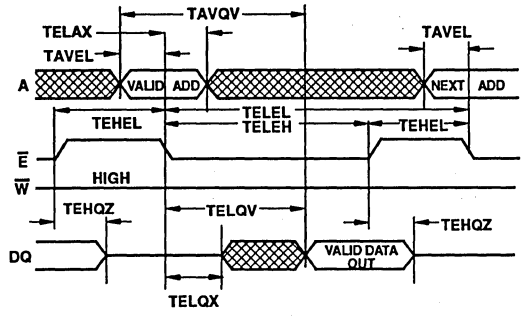


WRITE CYCLE II: EARLY WRITE - CONTROLLED BY $\overline{E}$, $\overline{E1}$



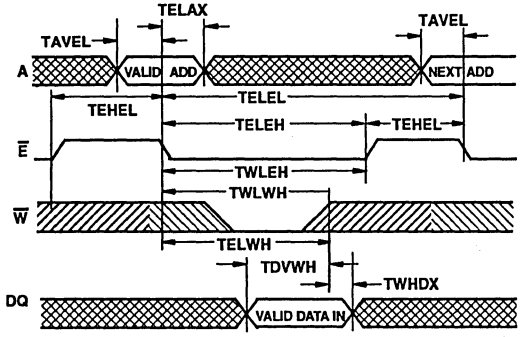
HS-65643RH, HS-65647RH Synchronous Operation

READ CYCLE



The address information is latched in the HSC373's on the falling edge of $\overline{E}$ or $\overline{E1}$; minimum address setup and hold time requirements at the SRAM must be met. After the required hold time, the addresses may change state without affecting device operation. $\overline{W}$ must remain high throughout the read cycle. After the data has been read, $\overline{E}$ or $\overline{E1}$ may return high. This will force the output buffers into a high impedance mode after TEHQZ elapses.

WRITE CYCLE



The write cycle is initiated on the falling edge of $\overline{E}$ or $\overline{E1}$ which latches the address information in the HCS373's. TDVWH and TWHDX at the SRAM inputs must be met for proper device operation. If $\overline{E}$ or $\overline{E1}$ rises before $\overline{W}$ rises, reference data setup and hold times to the $\overline{E}$ or $\overline{E1}$ rising edge. The write operation is terminated by the first rising edge of $\overline{W}$, $\overline{E}$, or $\overline{E1}$. After the minimum $\overline{E}$ high time (TEHEL), the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising edge of $\overline{E}$ or $\overline{E1}$.

Harris Semiconductor

APPNOTE

No. 9106 June 1992

Military and Aerospace

SPECIAL ESD CONSIDERATIONS FOR THE HS-65643RH AND HS-65647RH RADIATION HARDENED SOS SRAMs

Author: Steve Rivet

The HS-65643RH and HS-65647RH SRAMs are fabricated on TSOS4, an advanced 1.25mm dual level metal silicon on sapphire process. The sapphire substrate used in this process is an excellent electrical insulator, and allows the SRAMs to operate in a wide variety of extremely severe radiation environments; however, the sapphire is also a good thermal insulator, which makes dissipation of heat generated in ESD protection devices difficult. This situation leads to ESD immunity levels of 1000V - 2000V (HBM testing) for these SRAMs.

Until recently, the human body model (HBM) was the accepted standard for the evaluation of a semiconductor's susceptibility to electrostatic discharge induced damage. The charged device model (CDM) was proposed by Speakman (1) in 1974 to more accurately model the electrostatic discharges most commonly resulting in damage to current generation, small geometry semiconductors; the CDM is now generally accepted as the best approximation to charged metal surfaces, the worst case situation generally encountered. The equivalent circuit for this model is shown in Figure 1, and a test circuit implementing the model is shown in Figure 2. The voltage threshold levels at which damage to semiconductor devices occurs is typically much lower for CDM than HBM waveforms; the failure modes are also significantly different.

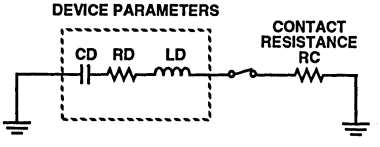


FIGURE 1. CDM EQUIVALENT CIRCUIT PROPOSED BY BOSSARD, CHEMELLI AND UNGER

During HBM discharges the voltage rise at the stressed pin is slow enough for active protection devices to turn on. The failure mechanism is normally metal penetration of the protection device junctions (2), or melting of the input or output protection resistors (3). CDM discharges are oscilla- tory, and have very fast voltage rise times. Active protection devices do not have time to turn on to their low impedance state; failure modes are typically punctures of the gate or field oxides (4).

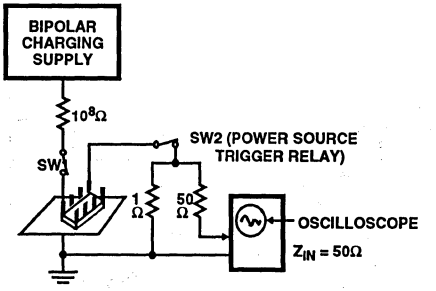


FIGURE 2. CHARGED DEVICE MODEL TEST CIRCUIT PROPOSED BY BOSSARD, CHEMELLI AND UNGER

HBM testing of the SRAMs has shown an immunity level of 1000V for the HS-65643RH and 1200V for the HS-65647RH. The most sensitive pins are I/O's, where the metal migrates into the source of the N or P channel output device. (See Figure 3 for input, Figure 4 for I/O, protection structures. Figure 5 shows the gated diodes in cross section.) This failure mode is consistent with the HBM damage observed by Pierce (2). Input pins, however, fail at levels 800V to 1000V higher than I/O's; in these pins melting of the P+ epi resistor (which is thermally and electrically insulated in TSOS4) is the failure mode.

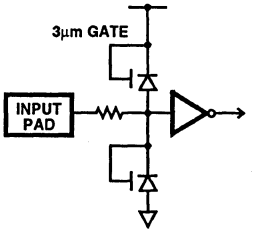


FIGURE 3.

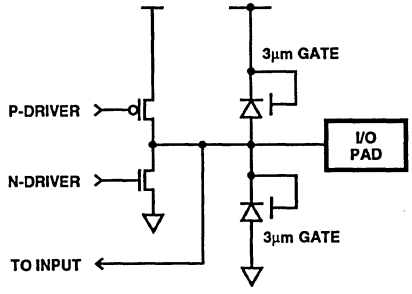


FIGURE 4.

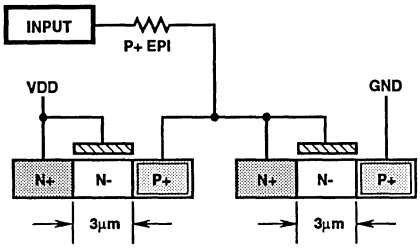


FIGURE 5. TSOS4 GATED DIODE INPUT

CDM testing of the HS-65643RH and 65647RH has not yet been performed. Failure modes for HBM testing of TSOS4 material are consistent with those already documented for JI material; results of CDM waveform testing for the TSOS4 devices are also expected to yield correspondingly lower immunity levels.

The fairly low ESD immunity levels characteristic of these SRAMs (and consequently, of other circuits produced on SOS processes) dictate that ESD prevention measures be scrupulously administered. Precautions related to grounding personnel and work stations are insufficient; any automated handling equipment must be carefully evaluated for accumulation of CDM-like static charge. A good static control program will allow the use of these high performance, extremely hard devices while maintaining the highest quality and reliability standards designed and built into them.

References

1) T. S. Speakman, "A Model for Failure of Bipolar Silicon Integrated Circuits Subject to Electrostatic Discharge." 12th Annual Proceedings of the Reliability Physics Symposium, pp. 60-69, April 1974.

2) D. G. Pierce, "Electro-Thermomigration as an Electrical Overstress Failure Mechanism." EOS/ESD Symposium Proceedings, pp. 67-76, 1986.

3) J. E. Clark, "TSOS4 ESD Test Results and Failure Analysis," internal Harris Semi. memo, 20 August, 1990.

4) L. R. Avery, "Charged Device Model Testing; Trying to Duplicate Reality," EOS/ESD Symposium Proceedings, pp 88-92, 1987.

RAD HARD 14

QUALITY AND RELIABILITY

Basic Operating Principles for Quality First

Customer Focus

Customer satisfaction is the paramount purpose of all company activities. Meeting the requirements and value expectations of our internal and external customers is the primary task of every employee.

Continuous Improvement

Our planning activities will recognize continuous improvement as a primary business objective. Our products and services, together with the processes and systems which produce them, will be world class.

Employee Improvement

We will provide an environment and related value system in which all Harris people are personally involved, individually and as team members, in establishing and achieving quality goals.

Supplier Partnerships

We will develop and maintain mutually beneficial partnerships with suppliers who share our commitment to achieving increasing levels of customer satisfaction through continuing improvements in quality, service, timeliness and cost.

Highest Standards of Conduct, Ethics and Integrity

We will conduct our business in strict compliance with applicable laws, rules and regulations; with honesty and integrity; and with a strong commitment to the highest standards of business ethics.

Quality and Reliability

Introduction

The needs of the military and aerospace community for a wide variety of specialized, hi-rel microcircuits are filled by the Harris Military and Aerospace Division. These circuits are typically manufactured to Mil-M-38510 and Mil-Std-883, as well as to unique customer requirements. In all cases, Harris is committed to continue its tradition of supplying only the highest quality devices for hi-rel applications.

Harris Semiconductor's commitment to supply only top value integrated circuits has made quality improvement a mandate for every person in our work force - from circuit designer to manufacturing operator, from hourly employee to corporate executive. Price is no longer the only determinant in marketplace competition. Quality, reliability, and performance enjoy significantly increased importance as measures of value in integrated circuits.

Quality in integrated circuits cannot be added on or considered after the fact. It begins with the development of capable process technology and product design. It continues in manufacturing, through effective controls at each process or step. It culminates in the delivery of products which meet or exceed the expectations of the customer.

The Role of the Quality Organization

The emphasis on building quality into the design and manufacturing processes of a product has resulted in a significant refocus of the role of the Quality organization. This group facilitates the development of Statistical Process Control (SPC) and Design of Experiments (DOX) programs and works with manufacturing to establish control charts. In addition, Quality professionals are involved in the measurement of equipment capability, standardization of inspection equipment and processes, procedures for chemical controls, analysis of inspection data and feedback to the manufacturing areas, coordination of efforts for process and product improvement, optimization of environmental or raw materials quality, and the development of quality improvement programs with vendors.

"Total Quality Management" at Harris requires ownership and responsibility by each person at every level of the organization. At critical manufacturing operations, process and product quality is analyzed through random statistical sampling and product monitors. The Quality organization's role is changing from policing quality to leadership and coordination of quality programs or procedures in other organizations - through auditing, sampling, consulting, and managing Quality Improvement projects.

To support specific market requirements, or to ensure conformance to military or customer specifications, the Quality organization still performs many of the conventional quality functions (e.g., group testing for military products or wafer lot acceptance). But, true to the philosophy that quality is everyone's job, much of the traditional on-line measurement and control of quality characteristics is where it belongs - with the people who make the product. The Quality organization is there to provide leadership and assistance in the deployment of quality techniques, and to monitor progress. (See Figure 3 and Table 4.)

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/QC MONITOR AUDIT
Wafer Fab	• JAN Self-Audit		X
	• Environmental		
	- Room/Hood Particulates	X	X
	- Temperature/Humidity	X	X
	- Water Quality		X
	• Product		
	- Junction Depth	X	
	- Sheet Resistivities	X	
	- Defect Density	X	X
	- Critical Dimensions	X	X
	- Visual Inspection	X	X
	- Lot Acceptance	X	
	• Process		
	- Film Thickness	X	X
	- Implant Dosages	X	
	- Capacitance Voltage Changes	X	X
	- Conformance to Specification	X	X
	• Equipment		
	- Repeatability	X	X
	- Profiles	X	X
	- Calibration		X
	- Preventive Maintenance	X	X

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS (Continued)

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/QC MONITOR AUDIT
Assembly	• JAN Self-Audit		X
	• Environmental		
	- Room/Hood Particulates	X	X
	- Temperature/Humidity	X	X
	- Water Quality		X
	• Product		
	- Documentation Check		X
	- Dice Inspection	X	X
	- Wire Bond Pull Strength/Controls	X	X
	- Die Sear Controls		X
	- Pre-Seal Visual	X	X
	- Fine/Gross Leak	X	X
	- PIND Test	X	
	- Lead Finish Visuals, Thickness	X	X
	- Die Shear		X
	- Solderability		X
	• Process		
	- Operator Quality Performance	X	X
	- Saw Controls	X	
	- Die Attach Temperatures	X	X
	- Seal Parameters	X	
	- Seal Temperature Profile	X	X
	- Sta-Bake Profile	X	
	- Temp Cycle Chamber Temperature	X	X
	- ESD Protection	X	X
	- Plating Bath Controls	X	
	- Mold Parameters	X	X
Test	• JAN Self-Audit		X
	• Temperature/Humidity	X	X
	• ESD Controls	X	
	• Temperature Test Calibration	X	
	• Test System Calibration	X	
	• Test Procedures	X	
	• Control Unit Compliance	X	
	• Lot Acceptance Conformance	X	
	• Group A Lot Acceptance		X
Probe	• JAN Self-Audit		X
	• Wafer Repeat Correlation	X	
	• Visual Requirements	X	X
	• Documentation	X	X
	• Process Performance	X	X
Burn-In	• JAN Self-Audit		X
	• Functionality Board Check		X
	• Oven Temperature Controls	X	
	• Procedural Conformance		X
Brand	• JAN Self-Audit		X
	• ESD Controls	X	X
	• Brand Permanency	X	X
	• Temperature/Humidity	X	X
	• Procedural Conformance		X
QCI Inspection	• JAN Self-Audit		X
	• Group B Conformance		X
	• Group C and D Conformance		X

Designing for Manufacturability

Assuring quality and reliability in integrated circuits begins with good product and process design. This has always been a strength in Harris Semiconductor's quality approach. We have a very long lineage of high reliability, high performance products that have resulted from our commitment to design excellence. All Harris products are designed to meet the stringent quality and reliability requirements of the most demanding end equipment applications, from military and space to industrial and telecommunications. The application of new tools and methods has allowed us to continuously upgrade the design process.

Each new design is evaluated throughout the development cycle to validate the capability of the new product to meet the end market performance, quality, and reliability objectives.

The validation process has four major components:

1. Design simulation/optimization
2. Layout verification
3. Product demonstration
4. Reliability assessment.

Harris designers have an extensive set of very powerful Computer-Aided Design (CAD) tools to create and optimize product designs (see Table 2).

Harris Semiconductor Standard Process Flows

Harris Semiconductor offers a variety of Mil-Std-883 compliant and non-compliant standard screening flows for cost-effective support of the customer's specific testing and reliability requirements. These flows include environmental stress testing, burn-in and electrical testing at room, high and low temperatures. The Mil-Std-883/JAN Quality Conformance Inspections are shown on pages 14-6 to 14-23. In addition, Harris can supply products tested to customer specifications for both electrical requirements and non-standard environmental stress screening. Consult your field sales representative for details.

TABLE 2. APPROACH AND IMPACT OF STATISTICAL QUALITY TECHNOLOGY

STAGE		APPROACH	IMPACT
I	Product Screening	• Stress and Test • Defective Prediction	• Limited Quality • Costly • After-The-Fact
II	Process Control	• Statistical Process Control • Just-In-Time Manufacturing	• Identifies Variability • Reduces Costs • Real Time
III	Process Optimization	• Design of Experiments • Process Simulation	• Minimizes Variability • Before-The-Fact
IV	Product Optimization	• Design for Producibility • Product Simulation	• Insensitive to Variability • Designed-In Quality • Optimal Results

TABLE I. MIL-STD-883/JAN QUALITY CONFORMANCE INSPECTIONS GROUP A ELECTRICAL TESTS FOR CLASSES S AND B DEVICES (NOTE 1)

SUBGROUPS (NOTE 2) **QUALITY/ACCEPT NO. = 116/0** (NOTES 3, 4, 5)	
Subgroup 1	Static tests at +25°C
Subgroup 2	Static tests at maximum rated operating temperature
Subgroup 3	Static tests at minimum rated operating temperature
Subgroup 4	Dynamic tests at +25°C
Subgroup 5	Dynamic tests at maximum rated operating temperature
Subgroup 6	Dynamic tests at maximum rated operating temperature
Subgroup 7	Functional tests at +25°C
Subgroup 8A	Dynamic tests at maximum rated operating temperature
Subgroup 8B	Dynamic tests at minimum rated operating temperature
Subgroup 9	Switching tests at +25°C
Subgroup 10	Switching tests at maximum rated operating temperature
Subgroup 11	Switching tests at minimum rated operating temperature

NOTES:

1. The specific parameters to be included for tests in each subgroup shall be as specified in the applicable acquisition document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.
2. At the manufacturer's option, the applicable tests required for group A testing (see Note 1) may be conducted individually or combined into sets of tests, subgroups (as defined in Table 1), or sets of subgroups. However, the manufacturer shall predesignate these groupings prior to group A testing. Unless otherwise specified, the individual tests, subgroups, or sets of tests/subgroups may be performed in any sequence.
3. The sample plan (quantity and accept number) for each test, subgroup, or set of tests/subgroups as predesignated in Note 2, shall be 116/0.
4. A greater sample size may be used at the manufacturer's option; however, the accept number shall remain at zero. When the (sub)lot size is less than the required sample size, each and every device in the (sub)lot shall be inspected and all failed devices removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable.
5. If any device in the sample fails any parameter in the test, subgroup, or set of tests/subgroups being sampled, each and every additional device in the (sub)lot represented by the sample shall be tested on the same test set-up for all parameters in that test, subgroup, or set of tests/subgroups for which the sample was selected, and all failed devices shall be removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicalbe. For class S only, if this testing results in a percent defective greater than 5 percent, the (sub)lot shall be rejected, except that for (sub)lots previously unscreened to the tests that caused failure of this percent devective, the (sub)lot may be accepted by resubmission and passing the failed individual tests, subgroups, or set of tests/subgroups, as applicable, using a 116/0 sample.

HARRIS STANDARD RAD HARD PRODUCT DATA PACKAGES

	A	B	C	D	E	F	G	H	I	J
Die	•	•						•		•
JAN Class B (Note 1)	•	•		•						
CD4XXX Series (Notes 2, 3)						•	•			•
JAN Class S	•	•	•	•	•					
CD4XXX Series (Note 4)						•	•	•	•	•
MSR, CD4XXX, HC/HCTS	•	•	•	•	•	•		•	•	•
Memory, Microprocessor, Analog	•	•	•	•	•	•		•	•	•
Harris Noncompliant Space Flow										
Memory, Microprocessor, Analog		•		•		•				•
Harris Noncompliant Class B Flow										
Memory, Microprocessor and Analog (Note 1)	•	•		•		•				
/883 (Note 2, 3)							•			•
Memory, Microprocessor and Analog (Note 4)	•	•	•	•	•	•				
/883S							•	•	•	•

NOTES:

1. Attributes from burn-in through end of 100% screening operations.
2. Groups A, B, C and D data summary.
3. Per applicable JAN requirements.
4. Groups A, B and D data summary.

A. Cover Sheet: (Will include as a minimum)
- Purchase Order Number and Revision
- Customer Part Number
- Lot Date Code
- Harris Part Number
- Lot Number
- Quantity

B. Certificate of Conformance
- As found on Shipper

C. Lot Serial Number Sheet
- Good unit(s) serial numbers and lot number

D. Screening Attributes Data
- Identify test operations
- Quantity of units subjected to each test operation
- Quantity accepted after test operation was performed
- Date of each test
- Attributes from post encapsulation screening through end of 100% screening operations

E. Variables data for all read/record and/or delta operations. Each value shall be identified to the specific serial number of the device for which the data represents.

F. Groups A attributes data summary

G. Groups B and D data summary is only available on JAN product or R-Spec product. Conformance data is not available on standard product.

H. Wafer Lot Acceptance Report (Method 5007) to include SEM photographs
*Note: SEM photographs to include % of step coverage
*Note: If more than one shipment is made from the same wafer lot, only the initial shipment will include the SEM photograph.

I. X-Ray report and Film(s) - including penetrameter measurements.

J. GAMMA Radiation Report with each shipment of devices.

HARRIS SMALL LOT GROUP B (CLASS B) SAMPLE PLAN (NOTES 1, 2)

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LOT SIZE/QUANTITY (ACC NO) OR LTPD 0 - 50	51 - 100	101 - 200	(NOTE 9) > 200
SUBGROUP 2 (Note 3)						
a. Resistance to Solvents	2015		2 (0)	2 (0)	4 (0)	4 (0)
SUBGROUP 3						
a. Solderability (Note 4) # Devices # Bond Pulls	2003 or 2022		1	2	3 LTPD = 10	3 LTPD = 10
SUBGROUP 5						
a. Bond Strength (Note 5) #Devices # Bond Pulls	2011	Test Condition C	1 (Note 7)	1 (Note 7)	1 (Note 7)	4 LTPD = 15

NOTES:

1. Electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required provided that the rejects are processed identically to the inspection lot through pre-burn-in electricals and provided the rejects are exposed to the full time/temperature exposure of burn-in.
2. Subgroups 1, 4, 6, 7 and 8 have been deleted from this table. For convenience, the remaining subgroups will not be renumbered.
3. Resistance to solvents testing required only on devices using inks or paints as the marking or contrast medium. Resistance to solvent testing shall consist of subjecting 1 unit to solvent C and 1 unit to solvent D only.
4. All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the time/temperature exposure of burn-in. All leads shall be tested for packages with lead counts ≤ 22. For packages with lead counts ≥ 22, the number of leads shall be based on an LTPD of 10.
5. Test samples for bond strength may, at the manufacturer's option, unless otherwise specified, be randomly selected prior to or following internal visual (PRESEAL) inspection specified in method 5004, prior to sealing provided all other specifications requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond strength samples shall be counted even if the bond would have failed internal visual examination). All wires shall be tested for packages with lead counts ≤ 15. For packages with wire counts ≥ 15, the number of wires shall be based on an LTPD of 15.

HARRIS SMALL LOT GROUP C (CLASS B) SAMPLE PLAN (NOTE 1)

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LOT SIZE/QUANTITY (ACC NO) OR LTPD 0 - 50	51 - 100	101 - 200	(NOTE 9) > 200
SUBGROUP 1						
			8 (0)	15 (0)	20 (0)	77 (1)
a. End-Point Electrical Parameters		Per applicable device specification				
b. Steady State Life	1005	Test condition per device specification				
c. End-Point Electrical Parameters		Per applicable device specification				

HARRIS SMALL LOT GROUP D (CLASS B) SAMPLE PLAN (NOTE 1)

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LOT SIZE/QUANTITY (ACC NO) OR LTPD 0 - 50	51 - 100	101 - 200	(NOTE 9) > 200
SUBGROUP 1						
a. Physical Dimension (Note 2)	2016		3 (0)	3 (0)	5 (0)	15 (0)
SUBGROUP 2						
a. Lead Integrity # Devices # Leads	2004		 1 5 (0)	 2 10 (0)	 3 15 (0)	 3 45 (0)
b. Seal a. Fine b. Gross	1014		1 (0)	2 (0)	3 (0)	3 (0)
SUBGROUP 3						
			3 (0)	3 (0)	5 (0)	25 (1)
a Thermal Shock	1011	Per applicable	3 (0)	3 (0)	5 (0)	25 (1)
b. Temperature Cycling	1010					
c. Moisture Resistance	1004					
d. Seal a. Fine b. Gross	1014					
e. Visual Examination	1004, 1010					
f. End-Point Electrical Parameters		Per applicable device specification				
SUBGROUP 4						
			3 (0)	3 (0)	5 (0)	25 (1)
a. Mechanical Shock	2002					
b. Vibration, Variable Frequency	2007					
c. Constant Acceleration	2001					
d. Seal a. Fine b. Gross	1014					
e. Visual Examination	1010 or 1011					
f. End-Point Electrical Parameters		Per applicable device specification				
SUBGROUP 5						
			3 (0)	3 (0)	5 (0)	15 (0)
a. Salt Atmosphere	1009					
b. Seal a. Fine b. Gross	1014					
c. Visual Examination	1009	Visual criteria only				
SUBGROUP 6						
a. Internal Water-vapor Content	1018	5,000ppm maximum water content at 100°C	1 (0) or 3 (0)	1 (0) or 3 (0)	2 (0) or 4 (1)	3 (0) or 5 (1)
SUBGROUP 7						
a. Adhesion of Lead Finish # Devices # Leads	2025		 1 5 (0)	 2 10 (0)	 3 15 (0)	 3 15 (0)
SUBGROUP 8						
a Lid Torque	2024		1 (0)	2 (0)	3 (0)	5 (0)
TOTAL # OF GOOD DEVICES REQUIRED:			9	9	14	55

NOTES:

1. The notes of Table IV, MIL-STD-883, method 5005 shall apply in addition to the Notes specified herein. This table is used for reference to sampling plan only. The actual tests and subgroups required to be inspected shall be in accordance with the latest revision of Table IV, MIL-STD-883, method 5005.
2. Units may be selected at any time after device sealing operation and in the final lead finish. Rejects may be used for these subgroup tests.
3. The > 200 column sample sizes are based on those currently specified in method 5005.

ATTACHMENT I. HARRIS SMALL LOT GROUP B (CLASS S) SAMPLE PLAN (NOTE 1)

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LOT SIZE/QUANTITY (ACC NO) OR LTPD 0 - 50	51 - 100	101 - 200	(NOTE 9) > 200
SUBGROUP 1						
a. Physical Dimension (Note 2)	2016		1 (0)	1 (0)	2 (0)	2 (0)
b. Internal Water-Vapor Content (Note 3)	1018	5,000ppm max water content at +100°C	1 (0)	1 (0)	2 (0)	2 (0)
SUBGROUP 2						
a. Resistance to Solvents	2015		2 (0) (Note 4)	2 (0) (Note 4)	4 (0)	4 (0)
b. Internal Visual and Mechanical	2013, 2014		1 (0)	1 (0)	1 (0)	2 (0)
c. Bond Strength # Devices # Bond Pulls	2011	Test Condition C	1 (Note 5)	1 (Note 5)	1 (Note 5)	3 LTPD = 10
d. Die Shear	2019		1 (0)	1 (0)	1 (0)	1 (0)
SUBGROUP 3						
Solderability # Devices # Leads	2003 or 2022		1 (Note 5)	2 (Note 5)	3 LTPD = 10	3 LTPD = 10
SUBGROUP 4						
a. Lead Integrity	2004	Test Condition B2	1 (0) (Note 6)	2 (0) (Note 6)	2 (0) (Note 6)	2 (0) (Note 6)
b. Seal a. Fine b. Gross	1014	Test Condition B2				
c. Lid Torque						
SUBGROUP 5						
a. End-Point Electrical Parameters		Per applicable device specification	8 (0)	15 (0)	20 (0)	77 (1)
b. Steady State Life	1005	Test condition per device specification				
c. End-Point Electrical Parameters		Per applicable device specification				
SUBGROUP 6 (Note 7)						
a. End-Point Electrical Parameters		Per applicable device specification	3 (0)	3 (0)	5 (0)	25 (1)
b. Temperature Cycling	1010	Condition C, 100 cycles				
c. Constant Acceleration	2001	Condition E, Y1 Orientation				
d. Seal a. Fine b. Gross	1014					
e. End-Point Electrical Parameters		Per applicable device specification				
SUBGROUP 7						
a. End-Point Electrical Parameters		Group A and delta limits in accordance with method 3015	(Note 8)	(Note 8)	(Note 8)	15 (0) (Note 8)
b. Electrostatic Discharge	3015					
c. End-Point Electrical Parameters		Group A and delta limits in accordance with method 3015				
TOTAL # GOOD UNITS REQUIRED:			12	18	26	102

See Notes Next Page

NOTES:

1. The Notes of Table IIa, MIL-STD-883, method 5005 shall apply in addition to the Notes specified herein.
2. Units may be selected at any time after device sealing operation and in the final lead finish. Rejects may be used for these subgroup tests.
3. Units may be selected at any time after burn-in and need not be branded.
4. Resistance to solvent testing shall consist of subjecting 1 unit to solvent C and 1 unit to solvent D only.
5. All wires or leads (as applicable) shall be tested for packages with lead counts ≤ 22. For packages with lead counts ≥ 23, the number of wires or leads shall be based upon an LTPD of 10.
6. 3 leads per device shall be sampled.
7. Subgroup B-6 is nondestructive based on Harris test results of this subgroup per MIL-M-38510.
8. Subgroup 7 is performed for initial qualification and product redesign as a minimum. Sample size will be 3 (0) with repeat for cumulative effects 15 (0).
9. The > 200 pieces column sample sizes are based upon those specified in method 5005.

ATTACHMENT I - HARRIS SMALL LOT GROUP D (CLASS S) SAMPLE PLAN (NOTE 1)

	MIL-STD-883		LOT SIZE/QUANTITY (ACC NO) OR LTPD			
TEST	**METHOD**	**CONDITION**	**0 - 50**	**51 - 100**	**101 - 200**	(NOTE 3) **> 200**
SUBGROUP 1						
a. Physical Dimension (Note 2)	2016		3 (0)	3 (0)	5 (0)	15 (0)
SUBGROUP 2						
a. Lead Integrity # Devices # Leads	2004		1 5 (0)	2 10 (0)	3 15 (0)	15 45 (0)
b. Seal a. Fine b. Gross	1014		1 (0)	2 (0)	3 (0)	15 (0)
SUBGROUP 3						
a. Thermal Shock	1011		3 (0)	3 (0)	5 (0)	25 (1)
b. Temperature Cycling	1010					
c. Moisture Resistance	1004					
d. Seal a. Fine b. Gross	1014					
e. Visual Examination	1004, 1010					
f. End-Point Electrical Parameters		Per applicable device specification				
SUBGROUP 4						
			3 (0)	3 (0)	5 (0)	25 (1)
a. Mechanical Shock	2002					
b. Vibration, Variable Frequency	2007					
c. Constant Acceleration	2001					
d. Seal a. Fine b. Gross	1014					
e. Visual Examination	1010 or 1011					
f. End-Point Electrical Parameters		Per applicable device specification				
SUBGROUP 5						
a. Salt Atmosphere	1009		3 (0)	3 (0)	5 (0)	15 (0)
b. Seal a. Fine b. Gross	1014					
c. Visual Examination	1009	Visual criteria only				

ATTACHMENT I - HARRIS SMALL LOT GROUP D (CLASS S) SAMPLE PLAN (NOTE 1) **(Continued)**

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LOT SIZE/QUANTITY (ACC NO) OR LTPD 0 - 50	51 - 100	101 - 200	(NOTE 3) > 200
SUBGROUP 6						
a. Internal Water-Vapor Content	1018	5,000ppm max water content at +100°C	1 (0) or 3 (0)	1 (0) or 3 (0)	2 (0) or 4 (1)	3 (0) or 5 (1)
SUBGROUP 7						
a. Adhesion of Lead Finish # Devices # Leads	2025		 1 5 (0)	 2 10 (0)	 3 15 (0)	 3 15 (0)
SUBGROUP 8						
a. Lid Torque	2024		1 (0)	2 (0)	3 (0)	5 (0)
TOTAL # GOOD UNITS REQUIRED:			9	9	14	55

NOTES:

1. The Notes of Table IV, MIL-STD-883, method 5005 shall apply in addition to the Notes specified herein.
2. Units may be selected at any time after device sealing operation and in the final lead finish. Rejects may be used for these subgroup tests.
3. The > 200 pieces column sample sizes are based upon those specified in method 5005.

TABLE IIA. MIL-STD-883/JAN QUALITY CONFORMANCE INSPECTIONS GROUP B TESTS FOR CLASS S DEVICES (NOTE 1)

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	QUANTITY/ (ACCEPT NO.) OR LTPD
SUBGROUP 1			
A. Physical dimensions (Note 2)	2016		2(0)
B. Internal water-vapor content (Notes 2, 3)	1018	5,000 ppm maximum water content at +100°C	3(0) or 5(1) (Note 4)
SUBGROUP 2 (Note 5)			
A. Resistance to solvents	2015	4(0)	
B. Internal visual and mechanical	2013, 2014	Failure criteria from design and construction requirements of applicable acquisition document	2(0)
C. Bond Strength	2011		LTPD = 10 (Note 6)
1. Thermo compression		1. Test condition C or D	
2. Ultrasonic		2. Test condition C or D	
3. Flip-chip		3. Test condition F	
4. Beam lead		4. Test condition H	
D. Die shear test		In accordance with Method 2019 for the applicable die size	3(0)
SUBGROUP 3			
Solderability (Note 7)	2003 or 2022	Soldering temperature of 245°C 5°C	LTPD = 10
SUBGROUP 4 (Note 2)			
A. Lead integrity (Note 8)	2004	Test condition B_2, lead fatigue	2(0)
B. Seal a. Fine	1014	As applicable	
C. Lid torque (Note 9)	2024	As applicable	

TABLE IIA. MIL-STD-883/JAN QUALITY CONFORMANCE INSPECTIONS GROUP B TESTS FOR CLASS S DEVICES (NOTE 1) **(Continued)**

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	QUANTITY/ (ACCEPT NO.) OR LTPD
SUBGROUP 5 (Note 10)			
A End-point electrical parameters (Notes 11, 12)		As specified in the applicable device specification	
B. Steady state life (Note 13)	1005	Test condition C, D or E	LTPD = 5
C. End-point electrical parameter (Note 11)		As specified in the applicable device specification	
SUBGROUP 6			
A End-point electrical parameters		As specified in the applicable device specification	LTPD = 15
B. Temperature cycling	1010	Condition C, 100 cycles minimum	
C. Constant acceleration	2001	Test condition E: Y_1 orientation only	
D. Sea a. Fine b. Gross	1014		
E. End-point electrical parameters		As specified in the applicable device specification	

NOTES:

1. Post burn-in electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required.
2. Not required for qualification or quality conformance inspections where group D inspection is being performed on samples from the same inspection lot.
3. This test is required only if it is a glass-frit-sealed package. Unless handling precautions for beryllia packages are available and followed method 1018, procedure 3 shall be used. See Note 6 of Table 4.
4. Test three devices; if one fails, test two additional devices with no failures. At the manufacturer's option, if the initial test sample (i.e., 3 or 5 devices) fails, a second complete sample may be tested at an alternate laboratory that has been granted current suitability status by the qualifying activity. If this sample passes, the lot shall be accepted provided the devices and data from both submissions are submitted to the qualifying activity along with five additional devices from the same lot.
5. Resistance to solvents testing required only on devices using inks or paints as a marking medium.
6. Unless otherwise specified, the LTPD sample size for conditions C and D is the number of bond pulls selected from a minimum number of four devices, and for condition F or H is the number of dice (not bonds).
7. All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin fusing after burn-in. The LTPD applies to the number of leads inspected except in no case shall less than three devices be used to provide the number of leads required.
8. For leadless chip carrier packages only, use test condition D. For pin grid array leads and rigid leads use method 2028. See method 5005.11
9. Lid torque test shall apply only to glass-frit-sealed packages.
10. The alternate removal-of-bias provisions of 3.3.1 of method 1005 shall not apply for test temperatures above 125°C.
11. Read and record group A subgroups 1, 2 and 3.
12. For qualification, read and record data for all group A subgroups satisfies the data requirement of Mil-M-38510, 4.4.2.1.6A.
13. The same test temperature that was used for burn-in shall be used for the steady-state life test.
14. Unless otherwise specified, test shall be performed for initial qualification and product redesign as a minimum.

TABLE IIB. MIL-STD-883/JAN QUALITY CONFORMANCE INSPECTIONS GROUP B TESTS FOR CLASS B DEVICES (NOTES 1, 2)

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	QUANTITY/ (ACCEPT NO.) OR LTPD
SUBGROUP 2 (Note 3)			
A. Resistance to solvents	2015	4(0)	
SUBGROUP 3			
A. Solderability (Note 4)	2022 or 2003	Soldering temperatures of 245°C ± 5°C	10
SUBGROUP 5			
A. Bond Strength (Note 5) 1. Thermocompression 2. Ultrasonic or wedge 3. Flip-chip 4. Beam lead	2011	1. Test condition C or D 2. Test condition C or D 3. Test condition F 4. Test condition H	15

NOTES:

1. Post burn-in electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required.
2. Subgroups 1, 4, 6, 7 and 8 have been deleted from this table. For convenience, the remaining subgroups will not be renumbered.
3. Resistance to solvents testing required only on devices using inks or paints as the marking or contrast medium.
4. All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure to burn-in except for devices which have been hot solder dipped or undergone tin fusing after burn-in. The LTPD for solderability test applies to the number of leads inspected except in no case shall less than 3 devices be used to provide the number of leads required.
5. Test samples for bond strength may, at the manufacturer's option, unless otherwise specified, be randomly selected prior to or following internal visual (PRESEAL) inspection specified in method 5004, prior to sealing provided all other specifications requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond strength samples shall be counted even if the bond would have failed internal visual exam). Unless otherwise specified, the LTPD sample size for condition C or D is the number of bond pulls selected from a minimum number of 4 devices, and for condition F or H is the number of dice (not bonds) (see method 2011).

TABLE III. MIL-STD-883/JAN QUALITY CONFORMANCE INSPECTIONS GROUP C DIE-RELATED TESTS FOR CLASS B ONLY

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	QUANTITY/ (ACCEPT NO. OR LTPD
SUBGROUP 1			
A. Steady-state life test	1005	Test condition to be specified (1,000 hours at 125°C)	5
B. End point electrical parameters		As specified in the applicable device specification	

TABLE IV. MIL-STD-883/JAN QUALITY CONFORMANCE INSPECTIONS GROUP D PACKAGE RELATED TESTS FOR ALL CLASSES

(NOTE 1) TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	QUANTITY/ (ACCEPT NO.) OR LTD
SUBGROUP 1 (Note 2)			
A. Physical dimensions	2016		15
SUBGROUP 2 (Note 2)			
A. Lead integrity (Note 3)	2004	Test condition B2 (lead fatigue)	15
B. Seal (Note 4) 1. Fine 2. Gross	1014	As applicable	

TABLE IV. MIL-STD-883/JAN QUALITY CONFORMANCE INSPECTIONS GROUP D PACKAGE RELATED TESTS FOR ALL CLASSES (Continued)

(NOTE 1) TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	QUANTITY/ (ACCEPT NO.) OR LTD
SUBGROUP 3 (Note 5)			
A. Thermal shock	1011	Test condition B as a minimum, 15 cycles minimum	15
B. Temperature cycling	1010	Test condition C, 100 cycles minimum	
C. Moisture resistance (Note 6)	1004		
D. Seal a. Fine b. Gross	1014	As applicable	
E. Visual examination		In accordance with visual criteria of method 1004 and 1010	
F. End-point electrical parameters (Note 7)		As specified in the applicable device specification	
SUBGROUP 4 (Note 5)			
A. Mechanical shock	2002	Test condition B minimum	15
B. Vibration, variable frequency	2007	Test condition A minimum	
C. Constant acceleration	2001	Test condition E minimum (see 3), Y1 orientation only	
D. Seal a. Fine b. Gross	1014	As applicable	
E. Visual examination Note 8			
F. End-point electrical parameters		As specified in the applicable device specification	
SUBGROUP 5 (Note 2)			
A. Salt atmosphere (Note 6)	1009	Test condition A minimum	15(0)
B. Seal a. Fine b. Gross	1014	As applicable	
C. Visual examination		In accordance with visual criteria of method 1009	
SUBGROUP 6 (Note 2)			
A. Internal water-vapor content	1018	5,000 ppm maximum water content at 100°C	3(0) or 5(1) (Note 9)
SUBGROUP 7 (Note 2)			
A. Adhesion of lead finish (Notes 10, 11)	2025	15(0)	
SUBGROUP 8			
A. Lid torque (Notes 2, 12)	2024		5(0)

NOTES:

1. In-line monitor data may be substituted for subgroups D1, D2, D6, D7 and D8 upon approval by the qualifying activity. The monitors shall be performed by package type and to the specified subgroup test method(s). The monitor sample shall be taken at a point where no further parameter change occurs, using a sample size and frequency of equal or greater severity than specified in the particular subgroup. This in-line monitor data shall be traceable to the specific inspection lot(s) represented (accepted or rejected) by the data.
2. Electrical reject devices from that same inspection lot may be used for samples.
3. For leadless chip carrier packages only, use test condition D. For pin grid array and other rigid leads use method 2028.
4. Seal test (subgroup 2B) need be performed only on packages having leads exiting through a glass seal.
5. Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".
6. Lead bend stress initial conditioning is not required for leadless chip carrier packages.
7. At the manufacturer's option, end-point electrical parameters may be performed after moisture resistance and prior to seal test.
8. Visual examination shall be in accordance with method 1010 or 1011.
9. Test three devices; if one fails, test two additional devices with no failures. At the manufacturer's option, if the initial test sample (i.e., 3 or 5 devices) fails a second complete sample may be tested at an alternate laboratory that has been issued suitability by the qualifying activity. If this sample passes the lot shall be accepted provided the devices and data from both submissions are submitted to the qualifying activity along with 5 additional devices from the same lot.
10. The adhesion of lead finish test shall not apply for leadless chip carrier packages.
11. Quantity/(accept number) based on number of leads.
12. Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame, lead or package body (i.e., wherever frit seal establishes hermiticity or package integrity).

TABLE V. MIL-STD-883/JAN QUALITY CONFORMANCE INSPECTIONS GROUP E RADIATION HARDNESS ASSURANCE TESTS (NOTE 1)

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	CLASS S QUANTITY/ (ACCEPT NUMBER)	CLASS S NOTES	CLASS B QUANTITY/ (ACCEPT NUMBER)	CLASS B NOTES
SUBGROUP 1 (Note 2)						
Neutron irradiation	1017	25°C				
A. Qualification			A. 11(0)	3	A. 11(0)	4
B. QCI			B. 11(0)	3	B. 11(0)	4
Endpoint electrical parameters		As specified in accordance with detail specification				
SUBGROUP 2 (Note 5)						
Steady-state total dose irradiation	1019	25°C Maximum supply voltage				
A. Qualification			A. 4(0) 2(0)	A. 6 8	A. 22(0)	7
B. QCI			B. 4(0) 2(0)	B. 6 8	B. 22(0)	7
Endpoint electrical parameters		As specified in accordance with detail specification				
SUBGROUP 3 (Note 9)						
Transient ionizing irradiation	1021 1023	25°C 25°C	11(0)	3	11(0)	4
Endpoint electrical		As specified in accordance with detail specification				

NOTES:

1. Parts used for one subgroup test may not be used for other subgroups but may be used for higher levels in the same subgroup. Total exposure shall not be considered cumulative unless testing is performed within the time limits of the test method. Group E tests may be performed prior to device screening (see 3.5.3).
2. Waive neutron tests for MOS devices except for charge coupled devices or where, by design, bipolar elements are an integral part of the device function.
3. In accordance with wafer lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).
4. In accordance with inspection lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).
5. Class B devices shall be inspected using either the class B quantity/accept number criteria as specified, or by using the class S criteria on each wafer.
6. In accordance with wafer for device types with less than or equal to 4,000 equivalent transistors/chip selected from the wafer at a radius approximately equal to two-thirds of the wafer radius, and spaced uniformly around this radius.
7. In accordance with inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 38(1).
8. In accordance with wafer for device types with greater than 4,000 equivalent transistors/chip selected from the wafer at a radius approximately equal to two-thirds of the wafer radius and spaced uniformly around this radius.
9. Upset testing during qualification on first QCI shall be conducted when specified in purchase order or contract. When specified, the same microcircuits may be tested in more than one subgroup

TABLE III. GROUP A INSPECTION (NOTE 1)

SUBGROUPS	JANS SAMPLING PLAN (N/C)	JAN, JANTX, JANTXV SAMPLING PLAN
SUBGROUP 1 (PPM-3)		
Visual and mechanical inspection (Note 2) (Mil-Std-750, method 2071)	15 device c = 0	LTPD = 5 (Note 3)
SUBGROUP 2 (PPM-2)		
DC (static) tests at 25oC	116 devices c = 0 (Notes 4, 5)	116 devices (Note 4) c = 0
SUBGROUP 3 (PPM-2)		
DC (static) tests at maximum rated and minimum rated operating temperatures	116 devices c = 0 (Notes 4, 5)	116 devices (Note 4) c = 0
SUBGROUP 4 (PPM-2)		
Dynamic tests at 25°C	116 devices c = 0 (Notes 4, 5)	116 devices (Note 4) c = 0
SUBGROUP 5		
Safe operating area test (for power transistors only): a. DC b. Clamped inductive (Notes 3, 6) c. Unclamped inductive End-point electrical measurement	LTPD = 10 (Notes 3, 6)	LTPD = 5 (Note 3)
SUBGROUP 6 (Note 7)		
Surge current (for diodes/rectifiers only) End-point electrical measurements	LTPD = 10 (Notes 3, 6)	LTPD = 10 (Note 3)
SUBGROUP 7		
Selected static and dynamic tests	LTPD = 10 (Notes 3, 6)	LTPD = 10 (Note 3)

NOTES:

1. The specific parameters to be included for tests in each subgroup shall be as specified in the applicable associated detail specification. Where no parameters have been specified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements. A single sample may be used for all subgroup testing. These tests are considered nondestructive and devices may be shipped.
2. PPM-3 applies only to mechanical inspection.
3. For these subgroups, the maximum accept number (c) shall be two.
4. If a device in the sample fails one or more test(s) in the subgroup or subgroups being sampled, each device in the (sub) lot represented by the sample may be screened for the test(s) for which the sample failed. Alternatively, an engineering evaluation shall be performed to determine an appropriate 25oC electrical screen(s) necessary to remove the failure mode. A second sample shall be tested to the failed subgroup. If the second sample fails, the same subgroup 100 percent rescreen of the failed subgroup shall be performed or the lot shall be rejected.
5. All devices required by the specified LTPD shall be subjected to subgroups 2, 3 and 4 combined.
6. All devices required by the specified LTPD shall be randomly selected from the devices subjected to subgroups 2, 3 and 4, and shall be subjected to subgroups 5, 6 and 7 combined.
7. Not applicable when performed as a 100 percent screen.

TABLE IVA. GROUP B INSPECTIONS FOR JANS DEVICES

INSPECTIONS	MIL-STD-750 METHOD	MIL-STD-750 CONDITION	QUALIFICATION AND LARGE LOT QUALITY CONFORMANCE INSPECTION SAMPLING PLAN	SMALL LOT QUALITY CONFORMANCE INSPECTION N/C
SUBGROUP 1 (NOTE 1)				
Physical dimensions	2066	Dimensions per case outline specified	10	8 devices c = 0
SUBGROUP 2 (Note 1)				
Solderability	2026	Separate samples may be used for each test. The LTPD applies to the number of loads inspected. A minimum of 3 devices shall be tested	15	6 devices c = 0
Resistance to solvents	1022			
SUBGROUP 3				
Temperature cycling (air-to-air)	1051	No dwell is required at 25°C. Test devices c = 0 condition C3, (100 cycles) except step 3 at 175°C + 5° - 0°C for t(extreme) ≤ 10 min.	10	6 devices c = 0
Surge (Note 2)	4066	As specified		
Hermetic seal a. Fine	1071	Not required for double plug diodes. Test condition G or H, max leak rate = 5×10^{-8} atm cc/s, except 5×10^{-7} atm cc/s for devices with internal cavity > 0.3 cc		
b. Gross				
Electrical measurements		As specified		
Decap-internal visual (design verification) (Note 3)	2075	Visual criteria in accordance with qualified design and internal visual precap criteria	6 devices c = 0	
SEM (when specified)	2077		6 devices c = 0	
Bond strength (wire or clip bonded devices only)	2037	The sampling plan applies to the number of wires pulled. The sample shall include a minimum of 3 devices and shall include all wire sizes		6 devices c = 0
Die shear (excluding axial leaded devices)	2017	Only devices previously subjected to the bond strength test shall be used for this test		
SUBGROUP 4				
Intermittent operation life	1037 1042	2,000 cycles, as specified Condition D	10	8 devices c = 0
Electrical measurements		Thermal response and other electrical measurements as specified		
Thermal shock (liquid-to-liquid) (For axial lead glass diodes only)	1056	25 cycles condition A		
SUBGROUP 5				
Accelerated steady-state operation life		Bias conditions as specified	10	12 devices c = 0
	1027	Eutectic die attached semiconductors: T_J = 275°C min (for 96 hours min)		
	1027	Soft solder die attached power semiconductors: T_J = 225°C min (for 168 hours min) For Schottky diodes: T_J = 175°C min (for 240 hours min)		

TABLE IVA. GROUP B INSPECTIONS FOR JANS DEVICES (Continued)

INSPECTIONS	MIL-STD-750 METHOD	MIL-STD-750 CONDITION	QUALIFICATION AND LARGE LOT QUALITY CONFORMANCE INSPECTION SAMPLING PLAN	SMALL LOT QUALITY CONFORMANCE INSPECTION N/C
	1042	Power MOSFETs: T_J = 200°C min (for 120 hours min); condition C; (see 4.6.4)		
Electrical measurements		Thermal response and other electrical measurements as specified		
Bond strength (Al-Au interconnects only)	2037	As specified. Bond strength samples shall have passed accelerated steady-state operation life	LTPD = 10, c = 0	LTPD = 10, c = 0
SUBGROUP 6				
Thermal resistance		As specified	10	8 devices c = 0
Diodes	3101			
Transistors (bipolar)	3131			
Transistors (POWERFETs)	3161			
Thyristors	3181			
IGBT	3103			
GaAs	3104			

NOTES:

1. Electrical reject devices (and X-Ray for JANS) and PIND rejects from the same inspection lot may be used for all subgroups when electrical end-point measurements are not required. Post burn-in electrical rejects may be used.
2. Surge shall be performed on rectifiers and reverse surge for transient suppressors.
3. For axial lead diodes a lead pull to destruction shall be performed.

TABLE IVB. GROUP B INSPECTIONS FOR JAN, JANTX AND JANTXV DEVICES

INSPECTIONS	MIL-STD-750 METHOD	MIL-STD-750 CONDITION	SAMPLING PLAN	SMALL LOT QUALITY CONFORMANCE INSPECTION N/C
SUBGROUP 1 (Note 1)				
Solderability	2026	Separate samples may be used for each test. The sampling plan applies to the number of leads in spected. A minimum of 3 devices shall be tested.	15	4 devices c = 0
Resistance to solvents	1022			
SUBGROUP 2				
Temperature cycling (air-to-air) except for axial lead glass diode	1051	No dwell is required at 25°C. Test condition C,except step 3 at 175°C +5°C, -0°C, (45 cycles including screening, t(extreme) > 10 min	10	6 devices c = 0
Thermal shock (liquid-to-liquid) (for axial lead glass diodes only)	1056	10 cycles, condition A		
Surge (Note 2)	4066	As specified		
Hermetic seal a. Fine Leak	1071	Not required for double plug diode. Test condition G or H, max leak rate = 5 x 10^{-8} atm cc/s, except 5 x 10^{-7} atm cc/s for devices with internal cavity > 0.3 cc		
b. Gross leak				
Electrical measurements		As specified		

TABLE IVB. GROUP B INSPECTIONS FOR JAN, JANTX AND JANTXV DEVICES (Continued)

INSPECTIONS	MIL-STD-750 METHOD	MIL-STD-750 CONDITION	SAMPLING PLAN	SMALL LOT QUALITY CONFORMANCE INSPECTION N/C
SUBGROUP 3 (Note 3)				
		A separate sample may be used for each test. 340 hours min	5	12 devices c = 0
Steady-state-operation life or intermittent operation life (Note 4)	1027 1037 1042	Bias conditions as specified Condition D, 2,000 cycles		
Electrical measurements		As specified		
Bond strength (wire or clip bonded devices only) (Rectifiers only)	2037	The sample shall include a minimum of 3 devices and shall include all wire sizes	10 (c = 1)	LTPD = 10 (c = 1)
Steady-state DC blocking life	1048	340 hours (as specified)	5	12 devices c = 0
Electrical measurements		As specified		
Bond strength (wire or clip bonded devices only)	2037	The sample shall include a minimum of 3 devices and shall include all wire sizes	10 c = 1	LTPD = 10, c = 1
SUBGROUP 4 (Notes 1, 5)				
Decap internal visual (design verification)	2075	Visual criteria in accordance with qualified design	1 device c = 0	1 device c = 0
SEM (when specified)	2077		6 devices c = 0	6 devices c = 0
SUBGROUP 5				
Thermal resistance:		Thermal resistance may be performed on group E frequency whenever 100 percent thermal response is performed. As specified	15	6 devices c = 0
Diodes Transistors (Bipolar) Transistors (POWERFETs) Thyristors IGBT GaAs	3101 3131 3161 3181 3103 3104			
SUBGROUP 6				
High-temp life (Nonoperating)	1032	340 hours min, T_{STG} (max) = T_A	7	12 devices c = 0
Electrical measurements		As specified		
SUBGROUP 7 (Note 6)				
Constant acceleration	2006	1 minute min in each orientation, X1, Y1 and Z1 at 20,000 G min, except at 10,000 G min for devices with power rating of ≤ 10 watts. T_C = 25°C	10	6 devices c = 0
Particle impact noise detection	2052	Condition A (see 4.3.4.2.1)		
Electrical measurements		As specified		

NOTES:

1. Electrical reject devices (and X-Ray for JANS) and PIND rejects from the same inspection lot may be used for all subgroups when electrical end-point measurements are not required. Post burn-in electrical rejects may be used.
2. Surge shall be performed on rectifiers and reverse surge for transient suppressors.
3. If a given inspection lot undergoing group B inspection has been selected to satisfy group C inspection requirements, the 340-hour or 2,000 cycle life tests may be continued on test to 1,000 hours or 6,000 cycles, as applicable, in order to satisfy the group C life test requirements and bond pull may be performed after group C life test. In such cases, either the 340-hour or 2,000 cycle, as applicable, end-point measurements.
4. Intermittent operation life shall be performed on all case mounted devices.
5. For axial lead diodes a lead pull to destruction shall be performed.
6. Not applicable to any devices with external and internal pressure contacts (die to electrical contacts), optical coupled isolators, double plug diodes. Subgroup 7 is applicable to JANTX and JANTXV only.

TABLE V. GROUP C PERIODIC INSPECTIONS (ALL QUALITY LEVELS)

INSPECTIONS	MIL-STD-750 METHOD	MIL-STD-750 CONDITION	SAMPLING PLAN	SMALL LOT QUALITY CONFORMANCE INSPECTION N/C
SUBGROUP 1				
Physical dimensions (Note 1)	2066	Dimensions per case outline specified	15	6 devices c = 0
SUBGROUP 2				
Thermal shock (glass strain)	1056	Test condition A, except test condition B for devices with power rating of > 5 watts at T_C = 25°C	10	6 devices c = 0
Terminal Strength	2036	As specified		
Hermetic seal a. Fine leak	1071	Not required for double plug diodes. Test condition G or H, max, leak rate = 5 x 10^{-8} atm cc/s, except 5 x 10^{-7} atm cc/s for devices with internal cavity > 0.3 cc		
b. Gross leak				
Moisture resistance	1021	Omit initial conditioning		
Electrical measurements		As specified		
SUBGROUP 3				
		Not required for disc packages. Nonoperating,1500 G's, 0.5ms		
Shock	2016	5 blows in each orientation: X1, Y1 and Z1. (Y1 only for axial glass diodes)	10	6 devices c = 0
Vibration, variable frequency	2056			
Constant acceleration (see 4.6) (not required when performed in group B)	2006	1 minute min in each orientation, X1, Y1 and Z1 at 20,000 G min, except at 10,000 G min for devices with power rating of ≥ 10 watts. T_C = 25°C		
Electrical measurements		As specified		
SUBGROUP 4				
Salt atmosphere (corrosion) (Note 1)	1041		15	6 devices c = 0
SUBGROUP 5				
Not applicable				
SUBGROUP 6 (Notes 2, 3)				
		Not required for disc packages. 1000 hours min at max operating junction temperature		
Steady-state-operation life or	1026	Condition D, 6000 cycles min	λ = 10	12 devices c = 0
Intermittent operation life or	1036			
Blocking life	1042			
Electrical measurements		As specified		

NOTES:

1. Electrical reject devices (and X-Ray for JANS) and PIND rejects from the same inspection lot may be used for all subgroups when electrical end-point measurements are not required. Not required for JANS.
2. If a given inspection lot undergoing group B inspection has been selected to satisfy group C inspection requirements, the 340-hour or 2,000 cycles life tests may be continued on test to 1,000 hours or 6,000 cycles, as applicable, in order to satisfy the group C life test requirements. In such cases, either the 340-hour or 2,000-cycle, as applicable, end-point measurements are optional and acceptance shall be determined by the 1,000-hour or 6,000-cycle, as applicable, end-point measurements.
3. Intermittent operation life shall be performed on all case mounted devices.

TABLE VI. GROUP D (RADIATION HARDNESS ASSURANCE TESTS) (NOTE 1)

TEST	MIL-STD-750 METHOD	MIL-STD-750 CONDITION	JANS QUALITY/ ACCEPT NUMBER	JANS NOTE	JANTXV QUANTITY /ACCEPT NUMBER	JANTXV NOTE
SUBGROUP 1 (Note 2)						
Neutron irradiation	1017	25°C				
a. Qualification			(a) 11(0)	3	(a) 11(0)	4
b. QCI			(b) 11(0)	3	(b) 11(0)	4
End-point electrical parameters		As specified in accordance with associated detail specification				
SUBGROUP 2 (Note 5)						
Steady-state total dose irradiation	1019	25°C Maximum supply voltage				
a. Qualification			(a) 4(0) 2(0)	(a) 6 8	(a) 22(0)	7
b. QCI			(b) 4(0) 2(0)	(b) 6 8	(b) 22(0)	7
End-point electrical parameters		As specified in accordance with associated detail specification				
SUBGROUP 3 (Note 9)						
Gamma dot Single event upset	3478	25°C 25°C	11 (0)	3	11 (0)	4
End-point electrical parameters		As specified in accordance with associated detail specification				

NOTES:

1. Parts used for one subgroup test may not be used for other subgroups but may be used for higher levels in the same subgroup. Total exposure shall not be considered cumulative unless testing is performed within the time limits of the test method. Group D tests may be performed prior to device screening (see 4.7.7).
2. Waive neutron tests for MOS devices except for charge coupled devices or where, by design, bipolar elements are an integral part of the device function.
3. In accordance with wafer lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).
4. In accordance with inspection lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).
5. JANTXV devices shall be inspected using either the JANTXV quantity/accept number criteria as specified, or by using the JANS criteria on each wafer.
6. In accordance with wafer for device types with less than or equal to 4,000 equivalent transistors/chip selected from the wafer at a radius approximately equal to two-thirds of the wafer radius, and spaced uniformly around this radius.
7. In accordance with inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 38(1).
8. In accordance with wafer for device types with greater than 4,000 equivalent transistors/chip selected from the wafer at a radius approximately equal to two-thirds of the wafer radius and spaced uniformly around this radius.
9. Upset testing during qualification on first QCI shall be conducted when specified in purchase order or contract. When specified, the same devices may be tested in more than one subgroup.

TABLE VII. GROUP E INSPECTIONS (ALL QUALITY LEVELS) FOR QUALIFICATION ONLY (NOTE 1)

INSPECTIONS	MIL-STD-750		SAMPLING PLAN
	METHOD	CONDITION	
SUBGROUP 1			
Thermal shock Electrical measurements	1051	500 cycles min or as specified	As specified
SUBGROUP 2			
Dynamic AC intermittent operating life Electrical measurements or steady-state DC intermittent operating life Electrical measurements or steady-state DC blocking life Electrical measurements		As specified	As specified
SUBGROUP 3			
Destructive physical analysis	2101 2102	As specified	3 devices c = 0
SUBGROUP 4			
Thermal resistance Transistors: POWERFETs Bipolar Diodes IGBT GaAs	 3161 3131 3101 3103 3104	As specified	15
SUBGROUP 5 (Note 2)			
Barometric pressure (reduced) (required only on devices with rated voltage > 200V)	1001	As specified	15

NOTES:

1. Group E is required prior to shipping whenever group E is added to the associated detail specification. Manufacturers currently qualified to an associated detail specification shall also perform group E when the associated detail specification is revised to include group E.
2. The barometric pressure test shall be performed on a subgroup of the highest voltage type device for each barometric pressure group to accept that type and all other types of the same or lower voltage rating at that barometric pressure. In the event that a subsequent lot contains a higher voltage type, that type shall be tested to subgroup 5 of group C prior to acceptance of the lot.

TABLE 3. SUMMARIZING CONTROL APPLICATIONS

FAB			
• Diffusion - Junction Depth - Sheet Resistivities - Oxide Thickness - Implant Dose Calibration - Uniformity	• Thin Film - Film Thickness - Uniformity - Refractive Index - Film Composition	• Photo Resist - Critical Dimension - Resist Thickness - Etch Rates	• Measurement Equipment - Critical Dimension - Film Thickness - 4 Point Probe - Ellipsometer
ASSEMBLY			
• Pre-Seal - Die Prep Visuals - Yields - Die Attach Heater Block - Die Shear - Wire Pull - Saw Blade Wear - Pre-Cap Visuals	• Post-Seal - Internal Package Moisture - Tin Plate Thickness - PIND Defect Rate - Solder Thickness - Leak Tests - Module Rm. Solder Pot Temp. - Seal - Temperature Cycle	• Measurement - XRF - Radiation Counter - Thermocouples - GN-Force Measurement	
TEST			
	- Handlers/Test System - Defect Pareto Charts - Lot % Defective - ESD Failures per Month	- Monitor Failures - Lead Strengthening Quality - After Burn-In PDA	
OTHER			
• IQC - Vendor Performance - Material Criteria - Quality Levels	• Enviornment - Water Quality - Clean Room Control	• IQC Measurement/Analysis - XRF - ADE - 4 Point Probe - Chemical Analysis Equipment	

Controlling and Improving the Manufacturing Process

SPC/DOX Statistical process control (SPC) is the basis for quality control and improvement at Harris Semiconductor. Harris manufacturing people use over 1,000 Shewhart control charts to determine the normal variabilities in processes, materials, and products. Critical process variables are measured and control limits are plotted on the control charts. Appropriate action is taken if the charts show that an operation is outside the process control limits or indicates a trend toward the limit. These same control charts are powerful tools for use in reducing variations in processing, materials, and products. Table 3 lists some typical manufacturing applications of control charts at Harris Semiconductor.

SPC is important, but still considered only part of the solution. Processes which operate in statistical control are not always capable of meeting engineering requirements. The conventional way of dealing with this in the semiconductor industry has been to implement 100% screening or inspection steps to remove defects, but these techniques are insufficient to meet today's demands for the highest reliability and perfect quality performance.

Harris still uses screening and inspection to "grade" products and to satisfy specific customer requirements for burn-in, multiple temperature test insertions, environmental screening, and visual inspection as value-added testing options. However, inspection and screening are limited in their ability to reduce product defects to the levels expected by today's buyers. In addition, screening and inspection have an associated expense, which raises product cost.

TABLE 4. HARRIS I.C. DESIGN TOOLS

DESIGN STEP	PRODUCTS	
	ANALOG	DIGITAL
Functional Simulation	Slice	Silos Proteous Socrates
Parametric Simulation	Slice Monte Carlo	Slice
Schematic Capture	Note 1	Daisy SDA-Mass Comp
Functional Checking	Note 1	SDA-LVS
Rules Checking	Calma-DRC	Harris Dash
Parasitic Extraction	Note 1	SDA-LVS

NOTE:1. Tools are in Development.

Harris engineers are, instead, using Design of Experiments (DOX), a scientifically disciplined mechanism for evaluating and implementing improvements in product processes, materials, equipment, and facilities. These improvements are aimed at reducing the number of defects by studying the key variables controlling the process, and optimizing the procedures or design to yieldthe best result. This approach is a more time-consuming method of achieving quality perfection, but a better product results from the efforts, and the basic causes of product nonconformance can be eliminated.

SPC, DOX, and design for manufacturability, coupled with our 100% test flows, combine in a product assurance program that delivers the quality and reliability performance demanded for today and for the future.

Average Outgoing Quality (AOQ)

Average Outgoing Quality is a yardstick for our success in quality manufacturing. The average outgoing electrical defective is determined by randomly sampling units from each lot and is measured in parts per million (PPM). The current procedures and sampling plans outlined in MIL-STD-883 and MIL-M-38510 are used by our quality inspectors. The focus on this quality parameter has resulted in a continuous improvement over the past three years. AOQ has decreased from 1,000 PPM to approximately 100 PPM, and the goal is to continue improvement toward 0 PPM.

Training

The basis of a successful transition from conventional quality programs to more effective, total involvement is training. Extensive training of personnel involved in product manufacturing began in 1984 at Harris, with a comprehensive development program in statistical methods. Using the resources of the University of Tennessee, private consultants, and internally developed programs, training of over 2,000 engineers, supervisors, and operators/technicians has been completed.

Nearly 1,000 operators, 100 supervisors, and more than 800 engineers have been trained in SPC methods, providing them with tools to improve the overall level of uniformity of Harris products. Almost 300 engineers have received training in DOX methods: learning to evaluate changes in process operations, set up new processes, select or accept new equipment, evaluate materials, select vendors, compare two or more pieces of equipment, and compare two or more process techniques.

Over the past four years, Harris has also deployed a comprehensive training program for hourly operators and supervisors in job requirements and functional skills. All hourly manufacturing employees participate (see Table 5).

TABLE 5. SUMMARY OF TRAINING PROGRAMS

COURSE	AUDIENCE	LENGTH	TOPICS COVERED
SPC	Manufacturing Operators	8 Hours	Basic Philosophy, Statistical Calculations Graphing Techniques, Pareto Charts, Control Charts
SPC	Manufacturing Supervisors	21 Hours	Basic Philosophy, Statistical Calculations Graphing Techniques, Pareto Charts, Control Charts, Testing for Inspector Agreement, Cause & Effect Diagrams, 1 & 2 Sample Methods
SPC	Engineers and Managers	48 Hours	Basic Philosophy, Graphical Methods, Control Charts, Rational Subgrouping, Variance Components, 1 & 2 Sample Methods, Pareto Charts, Cause & Effect Diagrams
DOX (Design of Experiments)	Engineers and Managers	88 Hours	Factorial Designs, Fractional Factorial Designs, Blocking Designs, Variance Components, Computer Usage, Normal Probability Plotting
RSM (Response Surface Methods)	Engineers and Managers	40 Hours	Steepest Ascent, Central Composite Designs, Box-Behnken Designs, Computer Usage, Contour Plotting, Second Order Response Surfaces
Continuous Improvement Methods	Manufacturing Supervisors	12 Hours	Basic Philosophy, Pareto Analysis, Imagineering, Run Charts, Cause & Effect Diagrams, Histograms, Ideas of Control Charts
SPC-The Essentials	Department-Level Work Groups	20 Hours	Basic Philosophy, of Continous Improvement, Imagineering Pareto Charts, Cause & Effect Diagrams, Flow Charts, Graphical Display, Control Charts, Ideas of Experiment

Incoming Materials

Improving the quality and reducing the variability of critical incoming materials is essential to product quality enhancement, yield improvement, and cost control. With the use of statistical techniques, the influence of silicon, chemicals, gases and other materials on manufacturing is highly measurable. Current measurements indicate that results are best achieved when materials feeding a statistically controlled manufacturing line have also been produced by statistically controlled vendor processes.

To assure optimum quality of all incoming materials, Harris has initiated an aggressive program, linking key suppliers with our manufacturing lines. This user-supplier network is the Harris Vendor Certification process by which strategic vendors, who have performance histories of the highest quality, participate with Harris in a lined network; the vendor's factory acts as if it were a beginning of the Harris production line.

SPC seminars, development of open working relationships, understanding of Harris' manufacturing needs and vendor capabilities, and continual improvement programs are all part of the certification process. The sole use of engineering limits no longer is the only quantitative requirement of incoming materials. Specified requirements include centered means, statistical control limits, and the requirement that vendors deliver their products from their own statistically evaluated, in-control manufacturing processes.

In addition to the certification process, Harris has worked to promote improved quality in the performance of all our qualified vendors who must meet rigorous incoming inspection criteria (see Table 6).

TABLE 6. INCOMING QUALITY CONTROL MATERIAL QUALITY CONFORMANCE

MATERIAL	INCOMING INSPECTIONS	VENDOR DATA REQUIREMENTS
Silicon	• Resistivity • Crystal Orientation • Dimensions • Edge Conditions • Taper • Thickness • Total Thickness Variation • Backside Criteria • Oxygen • Carbon	• Equipment Capability Control Charts - Oxygen - Resistivity • Control Charts Related to - Enhanced Gettering - Total Thickness Variation - Total Indicated Reading - Particulates • Certificated of Analysis for all Critical Parameters • Control Charts from On-Line Processing
Chemicls/Photoresists/Gases	• Chemicals - Assay - Major Contaminants • Molding Compounds - Spiral Flow - Thermal Characteristics • Gases - Impurities • Photoresists - Viscosity - Film Thickness - Solids - Pinholes	• Certicate of Analysis on all Critical Parameters • Control Charts from On-Line Processing • Control Charts - Assay - Contaminants - Water - Selected Parameters • Control Charts - Assay - Contaminants • Control Charts on - Photospeed - Thickness - UV Absorbance - Filterability - Water - Contaminants
Thin Film Materials	• Assay • Selected Contaminants	• Control Charts from On-Line Processing • Control Charts - Assay - Contaminants - Dimensional Characteristics • Certificate of Analysis for all Critical Parameters
Assembly Materials	• Visual Inspection • Physical Dimension Checks • Lead Integrity • Glass Composition • Bondability • Intermetallic Layer Adhesion • Ionic Contaminants • Thermal Characteristics • Lead Coplanarity • Plating Thickness • Hermeticity	• Certificate of Analysis • Process Control Charts on Outgoing Product Checks and In-Line Process Controls

Manufacturing Science CAM

In addition to SPC and DOX as key tools to control the product and processes, Harris is deploying other management mechanisms in the factory. On first examination, these tools appear to be directed more at schedules and capacity. However, they have a significant impact on quality results.

Computer Aided Manufacturing (CAM)

CAM is a computer based inventory and productivity management tool which allows personnel to quickly identify production line problems and take corrective action. In addition, CAM improves scheduling and allows Harris to more quickly respond to changing customer requirements and aids in managing work in process (WIP) and inventories.

The use of CAM has resulted in significant improvements in many areas. Better wafer lot tracking has facilitated a number of process improvements by correlating yields to process variables. In several places CAM has greatly improved capacity utilization through better planning and scheduling. Queues have been reduced and cycle times have been shortened - in some cases by as much as a factor of 2.

The most dramatic benefit has been the reduction of WIP inventory levels, in one area by 500%. This results in fewer lots in the area and a resulting quality improvement. In wafer fab, defect rates are lower because wafers spend less time in production areas awaiting processing. Lower inventory also improves morale and brings a more orderly flow to the area. CAM facilitates all of these advantages.

Measurement

Analytical Services Laboratory

The Harris Analytical Laboratory is a company-wide technical resource for the physical and chemical characterization of microelectronic materials and products. Harris Facilities, Engineering, Manufacturing, and Quality are supported by the laboratory. Organized as chemical or microbeam analysis methodology, staff and instrumentation from both areas cooperate in fully integrated approaches necessary to complete any analytical study. The lab is widely staffed and equipped to provide all manufacturing and operational functions with the following:

- Real time materials and process analyses to support routine manufacturing and development.
- Cooperative planning of all analytical investigations.
- Development of new techniques and method refinements as necessary to support internal and external customer requirements.
- Maintenance of awareness and accessibility to outside plant capabilities at commercial and university laboratories.
- Materials analyses with ultimate concern for product yield, quality and reliability.

The Microbeam Laboratory equipment is engaged principally in high resolution imaging and localized chemical analysis of microcircuits. The equipment includes:

- Electron Beam Analysis - Scanning Auger Microprobe, Scanning Electron Microscopes, and Transmission Electron Microscope.
- Ion Beam Analysis - Ion Microprobe, Secondary Ion Mass Spectrometer, and Ion Scattering Spectrometer.
- X-Ray Analysis - Energy Dispersive X-Ray (SEM), Wavelength Dispersive X-Ray (SEM), X-Ray Photoelectron Spectrometer, X-Ray Diffraction, and X-Ray Fluorescence.

The Chemistry Laboratory equipment affords a wide variety of analyses, capable for solid, liquid, and gaseous materials.

- Spectroscopy - Emission Spectrograph, Fourier Transform Infrared Spectrophotometer, Ultraviolet-Visible Spectrophotometer, Organic Carbon Analyzer, Mass Spectrometer, Atomic Absorption Spectrophotometer (flame and graphite furnace) and an Inductively Coupled Plasma Emission Spectrophotometer.
- Thermal Analysis - Differential Scanning Colorimeter, Thermogravimetric Analyzer Thermomechanical Analyzer.
- Separation Methods - Gas Chromatograph, Ion Chromatograph, Gas Chromatograph Mass Spectrometer, and Water, Oxygen, and Total Hydrocarbon Analyzers.
- Physical Testing - Profilometer, Microhardness Measurement, and Viscometers.
- Wet Chemistry - Titrimetry, Gravimetry, specific Ion Electrodes, Colorimeters, Bacteria Testing, and other qualitative chemical testing.

Capability for all process/product Mil-Spec test method methodology is maintained by the laboratory.

The department also maintains ongoing working arrangements with commercial, university, and equipment manufacturers' technical service laboratories and can obtain any material analysis in cases where instrumental capabilities are not available in our own facility.

Calibration Laboratory

Another important resource in the product assurance system is Harris Semiconductor's Calibration Lab. This area is responsible for calibrating the electronic, electrical, electro/mechanical, and optical equipment used in both the production and engineering areas. The accuracy of instruments used at Harris in calibration is traceable to the National Bureau of Standards. The lab maintains a system which conforms to the current revision of MIL-STD-45662, "Calibration System Requirements."

Each instrument requiring calibration is given a calibration interval based upon stability, purpose, and degree of use. The equipment is labeled with an identification tag on which is specified both the date of the last calibration and of the next required calibration. The Calibration Lab reports on a regular basis to each user department. Equipment out of calibration is taken out of service until calibration is performed. The Quality organization performs periodic audits to assure proper control in the using areas. Statistical procedures are used where applicable in the calibration process.

Failure Analysis Laboratory

The Failure Analysis Laboratory's capabilities encompass the isolation and identification of all failure modes/failure mechanisms, preparing comprehensive technical reports, and assigning appropriate corrective actions. Research vital to understanding the basic physics of the failure is also undertaken.

Failure analysis is a method of enhancing product reliability and determining corrective action. It is the final and crucial step used to isolate potential reliability problems that may have occurred during reliability stressing. Accurate analysis results are imperative to assess effective corrective actions. To ensure the integrity of the analysis, correlation of the failure mechanism to the initial electrical failure is essential.

A general failure analysis procedure has been established in accordance with the current revision of MIL-STD-883, Section 5003. The analysis procedure was designed on the premise that each step should provide information on the failure without destroying information to be obtained from subsequent steps. The exact steps for an analysis are determined as the situation dictates. See Figures 4 and 5 that represent the Failure Analysis Flow. Records are maintained by laboratory personnel and contain data, the failure analyst's notes, and the formal Product Analysis Report.

Reliability

Reliability Assessment and Enhancement

At Harris Semiconductor, reliability is built into every product by emphasizing quality throughout manufacturing. This starts by ensuring the excellence of the design, layout, and manufacturing process. The quality of the raw materials and workmanship is monitored using statistical process control (SPC) to preserve the reliability of the product. The primary and ultimate goal of these efforts is to provide full performance to the product specification throughout its useful life. Product reliability is maintained through the following sources.

Qualifications

Qualifications at Harris de-emphasize the sole dependence on production product which is only available late in the development cycle. The focus is primarily on the use of test vehicles to establish design ground rules for the product and the process that will eliminate any wearout mechanisms during the useful life of the product. However, to comply with the military requirements concerning reliability, product qualifications are performed.

In-line Reliability Monitors

In-line reliability monitors provide immediate feedback to manufacturing regarding the quality of workmanship, quality of raw materials, and the ultimate reliability implications. The rudimentary implementation of this monitoring is the "First Line of Defense," which is a pass/fail acceptance procedure based on control charts and trend analysis. The second level of monitoring is referred to as the "Early Warning System" and incorporates extensive diagnostic and characterization capabilities of various components that may impact the device reliability or stability. The quick feedback from these schemes allows more accurate correlation to process steps and corrective actions.

Reliability Fundamentals

Reliability, by its nature, is a mixture of engineering and probability statistics. This combination has derived a vocabulary of terms essential for describing the reliability of a device or system. Since reliability involves a measurement of time, it is necessary to accelerate the failures which may occur. This, then, introduces terms like "activation energy" and "acceleration factor," which are needed to relate results

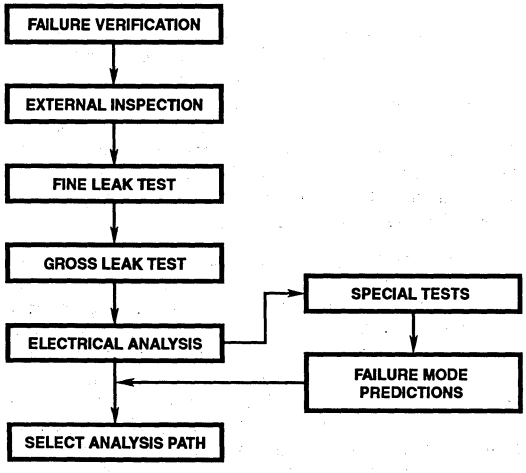


FIGURE 2. NON-DESTRUCTIVE

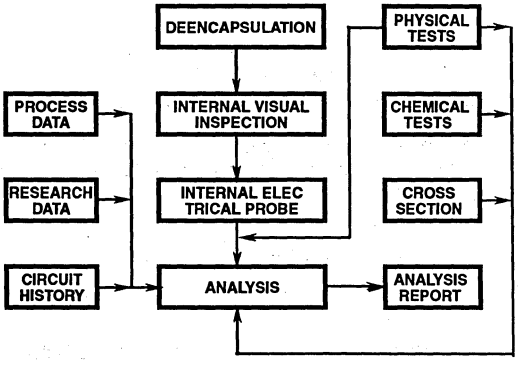


FIGURE 3. DESTRUCTIVE

of stressing to normal operating conditions (see Table 7). Also, to assess product reliability requires failures. Therefore, only a statistical sample can be used to determine the model of the failure distribution for the entire population of product.

Failure Rate Primer

Failure Rate Calculations

Reliability data for products may be composed of several different failure mechanisms and requires careful combining of diverse failure rates into one comprehensive failure rate. Calculating the failure rate is further complicated because failure mechanisms are thermally accelerated at varying rates and thereby have differing accelerating factors. Additionally, this data is usually obtained from a variety of life tests at unique stress temperatures. The equation (right) accounts for these considerations and then inserts a statistical factor to obtain the confidence interval for the failure rate.

In the failure rate calculation, Acceleration Factors (AFij) are used to derate the failure rate from thermally accelerated Life Test conditions to a failure rate indicative of use temperatures. Though no standards exist, a temperature of +55°C has been popular and allows some comparison of product failure rates. All Harris Semiconductor Reliability Reports will derate to +55°C at both the 60% and 95% confidence intervals.

$$FIT = \left(\sum_{i=1}^{B} \frac{X_i}{K \sum_{j=1} TDH_j \; AF_{ij}} \right) \times 10^9 \times M$$

B = # of distinct possible failure mechanisms

K = # of life tests being combined

Xi = # of failures for a given failure mechanism
i = 1, 2, . . . B

TDGj = Total device hours of test time (unaccelerated) for Life Testj

AFij = Acceleration factor for appropriate failure mechanism
i = 1, 2, . . . K

M = Statistical factor for calculating the upper confidence limit (M is a function of the total number of failures and an estimate of the standard deviation of the failure rates)

TABLE 1. FAILURE RATE PRIMER

GLOSSARY OF TERMS

TERMS/DEFINITIONS	UNITS/DESCRIPTION
FAILURE RATE λ For Semiconductors, usually expressed in FITs. Represents useful life failure rate (which implies a constant failure rate). FITs are not applicable for infant mortality or wearout failure rate expressions.	**FIT - Failure In Time** 1 FIT - 1 failure in 10^9 device hours. Equivalent to 0.0001%/1000 hours FITs = $\frac{\#\ \text{Failures}}{\#\ \text{Devices x \# hours stress x AF}} \times 10^9 \times m$ m - Factor to establish Confidence Interval 10^9 - Establishes in terms of FITs AF - Acceleration Factor at temperature for a given failure mechanism
MTTF - Mean Time To Failure For semiconductors, MTTF is the average or mean life expectancy of a device. If an exponential distribution is assumed then the mean time to fail of the population will be when 63% of the parts have failed.	Mean Time is measured usually in hours or years. 1 Year = 8760 hours When working with a constant failure rate the MTTF can be calculated by taking the reciprocal of the failure rate. MTTF = $1/\lambda$ (exponential model) Example: =10 FITs at +55°C The MTTF is: MTTF = $1/\lambda = 0.1 \times 10^9$ hours = 100M hours
CONFIDENCE INTERVAL (C. I.) Establishes a Confidence Interval for failure rate predictions. Usually the upper limit is most significant in expressing failure rates.	Example: "10 FITs @ a 95% C. I. @ 55°C" means *only* that you are 95% certain the the FITs <10 at +55°C use conditions.

Acceleration Factors

The Acceleration Factors (AF) are determined from the Arrhenius Equation. This equation is used to describe physiochemical reaction rates and is an appropriate model for expressing the thermal acceleration of semiconductor failure mechanisms.

$$AF = EXP \left[\frac{E_a}{K} \left(\frac{1}{T_{use}} - \frac{1}{T_{stress}} \right) \right]$$

AF = Acceleration Factor

E_a = Thermal Activation Energy in eV from Table 8

K = Boltzmann's Constant (8.62×10^{-5} eV/°K)

Both Tuse and Tstress (in degrees Kelvin) include the internal temperature rise of the device and therefore represent the junction temperature. With the use of the Arrhenius Equation, the thermal Activation Energy (E_a) term is a major influence on the result. This term is usually empirically derived and can vary widely.

Activation Energy

To determine the Activation Energy (E_a) of a mechanism (see Table 8) you must run at least two (preferably more) tests at different stresses (temperature and/or voltage). The stresses will provide the time to failure (Tf) for the populations which will allow the simultaneous solution for the Activation Energy by putting the experimental results into the following equations.

$$\ln (t_{f1}) = C + \frac{E_a}{KT_1} \qquad \ln (tf_2) = C + \frac{E_a}{KT_2}$$

Then, by subtracting the two equations, the Activation Energy becomes the only variable, as shown below.

$\ln(t_{f1}) - \ln(t_{f2}) = E_a/k(1/T1-1/T2)$

$E_a = K^* ((\ln(t_{f1}) - \ln(t_{f2}))/(1/T1 - 1/T2))$

The Activation Energy may be estimated by graphical analysis plots. Plotting ln time and ln temperature then provides a convenient nomogram that solves (estimates) the Activation Energy.

Table 9 is a summary of military generic groups by process descriptions.

All Harris Reliability Reports from qualifications and Group C1 (all high temperature operating life tests) will provide the data on all factors necessary to calculate and verify the reported failure rate (in FITs) using the methods outlined in this primer.

TABLE 2. FAILURE MECHANISM

FAILURE MECHANISM	ACTIVATION ENERGY	SCREENING AND TESTING METHODOLOGY	CONTROL METHODOLOGY
Oxide Defects	0.3 - 0.5eV	High temperature operating life (HTOL) and voltage stress. Defect density test vehicles.	Statistical Process Control of oxide parameters, defect density control, and voltage stress testing.
Silicon Defects (Bulk)	0.3 - 0.5eV	HTOL & voltage stress screens.	Vendor statistical Quality Control programs, and Statistical Process Control on thermal processes.
Corrosion	0.45eV	Highly accelerated stress testing (HAST)	Passivation dopant control, hermetic seal control, improved mold compounds, and product handling.
Assembly Defects	0.5 - 0.7eV	Temperature cycling, temperature and mechanical shock, and environmental stressing.	Vendor Statistical Quality Control programs, Statistical Process Control of assembly processes proper handling methods.
Electromigration - Al Line - Contact	 0.6eV 0.9eV	Test vehicle characterizations at highly elevated temperatures.	Design ground rules, wafer process statistical process steps, photoresist, metals and passivation
Mask Defects/ Photoresist Defects	0.7eV	Mask FAB comparator, print checks, defect density monitor in FAB, voltage stress test and HTOL.	Clean room control, clean mask, pellicles Statistical Process Control or photoresist/etch processes.
Contamination	1.0eV	C-V stress at oxide/interconnect, wafer FAB device stress test (EWS) and HTOL.	Statistical Process Control C-V data, oxide/interconnect cleans, high integrity glassivation and clean assembly processes.
Charge Injection	1.3eV	HTOL & oxide characterization.	Design ground rules, wafer level Statistical Process Control and critical dimensions for oxides.

Qualification Procedures

New products are reliably introduced to market by the proper use of design techniques and strict adherence to process layout ground rules. Each design is reviewed from its conception through early production to ensure compliance to minimum failure rate standards. Ongoing monitoring of reliability performance is accomplished through compliance to MIL-STD-883 and standard Quality Conformance Inspection as defined in Method 5005. New process/product qualifications have two major requirements imposed. First is a check to verify the proper use of process methodology, design techniques, and layout ground rules. Second is a series of stress tests designed to accelerate failure mechanisms and demonstrate the reliability of integrated circuits. From the earliest stages of a new product's life, the design phase, through layout, and in every step of the manufacturing process, reliability is an integral part of every Harris Semiconductor product. This kind of attention to detail "from the ground up" is the reason why our customers can expect the highest quality for any application.

TABLE 9. HIGH TEMPERATURE OPERATING LIFE TEST SUMMARY

GROUP NAME	PROCESS DESCRIPTION	QUANTITY	QUANTITY FAILS	HOURS AT +125°C	+55°C FITS	95% UCL MTTF	LIFETEST DATES
CD4000	Metal Gate epi CMOS	20,288	19	2.62×10^7	3	4.0×10^8	1-'91 to 3-'92
HCS/HCTS	SOSLT	3352	0	2.77×10^6	3	3.4×10^8	2-'91 to 3-'92
ACS/ACTS	TSOS4	540	0	5.13×10^5	14	7.3×10^7	10-'91 to 3-'92
64K SRAMs	TSOS4	134	0	1.34×10^5	44	2.3×10^6	3-'92
16K SRAMs	SAJI5RH	447	0	4.15×10^5	17	6.0×10^7	5-'90 to 3-'92
16K PROM	SAJI4RH						
MUX, Switches	DI CMOS	899	3	9.14×10^5	173	5.8×10^6	1-'86 to 3-'92
Op Amps	DI Bipolar	170	1	2.0×10^5	504	2.0×10^6	1-'89 to 3-'92
80C86RH Family	SAJI4RH	762	1	7.85×10^5	87	1.2×10^7	1-'90 to 3-'92
80C85RH Family	Sandia 4/3	340	0	4.71×10^5	15	6.7×10^7	8-'87 to 3-'92

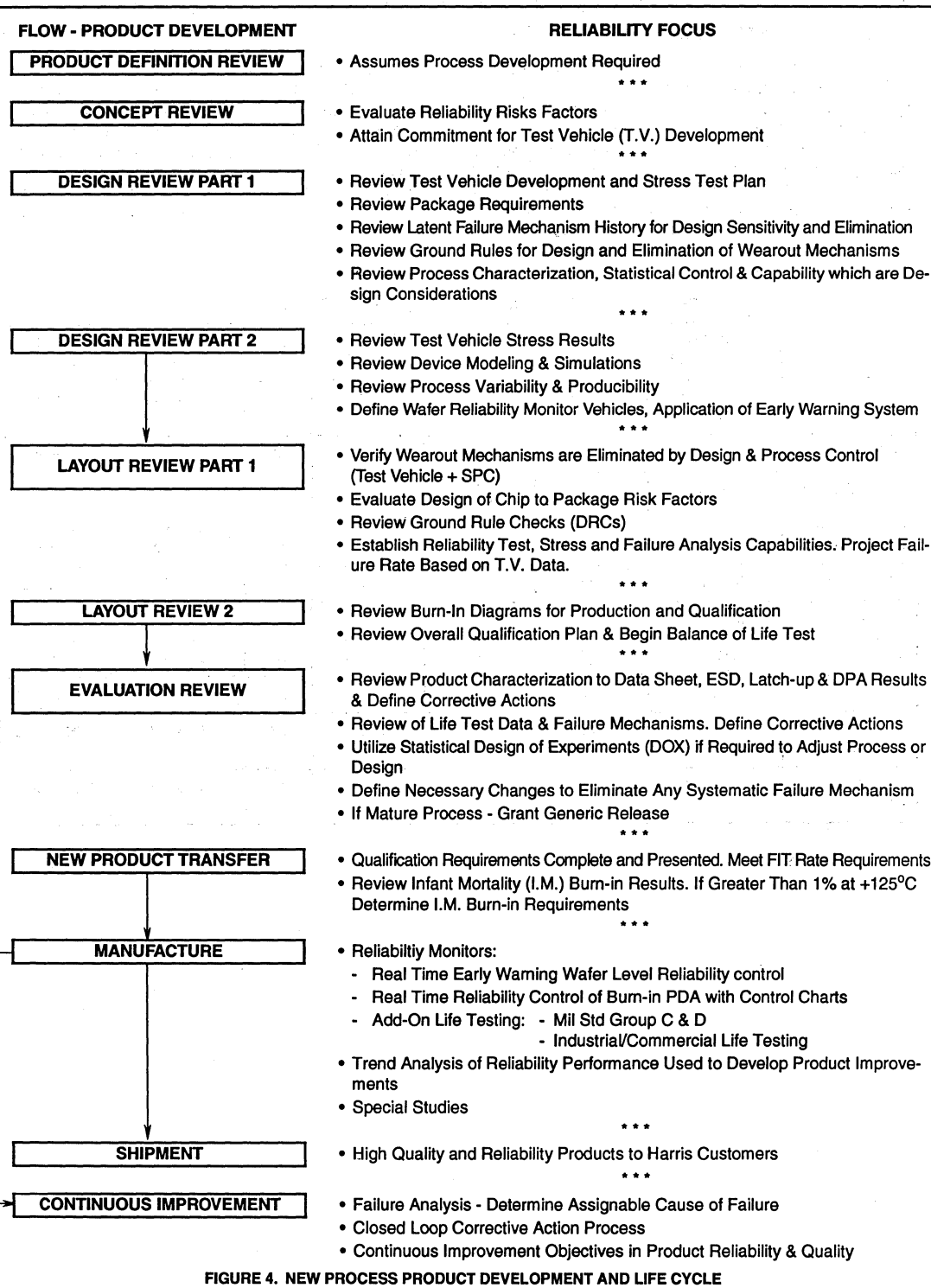


FIGURE 4. NEW PROCESS PRODUCT DEVELOPMENT AND LIFE CYCLE

JAN/SMD Certification

Harris Semiconductor has been an active participant in the JAN program since 1972 when it became the first manufacturer to JAN qualify a PROM. In the years since then, Harris has continued to offer an expanding line of JAN qualified devices including MIL-M- 38510 JAN Class S line certification for the manufacture of radiation-hardened products. The complete listing of JAN Class S and Class B devices can be found in Section 16.

Harris is also an active participant in the Standard Military Drawing (SMD) Program. The SMD provides standardized Mil-Std-883 processing in conjunction with compliant, non-JAN devices as specified in paragraph 1.2.1 of Mil-Std-883. Manufacturer's qualified to supply a particular SMD device are listed in the back of the individual DESC drawing.

Radiation Hardening

Military, space and industrial electronic systems are receiving increasing demands for higher immunity from the damage that radiation can inflict upon them. The optimization of radiation hardness is a systems problem which flows through to each subsystem and component integrated circuit. Harris Semiconductor is the leader in providing radiation hardened microcircuits for systems designed to be exposed to space or nuclear events.

An integrated circuit can be classified as radiation hardened, radiation tolerant, or radiation resistant. Radiation hardened devices are guaranteed to meet full parametric levels specified in the data sheets up to the radiation level specified. Functional failure of a radiation hard device can be 10-100 times greater than the parametric levels listed in the respective data sheet. Devices classified as radiation tolerant or radiation resistant typically meet functional failure levels that are not guaranteed. Hardening is achieved through:

- Design
- Special fabrication processes
- Continuous screening and quality control

Radiation affects circuits primarily through two basic mechanisms: displacement damage and ionization. Displacement damage occurs when high energy neutrons penetrate the semiconductor crystal lattice and physically dislocate atoms within the structure. It permanently affects lifetime, carrier mobility, leakage current, and bipolar device gain. Ionizing radiation effects can cause interface charge accumulation, which modifies MOS device thresholds and induces parasitic leakage paths. Both effects adversely affect IC performance. After a device technology has been selected, the circuit is designed to take maximum advantage of the hardening options available for that technology.

BIPOLAR:

- Stabilizing expected gain
- Maximum emitter current density
- Guard-banding for increased resistor values

MOS:

- Allowances for changes in threshold voltages and leakage currents
- Dielectric isolation
- P+ guard-bands of N-channel transistors

Processing also lends hardness to these circuits. By minimizing gate oxide thickness, employing "hardened oxides," and utilizing proprietary hardening processes, Harris Semiconductor delivers circuits with higher packing densities and lower redesign costs.

Reliability is an issue that has distinguished Harris Semiconductor as a leader in the design and manufacture of radiation hardened memories, microprocessors, op amps, and full custom devices. Strict lot qualification, screening and testing procedures are maintained, along with stringent radiation screening procedures. All wafers in a run are processed together through all high temperature steps and metallization, and a sample of probed good dice is selected. These dice are assembled and tested for functionality, then subjected to the total dose radiation level guaranteed for each device, using Harris's own Gammacell 220 Cobalt 60 source with conditions specified by Mil-Std-883, method 1019 or customer requirements. The samples are then tested and accepted by previously defined criteria.

Harris Mil-Std-883 Compliant Screening Flows

SCREEN	METHOD PER MIL-STD-883	REQUIREMENT	
		CLASS S	CLASS B
Wafer Lot Acceptance	5007		No
SEM (Traceable to Diffusion)	2018	Yes	No
Wire Bond Pull Monitor	2011, condition D, LTPD = 10 on number of leads pulled, 2 units minimum		No
Die Shear Monitor	2019, 2(0)		No
Gamma Radiation Assurance Tests	1019	As required	No
Nondestructive Bond Pull	2023	Yes/No	No
Internal Visual Inspection	2010	Condition A	Condition B
Customer Source Inspection	Per detail part drawing	As required	No
Temperature Cycling	1010 condition C, 10 cycles	Yes	Yes
Constant Acceleration	2001, Y1 orientation, 30Kg	Yes	Yes
Particle Impact Noise Detection	2020, condition A, 20g Yes	No	
Visual Inspection	None, Missing leads, broken packages, lids off	Yes	No
Initial Electrical Test	At Harris' discretion	Yes	Yes
Marking	Per detail part drawing	Yes	No
Serialization	None. No duplication of numbers in a single datecode	Yes	No
Radiographic Inspection	2010, 2 copies, 2 views	Yes	No
+25°C Electrical Test	Per detail part drawing with datalog of selected parameters	Yes	No
Burn-In, Static	1015, condition A or B, 72 hours minimum at 125°C	Yes	No
Burn-In	1015, condition A, B or D, 160 hours at 125°C or equivalent	No	Yes
+25°C Electrical Test	Per detail part drawing with datalog of selected parameters Go/ no-go per detail part drawing	Yes No	No Yes
Delta Calculation	Per detail part drawing	Yes	No
Burn-In, Dynamic	1015, condition D, 240 hours minimum at 125°C	Yes	No
Percent Defective Allowable	5% on +25°C DC and W fails combined. 3% on +25°C functional failures. 5004, para 3.5.1, 5% on subgroup 1 (+25°C DC) failures	Yes No	No Yes
-55°C or +125°C Electrical Test	Per detail part drawing with datalog of selected parameters Go/ no-go per detail part drawing	Yes No	No Yes
Fine Leak Test	1014, condition A or B	Yes	Yes
Gross Leak Test	1014, condition C	Yes	Yes
Marking	Per detail part drawing	No	Yes
-55°C or +125°C Electrical Test	Go/no-go per detail part drawing	No	Yes
External Visual Inspection	2009	Yes	Yes
Group A Inspection	5005, Table 1, 116/0, each lot. Para 3.5.1 of 5005 exercized	Yes	Yes
Customer Source Inspection	Per detail part drawing	As required	No
Group B Inspection	5005, Table 2A, 5005, Table 2B	Yes No	No Yes
Group C Inspection	5005, Table 3, every four quarter or as required	No	Yes
Group D Inspection	5005, Table 4, every 52 weeks or as required	Yes	Yes
External Visual Examination	2009 on shippable QCI units	Yes	Yes

For details explaination please refer to latest version of Mil-Std-833.

TABLE II. SCREENING REQUIREMENTS

SCREEN	MIL-STD-750 METHOD	CONDITION	JANS REQUIREMENTS	JANTXV REQUIREMENTS	JANTX REQUIREMENTS
1. Internal visual (pre-cap) inspection (Note 1)					
POWERFETs	2069 2070		100%	100%	-
Microwave transistors	2072 2073				
Transistors	2074				
Diodes			-	When specified	-
2. High temperature life Non-operating life (stabilization bake)	1032	TSTG max	Optional	Optional	Optional
3. Temperature cycling	1051	No dwell is required at 25°C. Test condition C, except step 3 at 175°C, +5°C, -0°C, 20 cycles, t(extremes) > 10 min	100%	100%	100%
Surge (as specified) (Note 2)	4066	Condition B, as specified	100%	100%	100%
Thermal response (as specified)		As specified	100%	100%	100%
Transistors, POWERFETs	3161 3131		-	-	-
Bipolar	3101		-	-	-
Diodes	3103 3104		-	-	-
IGBT			-	-	-
GaAs			-	-	-
4. Constant acceleration (see 4.6)	2006	Y1 direction at 20,000 G min except at 10,000 G min for devices with power rating of ≥ 10 watts at T_C = +25°C. The 1 minute hold time requirement shall not apply	100% except not required for metallurgically bond diodes	Optional (Note 3)	Optional (Note 3)
5. Particle impact noise detection (Note 4)	2052	Condition A	100% See 4.6.4.2		
6. Instability shock test (axial lead diodes only) (Note 5)		100% 100%			
a. Forward instability shock test (FIST)	2081				
b. Backward instability vibration test (BIST)	2082				
7. Hermetic seal	1071	Test condition G or H, max leak rate = 5 x 10^{-8} atm cc/s except 5 x 10^{-7} atm cc/s for devices with internal cavity > 0.3 cc. Omit for double plug diodes	Optional	100% (Note 6)	100% (Note 6)
a. Fine					
b. Gross			-	100% (Note 6)	100% (Note 6)
8. Serialization		See 3.7.9	100%	-	-
9. Interim electrical parameters		As specified	100% (Read and record)	For case mounted rectifiers as specified	For case mounted rectifiers as rectified

See Notes at End of Table

TABLE II. SCREENING REQUIREMENTS (Continued)

SCREEN	MIL-STD-750 METHOD	CONDITION	JANS REQUIREMENTS	JANTXV REQUIREMENTS	JANTX REQUIREMENTS
10. High temperature reverse bias (HTRB) a. Transistors b. POWERFETs c. For diodes and recitifers	1039	48 hours min at T_A, (T_C, or T_L is optional) = 150°C (min) and munimum applied voltage as follows: a. Transistors - 80% to 85% (min) of rated V_{CB} (bipolar, V_{GS}(FET), or V_{DS}(FET) as applicable. Test condition B b. POWERFETs - 80% to 85% of rated V_{GS}. Test condition B c. Diodes (except LEDs and zeners) 80% to 85% of rated V_R, or 95%-100% of V_{RWM} when half sine condition is specified. Test condition A			
11. Interim electrical and delta parameters for PDA (see 4.6.1) For stud rectifiers as a minimum		As specified but including all delta parameters as a minimum. Leakage current shall be seasured on each device before any other test is made	100% (measure all specified parameters within 16 hrs after removal of applied voltage in HTRB. Record those parameters which have a delta limit). (See screen 13	100% (measure all specified parameters within 24 hrs after removal of applied voltage in HTRB. Record those parameters which have a delta limit). (See screen 13	100% (measure all specified parameters within 24 hrs after removal of applied voltage in HTRB. Record those parameters which have a delta limit). (See screen 13
12. Power burn-in a. Bipolar transistors b. POWERFETs c. Diodes, zeners and rectifiers d. Thyristors (Note 8)	 1039 1042 1038 1040	As specified a. Transistors. Test condition B b. POWERFETs (see 4.6.7) Codition C shall precede condition A 1. Test condition C 2. Test condition A c. Diodes, zeners (except case mounted rectifier packages for JANTX and JANTXV) Test condition B d. Thyristors	100% 240 hrs (min) 240 hrs (min) 160 hrs (min) 240 hrs (min) 240 hrs (min)	100% 160 hrs (min) 160 hrs (min) 96 hrs (min) 96 hrs (min)	100% 160 hrs (min) 160 hrs (min) 96 hrs (min) 96 hrs (min)
13. Final electrical test (See 4.6 and 4.6.5) a. Interim electrical & delta parameters for PDA see (4.6.1) b. Other electrical parameters		As specified All interim and delta parameter measurements must be completed within 96 hrs after removal from burn-in conditions	100% Interim electrical and delta parameters as a min. (Read & record) Group A, Subgroup 2 & 3	100% Interim electrical and delta parameters as a min. (Read & record) (See 4.6.3.2.) Group A, Subgroup 2	100% Interim electrical and delta parameters as a min. (Read & record) (See 4.6.3.2.) Group A, Subgroup 2
14. Hermetic seal a.Fine b.Gross	1071	(Same as 7 above) (Note 9)	100%	Optional (Note 6)	Optional (Note 6)
15. Radiography	2076	(Note 9)	100%	-	-
16. External visual examination	2071	To be performed after complete marking	100%	-	-

See Notes Next Page

NOTES:

1. Visual inspection (method 2074) on clear glass diodes shall be performed any time prior to screen 8.
2. Shall be performed any time before screen 13. Surge shall precede thermal response when both tests are performed.
3. Constant acceleration shall be performed on gold bond devices.
4. PIND is not applicable to any device with external and internal pressure contacts (die to electrical contacts) optical coupled isolators, and double plug diodes. PIND screening may be performed any time after screen 4 when imposed by contract or purchase order (see 3.7.6.1).
5. Omit BIST and FIST tests for double plug or case-mounted diodes. Omit FIST test for temperature compensated referenced diodes.
6. Fine and gross seal leak test for JANTX and JANTXV shall be performed in either screen 7 or screen 14.
7. For JANS only, zener diodes shall be subjected to high temperature reverse bias at 80% to 85% of nominal VZ for VZ ≥ 10VZ. Omit test for devices with VZ ≤ 10VZ.
8. For JANTX and JANTXV levels full wave-blocking test shall replace power burn-in for all thyristors.
9. The radiographic and seal screens for JANS may be performed in any order following final electrical test. Glass diodes shall not be painted until after seal tests. When hermetic seal testing is performed in screen 7 it does not have to be performed again in screen 14 for double plug diode construction.

Assembly Location Identification Codes

The following codes will identify assembly locations for devices branded with Harris Logo or equivalent Manufacturers Code.

A - Toshiba, Japan
B - Harris, Milpitas, California
C - Harris, Mountaintop, Pennsylvania
D - Pantronix, San Jose, California
E - Swire Technologies, Hong Kong
F - Harris, Findlay, Ohio
G - CARSEM, Malaysia
H - Harris, Kuala Lumpur, Malaysia
I - Harris, Camberley, United Kingdom
J - Harris, Singapore
K - Harris, Bombay, India
L - AMKOR/ANAM, Philippines
M - INDY Electronics Inc., Manteca, California
N - AMKOR/ANAM, South Korea
R - Rohm Corporation, Japan
T - Harris, Dundalk, Ireland
U - Harris, RTP, North Carolina
V - Seiko, Japan (IC)
W - Chinteik, Thailand
X - Harris, Melbourne, Florida
Y - Harris, Santa Clara, California
Z - Harris, Taoyuan, Taiwan

The following codes have been retired from the previous table.

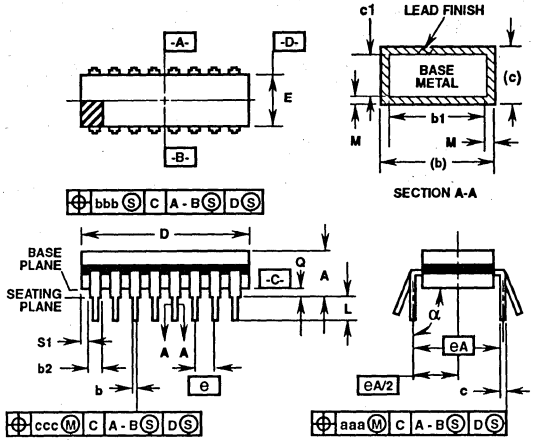
	RETIRED
A - Philip, Taiwan	3-16-90
B - ASE, Taiwan	3-16-90
C - Intersil, Chinteik, Thailand	12-1-89 (to "W")
D - DYNETICS, Manila, Philippines	1-5-88
E - SHARP, Japan	1-5-88
K - Comtronics, Philippines	1-5-88
L - GE Ceramics, Chattanooga, Tennessee	11-3-89
S - Harris, Singapore	10-15-90
V - Toshiba, (Buy/Resell Power)	1-5-88
W - West Palm Beach, Florida	1-5-88
X - Rohm, Japan	1-5-88

RAD HARD 15

PACKAGING INFORMATION

Package Outlines

Dual-In-Line Ceramic Packages



F14.3 MIL-STD-1835 GDIP1-T14 (D-1, CONFIGURATION A)
14 LEAD FRIT SEAL DUAL-IN-LINE CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	6
Q	0.015	0.060	0.38	1.52	7
S1	0.005	-	0.13	-	8
S2	0.005	-	0.13	-	-
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	14		14		9

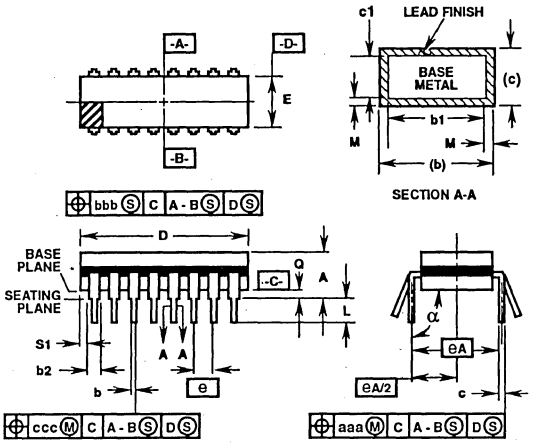
NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Pointed or rounded lead tips are preferred to ease insertion, but are not mandatory.
7. Dimension Q shall be measured from the seating plane to the base plane.
8. Measure dimension S1 at all four corners.
9. N is the maximum number of terminal positions.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD FRIT SEAL DUAL-IN-LINE CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	6
Q	0.015	0.060	0.38	1.52	7
S1	0.005	-	0.13	-	8
S2	0.005	-	0.13	-	-
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		9

Dual-In-Line Ceramic Packages (Continued)



F20.3 MIL-STD-1835 GDIP1-T20 (D-8, CONFIGURATION A)
20 LEAD FRIT SEAL DUAL-IN-LINE CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.060	-	26.92	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	6
Q	0.015	0.070	0.38	1.78	7
S1	0.005	-	0.13	-	8
S2	0.005	-	0.13	-	-
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	20		20		9

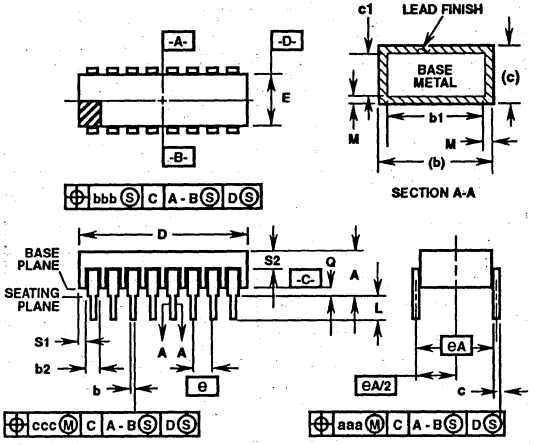
NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Pointed or rounded lead tips are preferred to ease insertion, but are not mandatory.
7. Dimension Q shall be measured from the seating plane to the base plane.
8. Measure dimension S1 at all four corners.
9. N is the maximum number of terminal positions.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.

F24.6 MIL-STD-1835 GDIP1-T24 (D-3, CONFIGURATION A)
24 LEAD FRIT SEAL DUAL-IN-LINE CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.290	-	32.77	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.120	0.200	3.05	5.08	6
Q	0.015	0.075	0.38	1.91	7
S1	0.005	-	0.13	-	8
S2	0.005	-	0.13	-	-
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	24		24		9

Dual-In-Line Ceramic Packages (Continued)



D14.3 MIL-STD-1835 CDIP2-T14 (D-1, CONFIGURATION C)
14 LEAD METAL SEAL DUAL-IN-LINE CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	6
Q	0.015	0.060	0.38	1.52	7
S1	0.005	-	0.13	-	8
S2	0.005	-	0.13	-	9
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	14		14		10

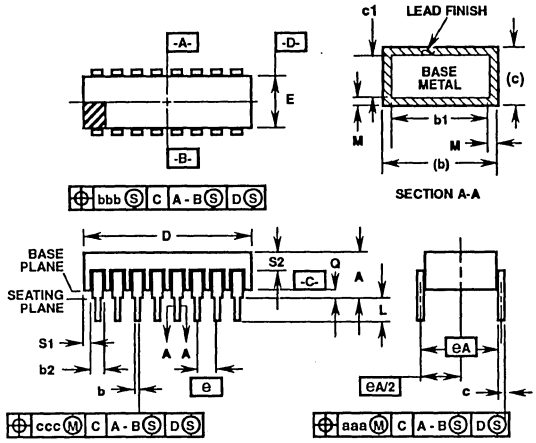
NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Pointed or rounded lead tips are preferred to ease insertion, but are not mandatory.
7. Dimension Q shall be measured from the seating plane to the base plane.
8. Measure dimension S1 at all four corners.
9. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
10. N is the maximum number of terminal positions.
11. Braze fillets shall be concave.
12. Dimensioning and tolerancing per ANSI Y14.5M - 1982.

D16.3 MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 LEAD METAL SEAL DUAL-IN-LINE CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	6
Q	0.015	0.060	0.38	1.52	7
S1	0.005	-	0.13	-	8
S2	0.005	-	0.13	-	9
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		10

Dual-In-Line Ceramic Packages (Continued)



D18.3 MIL-STD-1835 CDIP2-T18 (D-6, CONFIGURATION C)
18 LEAD METAL SEAL DUAL-IN-LINE CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.960	-	24.38	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	6
Q	0.015	0.070	0.38	1.78	7
S1	0.005	-	0.13	-	8
S2	0.005	-	0.13	-	9
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	18		18		10

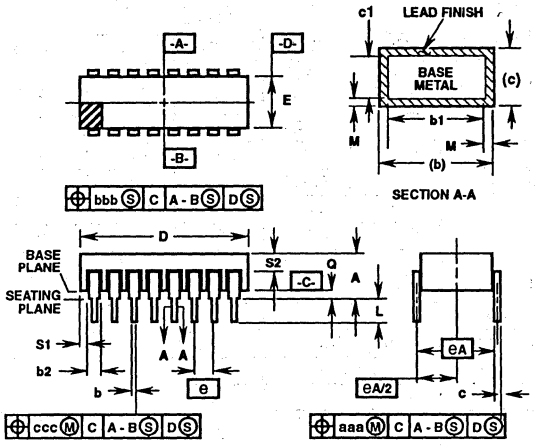
NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Pointed or rounded lead tips are preferred to ease insertion, but are not mandatory.
7. Dimension Q shall be measured from the seating plane to the base plane.
8. Measure dimension S1 at all four corners.
9. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
10. N is the maximum number of terminal positions.
11. Braze fillets shall be concave.
12. Dimensioning and tolerancing per ANSI Y14.5M - 1982.

D20.3 MIL-STD-1835 CDIP2-T20 (D-8, CONFIGURATION C)
20 LEAD METAL SEAL DUAL-IN-LINE CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.060	-	26.92	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	6
Q	0.015	0.070	0.38	1.78	7
S1	0.005	-	0.13	-	8
S2	0.005	-	0.13	-	9
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	20		20		10

Dual-In-Line Ceramic Packages (Continued)



D22.4 MIL-STD-1835 CDIP2-T22 (D-7, CONFIGURATION C)
22 LEAD METAL SEAL DUAL-IN-LINE CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.111	-	28.22	5
E	0.350	0.410	8.89	10.41	5
e	0.100 BSC		2.54 BSC		-
eA	0.400 BSC		10.16 BSC		-
eA/2	0.200 BSC		5.08 BSC		-
L	0.125	0.200	3.18	5.08	6
Q	0.015	0.070	0.38	1.78	7
S1	0.005	-	0.13	-	8
S2	0.005	-	0.13	-	9
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	22		22		10

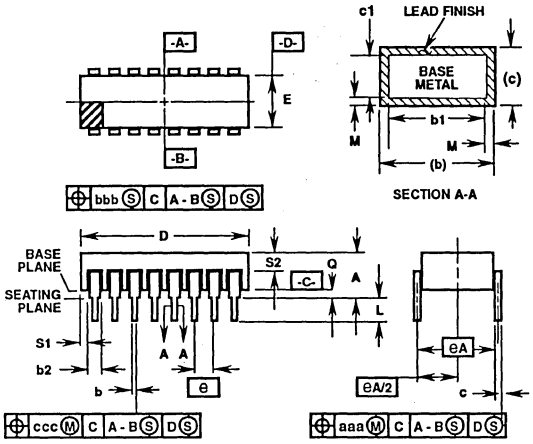
NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Pointed or rounded lead tips are preferred to ease insertion, but are not mandatory.
7. Dimension Q shall be measured from the seating plane to the base plane.
8. Measure dimension S1 at all four corners.
9. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
10. N is the maximum number of terminal positions.
11. Braze fillets shall be concave.
12. Dimensioning and tolerancing per ANSI Y14.5M - 1982.

D24.6 MIL-STD-1835 CDIP2-T24 (D-3, CONFIGURATION C)
24 LEAD METAL SEAL DUAL-IN-LINE CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.290	-	32.77	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.120	0.200	3.05	5.08	6
Q	0.015	0.075	0.38	1.91	7
S1	0.005	-	0.13	-	8
S2	0.005	-	0.13	-	9
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	24		24		10

Dual-In-Line Ceramic Packages (Continued)



D28.6 MIL-STD-1835 CDIP2-T28 (D-10, CONFIGURATION C)
28 LEAD METAL SEAL DUAL-IN-LINE CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.232	-	5.92	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.490	-	37.85	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	6
Q	0.015	0.060	0.38	1.52	7
S1	0.005	-	0.13	-	8
S2	0.005	-	0.13	-	9
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	28		28		10

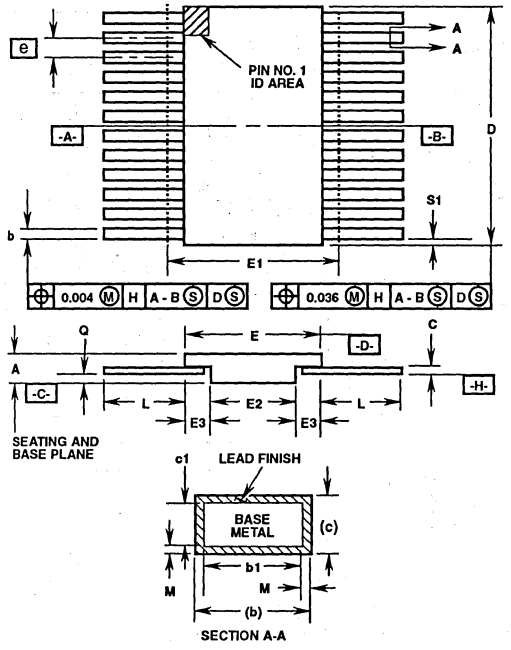
NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Pointed or rounded lead tips are preferred to ease insertion, but are not mandatory.
7. Dimension Q shall be measured from the seating plane to the base plane.
8. Measure dimension S1 at all four corners.
9. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
10. N is the maximum number of terminal positions.
11. Braze fillets shall be concave.
12. Dimensioning and tolerancing per ANSI Y14.5M - 1982.

D40.6 MIL-STD-1835 CDIP2-T40 (D-5, CONFIGURATION C)
40 LEAD METAL SEAL DUAL-IN-LINE CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	2.096	-	53.24	5
E	0.510	0.620	12.95	15.75	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	6
Q	0.015	0.070	0.38	1.78	7
S1	0.005	-	0.13	-	8
S2	0.005	-	0.13	-	9
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	40		40		10

Ceramic Flatpack Packages



K14.A MIL-STD-1835 CDFP3-F14 (F-2A, CONFIGURATION B)
14 LEAD METAL SEAL CERAMIC FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.390	-	9.91	3
E	0.235	0.260	5.97	6.60	-
E1	-	0.290	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.270	0.370	6.86	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	14		14		-

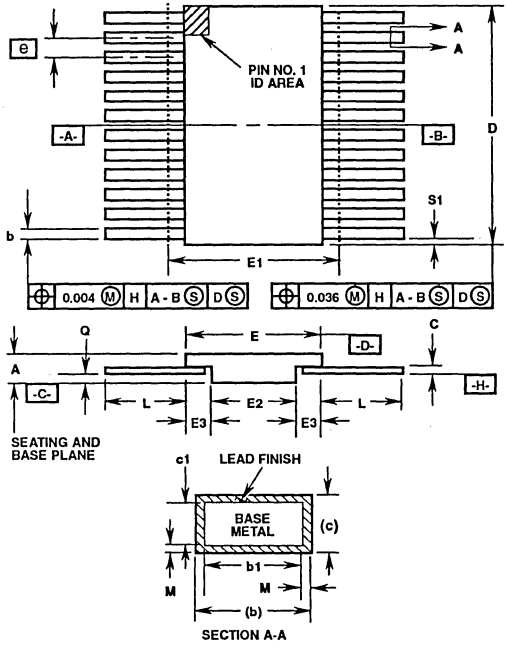
NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternatively, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.

K16.A MIL-STD-1835 CDFP4-F16 (F-5A, CONFIGURATION B)
16 LEAD METAL SEAL CERAMIC FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.25	0.56	-
b1	0.015	0.019	0.25	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.440	-	11.18	3
E	0.245	0.285	6.22	7.24	-
E1	-	0.315	-	8.00	3
E2	0.130	-	3.30	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	16		16		-

Ceramic Flatpack Packages (Continued)



K20.A MIL-STD-1835 CDFP4-F20 (F-9A, CONFIGURATION B)
20 LEAD METAL SEAL CERAMIC FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.540	-	13.72	3
E	0.245	0.300	6.22	7.62	-
E1	-	0.330	-	8.38	3
E2	0.130	-	3.30	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.00	-	0.00	-	6
M	-	0.0015	-	0.04	-
N	20		20		-

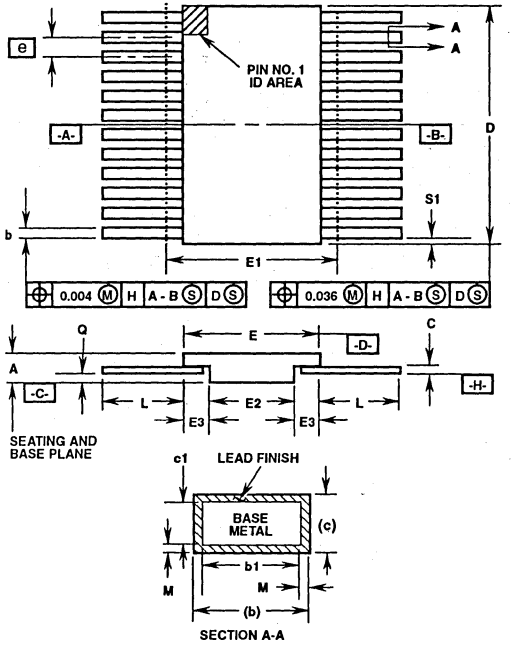
NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.

K24.A MIL-STD-1835 CDFP4-F24 (F-6A, CONFIGURATION B)
24 LEAD METAL SEAL CERAMIC FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.640	-	16.26	3
E	0.350	0.420	9.14	10.67	-
E1	-	0.450	-	11.43	3
E2	0.180	-	4.57	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	24		24		-

Ceramic Flatpack Packages (Continued)



K28.A MIL-STD-1835 CDFP3-F28 (F-11A, CONFIGURATION B)
28 LEAD METAL SEAL CERAMIC FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.740	-	18.80	3
E	0.460	0.520	11.68	13.21	-
E1	-	0.550	-	13.97	3
E2	0.180	-	4.57	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.00	-	0.00	-	6
M	-	0.0015	-	0.04	-
N	28		28		-

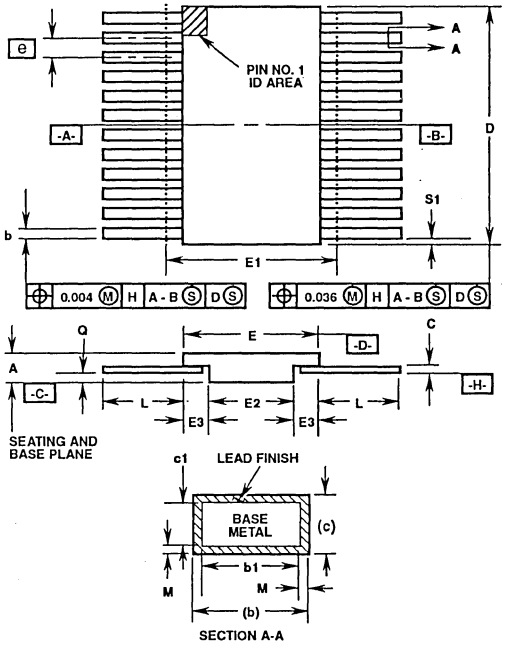
NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.

K16.B
16 LEAD METAL SEAL CERAMIC FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.115	-	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.003	0.009	0.08	0.23	-
c1	0.003	0.006	0.08	0.15	-
D	-	0.440	-	11.18	3
E	0.280	0.295	7.24	7.49	-
E1	-	0.315	-	8.00	3
E2	0.130	-	3.30	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	16		16		-

Ceramic Flatpack Packages (Continued)



K18.A

18 LEAD METAL SEAL CERAMIC FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.100	-	2.54	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	0.430	0.450	10.92	11.43	3
E	0.320	0.340	8.13	8.64	-
E1	-	0.360	-	9.14	3
E2	0.220	0.240	5.59	6.10	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.280	0.320	7.11	8.13	-
Q	0.012	-	0.30	-	8
S1	-	-	-	-	-
M	-	0.0015	-	0.04	-
N	18		18		-

NOTES:

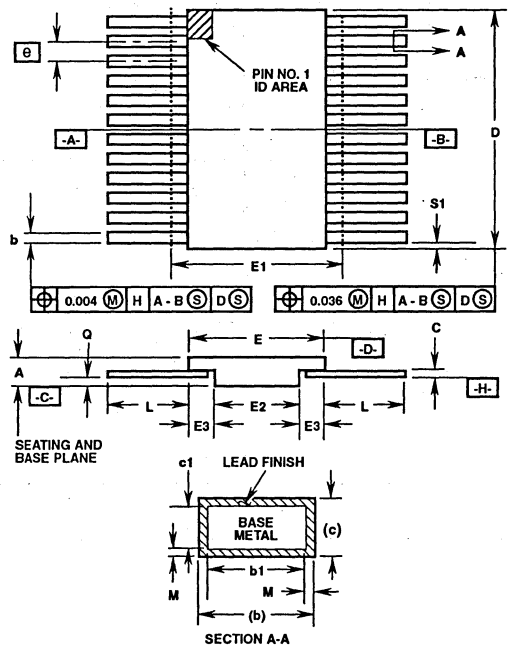
1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.

K24.B

24 LEAD METAL SEAL CERAMIC FLATPACK PACKAGE

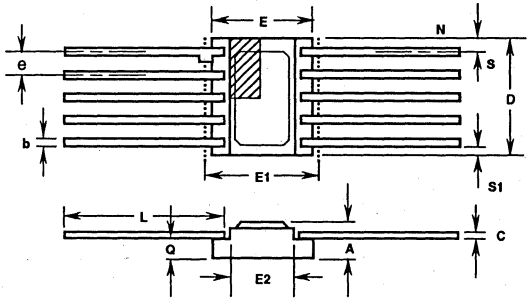
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.070	0.115	1.78	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	0.590	0.610	14.99	15.49	3
E	0.490	0.510	12.45	12.95	-
E1	-	0.520	-	13.20	3
E2	0.370	0.390	9.40	9.91	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	-	-	-	-	-
L	0.330	0.350	8.38	8.89	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	24		24		-

Ceramic Flatpack Packages (Continued)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
1. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish A is applied.
1. This dimension allows for off-center lid.
1. The basic lead spacing is 0.050 inch (1.27mm) between center lines. Each lead centerline shall be located within ± 0.005 inch (0.13mm) of its exact longitudinal position relative to lead 1 and the highest numbered (N) lead.
1. All leads: increase maximum limit by 0.003 inch (0.08mm) measured at the center of the flat, when lead finish A (solder dip) is applied.

K36.A

36 LEAD METAL SEAL CERAMIC FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.138	-	3.51	-
b	0.006	0.013	0.15	0.33	-
b1	0.006	0.010	0.15	0.25	-
c	0.004	0.011	0.10	0.28	-
c1	0.004	0.008	0.10	0.20	-
D	0.620	0.640	15.75	16.26	3
E	0.620	0.640	15.75	8.64	-
E1	-	0.660	-	16.76	3
E2	0.470	0.490	11.94	12.45	-
E3	0.030	-	0.76	-	7
e	0.025 BSC		0.64 BSC		-
k	-	-	-	-	-
L	0.240	0.280	6.10	7.11	-
Q	0.026	0.045	0.66	1.14	8
S1	-	-	-	-	-
M	-	0.0015	-	0.04	-
N	36		36		-

4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.

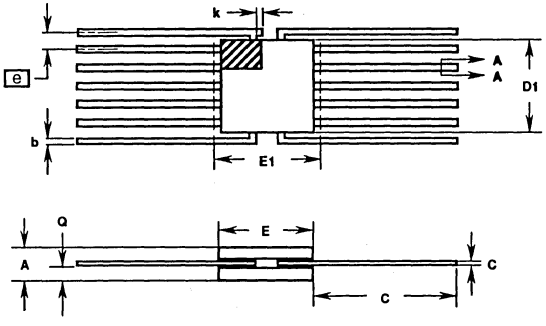
K42.A TOP BRAZED

42 LEAD METAL SEAL CERAMIC FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.100	-	2.54	-
b	0.017	0.023	0.43	0.58	5
c	0.007	0.010	0.18	0.25	5
D	1.045	1.075	26.54	27.31	3
E	0.630	0.650	16.00	16.51	-
E1	-	0.680	-	17.27	3
E2	0.530	0.550	13.46	13.97	-
e	0.050 BSC		1.27 BSC		4, 6
L	0.320	0.350	8.13	8.89	-
Q	0.045	0.065	1.14	1.65	2
S	-	-	-	-	7
S1	0.000	-	0.00	-	7
N	42		42		-

1. Total number of spaces = (N - 2). Symbol "N" is the maximum number of leads.
1. Measure all four corner leads.
1. For bottom-brazed lead configuration. When this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

Ceramic Flatpack Packages (Continued)



NOTES:

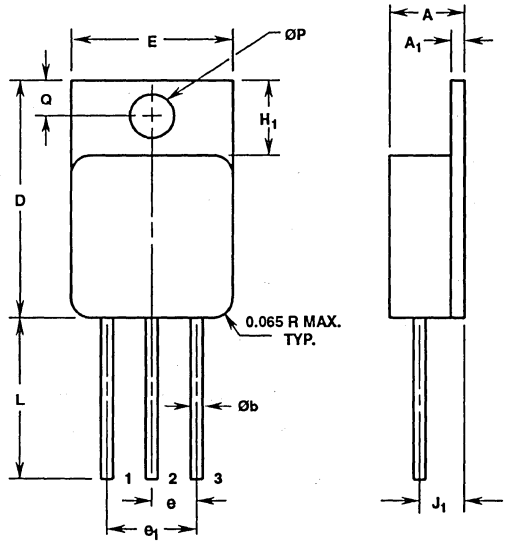
1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternatively, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish A is applied.

A14.A

14 LEAD FRIT SEAL CERAMIC FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.085	-	2.16	-
b	0.013	0.020	0.33	0.51	-
b1	0.013	0.017	0.33	0.43	4
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	4
D1	0.238	0.260	6.05	6.60	-
E	0.238	0.260	6.05	6.60	-
E1	-	0.290	-	7.37	3
e	0.050 BSC		1.27 BSC		-
k	0.005	0.015	0.13	0.38	2
L	0.260	0.290	6.60	7.37	-
Q	0.026	0.045	0.66	1.14	6
M	-	0.0015	-	0.04	4
N	14		14		-

Hermetic Metal Packages



TO-254AA

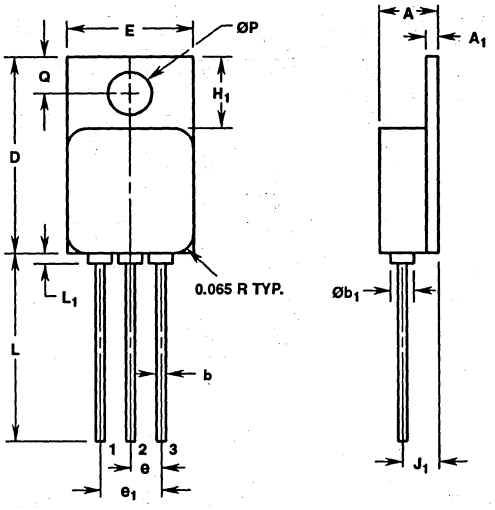
3 LEAD JEDEC HERMETIC METAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.249	0.260	6.33	6.60	-
A_1	0.040	0.050	1.02	1.27	-
Øb	0.035	0.045	0.89	1.14	2, 3
D	0.790	0.800	20.07	20.32	-
E	0.535	0.545	13.59	13.84	-
e	0.150 TYP		3.81 TYP		4
e_1	0.300 BSC		7.62 BSC		4
H_1	0.245	0.265	6.23	6.73	-
J_1	0.140	0.160	3.56	4.06	4
L	0.520	0.560	13.21	14.22	-
ØP	0.139	0.149	3.54	3.78	-
Q	0.110	0.130	2.80	3.30	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC outline TO-254AA dated 11-86.
2. Add typically 0.002 inch (0.05mm) for solder coating.
3. Lead dimension (without solder).
4. Position of lead to be measured 0.250 inch (6.35mm) from bottom of dimension D.
5. Die to base Be0 isolated, terminals to case ceramic isolated.
6. Controlling dimension: inch.
7. Revision 1 dated 1-93.

Hermetic Metal Packages (Continued)



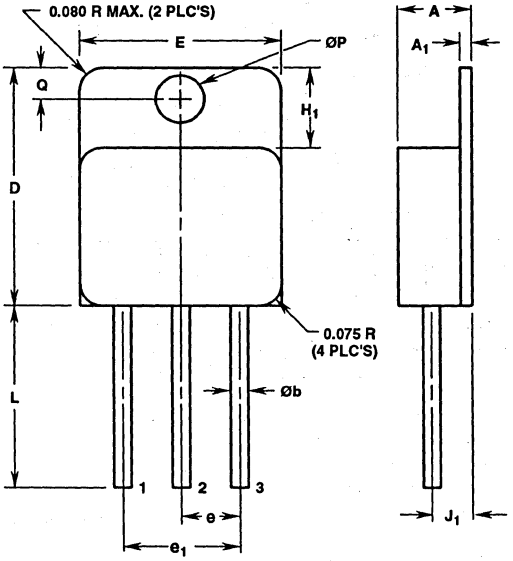
TO-257AA

3 LEAD JEDEC HERMETIC METAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.190	0.200	4.83	5.08	-
A_1	0.035	0.045	0.89	1.14	-
Øb	0.025	0.035	0.64	0.88	2, 3
$Øb_1$	0.060	0.090	1.53	2.28	-
D	0.645	0.665	16.39	16.89	-
E	0.410	0.420	10.42	10.66	-
e	0.100 TYP		2.54 TYP		4
e_1	0.200 BSC		5.08 BSC		4
H_1	0.230	0.250	5.85	6.35	-
J_1	0.110	0.130	2.80	3.30	4
L	0.600	0.650	15.24	16.51	-
L_1	-	0.035	-	0.88	-
ØP	0.140	0.150	3.56	3.81	-
Q	0.113	0.133	2.88	3.37	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. B of JEDEC T0-257AA dated 9-88.
2. Add typically 0.002 inch (0.05mm) for solder coating.
3. Lead dimension (without solder).
4. Position of lead to be measured 0.150 inch (3.81mm) from bottom of dimension D.
5. Die to base Be0 isolated, terminals to case ceramic isolated.
6. Controlling dimension: inch.
7. Revision 1 dated 1-93.



TO-258

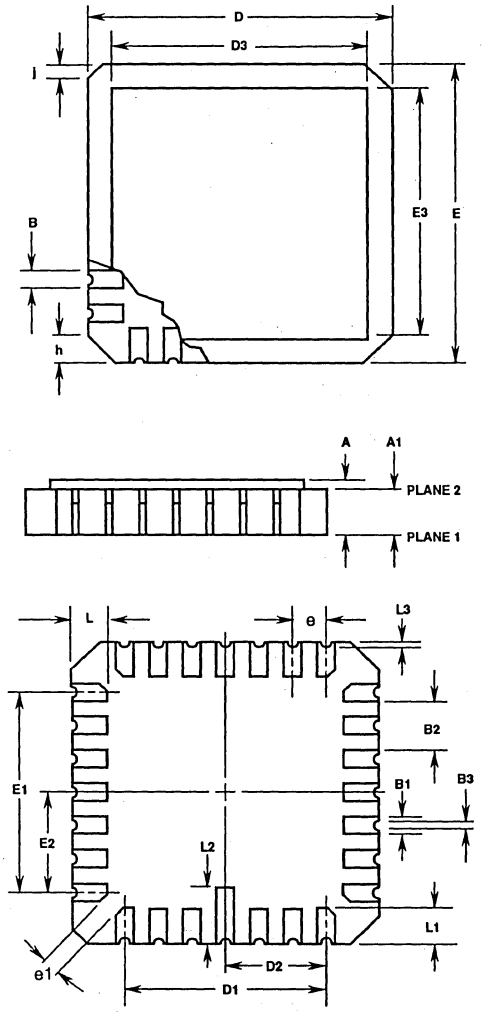
3 LEAD HERMETIC METAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.250	0.270	6.35	6.85	-
A_1	0.035	0.045	0.89	1.14	-
Øb	0.055	0.065	1.40	1.65	2, 3
D	0.810	0.830	20.58	21.08	-
E	0.680	0.700	17.28	17.78	-
e	0.200 TYP		5.08 TYP		4
e_1	0.400 BSC		10.16 BSC		4
H_1	0.270	0.290	6.86	7.36	-
J_1	0.130	0.150	3.31	3.81	4
L	0.600	0.650	15.24	16.51	-
ØP	0.155	0.165	3.94	4.19	-
Q	0.100	0.120	2.54	3.04	-

NOTES:

1. No current JEDEC outline for this package.
2. Add typically 0.002 inch (0.05mm) for solder coating.
3. Lead dimension (without solder).
4. Position of lead to be measured 0.250 inch (6.35mm) from bottom of dimension D.
5. Die to base Be0 isolated, terminals to case ceramic isolated.
6. Controlling dimension: inch.
7. Revision 1 dated 1-93.

Leadless Ceramic Chip Carrier Packages



J18.A

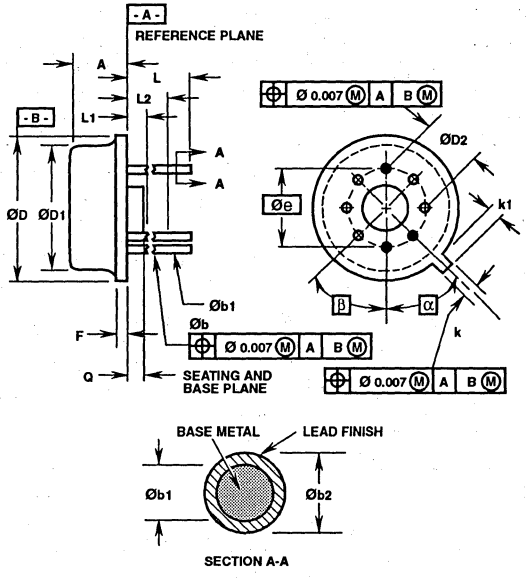
18 PAD METAL SEAL LEADLESS CERAMIC CHIP CARRIER

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.054	0.075	1.37	1.91	6, 7
A1	0.044	0.063	1.12	1.60	7
B	-	-	-	-	-
B1	0.020	0.030	0.51	0.76	2, 4
B2	-	-	-	-	-
B3	0.006	0.022	0.15	0.56	-
D	0.340	0.355	8.64	9.02	-
D1	0.150 BSC		3.81 BSC		-
D2	0.075 BSC		1.91 BSC		-
D3	0.320	0.330	8.13	8.38	1, 2
E	0.410	0.425	10.41	10.80	-
E1	0.200 BSC		5.08 BSC		-
E2	0.100 BSC		2.54 BSC		-
E3	0.390	0.400	9.91	10.16	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.012R REF		0.30R REF		5
j	0.012R REF		0.30R REF		5
L	0.037	0.052	0.94	1.32	-
L1	0.037	0.052	0.94	1.32	-
L2	-	-	-	-	-
L3	0.003	0.015	0.08	0.38	-
ND	4		4		3
NE	5		5		3
N	18		18		3

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.381mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals shall be ellectrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Maximum limits allows for 0.007 inch solder thickness on pads.

Metal Can Packages

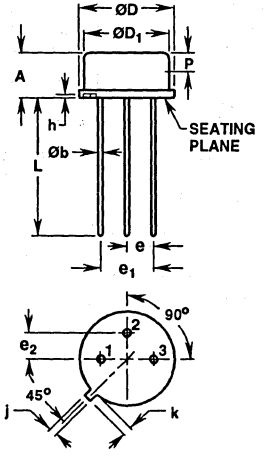


T8.C MIL-STD-1835 MACY1-X8 (A-1)
8 LEAD TO-99 METAL CAN PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
Øb	0.016	0.019	0.41	0.48	1
Øb1	0.016	0.021	0.41	0.53	1
Øb2	0.016	0.024	0.41	0.61	-
ØD	0.335	0.375	8.51	9.40	-
ØD1	0.305	0.335	7.75	8.51	-
ØD2	0.110	0.160	2.79	4.06	-
e	0.200 BSC		5.08 BSC		-
e1	0.100 BSC		2.54 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	0.010	0.045	0.25	1.14	-
α	45° BSC		45° BSC		3
β	45° BSC		45° BSC		3
N	8		8		1, 4

NOTES:

1. (All leads) Øb applies between L1 and L2. Øb1 applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
2. Measured from maximum diameter of the product.
3. α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position (N -1 places) from α, looking at the bottom of the package.
4. N is the maximum number of terminal positions.
5. Dimensioning and tolerancing per ANSI 414.5M - 1982.



TO-205AF

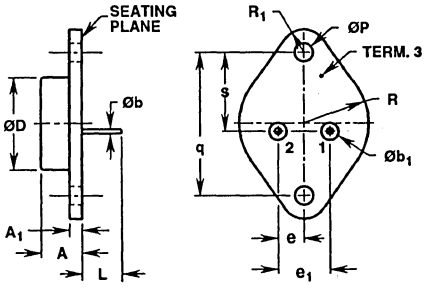
3 LEAD JEDEC TO-205AF HERMETIC METAL CAN PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.160	0.180	4.07	4.57	-
Øb	0.016	0.021	0.41	0.53	2, 3
ØD	0.350	0.370	8.89	9.39	-
$ØD_1$	0.315	0.335	8.01	8.50	-
e	0.095	0.105	2.42	2.66	4
e_1	0.190	0.210	4.83	5.33	4
e_2	0.095	0.105	2.42	2.66	4
h	0.010	0.020	0.26	0.50	-
j	0.028	0.034	0.72	0.86	-
k	0.029	0.045	0.74	1.14	-
L	0.500	0.540	12.70	13.71	3
P	0.075	-	1.91	-	5

NOTES:

1. These dimensions are within allowable dimensions of Rev. E of JEDEC TO-205AF outline dated 11-82.
2. Lead dimension (without solder).
3. Solder coating may vary along lead length, add typically 0.002 inch (0.05mm) for solder coating.
4. Position of lead to be measured 0.100 inch (2.54mm) from bottom of seating plane.
5. This zone controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 inch (0.254mm).
6. Controlling dimension: inch.
7. Revision 1 dated 1-93.

Hermetic Steel Packages



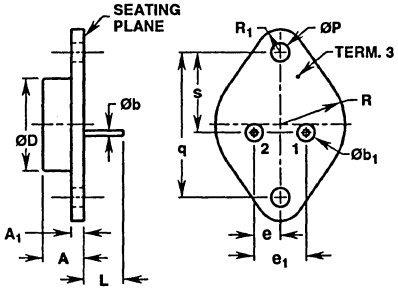
TO-204AA

JEDEC TO-204AA HERMETIC STEEL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.310	0.330	7.88	8.38	-
A_1	0.060	0.065	1.53	1.65	-
Øb	0.038	0.042	0.97	1.06	2, 3
$Øb_1$	0.138	0.145	3.51	3.68	-
ØD	-	0.800	-	20.32	-
e	0.215 TYP		5.46 TYP		4
e_1	0.430 BSC		10.92 BSC		4
L	0.440	0.460	11.18	11.68	-
ØP	0.155	0.160	3.94	4.06	-
q	1.187 BSC		30.15 BSC		-
R	0.495	0.525	12.58	13.33	-
R_1	0.131	0.185	3.33	4.69	-
s	0.655	0.675	16.64	17.14	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-204AA outline dated 11-82.
2. Lead dimension (without solder).
3. Add typically 0.002 inch (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inch (6.35mm) from bottom of seating plane.
5. Controlling dimension: inch.
6. Revision 1 dated 1-93.



TO-204AE

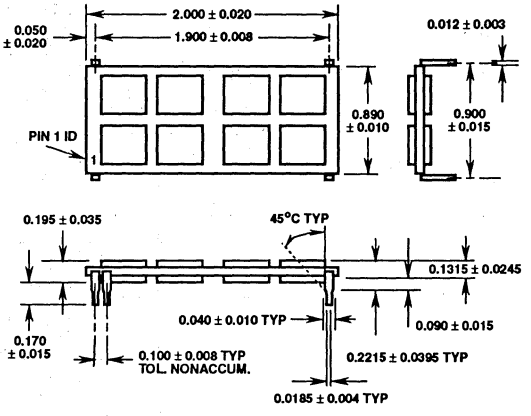
JEDEC TO-204AE HERMETIC STEEL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.310	0.330	7.88	8.38	-
A_1	0.060	0.065	1.53	1.65	-
Øb	0.057	0.063	1.45	1.60	2, 3
$Øb_1$	0.138	0.145	3.51	3.68	-
ØD	-	0.800	-	20.32	-
e	0.215 TYP		5.46 TYP		4
e_1	0.430 BSC		10.92 BSC		4
L	0.440	0.460	11.18	11.68	-
ØP	0.155	0.160	3.94	4.06	-
q	1.187 BSC		30.15 BSC		-
R	0.495	0.525	12.58	13.33	-
R_1	0.131	0.185	3.33	4.69	-
s	0.655	0.675	16.64	17.14	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-204AE outline dated 11-82.
2. Lead dimension (without solder).
3. Add typically 0.002 inch (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inch (6.35mm) from bottom of seating plane.
5. Controlling dimension: inch.
6. Revision 1 dated 1-93.

HS-6564RH MODULE



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