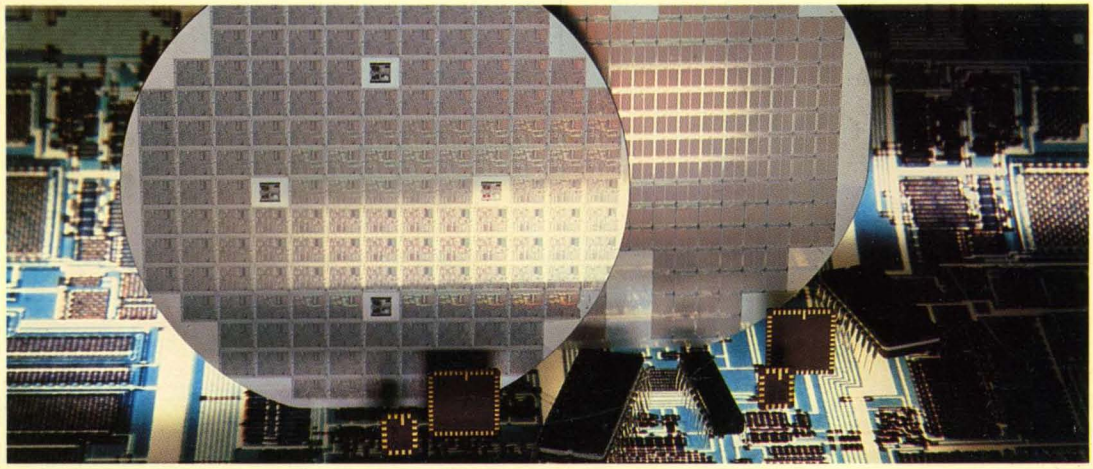
Western Microtechnology
10040 Bubb Road
Cupertino, CA 95014
Phone (408) 725-1660
TWX 910-338-0013

CMOS
DIGITAL DATA BOOK



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1984 Harris CMOS Digital Data Book

Harris Semiconductor CMOS Digital Products Division's products represent state-of-the-art in density and high performance. The HARRIS expertise in CMOS design and processing offers the user the most reliable product available in a wide choice of formats, options, and package types. With continuing research and development and the introduction of new products, Harris will provide its customers with the most advanced CMOS technology.

This book describes Harris Semiconductor CMOS Digital Products Division's complete line of digital products and includes a complete set of product specifications and data sheets. Also included are sections on reliaiblity, programming, and packaging.

Please fill out the registration card at the back of this book and return it to us so we may keep you informed of our latest new product developments over the next year.

If you need more information on these and other HARRIS products, please contact the nearest HARRIS sales office listed in the back of this data book.

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CMOS 1984 Digital Data Book

General Information 1

CMOS Memory 2

CMOS 80C86 Family 3

CMOS 12-Bit Microprocessors & Peripherals 4

CMOS Data Communication 5

Harris Reliability and Quality 6

Hi-Reliability & Military Products 7

Article Reprints 8

Custom — Semi-Custom CMOS IC Information 9

Ordering and Packaging 10

DICE Information 11

Appendices 12

Table of Contents

		PAGE
SECTION 1	GENERAL INFORMATION	
	Sector Capabilities	1-2
	CMOS Alpha-Numeric Index	1-3
	CMOS Devices by Families	1-4
	Classification of Literature	1-6
	Symbols and Abbrevations	1-6
SECTION 2	CMOS MEMORY	
	CMOS Memory Product Index	2-2
	Low Voltage Data Retention	2-3
	Industry CMOS RAM Cross-Reference	2-4
	1K CMOS RAM Data Sheets	2-5
	4K CMOS RAM Data Sheets	2-29
	16K CMOS RAM Data Sheets	2-51
	CMOS RAM Module Data Sheets	2-85
	CMOS PROM Data Sheets	2-113
	Preview of CMOS PROM Products	2-126
	Programming Format for Harris PROMs	2-127
	Preview of Future CMOS HPL Circuits	2-130
SECTION 3	CMOS 80C86 FAMILY	
	CMOS 80C86 Family Product Index	3-2
	CMOS 80C86 Family Cross Reference	3-3
	Harris 80C86 Family Data Sheets	3-4
	Preview of Future Harris 80C86 Family Products	3-96
SECTION 4	CMOS 12 BIT MICROPROCESSORS AND PERIPHERALS	
	CMOS 12 Bit Microprocessor and Peripheral Product Index	4-2
	CMOS Microprocessor Data Sheets	4-3
	CMOS Peripheral Data Sheets	4-59
SECTION 5	CMOS DATA COMMUNICATIONS	
	CMOS Data Communications Product Index	5-2
	CMOS Data Communications Data Sheets	5-3
SECTION 6	HARRIS RELIABILITY AND QUALITY	
	Harris Reliability and Quality Table of Contents	6-1
SECTION 7	HARRIS HI-REL AND MILITARY PRODUCTS	
	Harris Hi-Rel and Military Products Table of Contents	7-1
SECTION 8	ARTICLE REPRINTS	
	Article Reprints Table of Contents	8-2
SECTION 9	CUSTOM – SEMI-CUSTOM CMOS IC INFORMATION	
	Custom – Semi-Custom CMOS IC Information Table of Contents	9-1
SECTION 10	ORDERING AND PACKAGING	
	Ordering and Packaging Information	10-1
SECTION 11	DICE INFORMATION	
	Dice Information	11-1
SECTION 12	APPENDICES	
	Sector Alpha-Numeric Product Index	12-3
	Harris Sales Locations	12-8

CMOS General Information 1

Sector Capabilities	1-2
CMOS Alpha-Numeric Index	1-3
CMOS Devices by Families	1-4
Classification of Literature	1-6
Symbols and Abbreviations	1-6

Harris Semiconductor
Sector Capabilities

Harris Semiconductor is one of the five management groups of Harris Corporation, a producer of high-technology communication and information processing systems sold in over 160 countries. Five main operations of Harris Semiconductor produce standard and custom semiconductor devices. These operations are:

ANALOG PRODUCTS DIVISION
Harris is a major force in analog integrated circuitry, offering a broad line of products including: analog-to-digital converters, digital-to-analog converters, switches, multiplexers, voltage references, operational amplifiers, telecommunications and speech processing products.

BIPOLAR DIGITAL PRODUCTS DIVISION
Harris introduced the industry's first bipolar programmable read only memory in 1970 and has continued as a leader in the field of bipolar PROMs. Harris offers a complete spectrum of bipolar PROMs from 256 bits to 64K bits. Also, offered is a new family of programmable logic products featuring on-chip testability.

CMOS DIGITAL PRODUCTS DIVISION
Harris is a pioneer in developing and producing digital CMOS products including: CMOS RAMs, CMOS PROMs, CMOS microprocessors, CMOS peripherals, CMOS data communications products, and this year introducing a full line of 80C86 microprocessors and peripherals.

CUSTOM INTEGRATED CIRCUITS DIVISION
Harris designs, develops and manufactures custom analog, digital bipolar, radiation-hardened, and CMOS circuits for specialized military and commercial applications.

MICROWAVE SEMICONDUCTOR, INC.
Harris Microwave Semiconductor, Inc. develops and manufactures gallium arsenide transistors, integrated circuits and microwave amplifiers.

CMOS Alpha-Numeric Index

PRODUCT	DESCRIPTION	PAGE NO.
HD-15530	Manchester Encoder-Decoder	5-3
HD-15531	Manchester Encoder-Decoder	5-10
HD-4702	Programmable Bit Rate Generator	5-56
HD-6101	Parallel Interface Element	4-51
HD-6120	12 Bit High Performance Microprocessor	4-3
HD-6121	I/O Controller	4-22
HD-6402	LSI Universal Asynchronous Receiver Transmitter	5-51
HD-6406	Programmable Asynchronous Communication Interface	5-39
HD-6408	Asynchronous Manchester Adapter	5-25
HD-6409	Manchester Encoder-Decoder	5-30
HD-6431	Hex Latching Bus Driver	4-59
HD-6432	Hex Bi-directional Bus Driver	4-62
HD-6433	Quad Bus Separator/Driver	4-65
HD-6434	Octal Resettable Latch	4-68
HD-6436	Octal Bus Buffer/Driver	4-71
HD-6440	Latch Decoder/Driver	4-74
HD-6495	Hex Bus Driver	4-78
HM-6100	12 Bit Static Microprocessor	4-30
HM-6504	4K X 1 Synchronous RAM	2-29
HM-6508	1K X 1 Synchronous RAM	2-5
HM-6514	1K X 4 Synchronous RAM	2-40
HM-6516	2K X 8 Synchronous RAM	2-51
HM-65162	2K X 8 Asynchronous RAM	2-57
HM-65172	2K X 8 Asynchronous RAM	2-70
HM-6518	1K X 1 Synchronous RAM	2-11
HM-65262	16K X 1 Asynchronous RAM	2-83
HM-6551	256 X 4 Synchronous RAM	2-17
HM-6561	256 X 4 Synchronous RAM	2-23
HM-6564	64K Synchronous RAM Module	2-85
HM-6616	2K X 8 Fuse Link PROM	2-118
HM-6641	512 X 8 PROM	2-113
HM-6664	8K X 8 Fuse Link PROM	2-126
HM-92560	256K Synchronous RAM Module	2-96
HM-92570	256K Synchronous RAM Module	2-104
HPL- 16LC8	Programmable Logic	2-130
HPL-16RC4	Programmable Logic	2-132
HPL-16RC6	Programmable Logic	2-132
HPL-16RC8	Programmable Logic	2-132
80C86	16 Bit Microprocessor	3-4
80C88	8 Bit Microprocessor	3-96
82C37A	High Performance Programmable DMA Controller	3-97
82C52	Full Duplex UART	3-27
82C54	Programmable Interval Timer	3-28
82C55A	Programmable Peripheral Interface	3-43
82C59A	Priority Interrupt Controller	3-62
82C82	Octal Latch	3-77
82C83	Octal Latching Inverting Bus Driver	3-98
82C84A	Clock Generator/Driver	3-82
82C84B	Clock Generator Driver	3-99
82C86	Octal Bus Transceiver	3-100
82C87	Octal Bus Transceiver	3-101
82C88	Bus Controller	3-89
82C89	Bus Arbiter	3-102

CMOS Devices by Families

CMOS Microprocessor and Support Circuits

		PAGE
8/16 BIT MICROPROCESSORS		
80C86	16 Bit CMOS Microprocessor	3-4
80C88	8 Bit CMOS Microprocessor	3-96
80C86/88 PERIPHERAL CIRCUITS		
82C37A	CMOS DMA Controller	3-97
82C52	CMOS Serial Communication Interface	3-27
82C54	CMOS Programmable Interval Timer	3-28
82C55A	CMOS Programmable Peripheral Interface	3-43
82C59A	CMOS Priority Interrupt Controller	3-62
80C86/88 BUS SUPPORT CIRCUITS		
82C82	CMOS Octal Latching Bus Driver	3-77
82C83	CMOS Octal Latching Inverting Bus Driver	3-98
82C84A	CMOS Clock Generator Driver	3-82
82C84B	CMOS Clock Generator Driver	3-99
82C86	CMOS Octal Bus Transceiver	3-100
82C87	CMOS Octal Inverting Bus Transceiver	3-101
82C88	CMOS Bus Controller	3-89
82C89	CMOS Bus Arbiter	3-102
12 BIT MICROPROCESSORS		
HM-6100	CMOS 12 Bit Microprocessor	4-30
HD-6120	CMOS High Performance 12 Bit Microprocessor	4-3
12 BIT PERIPHERAL CONTROLLERS		
HD-6101	CMOS Parallel Interface Element (PIE)	4-51
HD-6121	CMOS I/O Controller (IOC)	4-22
BUS SUPPORT CIRCUITS		
HD-6431	CMOS Hex Latching Bus Driver	4-59
HD-6432	CMOS Hex Bi-directional Bus Driver	4-62
HD-6433	CMOS Quad Bus Separator/Driver	4-65
HD-6434	CMOS Octal Bus Driver W/Reset	4-68
HD-6436	CMOS Octal Bus Buffer/Driver	4-71
HD-6440	CMOS Latched 3 to 8 Line Decoder/Driver	4-74
HD-6495	CMOS Hex Bus Driver	4-78
SERIAL COMMUNICATION CIRCUITS		
HD-4702	CMOS Bit Rate Generator	5-56
HD-6402	CMOS UART	5-51
HD-6406	CMOS Prog. Async. Communication Interface	5-39
HD-6408	CMOS Async. Serial Manchester Adapter (ASMA)	5-25
HD-6409	CMOS Manchester Encoder-Decoder	5-30
HD-15530	CMOS Manchester Encoder-Decoder	5-3
HD-15531	CMOS Manchester Encoder-Decoder	5-10

CMOS Devices by Families

(continued)

CMOS Static RAMS		PAGE
1K - SYNCHRONOUS		
HM-6508	1K X 1	2-5
HM-6518	1K X 1	2-11
HM-6551	256 X 4	2-17
HM-6561	256 X 4	2-25
4K - SYNCHRONOUS		
HM-6504	4K X 1	2-29
HM-6514	1K X 4	2-40
16K-SYNCHRONOUS		
HM-6516	2K X 8	2-51
16K- ASYNCHRONOUS		
HM-65162	2K X 8	2-57
HM-65172	2K X 8	2-70
HM-65262	16K X 1	2-83
CMOS RAM MODULES		
HM-6564	64K	2-85
HM-92560	256K	2-96
HM-92570	Buffered 256K	2-104
CMOS RADIATION HARDENED RAMS		
HS-6504RH	4K X 1	9-18
HS-6508RH	1K X 1	9-19
HS-6514RH	1K X 4	9-20
HS-6551RH	256 X 4	9-21
HS-6564RH	16K X 4 or 8K X 8	9-2

CMOS Fuse Link PROMS		
HM-6641	512 X 8	2-113
HM-6616	2K X 8	2-118
HM-6664	8K X 8	2-126

CMOS Programmable Logic		
HPL-16LC8	Programmable Logic	2-130
HPL-16RC4	Programmable Logic	2-132
HPL-16RC6	Programmable Logic	2-132
HPL-16RC8	Programmable Logic	2-132

Classification of Literature

CLASSIFICATION	PRODUCT STAGE	DISCLAIMERS
Preview DATA SHEET	Formative or Design	This document contains the design specifications for product under development. Specifications may be changed in any manner without notice.
Advance Information DATA SHEET	Sampling or Pre-Production	This is advanced information, and specifications are subject to change without notice.
Preliminary DATA SHEET	First Production	Supplementary data may be published at a later date. Harris reserves the right to make changes at any-time without notice, in order to improve design and supply the best product possible.

Symbols & Abbreviations

This data book utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe that, once acclimated, you will find this standardized format easy to read and use.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

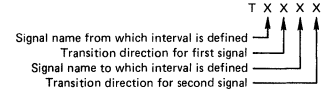
V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurements. Examples:

VIL — Input Low Voltage
IOZ — Output Leakage Current

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:



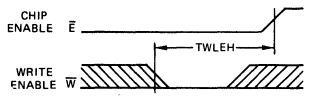
Signal Definitions:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S = Chip Select
G = Output Enable

Transition Definitions:

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)

EXAMPLE:



The example shows Write pulse setup time defined as TWLEH-Time from Write enable Low to chip Enable High.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	—	HIGH IMPEDANCE

CMOS

CMOS Memory 2

Product Index 2-2

Low Voltage Data Retention 2-3

Industry CMOS RAM Cross-Reference 2-4

Product Information 2-5

CMOS Memory Product Index

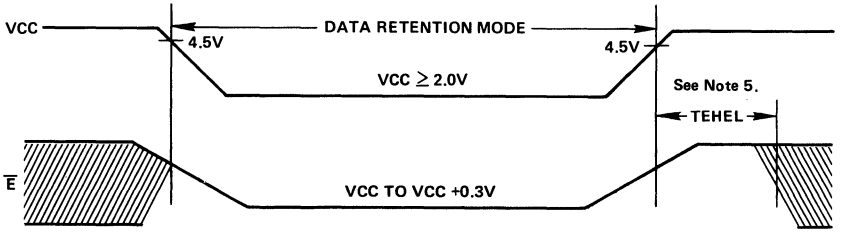
		PAGE
1K CMOS RAM DATA SHEETS		
HM-6508	1K x 1 Synchronous RAM	2-5
HM-6518	1K x 1 Synchronous RAM	2-11
HM-6551	256 x 4 Synchronous RAM	2-17
HM-6561	256 x 4 Synchronous RAM	2-23
4K CMOS RAM DATA SHEETS		
HM-6504	4K x 1 Synchronous RAM	2-29
HM-6514	1K x 4 Synchronous RAM	2-40
16K CMOS RAM DATA SHEETS		
HM-6516	2K x 8 Synchronous RAM	2-51
HM-65162	2K x 8 Asynchronous RAM	2-57
HM-65172	2K x 8 Asynchronous RAM	2-70
PREVIEW OF FUTURE CMOS RAM PRODUCTS		
HM-65262	16K x 1 Asynchronous RAM	2-83
CMOS RAM MODULE DATA SHEETS		
HM-6564	64K Synchronous RAM Module	2-85
HM-92560	256K Synchronous RAM Module	2-96
HM-92570	256K Synchronous RAM Module	2-104
CMOS PROM DATA SHEETS		
HM-6641	512 x 8 Fuse Link PROM	2-113
HM-6616	2K x 8 Fuse Link PROM	2-118
PREVIEW OF FUTURE CMOS PROM PRODUCTS		
HM-6664	8K x 8 Fuse Link PROM	2-126
PROGRAMMING FORMAT FOR HARRIS PROMs		2-128
PREVIEW OF FUTURE CMOS HPL CIRCUITS		
HPL-16LC8	Programmable Logic	2-130
HPL-16RC4	Programmable Logic	2-132
HPL-16RC6	Programmable Logic	2-132
HPL-16RC8	Programmable Logic	2-132

Low Voltage Data Retention

HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC to VCC +0.3V
2. On RAMs which have selects or output enables (e.g. $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL (for synchronous RAMs) and > 55ns (for asynchronous RAMs) after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



HARRIS CMOS/NMOS RAM Cross-Reference

CMOS RAMs

	FEATURES	AMI	FUJITSU	HITACHI	IDT	INTERSIL	MICRO POWER SYSTEMS	MITSUBISHI	MOTOROLA	NATIONAL	NEC	OKI	RCA	TOSHIBA	NMOS MEMORIES (GENERIC)
1K CMOS RAMs															
HM-6508 – 1K x 1	16 PIN SYNCH	6508	8401			6508	6508		6508	6508 74C929	443		6508 1821	5508	2125 4015
HM-6518 – 1K x 1	18 PIN SYNCH	6518				6518	6518		6518	6518 74C930					
HM-6561 – 256 x 4	22 PIN SYNCH					6551				6551 74C920			1822	5101	2101
HM-6561 – 256 x 4	18 PIN SYNCH					6561									2111
4K CMOS RAMs															
HM-6504 – 4K x 1	18 PIN SYNCH	6504	8404	4315 6147		6504	6504		6504	6504		5104		5504	2141/47 315D 4104 4404
HM-6514 – 1K x 4	18 PIN SYNCH	6514	8414	4334 6148		6514	6514	58981	6514	6514	444	5114 5115	5114	5514	2114 2148/49 4045 314A
16K CMOS RAMs															
HM-6516 – 2K x 8	24 PIN SYNCH	6516								6516					
HM-65162 – 2K x 8	24 PIN ASYNCH		8416	6116	6116			5117	65116	6116	446	5128	6116	5517	4802 2116 2016 4016
HM-65172 – 2K x 8	24 PIN ASYNCH		8418	6117				5116			449			5516	
HM-65262 – 16K x 1	20 PIN ASYNCH			6167	6167										2167 8167

HM-6508

1024 x 1 CMOS RAM

Features

- LOW STANDBY POWER — 50 μW MAX
- LOW OPERATING POWER — 20mW/MHz MAX
- FAST ACCESS TIME — 180nsec MAX
- DATA RETENTION VOLTAGE — 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE – 2 TTL LOADS
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTER
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- THREE-STATE OUTPUTS
- 16 PIN PACKAGE FOR HIGH DENSITY

Description

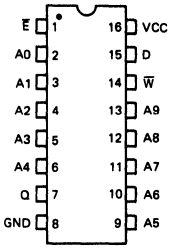
The HM-6508 is a 1024 by 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6508 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

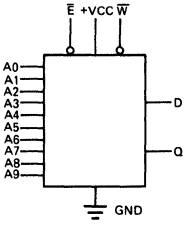
Pinout

TOP VIEW

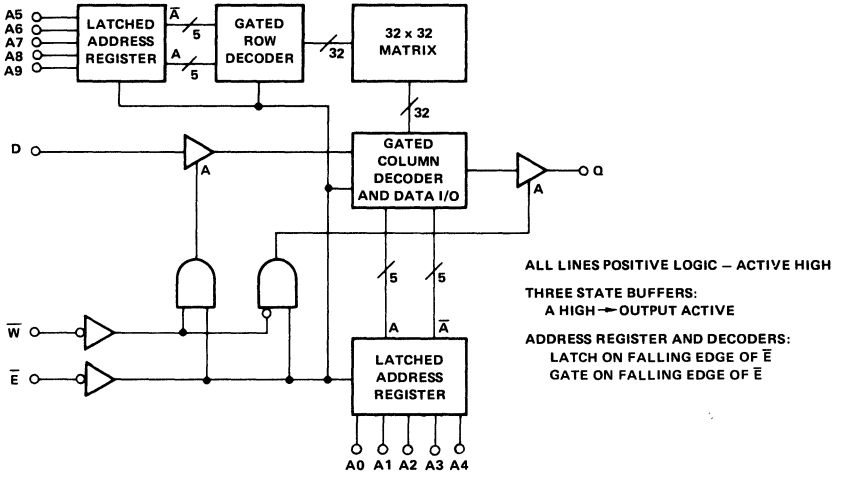


A – Address Input
Ē – Chip Enable
W̄ – Write Enable
D – Data Input
Q – Data Output

Logic Symbol



Functional Diagram



ALL LINES POSITIVE LOGIC – ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

ADDRESS REGISTER AND DECODERS:
LATCH ON FALLING EDGE OF Ē
GATE ON FALLING EDGE OF Ē

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage - (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage -VCC	
		Military (-2)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Industrial (-9)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	-65°C to +150°C	Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	0.1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		5	0.01	μA	VCC = 2.0, IO = 0 VI = VCC or GND $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	6	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		180	100	ns	④
	TAVQV	Address Access Time		180	90	ns	④
	TELQX	Chip Enable Output Enable Time	20	120	40	ns	④
	TWLQZ	Write Enable Output Disable Time		120	40	ns	④
	TEHQZ	Chip Enable Output Disable Time		120	40	ns	④
	TELEH	Chip Enable Pulse Negative Width	180		100	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
	TAVEL	Address Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	40		20	ns	④
	TDVWH	Data Setup Time	80		40	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	100		50	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	100		50	ns	④
	TWLWH	Write Enable Pulse Width	100		50	ns	④
	TELEL	Read or Write Cycle Time	280		150	ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage - (VCC - GND)	-0.3V to +8.0V	Operating Supply Voltage -VCC	
		Military (-2)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (GND +0.3V)	Industrial (-9)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	-65°C to +150°C	Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	0.1	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10	0.01	µA	VCC = 2.0, IO = 0 VI = VCC or GND $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	6	pF	VO=VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		250	110	ns	④
	TAVQV	Address Access Time		250	100	ns	④
	TELQX	Chip Enable Output Enable Time	20	160	60	ns	④
	TWLQZ	Write Enable Output Disable Time		160	60	ns	④
	TEHQZ	Chip Enable Output Disable Time		160	60	ns	④
	TELEH	Chip Enable Pulse Negative Width	250		110	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
	TAVEL	Address Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	50		30	ns	④
	TDVWH	Data Setup Time	110		50	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	130		60	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	130		60	ns	④
	TWLWH	Write Enable Pulse Width	130		60	ns	④
	TELEL	Read or Write Cycle Time	350		160	ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

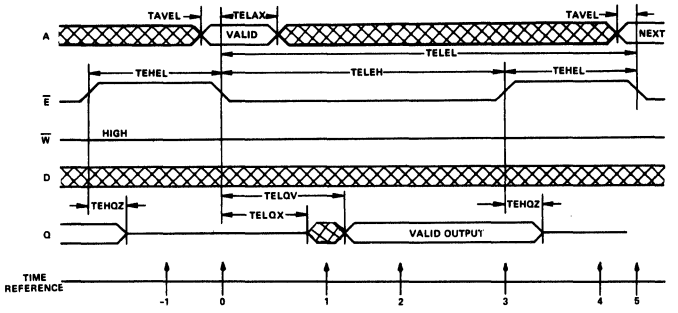
ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -(VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage -VCC Commercial	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)		
Storage Temperature	-65°C to +150°C	Operating Temperature Commercial	0°C to +70°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100	10	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		100	1.0	μA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0			V	$\overline{E}$ = VCC
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.2mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	6	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300	160	ns	④
	TAVQV	Address Access Time		310	160	ns	④
	TELQX	Chip Enable Output Enable Time	20	200	60	ns	④
	TWLQZ	Write Enable Output Disable Time		200	60	ns	④
	TEHQZ	Chip Enable Output Disable Time		200	60	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		160	ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		90	ns	④
	TAVEL	Address Setup Time	10		0	ns	④
	TELAX	Address Hold Time	70		40	ns	④
	TDVWH	Data Setup Time	130		80	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	160		100	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	160		100	ns	④
	TWLWH	Write Enable Pulse Width	160		100	ns	④
	TELEL	Read or Write Cycle Time	450		250	ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

Read Cycle

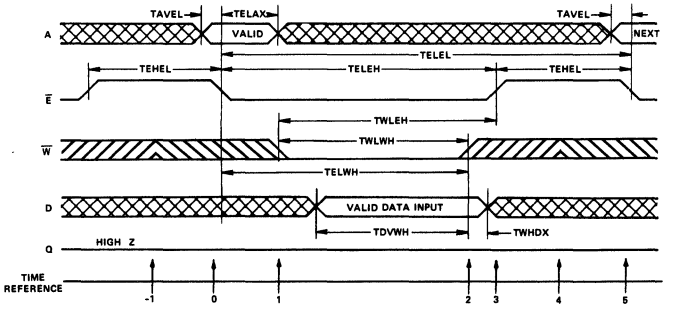


TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUTS Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	X	OUTPUT ENABLED
2	L	H	X	X	V	OUTPUT VALID
3	↗	H	X	X	V	READ ACCOMPLISHED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

In the HM-6508 Read Cycle, the address information is latched into the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the data output becomes enabled; however, the data is not valid until during time (T = 2). $\overline{W}$ must remain high for the read cycle. After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the chip and force the output buffer to a high impedance state. After the required $\overline{E}$ high time (TEHEL) the RAM is ready for the next memory cycle (T = 4).

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUTS Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	X	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	↘	X	X	Z	WRITE PERIOD BEGINS
2	L	↗	X	V	Z	DATA IS WRITTEN
3	↗	H	X	X	Z	WRITE COMPLETED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated by the falling edge of $\overline{E}$ which latches the address information into the on chip registers. The write portion of the cycle is defined as both $\overline{E}$ and $\overline{W}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle provided that the write enable pulse setup time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $\overline{E}$ or $\overline{W}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$. By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed.

If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TELQX), a combination read write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH). The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method allow a minimum of one output disable time (TWLQZ) after $\overline{W}$ goes low before applying input data to the bus. This will insure that the output buffers are not active.

HM-6518

1024 x 1 CMOS RAM

Features

- HM-6100 COMPATIBLE
- LOW STANDBY POWER — 50 μW MAX
- LOW OPERATING POWER — 20mW/MHz MAX
- FAST ACCESS TIME — 180nsec MAX
- DATA RETENTION VOLTAGE — 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE - 2 TTL LOADS
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTER
- TWO CHIP SELECTS FOR EASY ARRAY EXPANSION
- THREE STATE OUTPUTS
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE

Description

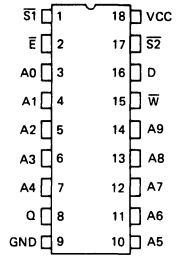
The HM-6518 is a 1024 by 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6518 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

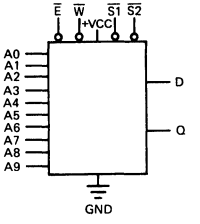
Pinout

TOP VIEW

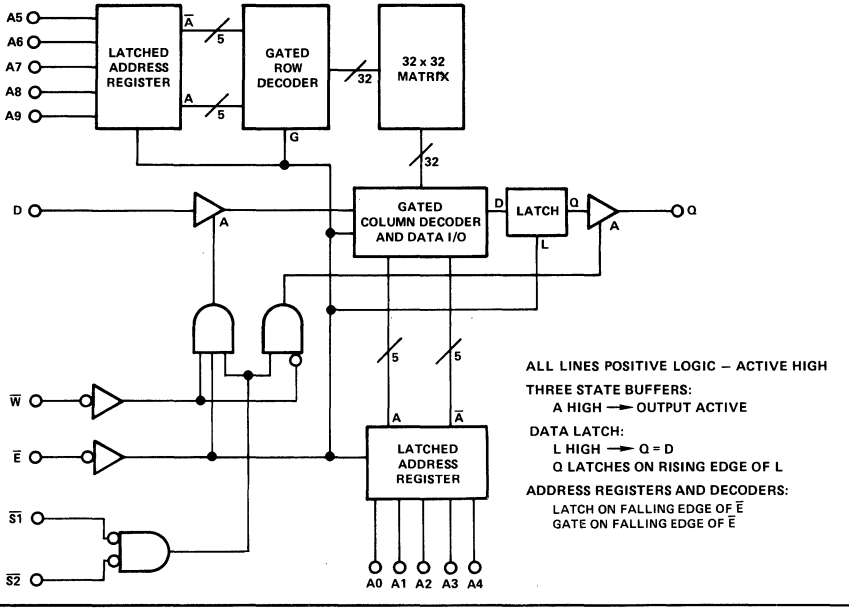


A - ADDRESS INPUT
E - CHIP ENABLE
S - CHIP SELECT
W - WRITE ENABLE
D - DATA INPUT
Q - DATA OUTPUT

Logic Symbol



Functional Diagram



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage - (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage -VCC	
		Military (-2)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Industrial (-9)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	-65°C to +150°C	Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	0.1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		5	0.01	μA	VCC = 2.0, IO = 0 VI = VCC or GND $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	6	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		180	100	ns	④
	TAVQV	Address Access Time		180	90	ns	④
	TSLQX	Chip Select Output Enable Time	20	120	40	ns	④
	TWLQX	Write Enable Output Disable Time		120	40	ns	④
	TSHQX	Chip Select Output Disable Time		120	40	ns	④
	TELEH	Chip Enable Pulse Negative Width	180		100	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
	TAVEL	Address Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	40		20	ns	④
	TDVWH	Data Setup Time	80		30	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLSH	Chip Select Write Pulse Setup Time	100		50	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	100		50	ns	④
	TSLWH	Chip Select Write Pulse Hold Time	100		50	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	100		50	ns	④
	TWLWH	Write Enable Pulse Width	100		50	ns	④
	TELEL	Read or Write Cycle Time	280		150	ns	④

NOTES
① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
④ AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -(VCC - GND)	-0.3V to +8.0V	Operating Supply Voltage -VCC	
		Military (-2)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (GND +0.3V)	Industrial (-9)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	-65°C to +150°C	Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	0.1	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10	0.01	µA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	$\overline{E}$ = VCC
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ⩽ VI ⩽ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	µA	GND ⩽ VO ⩽ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	6	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		250	110	ns	④
	TAVQV	Address Access Time		250	100	ns	④
	TSLQX	Chip Select Output Enable Time	20	160	60	ns	④
	TWLQX	Write Enable Output Disable Time		160	60	ns	④
	TSHQX	Chip Select Output Disable Time		160	60	ns	④
	TELEH	Chip Enable Pulse Negative Width	250		110	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
	TAVEL	Address Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	50		30	ns	④
	TDVWH	Data Setup Time	110		50	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLSH	Chip Select Write Pulse Setup Time	130		60	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	130		60	ns	④
	TSLWH	Chip Select Write Pulse Hold Time	130		60	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	130		60	ns	④
	TWLWH	Write Enable Pulse Width	130		60	ns	④
	TELEL	Read or Write Cycle Time	350		160	ns	④

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ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -(VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage -VCC Commercial	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)		
Storage Temperature	-65°C to +150°C	Operating Temperature Commercial	0°C to +70°C

ELECTRICAL CHARACTERISTICS

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	VCCDR	Data Retention Supply Voltage	2.0			V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.2mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	6	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300	160	ns	④
	TAVQV	Address Access Time		310	160	ns	④
	TSLQX	Chip Select Output Enable Time	20	200	60	ns	④
	TWLQX	Write Enable Output Disable Time		200	60	ns	④
	TSHQX	Chip Select Output Disable Time		200	60	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		160	ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		90	ns	④
	TAVEL	Address Setup Time	10		0	ns	④
	TELAX	Address Hold Time	50		30	ns	④
	TDVWH	Data Setup Time	130		80	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLSH	Chip Select Write Pulse Setup Time	160		100	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	160		100	ns	④
	TSLWH	Chip Select Write Pulse Hold Time	160		100	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	160		100	ns	④
	TWLWH	Write Enable Pulse Width	160		100	ns	④
	TELEL	Read or Write Cycle Time	450		250	ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
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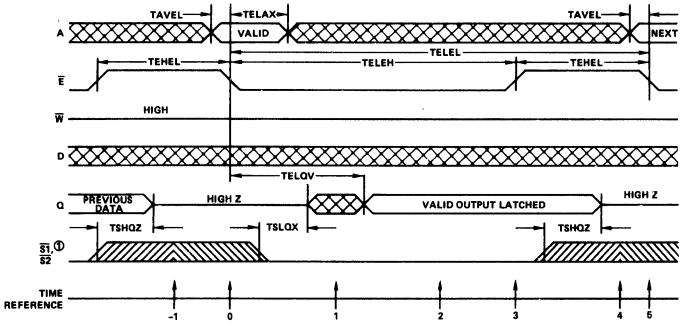
④ AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

Read Cycle



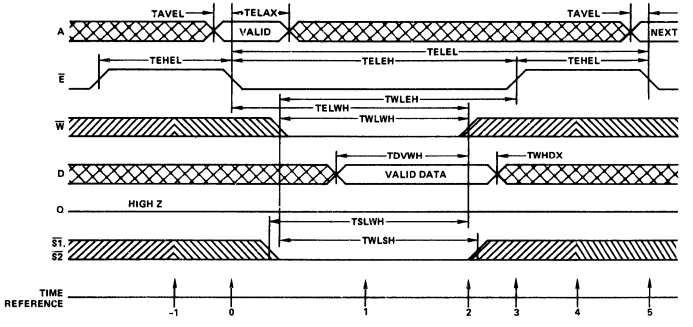
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S}$① $\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	H X	X	X	Z	MEMORY DISABLED
0	↘	X H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L H	X	X	X	OUTPUT ENABLED
2	L	L H	X	X	V	OUTPUT VALID
3	↗	L H	X	X	V	OUTPUT LATCHED
4	H	H X	X	X	Z	DEVICE DISABLED, PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTES: ① Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

In the HM-6518 read cycle the address information is latched into the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. In order for the output to be read $\overline{S1}$, $\overline{S2}$, and $\overline{E}$ must be low, $\overline{W}$ must be high. When $\overline{E}$ goes high the output data is latched into an on chip register. Taking either or both $\overline{S1}$ or $\overline{S2}$ high forces the output buffer to a high impedance state. The output data may be re-enabled at any time by taking $\overline{S1}$ and $\overline{S2}$ low. On the falling edge of $\overline{E}$ the data will be unlatched.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	$\overline{S}$①	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	X	Z	MEMORY DISABLED
0	↘	X	X	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	L	X	V	Z	WRITE MODE HAS BEGUN
2	L	↗	L	X	V	Z	DATA IS WRITTEN
3	↗	X	X	X	X	Z	WRITE COMPLETED
4	H	X	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	X	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTES: ① Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The write cycle is initiated by the falling edge of $\overline{E}$ which latches the address information into the on chip registers. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$, and $\overline{S2}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle provided that the write enable pulse set-up time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $\overline{E}$, $\overline{W}$, $\overline{S1}$ or $\overline{S2}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used data setup and hold times must be referenced to the rising edge of $\overline{E}$.

By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed. If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TSLQX), a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method allow a minimum of one output disable time (TWLQZ) after $\overline{W}$ goes low before applying input data to the bus. This will insure that the output buffers are not active.

HM-6551

256 x 4 CMOS RAM

Features

- LOW STANDBY POWER — 50 μW MAX
- LOW OPERATING POWER — 20mW/MHz MAX
- FAST ACCESS TIME — 220nsec MAX
- DATA RETENTION VOLTAGE — 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRVIE – 1 TTL LOAD
- INTERNAL LATCHED CHIP SELECT
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTERS
- LATCHED OUTPUTS
- THREE STATE OUTPUTS
- MILITARY AND INDUSTRIAL TEMPERATURE RANGES

Description

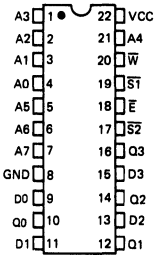
The HM-6551 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for addresses and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6551 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

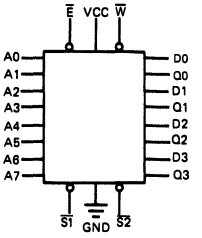
Pinout

TOP VIEW

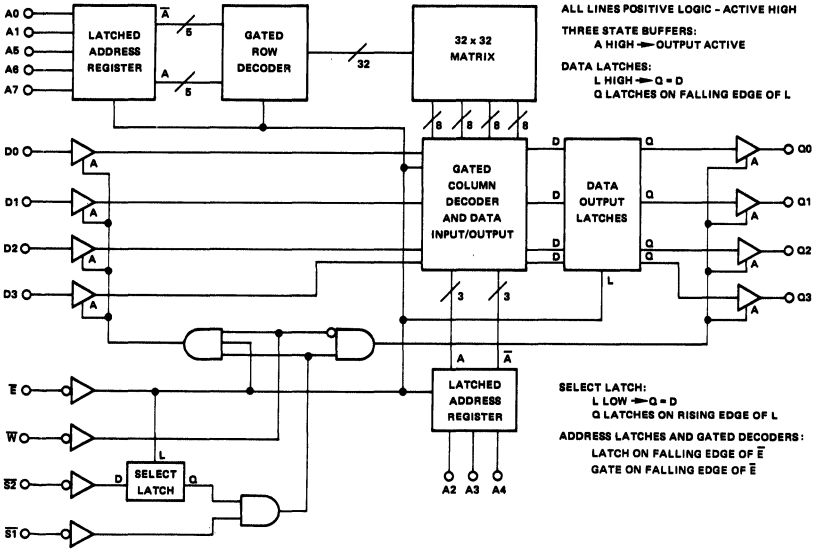


A – Address Input
E – Chip Enable
S – Chip Select
W – Write Enable
D – Data Input
Q – Data Output

Logic Symbol



Functional Diagram



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -(VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage -VCC	
Applied Input or Output Voltage	(GND -0.3V) to (GND +0.3V)	Military (-2)	4.5V to 5.5V
		Industrial (-9)	4.5V to 5.5V
Storage Temperature	-65°C to +150°C	Operating Temperature	
		Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	0.1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10	0.01	μA	$\overline{W}$ = GND VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	$\overline{E}$ = VCC
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	6	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		220	120	ns	④
	TAVQV	Address Access Time		220	110	ns	④
	TS1LQX	Chip Select 1 Output Enable Time	20	130	50	ns	④
	TWLQZ	Write Enable Output Disable Time		130	50	ns	④
	TS1HQZ	Chip Select 1 Output Disable Time		130	50	ns	④
	TELEH	Chip Enable Pulse Negative Width	220		120	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
	TAVEL	Address Setup Time	0		-10	ns	④
	TS2LEL	Chip Select 2 Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	40		20	ns	④
	TELS2X	Chip Select 2 Hold Time	40		20	ns	④
	TDVWH	Data Setup Time	100		50	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLS1H	Chip Select 1 Write Pulse Setup Time	120		60	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	120		60	ns	④
	TS1LWH	Chip Select 1 Write Pulse Hold Time	120		60	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	120		60	ns	④
	TWLWH	Write Enable Pulse Width	120		60	ns	④
	TELEL	Read or Write Cycle Time	320		170	ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
④ AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -(VCC - GND)	-0.3V to +8.0V	Operating Supply Voltage -VCC	
		Military (-2)	4.5V to 5.5V
Applied Input or Output Voltage	(GND -0.3V) to (VCC +0.3V)	Industrial (-9)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	-65°C to +150°C	Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
	ICCSB	Standby Supply Current		10	0.1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND $\overline{W}$ = GND
	ICCDR	Data Retention Supply Current		10	0.01	μA	VCC = 2.0, IO = 0 VI = VCC or GND $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
D.C.	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	6	pF	VO= VCC or GND f = 1MHz
	TELQV	Chip Enable Access Time		300	160	ns	④
	TAVQV	Address Access Time		300	150	ns	④
	TS1LQX	Chip Select 1 Output Enable Time	20	150	60	ns	④
	TWLQZ	Write Enable Output Disable Time		150	60	ns	④
	TS1HQZ	Chip Select 1 Output Disable Time		150	60	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		160	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
	TAVEL	Address Setup Time	0		-10	ns	④
A.C.	TS2LEL	Chip Select 2 Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	50		30	ns	④
	TELS2X	Chip Select 2 Hold Time	50		30	ns	④
	TDVWH	Data Setup Time	150		100	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLS1H	Chip Select 1 Write Pulse Setup Time	180		120	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	180		120	ns	④
	TS1LWH	Chip Select 1 Write Pulse Hold Time	180		120	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	180		120	ns	④
	TWLWH	Write Enable Pulse Width	180		120	ns	④
	TELEL	Read or Write Cycle Time	400		170	ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
④ AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

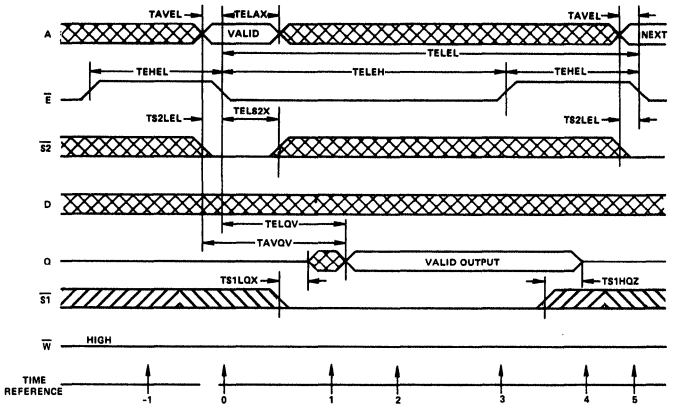
ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage - (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage -VCC Commercial	4.5V to 5.5V
Applied Input or Output Voltage	(GND -0.3V) to (GND +0.3V)		
Storage Temperature	-65°C to +150°C	Operating Temperature Commercial	0°C to +70°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100	10	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND $\overline{W}$ = GND
	ICCDR	Data Retention Supply Current		100	1.0	μA	VCC = 2.0, IO = 0 VI = VCC or GND $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.2mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	6	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350	200	ns	④
	TAVQV	Address Access Time		360	200	ns	④
	TS1LQX	Chip Select 1 Output Enable Time	20	180	80	ns	④
	TWLQZ	Write Enable Output Disable Time		180	80	ns	④
	TS1HQZ	Chip Select 1 Output Disable Time		180	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		200	ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		90	ns	④
	TAVEL	Address Setup Time	10		0	ns	④
	TS2LEL	Chip Select 2 Setup Time	10		0	ns	④
	TELAX	Address Hold Time	70		40	ns	④
	TELS2X	Chip Select 2 Hold Time	70		40	ns	④
	TDVWH	Data Setup Time	170		120	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLS1H	Chip Select 1 Write Pulse Setup Time	210		150	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	210		150	ns	④
	TS1LWH	Chip Select 1 Write Pulse Hold Time	210		150	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	210		150	ns	④
	TWLWH	Write Enable Pulse Width	210		150	ns	④
	TELEL	Read or Write Cycle Time	500		290	ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
④ AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

Read Cycle



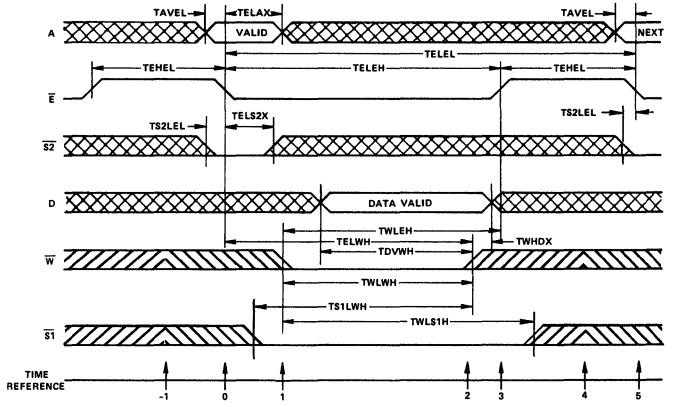
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	$\overline{S2}$	$\overline{W}$	A	D	OUTPUTS Q	FUNCTION
-1	H	H	X	X	X	X	Z	MEMORY DISABLED
0	↘	X	L	H	V	X	Z	ADDRESSES AND $\overline{S2}$ ARE LATCHED, CYCLE BEGINS
1	L	L	X	H	X	X	X	OUTPUT ENABLED BUT UNDEFINED
2	L	L	X	H	X	X	V	DATA OUTPUT VALID
3	↗	L	X	H	X	X	V	OUTPUTS LATCHED, VALID DATA, $\overline{S2}$ UNLATCHES
4	H	H	X	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	L	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The HM-6551 Read Cycle is initiated by the falling edge of $\overline{E}$. This signal latches the input address word and $\overline{S2}$ into on chip registers providing that minimum setup and hold times are met. After the required hold time, these inputs may change state without affecting device operation. $\overline{S2}$ acts as a high order address and simplifies decoding. For the output to be read, $\overline{E}$, $\overline{S1}$ must be low and $\overline{W}$ must be high. $\overline{S2}$ must have been latched low on the falling edge of $\overline{E}$. The output data will be valid at access time (TELQV).

The HM-6551 has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains in that state until $\overline{E}$ falls. Also on the rising edge of $\overline{E}$, $\overline{S2}$ unlatches and controls the outputs along with $\overline{S1}$. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS E	S1	S2	W	A	D	OUTPUTS Q	FUNCTION
-1	H	H	X	X	X	X	Z	MEMORY DISABLED
0	↘	X	L	X	V	X	Z	CYCLE BEGINS, ADDRESSES AND $\overline{S2}$ ARE LATCHED
1	L	L	X	↘	X	X	Z	WRITE PERIOD BEGINS
2	L	L	X	↗	X	V	Z	DATA IN IS WRITTEN
3	↗	X	X	H	X	X	Z	WRITE IS COMPLETED
4	H	H	X	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	L	X	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

In the Write Cycle the falling edge of $\overline{E}$ latches the addresses and $\overline{S2}$ into on chip registers. $\overline{S2}$ must be latched in the low state to enable the device. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$ being low and $\overline{S2}$ being latched low simultaneously. The $\overline{W}$ line may go low at any time during the cycle providing that the write pulse setup times (TWLEH and TWLS1H) are met. The write portion of the cycle is terminated on the first rising edge of either $\overline{E}$, $\overline{W}$, or $\overline{S1}$.

If a series of consecutive write cycles are to be executed, the $\overline{W}$ line may be held low until all desired locations have been written. If this method is used, data setup and hold times must be referenced to the first rising edge of $\overline{E}$ or $\overline{S1}$. By positioning the write pulse at different times within the $\overline{E}$ and $\overline{S1}$ low time (TELEH) various types of write cycles may be performed. If the $\overline{S1}$ low time (TS1LS1H) is greater than the $\overline{W}$ pulse plus an output enable time (TS1LQX), a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The HM-6551 may be used on a common I/O bus structure by tying the input and output pins together. The multiplexing is accomplished internally by the $\overline{W}$ line. In the write cycle, when $\overline{W}$ goes low, the output buffers are forced to a high impedance state. One output disable time delay (TWLQZ) must be allowed before applying input data to the bus.

HM-6561

256 x 4 CMOS RAM

Features

- HM-6100 COMPATIBLE
- LOW STANDBY POWER — 50μW MAX
- LOW OPERATING POWER — 20 mW/MHz MAX
- FAST ACCESS TIME — 220nsec MAX
- DATA RETENTION VOLTAGE — 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE – 1 TTL LOAD
- ON CHIP ADDRESS REGISTERS
- COMMON DATA IN/OUT
- THREE STATE OUTPUTS
- EASY MICROPROCESSOR INTERFACING
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE

Description

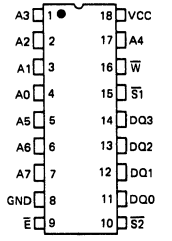
The HM-6561 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays. The data inputs and outputs are multiplexed internally for common I/O bus compatibility.

The HM-6561 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

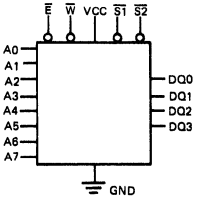
Pinout

TOP VIEW

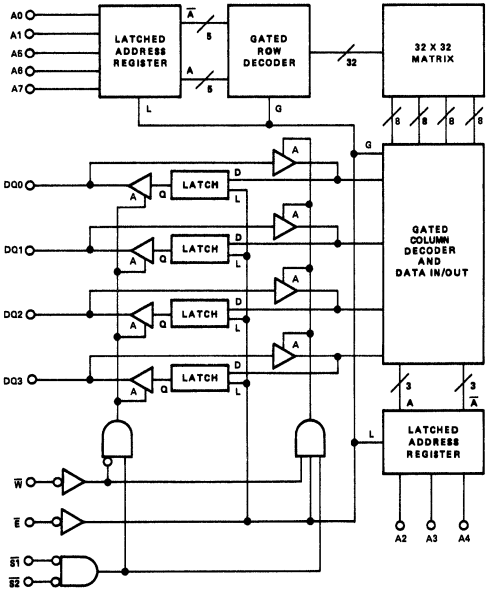


A – Address Input
E – Chip Enable
S – Chip Select
W – Write Enable
DQ – Data In/Out

Logic Symbol



Functional Diagram



ALL LINES POSITIVE LOGIC - ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

DATA LATCHES:
L HIGH → Q = D
Q LATCHES ON FALLING EDGE OF L

ADDRESS LATCHES AND GATED DECODERS:
LATCH ON FALLING EDGE OF E
GATE ON FALLING EDGE OF E

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage - (VCC - GND)	-0.3V to +8.0V	Operating Supply Voltage -VCC	
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Military (-2)	4.5V to 5.5V
		Industrial (-9)	4.5V to 5.5V
Storage Temperature	-65°C to +150°C	Operating Temperature	
		Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	0.1	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND $\overline{W}$ = GND
	ICCDR	Data Retention Supply Current		10	0.01	µA	VCC = 2.0, IO = 0 VI = VCC or GND $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤VIO≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10	6	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		220	120	ns	④
	TAVQV	Address Access Time		220	110	ns	④
	TSLQX	Chip Select Output Enable Time	20	120	50	ns	④
	TWLQZ	Write Enable Output Disable Time		120	50	ns	④
	TSHQZ	Chip Select Output Disable Time		120	50	ns	④
	TELEH	Chip Enable Pulse Negative Width	220		120	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
	TAVEL	Address Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	40		20	ns	④
	TDVWH	Data Setup Time	100		50	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLDV	Write Data Delay Time	120		50	ns	④
	TWLSH	Chip Select Write Pulse Setup Time	120		60	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	120		60	ns	④
	TSLWH	Chip Select Write Pulse Hold Time	120		60	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	120		60	ns	④
	TWLWH	Write Enable Pulse Width	120		60	ns	④
	TWLSL	Early Output High Z Time	0		-10	ns	④
	TSHWH	Late Output High Z Time	0		-10	ns	④
	TELEL	Read or Write Cycle Time	320		170	ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
④ AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -(VCC - GND)	-0.3V to +8.0V	Operating Supply Voltage -VCC	
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Military (-2)	4.5V to 5.5V
		Industrial (-9)	4.5V to 5.5V
Storage Temperature	-65°C to +150°C	Operating Temperature	
		Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	0.1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND $\overline{W}$ = GND
	ICCDR	Data Retention Supply Current		10	0.01	μA	VCC = 2.0, IO = 0 VI = VCC or GND $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10	6	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300	160	ns	④
	TAVQV	Address Access Time		300	150	ns	④
	TSLQX	Chip Select Output Enable Time	20	150	60	ns	④
	TWLQZ	Write Enable Output Disable Time		150	60	ns	④
	TSHQZ	Chip Select Output Disable Time		150	60	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		160	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
	TAVEL	Address Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	50		30	ns	④
	TDVWH	Data Setup Time	150		100	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLDV	Write Data Delay Time	150		60	ns	④
	TWLSH	Chip Select Write Pulse Setup Time	180		120	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	180		120	ns	④
	TSLWH	Chip Select Write Pulse Hold Time	180		120	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	180		120	ns	④
	TWLWH	Write Enable Pulse Width	180		120	ns	④
	TWLSL	Early Output High Z Time	0		-10	ns	④
	TSHWH	Late Output High Z Time	0		-10	ns	④
	TELEL	Read or Write Cycle Time	400		210	ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
④ AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

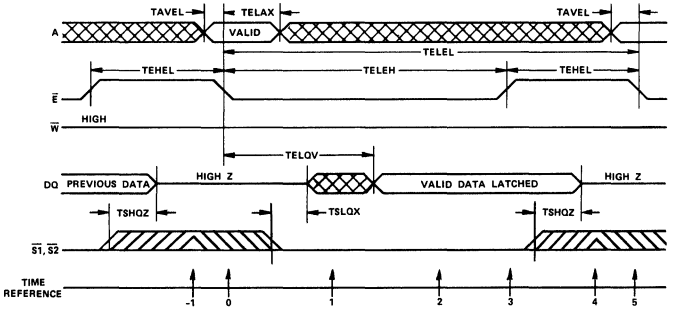
ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage - (VCC - GND)	-0.3V to +8.0V	Operating Supply Voltage -VCC Commercial	4.5V to 5.5V
Applied Input or Output Voltage	(GND -0.3V) to (VCC +0.3V)		
Storage Temperature	-65°C to +150°C	Operating Temperature Commercial	0°C to +70°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100	10	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND $\overline{W}$ = GND
	ICCDR	Data Retention Supply Current		100	1	μA	VCC = 2.0, IO = 0 VI = VCC or GND $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0			V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤VIO≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.2mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10	6	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350	200	ns	④
	TAVQV	Address Access Time		360	200	ns	④
	TSLQX	Chip Select Output Enable Time	20	180	80	ns	④
	TWLQZ	Write Enable Output Disable Time		180	80	ns	④
	TSHQZ	Chip Select Output Disable Time		180	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		200	ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		90	ns	④
	TAVEL	Address Setup Time	10		0	ns	④
	TELAX	Address Hold Time	70		40	ns	④
	TDVWH	Data Setup Time	170		120	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLDV	Write Data Delay Time	200		60	ns	④
	TWLSH	Chip Select Write Pulse Setup Time	210		150	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	210		150	ns	④
	TSLWH	Chip Select Write Pulse Hold Time	210		150	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	210		150	ns	④
	TWLWH	Write Enable Pulse Width	210		150	ns	④
	TWLSL	Early Output High Z Time	0		-10	ns	④
	TSHWH	Late Output High Z Time	0		-10	ns	④
	TELEL	Read or Write Cycle Time	500		290	ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
④ AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

Read Cycle



TRUTH TABLE

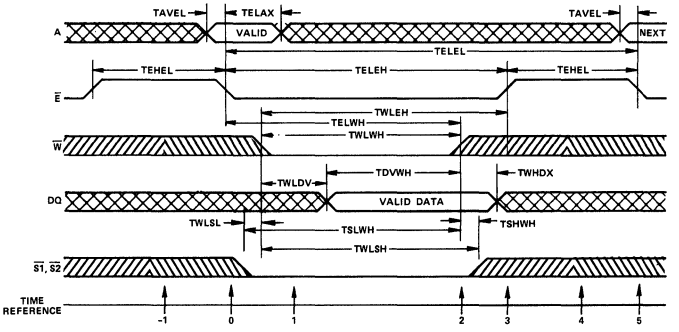
TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	$\overline{W}$	A	OUTPUT DQ	FUNCTION
-1	H	H	X	X	Z	MEMORY DISABLED
0	↘	X	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	H	X	X	OUTPUT ENABLED
2	L	L	H	X	V	OUTPUT VALID
3	↗	L	H	X	V	OUTPUT LATCHED
4	H	H	X	X	Z	DEVICE DISABLED, PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTES: 1) Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The HM-6561 Read Cycle is initiated on the falling edge of $\overline{E}$. This signal latches the input address word into on chip registers. Minimum address setup and hold times must be met. After the required hold time, the address lines may change state without affecting device operation. In order to read the output data $\overline{E}$, $\overline{S1}$ and $\overline{S2}$ must be low and $\overline{W}$ must be high. The output data will be valid at access time (TELQV).

The HM-6561 has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains latched until $\overline{E}$ falls. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	$\overline{W}$	A	DQ	FUNCTION
-1	H	H	X	X	X	MEMORY DISABLED
0	↘	X	X	V	X	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	L	X	X	WRITE PERIOD BEGINS
2	L	L	↗	X	V	DATA IN IS WRITTEN
3	↗	X	H	X	X	WRITE IS COMPLETED
4	H	H	X	X	X	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	X	V	X	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTES: 1) Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The write cycle begins with the $\overline{E}$ falling edge latching the address. The write portion of the cycle is defined by $\overline{E}$, $\overline{S1}$, $\overline{S2}$ and $\overline{W}$ all being low simultaneously. The write portion of the cycle is terminated by the first rising edge of any control line, $\overline{E}$, $\overline{S1}$, $\overline{S2}$ or $\overline{W}$. The data setup and data hold times (TDVWH and TWHDX) must be referenced to the terminating signal. For example, if $\overline{S2}$ rises first, data setup and hold times become TDVS2H and TS2HDX; and are numerically equal to TDVWH and TWHDX.

Data input/output multiplexing is controlled by $\overline{W}$. Care must be taken to avoid data bus conflicts, where the RAM outputs become enabled when another device is driving the data inputs. The following two examples illustrate the timing required to avoid bus conflicts.

Case 1: Both $\overline{S1}$ and $\overline{S2}$ fall before $\overline{W}$ falls.

If both selects fall before $\overline{W}$ falls, the RAM outputs will become enabled. $\overline{W}$ is used to disable the outputs, so a disable time (TWLQZ = TWLDV) must pass before any other device can begin to drive the data inputs. This method of operation requires a wider write pulse, because TWLDV + TDVWH is greater than TWLWH. In this case TWLSL and TSHWH are meaningless and can be ignored.

Case 2: $\overline{W}$ falls before both $\overline{S1}$ and $\overline{S2}$ fall.

If one or both selects are high until $\overline{W}$ falls the outputs are guaranteed not to enable at the beginning of the cycle. This eliminates the concern for data bus conflicts and simplifies data input timing. Data input may be applied as early as convenient, and TWLDV is ignored. Since $\overline{W}$ is not used to disable the outputs it can be shorter than in case 1; TWLWH is the minimum write pulse. At the end of the write period, if $\overline{W}$ rises before either select the outputs will enable, reading the data just written. They will not disable until either select goes high (TSHQZ).

	IF	OBSERVE	IGNORE
Case 1	Both $\overline{S1}$ and $\overline{S2}$ = low before $\overline{W}$ = low	TWLQZ TWLDV TDVWH	TWLWH TWLSL TSHWH
Case 2	$\overline{W}$ = low before both $\overline{S1}$ and $\overline{S2}$ = low	TWLWH TDVWH TWLSL TSHWH	TWLQZ TWLDV

If a series of consecutive write cycles are to be performed, $\overline{W}$ may remain low until all desired locations are written. This is an extension of Case 2.

Read-Modify-Write cycles and Read-Write-Read cycles can be performed (extension of Case 1). In fact, data may be modified as many times as desired with $\overline{E}$ remaining low.

HM-6504

4096 x 1 CMOS RAM

Features

- LOW POWER STANDBY — 125 μW MAX.
- LOW POWER OPERATION — 35mW/MHz MAX.
- EXTREMELY LOW SPEED-POWER PRODUCT
- DATA RETENTION — @ 2.0V MIN.
- TTL COMPATIBLE INPUT/OUTPUT
- THREE-STATE OUTPUT
- STANDARD JEDEC PINOUT
- FAST ACCESS TIME — 120/200nsec MAX.
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER
- GATED INPUTS-NO PULL UP OR PULL DOWN RESISTORS REQUIRED

Description

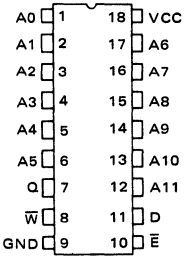
The HM-6504 is a 4096 x 1 static CMOS RAM fabricated using self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance for use in expanded memory arrays. Gated inputs allow lower operating current and also eliminates the need for pull-up or pull-down resistors. The HM-6504 is a fully static RAM and may be maintained in any state for an indefinite period of time.

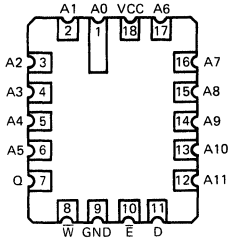
Data retention supply voltage and supply current are guaranteed over temperature.

Pinouts

TOP VIEW

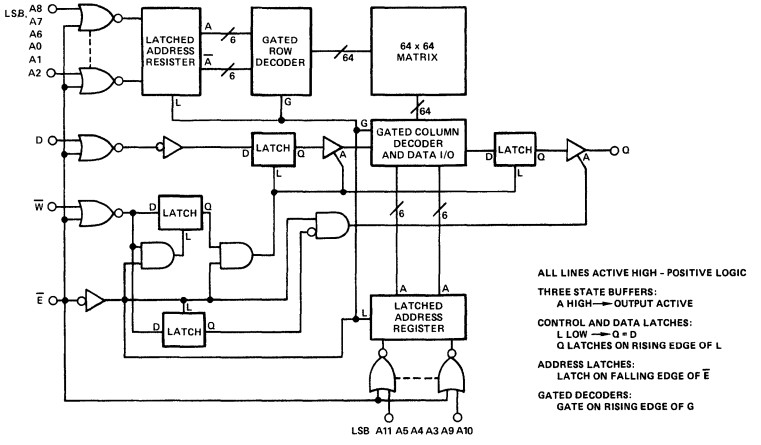


TOP VIEW



A — Address Input
$\overline{E}$ — Chip Enable
$\overline{W}$ — Write Enable
D — Data Input
Q — Data Output

Functional Diagram



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS *

Supply Voltage – (VCC -GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage Military (-2)	4.5V to 5.5V
Operating Temperature Military (-2)	-55°C to +125°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS PRELIMINARY

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	5.0	µA	IO = 0 $\overline{E}$ = VCC –0.3V
	ICCOP	Operating Supply Current (2)		7	5	mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		25	3.0	µA	IO = 0, VCC = 2.0V $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance (3)		10.0	6.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		120		ns	(4)
	TAVQV	Address Access Time		120		ns	(4)
	TELQX	Chip Enable Output Enable Time	10			ns	(4)
	TEHQZ	Chip Enable Output Disable Time		50		ns	(4) (5)
	TELEH	Chip Enable Pulse Negative Width	120			ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	50			ns	(4)
	TAVEL	Address Setup Time	0			ns	(4)
	TELAX	Address Hold Time	40			ns	(4)
	TWLWH	Write Enable Pulse Width	20			ns	(4)
	TWLEH	Write Enable Pulse Setup Time	70			ns	(4)
	TWLEL	Early Write Pulse Setup Time	0			ns	(4)
	TWHEL	Write Enable Read Mode Setup Time	0			ns	(4)
	TELWH	Early Write Pulse Hold Time	40			ns	(4)
	TDVWL	Data Setup Time	0			ns	(4)
	TDVEL	Early Write Data Setup Time	0			ns	(4)
	TWLDX	Data Hold Time	25			ns	(4)
	TELDX	Early Write Data Hold Time	25			ns	(4)
	TQVWL	Data Valid to Write Time	0			ns	(4)
	TELEL	Read or Write Cycle Time	170			ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC Test Conditions: Inputs – TRISE = TFALL = 5 nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
(5) This parameter is guaranteed and not tested.

ABSOLUTE MAXIMUM RATINGS *		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Industrial (-9)	4.5V to 5.5V
Storage Temperature	-65°C to +150°C	Operating Temperature	
		Industrial (-9)	-40°C to +85°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS PRELIMINARY

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		25	3.0	µA	$\overline{E}$ = VCC –0.3V
	ICCOP	Operating Supply Current (2)		7	5	mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		15	2.0	µA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance (3)		10.0	6.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		120		ns	(4)
	TAVQV	Address Access Time		120		ns	(4)
	TELQX	Chip Enable Output Enable Time	10			ns	(4)
	TEHQZ	Chip Enable Output Disable Time		50		ns	(4) (5)
	TELEH	Chip Enable Pulse Negative Width	120			ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	50			ns	(4)
	TAVEL	Address Setup Time	0			ns	(4)
	TELAX	Address Hold Time	40			ns	(4)
	TWLWH	Write Enable Pulse Width	20			ns	(4)
	TWLEH	Write Enable Pulse Setup Time	70			ns	(4)
	TWLEL	Early Write Pulse Setup Time	0			ns	(4)
	TWHEL	Write Enable Read Mode Setup Time	0			ns	(4)
	TELWH	Early Write Pulse Hold Time	40			ns	(4)
	TDVWL	Data Setup Time	0			ns	(4)
	TDVEL	Early Write Data Setup Time	0			ns	(4)
	TWLDX	Data Hold Time	25			ns	(4)
	TELDX	Early Write Data Hold Time	25			ns	(4)
	TQVWL	Data Valid to Write Time	0			ns	(4)
	TELEL	Read or Write Cycle Time	170			ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room temp., 5 volt data provided for information,– not guaranteed
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC Test Conditions: Inputs – TRISE = TFALL = 5 nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
(5) This parameter is guaranteed and not tested.

ABSOLUTE MAXIMUM RATINGS *		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage Military (-2)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)		
Storage Temperature	-65°C to +150°C	Operating Temperature Military (-2)	-55°C to +125°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	5.0	μA	IO = 0 $\overline{E}$ = VCC –0.3V
	ICCOP	Operating Supply Current (2)		7	5	mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		25	3.0	μA	VCC = 2.0 V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance (3)		10.0	6.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		200		ns	(4)
	TAVQV	Address Access Time		220		ns	(4)
	TELQX	Chip Enable Output Enable Time	20			ns	(4)
	TEHQZ	Chip Enable Output Disable Time		80		ns	(4) (5)
	TELEH	Chip Enable Pulse Negative Width	200			ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	90			ns	(4)
	TAVEL	Address Setup Time	20			ns	(4)
	TELAX	Address Hold Time	50			ns	(4)
	TWLWH	Write Enable Pulse Width	60			ns	(4)
	TWLEH	Write Enable Pulse Setup Time	150			ns	(4)
	TWLEL	Early Write Pulse Setup Time	0			ns	(4)
	TWHEL	Write Enable Read Mode Setup Time	0			ns	(4)
	TELWH	Early Write Pulse Hold Time	60			ns	(4)
	TDVWL	Data Setup Time	0			ns	(4)
	TDVEL	Early Write Data Setup Time	0			ns	(4)
	TWLDX	Data Hold Time	60			ns	(4)
	TELDX	Early Write Data Hold Time	60			ns	(4)
	TQVWL	Data Valid to Write Time	0			ns	(4)
	TELEL	Read or Write Cycle Time	290			ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room temp., 5 volt data provided for information.– not guaranteed
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC Test Conditions: Inputs – TRISE = TFALL = 10ns; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
(5) This parameter is guaranteed and not tested.

ABSOLUTE MAXIMUM RATINGS *		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage Industrial (-9)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Operating Temperature Industrial (-9)	-40°C to +85°C
Storage Temperature	-65°C to +150°C		

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		25	3.0	µA	IO = 0 $\overline{E}$ = VCC –0.3V
	ICCOP	Operating Supply Current ②		7	5	mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		15	2.0	µA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance ③		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance ③		10.0	6.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		200		ns	④
	TAVQV	Address Access Time		220		ns	④
	TELQX	Chip Enable Output Enable Time	20			ns	④
	TEHQZ	Chip Enable Output Disable Time		80		ns	④⑤
	TELEH	Chip Enable Pulse Negative Width	200			ns	④
	TEHEL	Chip Enable Pulse Positive Width	90			ns	④
	TAVEL	Address Setup Time	20			ns	④
	TELAX	Address Hold Time	50			ns	④
	TWLWH	Write Enable Pulse Width	60			ns	④
	TWLEH	Write Enable Pulse Setup Time	150			ns	④
	TWLEL	Early Write Pulse Setup Time	0			ns	④
	TWHEL	Write Enable Read Mode Setup Time	0			ns	④
	TELWH	Early Write Pulse Hold Time	60			ns	④
	TDVWL	Data Setup Time	0			ns	④
	TDVEL	Early Write Data Setup Time	0			ns	④
	TWLDX	Data Hold Time	60			ns	④
	TELDX	Early Write Data Hold Time	60			ns	④
	TQVWL	Data Valid to Write Time	0			ns	④
	TELEL	Read or Write Cycle Time	290			ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information.– not guaranteed
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
③ Capacitance sampled and guaranteed – not 100% tested.
④ AC Test Conditions: Inputs – TRISE = TFALL = 10nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
⑤ This parameter is guaranteed and not tested.

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage Military (-2)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Operating Temperature Military (-2)	-55°C to +125°C
Storage Temperature	-65°C to +150°C		

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	5.0	μA	IO = 0 $\overline{E}$ = VCC-0.3V
	ICCOP	Operating Supply Current (2)		7	5	mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		25	3.0	μA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance (3)		10.0	6.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		300		ns	(4)
	TAVQV	Address Access Time		320		ns	(4)
	TELQX	Chip Enable Output Enable Time	20			ns	(4)
	TEHQZ	Chip Enable Output Disable Time		100		ns	(4) (5)
	TELEH	Chip Enable Pulse Negative Width	300			ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	120			ns	(4)
	TAVEL	Address Setup Time	20			ns	(4)
	TELAX	Address Hold Time	50			ns	(4)
	TWLWH	Write Enable Pulse Width	80			ns	(4)
	TWLEH	Write Enable Pulse Setup Time	200			ns	(4)
	TWLEL	Early Write Pulse Setup Time	0			ns	(4)
	TWHEL	Write Enable Read Mode Setup Time	0			ns	(4)
	TELWH	Early Write Pulse Hold Time	80			ns	(4)
	TDVWL	Data Setup Time	0			ns	(4)
	TDVEL	Early Write Data Setup Time	0			ns	(4)
	TWLDX	Data Hold Time	80			ns	(4)
	TELDX	Early Write Data Hold Time	80			ns	(4)
	TQVWL	Data Valid to Write Time	0			ns	(4)
	TELEL	Read or Write Cycle Time	420			ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room temp., 5 volt data provided for information.– not guaranteed
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC Test Conditions: Inputs – TRISE = TFALL = 10nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
(5) This parameter is guaranteed and not tested.

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage Industrial (-9)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)		
Storage Temperature	-65°C to +150°C	Operating Temperature Industrial (-9)	-40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		25	3.0	μA	IO = 0, $\overline{E}$ = VCC-0.3V
	ICCOP	Operating Supply Current (2)		7	5	mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		15	2.0	μA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance (3)		10.0	6.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		300		ns	(4)
	TAVQV	Address Access Time		320		ns	(4)
	TELQX	Chip Enable Output Enable Time	20			ns	(4)
	TEHQZ	Chip Enable Output Disable Time		100		ns	(4)(5)
	TELEH	Chip Enable Pulse Negative Width	300			ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	120			ns	(4)
	TAVEL	Address Setup Time	20			ns	(4)
	TELAX	Address Hold Time	50			ns	(4)
	TWLWH	Write Enable Pulse Width	80			ns	(4)
	TWLEH	Write Enable Pulse Setup Time	200			ns	(4)
	TWLEL	Early Write Pulse Setup Time	0			ns	(4)
	TWHEL	Write Enable Read Mode Setup Time	0			ns	(4)
	TELWH	Early Write Pulse Hold Time	80			ns	(4)
	TDVWL	Data Setup Time	0			ns	(4)
	TDVEL	Early Write Data Setup Time	0			ns	(4)
	TWLDX	Data Hold Time	80			ns	(4)
	TELDX	Early Write Data Hold Time	80			ns	(4)
	TQVWL	Data Valid to Write Time	0			ns	(4)
	TELEL	Read or Write Cycle Time	420			ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room temp., 5 volt data provided for information.– not guaranteed
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC Test Conditions: Inputs – TRISE = TFALL = 10nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
(5) This parameter is guaranteed and not tested.

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage Industrial (-9)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)		
Storage Temperature	-65°C to +150°C	Operating Temperature Industrial (-9)	-40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100	20	µA	IO = 0 $\overline{E}$ = VCC-0.3V
	ICCOP	Operating Supply Current (2)		7	5	mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		50	12	µA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance (3)		10.0	6.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		300		ns	(4)
	TAVQV	Address Access Time		320		ns	(4)
	TELQX	Chip Enable Output Enable Time	20			ns	(4)
	TEHQZ	Chip Enable Output Disable Time		100		ns	(4)(5)
	TELEH	Chip Enable Pulse Negative Width	300			ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	120			ns	(4)
	TAVEL	Address Setup Time	20			ns	(4)
	TELAX	Address Hold Time	50			ns	(4)
	TWLWH	Write Enable Pulse Width	80			ns	(4)
	TWLEH	Write Enable Pulse Setup Time	200			ns	(4)
	TWLEL	Early Write Pulse Setup Time	0			ns	(4)
	TWHEL	Write Enable Read Mode Setup Time	0			ns	(4)
	TELWH	Early Write Pulse Hold Time	80			ns	(4)
	TDVWL	Data Setup Time	0			ns	(4)
	TDVEL	Early Write Data Setup Time	0			ns	(4)
	TWLDX	Data Hold Time	80			ns	(4)
	TELDX	Early Write Data Hold Time	80			ns	(4)
	TQVWL	Data Valid to Write Time	0			ns	(4)
	TELEL	Read or Write Cycle Time	420			ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC Test Conditions: Inputs – TRISE = TFALL = 10nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
(5) This parameter is guaranteed and not tested.

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage Commercial	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)		
Storage Temperature	-65°C to +150°C	Operating Temperature Commercial	0°C to +70°C

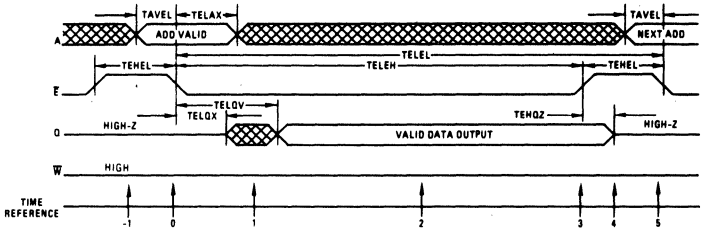
**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		350	50	µA	IO = 0, $\overline{E}$ = VCC-0.3V
	ICCOP	Operating Supply Current (2)		7	5	mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		200	30	µA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-10.0	+10.0	±0.5	µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-10.0	+10.0	±0.5	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance (3)		10.0	6.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		350		ns	(4)
	TAVQV	Address Access Time		370		ns	(4)
	TELQX	Chip Enable Output Enable Time	20			ns	(4)
	TEHQZ	Chip Enable Output Disable Time		100		ns	(4) (5)
	TELEH	Chip Enable Pulse Negative Width	350			ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	150			ns	(4)
	TAVEL	Address Setup Time	20			ns	(4)
	TELAX	Address Hold Time	50			ns	(4)
	TWLWH	Write Enable Pulse Width	100			ns	(4)
	TWLEH	Write Enable Pulse Setup Time	250			ns	(4)
	TWLEL	Early Write Pulse Setup Time	0			ns	(4)
	TWHEL	Write Enable Read Mode Setup Time	0			ns	(4)
	TELWH	Early Write Pulse Hold Time	100			ns	(4)
	TDVWL	Data Setup Time	30			ns	(4)
	TDVEL	Early Write Data Setup Time	30			ns	(4)
	TWLDX	Data Hold Time	100			ns	(4)
	TELDX	Early Write Data Hold Time	100			ns	(4)
	TQVWL	Data Valid to Write Time	0			ns	(4)
	TELEL	Read or Write Cycle Time	500			ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC Test Conditions: Inputs – TRISE = TFALL = 10nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
(5) This parameter is guaranteed and not tested.

Read Cycle

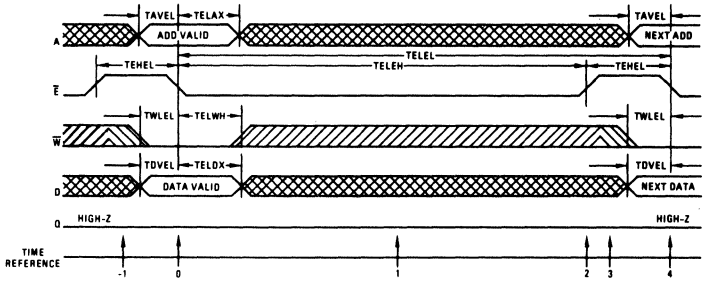


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	OUTPUT Q	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and all inputs and ready the RAM for the next memory cycle (T = 4).

Early Write Cycle

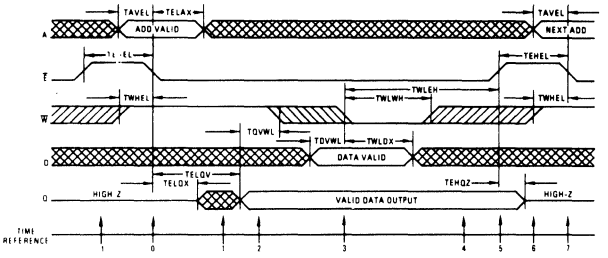


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	L	V	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	X	X	X	Z	WRITE IN PROGRESS INTERNALLY
2	↗	X	X	X	Z	WRITE COMPLETED
3	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
4	↘	L	V	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls determines the state of the output buffer for that cycle. Since $\overline{W}$ is low when $\overline{E}$ falls, the output buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; therefore data set up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state the output buffer and all inputs are disabled and all signals are unlatched. The device is now ready for the next cycle.

Read Modify Write Cycle

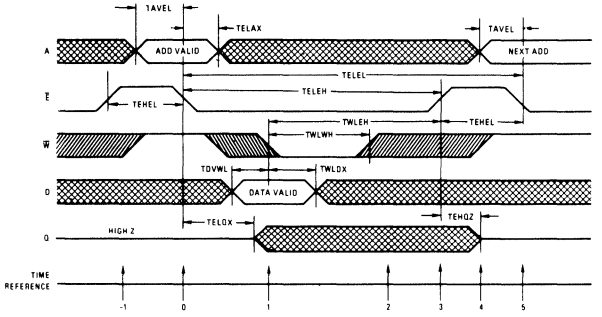


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	V	X	Z	CYCLE BEGINS, ADDRESS ARE LATCHED
1	L	H	X	X	X	OUTPUT ENABLED
2	L	H	X	X	V	OUTPUT VALID, READ AND MODIFY TIME
3	L	↘	X	V	V	WRITE BEGINS, DATA IS LATCHED
4	L	X	X	X	V	WRITE IN PROGRESS INTERNALLY
5	↗	X	X	X	V	WRITE COMPLETED
6	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↘	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The read modify write cycle begins as all other cycles on the falling edge of $\overline{E}$ (T = 0). The $\overline{W}$ line should be high at (T = 0) in order to latch the output buffers in the active state. During (T = 1) the output will be active but not valid until (T = 2). On the falling edge of the $\overline{W}$ (T = 3) the data present at the output and input are latched. The $\overline{W}$ signal also latches itself on its low going edge. All input signals excluding $\overline{E}$ have been latched and have no further effect on the RAM. The rising edge of $\overline{E}$ (T = 5) completes the write portion of the cycle and unlatches and disables all inputs and output. The output goes to a high impedance and the RAM is ready for the next cycle.

Late Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	↘	X	V	X	WRITE BEGINS, DATA IS LATCHED
2	L	H	X	X	X	WRITE IN PROGRESS INTERNALLY
3	↗	H	X	X	X	WRITE COMPLETED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The late write cycle is a cross between the early write cycle and the read-modify-write cycle.

Recall that in the early write the output is guaranteed to remain high impedance, and in the read-modify-write the output is guaranteed valid at access time. The late write is between these two cases. With this cycle the output may become active, and may become valid data, or may remain active but undefined. Valid data is written into the RAM if data setup, data hold, write setup and write pulse widths are observed.

HARRIS

HM-6514

1024 x 4 CMOS RAM

Features

- LOW POWER STANDBY — **125µW MAX.**
- LOW POWER OPERATION — **35mW/MHz MAX.**
- DATA RETENTION — **@ 2.0V MIN.**
- TTL COMPATIBLE INPUT/OUTPUT
- COMMON DATA IN/OUT
- THREE-STATE OUTPUTS
- STANDARD JEDEC PINOUT
- FAST ACCESS TIME — **120 /200nsec MAX.**
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON-CHIP ADDRESS REGISTER
- GATED INPUTS—NO PULL UP OR PULL DOWN RESISTORS REQUIRED

Description

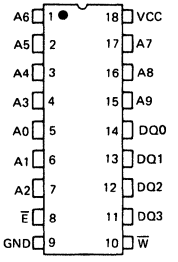
The HM-6514 is a 1024 x 4 static CMOS RAM fabricated using self aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On-chip latches are provided for the addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory systems. Gated inputs allow low operating current and also eliminates the need for pull-up or pulldown resistors.

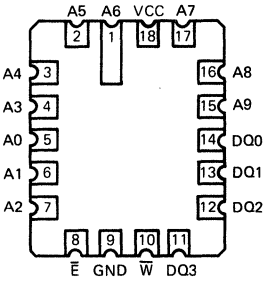
The HM-6514 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Pinouts

TOP VIEW

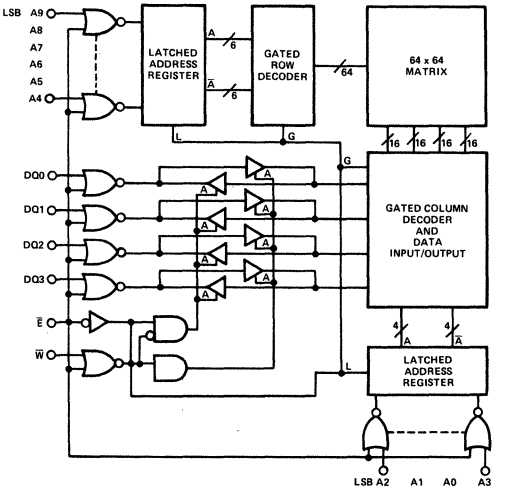


TOP VIEW



A — Address Input
E — Chip Enable
W — Write Enable
DQ — Data In/Out

Functional Diagram



ALL LINES ACTIVE HIGH - POSITIVE LOGIC

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

ADDRESS LATCHES:
LATCH ON FALLING EDGE OF E

GATED DECODERS:
GATE ON RISING EDGE OF G

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS *		OPERATING RANGE	
Supply Voltage - (VCC - GND)	-0.3V to +8.0V	Operating Supply Voltage Military (-2)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Operating Temperature Military (-2)	-55°C to +125°C
Storage Temperature	-65°C to +150°C		

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS — PRELIMINARY

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	5.0	µA	$\overline{IO}$ = 0 $\overline{E}$ = VCC −0.3V
	ICCOP	Operating Supply Current (2)		7	5	mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		25	3.0	µA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance (3)		10.0	6.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		120		ns	(4)
	TAVQV	Address Access Time		120		ns	(4)
	TELQX	Chip Enable Output Enable Time	10			ns	(4)
	TWLQZ	Write Enable Output Disable Time		50		ns	(4) (5)
	TEHQZ	Chip Enable Output Disable Time		50		ns	(4) (5)
	TELEH	Chip Enable Pulse Negative Width	120			ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	50			ns	(4)
	TAVEL	Address Setup Time	0			ns	(4)
	TELAX	Address Hold Time	40			ns	(4)
	TWLWH	Write Enable Pulse Width	120			ns	(4)
	TWLEH	Write Enable Pulse Setup Time	120			ns	(4)
	TELWH	Write Enable Pulse Hold Time	120			ns	(4)
	TDVWH	Data Setup Time	50			ns	(4)
	TWHDX	Data Hold Time	0			ns	(4)
	TWLDV	Write Data Delay Time	70			ns	(4)
	TWLEL	Early Output High-Z Time	0			ns	(4)
	TEHWH	Late Output High-Z Time	0			ns	(4)
	TELEL	Read or Write Cycle Time	170			ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room Temp., 5V data provided for information — not guaranteed
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Ex: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed — not 100% tested.
(4) AC test conditions: Inputs — TRISE = TFALL = 5ns; Output — CLOAD = 50pF. All timing measured at 1.5V reference level.
(5) This parameter is guaranteed and not tested.

ABSOLUTE MAXIMUM RATINGS *

Supply Voltage - (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage Industrial (-9)	4.5V to 5.5V
Operating Temperature Industrial (-9)	-40°C to +85°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS — PRELIMINARY

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		25	3.0	µA	$\overline{E}$ = VCC −0.3V
	ICCOP	Operating Supply Current (2)		7	5	mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		15	2.0	µA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance (3)		10.0	6.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		120		ns	(4)
	TAVQV	Address Access Time		120		ns	(4)
	TELQX	Chip Enable Output Enable Time	10			ns	(4)
	TWLQZ	Write Enable Output Disable Time		50		ns	(4) (5)
	TEHQZ	Chip Enable Output Disable Time		50		ns	(4) (5)
	TELEH	Chip Enable Pulse Negative Width	120			ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	50			ns	(4)
	TAVEL	Address Setup Time	0			ns	(4)
	TELAX	Address Hold Time	40			ns	(4)
	TWLWH	Write Enable Pulse Width	120			ns	(4)
	TWLEH	Write Enable Pulse Setup Time	120			ns	(4)
	TELWH	Write Enable Pulse Hold Time	120			ns	(4)
	TDVWH	Data Setup Time	50			ns	(4)
	TWHDX	Data Hold Time	0			ns	(4)
	TWLDV	Write Data Delay Time	70			ns	(4)
	TWLEL	Early Output High-Z Time	0			ns	(4)
	TEHWH	Late Output High-Z Time	0			ns	(4)
	TELEL	Read or Write Cycle Time	170			ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room Temp., 5V data provided for information — not guaranteed
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Ex: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed — not 100% tested.
(4) AC test conditions: Inputs — TRISE = TFALL = 5ns; Output — CLOAD = 50pF. All timing measured at 1.5V reference level.
(5) This parameter is guaranteed and not tested.

ABSOLUTE MAXIMUM RATINGS *		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage Military (-2)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)		
Storage Temperature	-65°C to +150°C	Operating Temperature Military (-2)	-55°C to +125°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	5.0	µA	IO = 0 $\overline{E}$ = VCC –0.3V
	ICCOP	Operating Supply Current (2)		7	5	mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		25	3.0	µA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance (3)		10.0	6.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		200		ns	(4)
	TAVQV	Address Access Time		220		ns	(4)
	TELQX	Chip Enable Output Enable Time	20			ns	(4)
	TWLQZ	Write Enable Output Disable Time		80		ns	(4) (5)
	TEHQZ	Chip Enable Output Disable Time		80		ns	(4) (5)
	TELEH	Chip Enable Pulse Negative Width	200			ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	90			ns	(4)
	TAVEL	Address Setup Time	20			ns	(4)
	TELAX	Address Hold Time	50			ns	(4)
	TWLWH	Write Enable Pulse Width	200			ns	(4)
	TWLEH	Write Enable Pulse Setup Time	200			ns	(4)
	TELWH	Write Enable Pulse Hold Time	200			ns	(4)
	TDVWH	Data Setup Time	120			ns	(4)
	TWHDX	Data Hold Time	0			ns	(4)
	TWLDV	Write Data Delay Time	80			ns	(4)
	TWLEL	Early Output High-Z Time	0			ns	(4)
	TEHWH	Late Output High-Z Time	0			ns	(4)
	TELEL	Read or Write Cycle Time	290			ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room Temp., 5V data provided for information – not guaranteed
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Ex: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC test conditions: Inputs – TRISE = TFALL = 10ns; Output – CLOAD = 50pF. All timing measured at 1.5V reference level.
(5) This parameter is guaranteed and not tested.

ABSOLUTE MAXIMUM RATINGS *		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Industrial (-9)	4.5V to 5.5V
Storage Temperature	-65°C to +150°C	Operating Temperature	
		Industrial (-9)	-40°C to +85°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
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	ICCOP	Operating Supply Current (2)		7	5	mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		15	2.0	µA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance (3)		10.0	6.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		200		ns	(4)
	TAVQV	Address Access Time		220		ns	(4)
	TELQX	Chip Enable Output Enable Time	20			ns	(4)
	TWLQZ	Write Enable Output Disable Time		80		ns	(4) (5)
	TEHQZ	Chip Enable Output Disable Time		80		ns	(4) (5)
	TELEH	Chip Enable Pulse Negative Width	200			ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	90			ns	(4)
	TAVEL	Address Setup Time	20			ns	(4)
	TELAX	Address Hold Time	50			ns	(4)
	TWLWH	Write Enable Pulse Width	200			ns	(4)
	TWLEH	Write Enable Pulse Setup Time	200			ns	(4)
	TELWH	Write Enable Pulse Hold Time	200			ns	(4)
	TDVWH	Data Setup Time	120			ns	(4)
	TWHDX	Data Hold Time	0			ns	(4)
	TWLDV	Write Data Delay Time	80			ns	(4)
	TWLEL	Early Output High-Z Time	0			ns	(4)
	TEHWH	Late Output High-Z Time	0			ns	(4)
	TELEL	Read or Write Cycle Time	290			ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room Temp., 5V data provided for information – not guaranteed
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Ex: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC test conditions: Inputs – TRISE = TFALL = 10ns; Output – CLOAD = 50pF. All timing measured at 1.5V reference level.
(5) This parameter is guaranteed and not tested.

ABSOLUTE MAXIMUM RATINGS *		OPERATING RANGE	
Supply Voltage - (VCC - GND)	-0.3V to +8.0V	Operating Supply Voltage Military (-2)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Operating Temperature Military (-2)	-55°C to +125°C
Storage Temperature	-65°C to +150°C		

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	5.0	µA	IO = 0 $\overline{E}$ = VCC –0.3V
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	ICCDR	Data Retention Supply Current		25	3.0	µA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.45	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance (3)		10.0	6.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		ns	(4)
	TAVQV	Address Access Time		320		ns	(4)
	TELQX	Chip Enable Output Enable Time	20			ns	(4)
	TWLQZ	Write Enable Output Disable Time		100		ns	(4) (5)
	TEHQZ	Chip Enable Output Disable Time		100		ns	(4) (5)
	TELEH	Chip Enable Pulse Negative Width	300			ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	120			ns	(4)
	TAVEL	Address Setup Time	20			ns	(4)
	TELAX	Address Hold Time	50			ns	(4)
	TWLWH	Write Enable Pulse Width	300			ns	(4)
	TWLEH	Write Enable Pulse Setup Time	300			ns	(4)
	TELWH	Write Enable Pulse Hold Time	300			ns	(4)
	TDVWH	Data Setup Time	200			ns	(4)
	TWHDZ	Data Hold Time	0			ns	(4)
	TWLDV	Write Data Delay Time	100			ns	(4)
	TWLEL	Early Output High-Z Time	0			ns	(4)
	TEHWH	Late Output High-Z Time	0			ns	(4)
	TELEL	Read or Write Cycle Time	420			ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC Test Conditions: Inputs – TRISE = TFALL = 10nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
(5) **This value is guaranteed and tested at 25°C.**

ABSOLUTE MAXIMUM RATINGS *		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Industrial (-9)	4.5V to 5.5V
Storage Temperature	-65°C to +150°C	Operating Temperature	
		Industrial (-9)	-40°C to +85°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		25	3.0	µA	$\overline{E}$ = VCC –0.3V, IO = 0
	ICCOP	Operating Supply Current (2)		7	5	mA	$\overline{E}$ = 1MHz, IO = 0, VI = GND
	ICCDR	Data Retention Supply Current		15	2.0	µA	VCC = 2.0V, IO = 0, $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.45	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	VI = VCC or GND, f = 1MHz
	CIO	Input/Output Capacitance (3)		10.0	6.0	pF	VIO = VCC or GND, f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		ns	(4)
	TAVQV	Address Access Time		320		ns	(4)
	TELQX	Chip Enable Output Enable Time	20			ns	(4)
	TWLQZ	Write Enable Output Disable Time		100		ns	(4) (5)
	TEHQZ	Chip Enable Output Disable Time		100		ns	(4) (5)
	TELEH	Chip Enable Pulse Negative Width	300			ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	120			ns	(4)
	TAVEL	Address Setup Time	20			ns	(4)
	TELAX	Address Hold Time	50			ns	(4)
	TWLWH	Write Enable Pulse Width	300			ns	(4)
	TWLEH	Write Enable Pulse Setup Time	300			ns	(4)
	TELWH	Write Enable Pulse Hold Time	300			ns	(4)
	TDVWH	Data Setup Time	200			ns	(4)
	TWHDX	Data Hold Time	0			ns	(4)
	TWLDV	Write Data Delay Time	100			ns	(4)
	TWLEL	Early Output High-Z Time	0			ns	(4)
	TEHWH	Late Output High-Z Time	0			ns	(4)
	TELEL	Read or Write Cycle Time	420			ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC Test Conditions: Inputs – TRISE = TFALL = 10nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
(5) This parameter is guaranteed and not tested.

ABSOLUTE MAXIMUM RATINGS *		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage Industrial (-9)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Operating Temperature Industrial (-9)	-40°C to +85°C
Storage Temperature	-65°C to +150°C		

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100	20	µA	IO = 0 $\overline{E}$ = VCC –0.3V
	ICCOP	Operating Supply Current (2)		7	5	mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		50	12	µA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance (3)		10.0	6.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		ns	(4)
	TAVQV	Address Access Time		320		ns	(4)
	TELQX	Chip Enable Output Enable Time	20			ns	(4)
	TWLQZ	Write Enable Output Disable Time		100		ns	(4) (5)
	TEHQZ	Chip Enable Output Disable Time		100		ns	(4) (5)
	TELEH	Chip Enable Pulse Negative Width	300			ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	120			ns	(4)
	TAVEL	Address Setup Time	20			ns	(4)
	TELAX	Address Hold Time	50			ns	(4)
	TWLWH	Write Enable Pulse Width	300			ns	(4)
	TWLEH	Write Enable Pulse Setup Time	300			ns	(4)
	TELWH	Write Enable Pulse Hold Time	300			ns	(4)
	TDVWH	Data Setup Time	200			ns	(4)
	TWHDX	Data Hold Time	0			ns	(4)
	TWLDV	Write Data Delay Time	100			ns	(4)
	TWLEL	Early Output High-Z Time	0			ns	(4)
	TEHWH	Late Output High-Z Time	0			ns	(4)
	TELEL	Read or Write Cycle Time	420			ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC Test Conditions: Inputs – TRISE = TFALL = 10nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
(5) This parameter is guaranteed and not tested.

ABSOLUTE MAXIMUM RATINGS *		OPERATING RANGE	
Supply Voltage – (VCC - GND)	-0.3V to +8.0V	Operating Supply Voltage Commercial	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Operating Temperature Commercial	0°C to +70°C
Storage Temperature	-65°C to +150°C		

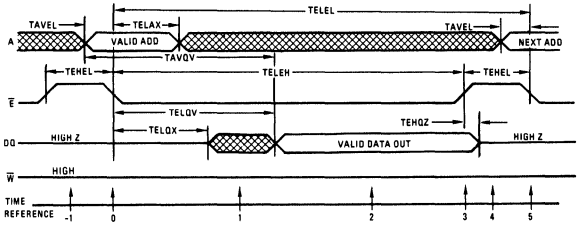
** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		350	50	μA	$\overline{E}$ = VCC –0.3V IO = 0
	ICCOP	Operating Supply Current (2)		7	5	mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		200	30	μA	VCC = 2.0V, IO = 0 $\overline{E}$=VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-10.0	+10.0	±0.5	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-10.0	+10.0	±0.5	μA	VCC ≤ VIO ≤ GND
	VIL	Input Low Voltage	-0.3	0.8	1.2	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -0.4mA
	CI	Input Capacitance (3)		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance (3)		10.0	6.0	pF	VI = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350		ns	(4)
	TAVQV	Address Access Time		370		ns	(4)
	TELQX	Chip Enable Output Enable Time	20			ns	(4)
	TWLQZ	Write Enable Output Disable Time		100		ns	(4) (5)
	TEHQZ	Chip Enable Output Disable Time		100		ns	(4) (5)
	TELEH	Chip Enable Pulse Negative Width	350			ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	150			ns	(4)
	TAVEL	Address Setup Time	20			ns	(4)
	TELAX	Address Hold Time	50			ns	(4)
	TWLWH	Write Enable Pulse Width	350			ns	(4)
	TWLEH	Write Enable Pulse Setup Time	350			ns	(4)
	TELWH	Write Enable Pulse Hold Time	350			ns	(4)
	TDVWH	Data Setup Time	250			ns	(4)
	TWHDX	Data Hold Time	0			ns	(4)
	TWLDV	Write Data Delay Time	100			ns	(4)
	TWLEL	Early Output High-Z Time	0			ns	(4)
	TEHWH	Late Output High-Z Time	0			ns	(4)
	TELEL	Read or Write Cycle Time	500			ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC Test Conditions: Inputs – TRISE = TFALL = 10nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
(5) This parameter is guaranteed and not tested.

Read Cycle

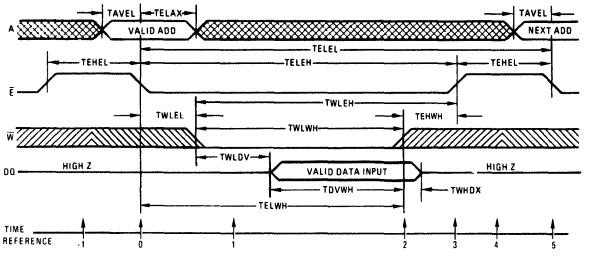


TRUTH TABLE

TIME REFERENCE	INPUTS E	W	A	DATA I/O DQ	FUNCTION
1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. During time (T = 1) the outputs become enabled but data is not valid until time (T = 2). $\overline{W}$ must remain high throughout the read cycle. After the data has been read $\overline{E}$ may return high (T = 3). This will force the output buffers and all inputs to a disabled state at time (T = 4). The memory is now ready for the next cycle.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS E	W	A	DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	X	Z	WRITE PERIOD BEGINS
2	L	↗	X	V	DATA IN IS WRITTEN
3	↗	H	X	Z	WRITE COMPLETED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated by the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on-chip registers. There are two basic types of write cycles, which differ in the control of the common data-in/data-out bus.

Case 1: $\overline{E}$ falls before $\overline{W}$ falls

The output buffers may become enabled (reading) if $\overline{E}$ falls before $\overline{W}$ falls. $\overline{W}$ is used to disable (three-state) the outputs so input data can be applied. TWLDV must be met to allow the $\overline{W}$ signal time to disable the outputs before applying input data. Also, at the end of the cycle the outputs may become active if $\overline{W}$ rises before $\overline{E}$. The RAM outputs and all inputs will-state) after $\overline{E}$ rises (TEHQZ). In this type of write cycle TWLEL and TEHWH may be ignored.

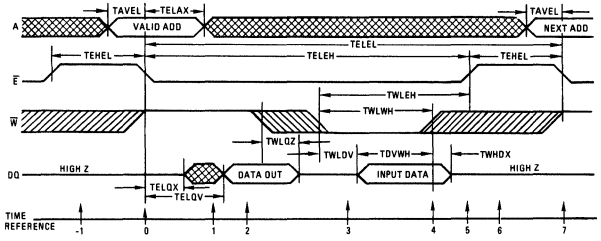
Case 2: $\overline{E}$ falls equal to or after $\overline{W}$ falls, and $\overline{E}$ rises before or equal to $\overline{W}$ rising

This $\overline{E}$ and $\overline{W}$ control timing will guarantee that the data outputs will stay disabled throughout the cycle, thus simplyifying the data input timing. TWLEL and TEHWH must be met but TWLDV becomes meaningless and can be ignored. In this cycle TDVWH and TWHDX become TDVEH and TEHDX. In other words, reference data setup and hold times to the $\overline{E}$ rising edge.

	IF	OBSERVE	IGNORE
Case 1	$\overline{E}$ falls before $\overline{W}$	TWLDV	TWLEL
Case 2	$\overline{E}$ falls after $\overline{W}$ & $\overline{E}$ rises before $\overline{W}$	TWLEL TEHWH	TWLDV TWHDX

If a series of consecutive write cycles are to be performed, $\overline{W}$ may be held low until all desired locations have been written (an extension of Case 2).

Read Modify Write Cycle



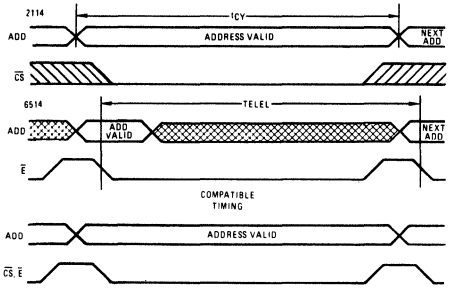
TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	DATAI/O DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	READ MODE, OUTPUT ENABLED
2	L	H	X	V	READ MODE, OUTPUT VALID
3	L	L	X	Z	WRITE MODE, OUTPUT HIGH Z
4	L	↗	X	V	WRITE MODE, DATA IS WRITTEN
5	↗	H	X	Z	WRITE COMPLETED
6	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

If the pulse width of $\overline{W}$ is relatively short in relation to that of $\overline{E}$ a combination read-write cycle may be performed. If $\overline{W}$ remains high for the first part of the cycle, the outputs will become active during time (T = 1). Data out will be valid during time (T = 2). After the data is read, $\overline{W}$ can go low. After minimum TWLWH, $\overline{W}$ may return high. The information just written may now be read or $\overline{E}$ may return high, disabling the output buffers and all inputs and preparing the device for the next cycle. Any number or sequence of read-write operation may be performed while $\overline{E}$ is low providing all timing requirements are met.

NOTES: In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

2114 Compatibility



2114 – Requires the Address to Remain Valid Throughout the Cycle.

6514 – Requires Valid Address for Only a Small Portion of the Cycle, but Requires $\overline{E}$ to Fall to Initiate Each Cycle.

HM-6516

2K x 8 CMOS RAM

Features

- LOW POWER STANDBY — 275 μW MAX
- LOW POWER OPERATION — 55mW/MHz MAX
- FAST ACCESS — 120/200 ns MAX
- INDUSTRY STANDARD PINOUT
- SINGLE SUPPLY — 5 VOLT VCC
- TTL COMPATIBLE
- STATIC MEMORY CELLS
- HIGH OUTPUT DRIVE
- ON CHIP ADDRESS LATCHES
- EASY MICROPROCESSOR INTERFACING
- WIDE TEMPERATURE RANGE

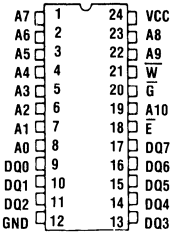
Description

The HM-6516 is a CMOS 2048 x 8 Static Random Access Memory. Extremely low power operation is achieved by the use of complementary MOS design techniques. This low power is further enhanced by the use of synchronous circuit techniques that keep the active (operating) power low, and also give fast access times. The pinout of the HM-6516 is the popular 24 pin, 8 bit wide JEDEC standard which allows easy memory board layouts, flexible enough to accomodate a variety of PROMs, RAMs, EPROMs, and ROMs.

The HM-6516 is ideally suited for use in microprocessor based systems. The byte wide organization simplifies the memory array design,and keeps operating power down to a minimum because only one device is enabled at a time. The address latches allow very simple interfacing to recent generation microprocessors which employ a multiplexed address/data bus. The convenient output enable control also simplifies multiplexed bus interfacing by allowing the data outputs to be controlled independent of the chip enable.

Pinouts

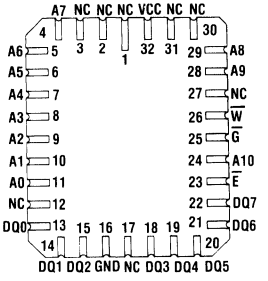
TOP VIEW



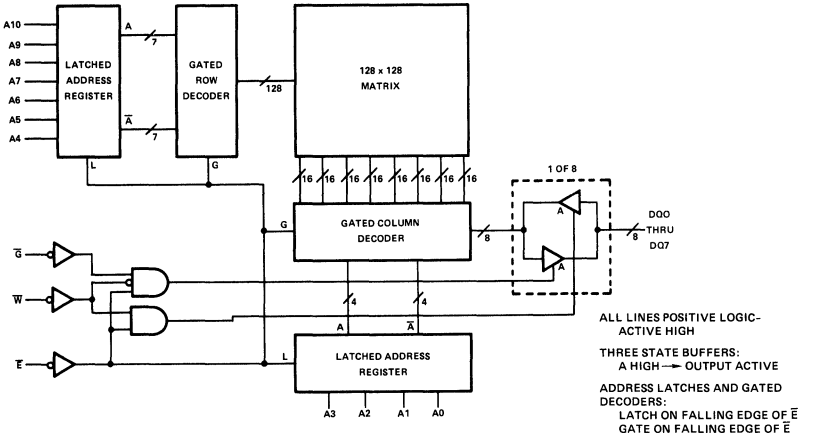
PIN NAMES

A	Address Input
DQ	Data Input/Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
NC	No Connect

TOP VIEW – LCC



Functional Diagram



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (VCC – GND)	–0.3 to 8.0V
Input or Output Voltage Applied	(GND –0.3V) to (VCC +0.3V)
Storage Temperature	–65°C to 150°C

OPERATING RANGE

Operating Supply Voltage	
Military (B–2)	4.5V to 5.5V
Industrial (B–9)	4.5V to 5.5V
Operating Temperature	
Military (B–2)	-55°C to +125°C
Industrial (B–9)	-40°C to +85°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		10	mA	f=1MHz,IO=0,$\overline{G}$=VCC VI = VCC or GND
	ICCDR	Data Retention Supply Current		25	µA	IO = 0, VCC = 2.0, VI = VCC or GND, $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	–1.0	+1.0	µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	–1.0	+1.0	µA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	–0.3	0.8	V	
	VIH	Input High Voltage	2.4	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		V	IO = –1.0mA
	CI	Input Capacitance ③		8.0	pF	VI = VCC or GND, f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	pF	VIO = VCC or GND, f = 1MHz
A.C.	TELQV	Chip Enable Access Time		120	ns	④
	TAVQV	Address Access Time		120	ns	④
	TELQX	Chip Enable Output Enable Time	10		ns	④
	TWLQZ	Write Enable Output Disable Time		50	ns	④
	TEHQZ	Chip Enable Output Disable Time		50	ns	④
	TGLQV	Output Enable Output Valid Time		80	ns	④
	TGLQX	Output Enable Output Enable Time	10		ns	④
	TGHQZ	Output Enable Output Disable Time		50	ns	④
	TELEH	Chip Enable Pulse Negative Width	120		ns	④
	TEHEL	Chip Enable Pulse Positive Width	50		ns	④
	TAVEL	Address Setup Time	0		ns	④
	TELAX	Address Hold Time	30		ns	④
	TWLWH	Write Enable Pulse Width	120		ns	④
	TWLEH	Write Enable Pulse Setup Time	120		ns	④
	TELWH	Write Enable Pulse Hold Time	120		ns	④
	TDVWH	Data Setup Time	50		ns	④
	TWHDX	Data Hold Time	10		ns	④
	TWLDV	Write Data Delay Time	50		ns	④
	TELEL	Read or Write Cycle Time	170		ns	④

NOTES:

① All devices tested at worst case limits.

② Operating Supply Current (ICCOP) is proportional to Operating Frequency.
Example: Typical ICCOP = 5mA/MHz. This parameter is sampled and guaranteed - Not 100% tested.

③ Capacitance sampled and guaranteed - not 100% tested.

④ AC test conditions: Inputs – TRISE = TFALL = 5ns; Output – CLOAD = 50pF. All timing measured at 1.5V reference level. Input pulse levels: 0V to 3V.

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC – GND)	–0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND –0.3V) to (VCC +0.3V)	Military (–2)	4.5V to 5.5V
		Industrial (–9)	4.5V to 5.5V
Storage Temperature	–65°C to 150°C	Operating Temperature	
		Military (–2)	–55°C to +125°C
		Industrial (–9)	–40°C to +85°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP.& VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		10	mA	f=1MHz,IO=0,$\overline{G}$=VCC VI = VCC or GND
	ICCDR	Data Retention Supply Current		50	µA	IO = 0, VCC = 2.0, VI = VCC or GND,
	VCCDR	Data Retention Supply Voltage	2.0		V	$\overline{E}$ = VCC
	II	Input Leakage Current	–1.0	+1.0	µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	–1.0	+1.0	µA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	–0.3	0.8	V	
	VIH	Input High Voltage	2.4	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		V	IO = –1.0mA
	CI	Input Capacitance ③		8.0	pF	VI = VCC or GND, f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	pF	VIO = VCC or GND, f = 1MHz
A.C.	TELQV	Chip Enable Access Time		200	ns	④
	TAVQV	Address Access Time		200	ns	④
	TELQX	Chip Enable Output Enable Time	10		ns	④
	TWLQZ	Write Enable Output Disable Time		80	ns	④
	TEHQZ	Chip Enable Output Disable Time		80	ns	④
	TGLQV	Output Enable Output Valid Time		80	ns	④
	TGLQX	Output Enable Output Enable Time	10		ns	④
	TGHQZ	Output Enable Output Disable Time		80	ns	④
	TELEH	Chip Enable Pulse Negative Width	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	80		ns	④
	TAVEL	Address Setup Time	0		ns	④
	TELAX	Address Hold Time	50		ns	④
	TWLWH	Write Enable Pulse Width	200		ns	④
	TWLEH	Write Enable Pulse Setup Time	200		ns	④
	TELWH	Write Enable Pulse Hold Time	200		ns	④
	TDVWH	Data Setup Time	80		ns	④
	TWHDX	Data Hold Time	10		ns	④
	TWLDV	Write Data Delay Time	80		ns	④
	TELEL	Read or Write Cycle Time	280		ns	④

NOTES:

① All devices tested at worst case limits.

② Operating Supply Current (ICCOP) is proportional to Operating Frequency.
Example: Typical ICCOP = 5mA/MHz. This parameter is sampled and guaranteed - Not 100% tested.

③ Capacitance sampled and guaranteed - not 100% tested.

④ AC test conditions: Inputs – TRISE = TFALL = 10ns; Output – CLOAD = 100pF All timing measured at 1.5V reference level. Input pulse levels: 0V to 3V.

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC – GND)	–0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND –0.3V) to (VCC +0.3V)	Commercial (–5)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	–65°C to 150°C	Commercial (–5)	0°C to 70°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP.&VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		500	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		10	mA	f=1MHz,IO=0,$\overline{G}$=VCC VI = VCC or GND
	ICCDR	Data Retention Supply Current		250	µA	IO = 0, VCC = 2.0, VI = VCC or GND,
	VCCDR	Data Retention Supply Voltage	2.0		V	$\overline{E}$ = VCC
	II	Input Leakage Current	–5.0	+5.0	µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	–5.0	+5.0	µA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	–0.3	0.8	V	
	VIH	Input High Voltage	2.4	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		V	IO = –1.0mA
	CI	Input Capacitance ③		8.0	pF	VI = VCC or GND, f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	pF	VIO = VCC or GND, f = 1MHz
A.C.	TELQV	Chip Enable Access Time		200	ns	④
	TAVQV	Address Access Time		200	ns	④
	TELQX	Chip Enable Output Enable Time	10		ns	④
	TWLQZ	Write Enable Output Disable Time		80	ns	④
	TEHQZ	Chip Enable Output Disable Time		80	ns	④
	TGLQV	Output Enable Output Valid Time		80	ns	④
	TGLQX	Output Enable Output Enable Time	10		ns	④
	TGHQZ	Output Enable Output Disable Time		80	ns	④
	TELEH	Chip Enable Pulse Negative Width	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	80		ns	④
	TAVEL	Address Setup Time	0		ns	④
	TELAX	Address Hold Time	50		ns	④
	TWLWH	Write Enable Pulse Width	200		ns	④
	TWLEH	Write Enable Pulse Setup Time	200		ns	④
	TELWH	Write Enable Pulse Hold Time	200		ns	④
	TDVWH	Data Setup Time	80		ns	④
	TWHDX	Data Hold Time	10		ns	④
	TWLDV	Write Data Delay Time	80		ns	④
	TELEL	Read or Write Cycle Time	280		ns	④

NOTES:

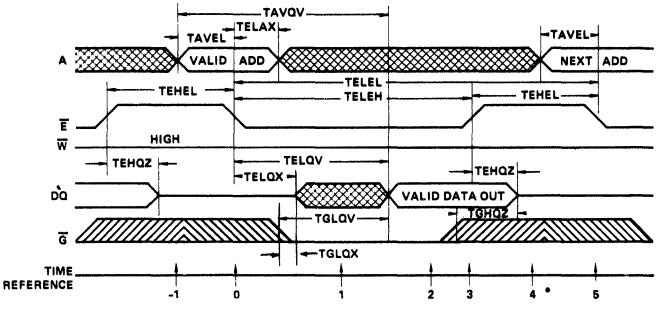
① All devices tested at worst case limits.

② Operating Supply Current (ICCOP) is proportional to Operating Frequency.
Example: Typical ICCOP = 5mA/MHz. This parameter is sampled and guaranteed - Not 100% tested.

③ Capacitance sampled and guaranteed - not 100% tested.

④ AC test conditions: Inputs – TRISE = TFALL = 10ns; Output – CLOAD = 100pF. All timing measured at 1.5V reference level. Input pulse levels: 0V to 3V.

Read Cycle

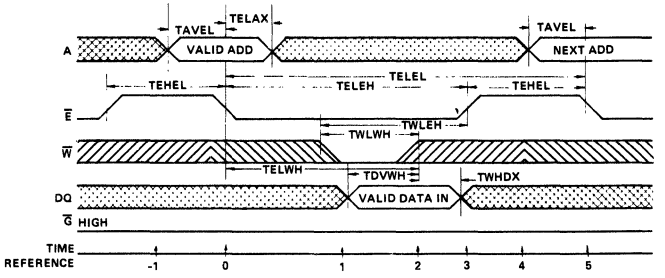


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	$\overline{G}$	A	DQ	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	L	X	X	OUTPUT ENABLED
2	L	H	L	X	V	OUTPUT VALID
3	↗	H	X	X	V	READ ACCOMPLISHED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0), minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1), the outputs become enabled but data is not valid until time (T = 2), $\overline{W}$ must remain high throughout the read cycle. After the data has been read, $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). $\overline{G}$ is used to disable the output buffers when in a logical "1" state (T = -1, 0, 3, 4, 5). After (T = 4) time, the memory is ready for the next cycle.

Write Cycle

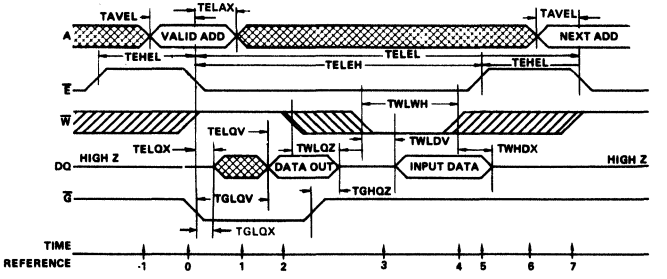


TRUTH TABLE

TIME REFERENCE	INPUTS E	$\overline{W}$	$\overline{G}$	A	DQ	FUNCTION
-1	H	X	H	X	X	MEMORY DISABLED
0	↘	X	H	V	X	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	H	X	X	WRITE PERIOD BEGINS
2	L	↗	H	X	V	DATA IN IS WRITTEN
3	↗	H	H	X	X	WRITE COMPLETED
4	H	X	H	X	X	PREPARE FOR NEXT CYCLE (SAME AS-1)
5	↘	X	H	V	X	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated on the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on chip registers. If a write cycle is to be performed where the output is not to become active, $\overline{G}$ can be held high (inactive). TDVWH and TWHDX must be met for proper device operation regardless of $\overline{G}$. If $\overline{E}$ and $\overline{G}$ fall before $\overline{W}$ falls (read mode), a possible bus conflict may exist. If $\overline{E}$ rises before $\overline{W}$ rises, reference data setup and hold times to the $\overline{E}$ rising edge. The write operation is terminated by the first rising edge of $\overline{W}$ (T = 2) or $\overline{E}$(T = 3). After the minimum $\overline{E}$ high time (TEHEL), the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low unitl all desired locations have been written. In this case, data setup and hold times must be referenced to the rising edge of $\overline{E}$.

Read Modify Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	$\overline{G}$	A	DATA I/O DQ	FUNCTION
-1	H	X	H	X	Z	MEMORY DISABLED
0	↘	H	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	L	X	X	READ MODE, OUTPUT ENABLED ($\overline{W}$ = HIGH, $\overline{G}$ = LOW)
2	L	H	L	X	V	READ MODE, OUTPUT VALID
3	L	L	H	X	Z	WRITE MODE, OUTPUT HIGH Z
4	L	↙	H	X	V	WRITE MODE, DATA IS WRITTEN
5	↙	H	H	X	Z	WRITE COMPLETED
6	H	X	H	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↘	H	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

If the pulse width of $\overline{W}$ is relatively short in relation to that of $\overline{E}$, a combination read write cycle may be performed. If $\overline{W}$ remains high for the first part of the cycle, the output will become active during time (T = 1) provided $\overline{G}$ is low. Data out will be valid during time (T = 2). After the data is read, $\overline{W}$ can go low. After minimum TWLWH, $\overline{W}$ may return high. The information just written may now be read or $\overline{E}$ may return high, disabling the output buffer and preparing the device for the next cycle. Any number or sequence of read-write operations may be performed while $\overline{E}$ is low providing all timing requirements are met.

NOTES:

In the above descriptions, the numbers in parentheses (T = n), refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

Advance Information

Features

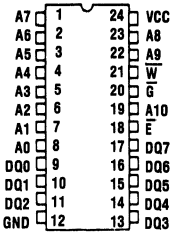
- FAST ACCESS TIME — 55/70/90/120 ns MAX
- LOW STANDBY CURRENT — 50μA MAX
- LOW OPERATING CURRENT — 70 mA MAX
- DATA RETENTION @ 2.0 VOLTS — 20μA MAX
- TTL COMPATIBLE INPUTS AND OUTPUTS
- JEDEC APPROVED PINOUT (2716, 6116 TYPE)
- NO CLOCKS OR STROBES REQUIRED
- WIDE TEMPERATURE RANGE — −55°C to +125°C
- EQUAL CYCLE AND ACCESS TIME
- SINGLE 5 VOLT SUPPLY
- GATED INPUTS – NO PULL-UP OR PULL-DOWN RESISTORS ARE REQUIRED

Description

The HM-65162 is a CMOS 2048 x 8 Static Random Access Memory manufactured using the HARRIS advanced SAJI V process. The device utilizes asynchronous circuit design for fast cycle time and ease of use. The pinout is the JEDEC 24 pin, 8 bit wide standard which allows easy memory board layouts flexible to accommodate a variety of industry standard PROMs, RAMs, ROMs and EPROMs. The HM-65162 is ideally suited for use in microprocessor based systems with its 8 bit word length organization. The convenient output enable also simplifies the bus interface by allowing the data outputs to be controlled independent of the chip enable. Gated inputs lower operating current and also eliminate the need for pull-up or pull-down resistors.

Pinouts

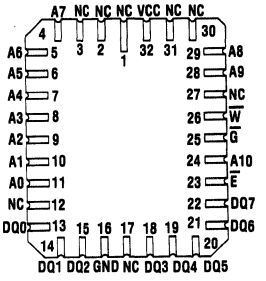
TOP VIEW



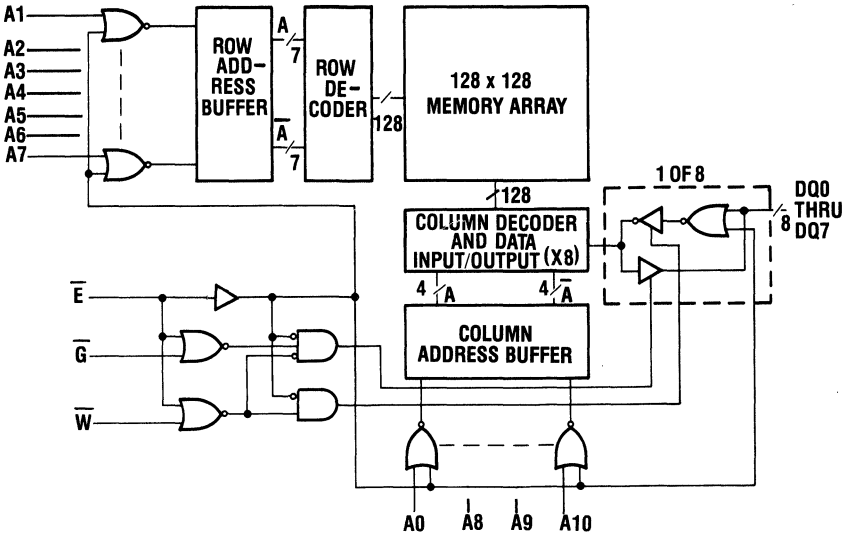
PIN NAMES

A	Address Input
DQ	Data Input/Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
NC	No Connect

TOP VIEW – LCC



Functional Diagram



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC - GND)	−0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)	Military (−2)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	−65°C to 150°C	Military (−2)	−55°C to +125°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		50	μA	IO = 0, $\overline{E}$ = VCC−0.3V
	ICCSB	Standby Supply Current		8	mA	$\overline{E}$ = VIH, IO = 0
	ICC	Enabled Supply Current		70	mA	$\overline{E}$ = VIL, IO = 0
	ICCOP	Operating Supply Current ②		70	mA	$\overline{E}$ = VIL, IO = 0 f = 1 MHz
	ICCDR	Data Retention Supply Current		20	μA	IO = 0, VCC = 2.0 $\overline{E}$ = VCC−0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−1.0	+1.0	μA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	−1.0	+1.0	μA	GND≤VIO≤VCC
	VIL	Input Low Voltage	−0.3	0.8	V	
	VIH	Input High Voltage	2.2	VCC +0.3V	V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8	pF	VI = VCC or GND, f = 1 MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1 MHz
READ CYCLE	TAVAV	Read Cycle Time	70		ns	④
	TAVQV	Address Access Time		70	ns	④
	TELQV	Chip Enable Access Time		70	ns	④
	TELQX	Chip Enable Output Enable Time	5		ns	④
	TGLQV	Output Enable Output Enable Time		50	ns	④
	TGLQX	Output Enable Output Enable Time	5		ns	④
	TEHQZ	Chip Enable Output Disable Time		35	ns	④
	TGHQZ	Output Enable Output Disable Time		35	ns	④
	TAVQX	Output Hold from Address Change	5		ns	④
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	70		ns	④
	TELWH	Chip Selection to End of Write	45		ns	④
	TAVWL	Address Setup Time	10		ns	④
	TWLWH	Write Enable Pulse Width	40		ns	④
	TWHAV	Write Enable Read Setup Time	10		ns	④
	TGHQZ	Output Enable Output Disable Time		35	ns	④
	TWLQZ	Write Enable Output Disable Time		40	ns	④
	TDVWH	Data Setup Time	30		ns	④
	TWHDX	Data Hold Time	10		ns	④
	TWHQX	Write Enable Output Enable Time	0		ns	④
	TWLEH	Write Enable Pulse Setup Time	40		ns	④
	TDVEH	Chip Enable Data Setup Time	30		ns	④
	TAVWH	Address Valid to End of Write	65		ns	④

NOTES:
① All devices tested at worst case limits.
② Typical derating = 5mA/MHz increase in ICCOP; VI = VCC or GND.
③ Capacitance sampled and guaranteed – not 100% tested.
④ Input pulse levels: 0V to 3.0V; Input rise and fall times: 5 ns; Input and Output timing reference levels: 1.5V; Output load: 1TTL Gate and C_L = 100pF (including scope and jig)

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC - GND)	−0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)	Military (−2)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	−65°C to 150°C	Military (−2)	−55°C to +125°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		100	μA	IO = 0, $\overline{E}$ = VCC−0.3V
	ICCSB	Standby Supply Current		8	mA	$\overline{E}$ = VIH, IO = 0
	ICC	Enabled Supply Current		70	mA	$\overline{E}$ = VIL, IO = 0
	ICCOP	Operating Supply Current ②		70	mA	$\overline{E}$ = VIL, IO = 0 f = 1 MHz
	ICCDR	Data Retention Supply Current		40	μA	IO = 0, VCC = 2.0 $\overline{E}$ = VCC−0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−1.0	+1.0	μA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	−1.0	+1.0	μA	GND≤VIO≤VCC
	VIL	Input Low Voltage	−0.3	0.8	V	
	VIH	Input High Voltage	2.2	VCC +0.3V	V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8	pF	VI = VCC or GND, f = 1 MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1 MHz
READ CYCLE	TAVAV	Read Cycle Time	90		ns	④
	TAVQV	Address Access Time		90	ns	④
	TELQV	Chip Enable Access Time		90	ns	④
	TELQX	Chip Enable Output Enable Time	5		ns	④
	TGLQV	Output Enable Output Enable Time		65	ns	④
	TGLQX	Output Enable Output Enable Time	5		ns	④
	TEHQZ	Chip Enable Output Disable Time		50	ns	④
	TGHQZ	Output Enable Output Disable Time		40	ns	④
	TAVQX	Output Hold from Address Change	5		ns	④
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	90		ns	④
	TELWH	Chip Selection to End of Write	55		ns	④
	TAVWL	Address Setup Time	10		ns	④
	TWLWH	Write Enable Pulse Width	55		ns	④
	TWHAV	Write Enable Read Setup Time	10		ns	④
	TGHQZ	Output Enable Output Disable Time		40	ns	④
	TWLQZ	Write Enable Output Disable Time		50	ns	④
	TDVWH	Data Setup Time	30		ns	④
	TWHDX	Data Hold Time	15		ns	④
	TWHQX	Write Enable Output Enable Time	0		ns	④
	TWLEH	Write Enable Pulse Setup Time	55		ns	④
	TDVEH	Chip Enable Data Setup Time	30		ns	④
	TAVWH	Address Valid to End of Write	80		ns	④

NOTES:
① All devices tested at worst case limits.
② Typical derating = 5mA/MHz increase in ICCOP; VI = VCC or GND.
③ Capacitance sampled and guaranteed – not 100% tested.
④ Input pulse levels: 0V to 3.0V; Input rise and fall times: 5 ns; Input and Output timing reference levels: 1.5V; Output load: 1TTL Gate and C_L = 100pF (including scope and jig)

Specifications HM-65162C-2

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC - GND)	−0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)	Military (−2)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	−65°C to 150°C	Military (−2)	−55°C to +125°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		1000	μA	IO = 0, $\overline{E}$ = VCC−0.3V
	ICCSB	Standby Supply Current		8	mA	$\overline{E}$ = VIH, IO = 0
	ICC	Enabled Supply Current		70	mA	$\overline{E}$ = VIL, IO = 0
	ICCOP	Operating Supply Current ②		70	mA	$\overline{E}$ = VIL, IO = 0 f = 1 MHz
	ICCDR	Data Retention Supply Current		400	μA	IO = 0, VCC = 2.0 $\overline{E}$ = VCC−0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−5.0	+5.0	μA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	−5.0	+5.0	μA	GND≤VIO≤VCC
	VIL	Input Low Voltage	−0.3	0.8	V	
	VIH	Input High Voltage	2.2	VCC +0.3V	V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8	pF	VI = VCC or GND, f = 1 MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1 MHz
READ CYCLE	TAVAV	Read Cycle Time	120		ns	④
	TAVQV	Address Access Time		120	ns	④
	TELQV	Chip Enable Access Time		120	ns	④
	TELQX	Chip Enable Output Enable Time	5		ns	④
	TGLQV	Output Enable Output Enable Time		80	ns	④
	TGLQX	Output Enable Output Enable Time	5		ns	④
	TEHQZ	Chip Enable Output Disable Time		50	ns	④
	TGHQZ	Output Enable Output Disable Time		40	ns	④
	TAVQX	Output Hold from Address Change	5		ns	④
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	120		ns	④
	TELWH	Chip Selection to End of Write	70		ns	④
	TAVWL	Address Setup Time	10		ns	④
	TWLWH	Write Enable Pulse Width	70		ns	④
	TWHAV	Write Enable Read Setup Time	10		ns	④
	TGHQZ	Output Enable Output Disable Time		40	ns	④
	TWLQZ	Write Enable Output Disable Time		50	ns	④
	TDVWH	Data Setup Time	35		ns	④
	TWHDX	Data Hold Time	15		ns	④
	TWHQX	Write Enable Output Enable Time	0		ns	④
	TWLEH	Write Enable Pulse Setup Time	70		ns	④
	TDVEH	Chip Enable Data Setup Time	35		ns	④
	TAVWH	Address Valid to End of Write	105		ns	④

NOTES:
① All devices tested at worst case limits.
② Typical derating = 5mA/MHz increase in ICCOP; VI = VCC or GND.
③ Capacitance sampled and guaranteed – not 100% tested.
④ Input pulse levels: 0V to 3.0V; Input rise and fall times: 5 ns; Input and Output timing reference levels: 1.5V; Output load: 1TTL Gate and C_L = 100pF (including scope and jig)

Specifications HM-65162S-9

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC - GND)	−0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)	Industrial (−9)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	−65°C to 150°C	Industrial (−9)	−40°C to +85°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		100	μA	IO = 0, $\overline{E}$ = VCC−0.3V
	ICCSB	Standby Supply Current		8	mA	$\overline{E}$ = VIH, IO = 0
	ICC	Enabled Supply Current		70	mA	$\overline{E}$ = VIL, IO = 0
	ICCOP	Operating Supply Current ②		70	mA	$\overline{E}$ = VIL, IO = 0 f = 1 MHz
	ICCDR	Data Retention Supply Current		40	μA	IO = 0, VCC = 2.0 $\overline{E}$ = VCC−0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−1.0	+1.0	μA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	−1.0	+1.0	μA	GND≤VIO≤VCC
	VIL	Input Low Voltage	−0.3	0.8	V	
	VIH	Input High Voltage	2.4	VCC +0.3V	V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8	pF	VI = VCC or GND, f = 1 MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1 MHz
READ CYCLE	TAVAV	Read Cycle Time	55		ns	④
	TAVQV	Address Access Time		55	ns	④
	TELQV	Chip Enable Access Time		55	ns	④
	TELQX	Chip Enable Output Enable Time	5		ns	④
	TGLQV	Output Enable Output Enable Time		35	ns	④
	TGLQX	Output Enable Output Enable Time	5		ns	④
	TEHQZ	Chip Enable Output Disable Time		30	ns	④
	TGHQZ	Output Enable Output Disable Time		25	ns	④
	TAVQX	Output Hold from Address Change	5		ns	④
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	55		ns	④
	TELWH	Chip Selection to End of Write	45		ns	④
	TAVWL	Address Setup Time	5		ns	④
	TWLWH	Write Enable Pulse Width	35		ns	④
	TWHAV	Write Enable Read Setup Time	10		ns	④
	TGHQZ	Output Enable Output Disable Time		25	ns	④
	TWLQZ	Write Enable Output Disable Time		25	ns	④
	TDVWH	Data Setup Time	25		ns	④
	TWHDX	Data Hold Time	10		ns	④
	TWHQX	Write Enable Output Enable Time	0		ns	④
	TWLEH	Write Enable Pulse Setup Time	50		ns	④
	TDVEH	Chip Enable Data Setup Time	25		ns	④
	TAVWH	Address Valid to End of Write	50		ns	④

NOTES:
① All devices tested at worst case limits.
② Typical derating = 5mA/MHz increase in ICCOP; VI = VCC or GND.
③ Capacitance sampled and guaranteed – not 100% tested.
④ Input pulse levels: 0V to 3.0V; Input and Output timing reference levels: 1.5V
Input rise and fall times: 5 ns; Output load: 1TTL Gate and C_L = 100pF (including scope and jig)

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC - GND)	−0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)	Industrial (−9)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	−65°C to 150°C	Industrial (−9)	−40°C to +85°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		50	μA	IO = 0, $\overline{E}$ = VCC−0.3V
	ICCSB	Standby Supply Current		8	mA	$\overline{E}$ = VIH, IO = 0
	ICC	Enabled Supply Current		70	mA	$\overline{E}$ = VIL, IO = 0
	ICCOP	Operating Supply Current ②		70	mA	$\overline{E}$ = VIL, IO = 0 f = 1 MHz
	ICCDR	Data Retention Supply Current		20	μA	IO = 0, VCC = 2.0 $\overline{E}$ = VCC−0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−1.0	+1.0	μA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	−1.0	+1.0	μA	GND≤VIO≤VCC
	VIL	Input Low Voltage	−0.3	0.8	V	
	VIH	Input High Voltage	2.2	VCC +0.3V	V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8	pF	VI = VCC or GND, f = 1 MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1 MHz
A.C. READ CYCLE	TAVAV	Read Cycle Time	70		ns	④
	TAVQV	Address Access Time		70	ns	④
	TELQV	Chip Enable Access Time		70	ns	④
	TELQX	Chip Enable Output Enable Time	5		ns	④
	TGLQV	Output Enable Output Enable Time		50	ns	④
	TGLQX	Output Enable Output Enable Time	5		ns	④
	TEHQZ	Chip Enable Output Disable Time		35	ns	④
	TGHQZ	Output Enable Output Disable Time		35	ns	④
	TAVQX	Output Hold from Address Change	5		ns	④
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	70		ns	④
	TELWH	Chip Selection to End of Write	45		ns	④
	TAVWL	Address Setup Time	10		ns	④
	TWLWH	Write Enable Pulse Width	40		ns	④
	TWHAV	Write Enable Read Setup Time	10		ns	④
	TGHQZ	Output Enable Output Disable Time		35	ns	④
	TWLQZ	Write Enable Output Disable Time		40	ns	④
	TDVWH	Data Setup Time	30		ns	④
	TWHDX	Data Hold Time	10		ns	④
	TWHQX	Write Enable Output Enable Time	0		ns	④
	TWLEH	Write Enable Pulse Setup Time	40		ns	④
	TDVEH	Chip Enable Data Setup Time	30		ns	④
	TAVWH	Address Valid to End of Write	65		ns	④

NOTES:
① All devices tested at worst case limits.
② Typical derating = 5mA/MHz increase in ICCOP; VI = VCC or GND.
③ Capacitance sampled and guaranteed – not 100% tested.
④ Input pulse levels: 0V to 3.0V; Input rise and fall times: 5 ns; Input and Output timing reference levels: 1.5V; Output load: 1TTL Gate and C_L = 100pF (including scope and jig)

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC - GND)	−0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)	Industrial (−9)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	−65°C to 150°C	Industrial (−9)	−40°C to +85°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		100	μA	IO = 0, $\overline{E}$ = VCC−0.3V
	ICCSB	Standby Supply Current		8	mA	$\overline{E}$ = VIH, IO = 0
	ICC	Enabled Supply Current		70	mA	$\overline{E}$ = VIL, IO = 0
	ICCOP	Operating Supply Current		70	mA	$\overline{E}$ = VIL, IO = 0 f = 1 MHz
	ICCDR	Data Retention Supply Current		40	μA	IO = 0, VCC = 2.0 $\overline{E}$ = VCC−0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−1.0	+1.0	μA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	−1.0	+1.0	μA	GND≤VIO≤VCC
	VIL	Input Low Voltage	−0.3	0.8	V	
	VIH	Input High Voltage	2.2	VCC +0.3V	V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance		8	pF	VI = VCC or GND, f = 1 MHz
	CIO	Input/Output Capacitance		10	pF	VIO = VCC or GND, f = 1 MHz
A.C. READ CYCLE	TAVAV	Read Cycle Time	90		ns	④
	TAVQV	Address Access Time		90	ns	④
	TELQV	Chip Enable Access Time		90	ns	④
	TELQX	Chip Enable Output Enable Time	5		ns	④
	TGLQV	Output Enable Output Enable Time		65	ns	④
	TGLQX	Output Enable Output Enable Time	5		ns	④
	TEHQZ	Chip Enable Output Disable Time		50	ns	④
	TGHQZ	Output Enable Output Disable Time		40	ns	④
	TAVQX	Output Hold from Address Change	5		ns	④
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	90		ns	④
	TELWH	Chip Selection to End of Write	55		ns	④
	TAVWL	Address Setup Time	10		ns	④
	TWLWH	Write Enable Pulse Width	55		ns	④
	TWHAV	Write Enable Read Setup Time	10		ns	④
	TGHQZ	Output Enable Output Disable Time		40	ns	④
	TWLQZ	Write Enable Output Disable Time		50	ns	④
	TDVWH	Data Setup Time	30		ns	④
	TWHDX	Data Hold Time	15		ns	④
	TWHQX	Write Enable Output Enable Time	0		ns	④
	TWLEH	Write Enable Pulse Setup Time	55		ns	④
	TDVEH	Chip Enable Data Setup Time	30		ns	④
	TAVWH	Address Valid to End of Write	80		ns	④

NOTES:
① All devices tested at worst case limits.
② Typical derating = 5mA/MHz increase in ICCOP; VI = VCC or GND.
③ Capacitance sampled and guaranteed – not 100% tested.
④ Input pulse levels: 0V to 3.0V; Input rise and fall times: 5 ns; Input and Output timing reference levels: 1.5V; Output load: 1TTL Gate and C_L = 100pF (including scope and jig)

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC - GND)	−0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)	Industrial (−9)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	−65°C to 150°C	Industrial (−9)	−40°C to +85°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		1000	μA	IO = 0, $\overline{E}$ = VCC−0.3V
	ICCSB	Standby Supply Current		8	mA	$\overline{E}$ = VIH, IO = 0
	ICC	Enabled Supply Current		70	mA	$\overline{E}$ = VIL, IO = 0
	ICCOP	Operating Supply Current ②		70	mA	$\overline{E}$ = VIL, IO = 0 f = 1 MHz
	ICCDR	Data Retention Supply Current		400	μA	IO = 0, VCC = 2.0 $\overline{E}$ = VCC−0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−5.0	+5.0	μA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	−5.0	+5.0	μA	GND≤VIO≤VCC
	VIL	Input Low Voltage	−0.3	0.8	V	
	VIH	Input High Voltage	2.2	VCC +0.3V	V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8	pF	VI = VCC or GND, f = 1 MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1 MHz
READ CYCLE	TAVAV	Read Cycle Time	90		ns	④
	TAVQV	Address Access Time		90	ns	④
	TELQV	Chip Enable Access Time		90	ns	④
	TELQX	Chip Enable Output Enable Time	5		ns	④
	TGLQV	Output Enable Output Enable Time		65	ns	④
	TGLQX	Output Enable Output Enable Time	5		ns	④
	TEHQZ	Chip Enable Output Disable Time		50	ns	④
	TGHQZ	Output Enable Output Disable Time		40	ns	④
	TAVQX	Output Hold from Address Change	5		ns	④
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	90		ns	④
	TELWH	Chip Selection to End of Write	55		ns	④
	TAVWL	Address Setup Time	10		ns	④
	TWLWH	Write Enable Pulse Width	55		ns	④
	TWHAV	Write Enable Read Setup Time	10		ns	④
	TGHQZ	Output Enable Output Disable Time		40	ns	④
	TWLQZ	Write Enable Output Disable Time		50	ns	④
	TDVWH	Data Setup Time	30		ns	④
	TWHDX	Data Hold Time	10		ns	④
	TWHQX	Write Enable Output Enable Time	0		ns	④
	TWLEH	Write Enable Pulse Setup Time	55		ns	④
	TDVEH	Chip Enable Data Setup Time	30		ns	④
	TAVWH	Address Valid to End of Write	80		ns	④

NOTES:
① All devices tested at worst case limits.
② Typical derating = 5mA/MHz increase in ICCOP; VI = VCC or GND.
③ Capacitance sampled and guaranteed – not 100% tested.
④ Input pulse levels: 0V to 3.0V; Input rise and fall times: 5 ns; Input and Output timing reference levels: 1.5V; Output load: 1TTL Gate and C_L = 100pF (including scope and jig)

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC - GND)	−0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)	Commercial (−5)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	−65°C to 150°C	Commercial (−5)	0°C to +70°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		100	μA	IO = 0, $\overline{E}$ = VCC−0.3V
	ICCSB	Standby Supply Current		8	mA	$\overline{E}$ = VIH, IO = 0
	ICC	Enabled Supply Current		70	mA	$\overline{E}$ = VIL, IO = 0
	ICCOP	Operating Supply Current ②		70	mA	$\overline{E}$ = VIL, IO = 0 f = 1 MHz
	ICCDR	Data Retention Supply Current		40	μA	IO = 0, VCC = 2.0 $\overline{E}$ = VCC−0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−1.0	+1.0	μA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	−1.0	+1.0	μA	GND≤VIO≤VCC
	VIL	Input Low Voltage	−0.3	0.8	V	
	VIH	Input High Voltage	2.4	VCC +0.3V	V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8	pF	VI = VCC or GND, f = 1 MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1 MHz
READ CYCLE	TAVAV	Read Cycle Time	55		ns	④
	TAVQV	Address Access Time		55	ns	④
	TELQV	Chip Enable Access Time		55	ns	④
	TELQX	Chip Enable Output Enable Time	5		ns	④
	TGLQV	Output Enable Output Enable Time		35	ns	④
	TGLQX	Output Enable Output Enable Time	5		ns	④
	TEHQZ	Chip Enable Output Disable Time		30	ns	④
	TGHQZ	Output Enable Output Disable Time		25	ns	④
	TAVQX	Output Hold from Address Change	5		ns	④
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	55		ns	④
	TELWH	Chip Selection to End of Write	45		ns	④
	TAVWL	Address Setup Time	5		ns	④
	TWLWH	Write Enable Pulse Width	35		ns	④
	TWHAV	Write Enable Read Setup Time	10		ns	④
	TGHQZ	Output Enable Output Disable Time		25	ns	④
	TWLQZ	Write Enable Output Disable Time		25	ns	④
	TDVWH	Data Setup Time	25		ns	④
	TWHDX	Data Hold Time	10		ns	④
	TWHQX	Write Enable Output Enable Time	0		ns	④
	TWLEH	Write Enable Pulse Setup Time	50		ns	④
	TDVEH	Chip Enable Data Setup Time	25		ns	④
	TAVWH	Address Valid to End of Write	50		ns	④

NOTES:
① All devices tested at worst case limits.
② Typical derating = 5mA/MHz increase in ICCOP; VI = VCC or GND.
③ Capacitance sampled and guaranteed – not 100% tested.
④ Input pulse levels: 0V to 3.0V; Input rise and fall times: 5 ns; Input and Output timing reference levels: 1.5V; Output load: 1TTL Gate and C_L = 100pF (including scope and jig)

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC - GND)	−0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)	Commercial (−5)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	−65°C to 150°C	Commercial (−5)	0°C to +70°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		50	μA	IO = 0, $\overline{E}$ = VCC−0.3V
	ICCSB	Standby Supply Current		8	mA	$\overline{E}$ = VIH, IO = 0
	ICC	Enabled Supply Current		70	mA	$\overline{E}$ = VIL, IO = 0
	ICCOP	Operating Supply Current ②		70	mA	$\overline{E}$ = VIL, IO = 0 f = 1 MHz
	ICCDR	Data Retention Supply Current		20	μA	IO = 0, VCC = 2.0 $\overline{E}$ = VCC−0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−1.0	+1.0	μA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	−1.0	+1.0	μA	GND≤VIO≤VCC
	VIL	Input Low Voltage	−0.3	0.8	V	
	VIH	Input High Voltage	2.2	VCC +0.3V	V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8	pF	VI = VCC or GND, f = 1 MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1 MHz
READ CYCLE	TAVAV	Read Cycle Time	70		ns	④
	TAVQV	Address Access Time		70	ns	④
	TELQV	Chip Enable Access Time		70	ns	④
	TELQX	Chip Enable Output Enable Time	5		ns	④
	TGLQV	Output Enable Output Enable Time		50	ns	④
	TGLQX	Output Enable Output Enable Time	5		ns	④
	TEHQZ	Chip Enable Output Disable Time		35	ns	④
	TGHQZ	Output Enable Output Disable Time		35	ns	④
	TAVQX	Output Hold from Address Change	5		ns	④
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	70		ns	④
	TELWH	Chip Selection to End of Write	45		ns	④
	TAVWL	Address Setup Time	10		ns	④
	TWLWH	Write Enable Pulse Width	40		ns	④
	TWHAV	Write Enable Read Setup Time	10		ns	④
	TGHQZ	Output Enable Output Disable Time		35	ns	④
	TWLQZ	Write Enable Output Disable Time		40	ns	④
	TDVWH	Data Setup Time	30		ns	④
	TWHDX	Data Hold Time	10		ns	④
	TWHQX	Write Enable Output Enable Time	0		ns	④
	TWLEH	Write Enable Pulse Setup Time	40		ns	④
	TDVEH	Chip Enable Data Setup Time	30		ns	④
	TAVWH	Address Valid to End of Write	65		ns	④

NOTES:
① All devices tested at worst case limits.
② Typical derating = 5mA/MHz increase in ICCOP; VI = VCC or GND.
③ Capacitance sampled and guaranteed – not 100% tested.
④ Input pulse levels: 0V to 3.0V; Input rise and fall times: 5 ns; Input and Output timing reference levels: 1.5V; Output load: 1TTL Gate and C_L = 100pF (including scope and jig)

Specifications HM-65162-5

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC - GND)	−0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)	Commercial (−5)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	−65°C to 150°C	Commercial (−5)	0°C to +70°C

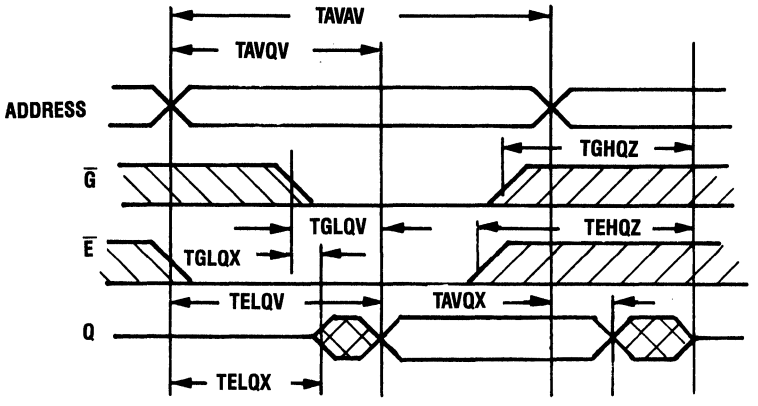
** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		100	μA	IO = 0, $\overline{E}$ = VCC−0.3V
	ICCSB	Standby Supply Current		8	mA	$\overline{E}$ = VIH, IO = 0
	ICC	Enabled Supply Current		70	mA	$\overline{E}$ = VIL, IO = 0
	ICCOP	Operating Supply Current ②		70	mA	$\overline{E}$ = VIL, IO = 0 f = 1 MHz
	ICCDR	Data Retention Supply Current		40	μA	IO = 0, VCC = 2.0 $\overline{E}$ = VCC−0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−1.0	+1.0	μA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	−1.0	+1.0	μA	GND≤VIO≤VCC
	VIL	Input Low Voltage	−0.3	0.8	V	
	VIH	Input High Voltage	2.2	VCC +0.3V	V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8	pF	VI = VCC or GND, f = 1 MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1 MHz
READ CYCLE	TAVAV	Read Cycle Time	90		ns	④
	TAVQV	Address Access Time		90	ns	④
	TELQV	Chip Enable Access Time		90	ns	④
	TELQX	Chip Enable Output Enable Time	5		ns	④
	TGLQV	Output Enable Output Enable Time		65	ns	④
	TGLQX	Output Enable Output Enable Time	5		ns	④
	TEHQZ	Chip Enable Output Disable Time		50	ns	④
	TGHQZ	Output Enable Output Disable Time		40	ns	④
	TAVQX	Output Hold from Address Change	5		ns	④
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	90		ns	④
	TELWH	Chip Selection to End of Write	55		ns	④
	TAVWL	Address Setup Time	10		ns	④
	TWLWH	Write Enable Pulse Width	55		ns	④
	TWHAV	Write Enable Read Setup Time	10		ns	④
	TGHQZ	Output Enable Output Disable Time		40	ns	④
	TWLQZ	Write Enable Output Disable Time		50	ns	④
	TDVWH	Data Setup Time	30		ns	④
	TWHDX	Data Hold Time	15		ns	④
	TWHQX	Write Enable Output Enable Time	0		ns	④
	TWLEH	Write Enable Pulse Setup Time	55		ns	④
	TDVEH	Chip Enable Data Setup Time	30		ns	④
	TAVWH	Address Valid to End of Write	80		ns	④

NOTES:
① All devices tested at worst case limits.
② Typical derating = 5mA/MHz increase in ICCOP; VI = VCC or GND.
③ Capacitance sampled and guaranteed – not 100% tested.
④ Input pulse levels: 0V to 3.0V; Input and Output timing reference levels: 1.5V
Input rise and fall times: 5 ns; Output load: 1TTL Gate and C_L = 100pF (including scope and jig)

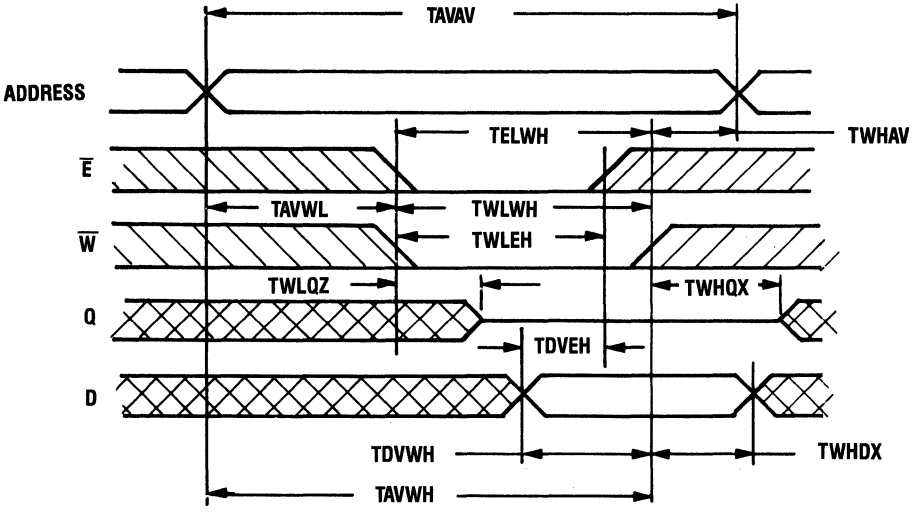
Read Cycle



NOTE: $\overline{W}$ IS HIGH FOR A READ CYCLE

Addresses must remain stable for the duration of the read cycle. To read, $\overline{G}$ and $\overline{E}$ must be $\leq$ VIL and $\overline{W} \geq$ VIH. The output buffers can be controlled independently by $\overline{G}$ while $\overline{E}$ is low. To execute consecutive read cycles, $\overline{E}$ may be tied low continuously until all desired locations are accessed. When $\overline{E}$ is low, addresses must be driven by stable logic levels and must not be in the high impedance state.

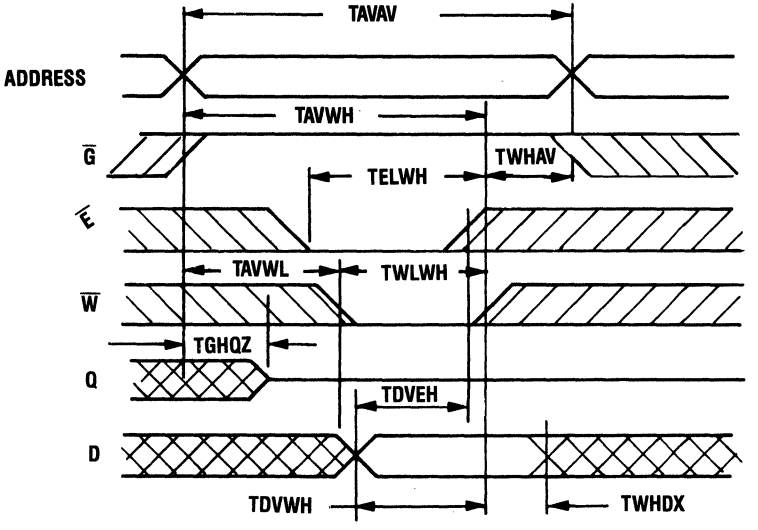
Write Cycle I



NOTE: $\overline{G}$ IS LOW THROUGHOUT WRITE CYCLE

To write, addresses must be stable, $\overline{E}$ low and $\overline{W}$ falling low for a period no shorter than TWLWH. Data in is referenced with the rising edge of $\overline{W}$. (TDVWH and TWHDX). While addresses are changing, $\overline{W}$ must be high. When $\overline{W}$ falls low, the I/O pins are still in the output state for a period of TWLQZ and input data of the opposite phase to the outputs must not be applied. (Bus contention). If $\overline{E}$ transitions low simultaneously with the $\overline{W}$ line transitioning low or after the $\overline{W}$ transition, the output will remain in a high impedance state. $\overline{G}$ is held continuously low.

Write Cycle II



In this write cycle $\overline{G}$ has control of the output after a period, TGHQZ. $\overline{G}$ switching the output to a high impedance state allows data in to be applied without bus contention after TGHQZ. When $\overline{W}$ transitions high, the data in can change after TWHDX to complete the write cycle.

HARRIS

HM-65172

2048 × 8 Asynchronous CMOS Static RAM

Advance Information

Features

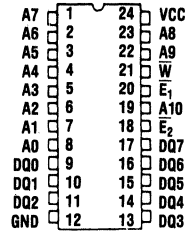
- FAST ACCESS TIME — 55/70/90/120 ns MAX
- LOW STANDBY CURRENT — 50 μA MAX
- LOW OPERATING CURRENT — 70 mA MAX
- DATA RETENTION @ 2.0 VOLTS — 20 μA MAX
- TTL COMPATIBLE INPUTS AND OUTPUTS
- TOSHIBA 5516/HITACHI 6117 PINOUT — TWO CHIP ENABLE INPUTS
- NO CLOCKS OR STROBES REQUIRED
- WIDE TEMPERATURE RANGE — −55°C to +125°C
- EQUAL CYCLE AND ACCESS TIME
- SINGLE 5 VOLT SUPPLY
- GATED INPUTS — NO PULL-UP OR PULL-DOWN RESISTORS ARE REQUIRED

Description

The HM-65172 is a CMOS 2048 x 8 Static Random Access Memory manufactured using the HARRIS advanced SAJI V process. The device utilizes asynchronous circuit design for fast cycle time and ease of use. The pinout is a 24-pin, industry standard which allows easy memory board layouts flexible to accommodate a variety of industry standard PROMs, RAMs, ROMs and EPROMs. The HM-65172 is ideally suited for use in microprocessor based systems with its 8 bit word length organization. Gated inputs lower operating current and also eliminate the need for pull-up or pull-down resistors. The HM-65172 features two chip enables; $\overline{E}_1$ for fast memory access and $\overline{E}_2$ for low power applications where battery operation or battery back-up for nonvolatility are required.

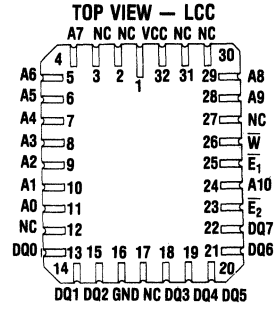
Pinouts

TOP VIEW

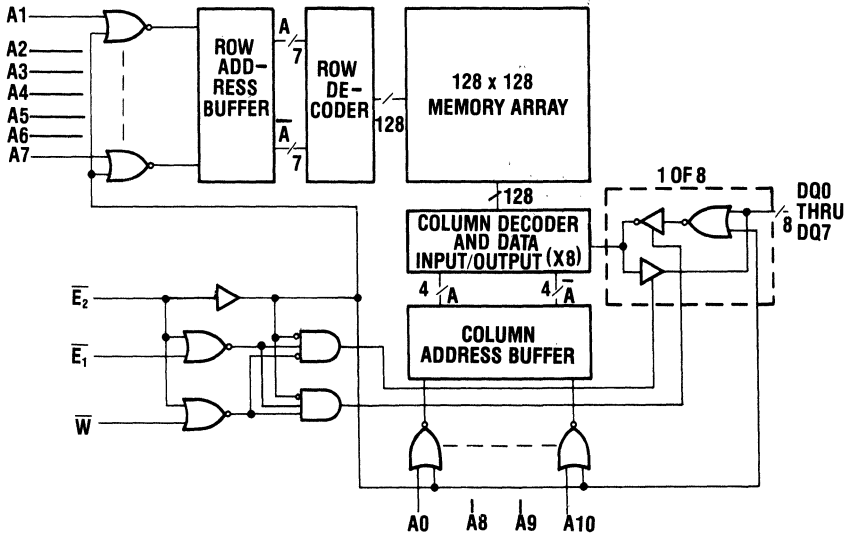


PIN NAMES	
A	Address Input
DQ	Data Input/Output
$\overline{E}_1\overline{E}_2$	Chip Enable
$\overline{W}$	Write Enable
NC	No Connect

TOP VIEW — LCC



Functional Diagram



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC - GND)	−0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)	Military (−2)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	−65°C to 150°C	Military (−2)	−55°C to +125°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		50	μA	$\overline{E_2}$ = VCC−0.2V OTHER INPUTS = 0.2V or VCC−0.2V
	ICC	Enabled Supply Current		70	mA	$\overline{E_1}$, $\overline{E_2}$ = VIL, IO = 0
	ICCOP	Operating Supply Current ②		70	mA	$\overline{E_1}$, $\overline{E_2}$ = VIL, IO = 0 f = 1 MHz
	ICCDR	Data Retention Supply Current		20	μA	IO = 0, VCC = 2.0 $\overline{E_1}$, $\overline{E_2}$ = VCC−0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−1.0	+1.0	μA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	−1.0	+1.0	μA	GND≤VIO≤VCC
	VIL	Input Low Voltage	−0.3	+0.8	V	
	VIH	Input High Voltage	2.2	VCC +0.3	V V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8	pF	VI = VCC or GND, f = 1 MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1 MHz
READ CYCLE	TAVAV	Read Cycle Time	70		ns	④
	TAVQV	Address Access Time		70	ns	④
	TE1LQV	$\overline{E_1}$ to Output Valid		40	ns	④
	TE2LQV	$\overline{E_2}$ to Output Valid		70	ns	④
	TE1LQX	$\overline{E_1}$ to Output in Low Z	0		ns	④
	TE2LQX	$\overline{E_2}$ to Output in Low Z	0		ns	④
	TE1HQZ	$\overline{E_1}$ Disable to Output in High Z		35	ns	④
	TE2HQZ	$\overline{E_2}$ Disable to Output in High Z		40	ns	④
	TAVQX	Output Hold from Address Change	5		ns	④
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	70		ns	④
	TE1LWH	$\overline{E_1}$ to End of Write	45		ns	④
	TE2LWH	$\overline{E_2}$ to End of Write	50		ns	④
	TAVWL	Address Setup Time	10		ns	④
	TAVWH	Address Valid to End of Write	65		ns	④
	TWLWH	Write Pulse Width	40		ns	④
	TWHAV	Write Recovery Time	10		ns	④
	TWLQZ	Write to Output in High Z		40	ns	④
	TDVWH	Data to Write Time Overlap	30		ns	④
	TWHDX	Data Hold from Write Time	15		ns	④
	TWHQX	Output Active from End of Write	0		ns	④

NOTES:
① All devices tested at worst case limits.
② Typical derating = 5mA/MHz increase in ICCOP; VI = VCC or GND.
③ Capacitance sampled and guaranteed - not 100% tested.
④ Input pulse levels: 0V to 3.0V Input and Output timing reference levels: 1.5V
Input rise and fall times: 5 ns Output load: 1TTL Gate and C_L = 100pF (including scope and jig)

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC - GND)	−0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)	Military (−2)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	−65°C to 150°C	Military (−2)	−55°C to +125°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		100	µA	$\overline{E_2}$ = VCC−0.2V OTHER INPUTS = 0.2V or VCC−0.2V
	ICC	Enabled Supply Current		70	mA	$\overline{E_1}$, $\overline{E_2}$ = VIL. IO = 0
	ICCOP	Operating Supply Current ②		70	mA	$\overline{E_1}$, $\overline{E_2}$ = VIL, IO = 0 f = 1 MHz
	ICCDR	Data Retention Supply Current		40	µA	IO = 0, VCC = 2.0 $\overline{E_1}$, $\overline{E_2}$ = VCC−0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−1.0	+1.0	µA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	−1.0	+1.0	µA	GND≤VIO≤VCC
	VIL	Input Low Voltage	−0.3	+0.8	V	
	VIH	Input High Voltage	2.2	VCC +0.3	V V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8	pF	VI = VCC or GND, f = 1 MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1 MHz
READ CYCLE	TAVAV	Read Cycle Time	90		ns	④
	TAVQV	Address Access Time		90	ns	④
	TE1LQV	$\overline{E_1}$ to Output Valid		70	ns	④
	TE2LQV	$\overline{E_2}$ to Output Valid		90	ns	④
	TE1LQX	$\overline{E_1}$ to Output in Low Z	0		ns	④
	TE2LQX	$\overline{E_2}$ to Output in Low Z	0		ns	④
	TE1HQZ	$\overline{E_1}$ Disable to Output in High Z		45	ns	④
	TE2HQZ	$\overline{E_2}$ Disable to Output in High Z		50	ns	④
	TAVQX	Output Hold from Address Change	5		ns	④
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	90		ns	④
	TE1LWH	$\overline{E_1}$ to End of Write	55		ns	④
	TE2LWH	$\overline{E_2}$ to End of Write	60		ns	④
	TAVWL	Address Setup Time	10		ns	④
	TAVWH	Address Valid to End of Write	80		ns	④
	TWLWH	Write Pulse Width	55		ns	④
	TWHAV	Write Recovery Time	10		ns	④
	TWLQZ	Write to Output in High Z		50	ns	④
	TDVWH	Data to Write Time Overlap	30		ns	④
	TWHDX	Data Hold from Write Time	15		ns	④
	TWHQX	Output Active from End of Write	0		ns	④

NOTES:
① All devices tested at worst case limits.
② Typical derating = 5mA/MHz increase in ICCOP; VI = VCC or GND.
③ Capacitance sampled and guaranteed - not 100% tested.
④ Input pulse levels: 0V to 3.0V Input and Output timing reference levels: 1.5V
Input rise and fall times: 5 ns Output load: 1TTL Gate and C_L = 100pF (including scope and jig)

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC - GND)	−0.3 to 8.0V	Operating Supply Voltage Military (−2)	4.5V to 5.5V
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)	Operating Temperature Military (−2)	−55°C to +125°C
Storage Temperature	−65°C to 150°C		

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
	ICCSB1	Standby Supply Current		1000	μA	$\overline{E_2}$ = VCC−0.2V OTHER INPUTS = 0.2V or VCC−0.2V
	ICC	Enabled Supply Current		70	mA	$\overline{E_1}$, $\overline{E_2}$ = VIL. IO = 0
	ICCOP	Operating Supply Current ②		70	mA	$\overline{E_1}$, $\overline{E_2}$ = VIL, IO = 0 f = 1 MHz
	ICCDR	Data Retention Supply Current		400	μA	IO = 0, VCC = 2.0 $\overline{E_1}$, $\overline{E_2}$ = VCC−0.3V
D.C.	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−5.0	+5.0	μA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	−5.0	+5.0	μA	GND≤VIO≤VCC
	VIL	Input Low Voltage	−0.3	+0.8	V	
	VIH	Input High Voltage	2.2	VCC +0.3	V V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8	pF	VI = VCC or GND, f = 1 MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1 MHz
	TAVAV	Read Cycle Time	120		ns	④
	TAVQV	Address Access Time		120	ns	④
	TE1LQV	$\overline{E_1}$ to Output Valid		100	ns	④
	TE2LQV	$\overline{E_2}$ to Output Valid		120	ns	④
READ CYCLE	TE1LQX	$\overline{E_1}$ to Output in Low Z	0		ns	④
	TE2LQX	$\overline{E_2}$ to Output in Low Z	0		ns	④
	TE1HQZ	$\overline{E_1}$ Disable to Output in High Z		45	ns	④
	TE2HQZ	$\overline{E_2}$ Disable to Output in High Z		50	ns	④
	TAVQX	Output Hold from Address Change	5		ns	④
	TAVAV	Write Cycle Time	120		ns	④
A.C.	TE1LWH	$\overline{E_1}$ to End of Write	65		ns	④
	TE2LWH	$\overline{E_2}$ to End of Write	70		ns	④
WRITE CYCLE	TAVWL	Address Setup Time	10		ns	④
	TAVWH	Address Valid to End of Write	105		ns	④
	TWLWH	Write Pulse Width	70		ns	④
	TWHAV	Write Recovery Time	10		ns	④
	TWLQZ	Write to Output in High Z		50	ns	④
	TDVWH	Data to Write Time Overlap	35		ns	④
	TWHDX	Data Hold from Write Time	15		ns	④
	TWHQX	Output Active from End of Write	0		ns	④

NOTES:
① All devices tested at worst case limits.
② Typical derating = 5mA/MHz increase in ICCOP; VI = VCC or GND.
③ Capacitance sampled and guaranteed - not 100% tested.
④ Input pulse levels: 0V to 3.0V Input and Output timing reference levels: 1.5V
Input rise and fall times: 5 ns Output load: 1TTL Gate and C_L = 100pF (including scope and jig)

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC - GND)	−0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)	Industrial (−9)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	−65°C to 150°C	Industrial (−9)	−40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		100	μA	$\overline{E_2}$ = VCC−0.2V OTHER INPUTS = 0.2V or VCC−0.2V
	ICC	Enabled Supply Current		70	mA	$\overline{E_1}$, $\overline{E_2}$ = VIL. IO = 0
	ICCOP	Operating Supply Current ②		70	mA	$\overline{E_1}$, $\overline{E_2}$ = VIL, IO = 0 f = 1 MHz
	ICCDR	Data Retention Supply Current		40	μA	IO = 0, VCC = 2.0 $\overline{E_1}$, $\overline{E_2}$ = VCC−0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−1.0	+1.0	μA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	−1.0	+1.0	μA	GND≤VIO≤VCC
	VIL	Input Low Voltage	−0.3	+0.8	V	
	VIH	Input High Voltage	2.4	VCC +0.3	V V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8	pF	VI = VCC or GND, f = 1 MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1 MHz
READ CYCLE	TAVAV	Read Cycle Time	55		ns	④
	TAVQV	Address Access Time		55	ns	④
	TE1LQV	$\overline{E_1}$ to Output Valid		35	ns	④
	TE2LQV	$\overline{E_2}$ to Output Valid		55	ns	④
	TE1LQX	$\overline{E_1}$ to Output in Low Z	0		ns	④
	TE2LQX	$\overline{E_2}$ to Output in Low Z	0		ns	④
	TE1HQZ	$\overline{E_1}$ Disable to Output in High Z		30	ns	④
	TE2HQZ	$\overline{E_2}$ Disable to Output in High Z		40	ns	④
	TAVQX	Output Hold from Address Change	5		ns	④
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	55		ns	④
	TE1LWH	$\overline{E_1}$ to End of Write	40		ns	④
	TE2LWH	$\overline{E_2}$ to End of Write	45		ns	④
	TAVWL	Address Setup Time	5		ns	④
	TAVWH	Address Valid to End of Write	50		ns	④
	TWLWH	Write Pulse Width	35		ns	④
	TWHAV	Write Recovery Time	10		ns	④
	TWLQZ	Write to Output in High Z		25	ns	④
	TDVWH	Data to Write Time Overlap	25		ns	④
	TWHDX	Data Hold from Write Time	15		ns	④
	TWHQX	Output Active from End of Write	0		ns	④

NOTES:
① All devices tested at worst case limits.
② Typical derating = 5mA/MHz increase in ICCOP; VI = VCC or GND.
③ Capacitance sampled and guaranteed − not 100% tested.
④ Input pulse levels: 0V to 3.0V Input and Output timing reference levels: 1.5V
Input rise and fall times: 5 ns Output load: 1TTL Gate and C_L = 100pF (including scope and jig)

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC - GND)	−0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)	Industrial (−9)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	−65°C to 150°C	Industrial (−9)	−40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
	ICCSB1	Standby Supply Current		50	µA	$\overline{E_2}$ = VCC−0.2V OTHER INPUTS = 0.2V or VCC−0.2V
	ICC	Enabled Supply Current		70	mA	$\overline{E_1}$, $\overline{E_2}$ = VIL. IO = 0
	ICCOP	Operating Supply Current ②		70	mA	$\overline{E_1}$, $\overline{E_2}$ = VIL, IO = 0 f = 1 MHz
	ICCDR	Data Retention Supply Current		20	µA	IO = 0, VCC = 2.0 $\overline{E_1}$, $\overline{E_2}$ = VCC−0.3V
D.C.	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−1.0	+1.0	µA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	−1.0	+1.0	µA	GND≤VIO≤VCC
	VIL	Input Low Voltage	−0.3	+0.8	V	
	VIH	Input High Voltage	2.2	VCC +0.3	V V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8	pF	VI = VCC or GND, f = 1 MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1 MHz
	TAVAV	Read Cycle Time	70		ns	④
	TAVQV	Address Access Time		70	ns	④
	TE1LQV	$\overline{E_1}$ to Output Valid		40	ns	④
	TE2LQV	$\overline{E_2}$ to Output Valid		70	ns	④
READ	TE1LQX	$\overline{E_1}$ to Output in Low Z	0		ns	④
CYCLE	TE2LQX	$\overline{E_2}$ to Output in Low Z	0		ns	④
	TE1HQZ	$\overline{E_1}$ Disable to Output in High Z		35	ns	④
	TE2HQZ	$\overline{E_2}$ Disable to Output in High Z		40	ns	④
	TAVQX	Output Hold from Address Change	5		ns	④
	TAVAV	Write Cycle Time	70		ns	④
A.C.	TE1LWH	$\overline{E_1}$ to End of Write	45		ns	④
	TE2LWH	$\overline{E_2}$ to End of Write	50		ns	④
WRITE	TAVWL	Address Setup Time	10		ns	④
CYCLE	TAVWH	Address Valid to End of Write	65		ns	④
	TWLWH	Write Pulse Width	40		ns	④
	TWHAV	Write Recovery Time	10		ns	④
	TWLQZ	Write to Output in High Z		40	ns	④
	TDVWH	Data to Write Time Overlap	30		ns	④
	TWHDX	Data Hold from Write Time	15		ns	④
	TWHQX	Output Active from End of Write	0		ns	④

NOTES:
① All devices tested at worst case limits.
② Typical derating = 5mA/MHz increase in ICCOP; VI = VCC or GND.
③ Capacitance sampled and guaranteed - not 100% tested.
④ Input pulse levels: 0V to 3.0V Input and Output timing reference levels: 1.5V
Input rise and fall times: 5 ns Output load: 1TTL Gate and C_L = 100pF (including scope and jig)

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC - GND)	−0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)	Industrial (−9)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	−65°C to 150°C	Industrial (−9)	−40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		100	μA	$\overline{E_2}$ = VCC−0.2V OTHER INPUTS = 0.2V or VCC−0.2V
	ICC	Enabled Supply Current		70	mA	$\overline{E_1}$, $\overline{E_2}$ = VIL. IO = 0
	ICCOP	Operating Supply Current ②		70	mA	$\overline{E_1}$, $\overline{E_2}$ = VIL, IO = 0 f = 1 MHz
	ICCDR	Data Retention Supply Current		40	μA	IO = 0, VCC = 2.0 $\overline{E_1}$, $\overline{E_2}$ = VCC−0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−1.0	+1.0	μA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	−1.0	+1.0	μA	GND≤VIO≤VCC
	VIL	Input Low Voltage	−0.3	+0.8	V	
	VIH	Input High Voltage	2.2	VCC +0.3	V V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8	pF	VI = VCC or GND, f = 1 MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1 MHz
READ CYCLE	TAVAV	Read Cycle Time	90		ns	④
	TAVQV	Address Access Time		90	ns	④
	TE1LQV	$\overline{E_1}$ to Output Valid		70	ns	④
	TE2LQV	$\overline{E_2}$ to Output Valid		90	ns	④
	TE1LQX	$\overline{E_1}$ to Output in Low Z	0		ns	④
	TE2LQX	$\overline{E_2}$ to Output in Low Z	0		ns	④
	TE1HQZ	$\overline{E_1}$ Disable to Output in High Z		45	ns	④
	TE2HQZ	$\overline{E_2}$ Disable to Output in High Z		50	ns	④
	TAVQX	Output Hold from Address Change	5		ns	④
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	90		ns	④
	TE1LWH	$\overline{E_1}$ to End of Write	55		ns	④
	TE2LWH	$\overline{E_2}$ to End of Write	60		ns	④
	TAVWL	Address Setup Time	10		ns	④
	TAVWH	Address Valid to End of Write	80		ns	④
	TWLWH	Write Pulse Width	55		ns	④
	TWHAV	Write Recovery Time	10		ns	④
	TWLQZ	Write to Output in High Z		50	ns	④
	TDVWH	Data to Write Time Overlap	30		ns	④
	TWHDX	Data Hold from Write Time	15		ns	④
	TWHQX	Output Active from End of Write	0		ns	④

NOTES:
① All devices tested at worst case limits.
② Typical derating = 5mA/MHz increase in ICCOP; VI = VCC or GND.
③ Capacitance sampled and guaranteed - not 100% tested.
④ Input pulse levels: 0V to 3.0V Input and Output timing reference levels: 1.5V
Input rise and fall times: 5 ns Output load: 1TTL Gate and C_L = 100pF (including scope and jig)

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC - GND)	−0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)	Industrial (−9)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	−65°C to 150°C	Industrial (−9)	−40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		1000	μA	$\overline{E_2}$ = VCC−0.2V OTHER INPUTS = 0.2V or VCC−0.2V
	ICC	Enabled Supply Current		70	mA	$\overline{E_1}$, $\overline{E_2}$ = VIL. IO = 0
	ICCOP	Operating Supply Current ②		70	mA	$\overline{E_1}$, $\overline{E_2}$ = VIL, IO = 0 f = 1 MHz
	ICCDR	Data Retention Supply Current		400	μA	IO = 0, VCC = 2.0 $\overline{E_1}$, $\overline{E_2}$ = VCC−0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−5.0	+5.0	μA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	−5.0	+5.0	μA	GND≤VIO≤VCC
	VIL	Input Low Voltage	−0.3	+0.8	V	
	VIH	Input High Voltage	2.2	VCC +0.3	V V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8	pF	VI = VCC or GND, f = 1 MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1 MHz
READ CYCLE	TAVAV	Read Cycle Time	90		ns	④
	TAVQV	Address Access Time		90	ns	④
	TE1LQV	$\overline{E_1}$ to Output Valid		70	ns	④
	TE2LQV	$\overline{E_2}$ to Output Valid		90	ns	④
	TE1LQX	$\overline{E_1}$ to Output in Low Z	0		ns	④
	TE2LQX	$\overline{E_2}$ to Output in Low Z	0		ns	④
	TE1HQZ	$\overline{E_1}$ Disable to Output in High Z		45	ns	④
	TE2HQZ	$\overline{E_2}$ Disable to Output in High Z		50	ns	④
	TAVQX	Output Hold from Address Change	5		ns	④
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	90		ns	④
	TE1LWH	$\overline{E_1}$ to End of Write	55		ns	④
	TE2LWH	$\overline{E_2}$ to End of Write	60		ns	④
	TAVWL	Address Setup Time	10		ns	④
	TAVWH	Address Valid to End of Write	80		ns	④
	TWLWH	Write Pulse Width	55		ns	④
	TWHAV	Write Recovery Time	10		ns	④
	TWLQZ	Write to Output in High Z		50	ns	④
	TDVWH	Data to Write Time Overlap	30		ns	④
	TWHDX	Data Hold from Write Time	15		ns	④
	TWHQX	Output Active from End of Write	0		ns	④

NOTES:
① All devices tested at worst case limits.
② Typical derating = 5mA/MHz increase in ICCOP; VI = VCC or GND.
③ Capacitance sampled and guaranteed - not 100% tested.
④ Input pulse levels: 0V to 3.0V Input and Output timing reference levels: 1.5V
Input rise and fall times: 5 ns Output load: 1TTL Gate and C_L = 100pF (including scope and jig)

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC - GND)	−0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)	Commercial (−5)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	−65°C to 150°C	Commercial (−5)	0°C to +70°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		100	μA	$\overline{E_2}$ = VCC−0.2V OTHER INPUTS = 0.2V or VCC−0.2V
	ICC	Enabled Supply Current		70	mA	$\overline{E_1}$, $\overline{E_2}$ = VIL. IO = 0
	ICCOP	Operating Supply Current ②		70	mA	$\overline{E_1}$, $\overline{E_2}$ = VIL, IO = 0 f = 1 MHz
	ICCDR	Data Retention Supply Current		40	μA	IO = 0, VCC = 2.0 $\overline{E_1}$, $\overline{E_2}$ = VCC−0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−1.0	+1.0	μA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	−1.0	+1.0	μA	GND≤VIO≤VCC
	VIL	Input Low Voltage	−0.3	+0.8	V	
	VIH	Input High Voltage	2.4	VCC	V	
				+0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8	pF	VI = VCC or GND, f = 1 MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1 MHz
READ CYCLE	TAVAV	Read Cycle Time	55		ns	④
	TAVQV	Address Access Time		55	ns	④
	TE1LQV	$\overline{E_1}$ to Output Valid		35	ns	④
	TE2LQV	$\overline{E_2}$ to Output Valid		55	ns	④
	TE1LQX	$\overline{E_1}$ to Output in Low Z	0		ns	④
	TE2LQX	$\overline{E_2}$ to Output in Low Z	0		ns	④
	TE1HQZ	$\overline{E_1}$ Disable to Output in High Z		30	ns	④
	TE2HQZ	$\overline{E_2}$ Disable to Output in High Z		40	ns	④
	TAVQX	Output Hold from Address Change	5		ns	④
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	55		ns	④
	TE1LWH	$\overline{E_1}$ to End of Write	40		ns	④
	TE2LWH	$\overline{E_2}$ to End of Write	45		ns	④
	TAVWL	Address Setup Time	5		ns	④
	TAVWH	Address Valid to End of Write	50		ns	④
	TWLWH	Write Pulse Width	35		ns	④
	TWHAV	Write Recovery Time	10		ns	④
	TWLQZ	Write to Output in High Z		25	ns	④
	TDVWH	Data to Write Time Overlap	25		ns	④
	TWHDX	Data Hold from Write Time	15		ns	④
	TWHQX	Output Active from End of Write	0		ns	④

NOTES:
① All devices tested at worst case limits.
② Typical derating = 5mA/MHz increase in ICCOP; VI = VCC or GND.
③ Capacitance sampled and guaranteed - not 100% tested.
④ Input pulse levels: 0V to 3.0V Input and Output timing reference levels: 1.5V
Input rise and fall times: 5 ns Output load: 1TTL Gate and C_L = 100pF (including scope and jig)

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC - GND)	−0.3 to 8.0V	Operating Supply Voltage Commercial (−5)	4.5V to 5.5V
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)	Operating Temperature Commercial (−5)	0°C to +70°C
Storage Temperature	−65°C to 150°C		

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		50	μA	$\overline{E_2}$ = VCC−0.2V OTHER INPUTS = 0.2V or VCC−0.2V
	ICC	Enabled Supply Current		70	mA	$\overline{E_1}$, $\overline{E_2}$ = VIL. IO = 0
	ICCOP	Operating Supply Current ②		70	mA	$\overline{E_1}$, $\overline{E_2}$ = VIL, IO = 0 f = 1 MHz
	ICCDR	Data Retention Supply Current		20	μA	IO = 0, VCC = 2.0 $\overline{E_1}$, $\overline{E_2}$ = VCC−0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−1.0	+1.0	μA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	−1.0	+1.0	μA	GND≤VIO≤VCC
	VIL	Input Low Voltage	−0.3	+0.8	V	
	VIH	Input High Voltage	2.2	VCC +0.3	V V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8	pF	VI = VCC or GND, f = 1 MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1 MHz
READ CYCLE	TAVAV	Read Cycle Time	70		ns	④
	TAVQV	Address Access Time		70	ns	④
	TE1LQV	$\overline{E_1}$ to Output Valid		40	ns	④
	TE2LQV	$\overline{E_2}$ to Output Valid		70	ns	④
	TE1LQX	$\overline{E_1}$ to Output in Low Z	0		ns	④
	TE2LQX	$\overline{E_2}$ to Output in Low Z	0		ns	④
	TE1HQZ	$\overline{E_1}$ Disable to Output in High Z		35	ns	④
	TE2HQZ	$\overline{E_2}$ Disable to Output in High Z		40	ns	④
	TAVQX	Output Hold from Address Change	5		ns	④
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	70		ns	④
	TE1LWH	$\overline{E_1}$ to End of Write	45		ns	④
	TE2LWH	$\overline{E_2}$ to End of Write	50		ns	④
	TAVWL	Address Setup Time	10		ns	④
	TAVWH	Address Valid to End of Write	65		ns	④
	TWLWH	Write Pulse Width	40		ns	④
	TWHAV	Write Recovery Time	10		ns	④
	TWLQZ	Write to Output in High Z		40	ns	④
	TDVWH	Data to Write Time Overlap	30		ns	④
	TWHDX	Data Hold from Write Time	15		ns	④
	TWHQX	Output Active from End of Write	0		ns	④

NOTES:
① All devices tested at worst case limits.
② Typical derating = 5mA/MHz increase in ICCOP; VI = VCC or GND.
③ Capacitance sampled and guaranteed – not 100% tested.
④ Input pulse levels: 0V to 3.0V Input and Output timing reference levels: 1.5V
Input rise and fall times: 5 ns Output load: 1TTL Gate and C_L = 100pF (including scope and jig)

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC - GND)	−0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)	Commercial (−5)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	−65°C to 150°C	Commercial (−5)	0°C to +70°C

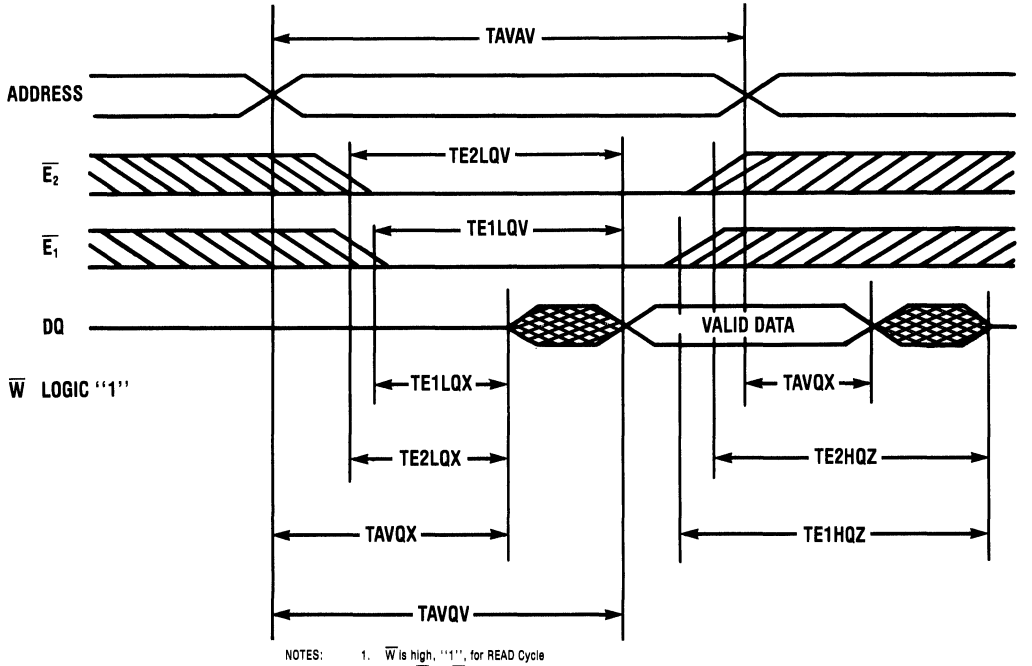
**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		100	μA	$\overline{E_2}$ = VCC−0.2V OTHER INPUTS = 0.2V or VCC−0.2V
	ICC	Enabled Supply Current		70	mA	$\overline{E_1}$, $\overline{E_2}$ = VIL. IO = 0
	ICCOP	Operating Supply Current ②		70	mA	$\overline{E_1}$, $\overline{E_2}$ = VIL, IO = 0 f = 1 MHz
	ICCDR	Data Retention Supply Current		40	μA	IO = 0, VCC = 2.0 $\overline{E_1}$, $\overline{E_2}$ = VCC−0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−1.0	+1.0	μA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	−1.0	+1.0	μA	GND≤VIO≤VCC
	VIL	Input Low Voltage	−0.3	+0.8	V	
	VIH	Input High Voltage	2.2	VCC +0.3	V V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8	pF	VI = VCC or GND, f = 1 MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1 MHz
READ CYCLE	TAVAV	Read Cycle Time	90		ns	④
	TAVQV	Address Access Time		90	ns	④
	TE1LQV	$\overline{E_1}$ to Output Valid		70	ns	④
	TE2LQV	$\overline{E_2}$ to Output Valid		90	ns	④
	TE1LQX	$\overline{E_1}$ to Output in Low Z	0		ns	④
	TE2LQX	$\overline{E_2}$ to Output in Low Z	0		ns	④
	TE1HQZ	$\overline{E_1}$ Disable to Output in High Z		45	ns	④
	TE2HQZ	$\overline{E_2}$ Disable to Output in High Z		50	ns	④
	TAVQX	Output Hold from Address Change	5		ns	④
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	90		ns	④
	TE1LWH	$\overline{E_1}$ to End of Write	55		ns	④
	TE2LWH	$\overline{E_2}$ to End of Write	60		ns	④
	TAVWL	Address Setup Time	10		ns	④
	TAVWH	Address Valid to End of Write	80		ns	④
	TWLWH	Write Pulse Width	55		ns	④
	TWHAV	Write Recovery Time	10		ns	④
	TWLQZ	Write to Output in High Z		50	ns	④
	TDVWH	Data to Write Time Overlap	30		ns	④
	TWHDX	Data Hold from Write Time	15		ns	④
	TWHQX	Output Active from End of Write	0		ns	④

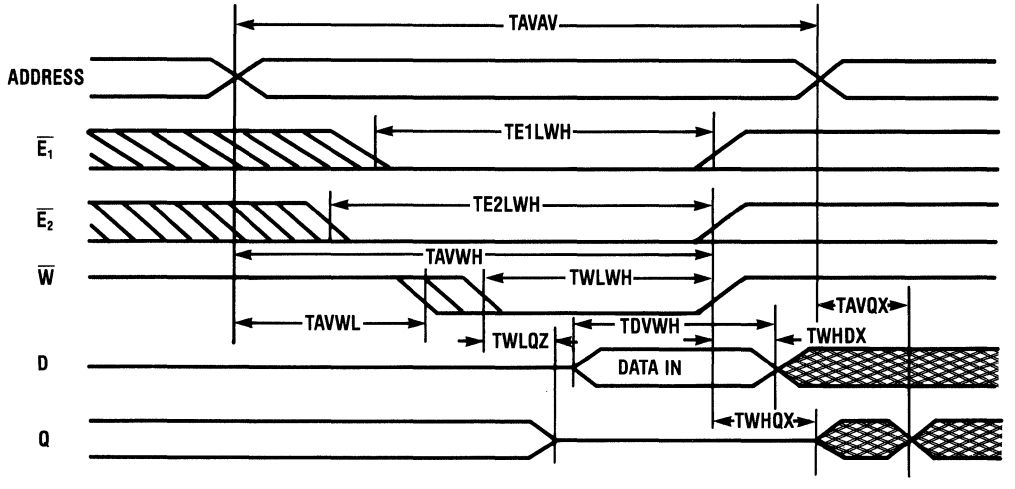
NOTES:
① All devices tested at worst case limits.
② Typical derating = 5mA/MHz increase in ICCOP; VI = VCC or GND.
③ Capacitance sampled and guaranteed - not 100% tested.
④ Input pulse levels: OV to 3.0V Input and Output timing reference levels: 1.5V
Input rise and fall times: 5 ns Output load: 1TTL Gate and C_L = 100pF (including scope and jig)

Read Cycle



NOTES:
1. $\overline{W}$ is high, "1", for READ Cycle
2. When $\overline{E}_1$ and $\overline{E}_2$ are low, "0", address inputs must not be in high impedance state.
3. $\overline{E}_2$="1" deselects the part and gates the inputs off. The HM-65172 will consume ICCSB1 regardless of input conditions within the absolute maximum ratings.

Write Cycle



Writing data into the memory requires an overlap of $\overline{E}_1$, $\overline{E}_2$ and $\overline{W}$. When $\overline{E}_1$ or $\overline{E}_2$ transition low simultaneously with the $\overline{W}$ low transition, or after $\overline{W}$ transitions low, the outputs will remain in a high impedance state. After $\overline{W}$ transitions high and if $\overline{E}_1$ and $\overline{E}_2$ are low, the DQ pins are in the output state. Care must be taken when applying data input at this time. Data of opposite phase must not be applied when the DQ lines are in the output state. Also, during TWLQZ, the DQ pins are in the output state and data of opposite phase must not be applied.

Truth Table

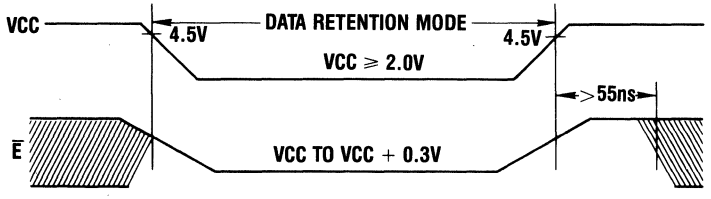
$\overline{E_2}$	$\overline{E_1}$	$\overline{W}$	D	Q	ICC	MODE
H	X	X	Z	Z	ISB	$\overline{E_2}$ = VIH; Deselect
H	X	X	Z	Z	ISB1	$\overline{E_2} \geq$ VCC = 0.3; Deselect
L	L	H	Z	VALID	ICC	Read
L	L	L	VALID	Z	ICC	Write
X	H	X	Z	Z	ICC	Deselect

Low Voltage Data Retention

Harris CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E_2}$) must be held high during data retention; within VCC to VCC + 0.3V.
2. On RAMs which have two chip enables, one of the enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. Inputs which are to be held high, must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
4. The RAM can begin operation > 55ns after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



16K x 1 Asynchronous CMOS Static RAM

JULY 1983 **Preview**

Features

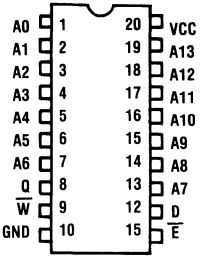
- LOW STANDBY CURRENT — 50 μA
- LOW OPERATING CURRENT — 60 mA
- FAST ADDRESS ACCESS TIME — 45/55/70 ns
- LOW VOLTAGE DATA RETENTION @ 2.0V
- CMOS/TTL COMPATIBLE INPUTS AND OUTPUTS
- JEDEC APPROVED PINOUT
- EQUAL CYCLE AND ACCESS TIMES
- NO CLOCKS OR STROBES REQUIRED
- SINGLE 5 VOLT SUPPLY
- GATED INPUTS—NO PULL-UP OR PULL-DOWN RESISTORS REQUIRED
- WIDE TEMPERATURE RANGE — −55°C to +125°C
- EASY MICROPROCESSOR INTERFACING

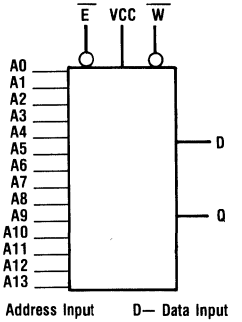
Description

The HM-65262 is a CMOS 16384 x 1 Static Random Access Memory manufactured using Harris' advanced SAJI-VI process. The device utilizes asynchronous circuit design for fast cycle time and ease of use. The pinout is the JEDEC 20-pin, 0.300-inch wide standard, providing high board-level packing density. Gated inputs lower operating current and also eliminate the need for pull-up or pull-down resistors.

Pinouts

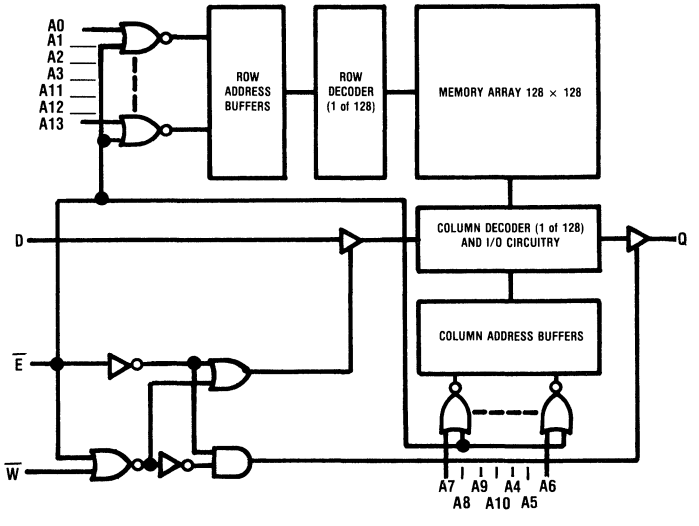
TOP VIEW





A— Address Input
E— Chip Enable
W— Write Enable
D— Data Input
Q— Data Output

Functional Diagram



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

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HARRIS

HM-6564

8K x 8, 16K x 4 CMOS RAM

Features

- LOW POWER STANDBY — 4mW MAX
- LOW POWER OPERATION — 280mW/MHz MAX
- DATA RETENTION — 2.0V MIN
- TTL COMPATIBLE IN/OUT
- THREE STATE OUTPUTS
- FAST ACCESS TIME — 350ns MAX
- FULL MILITARY TEMPERATURE AVAILABLE — -55°C to 125°C
- INDUSTRIAL TEMPERATURE STANDARD — -40°C to 85°C
- COMMERCIAL TEMPERATURE AVAILABLE — 0°C to 75°C
- ON CHIP ADDRESS REGISTERS
- ORGANIZABLE 8K x 8 or 16K x 4
- 40 PIN DIP PINOUT - 2.000" x 0.900"

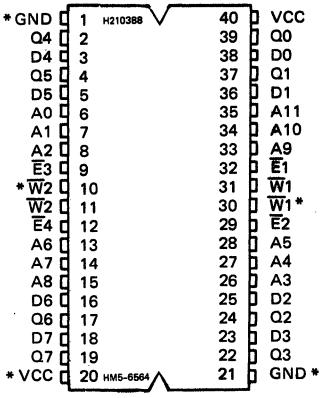
Description

The HM-6564 is a 64K bit CMOS RAM. It consists of 16 HM4-6504 4K x 1 CMOS RAMs, in leadless carriers, mounted on a ceramic substrate. The HM-6564 is configured as an extra wide, standard length 40 pin DIP. The memory appears to the system as an array of 16 4K x 1 static RAMs. The array is organized as two 8K by 4 blocks of RAM sharing only the address bus. The data inputs, data outputs, chip enables and write enables are separate for each block of RAM. This allows the user to organize the HM-6564 RAM as either an 8K by 8 or a 16K by 4 array. The HM-6564 also contains decoupling capacitors to reduce noise and to minimize the need for additional external decoupling.

This 64K memory provides a unique blend of low power CMOS semiconductor technology and advanced packaging techniques. The HM-6564 is intended for use in any application where a large amount of RAM is needed, and where power consumption and board space are prime concerns. The guaranteed low voltage data retention characteristics allow easy implementation of non-volatile read/write memory by using very small batteries mounted directly on the memory circuit board. Example applications include digital avionic instrumentation, remote data acquisition, and portable or hand held digital communications devices.

Pinout

TOP VIEW

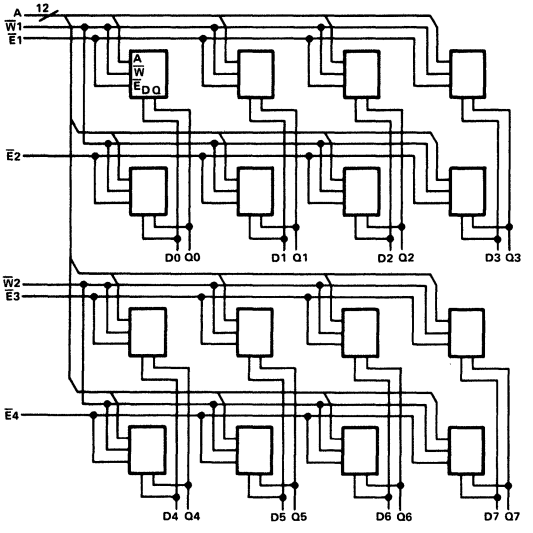


***NOTES:**

Pins 20 and 40 (VCC) are internally connected. Similarly pins 1 and 21 (Ground) are connected. The user is advised to connect all four VCC pins and Ground pins to his board busses. This will improve power distribution across the array and will enhance decoupling.

Pin 10 is internally connected to pin 11, and pin 30 is connected to pin 31.

Functional Diagram



To Organize 8K x 8:

Connect:	$\overline{E}1$ with $\overline{E}3$	(Pins 9 + 32)
	$\overline{E}2$ with $\overline{E}4$	(Pins 12 + 29)
	$\overline{W}1$ with $\overline{W}2$	(Pins 11 +31)

To Organize 16K x 4:

Connect:	Q0 with Q4	(Pins 2 + 39)
	D0 with D4	(Pins 3 + 38)
	Q1 with Q5	(Pins 4 + 37)
	D1 with D5	(Pins 5 + 36)
	D2 with D6	(Pins 16 +25)
	Q2 with Q6	(Pins 17 + 24)
	D3 with D7	(Pins 18 + 23)
	Q3 with Q7	(Pins 19 + 22)
Optional	$\overline{W}1$ may be common with $\overline{W}2$	(Pins 11 + 31)

Concerns for Proper Operation of Chip Enables:

The transition between blocks of RAM requires a change in the chip enable being used. When operating in the 8K x 8 mode, use the chip enables as if there were only two, $\overline{E}1$ and $\overline{E}2$. In the 16K x 4 mode, all chip enables must be treated separately. Transitions between chip enables must be treated with the same timing constraints that apply to any one chip enable. All chip enables must be high at least one chip enable high time (TEHEL) before any chip enable can fall. More than one chip enable low simultaneously, for devices whose outputs are tied common either internally or externally, is an illegal input condition and must be avoided.

Printed Circuit Board Mounting:

The leadless chip carrier packages used in the HM-6564 have conductive lids. These lids are electrically floating, not connected to VCC or GND. The designer should be aware of the possibility that the carriers on the bottom side could short conductors below if pressed completely down against the surface of the circuit board. The pins on the package are designed with a standoff feature to help prevent the leadless carriers from touching the circuit board surface.

Board Size Tradeoffs

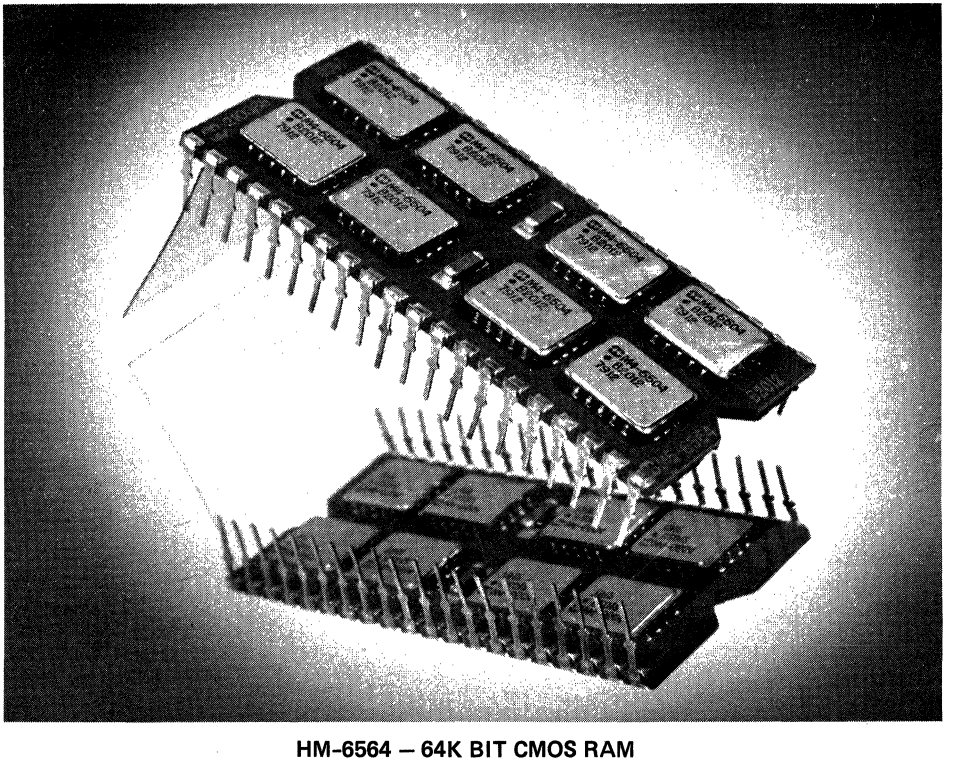
Printed circuit board real estate is a costly commodity. Actual board costs depend on layout tolerances, density, complexity, number of layers, choice of board material, and other factors.

The following table compares board space for 16 standard DIP 4K RAMs to the HM-6564 RAM array. Both fine line, close tolerance layout and standard "easy" layout board sizes are shown in the comparison.

64K ARRAY OF 16 4K RAMs ON A PC BOARD vs. THE HM-6564

PACKAGE	CIRCUIT SUBSTRATE	SIZE
18 Pin DIP	Standard Two Sided PCB	12 to 15 sq. in.
18 Pin DIP	Fine Line or Multilayer PCB	9 to 11 sq. in.
18 Pin Leadless Carrier	Multilayer Alumina Substrate	3 to 5 sq. in.
HM5-6564	Two Sided Mounting Multilayer Alumina Substrate	2 sq. in.

The cost of semiconductor circuits decline with time. If actual costs were included, they would be out of date in a very short time. We urge you to contact your local Harris office or sales representative for accurate pricing allowing cost tradeoff analysis. In your cost analysis, also consider the advantages of a lighter, smaller overall package for your system. Consider how much more valuable your system will be when the memory array size is decreased to about 1/6 of normal size.



HM-6564 – 64K BIT CMOS RAM

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage - (VCC - GND)	-0.3V to +8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Military (-2)/Industrial (-9)	+4.5V to +5.5V
Storage Temperature	-65°C to +150°C	Operating Temperature	
		Military (-2)	-55°C to +125°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		800	100	µA	IO = 0 VI = VCC or GND
	ICCOP1	Operating Supply Current (8K x 8) ②		56		mA	$\overline{E}$ =1MHz, IO = 0 VI = VCC or GND
	ICCOP2	Operating Supply Current (16K x 4) ②		28		mA	$\overline{E}$= 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		400	48	µA	IO = 0, VCC = 2.0, VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0			V	
	IIA	Address Input Leakage	-20	+20		µA	GND≤VI≤VCC
	IID1	Data Input Leakage (8K x 8)	-3	+3		µA	GND≤VI≤VCC
	IID2	Data Input Leakage (16K x 4)	-5	+5		µA	GND≤VI≤VCC
	IIE1	Enable Input Leakage (8K x 8)	-10	+10		µA	GND≤VI≤VCC
	IIE2	Enable Input Leakage (16K x 4)	-5	+5		µA	GND≤VI≤VCC
	IIW	Write Enable Input Leakage (Each)	-10	+10		µA	GND≤VI≤VCC
	IOZ1	Output Leakage (8K x 8)	-5	+5		µA	GND≤VO≤VCC
	IOZ2	Output Leakage (16K x 4)	-10	+10		µA	GND≤VO≤VCC
	VIL	Input Low Voltage	-0.3	0.8		V	
	VIH	Input High Voltage	VCC-2.0	VCC+0.3		V	
	VOL	Output Low Voltage		0.4		V	IO = 2.0mA
	VOH	Output High Voltage	2.4			V	IO = -1.0mA
	CIA	Address Input Capacitance ③		200		pF	f = 1MHz, VI = VCC or GND
	CID1	Data Input Capacitance (8K x 8) ③		50		pF	f = 1MHz, VI = VCC or GND
	CID2	Data Input Capacitance (16K x 4) ③		100		pF	f = 1MHz, VI = VCC or GND
	CIE1	Enable Input Capacitance (8K x 8) ③		160		pF	f = 1MHz, VI = VCC or GND
	CIE2	Enable Input Capacitance (16K x 4) ③		80		pF	f = 1MHz, VI = VCC or GND
	CIW	Write Enable Input Capacitance (Each) ③		100		pF	f = 1MHz, VI = VCC or GND
	CO1	Output Capacitance (8K x 8) ③		50		pF	f = 1MHz, VO = VCC or GND
	CO2	Output Capacitance (16K x 4) ③		100		pF	f = 1MHz, VO = VCC or GND
	CVCC	Decoupling Capacitance	.25			µF	f = 1MHz

NOTES:

① This value is guaranteed and tested at 25°C.

② Operating supply current is proportional to operating frequency. ICCOP is specified at an operating frequency of 1MHz, indicating repetitive accessing at a 1µs rate. Operation at slower rates will decrease ICCOP proportionally.

③ Capacitance sampled and guaranteed — not 100% tested.

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage - (VCC - GND)	-0.3V to +8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Industrial (-9)	+4.5 to +5.5V
Storage Temperature	-65°C to +150°C	Operating Temperature	
		Industrial (-9)	-40°C to +85°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		800	48	µA	IO = 0 VI = VCC or GND
	ICCOP1	Operating Supply Current (8K x 8) ②		56		mA	$\overline{E}$ = 1MHz, IO = 0 VI = VCC or GND
	ICCOP2	Operating Supply Current (16K x 4) ②		28		mA	$\overline{E}$ = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		400	32	µA	IO = 0, VCC = 2.0, VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0			V	
	IIA	Address Input Leakage	-20	+20		µA	GND ≤ VI ≤ VCC
	IID1	Data Input Leakage (8K x 8)	-3	+3		µA	GND ≤ VI ≤ VCC
	IID2	Data Input Leakage (16K x 4)	-5	+5		µA	GND ≤ VI ≤ VCC
	IIE1	Enable Input Leakage (8K x 8)	-10	+10		µA	GND ≤ VI ≤ VCC
	IIE2	Enable Input Leakage (16K x 4)	-5	+5		µA	GND ≤ VI ≤ VCC
	IIW	Write Enable Input Leakage (Each)	-10	+10		µA	GND ≤ VI ≤ VCC
	IOZ1	Output Leakage (8K x 8)	-5	+5		µA	GND ≤ VO ≤ VCC
	IOZ2	Output Leakage (16K x 4)	-10	+10		µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8		V	
	VIH	Input High Voltage	VCC-2.0	VCC+0.3		V	
	VOL	Output Low Voltage		0.4		V	IO = 2.0mA
	VOH	Output High Voltage	2.4			V	IO = -1.0mA
	CIA	Address Input Capacitance ③		200		pF	f = 1MHz, VI = VCC or GND
	CID1	Data Input Capacitance (8K x 8) ③		50		pF	f = 1MHz, VI = VCC or GND
	CID2	Data Input Capacitance (16K x 4) ③		100		pF	f = 1MHz, VI = VCC or GND
	CIE1	Enable Input Capacitance (8K x 8) ③		160		pF	f = 1MHz, VI = VCC or GND
	CIE2	Enable Input Capacitance (16K x 4) ③		80		pF	f = 1MHz, VI = VCC or GND
	CIW	Write Enable Input Capacitance (Each) ③		100		pF	f = 1MHz, VI = VCC or GND
	CO1	Output Capacitance (8K x 8) ③		50		pF	f = 1MHz, VO = VCC or GND
	CO2	Output Capacitance (16K x 4) ③		100		pF	f = 1MHz, VO = VCC or GND
	CVCC	Decoupling Capacitance	.25			µF	f = 1MHz

NOTES:

① This value is guaranteed and tested at 25°C.

② Operating supply current is proportional to operating frequency. ICCOP is specified at an operating frequency of 1MHz, indicating repetitive accessing at a 1µs rate. Operation at slower rates will decrease ICCOP proportionally.

③ Capacitance sampled and guaranteed — not 100% tested.

ELECTRICAL CHARACTERISTICS

A.C.

SYMBOL	PARAMETER	TEMP & VCC = OPERATING RANGE MIN	TEMP & VCC = OPERATING RANGE MAX	UNITS	TEST CONDITIONS
TELQV	Chip Enable Access		350	ns	④
TAVQV	Address Access (TAVQV=TELQV+TAVEL)		400	ns	④
TELQX	Output Enable	20	120	ns	④
TEHQZ	Output Disable		120	ns	④
TELEL	Read or Write Cycle	480		ns	④
TELEH	Chip Enable Low	350		ns	④
TEHEL	Chip Enable High	130		ns	④
TAVEL	Address Setup	50		ns	④
TELAX	Address Hold	50		ns	④
TWLWH	Write Enable Low	150		ns	④
TWLEH	Write Enable Setup	250		ns	④
TWLEL	Early Write Setup (Write Mode)	10		ns	④
TWHEL	Write Enable Read Setup	10		ns	④
TELWH	Early Write Hold (Write Mode)	100		ns	④
TDVWL	Data Setup	10		ns	④
TDVEL	Early Write Data Setup	10		ns	④
TWLDX	Data Hold	100		ns	④
TELDX	Early Write Data Hold	100		ns	④
TQVWL	Data Valid to Write (Read-Modify-Write)	0		ns	④

NOTES:

④ AC Test Conditions:
Inputs - Trise = Tfall $\leq$ 20ns.
Outputs - CLOAD = 100pF
Timing measured at 1.5V reference level.

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage - (VCC - GND)	-0.3V to +8.0V	Operating Supply Voltage Commercial (-5)	+4.5 to +5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Operating Temperature Commercial (-5)	0°C to +70°C
Storage Temperature	-65°C to +150°C		

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C VCC = 5.0V ① MAX	UNITS	TEST CONDITIONS
	ICCSB	Standby Supply Current		5.6	0.80	mA	IO = 0, VI = VCC or GND
	ICCOP1	Operating Supply Current (8K x 8) ②		60		mA	$\overline{E}$ = 1MHz, IO = 0 VI = VCC or GND
	ICCOP2	Operating Supply Current (16K x 4) ②		30		mA	$\overline{E}$ = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Curr.		3.2	0.48	mA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply V.	2.0			V	
	IIA	Address Input Leakage	-20	+20		µA	GND≤VI≤VCC
	IID1	Data Input Leakage (8K x 8)	-3	+3		µA	GND≤VI≤VCC
	IID2	Data Input Leakage (16K x 4)	-5	+5		µA	GND≤VI≤VCC
	IIE1	Enable Input Leakage (8K x 8)	-10	+10		µA	GND≤VI≤VCC
	IIE2	Enable Input Leakage (16K x 4)	-5	+5		µA	GND≤VI≤VCC
	IIW	Write Enable Input Leakage (Each)	-10	+10		µA	GND≤VI≤VCC
D.C.	IOZ1	Output Leakage (8K x 8)	-5	+5		µA	GND≤VO≤VCC
	IOZ2	Output Leakage (16K x 4)	-10	+10		µA	GND≤VO≤VCC
	VIL	Input Low Voltage	-0.3	0.8		V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3		V	
	VOL	Output Low Voltage		0.4		V	IO = 1.6mA
	VOH	Output High Voltage	2.4			V	IO = -0.4mA
	CIA	Address Input Capacitance ③		200		pF	f = 1MHz, VI = VCC or GND
	CID1	Data Input Capacitance (8K x 8) ③		50		pF	f = 1MHz, VI = VCC or GND
	CID2	Data Input Capacitance (16K x 4) ③		100		pF	f = 1MHz, VI = VCC or GND
	CIE1	Enable Input Capacitance (8K x 8) ③		160		pF	f = 1MHz, VI = VCC or GND
	CIE2	Enable Input Capacitance (16K x 4) ③		80		pF	f = 1MHz, VI = VCC or GND
	CIW	Write Input Capacitance (Each) ③		100		pF	f = 1MHz, VI = VCC or GND
	CO1	Output Capacitance (8K x 8) ③		50		pF	f = 1MHz, VO = VCC or GND
	CO2	Output Capacitance (16K x 4) ③		100		pF	f = 1MHz, VO = VCC or GND
	CVCC	Decoupling Capacitance	.25			µF	f = 1MHz

NOTES:

① This value is guaranteed and tested at 25°C.

② Operating supply current is proportional to operating frequency. ICCOP is specified at an operating frequency of 1MHz, indicating repetitive accessing at a 1µs rate. Operation at slower rates will decrease ICCOP proportionally.

③ Capacitance sampled and guaranteed — not 100% tested.

ELECTRICAL CHARACTERISTICS

A.C.

SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDTIONS
TELQV	Chip Enable Access		450	ns	④
TAVQV	Address Access (TAVQV=TELQV+TAVEL)		500	ns	④
TELQX	Output Enable	20	150	ns	④
TEHQZ	Output Disable		150	ns	④
TELEL	Read or Write Cycle	600		ns	④
TELEH	Chip Enable Low	450		ns	④
TEHEL	Chip Enable High	150		ns	④
TAVEL	Address Setup	50		ns	④
TELAX	Address Hold	50		ns	④
TWLWH	Write Enable Low	150		ns	④
TWLEH	Write Enable Setup	250		ns	④
TWLEL	Early Write Setup (Write Mode)	10		ns	④
TWHEL	Write Enable Read Setup	10		ns	④
TELWH	Early Write Hold (Write Mode)	100		ns	④
TDVWL	Data Setup	10		ns	④
TDVEL	Early Write Data Setup	10		ns	④
TWLDX	Data Hold	100		ns	④
TELDX	Early Write Data Hold	100		ns	④
TQVWL	Data Valid to Write (Ready-Modify-Write)	0		ns	④

NOTES:

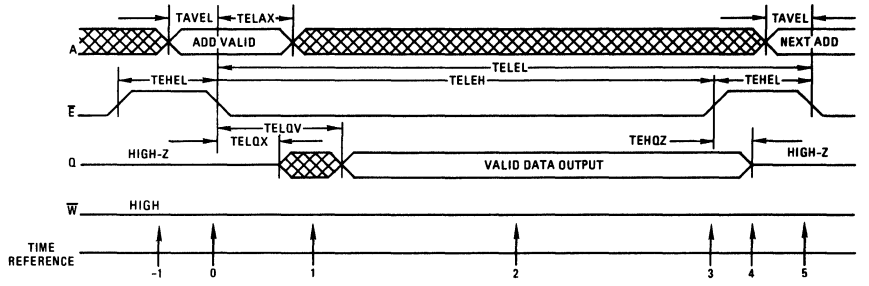
④ AC Test Conditions:

Inputs – Trise = Tfall $\leq$ 20ns.

Outputs – CLOAD = 100pF.

Timing measured at 1.5V reference level.

Read Cycle

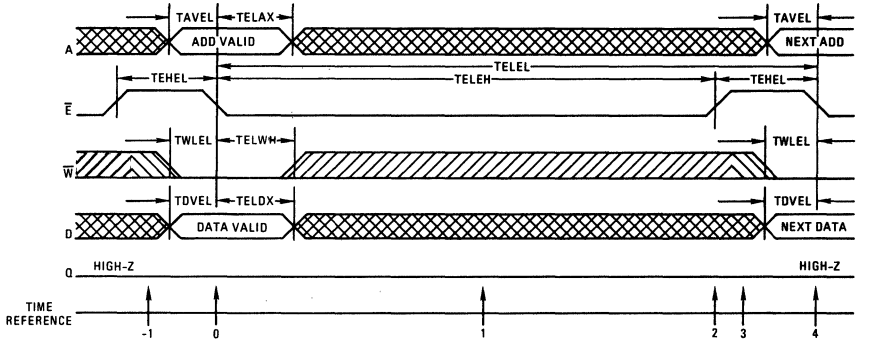


TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	OUTPUT Q	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and ready the RAM for the next memory cycle (T = 4).

Early Write Cycle

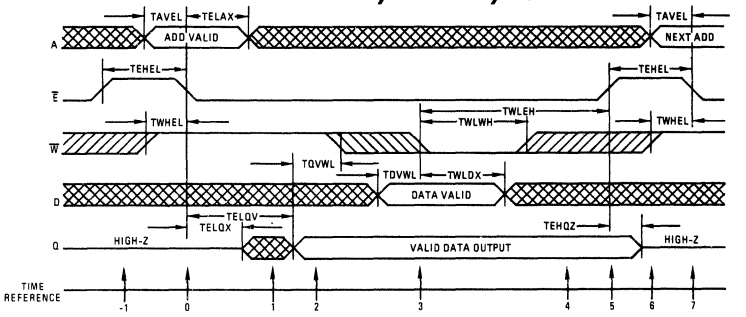


TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	L	V	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	X	X	X	Z	WRITE IN PROGRESS INTERNALLY
2	↗	X	X	X	Z	WRITE COMPLETED
3	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
4	↘	L	V	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls determines the state of the output buffer for that cycle. Since $\overline{W}$ is low when $\overline{E}$ falls, the output buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; therefore data set up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state the output buffer disables and all signals are unlatched. The device is now ready for the next cycle.

Read Modify Write Cycle

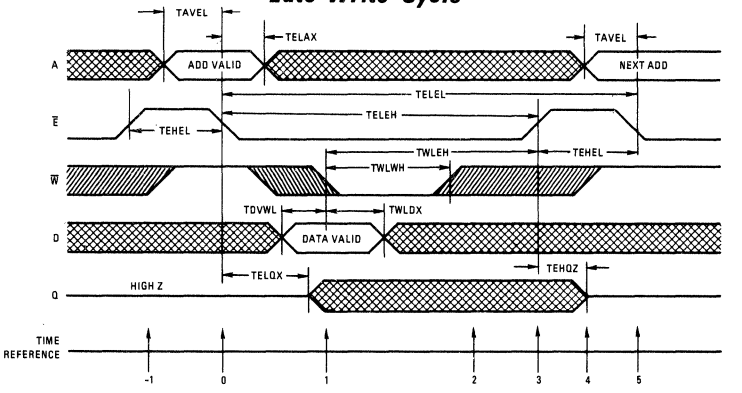


TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	V	X	Z	CYCLE BEGINS, ADDRESS ARE LATCHED
1	L	H	X	X	X	OUTPUT ENABLED
2	L	H	X	X	V	OUTPUT VALID, READ AND MODIFY TIME
3	L	↘	X	V	V	WRITE BEGINS, DATA IS LATCHED
4	L	X	X	X	V	WRITE IN PROGRESS INTERNALLY
5	↗	X	X	X	V	WRITE COMPLETED
6	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↘	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The read modify write cycle begins as all other cycles on the falling edge of Ē (T= 0). The W̄ line should be high at (T = 0) in order to latch the output buffers in the active state. During (T = 1) the output will be active but not valid until (T = 2). On the falling edge of the W̄ (T = 3) the data present at the output and input are latched. The W signal also latches itself on its low going edge. All input signals excluding Ē have been latched and have no further effect on the RAM. The rising edge of Ē (T = 5) completes the write portion of the cycle and unlatches all inputs and the output. The output goes to a high impedance and the RAM is ready for the next cycle.

Late Write Cycle



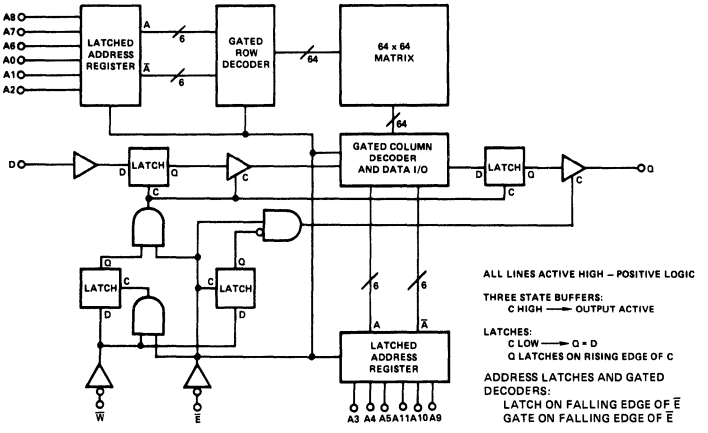
TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	↘	X	V	X	WRITE BEGINS, DATA IS LATCHED
2	L	H	X	X	X	WRITE IN PROGRESS INTERNALLY
3	↗	H	X	X	X	WRITE COMPLETED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The late write cycle is a cross between the early write cycle and the read-modify-write cycle.
Recall that in the early write the output is guaranteed to remain high impedance, and in the read-modify-write the output is guaranteed valid at access time. The late write is between these two cases. With this cycle the output may become active, and may become valid data, or may remain active but undefined. Valid data is written into the RAM if data set up, data hold, write setup and write pulse widths are observed.

NOTES: In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

HM-6504 (One of Sixteen)



HARRIS

HM-92560

256K SYNCHRONOUS CMOS RAM MODULE

Advanced Information

Features

- LOW STANDBY CURRENT — 500μA
- FAST ADDRESS ACCESS TIME — 170 ns
- DATA RETENTION — 2.0V min VCC
- THREE STATE OUTPUTS
- ORGANIZABLE AS 32K x 8 or 16K x 16 ARRAY
- ON CHIP ADDRESS REGISTERS
- 48 PIN DIP PINOUT – 2.53" x 1.30" x 0.29"
- SYNCHRONOUS OPERATION YIELDS
- LOW OPERATING POWER — 30mA/MHz
- WIDE TEMPERATURE RANGE — -55°C to +125°C

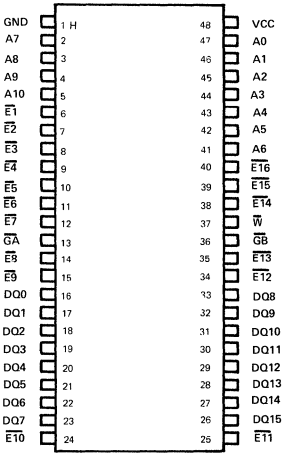
Description

The HM-92560 is a high density 256K bit CMOS RAM module. Sixteen synchronous HM-6516 2K × 8 CMOS RAMs in leadless chip carriers are mounted on a multilayer ceramic substrate. The HM-92560 RAM module is organized as two 16K by 8 CMOS RAM arrays sharing a common address bus. Separate data input/output buses and chip enables allow the user to format the HM-92560 as either a 16K×16 or 32K×8 array. Ceramic capacitors are included on the substrate to reduce noise and to minimize the need for additional external decoupling.

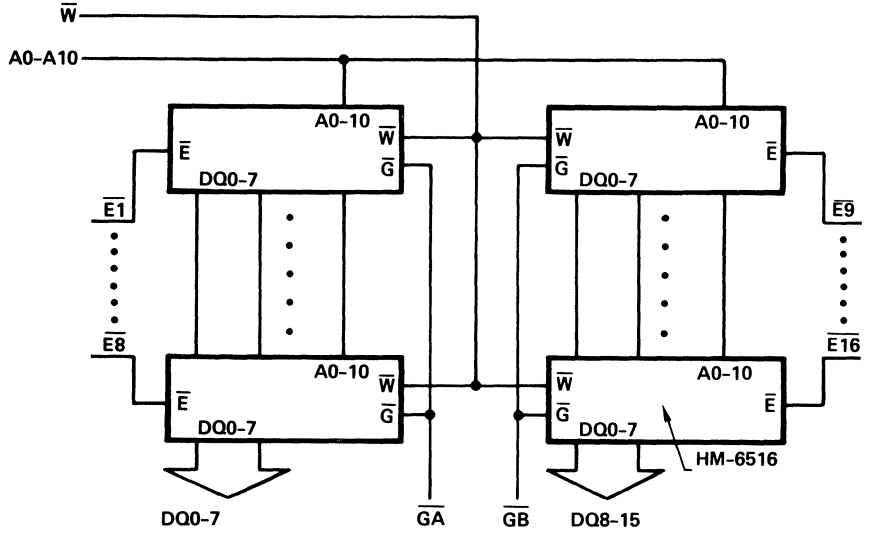
The synchronous design of the HM-92560 provides low operating power along with address latches for ease of interface to multiplexed address/data bus microprocessors.

The HM-92560 is physically constructed as an extra wide 48 pin dual-in-line package with standard 0.1'' centers between pins. This packaging technique combines the high packing density of CMOS and leadless chip carriers with the ease of use of DIP packaging.

Pinout



Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

FOR 32K x 8 CONFIGURATION

CONNECT: PIN 16 (DQ0) to PIN 33 (DQ8)
PIN 17 (DQ1) to PIN 32 (DQ9)
PIN 18 (DQ2) to PIN 31 (DQ10)
PIN 19 (DQ3) to PIN 30 (DQ11)
PIN 20 (DQ4) to PIN 29 (DQ12)
PIN 21 (DQ5) to PIN 28 (DQ13)
PIN 22 (DQ6) to PIN 27 (DQ14)
PIN 23 (DQ7) to PIN 26 (DQ15)

FOR 16K x 16 CONFIGURATION

CONNECT: PIN 6 (E1) to PIN 15 (E9)
PIN 7 (E2) to PIN 24 (E10)
PIN 8 (E3) to PIN 25 (E11)
PIN 9 (E4) to PIN 34 (E12)
PIN 10 (E5) to PIN 35 (E13)
PIN 11 (E6) to PIN 38 (E14)
PIN 12 (E7) to PIN 39 (E15)
PIN 14 (E8) to PIN 40 (E16)
PIN 13 (GA) to PIN 36 (GB)

Concerns for Proper Operation of Chip Enables:

The transition between blocks of RAM requires a change in the chip enable being used. When operating in the 16K x 16 mode use the chip enables as if there were only eight, E1 thru E8. In the 32K x 8 mode, all chip enables must be treated separately. Transitions between chip enables must be treated with the same timing constraints that apply to any one chip enable. All chip enables must be high at least one chip enable high time (TEHEL) before any chip enable can fall. As the HM-92560 is a synchrounous memory every address transition must be accompanied by a chip enable transition (see timing diagrams). More than one chip enable low simultaneously, for devices whose outputs are tied common either internally or externally, is an illegal input condition and must be avoided.

Printed Circuit Board Mounting:

The leadless chip carrier packages used in the HM-92560 have conductive lids. These lids are electrically connected to GND. The designer should be aware of the possibility that the carriers on the bottom side could short conductors below if pressed completely down against the surface of the circuit board. The pins on the package are designed with a standoff feature to help prevent the leadless carriers from touching the circuit board surface.

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC – GND)	-0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Military (-2, -8)	4.5V to 5.5V
		Industrial (-9)	4.5V to 5.5V
Storage Temperature	-65°C to 150°C	Operating Temperature	
		Military (-2, -8)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC * OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		500	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ② 16K x 16		30	mA	$\overline{E}$ = 1MHz, IO = 0 VI = VCC or GND, $\overline{G}$ = VCC
	ICCOP	Operating Supply Current ② 32K x 8		15	mA	$\overline{E}$ = 1MHz, IO = 0 VI = VCC or GND, $\overline{G}$ = VCC
	ICCDR	Data Retention Supply Current		350	μA	IO = 0, VCC = 2.0, VI = VCC or GND, $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-5	+5	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-5	+5	μA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		V	IO = -1.0mA
	CIA	Address Input ③ Capacitance		200	pF	VI = VCC or GND f = 1MHz
	CIE1	Enable Input ③ Capacitance (16K x 16)		100	pF	VI = VCC or GND f = 1MHz
	CIE2	Enable Input ③ Capacitance (32K x 8)		50	pF	VI = VCC or GND f = 1MHz
	CIG 1	Output Enable Input ③ Capacitance (16K x 16)		150	pF	VI = VCC or GND f = 1MHz
	CIG 2	Output Enable Input ③ Capacitance (32K x 8)		100	pF	VI = VCC or GND f = 1MHz
	CIO1	Input/Output ③ Capacitance (16K x 16)		150	pF	VI/O = VCC or GND f = 1MHz
	CIO2	Input/Output ③ Capacitance (32 x 8)		250	pF	VI/O = VCC or GND f = 1MHz
	CIW	Write Input ③ Capacitance		200	pF	VI = VCC or GND f = 1MHz
	CVcc	Decoupling Capacitance		.5	μf	f = 1MHz

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC – GND)	-0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Military (-2, -8)	4.5V to 5.5V
Storage Temperature	-65°C to 150°C	Industrial (-9)	4.5V to 5.5V
		Operating Temperature	
		Military (-2, -8)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

* *CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC * OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
A.C.	TELQV	Chip Enable Access Time		150	ns	④
	TAVQV	Address Access Time		170	ns	④
	TELQX	Chip Enable Output Enable Time	10		ns	④
	TWLQZ	Write Enable Output Disable Time		70	ns	④
	TEHQZ	Chip Enable Output Disable Time		70	ns	④
	TGLQX	Output Enable Output Enable Time	10		ns	④
	TGLQV	Output Enable Output Valid Time		70	ns	④
	TGHQZ	Output Enable Output Disable Time		70	ns	④
	TELEH	Chip Enable Pulse Negative Width	150		ns	④
	TEHEL	Chip Enable Pulse Positive Width	80		ns	④
	TAVEL	Address Setup Time	20		ns	④
	TELAX	Address Hold Time	50		ns	④
	TWLWH	Write Enable Pulse Width	150		ns	④
	TWLEH	Write Enable Pulse Setup Time	150		ns	④
	TELWH	Write Enable Pulse Hold Time	150		ns	④
	TDVWH	Data Setup Time	80		ns	④
	TWHDX	Data Hold Time	20		ns	④
	TWLDV	Write Data Delay Time	70		ns	④
	TELEL	Read or Write Cycle Time	230		ns	④

NOTES:
① All devices tested at worst case limits.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency.
③ Capacitance sampled and guaranteed – not 100% tested.
④ AC test conditions:
Input Pulse Levels: 0V to 3.0V
Input Rise Time: 10ns
Input to Output timing Reference Levels: 1.5V
Output load: 50pf

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC – GND)	-0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Commercial (-5)	4.5V to 5.5V
Storage Temperature	-65°C to 150°C	Operating Temperature	
		Commercial (-5)	0°C to +70°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC * OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		3.5	mA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ② 16K x 16		35	mA	$\overline{E}$ = 1MHz, 10 = 0 VI = VCC or GND, $\overline{G}$ = VCC
	ICCOP	Operating Supply Current ② 32K x 8		20	mA	$\overline{E}$ = 1MHz, 10 = 0 VI = VCC or GND, $\overline{G}$ = VCC
	ICCDR	Data Retention Supply Current		2.5	mA	IO = 0, VCC = 2.0, VI = VCC or GND, $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-10	+10	μA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	-10	+10	μA	GND≤VIO≤VCC
	VIL	Input Low Voltage	-0.3	.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		V	IO = -1.0mA
	CIA	Address Input ③ Capacitance		200	pF	VI = VCC or GND f = 1MHz
	CIE1	Enable Input ③ Capacitance (16K x 16)		100	pF	VI = VCC or GND f = 1MHz
	CIE2	Enable Input ③ Capacitance (32K x 8)		50	pF	VI = VCC or GND f = 1MHz
	CIG 1	Output Enable Input ③ Capacitance (16K x 16)		150	pF	VI =VCC or GND f = 1MHz
	CIG 2	Output Enable Input ③ Capacitance (32K x 8)		100	pF	VI = VCC or GND f = 1MHz
	CIO1	Input/Output ③ Capacitance (16K x 16)		150	pF	VI/O = VCC or GND f = 1MHz
	CIO2	Input/Output ③ Capacitance (32 x 8)		250	pF	VI/O = VCC or GND f = 1MHz
	CIW	Write Input ③ Capacitance		200	pF	VI = VCC or GND f = 1MHz
	CVcc	Decoupling Capacitance		.5	μf	f = 1MHz

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC – GND)	-0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Commercial (-5)	4.5V to 5.5V
Storage Temperature	-65°C to 150°C	Operating Temperature	
		Commercial (-5)	0°C to +70°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC * OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
A.C.	TELQV	Chip Enable Access Time		250	ns	④
	TAVQV	Address Access Time		270	ns	④
	TELQX	Chip Enable Output Enable Time	10		ns	④
	TWLQZ	Write Enable Output Disable Time		80	ns	④
	TEHQZ	Chip Enable Output Disable Time		80	ns	④
	TGLQX	Output Enable Output Enable Time	10		ns	④
	TGLQV	Output Enable Output Valid Time		70	ns	④
	TGHQZ	Output Enable Output Disable Time		80	ns	④
	TELEH	Chip Enable Pulse Negative Width	250		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		ns	④
	TAVEL	Address Setup Time	20		ns	④
	TELAX	Address Hold Time	50		ns	④
	TWLWH	Write Enable Pulse Width	250		ns	④
	TWLEH	Write Enable Pulse Setup Time	250		ns	④
	TELWH	Write Enable Pulse Hold Time	250		ns	④
	TDVWH	Data Setup Time	100		ns	④
	TWHDX	Data Hold Time	20		ns	④
	TWLDV	Write Data Delay Time	150		ns	④
	TELEL	Read or Write Cycle Time	350		ns	④

NOTES:

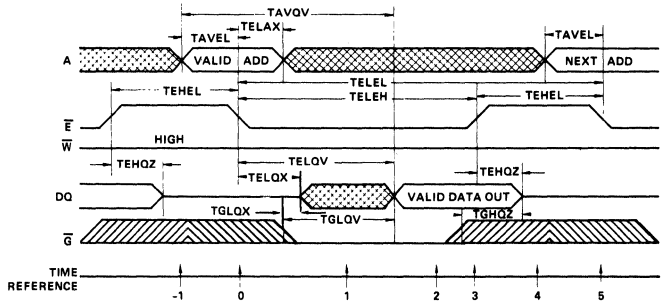
① All devices tested at worst case limits.

② Operating Supply Current (ICCOP) is proportional to Operating Frequency.

③ Capacitance sampled and guaranteed – not 100% tested.

④ AC test conditions:
Input Pulse Levels: 0V to 3.0V
Input Rise Time: 10ns
Input to Output timing Reference Levels: 1.5V
Output load: 50pf

Read Cycle

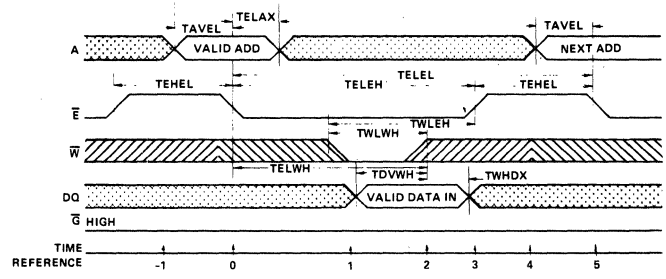


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	$\overline{G}$	A	DQ	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	L	X	X	OUTPUT ENABLED
2	L	H	L	X	V	OUTPUT VALID
3	↗	H	X	X	V	READ ACCOMPLISHED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0), minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1), the outputs become enabled but data is not valid until time (T = 2), $\overline{W}$ must remain high throughout the read cycle. After the data has been read, $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). $\overline{G}$ is used to disable the output buffers when in a logical "1" state (T = -1, 0, 3, 4, 5). After (T = 4) time, the memory is ready for the next cycle.

Write Cycle

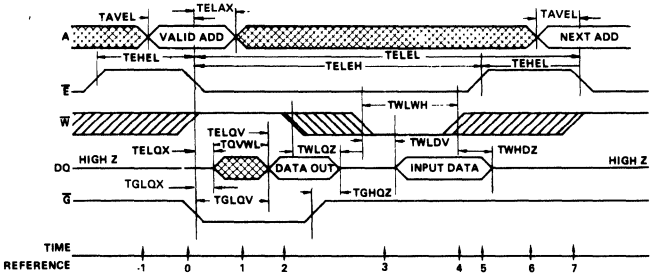


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	$\overline{G}$	A	DQ	FUNCTION
-1	H	X	H	X	X	MEMORY DISABLED
0	↘	X	H	V	X	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	H	X	X	WRITE PERIOD BEGINS
2	L	↗	H	X	V	DATA IN IS WRITTEN
3	↗	H	H	X	X	WRITE COMPLETED
4	H	X	H	X	X	PREPARE FOR NEXT CYCLE (SAME AS-1)
5	↘	X	H	V	X	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated on the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on chip registers. If a write cycle is to be performed where the output is not to become active, $\overline{G}$ can be held high (inactive). TDVWH and TWHDX must be met for proper device operation regardless of $\overline{G}$. If $\overline{E}$ and $\overline{G}$ fall before $\overline{W}$ falls (read mode), a possible bus conflict may exist. If $\overline{E}$ rises before $\overline{W}$ rises, reference data setup and hold times to the $\overline{E}$ rising edge. The write operation is terminated by the first rising edge of $\overline{W}$ (T = 2) or $\overline{E}$(T = 3). After the minimum $\overline{E}$ high time (TEHEL), the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low unitl all desired locations have been written. In this case, data setup and hold times must be referenced to the rising edge of $\overline{E}$.

Read Modify Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	$\overline{G}$	A	DATA I/O DQ	FUNCTION
-1	H	X	H	X	Z	MEMORY DISABLED
0	↘	H	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	L	X	X	READ MODE, OUTPUT ENABLED ($\overline{W}$ = HIGH, $\overline{G}$ = LOW)
2	L	H	L	X	V	READ MODE, OUTPUT VALID
3	L	L	H	X	Z	WRITE MODE, OUTPUT HIGH Z
4	L	↙	H	X	V	WRITE MODE, DATA IS WRITTEN
5	↗	H	H	X	Z	WRITE COMPLETED
6	H	X	H	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↘	H	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

If the pulse width of $\overline{W}$ is relatively short in relation to that of $\overline{E}$, a combination read write cycle may be performed. If $\overline{W}$ remains high for the first part of the cycle, the output will become active during time (T = 1) provided $\overline{G}$ is low. Data out will be valid during time (T = 2). After the data is read, $\overline{W}$ can go low. After minimum TWLWH, $\overline{W}$ may return high. The information just written may now be read or $\overline{E}$ may return high, disabling the output buffer and preparing the device for the next cycle. Any number or sequence of read-write operations may be performed while $\overline{E}$ is low providing all timing requirements are met.

NOTES:

In the above descriptions, the numbers in parentheses (T = n), refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

HM-92570

256K BUFFERED SYNCHRONOUS CMOS RAM MODULE

Advanced Information

Features

- LOW STANDBY CURRENT — 600μA/3.5mA
- FAST ACCESS TIME — 250ns
- DATA RETENTION — 2.0V min
- THREE STATE OUTPUTS
- ORGANIZABLE AS 32K x 8 or 16K x 16 ARRAY
- BUFFERED ADDRESS AND CONTROL LINES
- ON CHIP ADDRESS REGISTERS
- 48 PIN DIP PINOUT – 2.66" x 1.30" x 0.29"
- WIDE TEMPERATURE RANGE — -55°C to +125°C

Description

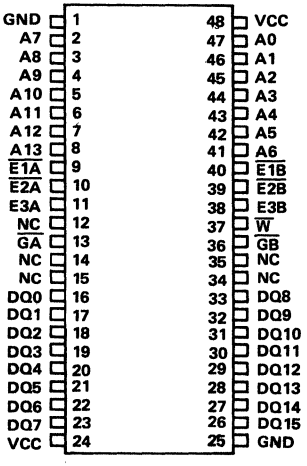
The HM-92570 is a fully buffered 256K bit CMOS RAM module consisting of sixteen HM-6516 2K x 8 CMOS RAMs, two HD-6495 CMOS hex buffers, and two HD-6440 CMOS 3:8 line decoders in leadless chip carriers mounted on a multilayer ceramic substrate. The HM-92570 RAM module is organized as two 16K by 8 CMOS RAM arrays sharing a common address bus. Separate data input/output buses allow the user to format the HM-92570 as either a 16K x 16 or 32K x 8 array.

On-board CMOS buffers and decoders reduce external package count requirements. Write enable and chip enable control signals are buffered along with address inputs. Ceramic capacitors are included on the substrate to reduce noise and to minimize the need for additional external decoupling.

The synchronous design of the HM-92570 provides low operating power along with address latches for ease of interface to multiplexed address/data bus microprocessor.

The HM-92570 is physically constructed as an extra wide 48 pin dual-in-line package with standard 0.1" centers between pins. This packaging technique combines the high packing density of CMOS and leadless chip carriers with the ease of use of DIP packaging.

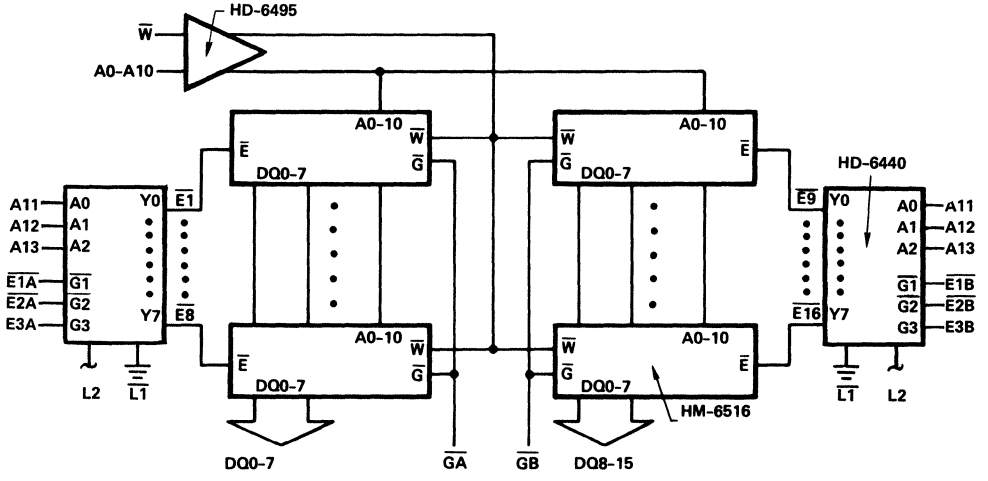
Pinout



PIN NAMES

A	–	Address Input
DQ	–	Data Input/Output
$\overline{GX}$	–	Output Enable
$\overline{EXX}$	–	Chip Enable
$\overline{W}$	–	Write Enable
NC	–	No Connection

Functional Diagram



CAUTION: Electronic devices are sensitive to elec

FOR 32K x 8 CONFIGURATION

CONNECT: PIN 16 (DQ0) to PIN 33 (DQ8)
PIN 17 (DQ1) to PIN 32 (DQ9)
PIN 18 (DQ2) to PIN 31 (DQ10)
PIN 19 (DQ3) to PIN 30 (DQ11)
PIN 20 (DQ4) to PIN 29 (DQ12)
PIN 21 (DQ5) to PIN 28 (DQ13)
PIN 22 (DQ6) to PIN 27 (DQ14)
PIN 23 (DQ7) to PIN 26 (DQ15)

FOR 16K x 16 CONFIGURATION

CONNECT: PIN 9 ($\overline{E1A}$) to PIN 40 ($\overline{E1B}$)
PIN 10 ($\overline{E2A}$) to PIN 39 ($\overline{E2B}$)
PIN 11 (E3A) to PIN 38 (E3B)
PIN 13 (GA) to PIN 36 (GB)

Concerns for Proper Operation of Chip Enables:

The transition between blocks of RAM requires a change in the chip enable being used. When operating in the 16K x 16 mode use the chip enables as if there were only three, E1 thru E3. In the 32K x 8 mode all chip enables must be treated separately. Transitions between chip enables must be treated with the same timing constraints that apply to any one chip enable. All chip enables must be high at least one chip enable high time (TEHEL) before any chip enable can fall.

As the HM-92570 is a synchrounous memory, every address transition must be accompanied by a chip enable transition (see timing diagrams). More than one chip enable low simultaneously, for devices whose outputs are tied common either internally or externally, is an illegal input condition and must be avoided. To properly decode the chip enables, addresses A11, A12, and A13 must be valid for the duration of TAVAV.

Printed Circuit Board Mounting:

The leadless chip carrier packages used in the HM-92570 have conductive lids. These lids are electrically connected to GND. The designer should be aware of the possibility that the carriers on the bottom side could short conductors below if pressed completely down against the surface of the circuit board. The pins on the package are designed with a standoff feature to help prevent the leadless carriers from touching the circuit board surface.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (VCC – GND)	-0.3 to 8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to 150°C

OPERATING RANGE

Operating Supply Voltage	
Military (-2, -8)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2, -8)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC * OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		600	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ② 16K x 16		30	mA	$\overline{E}$ = 1MHz, IO = 0 VI = VCC or GND, $\overline{G}$ = VCC
	ICCOP	Operating Supply Current ② 32K x 8		15	mA	$\overline{E}$ = 1MHz, IO = 0 VI = VCC or GND, $\overline{G}$ = VCC
	ICCDR	Data Retention Supply Current		450	μA	IO = 0, VCC = 2.0, VI = VCC or GND, $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	GND ≤ VI ≤ VCC
	IIG	Output Enable Leakage Current	-5.0	+5.0	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-5.0	+5.0	μA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	3.5	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		V	IO = -1.0mA
	CIA	Address Input ③ Capacitance		25	pF	VI = VCC or GND f = 1MHz
	CIE1	Decoder Enable Input ③ Capacitance (16K x 16)		50	pF	VI = VCC or GND f = 1MHz
	CIE2	Decoder Enable Input ③ Capacitance (32K x 8)		25	pF	VI = VCC or GND f = 1MHz
	CIG 1	Output Enable Input ③ Capacitance (16K x 16)		150	pF	VI = VCC or GND f = 1MHz
	CIG 2	Output Enable Input ③ Capacitance (32K x 8)		100	pF	VI = VCC or GND f = 1MHz
	CIO1	Input/Output ③ Capacitance (16K x 16)		150	pF	VI/O = VCC or GND f = 1MHz
	CIO2	Input/Output ③ Capacitance (32 x 8)		250	pF	VI/O = VCC or GND f = 1MHz
	CIW	Write Input ③ Capacitance		25	pF	VI = VCC or GND f = 1MHz
	CVcc	Decoupling Capacitance		.5	μf	f = 1MHz

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC – GND)	-0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Military (-2, -8)	4.5V to 5.5V
Storage Temperature	-65°C to 150°C	Industrial (-9)	4.5V to 5.5V
		Operating Temperature	
		Military (-2, -8)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC * OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
A.C.	TELQV	Chip Enable Access Time		250	ns	④
	TAVQV	Address Access Time		270	ns	④
	TELQX	Chip Enable Output Enable Time	10		ns	④
	TWLQZ	Write Enable Output Disable Time		120	ns	④
	TEHQZ	Chip Enable Output Disable Time		150	ns	④ ⑥
	TGLQX	Output Enable Output Enable Time	10		ns	④
	TGLQV	Output Enable Output Valid Time		70	ns	④
	TGHQZ	Output Enable Output Disable Time		100	ns	④ ⑥
	TELEH	Chip Enable Pulse Negative Width	250		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		ns	④
	TAVEL	Address Setup Time	20		ns	④ ⑤
	TELAX	Address Hold Time	120		ns	④
	TWLWH	Write Enable Pulse Width	140		ns	④
	TWLEH	Write Enable Pulse Setup Time	140		ns	④
	TELWH	Write Enable Pulse Hold Time	250		ns	④
	TDVWH	Data Setup Time	20		ns	④
	TWHDX	Data Hold Time	70		ns	④
	TWLDV	Write Data Delay Time	120		ns	④
	TELEL	Read or Write Cycle Time	350		ns	④
	TAVAV	Enable Decoder Address Valid Time	270		ns	Applies Only to A11, A12, A13

NOTES:

① All devices tested at worst case limits.

② Operating Supply Current (ICCOP) is proportional to Operating Frequency.

③ Capacitance sampled and guaranteed – not 100% tested.

④ AC test conditions:
Input Pulse Levels: 0V to 3.5V
Input Rise Time: 10ns
Input to Output timing Reference Levels: 1.5V
Output load: 50pf

⑤ Includes A11, A12, A13

⑥ Output Disable Time is faster when using $\overline{GA}$ or $\overline{GB}$ to Disable the Outputs.
See Note 1 in Read Cycle Timing Diagram.

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC – GND)	-0.3 to 8.0V	Operating Supply Voltage Commercial (-5)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Operating Temperature Commercial (-5)	0°C to +70°C
Storage Temperature	-65°C to 150°C		

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC * OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		3.5	mA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ② 16K x 16		35	mA	$\overline{E}$ = 1MHz, IO = 0 VI = VCC or GND, $\overline{G}$ = VCC
	ICCOP	Operating Supply Current ② 32K x 8		20	mA	$\overline{E}$ = 1MHz, IO = 0 VI = VCC or GND, $\overline{G}$ = VCC
	ICCDR	Data Retention Supply Current		2.5	mA	IO = 0, VCC = 2.0, VI = VCC or GND, $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-10.0	+10.0	µA	GND ≤ VI ≤ VCC
	IIG	Output Enable Leakage Current	-10.0	+10.0	µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-10.0	+10.0	µA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	3.5	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		V	IO = -1.0mA
	CIA	Address Input ③ Capacitance		25	pF	VI = VCC or GND f = 1MHz
	CIE1	Decoder Enable Input ③ Capacitance (16K x 16)		50	pF	VI = VCC or GND f = 1MHz
	CIE2	Decoder Enable Input ③ Capacitance (32K x 8)		25	pF	VI = VCC or GND f = 1MHz
	CIG 1	Output Enable Input ③ Capacitance (16K x 16)		150	pF	VI =VCC or GND f = 1MHz
	CIG 2	Output Enable Input ③ Capacitance (32K x 8)		100	pF	VI = VCC or GND f = 1MHz
	CIO1	Input/Output ③ Capacitance (16K x 16)		150	pF	VI/O = VCC or GND f = 1MHz
	CIO2	Input/Output ③ Capacitance (32 x 8)		250	pF	VI/O = VCC or GND f = 1MHz
	CIW	Write Input ③ Capacitance		25	pF	VI = VCC or GND f = 1MHz
	CVcc	Decoupling Capacitance		.5	µf	f = 1MHz

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC – GND)	-0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Commercial (-5)	4.5V to 5.5V
Storage Temperature	-65°C to 150°C	Operating Temperature	
		Commercial (-5)	0°C to +70°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC * OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
A.C.	TELQV	Chip Enable Access Time		300	ns	④
	TAVQV	Address Access Time		320	ns	④
	TELQX	Chip Enable Output Enable Time	10		ns	④
	TWLQZ	Write Enable Output Disable Time		120	ns	④
	TEHQZ	Chip Enable Output Disable Time		200	ns	④ ⑥
	TGLQX	Output Enable Output Enable Time	10		ns	④
	TGLQV	Output Enable Output Valid Time		80	ns	④
	TGHQZ	Output Enable Output Disable Time		120	ns	④ ⑥
	TELEH	Chip Enable Pulse Negative Width	300		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		ns	④
	TAVEL	Address Setup Time	20		ns	④ ⑤
	TELAX	Address Hold Time	130		ns	④
	TWLWH	Write Enable Pulse Width	150		ns	④
	TWLEH	Write Enable Pulse Setup Time	150		ns	④
	TELWH	Write Enable Pulse Hold Time	300		ns	④
	TDVWH	Data Setup Time	30		ns	④
	TWHDX	Data Hold Time	80		ns	④
	TWLDV	Write Data Delay Time	120		ns	④
	TELEL	Read or Write Cycle Time	450		ns	④
	TAVAV	Enable Decoder Address Valid Time	320		ns	Applies Only to A11, A12, A13

NOTES:

① All devices tested at worst case limits.

② Operating Supply Current (ICCOP) is proportional to Operating Frequency.

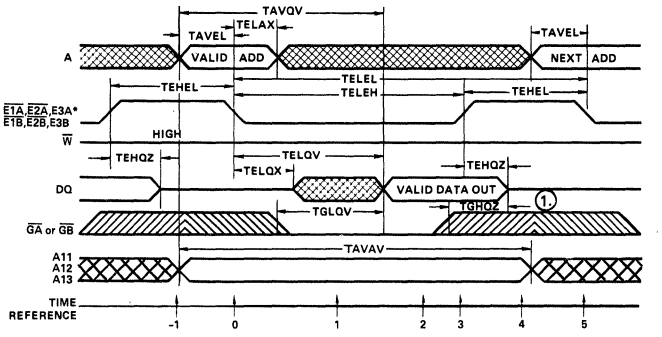
③ Capacitance sampled and guaranteed – not 100% tested.

④ AC test conditions:
Input Pulse Levels: 0V to 3.5V
Input Rise Time: 10ns
Input to Output timing Reference Levels: 1.5V
Output load: 50pf

⑤ Includes A11, A12, A13

⑥ Output Disable Time is faster when using $\overline{GA}$ or $\overline{GB}$ to Disable the Outputs.
See Note 1 in Read Cycle Timing Diagram.

Read Cycle



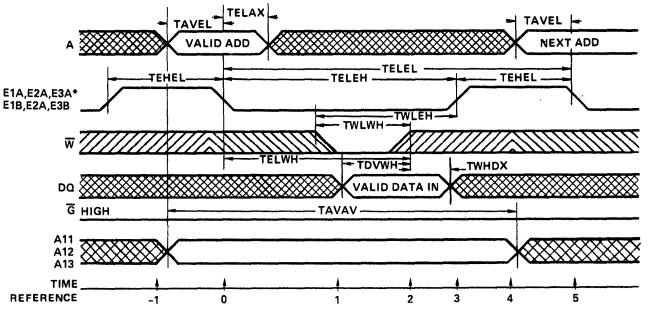
① To avoid bus contention in multiplexed Data/Address applications, $\overline{GA}$ or $\overline{GB}$ should transition high at the end of the read access. Propagation delays thru the Chip Enable Decoder allow DQ lines to be active with output data longer than TGHQZ if not accompanied by the $\overline{GA}$ or $\overline{GB}$ high transition.

TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	$\overline{G}$	A	A11 A12 A13	DATA I/O DQ	FUNCTION
-1	H	X	X	X	X	Z	MEMORY DISABLED
0	↘	H	X	V	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	L	X	V	X	OUTPUT ENABLED
2	L	H	L	X	V	V	OUTPUT VALID
3	↗	H	X	X	V	V	READ ACCOMPLISHED
4	H	X	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	X	V	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$(T = 0), minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1), the outputs become enabled but data is not valid until time (T = 2), $\overline{W}$ must remain high throughout the read cycle. After the data has been read, E may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). $\overline{G}$ is used to disable the output buffers when in a logical "1" state (T = -1, 0, 3, 4, 5). After T = 4) time, the memory is ready for the next cycle. *E3A and E3B are opposite polarity of $\overline{E}$1A.

Write Cycle

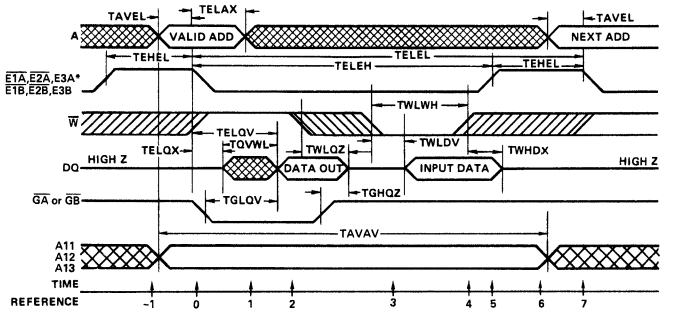


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	$\overline{G}$	A	A11 A12 A13	DATA I/O DQ	FUNCTION
-1	H	X	H	X	X	X	MEMORY DISABLED
0	↘	X	H	V	V	X	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	H	X	V	X	WRITE PERIOD BEGINS
2	L	↗	H	X	V	V	DATA IN IS WRITTEN
3	↗	H	H	X	V	X	WRITE COMPLETED
4	H	X	H	X	X	X	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	H	V	V	X	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated on the falling edge of E(T = 0), which latches the address information in the on chip registers. If a write cycle is to be performed where the output is not to become active, $\overline{G}$ can be held high (inactive). TDVWH and TWHDX must be met for proper device operation regardless of $\overline{G}$. If $\overline{E}$ and $\overline{G}$ fall before $\overline{W}$ falls (read mode), a possible bus conflict may exist. If $\overline{E}$ rises before $\overline{W}$ rises, reference data setup and hold times to the $\overline{E}$ rising edge. The write operation is terminated by the first rising edge of $\overline{W}$ (T = 2) or $\overline{E}$(T = 3). After the minimum $\overline{E}$ high time (TEHEL), the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising edge of $\overline{E}$. *E3A and E3B are opposite polarity of $\overline{E}$1A.

Read Modify Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	$\overline{G}$	A	A11 A12 A13	DATA I/O DQ	FUNCTION
-1	H	X	H	X	X	Z	MEMORY DISABLED
0	↘	H	H	V	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	L	X	V	X	READ MODE, OUTPUT ENABLED (W = HIGH, G = LOW)
2	L	H	L	X	V	V	READ MODE, OUTPUT VALID
3	L	L	H	X	V	Z	WRITE MODE, OUTPUT HIGH Z
4	L	↘	H	X	V	V	WRITE MODE, DATA IS WRITTEN
5	↘	H	H	X	V	Z	WRITE COMPLETED
6	H	X	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↘	H	H	V	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

If the pulse width of $\overline{W}$ is relatively short in relation to that of $\overline{E}$, a combination read write cycle may be performed. If $\overline{W}$ remains high for the first part of the cycle, the output will become active during time (T = 1) provided $\overline{G}$ is low. Data out will be valid during time (T =2). After the data is read, $\overline{W}$ can go low. After minimum TWLWH, $\overline{W}$ may return high. The information just written may now be read or $\overline{E}$ may return high, disabling the output buffer and preparing the device for the next cycle. Any number or sequence of read-write operations may be performed while $\overline{E}$ is low providing all timing requirement are met. *E3A and E3B are opposite polarity of $\overline{E1A}$.

NOTES:

In the above descriptions, the numbers in parentheses (T = 1), refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

HARRIS

HM-6641

512 x 8 CMOS PROM

Features

- LOW POWER STANDBY — 500μW MAX.
- LOW POWER OPERATION — 50mW/MHz MAX.
- FAST ACCESS TIME — 250ns MAX.
- FIELD PROGRAMMABLE
- POLYSILICON FUSE LINKS
- TTL COMPATIBLE IN/OUT
- POPULAR PINOUT LIKE BIPOLAR 7641
- THREE STATE OUTPUTS
- ADDRESS LATCHES INCLUDED ON CHIP
- EASY MICROPROCESSOR INTERFACING
- WIDE TEMPERATURE RANGES

Description

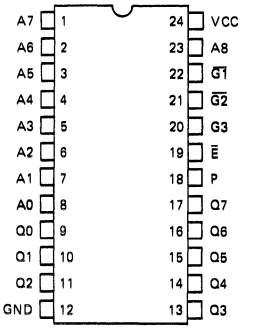
The HM-6641 is a 512 x 8 CMOS polysilicon fusible link Programmable Read Only Memory in the popular 24 pin, byte wide pinout. Synchronous circuit design techniques combine with CMOS processing to give this device high speed performance with very low power dissipation.

On chip address latches are provided, allowing easy interfacing with recent generation microprocessors that use multiplexed address/data bus structures, such as the 8085. The output enable controls, both active low and active high, further simplify microprocessor system interfacing by allowing output data bus control independent of the chip enable control. The data output latches allow the use of the HM-6641 in high speed pipelined architecture systems, and also in synchronous logic replacement functions.

Applications for the HM-6641 CMOS PROM include low power handheld microprocessor based instrumentation and communications systems, remote data acquisition and processing systems, processor control store, and synchronous logic replacement.

Pinout

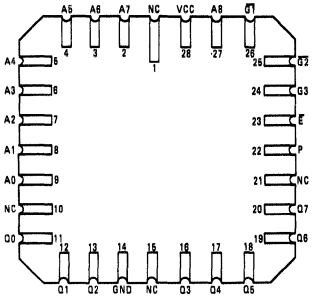
TOP VIEW – DIP



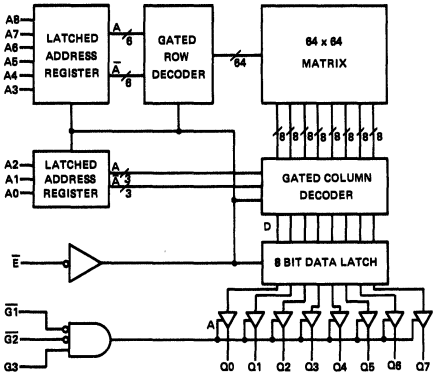
PIN NAMES

A Address Input	$\overline{G}$ Output Enable
Q Data Output	P Program Enable
$\overline{E}$ Chip Enable	(P = GND except during Programming)
NC No Connect	

TOP VIEW - LCC



Functional Diagram



ALL LINES POSITIVE LOGIC - ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

DATA LATCHES:
L HIGH → Q = D
Q LATCHES ON RISING EDGE OF $\overline{E}$

ADDRESS LATCHES AND GATED DECODERS:
LATCH ON FALLING EDGE OF $\overline{E}$
GATE ON FALLING EDGE OF $\overline{E}$

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS *		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply	
		Military (-2/-8)	4.5V to 5.5V
Input or Output Voltage Applied	GND -0.3Vto VCC +0.3V	Industrial (-9)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	-65°C to +150°C	Military (-2/-8)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

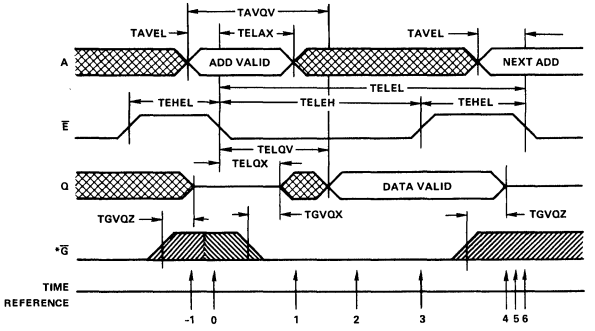
ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEMP & VCC = OPERATING RANGE MIN	TEMP & VCC = OPERATING RANGE MAX	TEMP=25°C VCC=5.0 ① TYPICAL	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current		100	10	μA	IO = 0 VI = GND OR VCC
ICCOP	Operating Supply Current ②		10	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND≤VI≤VCC
IOZ	Output Leakage Current	-1.0	+1.0	±0.5	μA	GND≤VO≤VCC
VIL	Input Low Voltage	-0.3	0.8	2.0	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	2.0	V	
VOL	Output Low Voltage		0.4	0.1	V	IOL = 3.2mA
VOH	Output High Voltage	2.4		4.25	V	IOH = -1.0mA
CI	Input Capacitance ③		10.0	5.0	pF	VI = VCC or GND f = 1MHz
CO	Output Capacitance ③		12.0	8.0	pF	VO = VCC OR GND f = 1MHz
TELQV	Chip Enable Access Time		250	150	ns	④
TAVQV	(TAVQV = TELQV + TAVEL) Address Access Time		270	150	ns	④
TELQX	Chip Enable Output Enable Time	20	150	70	ns	④
TGVQX	Output Enable Output Enable Time	20	150	70	ns	④
TGXQZ	Output Enable Output Disable Time	20	150	70	ns	④
TELEH	Chip Enable Pulse Negative Width	250		150	ns	④
TELEL	Read Cycle Time	400		230	ns	④
TEHEL	Chip Enable Pulse Positive Width	150		80	ns	④
TAVEL	Address Set-up Time	20		0	ns	④
TELAX	Address Hold Time	60		40	ns	④

NOTES:

① All devices tested at worst case limits. Room temp., 5 volt data provided for information - not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
③ Capacitance sampled and guaranteed - not 100% tested.
④ AC Test Conditions: Inputs-TRISE = TFALL = 20nsec; Outputs -CLOAD = 50pF. All timing measurements at 1.5V.

Read Cycle



*G HAS SAME TIMING AS $\overline{G}$ EXCEPT SIGNAL IS INVERTED

TRUTH TABLE

TIME REFERENCE	INPUTS E	G	A	OUTPUTS O	FUNCTION
-1	H	H	X	Z	MEMORY DISABLED
0	↓	H	V	Z	CYCLE BEGINS-ADDRESSES ARE LATCHED
1	L	L	X	X	OUTPUT ENABLED
2	L	L	X	V	OUTPUT VALID
3	↑	L	X	V	OUTPUT LATCHED
4	H	H	X	Z	READ ACCOMPLISHED AND OUTPUT DISABLED
5	H	H	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
6	↓	H	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

In the HM-6641 read cycle, the address information is latched into the on chip registers on the falling edge of $\overline{E}$(T = 0). Minimum address setup and hold time requirements must be met. After the required hold time,the addresses may change state without affecting device operation. To read data $\overline{G1}$ and $\overline{G2}$ must be low, and G3 must be high. After access time, $\overline{E}$ may be taken high to latch the data outputs and begin TEHEL. Taking either or both $\overline{G1}$ or $\overline{G2}$ high or G3 low will force the output buffers to a high impedance state. The output data may be re-enabled at any time taking $\overline{G1}$ and $\overline{G2}$ low and G3 high. On the falling edge of $\overline{E}$ the data will be unlatched. P should be grounded except when in the programming mode.

Programming

INTRODUCTION

The HM-6641 is a 512 word, by 8 bit field programmable read only memory utilizing polycrystalline silicon fusible links as programmable memory elements. Selected memory locations are permanently changed from their manufactured state, of all low (VOL) to a logical high (VOH), by the controlled application of programming potentials and pulses. Careful adherence to the following programming specifications will result in high programming yield. Both high VCC (6.0 volts) and low VCC (4.0 volts) verify cycles are specified to assure the integrity of the programmed fuse. This programming specification, although complete, does not preclude rapid programming. The worst case programming time required is 37.4 seconds, and typical programming time can be approximately 4 seconds per device.

The chip ($\overline{E}$) and output enable ($\overline{G}$) are used during the programming procedure. On PROM's which have more than one output enable control $\overline{G1}$ is to be used. The other output enables must be held in the active, or enabled, state throughout the entire programming sequence. The programmer designer is advised that all pins of the programmer's socket should be at ground potential when the PROM is inserted into the socket. VCC must be applied to the PROM before any input or output pin is allowed to rise*.

OVERALL PROGRAMMING PROCEDURE

1. The address of the first bit to be programmed is presented, and latched by the chip enable ($\overline{E}$) falling edge. The output is disabled by taking the output enable ($\overline{G}$) high.

2. VCC is raised to the programming voltage level, 12.5V.

3. The data output pin corresponding to the bit to be programmed is pulled low. All other bits in the word are pulled up to VCC (at the programming level).

4. A 500 μs pulse is applied to the programming control pin (P).

5. The data output pin is returned to VCC, and the VCC pin is returned to 6.0 volts.

6. The address of the bit is again presented, and latched by a second chip enable falling edge.

7. The data outputs are enabled, and read, to verify that the bit was successfully programmed.
   a). If verified, two post programming pulses are applied (the bit is programmed twice more). Then the next bit to be programmed is addressed and programmed .
   b). If not verified, the program/verify sequence is repeated up to 8 times total, at the programming voltage level, 12.5 volts.
   c). If data is not verified, the programming voltage is increased to +14.0 volts. The program/verify sequence is then repeated up to 8 additional times.

8. After all bits to be programmed have been verified at 6.0 volts, the VCC is lowered to 4.0 volts and all bits are verified.
   a). If all bits verify, the device is properly programmed.
   b). If any bit fails to verify, the device is rejected.

PROGRAMMING SYSTEM REQUIREMENTS

1. The power supply for the device to be programmed must be able to be set to four voltages; 4.0V, 6.0V, 12.5V, 14.0V. This supply must be able to supply 500mA average, and 1A dynamic, currents to the PROM during programming. The power supply rise fall times when switching between voltages must be no quicker than 1μs.

2. The address drivers must be able to maintain input voltage levels $\geq$70% VCC for VIH, and $\leq$ 20% VCC for VIL. The programming system designer has a choice between buffers that will track VCC up and down (e.g. open collector buffers with pull up resistors) or buffers used for VIH only at 4.0V and 6.0V and returned to VIL when the system is at programing voltages.*

3. The control input buffers have the same 70% and 20% VCC requirements as the address buffers. Notice that chip enable ($\overline{E}$) does not require a pull up to programming voltage levels, but that the output enable ($\overline{G}$) must have a pull up to track VCC up and down. The program control (P) must switch from ground to programming VCC level.*

4. The data input buffers must be able to sink up to 3mA from the PROM's output pins without rising more than 0.7 volts above ground, be able to hold the other outputs high with a current source capability of 0.5mA to 2.0mA, and not interfere with the reading and verifying of the data output of the PROM. Notice that a bit to be programmed is changed from a low state (VOL) to high (VOH) by pulling low on the output pin. A suggested implementation is open collector TTL buffers (or inverters) with 4.7KΩ pull up resistors to VCC.*

*Note: Never allow any input or output pin to rise more than 0.3 volts above VCC, or fall more than 0.3 volts below ground.

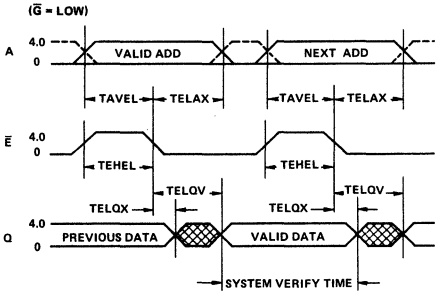
PROGRAMMING SYSTEM CHARACTERISTICS

PARAMETER	NAME	MIN	TARGET	MAX	UNITS
VCCN	Normal VCC	5.75	6.0	6.25	volts
VCC PGM	Programming Voltage	12.0	12.5	14.0	volts
VCC LV	Low Voltage Verify VCC	3.75	4.0	4.25	volts
ICC	System ICC Capability	500			mA
ICC Peak	Transient ICC Capability	1.0			A
	For PROM Input Pins:				
VOL	Output Low Voltage (to PROM)	-0.3	GND	20% VCC	volts
VOH	Output High Voltage (to PROM)	70% VCC	VCC	VCC +0.3	volts
IOL	Output Sink Current (at VOL)	.01			mA
IOH	Output Source Current (At VOH)	.01			mA
	For PROM Data Output Pins:				
VOL	Output Low Voltage (to PROM)	-0.3	GND	0.7	volts
VOH	Output High Voltage (to PROM)	70% VCC	VCC	VCC +0.3	volts
IOL	Output Sink Current (at VOL)	3.0			mA
IOH	Output Source Current (at VOH)	0.5	1.0	2.0	mA

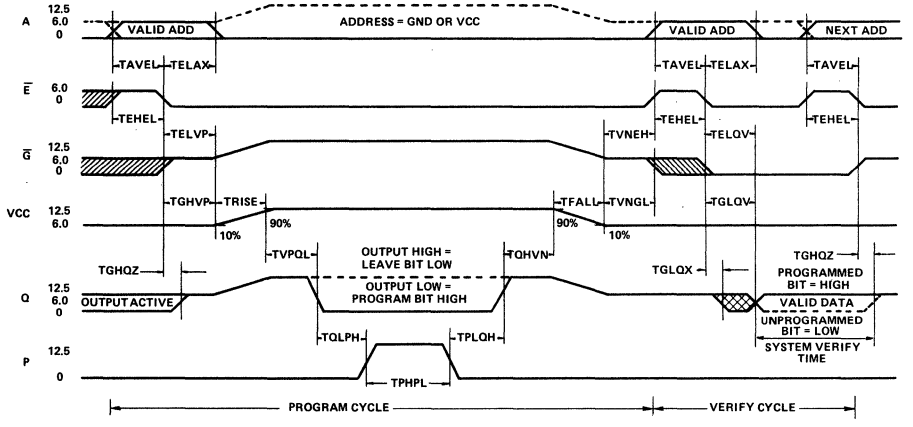
PROGRAMMING SYSTEM TIMING

SYMBOLS	PARAMETER	MIN	MAX	UNITS
TAVEL	Address Set-up Time	500		ns
TELAX	Address Hold Time	500		ns
TEHEL	Chip Enable High Time	500		ns
TELVP	Chip Enable Low to VCC Rising Delay	500		ns
TGHVP	Output Enable High to VCC Rising Delay	500		ns
TGHQZ	Output Disable Time		150	ns
TRISE	VCC Rise Time (to PGM Voltage)	1.0		µs
TVPQL	VCC High (PGM) to Output Low Delay	500		ns
TQLPH	Programming Data Setup Time	500		ns
TPHPL	Programming Pulse Width	450	550	µs
TPLQH	Programming Data Hold Time	500		ns
TQHVN	Output High to VCC Normal Delay	500		ns
TFALL	VCC Fall Time (to Normal VCC)	1.0		µs
TVNEH	VCC Normal to Chip Enable High Delay	500		ns
TVNGL	VCC Normal to Output Enable Low Delay	500		ns
TELQV	Chip Enable Access Time		500	ns
TGLQV	Output Enable Access Time		500	ns
TGLQX	Output Enable Time		150	ns

LOW VOLTAGE VERIFY CYCLE



PROGRAM AND VERIFY CYCLE



HARRIS

HM-6616

PRELIMINARY

2K x 8 CMOS PROM

Features

- LOW STANDBY AND OPERATING POWER
  - ICCSB - 50μA/100μA
  - ICCOP - 13mA/MHz
- FAST ACCESS TIME — 90/120 nsec
- INDUSTRY STANDARD PINOUT
- SINGLE 5.0 VOLT SUPPLY
- TTL COMPATIBLE INPUTS
- HIGH OUTPUT DRIVE — 12 LSTTL LOADS
- SYNCHRONOUS OPERATION
- ON-CHIP ADDRESS LATCHES
- SEPARATE OUTPUT ENABLE
- FULL INDUSTRIAL AND MILITARY TEMPERATURE RANGES

Description

The HM-6616 is a 16,384 bit fuse link CMOS PROM in a 2K word by 8 bit/word format with "Three State" outputs. This PROM is available in the standard 0.600 inch wide 24-Pin DIP, the 0.300 inch wide slimline DIP, and the JEDEC standard 32-Pin LCC.

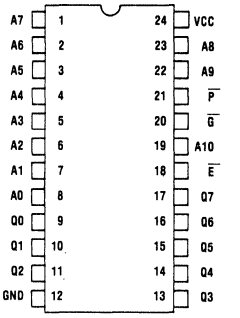
The HM-6616 utilizes a synchronous design technique. This includes on-chip address latches and a separate output enable control which makes this device ideal for applications utilizing recent generation microprocessors. This design technique, combined with the Harris advanced self-aligned silicon gate CMOS process technology offers ultra-low standby current. Low ICCSB is ideal for battery applications or other systems with low power requirements.

The Harris polysilicon fuse link technology is utilized on this and all other Harris CMOS PROMS. This gives the user a PROM with permanent, stable storage characteristics over the full industrial and military temperature and voltage ranges. Polysilicon fuse technology combined with the low power characteristics of CMOS provides an excellent alternative to standard Bipolar PROMS or NMOS EPROMS.

All bits are manufactured storing a logical "0" and can be selectively programmed for a logical "1" at any bit location.

Pinout

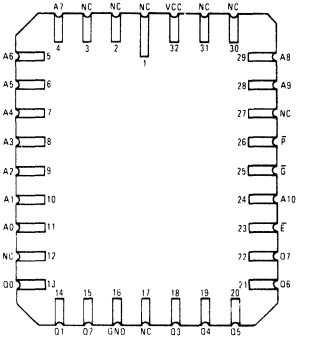
TOP VIEW



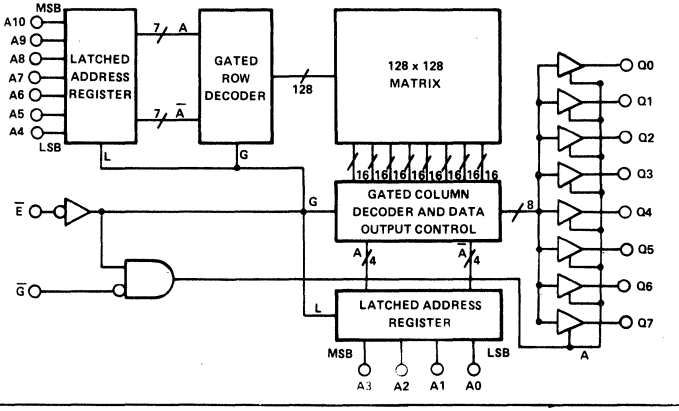
PIN NAMES

A	Address Input	Ḡ	Output Enable
Q	Data Output	P̄	Program Enable
Ē	Chip Enable		(P̄ = VCC except during Programming)

TOP VIEW - LCC



Functional Diagram



ALL LINES POSITIVE LOGIC:
ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH OUTPUT ACTIVE

ADDRESS LATCHES AND GATED DECODERS:
LATCH ON FALLING EDGE OF Ē
GATE ON FALLING EDGE OF Ḡ

P̄ = VCC EXCEPT DURING PROGRAMMING

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage	+7.0 Volts
Input/Output Voltage Applied	GND−0.3V to VCC+0.3V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military — HM-6616-2/-8	−55°C to +125°C
Industrial — HM-6616-9	−40°C to +85°C
Operating Voltage Range	+4V to +7V

**CAUTION: Stresses above those listed under the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

D.C. ELECTRICAL CHARACTERISTICS VCC = 5.0V ±10%; T_A = Industrial −40°C to +85°C (HM-6616-9)
= Military −55°C to +125°C (HM-6616-2/-8)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.4		V	
VIL	Logical Zero Input Voltage		0.8	V	
VOH	Logical One Output Voltage	2.4		V	IOH = −2.0 mA
VOL	Logical Zero Output Voltage		0.4	V	IOL = +4.8 mA
II	Input Leakage	−1.0	1.0	μA	0V≤VIN≤VCC
IOZ	Output Leakage	−1.0	1.0	μA	0V≤VO≤VCC $\overline{G}$ = HIGH
ICCSB	Standby Power Supply Current		100	μA	VIN = VCC or GND VCC = 5.5 V IO = 0
ICCOP	Operating Power Supply Current		15	mA	f = 1 MHz VCC = 5.5 V IO = 0 VIN = VCC or GND
CIN	Input Capacitance*		10	pF	f = 1 MHz VIN = VCC or GND
COUT	Output Capactiance*		12	pF	f = 1 MHz VIN = VCC or GND

*Guaranteed and sampled, but not 100% tested.

A.C. ELECTRICAL CHARACTERISTICS VCC = 5.0V ±10%; T_A = Industrial −40°C to +85°C (HM-6616-9)
= Military −55°C to +125°C (HM-6616-2/-8)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TAVQV	Address Access Time		140	ns	see notes 1,2
TELQV	Chip Enable Access Time		120	ns	
TELQX	Chip Enable Time	5		ns	
TAVEL	Address Setup Time	20		ns	
TELAX	Address Hold Time	25		ns	
TELEH	Chip Enable Low Width	120		ns	
TEHEL	Chip Enable High Width	40		ns	
TELEL	Cycle Time	160		ns	
TGLQV	Output Access Time		50	ns	
TGLQX	Output Enable Time	5		ns	
TGHQZ	Output Disable Time		50	ns	
TEHQZ	Chip Enable Disable Time		50	ns	

NOTE 1: All A.C. parameters tested at worst case limits and per test circuits and definitions in Figures 1 and 2.
NOTE 2: Input test signals must switch between 0V and 3.0V. Input rise and fall times must be <5 nsec.

Switching Waveforms

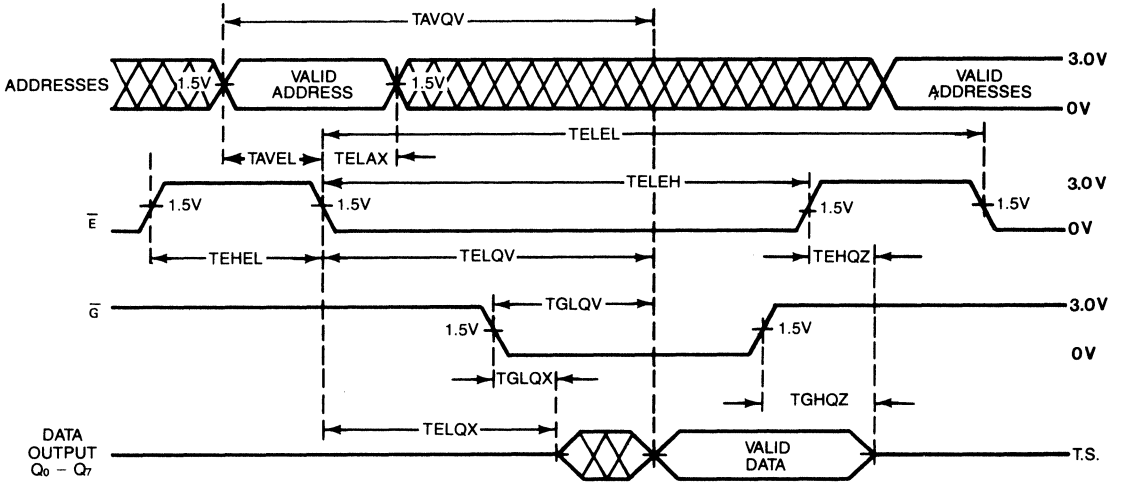


Figure 1 Read Cycle

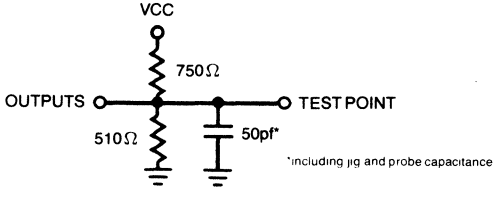


Figure 2 Output Test Circuit

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage	+7.0 Volts
Input/Output Voltage Applied	GND−0.3V to VCC+0.3V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military — HM-6616-2/-8	−55°C to +125°C
Industrial — HM-6616-9	−40°C to +85°C
Operating Voltage Range	+4V to +7V

**CAUTION: Stresses above those listed under the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

D.C. ELECTRICAL CHARACTERISTICS VCC = 5.0V ±10%; T_A = Industrial −40°C to +85°C (HM-6616B-9)
= Military −55°C to +125°C (HM-6616B-2/-8)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.4		V	
VIL	Logical Zero Input Voltage		0.8	V	
VOH	Logical One Output Voltage	2.4		V	IOH = −2.0 mA
VOL	Logical Zero Output Voltage		0.4	V	IOL = +4.8 mA
II	Input Leakage	−1.0	1.0	μA	0V≤VIN≤VCC
IOZ	Output Leakage	−1.0	1.0	μA	0V≤VO≤VCC $\overline{G}$ = HIGH
ICCSB	Standby Power Supply Current		50	μA	VIN = VCC or GND VCC = 5.5 V IO = 0
ICCOP	Operating Power Supply Current		15	mA	f = 1 MHz VCC = 5.5 V IO = 0 VIN = VCC or GND
CIN	Input Capacitance*		10	pF	f = 1 MHz VIN = VCC or GND
COUT	Output Capactiance*		12	pF	f = 1 MHz VIN = VCC or GND

*Guaranteed and sampled, but not 100% tested.

A.C. ELECTRICAL CHARACTERISTICS VCC = 5.0V ±10%; T_A = Industrial −40°C to +85°C (HM-6616B-9)
= Military −55°C to +125°C (HM-6616B-2/-8)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TAVQV	Address Access Time		105	ns	see notes 1,2
TELQV	Chip Enable Access Time		90	ns	
TELQX	Chip Enable Time	5		ns	
TAVEL	Address Setup Time	15		ns	
TELAX	Address Hold Time	20		ns	
TELEH	Chip Enable Low Width	90		ns	
TEHEL	Chip Enable High Width	30		ns	
TELEL	Cycle Time	120		ns	
TGLQV	Output Access Time		40	ns	
TGLQX	Output Enable Time	5		ns	
TGHQZ	Output Disable Time		40	ns	
TEHQZ	Chip Enable Disable Time		45	ns	

NOTE 1: All A.C. parameters tested at worst case limits and per test circuits and definitions in Figures 1 and 2
NOTE 2: Input test signals must switch between 0V and 3.0V. Input rise and fall times must be <5 nsec

Switching Waveforms

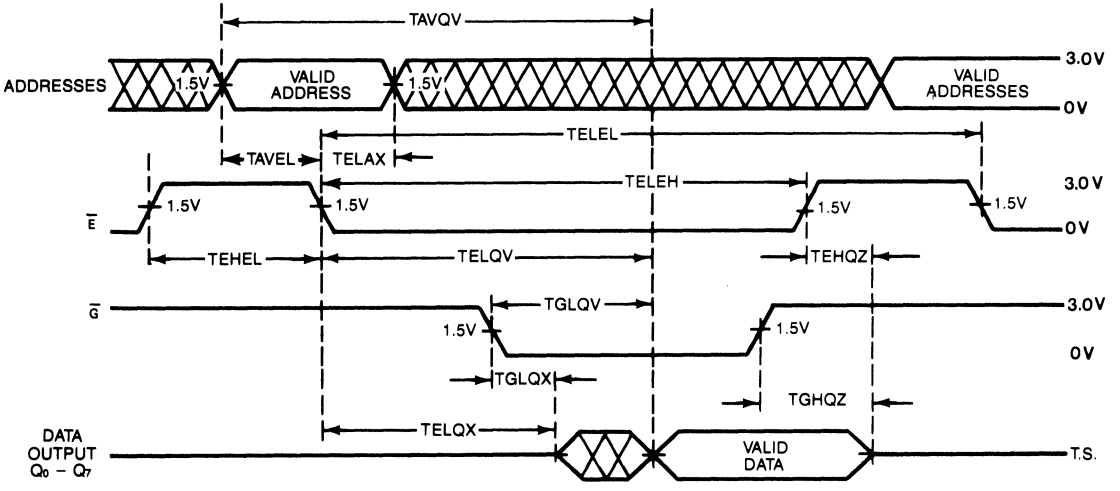


Figure 1 Read Cycle

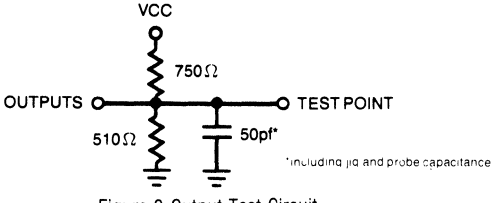


Figure 2 Output Test Circuit

HM-6616 CMOS PROM Programming Algorithm

The HM-6616 PROM is manufactured with all bits storing a logical "0" (output low). Any desired bit can be selectively programmed to a logical "1" (output high) by following the procedure shown below. One may build their own programmer to satisfy the specifications shown, or use any of the approved commercially available programmers.

PROGRAM SEQUENCE OF EVENTS

1) Apply V_{CC}(pin 24) = VCC1 to the PROM.
2) Read all fuse locations to verify (blank check) a 100% V_{OL} (unprogrammed) condition.
3) Place the PROM in the initial state for programming. $\overline{E}$ = VIH, $\overline{P}$ = VIH, $\overline{G}$ = VIL.
4) Apply the current binary address for the word to be programmed. An open circuit should not be used to address the PROM.
5) Apply $\overline{E}$ = VIL after a delay of td to access the addressed word.
6) Address may be held throughout cycle, but must be held at least time td (address hold time), after $\overline{E}$ = VIL.
7) After a delay of td tristate the outputs by applying $\overline{G}$ = VIH.
8) After a delay of td apply $\overline{P}$ = VIL.
9) After a delay of td raise VCC(pin 24) to VCCPROG with rise time = tr. All signals at VIH should track VCC(pin 24) within VCC-2V to VCC+0.3V (including outputs - pull-up resistors Rn to VCC would suffice).
10) After a delay of td pull the output to be programmed to VIL. After a duration tpw, allow the output to be pulled to VIH through the pull-up resistor Rn.
11) Repeat step 10 for all other bits to be programmed in the addressed word.
12) Lower Vcc(pin 24) to VCC1 with a fall time tf. Signals at VIH should track VCC (pin 24) in range VCC-2V to VCC+0.3V.
13) After a delay of td apply $\overline{E}$ = VIH for duration of TEHEL, and the apply $\overline{E}$ = VIL.
14) After a delay = TELPH1, apply $\overline{P}$ = VIH.
15) After a delay of td apply $\overline{G}$ = VIL. Following a delay of td examine the outputs for correct data.
16) If any location verifies incorrectly, repeat steps 4 through 15 (attempting to program only those bits in the word which verified incorrectly) up to a maximum of eight attempts for any given word. If a word does not program within eight attempts, it should be considered a programming reject.
17) Repeat steps 4 through 16 for all other words in the PROM.

POST PROGRAMMING VERIFICATION

18) Place the PROM in the post-programming verify mode. $\overline{E}$ = VIH, $\overline{G}$ = VIL, $\overline{P}$ = VIH. VCC(pin 24) = VCC1.
19) Apply the correct binary address of the word to be verified.
20) After a delay of td, apply $\overline{E}$ = VIL.
21) After a delay of td apply $\overline{G}$ = VIH to disable the outputs (outputs are tied to VCC through pull-up resistors Rn).
22) After a delay of td apply $\overline{P}$ = VIL.
23) After a delay of td apply $\overline{E}$ = VIH for duration TEHEL, then apply $\overline{E}$ = VIL.
24) After a delay = TELPH2 apply $\overline{P}$ = VIH.
25) After a delay of td apply $\overline{G}$ = VIL to enable the outputs. After a delay of td examine the outputs for correct data.
26) Repeat steps 19 through 25 for all possible address locations.

POST PROGRAMMING READ

27) Apply VCC2 = 4.0V to VCC(pin 24).
28) After a delay of td, apply $\overline{E}$ = VIH.
29) Apply the correct binary address of the word to be read.
30) After a delay of TAVEL, apply $\overline{E}$ = VIL.
31) After a delay of TELQV, examine the outputs for correct data. If any bit verifies incorrectly, the device is to be considered a programming reject.
32) Repeat steps 28 thru 31 for all other words in the PROM.
33) Repeat steps 27 thru 32 for VCC2 = 6.0V applied to VCC(pin 24).

Figure 3 — Programming and Verify Cycle

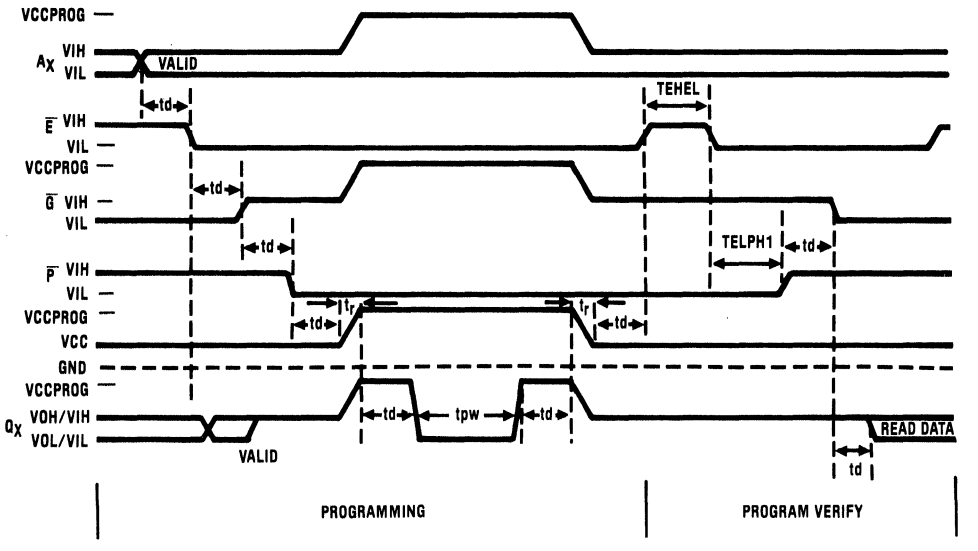
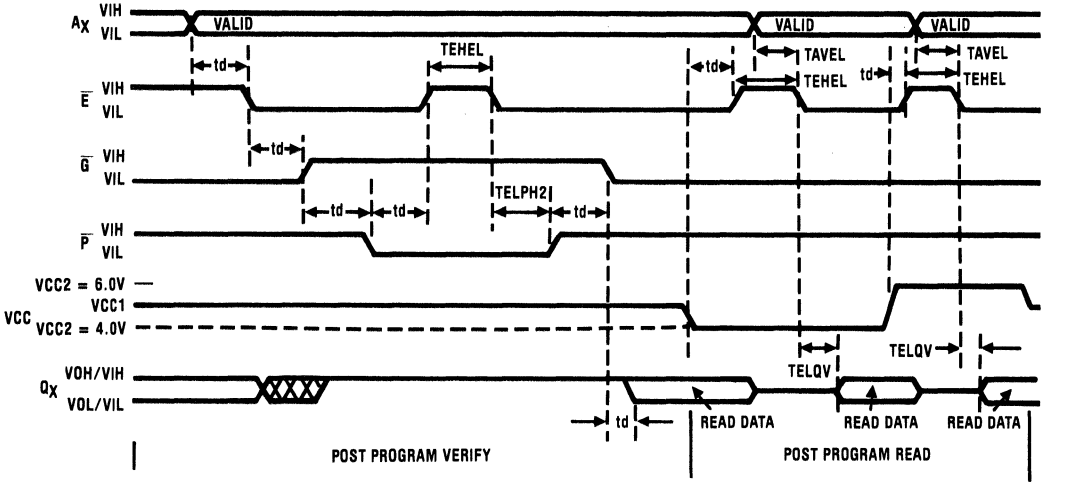


Figure 4 — Post Programming Verify & Read Cycle



PROGRAMMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	TYP.	MAX.	UNITS
VIL VIH (1)	Input "0" Voltage "1"	0.0 VCC-2	0.2 VCC	0.8 VCC+0.3	V V
VCCPROG(2) VCC1 VCC2 (3)	Programming VCC Operating VCC Special Verify VCC	13.5 4.5 4.0	14.0 5.0 ----	14.0 5.5 6.0	V V V
td	Delay Time	1.0	1.0	----	us
tr tf	Programming VCC Rise and Fall Times	1.0 1.0	10.0 10.0	10.0 10.0	us us
TEHEL	Chip Enable Pulse Width	50	----	----	ns
TAVEL	Address valid to Chip Enable low time	20	----	----	ns
TELQV	Chip Enable low to Output Valid time	----	----	120	ns
TELPH1 (4) TELPH2 (5)	$\overline{E}$ Low to $\overline{P}$ High Time	400 5.0	500 5.0	600 10.0	us us
tpw (6)	Programming Pulse Width	0.9	1.0	1.1	ms
IIP	Input Leakage at VCC=VCCPROG	−10	+1.0	10	uA
IOP	Data Output Current at VCC = VCCProg	----	−5.0	−10	mA
Rn (7)	Output pull-up resistor	5	10	15	kohms
Ta	Ambient Temperature	----	25	----	°C

Notes: 1) All inputs must track VCC(pin 24) within these limits
2) VCCPROG must be capable of supplying 500mA.
3) See steps 27 thru 33 of the programming algorithm.
4) See steps 13 & 14 of the programming algorithm.
5) See steps 23 & 24 of the programming algorithm.
6) See step 10 of the programming algorithm.
7) All outputs should be pulled up to VCC thru a resistor of value Rn.

HARRIS

HM-6664

8K x 8 CMOS Fuse Link PROM

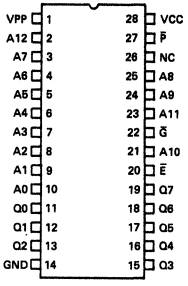
Preview

Features

- 175ns MAXIMUM ADDRESS ACCESS TIME
- LOW STANDBY CURRENT - 100μa MAXIMUM OVER THE VOLTAGE AND TEMPERATURE RANGE
- LOW OPERATING CURRENT - 10ma AT 1MHz
- JEDEC STANDARD 28-PIN DIP
- PIN COMPATIBLE WITH 2764 UV EPROM
- ASYNCHRONOUS OPERATION
- "THREE STATE" OUTPUT CONTROL WITH $\overline{G}$, AND $\overline{E}$
- GATED INPUTS - REMOVING THE NEED FOR PULL-UP OR PULL-DOWN RESISTORS
- SELF-POWER DOWN IN THE READ MODE

Pinout

TOP VIEW DIP



Description

The HM-6664 is a 65,536 bit fuse link CMOS PROM in an 8K word by 8 bit/word format with "Three State" outputs. This PROM is available in the JEDEC standard 28 pin 0.600" wide DIP.

The HM-6664 utilizes advanced design techniques coupled with the Harris advanced self-aligned silicon gate CMOS process technology. This provides a high speed PROM with ultra-low standby current. Low ICCSB is ideal for battery applications or other systems with low power requirements.

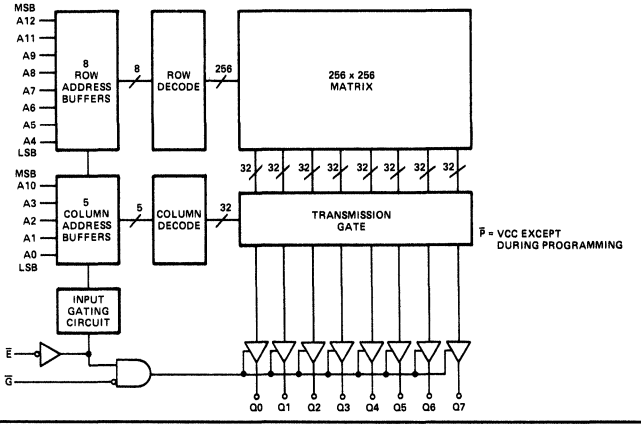
The Harris polysilicon fuse link technology is utilized on this and all other Harris CMOS PROMS. This gives the user a PROM with permanent, stable storage characteristics over the full industrial and military temperature and voltage ranges. Polysilicon fuse technology combined with the low power characteristics of CMOS provides an excellent alternative to standard Bipolar PROMS or NMOS EPROMS.

This PROM has a chip enable input $\overline{E}$ and an output enable input $\overline{G}$. The output enable input is used to "Three State" the output buffers by bringing $\overline{G}$ high. Bringing the chip enable input $\overline{E}$ high will "Three State" the output buffers, place the device in the standby power mode and gate the input buffers. Gated input buffers allow the user to float the inputs after chip enable $\overline{E}$ has gone high without exceeding the ICCSB specification due to excessive current drain in the input buffers. This eliminates the need for pull-up or pull-down resistors.

In addition, there is an input edge activated, retriggerable one-shot circuit internal to the HM-6664 which automatically reduces the supply current to the power down standby mode (ICCPD) after an address transition has been made and no further input transitions are made for approximately 1 micro second. The device will stay in the power down mode until another input transition takes place.

All bits are manufactured storing a logical "0" and can be selectively programmed for a logical "1" at any bit location.

Functional Diagram



Data Entry Formats for Harris Custom Programming*

For Harris to custom program to a user data pattern specification, the user must supply the data in one of the following formats:

1. Master PROM of same organization and pinout as device ordered. Two pieces required, three preferred.
2. Paper tape in Binary or ASCII BPNF.

* BINARY PAPER TAPE FORMAT

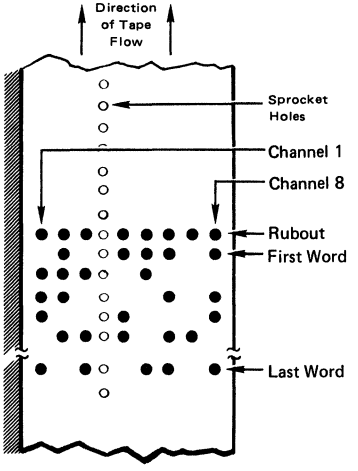
- A minimum of six inches of leader.
- A rubout (all eight locations punched).
- Data words beginning with the first word (word "0"), proceeding sequentially, ending with the last word (word "N"), with no interruptions or extraneous characters of any kind.
- Specify whether a punched hole is a VOH = "1" = logic high or is a VOL = "0" = logic low.
- A minimum trailer of six inches of tape.

* ASCII BPNF FORMAT

- A minimum leader of twenty rubouts (all eight locations punched).
- Any characters desired (none necessary) except "B".
- Data words beginning with the first word (word "0"), proceeding sequentially, ending with the last word (word "N").
- Data words consist of:
  1. The character "B" denoting the beginning of a data word.
  2. A sequence of characters, only "P" or "N", one character for each bit in the word.
  3. The character "F" denoting the finish of the data word.
- No extraneous characters of any kind may appear within a data word (between any "B" and the next "F").
- Errors may be deleted by rubouts superimposed over the entire word including the "B", and beginning the word again with a new "B".
- Any text of any kind (except the character "B") is allowed between data words (between any "F" and the next "B"), including carriage return and line feed.
- A minimum trailer of twenty-five rubouts.
- Specify whether a "P" is a "1" = VOH = logic high or is a "0" = VOL = logic low.
- The use of even or odd parity is optional.

* *Harris can not assume responsibility for PROMs programmed to data tapes or masters which contain errors. The user must insure the accuracy of the data provided to Harris. Harris guarantees that the programmed PROMs will contain the information provided if either of the following formats are followed.*

BINARY PAPER TAPE EXAMPLE



Punched Hole = "0" = VOL = Logic Low

Word					PROM Output Data ①							
AX ··· A2	A1	A0		Channel Output	8 O_8	7 O_7	6 O_6	5 O_5	4 O_4	3 O_3	2 O_2	1 O_1
0 ···· 0	0	0	First		0	1	0	0	0	1	0	1
0 ···· 0	0	1	Second		1	1	1	0	1	0	0	0
0 ···· 0	1	0	Third		0	1	0	1	1	1	0	0
0 ···· 0	1	1	Fourth		0	1	1	1	0	1	1	0
0 ···· 1	0	0	Fifth		1	0	0	1	0	0	0	1
1 ···· 1	1	1	Last		0	1	0	0	1	0	1	0

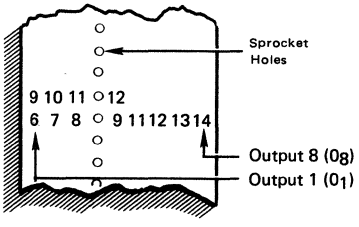
NOTES:

① PROMs with 4 bit wide data outputs require punching only first 4 channels on tape (Channels 1 thru 4).

② On HARRIS PROMs O_X (Example: O_1) designates a respective output pin on the device. O_1 (Output 1) is always LSB.

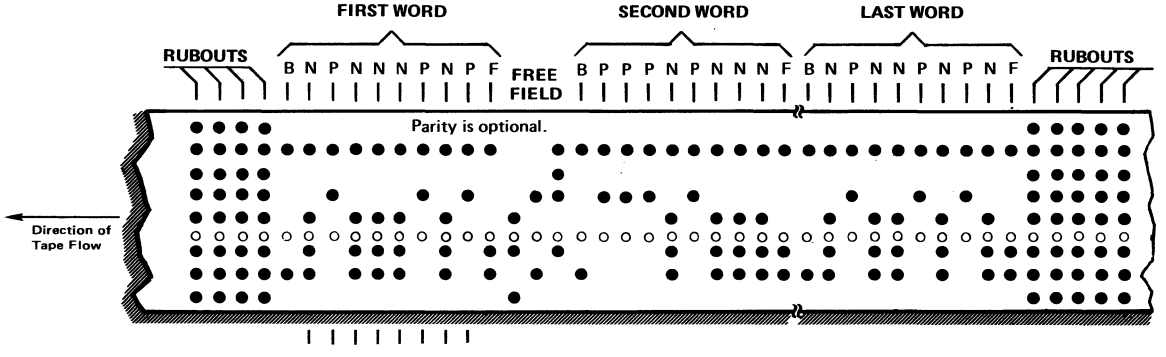
DEVICE OUTPUT PACKAGE PINS

EXAMPLE:



Package	Device Type
16 Pin CMOS	HM-6611

ASCII BPNF PAPER TAPE EXAMPLE



EXAMPLE	PACKAGE TYPE	DEVICE OUTPUT PINS
HM-6611	16 Pin Pkg.	12 11 10 9 (MOS)
HM-7649	20 Pin Pkg.	14 13 1211 9 8 7 6

Truth Table
Character "D" = "1" = VOH = Logic High
Character "V" = "0" = VOL = Logic Low

Word				PROM Outputs Data ①							
AX ···· A2	A1	A0		O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
0 ····· 0	0	0	First	0	1	0	0	0	1	0	1
0 ····· 0	0	1	Second	1	1	1	0	1	0	0	0
1 ····· 0	1	0	Last	0	1	0	0	1	0	1	0

NOTES:
① In the ASCII BPNF format, MSB data is punched after "B". On devices with 8 outputs, O_8 (Output 8) data is punched after "B". On devices with 4 outputs, O_4 (Output 4) data is punched after "B".

HARRIS

HPL-16LC8

Preview CMOS HPL™ Harris Programmable Logic

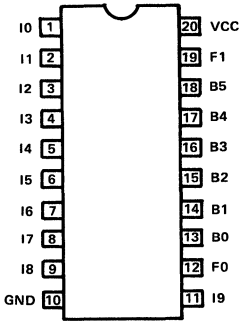
Features

- PIN & FUNCTION COMPATIBLE WITH THE BIPOLAR 16L8 PAL™
- SCALED SAJI IV CMOS PROCESS
- FAST ACCESS (INPUT TO OUTPUT) 90nsec. MAX.
- LOW STANDBY AND OPERATING POWER ICCSB 150μA ICCOP 10mA/MHz
- INDUSTRIAL AND MILITARY TEMPERATURE RANGES
- 20 PIN SLIMLINE DIP
- SECURITY FUSE FOR PATTERN PROTECTION
- TTL/CMOS COMPATIBLE INPUTS/OUTPUTS FOR MIXED SYSTEM COMPATIBILITY
- RELIABLE POLYSILICON FUSE TECHNOLOGY
- LOGIC PATHS TESTED TO INSURE FUNCTIONALITY

Applications

- RANDOM LOGIC REPLACEMENT
- CODE CONVERTORS
- ADDRESS DECODING
- FAULT DETECTORS
- BOOLEAN FUNCTION GENERATORS
- DIGITAL MULTIPLEXERS
- PARITY GENERATORS
- PATTERN RECOGNITION
- ROM PATCHING

Pinout



Description

The HPL-16LC8 is a programmable CMOS logic device which is designed to provide a high performance, low power alternative to the industry standard bipolar 16L8 programmable logic device.

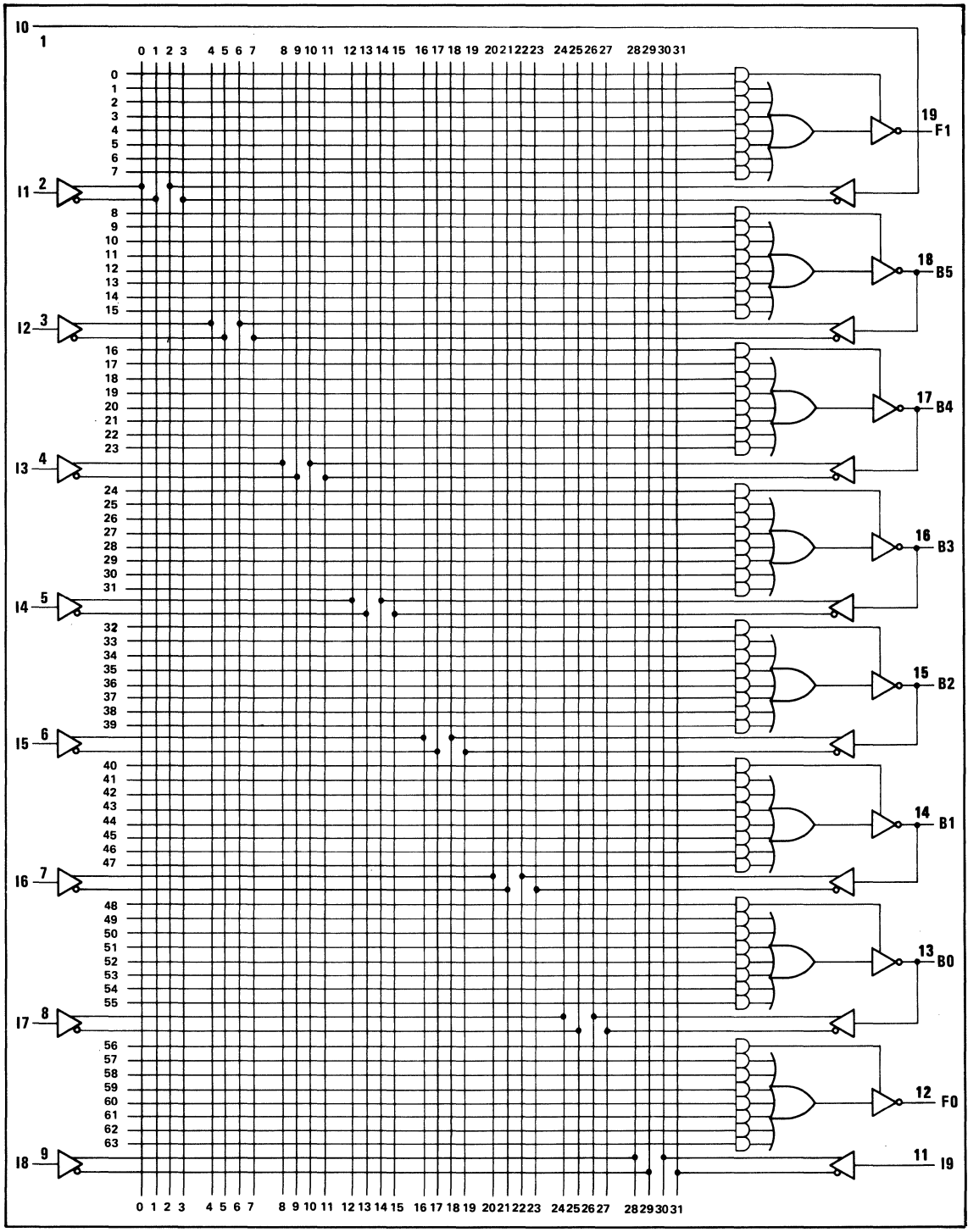
The Harris polysilicon fuse link technology provides a permanent fuse with stable storage characteristics over the full industrial/military temperature and voltage ranges. Like all Harris Programmable Logic (HPL), this device contains unique test circuitry developed by Harris which allows full AC, DC and functional testing before programming.

On-chip automatic power-down circuitry places internal circuitry into an ultra-low ICCSB power mode after output data becomes valid.

HPL is a trademark of Harris Corporation
PAL is a trademark of MMI
CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Functional Diagram

HPL-16LC8



HARRIS HPL-16RC4, 16RC6, 16RC8

Preview CMOS HPL™ Harris Programmable Logic

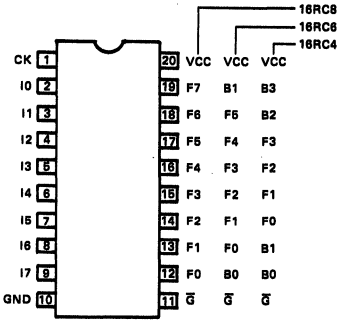
Features

- PIN & FUNCTION COMPATIBLE WITH THE BIPOLAR 16R4, 16R6, 16R8 PALs™
- SCALED SAJI IV CMOS PROCESS
- FAST ACCESS (INPUT TO OUTPUT) 90nsec. MAX.
- LOW STANDBY AND OPERATING POWER ICCSB 150μA ICCOP 10mA/MHz
- INDUSTRIAL AND MILITARY TEMPERATURE RANGES
- 20 PIN SLIMLINE DIP
- SECURITY FUSE FOR PATTERN PROTECTION
- TTL/CMOS COMPATIBLE INPUTS/OUTPUTS FOR MIXED SYSTEM COMPATIBILITY
- RELIABLE POLYSILICON FUSE TECHNOLOGY
- LOGIC PATHS TESTED TO INSURE FUNCTIONALITY

Applications

- RANDOM LOGIC REPLACEMENT
- CODE CONVERTORS
- ADDRESS DECODING
- CUSTOM SHIFT REGISTERS
- BOOLEAN FUNCTION GENERATORS
- DIGITAL MULTIPLEXERS
- PARITY GENERATORS
- PATTERN RECOGNITION
- STATE MACHINE DESIGN

Pinout



Description

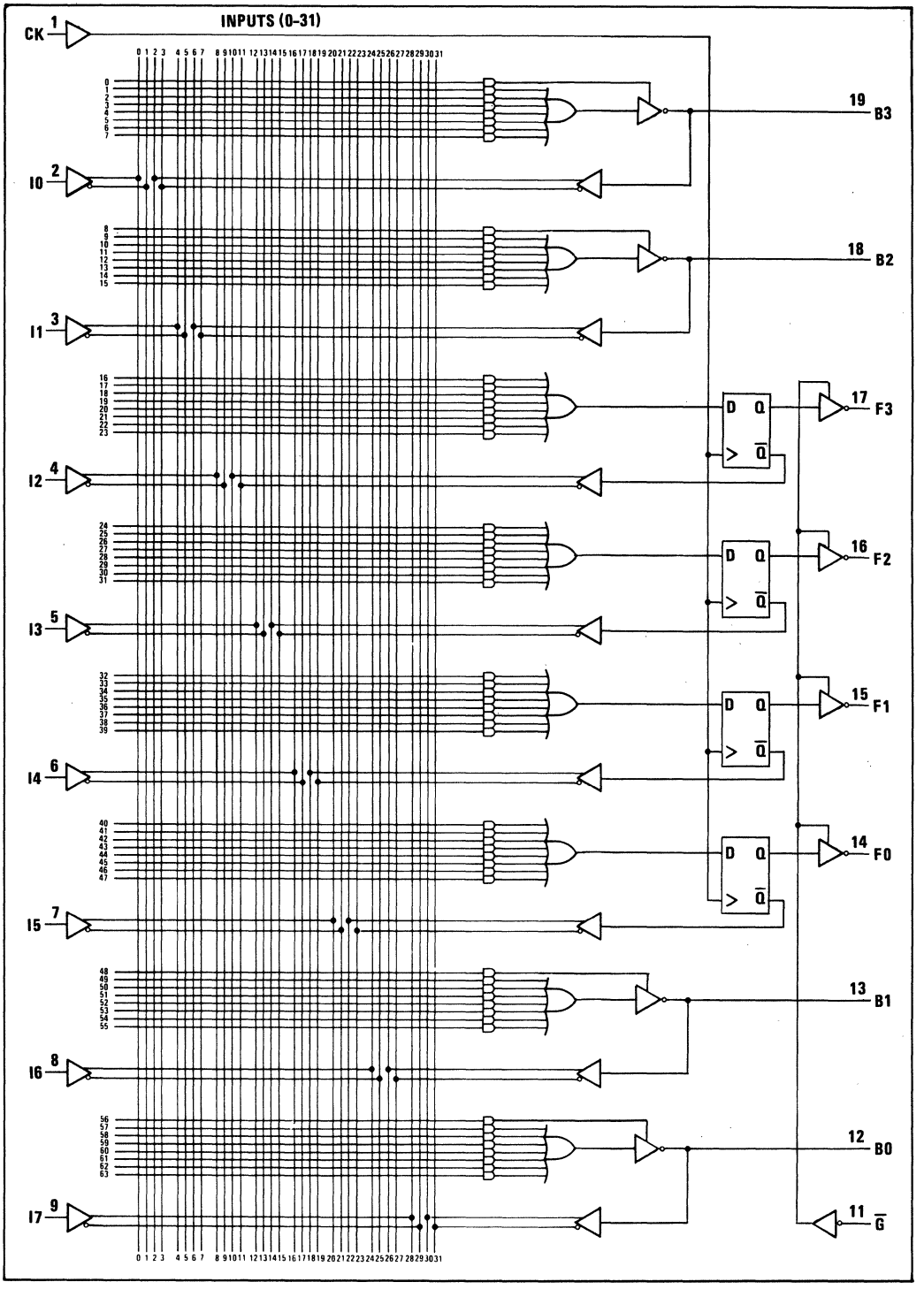
The HPL-16RC4, 16RC6 and 16RC8 are programmable CMOS logic devices which are designed to provide a high performance, low power alternative to the industry standard bipolar 16R4, 16R6 and 16R8 programmable logic devices.

The Harris polysilicon fuse link technology provides a permanent fuse with stable storage characteristics over the full industrial/military temperature and voltage ranges. Like all Harris Programmable Logic (HPL), these devices contain unique test circuitry developed by Harris which allows full AC, DC and functional testing before programming.

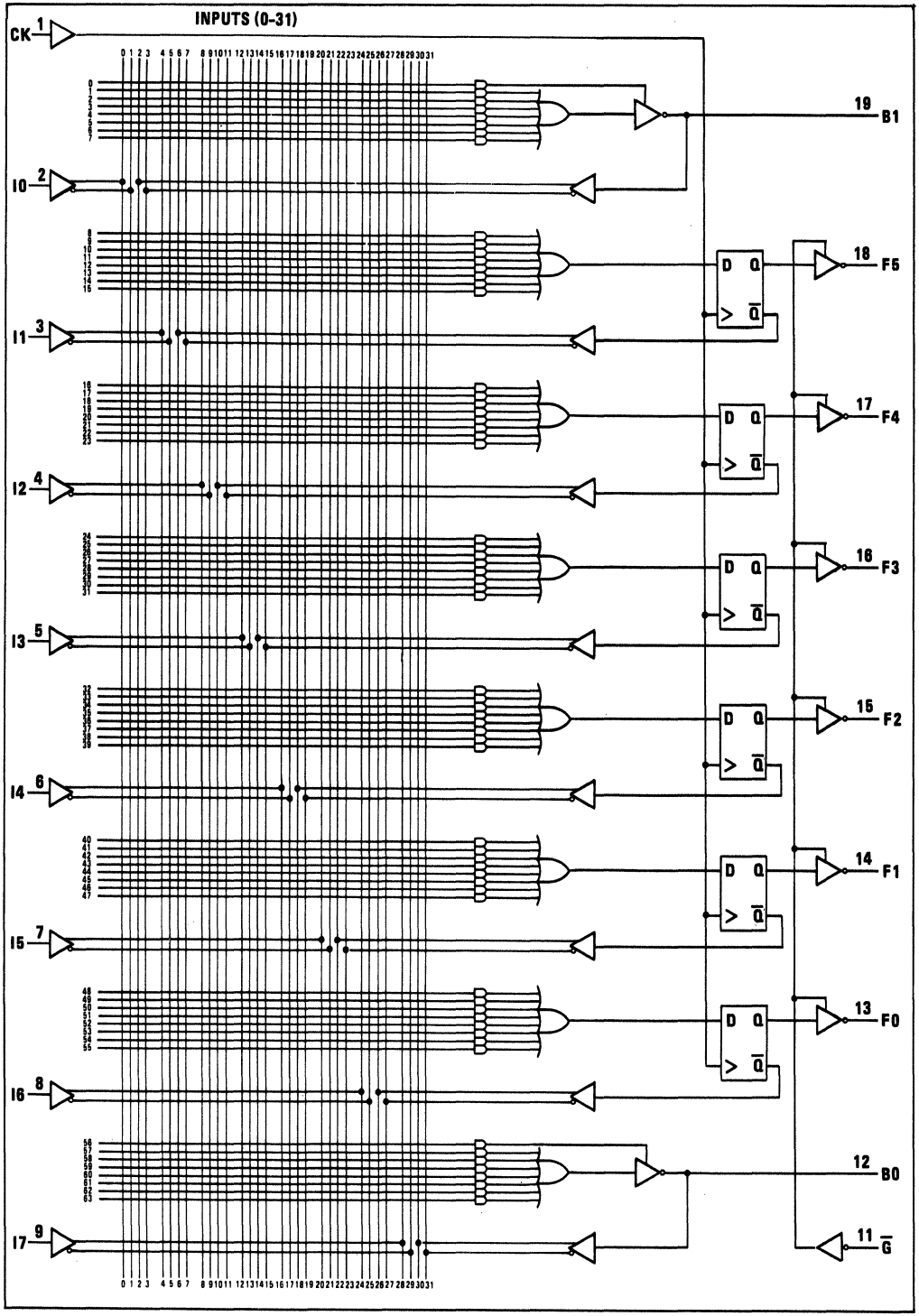
On-chip automatic power-down circuitry places internal circuitry into an ultra-low ICCSB power mode after output data becomes valid.

HPL is a trademark of Harris Corporation
PAL is a trademark of MMI
CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

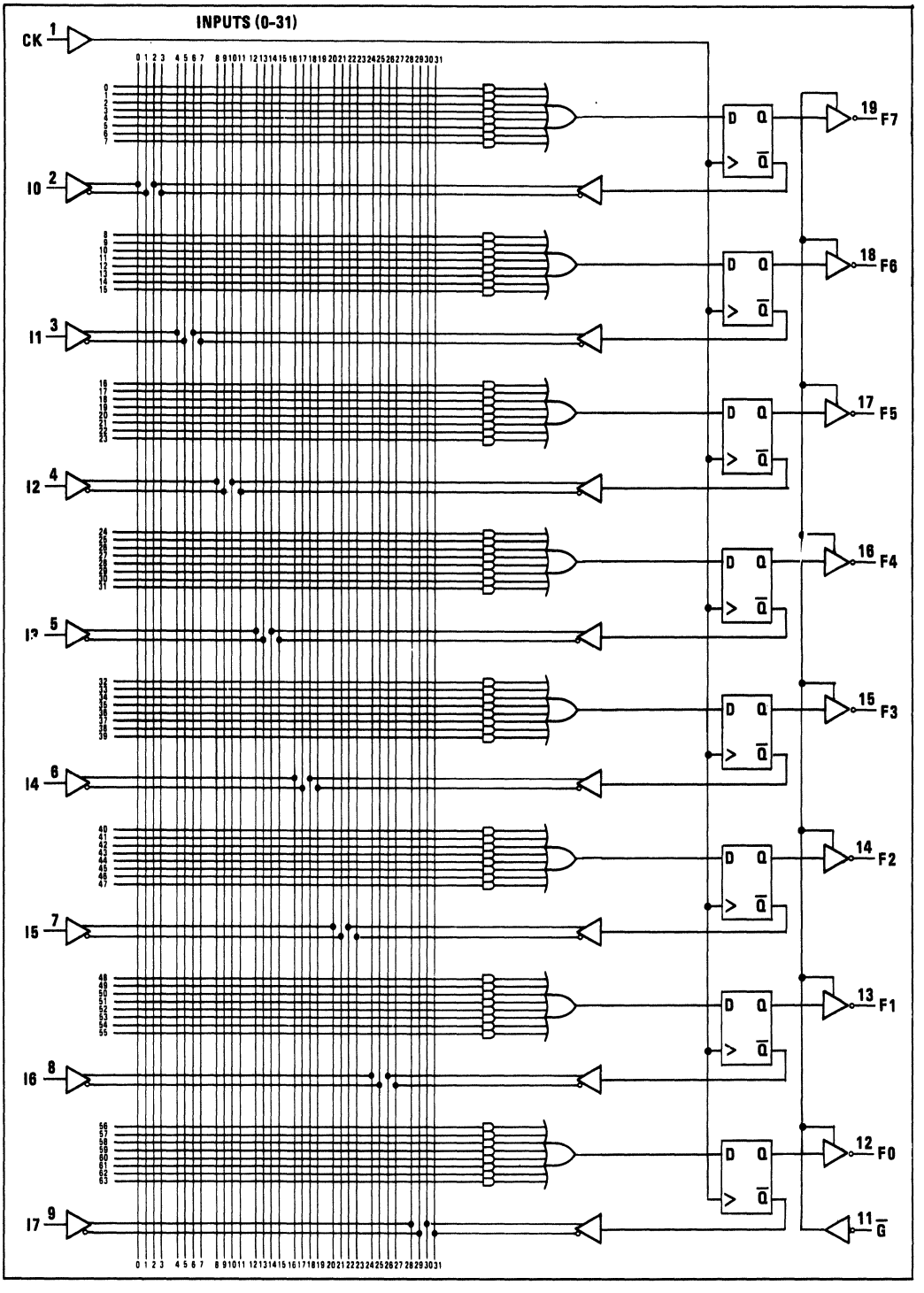
HPL-16RC4


INPUTS (0-31)
CK 1
I0 2
I1 3
I2 4
I3 5
I4 6
I5 7
I6 8
I7 9
19 B3
18 B2
17 F3
16 F2
15 F1
14 F0
13 B1
12 B0
11 G
D Q
Q

HPL-16RC6


INPUTS (0-31)
CK 1
I0 2
I1 3
I2 4
I3 5
I4 6
I5 7
I6 8
I7 9
19 B1
18 F5
17 F4
16 F3
15 F2
14 F1
13 F0
12 B0
11 G
D Q
Q

HPL-16RC8


INPUTS (0-31)
CK 1
I0 2
I1 3
I2 4
I3 5
I4 6
I5 7
I6 8
I7 9
D Q
> Q
19 F7
18 F6
17 F5
16 F4
15 F3
14 F2
13 F1
12 F0
11 G

CMOS 80C86 Family 3

Product Index	**3-2**
CMOS 80C86 Family Harris/Intel Cross-Reference	**3-3**
Product Information	**3-4**

CMOS 80C86 Family Product Index

HARRIS 80C86 FAMILY DATA SHEETS		PAGE
80C86	16 Bit Microprocessor	3-4
82C52	Full Duplex UART	3-27
82C54	Programmable Interval Timer	3-28
82C55A	Programmable Peripheral Interface	3-43
82C59A	Priority Interrupt Controller	3-62
HD-6406	Programmable Asynchronous Communications Interface	3-76
82C82	Octal Latch	3-77
82C84A	Clock Generator/Driver	3-82
82C88	Bus Controller	3-89

PREVIEW OF FUTURE HARRIS 80C86 FAMILY PRODUCTS		
80C88	8 Bit Microprocessor	3-96
82C37A	High Performance Programmable DMA	3-97
82C83	Octal Latching Inverting Bus Driver	3-98
82C84B	Clock Generator/Driver	3-99
82C86	Octal Bus Transceiver	3-100
82C87	Octal Bus Transceiver	3-101
82C89	Bus Arbiter	3-102

HARRIS CMOS 80C86 Family
Cross-Reference

INTEL	DESCRIPTION	HARRIS EQUIVALENT
80C86 CMOS 16 Bit Microprocessor		
D8086 ID8086 MD8086/B	Commercial temp, ceramic or plastic pkg Industrial temp, ceramic or plastic pkg Military temp range, ceramic pkg with DASH 8 processing without DASH 8 processing	CD80C86 or CP80C86 ID80C86 or IP80C86 MD80C86/B MD80C86
82C54 CMOS Programmable Timer		
P8254 D8254 MD8254/B	Commercial temp, plastic pkg Commercial temp, ceramic pkg Military temp, ceramic pkg with DASH 8 processing without DASH 8 processing	CP82C54 CD82C54 MD82C54/B MD82C54
82C55A CMOS Programmable Peripheral Interface (PPI)		
P8255A D8255A P8255A-5 D8255A-5 ID8255A MD8255A/B	Commercial temp, plastic pkg, 2MHz Commercial temp, ceramic pkg, 2MHz Commercial temp, plastic pkg, 3MHz Commercial temp, ceramic pkg, 3MHz Industrial temp, ceramic pkg, 2MHz Military temp range, ceramic pkg with DASH 8 processing without DASH 8 processing	CP82C55A CD82C55A CP82C55A CD82C55A IP82C55A or ID82C55A MD82C55A/B MD82C55A
82C59A CMOS Interrupt Controller		
D8259A P8259A D8259A-2 P8259A-2 D8259A-8 P8259A-8 ID8259A MD8259A	Commercial temp range, ceramic pkg, 5MHz Commercial temp range, plastic pkg, 5MHz Commercial temp range, ceramic pkg, 8MHz Commercial temp range, plastic pkg, 8MHz Commercial temp range, ceramic pkg, 2MHz Commercial temp range, plastic pkg, 2MHz Industrial temp range, ceramic or plastic pkg Military temp, ceramic pkg with DASH 8 processing without DASH 8 processing	CD82C59A CP82C59A CD82C59A CP82C59A CD82C59A CP82C59A IP82C59A or ID82C59A MD82C59A/B MD82C59A
82C82 CMOS Octal Non-inverting Latching Bus Driver		
D8282 P8282 ID8282 MD8282/B	Commercial temp range, ceramic pkg Commercial temp range, plastic pkg Industrial temp range, ceramic pkg Military temp range, ceramic pkg with DASH 8 processing without DASH 8 processing	CD82C82 CP82C82 IP82C82 or ID82C82 MD82C82/B MD82C82
82C84A CMOS Clock Generator Driver		
P8284A D8284A ID8284A MD8284A/B	Commercial temp, plastic pkg Commercial temp, ceramic pkg Industrial temp, ceramic pkg Military temp, ceramic pkg with DASH 8 processing without DASH 8 processing	CP82C84A CD82C84A IP82C84A or ID82C84A MD82C84A/B MD82C84A
82C88 CMOS Bus Controller		
D8288 ID8288 MD8288/B	Commercial temp, ceramic or plastic pkg Industrial temp, ceramic pkg Military temp, ceramic pkg with DASH 8 processing without DASH 8 processing	DP82C88 or CD82C88 IP82C88 or ID82C88 MD82C88/B MD82C88

HARRIS

80C86

CMOS 16 BIT MICROPROCESSOR

Advance Information

Features

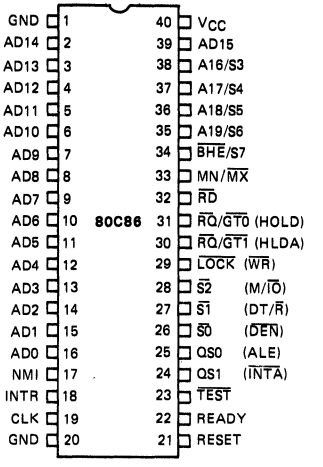
- COMPATIBLE WITH NMOS 8086
- COMPLETELY STATIC DESIGN
  - ▶ OPERATION FROM DC TO 5MHz
- LOW POWER OPERATION
  - ▶ ICCSB = 500μA MAXIMUM
  - ▶ ICCOP = 10mA/MHz TYPICAL
- 1 MBYTE OF DIRECT MEMORY ADDRESSING CAPABILITY
- 24 OPERAND ADDRESSING MODES
- BIT, BYTE, WORD, AND BLOCK MOVE OPERATIONS
- 8 and 16 BIT SIGNED/UNSIGNED ARITHMETIC
  - ▶ BINARY or DECIMAL
  - ▶ MULTIPLY and DIVIDE
- BUS-HOLD CIRCUITRY ELIMINATES PULL-UP RESISTORS
- SCALED SAJI IV CMOS PROCESS
- SINGLE 5V POWER SUPPLY
- COMMERCIAL, INDUSTRIAL and MILITARY TEMPERATURE RANGES

Description

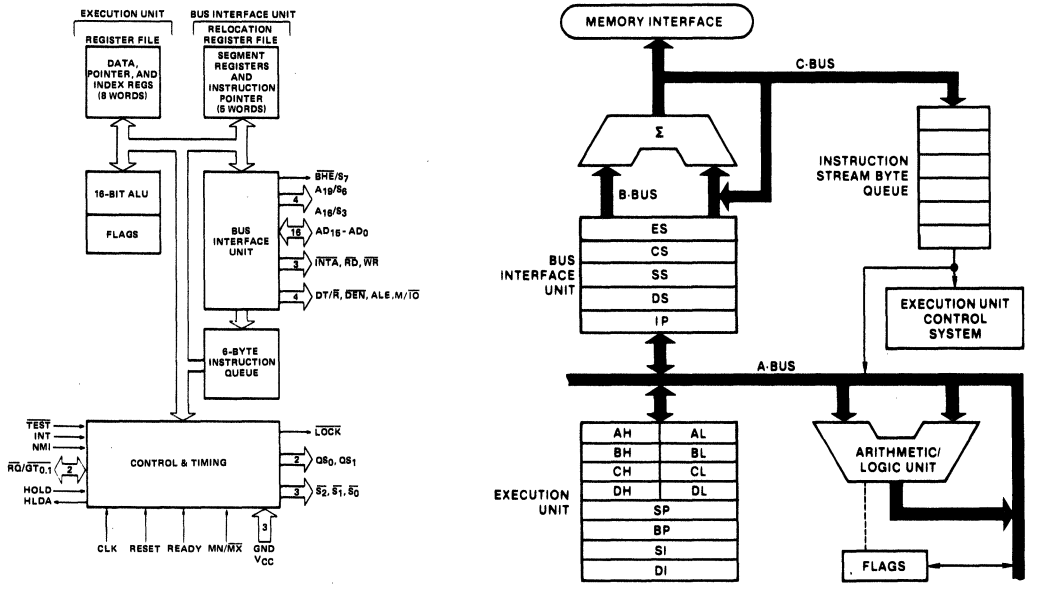
The Harris 80C86 high performance 16 bit CMOS CPU is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV).Two modes of operation, MINimum for small systems and MAXimum for larger applications such as multi-processing, allow user configuration to achieve the highest performance level. Full TTL compatibility and industry standard operation allow use of existing NMOS 8086 hardware and software designs.

Pinout

MAX (MIN)



Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Pin Description

The following pin function descriptions are for 80C86 systems in either minimum or maximum mode. The "Local Bus" in these descriptions is the direct multiplexed bus interface connection to the 80C86 (without regard to additional bus buffers).

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
AD_{15}-AD_0	2-16, 39	I/O	ADDRESS DATA BUS: These lines constitute the time multiplexed memory/IO address (T_1) and data (T_2, T_3, T_W, T_4) bus. A_0 is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D_7-D_0. It is LOW during T_1 when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use A_0 to condition chip select functions (See $\overline{BHE}$). These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge."
A_{19}/S_6 A_{18}/S_5 A_{17}/S_4 A_{16}/S_3	35-38	O	ADDRESS/STATUS: During T_1, these are the four most significant address lines for memory operations. During I/O operations these lines are LOW. During memory and I/O operations, status information is available on these lines during T_2, T_3, T_W, and T_4. The status of the interrupt enable FLAG bit (S_5) is updated at the beginning of each CLK cycle. A_{17}/S_4 and A_{16}/S_3 are encoded as shown in (Table 1). This information indicates which relocation register is presently being used for data accessing. These lines float to 3-state OFF during local bus "hold acknowledge."
$\overline{BHE}/S_7$	34	O	BUS HIGH ENABLE/STATUS: During T_1 the bus high enable signal ($\overline{BHE}$) should be used to enable data onto the most significant half of the data bus, pins D_{15}-D_8. Eight bit oriented devices tied to the upper half of the bus would normally use $\overline{BHE}$ to condition chip select functions. BHE is LOW during T_1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. The S_7 status information is available during T_2, T_3, and T_4. The signal is active LOW, and floats to 3-state OFF in "hold". It is LOW during T1 for the first interrupt acknowledge cycle. (See Table 2)
$\overline{RD}$	32	O	READ: Read strobe indicates that the processor is performing a memory of I/O read cycle, depending on the state of the $\overline{S_2}$ pin. This signal is used to read devices which reside on the 80C86 local bus. $\overline{RD}$ is active LOW during T_2, T_3, and T_W of any read cycle, and is guaranteed to remain HIGH in T_2 until the 80C86 local bus has floated. This signal floats to 3-state OFF in "hold acknowledge."
READY	22	I	READY: is the acknowledgement from the addressed memory or I/O device that will complete the data transfer. The RDY signal from memory/IO is synchronized by the 82C84A Clock Generator to form READY. This signal is active HIGH. The 80C86 READY input is not synchronized. Correct operation is not guaranteed if the setup and hold times are not met.
INTR	18	I	INTERRUPT REQUEST: a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.
$\overline{TEST}$	23	I	TEST: input is examined by the "Wait" instruction. If the $\overline{TEST}$ input is LOW execution continues, otherwise the processor waits in an "Idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
NMI	17	I	NON-MASKABLE INTERRUPT: an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	I	RESET: causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the Instruction Set description, when RESET returns LOW. RESET is internally synchronized.
CLK	19	I	CLOCK: provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
VCC	40		VCC: + 5V power supply pin.
GND	1, 20		GND: Ground Note: both must be connected.
MN/$\overline{MX}$	33	I	MINIMUM/MAXIMUM: Indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

Pin Description

The following pin function descriptions are for the 80C86/82C88 system in maximum mode (i.e., MN/$\overline{MX}$ = GND). Only the pin functions which are unique to maximum mode are described; all other pin functions are as described above.

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
$\overline{S_0}, \overline{S_1}, \overline{S_2}$	26-28	O	STATUS: active during T_4, T_1, and T_2 and is returned to the passive state (1, 1, 1) during T_3 or during T_W when READY is HIGH. This status is used by the 82C88 Bus Controller to generate all memory and I/O access control signals. Any change by $\overline{S_2}$, $\overline{S_1}$, or $\overline{S_0}$ during T_4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T_3 or T_W is used to indicate the end of a bus cycle. These signals float to 3-state OFF in "hold acknowledge. These status lines are encoded as shown in Table 3.
$\overline{RQ}/\overline{GT}_0$ $\overline{RQ}/\overline{GT}_1$	30, 31	I/O	REQUEST/GRANT: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}/\overline{GT}_0$ having higher priority than $\overline{RQ}/\overline{GT}_1$. $\overline{RQ}/\overline{GT}$ has an internal pull-up bus hold device so it may be left unconnected. The request/grant sequence is as follows (see Waveform Section): 1. A pulse of 1 CLK wide from another local bus master indicates a local bus request ("hold") to the 80C86 (pulse 1). 2. During a T_4 or T_1 clock cycle, a pulse 1 CLK wide from the 80C86 to the requesting master (pulse 2), indicates that the 80C86 has allowed the local bus to float and that it will enter the "hold acknowledge" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "hold acknowledge." 3. A pulse 1 CLK wide from the requesting master indicates to the 80C86 (pulse 3) that the "hold" request is about to end and that the 80C86 can reclaim the local bus at the next CLK. Each master-master exchange of the local bus is a sequence of 3 pulses. There must be one dead CLK cycle after each bus exchange. Pulses are active LOW. If the request is made while the CPU is performing a memory cycle, it will release the local bus during T_4 of the cycle when all the following conditions are met: 1. Request occurs on or before T_2. 2. Current cycle is not the low byte of a word (on an odd address). 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently excuting. If the local bus is idle when the request is made the two possible events will follow: 1. Local bus will be released during the next clock. 2. A memory cycle will start within three clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.
$\overline{LOCK}$	29	O	LOCK: output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and floats to 3-state OFF in "hold acknowledge." In MAX mode, $\overline{LOCK}$ is automatically generated during T_2 of the first INTA cycle and removed during T_2 of the second INTA cycle.
QS_1, QS_0	24, 25	O	QUEUE STATUS: The queue status is valid during the CLK cycle after which the queue operation is performed. QS_1, and QS_0 provide status to allow external tracking of the internal 80C86 instruction queue. Note that QS_1, QS_0 never become high impedance. QS_1 QS_0 0 (LOW) 0 — No Operation 0 1 — First Byte of Op Code from Queue 1 (HIGH) 0 — Empty the Queue 1 1 — Subsequent Byte from Queue

A_{17}/S_4	A_{16}/S_3	CHARACTERISTICS
0 (LOW)	0	Alternate Data
0	1	Stack
1 (HIGH)	0	Code or None
1	1	Data
S_6 is 0 (LOW)		

Table 1.

$\overline{BHE}$	A_0	CHARACTERISTICS
0	0	Whole word
0	1	Upper byte from/ to odd address
1	0	Lower byte from/ to even address
1	1	None

Table 2.

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	CHARACTERISTICS
0 (LOW)	0	0	Interrupt Acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1 (HIGH)	0	0	Code Access
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive

Table 3.

Pin Description

The following pin function descriptions are for the 80C86 in minimum mode (i.e. MN/$\overline{MX}$ = V_{CC}). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described above.

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
M/$\overline{IO}$	28	O	STATUS LINE: logically equivalent to S_2 in the maximum mode. It is used to distinguish a memory access from an I/O access. M/$\overline{IO}$ becomes valid in the T_4 preceding a bus cycle and remains valid until the final T_4 of the cycle (M = HIGH, IO = LOW). M/$\overline{IO}$ floats to 3-state OFF in local bus "hold acknowledge".
$\overline{WR}$	29	O	WRITE: Indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/$\overline{IO}$ signal. $\overline{WR}$ is active for T_2, T_3, and T_W of any write cycle. It is active LOW, and floats to 3-state OFF in local bus "hold acknowledge".
$\overline{INTA}$	24	O	INTERRUPT ACKNOWLEDGE: is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T_2, T_3, and T_W of each interrupt acknowledge cycle. Note that $\overline{INTA}$ is never floated.
ALE	25	O	ADDRESS LATCH ENABLE: provided by the processor to latch the address into the 82C82 address latch. It is a HIGH pulse active during T_1 of any bus cycle. Note that ALE is never floated.
DT/$\overline{R}$	27	O	DATA TRANSMIT/RECEIVE: needed in minimum system that desires to use a data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/$\overline{R}$ is equivalent to $\overline{S_1}$ in maximum mode, and its timing is the same as for M/$\overline{IO}$ (T = HIGH, R = LOW). DT/$\overline{R}$ floats to 3-state OFF in local bus "hold acknowledge."
$\overline{DEN}$	26	O	DATA ENABLE: provided as an output enable for a bus transceiver in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access and for INTA cycles. For a read or INTA cycle it is active from the middle of T_2 until the middle of T_4, while for a write cycle it is active from the beginning of T_2 until the middle of T_4. $\overline{DEN}$ floats to 3-state OFF in local bus "hold acknowledge."
HOLD HLDA	31, 30	I O	HOLD: indicates that another master is requesting a local bus "hold". To be a acknowledged, HOLD must be active HIGH. The processor receiving the "hold" will issue a "hold acknowledge" (HLDA) in the middle of a T_4 or T_1 clock cycle. Simultaneous with the issuance of HLDA, the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will LOWer HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. The same rules as for $\overline{RQ}$/$\overline{GT}$ apply regarding when the local bus will be released. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time.

Functional Description

Static Operation

All 80C86 circuitry is of static design. Internal registers, counters and latches are static and require no refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction placed on other microprocessors. The CMOS 80C86 can operate from DC to the appropriate upper frequency limit. The processor clock may be stopped in either state (high/low) and held there indefinitely. This type of operation is especially useful for system debug or power critical applications.

The 80C86 can be single stepped using only the CPU clock. This state can be maintained as long as is necessary during debug. Single step clock operation allows simple interface circuitry to provide critical information for bringing up your system.

Static design also allows very low frequency operation (down to DC). In a power critical situation, this can provide extremely low power operation since 80C86 power dissipation is directly related to operating frequency. As the system frequency is reduced, so is the operating power until, ultimately, at a DC input frequency, the 80C86 power requirement is the standby current. (500μA maximum)

Internal Architecture

The internal functions of the 80C86 processor are partitioned logically into two processing units. The first is the

Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the CPU functional diagram.

These units can interact directly but for the most part perform as separate asynchonous operational processors. The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocation. This unit also provides the basic bus control. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utilization. Up to 6 bytes of the instruction stream can be queued while waiting for decoding and execution.

The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 2 bytes in the queue, the BIU will attempt a word fetch memory cycle. This greatly reduces "dead time" on the memory bus. The queue acts as a First-In-First-Out (FIFO) buffer, from which the EU extracts instruction bytes as required. If the queue is empty (following a branch instruction, for example), the first byte into the queue immediately becomes available to the EU.

The execution unit receives pre-fetched instructions from the BIU queue and provides un-relocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage.

Memory Organization

The processor provides a 20-bit address to memory, which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra data, and stack segments of up to 64K bytes each, with each segment falling on 16-byte boundaries. (See Figure 1).

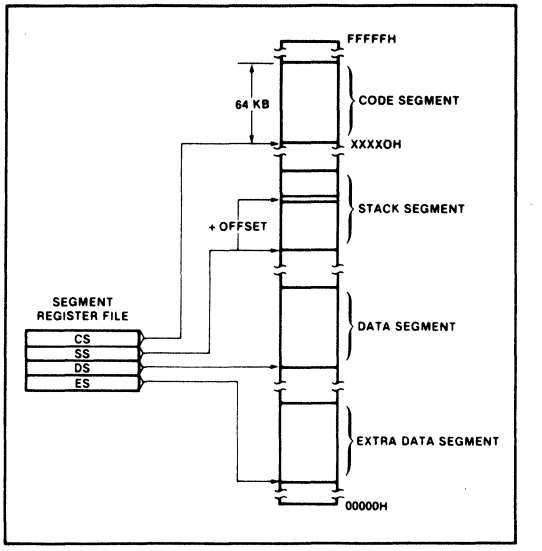


Figure 1. 80C86 Memory Organization

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to specific rules of operation. All information in one segment type share the same logical attributes (e.g. code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster, and more structured. (See Table 4).

Word (16-bit) operands can be located on even or odd address boundaries and are thus not constrained to even boundaries as is the case in many 16-bit computers. For address and data operands, the least significant byte of the

TYPE OF MEMORY REFERENCE	DEFAULT SEGMENT BASE	ALTERNATE SEGMENT BASE	OFFSET
Instruction Fetch	CS	NONE	IP
Stack Operation	SS	NONE	SP
Variable (except following)	DS	CS, ES, SS	Effective Address
String Source	DS	CS, ES, SS	SI
String Destination	ES	NONE	DI
BP Used As Base Register	SS	CS, DS, ES	Effective Address

Table 4.

word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU automatically performs the proper number of memory accesses, one if the word operand is on an even byte boundary and two is it is on an odd byte boundary. Except for the performance penalty, this double access is transparent to the software. The performance penalty does not occur for instruction fetches; only word operands.

Physically, the memory is organized as a high bank (D15-D8) and a low bank (D7-D0) of 512K 8-bit bytes addressed in parallel by the processor's address lines.

Byte data with even addresses is transferred on the D7-D0 bus lines while odd addressed byte data (A0 HIGH) is transferred on the D15-D8 bus lines. The processor provides two enable signals. $\overline{BHE}$ and A0 to selectively allow reading from or writing into either an odd byte location, even byte location, or both. The instruction stream is fetched from memory as words and is addressed internally by the processor at the byte level as necessary.

In referencing word data, the BIU requires one or two memory cycles depending on whether the starting byte of the word is on an even or odd address, respectively. Consequently, in referencing word operands performance can be optimized by locating data on even address boundaries. This is an especially useful technique for using the stack, since odd address references to the stack may adversely affect the context switching time for interrupt processing or task multiplexing.

Certain locations in memory are reserved for specific CPU operations (See Figure 2). Locations from address FFFF0H through FFFFFH are reserved for operations including a jump to the initial program loading routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be. Locations 00000H through 003FFH are reserved for interrupt operations. Each of the 256 possible interrupt types has its service routine pointed to be a 4-byte pointer element consisting of a 16-bit segment address and a 16-bit offset address. The pointer elements are assumed to have been stored at the respective places in reserved memory prior to occurrence of interrupts.

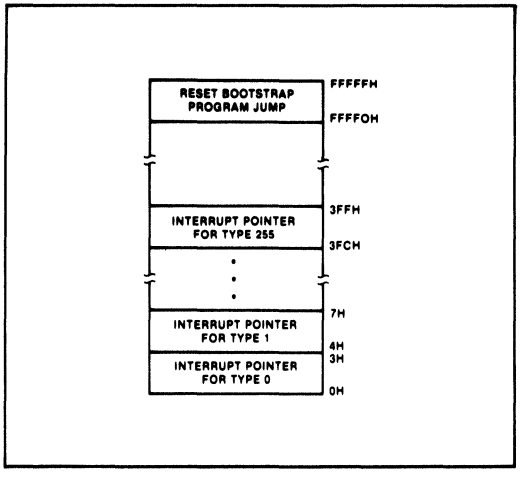


Figure 2. Reserved Memory Locations

Minimum and Maximum Operation Modes

The requirements for supporting minumum and maximum 80C86 systems are sufficiently different that they cannot be met efficiently using 40 uniquely defined pins. Consequently, the 80C86 is equipped with a strap pin (MN/$\overline{MX}$) which defines the system configuration. The definition of a certain subset of the pins changes dependent on the condition of the strap pin. When the MN/$\overline{MX}$ pin is strapped to GND, the 80C86 treats pins 24 through 31 in maximum mode. An 82C88 bus controller interprets status information coded into $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$ to generate bus timing and control signals compatible with the MULTIBUS ® architecture. When the MN/$\overline{MX}$ pin is strapped to VCC, the 80C86 generates bus control signals itself on pins 24 through 31.

Bus Operation

The 80C86 has a combined address and data bus commonly referred to as a time multiplexed bus. This technique provides the most efficient use of pins on the processor while permitting the use of a standard 40-lead package. This "local bus" can be buffered directly and used throughout the system with address latching provided on memory and I/O modules. In addition, the bus can also be demultiplexed at the processor with a single set of 82C82 address latches if a standard non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T_1, T_2, T_3 and T_4 (see Figure 3). The address is emitted from the processor during T_1 and data transfer occurs on the bus during T_3 and T_4. T_2 is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "Wait" states (TW) are inserted between T_3 and T_4. Each inserted "Wait" state is of the same duration as a CLK cycle. Periods between 80C86 bus cycles are referred to as "idle" states (T_I) or inactive CLK cycles. The processor uses these cycles for internal housekeeping and processing.

During T_1 of any bus cycle, the ALE (Address Latch Enable) signal is emitted (by either the processor or the

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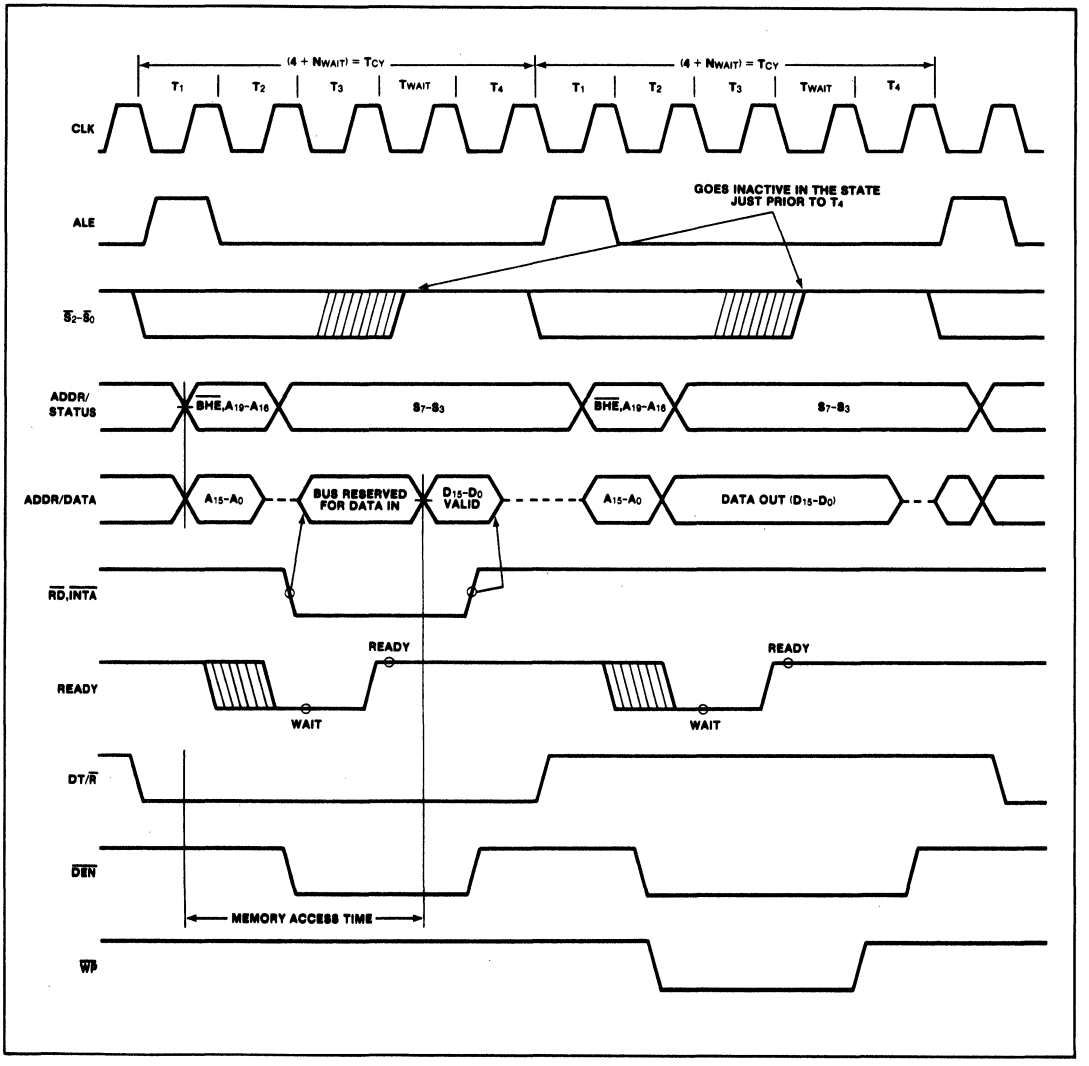


Figure 3. Basic System Timing

82C88 bus controller, depending on the MN/$\overline{MX}$ strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits $\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$ are used, in maximum mode, by the bus controller to identify the type of bus transaction according to the following table:

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	CHARACTERISTICS
0 (LOW)	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1 (HIGH)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Table 5.

Status bits S_3 through S_7 are time multiplexed with high order address bits and the $\overline{BHE}$ signal, and are therefore valid during T_2 through T_4. S_3 and S_4 indicate which segment register (see Instruction Set description) was used for this bus cycle in forming the address, according to the following table:

S_4	S_3	CHARACTERISTICS
0 (LOW)	0	Alternate Data (extra segment)
0	1	Stack
1 (HIGH)	0	Code or None
1	1	Data

Table 6.

S_5 is a reflection of the PSW interrupt enable bit. S_6 is undefined and S_7 is a spare status bit.

I/O Addressing

In the 80C86, I/O operations can address up to a maximum of 64K I/O byte registers on 32K I/O word registers. The I/O address appears in the same format as the memory address on bus lines A15-A0. The address lines A19-A16 are zero in I/O operations. The variable I/O instructions which use register DX as a pointer have full address capability while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space.

I/O ports are addressed in the same manner as memory locations. Even addressed bytes are transferred on the D7-D0 bus lines and odd addressed bytes on D15-D8. Care must be taken to ensure that each register within an 8-bit peripheral located on the lower portion of the bus be addressed as even.

External Interface

Processor Reset and Initialization

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The 80C86 RESET is required to be HIGH for greater than 4 CLK cycles. The 80C86 will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence. After this interval, the 80C86 operates normally beginning with the instruction in absolute location FFFF0H. The RESET input is internally synchronized to the processor clock. At initialization, the HIGH-to-LOW transition of RESET must occur no sooner than 50 μs (or 4 CLK cycles, whichever is greater) after power-up, to allow complete initialization of the 80C86.

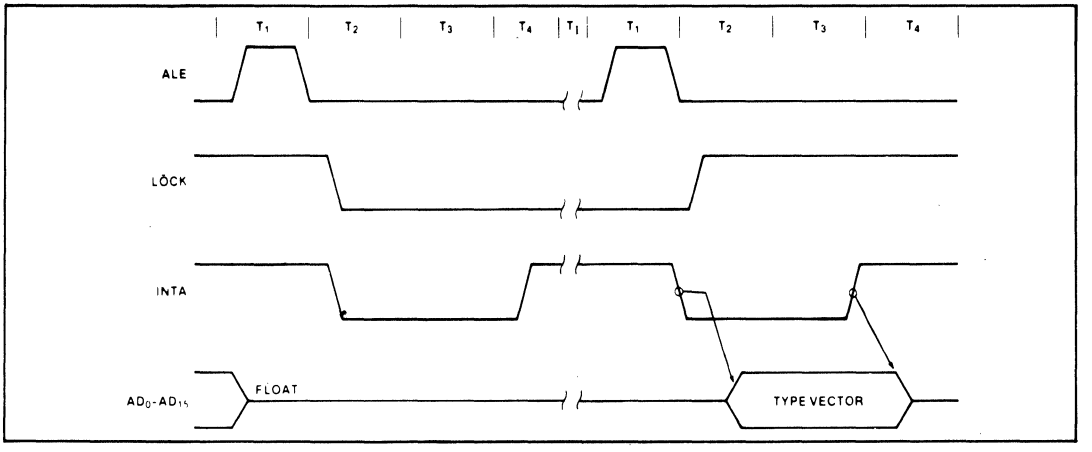


Figure 4. Interrupt Acknowledge Sequence

NMI may not be asserted prior to the second CLK cycle following the end of RESET.

Bus Hold Circuitry

To avoid high current conditions caused by floating inputs to CMOS devices, "bus-hold" circuitry has been used on the 80C86 pins 2-16, 26-32, and 34-39. These circuits will maintain the last valid logic state if no driving source is present (i.e. an unconnected pin or a driving source which goes to a high impedance state). To overdrive the "bus hold" circuits, an external driver must be capable of supplying approximately 400 μA minimum sink or source current at valid input voltage levels. Since this "bus hold" circuitry is active and not a "resistive" type element, the associated power supply current is negligible and power dissipation is significantly reduced when compared to the use of passive pull-up resistors.

Interrupt Operations

Interrupt operations fall into two classes; software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the Instruction Set description in the 80C86 data sheet. Hardware interrupts can be classified as non-maskable or maskable.

Interrupts result in a transfer of control to a new program location. A 256-element table containing address pointers to the interrupt service program locations resides in absolute locations 0 through 3FFH, which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt "type". An interrupting device supplies an 8-bit type number during the interrupt acknowledge sequence, which is used to "vector" through the appropriate element to the new interrupt service program location. All flags and both the Code Segment and Instruction Pointer registers and saved as part of the INTA sequence. These are restored upon execution of an Interrupt Return (IRET) instruction.

Non-Maskable Interrupt (NMI)

The processor provides a single non-maskable interrupt pin (NMI) which has higher priority than the maskable interrupt request pin (INTR). A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW-to-HIGH transition.

NMI is required to have a duration in the HIGH state of greater than two CLK cycles, but is not required to be synchronized to the clock. Any positive transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves of a block-type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during, or after the servicing of NMI. Another positive edge triggers another response if it occurs after the start of the NMI procedure. The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

Maskable Interrupt (INTR)

The 80C86 provides a single interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable FLAG status bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK. To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block-type instruction. During the interrupt response sequence further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt or single-step), although the FLAGS register which is automatically pushed onto the stack reflects the state of the processor prior to the interrupt. Until the old FLAGS register is restored the enable bit will be zero unless specifically set by an instruction.

During the response sequence (Figure 4) the processor executes two successive (back-to-back) interrupt acknowledge cycles. The 80C86 emits the LOCK signal from T_2 of the first bus cycle until T_2 of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle, a byte is supplied to the 80C86 by the 82C59A Interrupt Controller, which identifies the source (type) of the interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector look-up table. An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. The INTERRUPT RETURN instruction includes a FLAGS pop which returns the status of the original interrupt enable bit when it restores the FLAGS.

Halt

When a software "HALT" instruction is executed the processor indicates that it is entering the "HALT" state in one of two ways depending upon which mode is strapped. In minimum mode, the processor issues one ALE with no qualifying bus control signals. In maximum mode, the processor issues appropriate HALT status on $\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$ and the 82C88 bus controller issues one ALE. The 80C86 will not leave the "HALT" state when a local bus "hold" is entered while in "HALT". In this case, the processor reissues the HALT indicator. An NMI or interrupt request (when interrupts enabled) at the end of the bus hold period or RESET will force the 80C86 out of the "HALT" state.

Read/Modify/Write (Semaphore)

Operations Via Lock

The $\overline{\text{LOCK}}$ status information is provided by the processor when directly consecutive bus cycles are required during the execution of an instruction. This gives the processor the capability of performing read/modify/write operations on memory (via the Exchange Register With Memory instruction, for example) without the possibility of another system bus master receiving intervening memory cycles. This is useful in multiprocessor system configurations to accomplish "test and set lock" operations. The $\overline{\text{LOCK}}$ signal is activated (forced LOW) in the clock cycle following the one in which the software "LOCK" prefix instruction is decoded by the EU. It is deactivated at the end of the last bus cycle of the instruction following the "LOCK" prefix instruction. While $\overline{\text{LOCK}}$ is active a request on a $\overline{\text{RQ}}/\overline{\text{GT}}$ pin will be recorded and then honored at the end of the $\overline{\text{LOCK}}$.

External Synchronization Via TEST

As an alternative to the interrupts and general I/O capabilities, the 80C86 provides a single software testable input known as the $\overline{\text{TEST}}$ signal. At any time the program may execute a WAIT instruction. If at that time the $\overline{\text{TEST}}$ signal is inactive (HIGH), program execution becomes suspended while the processor waits for $\overline{\text{TEST}}$ to become active. It must remain active for at least five CLK cycles. The WAIT instruction is re-executed repeatedly until that time. This activity does not consume bus cycles. The processor remains in idle state while waiting. All 80C86 drivers go to 3-state OFF if bus "Hold" is entered. If interrupts are enabled, they may occur while the processor is waiting. When this occurs the processor fetches the WAIT instruction on extra time, processes the interupt, and then refetches and re-executes the WAIT instruction upon returning from the interrupt.

Basic System Timing

Typical system configurations for the processor operating in minimum mode and in maximum mode are shown in Figures 5a and 5b, respectively. In minimum mode, the MN/$\overline{\text{MX}}$ pin is strapped to VCC and the processor emits bus control signals (e.g. $\overline{\text{RD}}$, $\overline{\text{WR}}$, etc.) directly. In maximum mode, the MN/$\overline{\text{MX}}$ pin is strapped to GND and the processor emits coded status information which the 82C88 bus controller used to generate MULTIBUS® compatible bus control signals. Figure 3 shows the signal timing relationships.

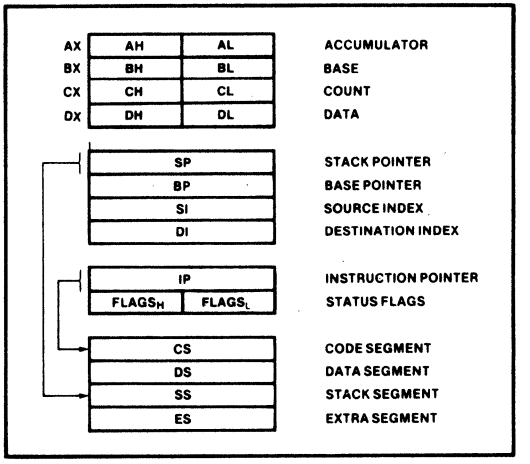


Table 7. 80C86 Register Model

System Timing – Minimum System

The read cycle begins in T_1 with the assertion of the Address Latch Enable (ALE) signal. The trailing (low-going) edge of this signal is used to latch the address information, which is valid on the local bus at this time, into the 82C82 latch. The $\overline{\text{BHE}}$ and A_0 signals address the low, high, or both bytes. From T_1 to T_4 the M/$\overline{\text{IO}}$ signal indicates a memory or I/O operation. At T_2, the address is removed from the local bus and the bus goes to a high impedance state. The read control signal is also asserted at T_2. The read ($\overline{\text{RD}}$) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later, valid data will be available on the bus and the addressed device will drive the READY line HIGH. When the processor returns the read signal to a HIGH level, the addressed device will again 3-state its bus drivers. If a transceiver is required to buffer the 80C86 local bus, signals DT/$\overline{\text{R}}$ and $\overline{\text{DEN}}$ are provided by the 80C86.

A write cycle also begins with the assertion of ALE and the emission of the address. The M/$\overline{\text{IO}}$ signal is again asserted to indicate a memory or I/O write operation. In T_2, immediately following the address emission, the processor emits the data to be written into the addressed location. This data remains valid until the middle of T_4. During T_2, T_3 and T_W, the processor asserts the write control signal. The write ($\overline{\text{WR}}$) signal becomes active a the beginning of T_2 as opposed to the read which is delayed somewhat into T_2 to provide time for the bus to float.

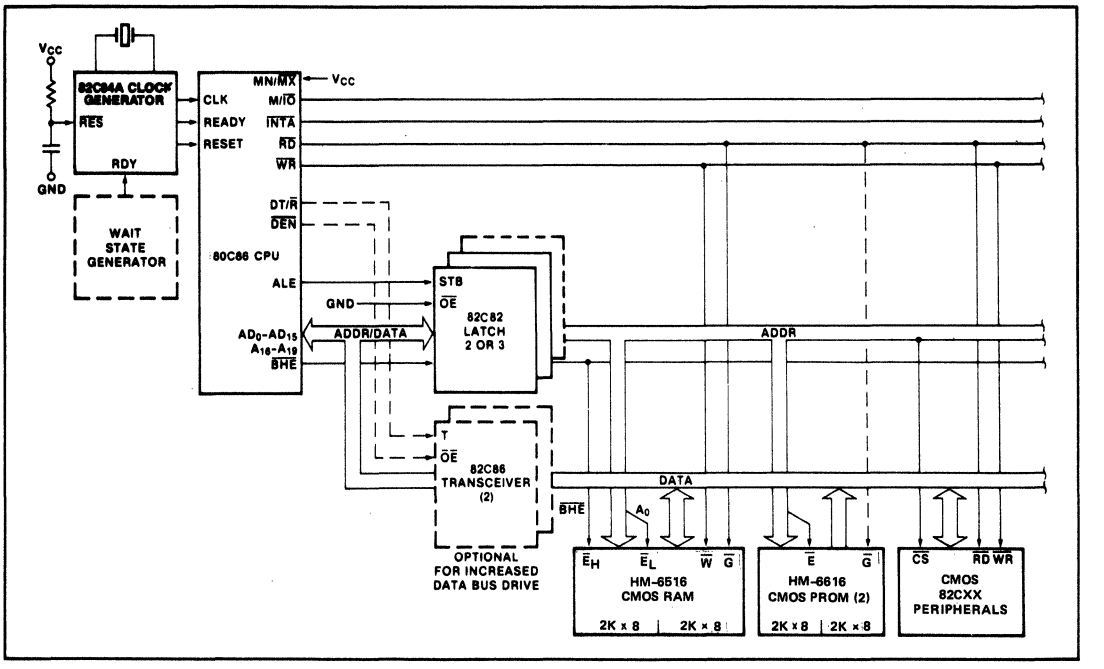


Figure 5a. Minimum Mode 80C86 Typical Configuration

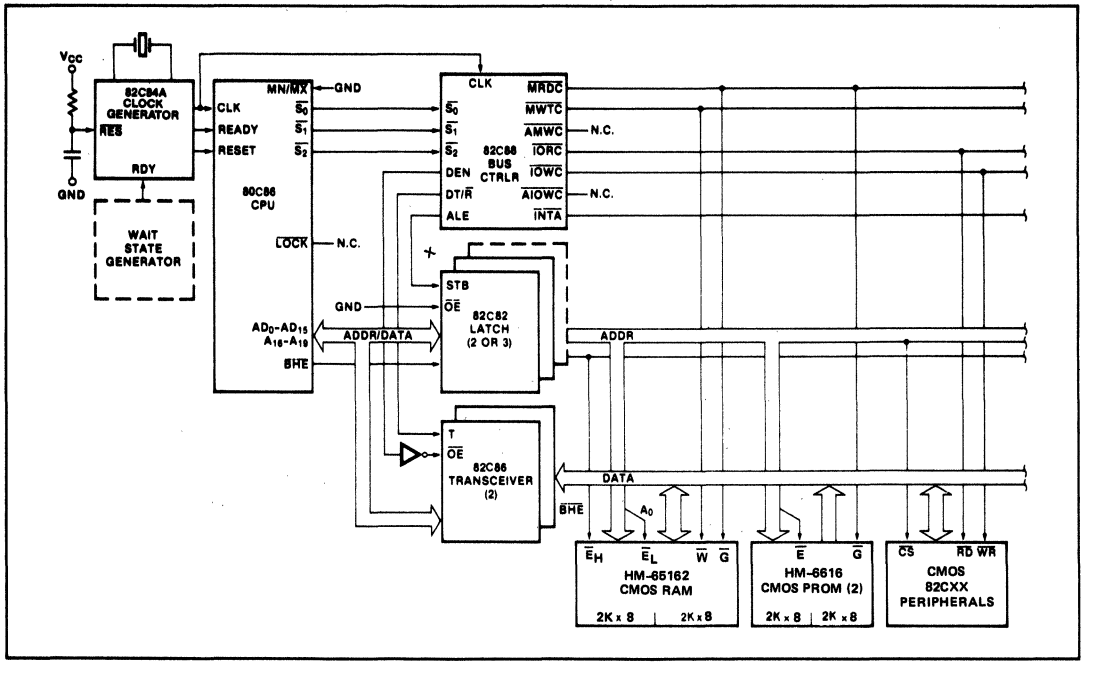


Figure 5b. Maximum Mode 80C86 Typical Configuration

The $\overline{BHE}$ and A_0 signals are used to select the proper byte(s) of the memory/IO word to be read or written according to the following table:

$\overline{BHE}$	A0	CHARACTERISTICS
0	0	Whole word
0	1	Upper byte from/ to odd address
1	0	Lower byte from/ to even address
1	1	None

Table 8.

I/O ports are addressed in the same manner as memory location. Even addressed bytes are transferred on the D7-D0 bus lines and odd addressed bytes on D15-D8.

The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge signal ($\overline{INTA}$) is asserted in place of the read ($\overline{RD}$) signal and the address bus is floated. (See Figure 4). In the second of two successive INTA cycles, a byte of information is read from bus lines D7-D0 as supplied by the interrupt system logic (i.e., 82C59A Priority Interrupt Controller). This byte identifies the source (type) of the interrupt. It is multiplied by four and used as a pointer into an interrupt vector lookup table, as described earlier.

Bus Timing – Medium Size Systems

For medium size systems the MN/$\overline{MX}$ pin is connected to GND and the 82C88 Bus Controller is added to the system as well as an 82C82 latch for latching the system address, and a transceiver to allow for bus loading greater than the 80C86 is capable of handling. ALE, $\overline{DEN}$, and DT/$\overline{R}$ are generated by the 82C88 instead of the processor in this configuration, although their timing remains relatively the same. The 80C86 status outputs ($\overline{S_2}$, $\overline{S_1}$, and $\overline{S_0}$) provide type-of-cycle information and become 82C88 inputs. This bus cycle information specifies read (code, data, or I/O), write (data or I/O), interrupt acknowledge, or software halt. The 82C88 thus issues control signals specifying memory read or write, I/O read or write, interrupt acknowledge, or halt. The 82C88 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing of write. The transceiver receives the usual T and $\overline{OE}$ inputs from the 82C88 DT/$\overline{R}$ and $\overline{DEN}$ signals.

The pointer into the interrupt vector table, which is passed during the second INTA cycle, can be derived from an 82C59A located on either the local bus or the system bus. If the master 82C59A Priority Interrupt Controller is positioned on the local bus, a TTL gate is required to disable the transceiver when reading from the master 82C59A during the interrupt acknowledge sequence and software "poll".

Specifications

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0 Volts	Operating Temperature Range	
Operating Voltage Range	+4V to +7V	Commercial	0°C to +70°C
Input Voltage Applied	GND -2.0V to 6.5V	Industrial	-40°C to +85°C
Output Voltage Applied	GND -0.5V to VCC +0.5V	Military	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C	Maximum Power Dissipation	1 Watt

CAUTION: Stresses above those listed in the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Specifications (continued)

D.C. ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V±10%; T_A = 0°C to +70°C (C80C86); T_A = -40°C to +85°C (I80C86); T_A = -55°C to +125°C (M80C86)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0 2.2		V V	C80C86, I80C86 M80C86
VIL	Logical Zero Input Voltage		0.8	V	
VIHC	CLK Logical One Input Voltage	VCC -0.8V		V	
VILC	CLK Logical Zero Input Voltage		0.8	V	
VOH	Output High Voltage	3.0 VCC -0.4		V V	IOH = -2.5mA IOH = -100μA
VOL	Output Low Voltage		0.4	V	IOL = +2.5mA
IIL	Input Leakage Current	-1.0	1.0	μA	$0V \leq VIN \leq VCC$
IBHH	Input Leakage Current-Bus Hold High	-40	-400	μA	VIN = 3.0V (see Note 1)
IBHL	Input Leakage Current-Bus Hold Low	40	400	μA	VIN = 0.8V (see Note 2)
IO	Output Leakage Current	-10.0	10.0	μA	$0V \leq VO \leq VCC$
ICCSB	Standby Power Supply Current		500	μA	VCC = 5.5V VIN = VCC or GND Outputs unloaded
ICCOP	Operating Power Supply Current		10	mA/MHz	TA = 25°C VCC = 5V, TYPICAL

CAPACITANCE

T_A = 25°C; V_{CC} = GND = OV; VIN = +5V or GND

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
CIN*	Input Capacitance		5	pf	FREQ = 1MHz Unmeasured pins returned to GND
COUT* CI/O*	Output Capacitance I/O Capacitance		15 20	pf pf	

* Guaranteed and sampled, but not 100% tested

Note 1: IBHH should be measured after raising VIN to VCC and then lowering to 3.0V on the following pins: 2-16, 26-32, 34-39.

Note 2: IBHL should be measured after lowering VIN to GND and then raising to 0.8V on the following pins: 2-16, 26-32, 34-39.

A.C. CHARACTERISTICS

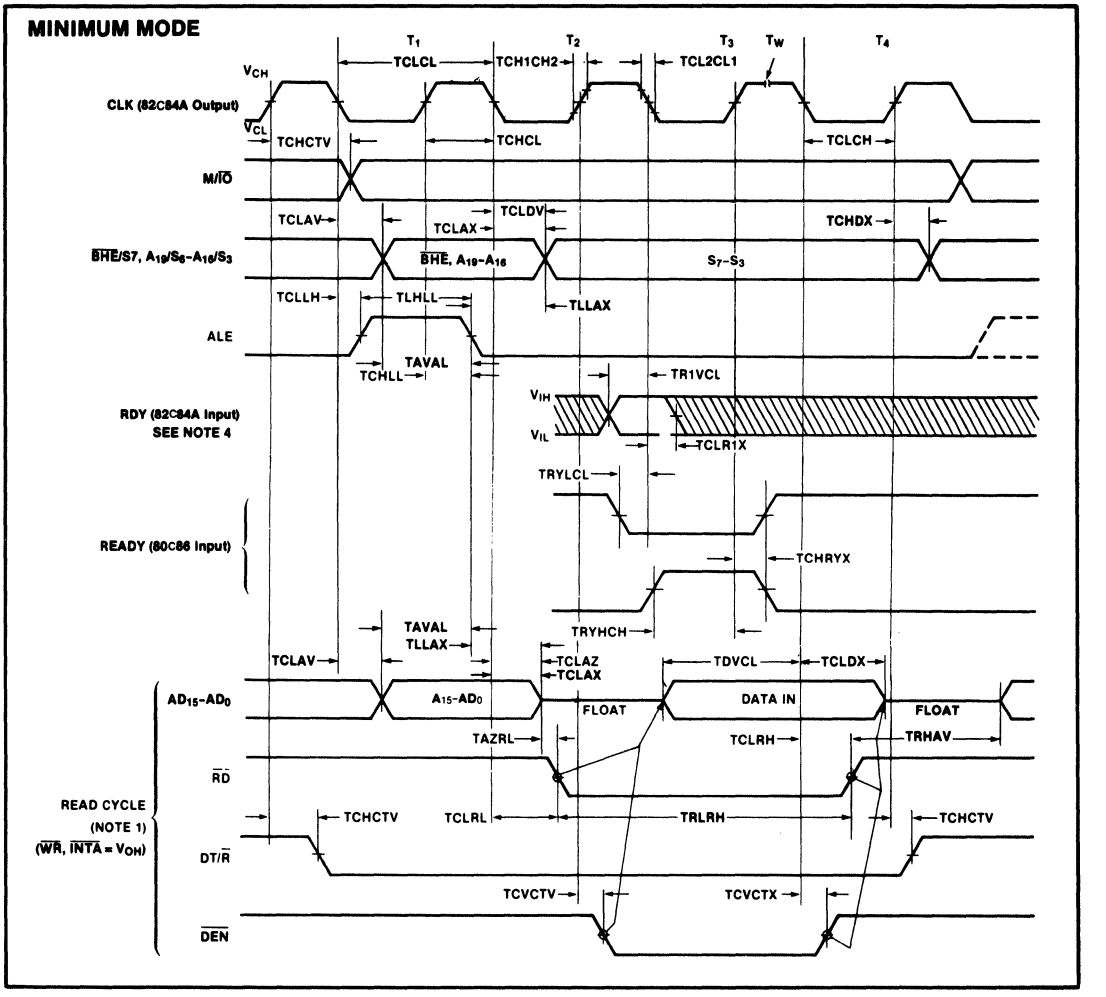
VCC = +5V±10%, GND = 0V: TA = 0°C to +70°C (C80C86)
: TA = -40°C to +85°C (I80C86)
: TA = -55°C to +125°C (M80C86)

MINIMUM COMPLEXITY SYSTEM

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TCLCL	CLK Cycle Period	200		ns	
TCLCH	CLK Low Time	118		ns	
TCHCL	CLK High Time	69		ns	
TCH1CH2	CLK Rise Time		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		ns	
TCLDX	Data in Hold Time	10		ns	
TR1VCL	RDY Setup Time into 82C84A (see Note 1,2)	35		ns	
TCLR1X	RDY Hold Time into 82C84A (see Note 1,2)	0			
TRYHCH	READY Setup Time into 80C86	118		ns	
TCHRYX	READY Hold Time into 80C86	30		ns	CL = 20 -100pF
TRYLCL	READY Inactive to CLK (see Note 3)	-8		ns	
THVCH	HOLD Setup Time	35		ns	
TINVCH	INTR, NMI, TEST Setup Time (See Note 2)	30		ns	
TILIH	Input Rise Time (Except CLK)		15	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		15	ns	From 2.0V to 0.8V
TIMING RESPONSES					
TCLAV	Address Valid Delay	10	110	ns	CL = 20 -100pF
TCLAX	Address Hold Time	10		ns	
TCLAZ	Address Float Delay	TCLAX	80	ns	
TLHLL	ALE Width	TCLCH-20		ns	
TCLLH	ALE Active Delay		80	ns	
TCHLL	ALE Inactive Delay		85	ns	
TLLAX	Address Hold Time to ALE Inactive	TCHCL-10		ns	
TCLDV	Data Valid Delay	10	110	ns	
TCHDX	Data Hold Time	10		ns	
TWHDX	Data Hold Time After WR	TCLCH-30		ns	
TCVCTV	Control Active Delay 1	10	110	ns	
TCHCTV	Control Active Delay 2	10	110	ns	
TCVCTX	Control Inactive Delay	10	110	ns	
TAZRL	Address Float to READ Active	0		ns	
TCLRL	RD Active Delay	10	165	ns	
TCLRH	RD Inactive Delay	10	150	ns	
TRHAV	RD Inactive to Next Address Active	TCLCL-45		ns	
TCLHAV	HLDA Valid Delay	10	160	ns	
TRLRH	RD Width	2TCLCL-75		ns	
TWLWH	WR Width	2TCLCL-60		ns	
TAVAL	Address Valid to ALE Low	TCLCH-60		ns	
TOLOH	Output Rise Time		15	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		15	ns	From 2.0V to 0.8V

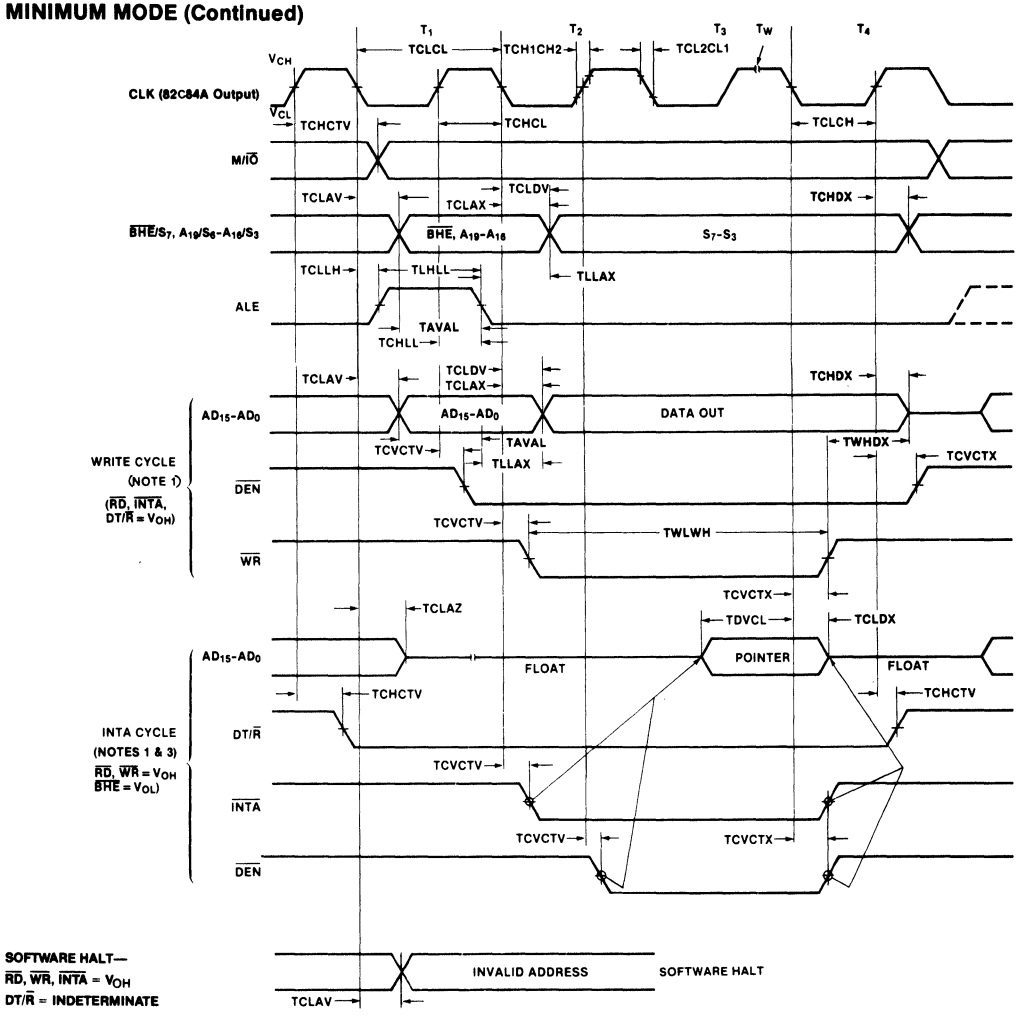
NOTES: 1. Signal at 82C84A shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T2 state (8 ns into T3).

Waveforms


MINIMUM MODE
T1
T2
T3
TW
T4
TCLCL
TCH1CH2
TCL2CL1
VCH
CLK (82C84A Output)
VCL
TCHCTV
TCHCL
TCLCH
M/IO
TCLAV
TCLAX
TCLDV
TCHDX
BHE/S7, A19/S6-A16/S3
BHE, A19-A16
S7-S3
TCLLH
TLHLL
TLLAX
ALE
TAVAL
TCHLL
TR1VCL
VIH
VIL
RDY (82C84A Input)
SEE NOTE 4
TCLR1X
TRYLCL
READY (80C86 Input)
TCHRYX
TAVAL
TLLAX
TRYHCH
TCLAV
TCLAZ
TCLAX
TDVCL
TCLDX
AD15-AD0
A15-AD0
FLOAT
DATA IN
FLOAT
TAZRL
TCLRH
TRHAV
RD
READ CYCLE
(NOTE 1)
(WR, INTA = VOH)
TCHCTV
TCLRL
TRLRH
TCHCTV
DT/R
TCVCTV
TCVCTX
DEN

Waveforms (continued)

MINIMUM MODE (Continued)



NOTES:

1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.
3. Two INTA cycles run back-to-back. The 80C86 LOCAL ADDR/DATA BUS is floating during both INTA cycles. Control signals shown for second INTA cycle.
4. Signals at 82C84A are shown for reference only.
5. All timing measurements are made at 1.5V unless otherwise noted.

A.C. CHARACTERISTICS

$V_{CC} = \pm 5V \pm 10\%$, GND = 0V : TA = 0°C to +70°C (C80C86)
: TA = -40°C to +85°C (I80C86)
: TA = -55°C to +125°C (M80C86)

MAX MODE SYSTEM (USING 82C88 BUS CONTROLLER)

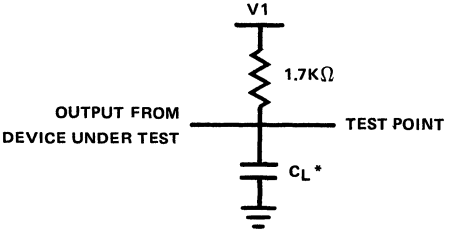
SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TIMING REQUIREMENTS					
TCLCL	CLK Cycle Period	200		ns	
TCLCH	CLK Low Time	118		ns	
TCHCL	CLK High Time	69		ns	
TCH1CH2	CLK Rise Time		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		ns	
TCLDX	Data in Hold Time	10		ns	
TR1VCL	RDY Setup Time into 82C84A (see Notes 1,2)	35		ns	
TCLR1X	RDY Hold Time into 82C84A (see Notes 1,2)	0		ns	
TRYHCH	READY Setup Time into 80C86	118		ns	
TCHRYX	READY Hold Time into 80C86	30		ns	CL = 20 - 100 pF
TRYLCL	READY inactive to CLK (see Note 4)	-8		ns	
TINVCH	Setup Time for Recognition (INTR, NMI, TEST) (see Note 2)	30		ns	
TGVCH	RQ/GT Setup Time	30		ns	
TCHGX	RQ Hold Time into 80C86	40		ns	
TILIH	Input Rise Time (Except CLK)		15	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		15	ns	From 2.0V to 0.8V
TIMING RESPONSES					
TCLML	Command Active Delay (see Note 1)	5	35	ns	
TCLMH	Command Inactive	5	35	ns	
TRYHSH	READY Active to Status Passive (see Note 3)		110	ns	
TCHSV	Status Active Delay	10	110	ns	
TCLSH	Status Inactive Delay	10	130	ns	
TCLAV	Address Valid Delay	10	110	ns	
TCLAX	Address Hold Time	10		ns	
TCLAZ	Address Float Delay	TCLAX	80	ns	
TSVLH	Status Valid to ALE High (see Note 1)		20	ns	
TSVMCH	Status Valid to MCE High (see Note 1)		30	ns	CL = 20 - 100 pf for all 80C86 Outputs (In addition to 80C86 self-load)
TCLLH	CLK Low to ALE Valid		15	ns	
TCLMCH	CLK Low to MCE High (see Note 1)		25	ns	
TCHLL	ALE Inactive Delay (see Note 1)	4	18	ns	
TCLMCL	MCE Inactive Delay (see Note 1)		15	ns	
TCLDV	Data Valid Delay	10	110	ns	
TCHDX	Data Hold Time	10		ns	
TCVNV	Control Active Delay (see Note 1)	5	45	ns	
TCVNX	Control Inactive Delay (see Note 1)	10	45	ns	
TAZRL	Address Float to Read Active	0		ns	

TIMING RESPONSES (Continued)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TCLRL	RD Active Delay	10	165	ns	CL = 20 -100pF
TCLRH	RD Inactive Delay	10	150	ns	
TRHAV	RD Inactive to Next Address Active	TCLCL-45		ns	
TCHDTL	Direction Control Active Delay (see Note 1)		50	ns	
TCHDTH	Direction Control Inactive Delay (see Note 1)		30	ns	
TCLGL	GT Active Delay	0	85	ns	
TCLGH	GT Inactive Delay	0	85	ns	
TRLRH	RD Width	2TCLCL-75		ns	
TOLOH	Output Rise Time		15	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		15	ns	From 2.0V to 0.8V

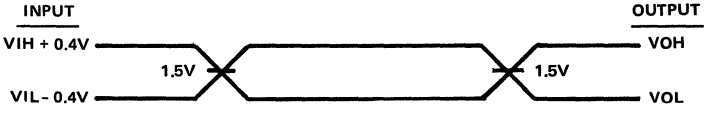
NOTES: 1. Signal at 82C84A or 82C88 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T3 and wait states.
4. Applies only to T2 state (8 ns into T3).

A.C. Test Circuits



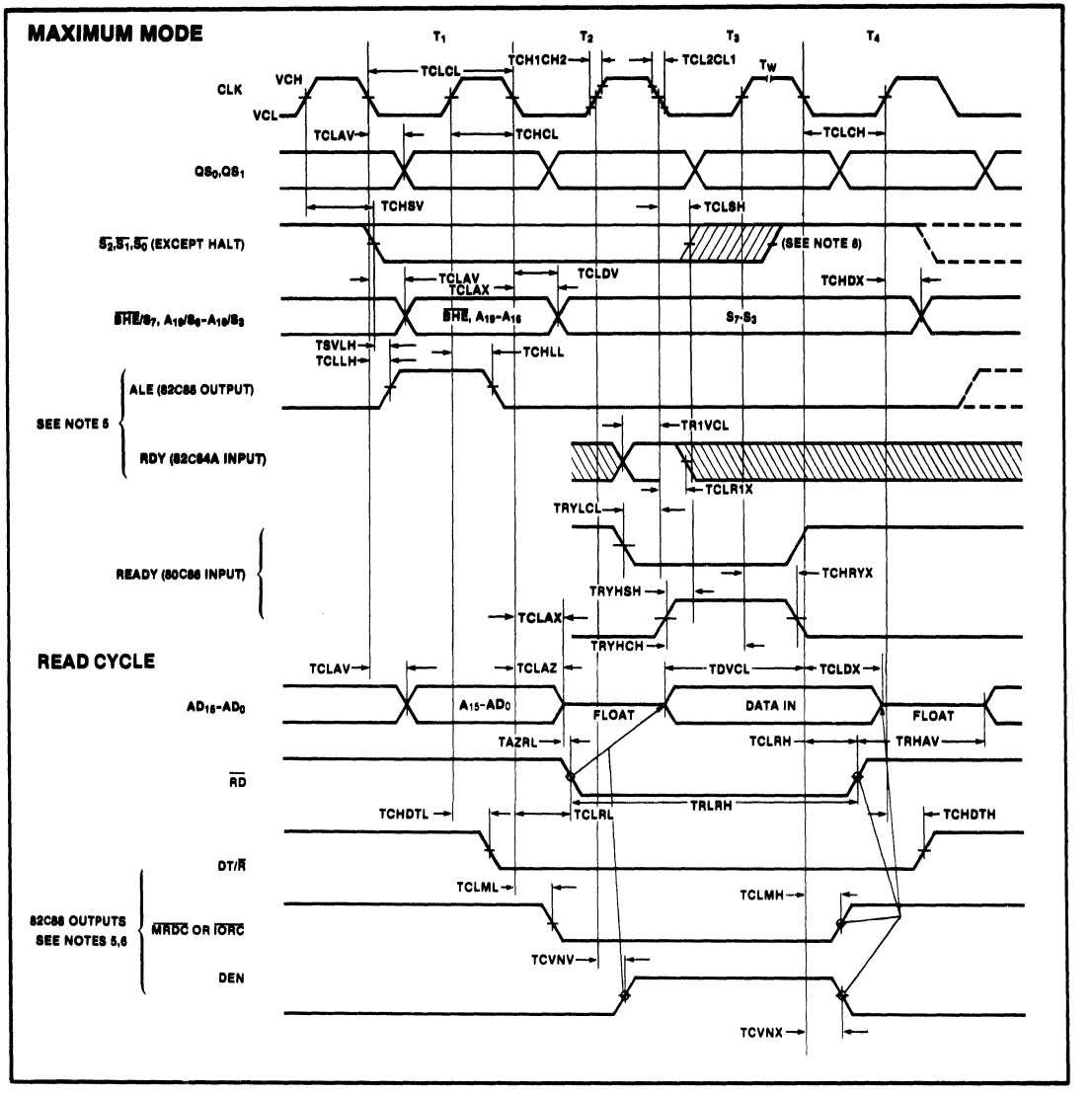
*Includes stray and jig capacitance

A.C. Testing Input, Output Waveform

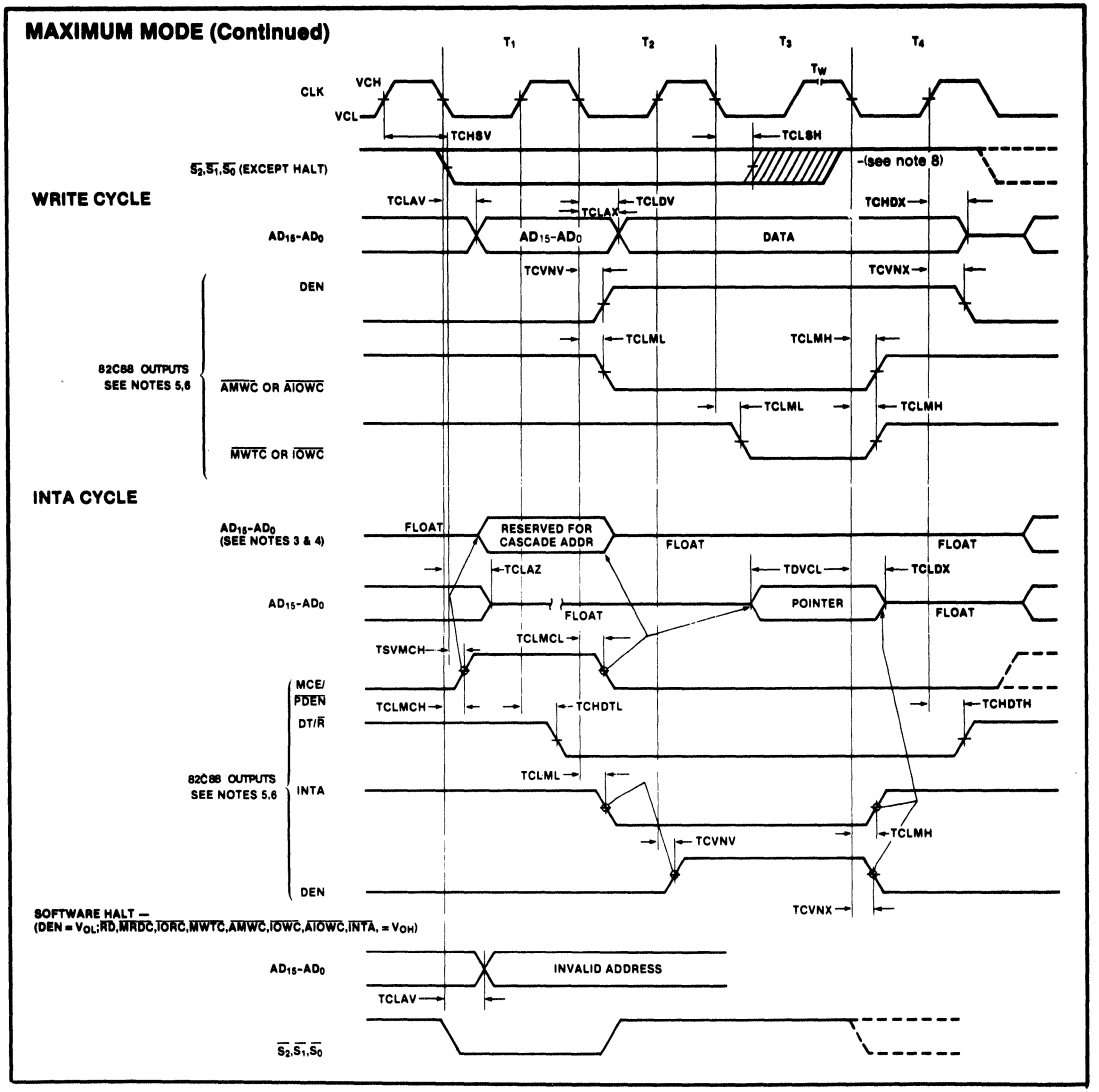


A. C. Testing: All input signals (other than CLK) must switch between VIL_{max} -0.4V and VIH_{min} +0.4V. CLK must switch between 0.4V and 3.9V. T_R and T_F must be less than or equal to 15ns. CLK T_R and T_F must be less than or equal to 10ns.

Waveforms


MAXIMUM MODE
T1
T2
T3
T4
CLK
VCH
VCL
TCLCL
TCH1CH2
TCL2CL1
TW
TCLAV
TCHCL
TCLCH
QS0,QS1
TCHSV
TCLSH
S2,S1,S0 (EXCEPT HALT)
(SEE NOTE 8)
TCLAV
TCLAX
TCLDV
TCHDX
SHE/S7, A19/S6-A16/S3
SHE, A19-A16
S7-S3
TSVLH
TCLLH
TCHLL
SEE NOTE 5
ALE (82C88 OUTPUT)
RDY (82C84A INPUT)
TR1VCL
TCLR1X
TRYLCL
READY (80C86 INPUT)
TCHRYX
TRYHSH
TCLAX
TRYHCH
READ CYCLE
TCLAV
TCLAZ
TDVCL
TCLDX
AD15-AD0
A15-AD0
FLOAT
DATA IN
FLOAT
TAZRL
TCLRH
TRHAV
RD
TCHDTL
TCLRL
TRLRH
TCHDTH
DT/R
TCLML
TCLMH
82C88 OUTPUTS SEE NOTES 5,6
MRDC OR IORC
DEN
TCVNV
TCVNX

Waveforms (continued)

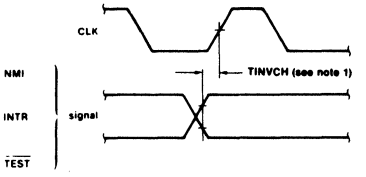


NOTES:

1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.
3. Cascade address is valid between first and second INTA cycle.
4. Two INTA cycles run back-to-back. The 80C86 LOCAL ADDR/DATA BUS is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
5. Signals at 82C84A or 82C88 are shown for reference only.
6. The issuance of the 82C88 command and control signals (MRDC, MWTC, AMWC, IORC, IOWC, AIOWC, INTA and DEN) lags the active high 82C88 CEN.
7. All timing measurements are made at 1.5V unless otherwise noted.
8. Status inactive in state just prior to T_4.

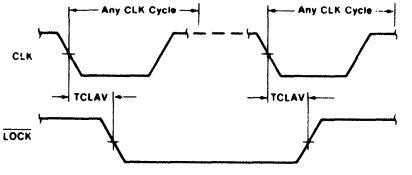
Waveforms (continued)

ASYNCHRONOUS SIGNAL RECOGNITION

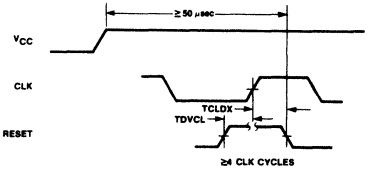


NOTE: 1. SETUP REQUIREMENTS FOR ASYNCHRONOUS SIGNALS ONLY TO GUARANTEE RECOGNITION AT NEXT CLK

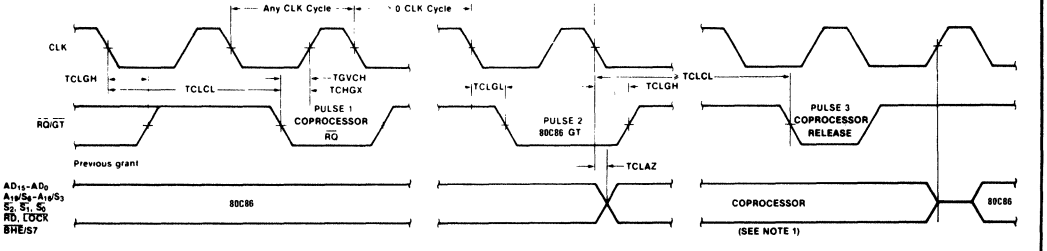
BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)



RESET TIMING

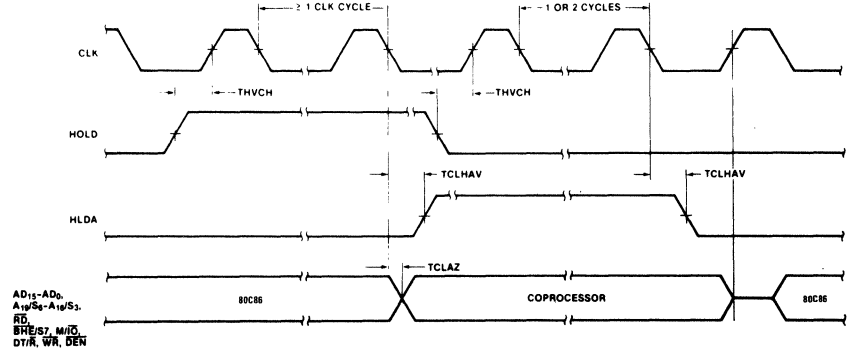


REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)

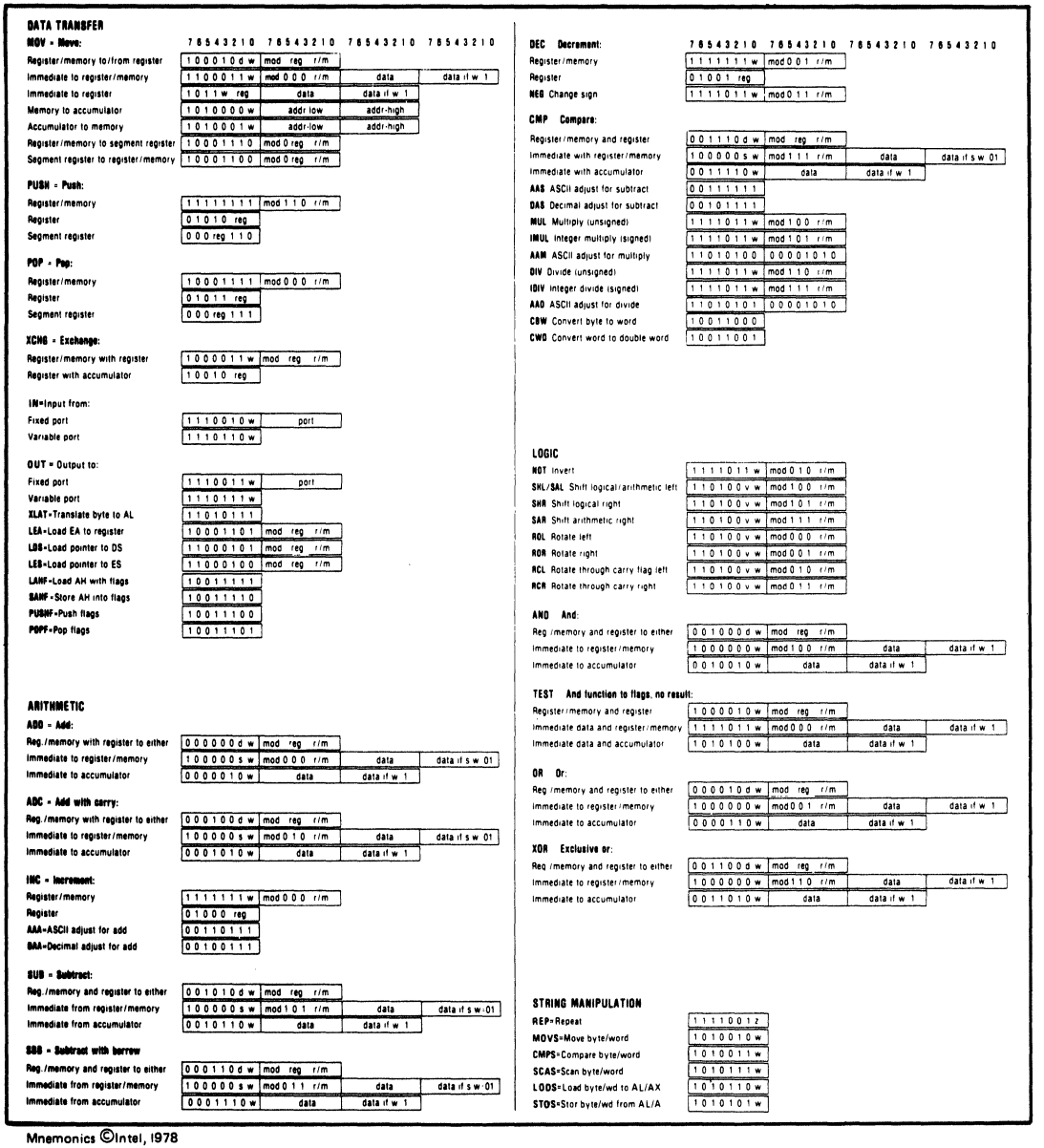


NOTES: 1 THE COPROCESSOR MAY NOT DRIVE THE BUSES OUTSIDE THE REGION SHOWN WITHOUT RISKING CONTENTION.

HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)



Instruction Set Summary



DATA TRANSFER

MOV = Move:	76543210	76543210	76543210	76543210
Register/memory to/from register	100010dw	mod reg r/m		
Immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1
Immediate to register	1011w reg	data	data if w=1	
Memory to accumulator	1010000w	addr-low	addr-high	
Accumulator to memory	1010001w	addr-low	addr-high	
Register/memory to segment register	10001110	mod0reg r/m		
Segment register to register/memory	10001100	mod0reg r/m		

PUSH = Push:	
Register/memory	11111111 mod110 r/m
Register	01010 reg
Segment register	000reg110

POP = Pop:	
Register/memory	10001111 mod000 r/m
Register	01011 reg
Segment register	000reg111

XCHG = Exchange:	
Register/memory with register	1000011w mod reg r/m
Register with accumulator	10010 reg

IN=Input from:	
Fixed port	1110010w port
Variable port	1110110w

OUT = Output to:	
Fixed port	1110011w port
Variable port	1110111w
XLAT=Translate byte to AL	11010111
LEA=Load EA to register	10001101 mod reg r/m
LDS=Load pointer to DS	11000101 mod reg r/m
LES=Load pointer to ES	11000100 mod reg r/m
LAHF=Load AH with flags	10011111
SAHF=Store AH into flags	10011110
PUSHF=Push flags	10011100
POPF=Pop flags	10011101

ARITHMETIC

ADD = Add:				
Reg./memory with register to either	000000dw	mod reg r/m		
Immediate to register/memory	100000sw	mod000 r/m	data	data if s w=01
Immediate to accumulator	0000010w	data	data if w=1	

ADC = Add with carry:				
Reg./memory with register to either	000100dw	mod reg r/m		
Immediate to register/memory	100000sw	mod010 r/m	data	data if s w=01
Immediate to accumulator	0001010w	data	data if w=1	

INC = Increment:				
Register/memory	1111111w	mod000 r/m		
Register	01000 reg			
AAA=ASCII adjust for add	00110111			
DAA=Decimal adjust for add	00100111			

SUB = Subtract:				
Reg./memory and register to either	001010dw	mod reg r/m		
Immediate from register/memory	100000sw	mod101 r/m	data	data if s w=01
Immediate from accumulator	0010110w	data	data if w=1	

SBB = Subtract with borrow				
Reg./memory and register to either	000110dw	mod reg r/m		
Immediate from register/memory	100000sw	mod011 r/m	data	data if s w=01
Immediate from accumulator	0001110w	data	data if w=1	

DEC Decrement:	76543210	76543210	76543210	76543210
Register/memory	1111111w	mod001 r/m		
Register	01001 reg			
NEG Change sign	1111011w	mod011 r/m		

CMP Compare:				
Register/memory and register	001110dw	mod reg r/m		
Immediate with register/memory	100000sw	mod111 r/m	data	data if s w=01
Immediate with accumulator	0011110w	data	data if w=1	
AAS ASCII adjust for subtract	00111111			
DAS Decimal adjust for subtract	00101111			
MUL Multiply (unsigned)	1111011w	mod100 r/m		
IMUL Integer multiply (signed)	1111011w	mod101 r/m		
AAM ASCII adjust for multiply	11010100	00001010		
DIV Divide (unsigned)	1111011w	mod110 r/m		
IDIV Integer divide (signed)	1111011w	mod111 r/m		
AAD ASCII adjust for divide	11010101	00001010		
CBW Convert byte to word	10011000			
CWD Convert word to double word	10011001			

LOGIC

NOT Invert	1111011w	mod010 r/m		
SHL/SAL Shift logical/arithmetic left	110100vw	mod100 r/m		
SHR Shift logical right	110100vw	mod101 r/m		
SAR Shift arithmetic right	110100vw	mod111 r/m		
ROL Rotate left	110100vw	mod000 r/m		
ROR Rotate right	110100vw	mod001 r/m		
RCL Rotate through carry flag left	110100vw	mod010 r/m		
RCR Rotate through carry right	110100vw	mod011 r/m		

AND And:				
Reg /memory and register to either	001000dw	mod reg r/m		
Immediate to register/memory	1000000w	mod100 r/m	data	data if w=1
Immediate to accumulator	0010010w	data	data if w=1	

TEST And function to flags, no result:				
Register/memory and register	1000010w	mod reg r/m		
Immediate data and register/memory	1111011w	mod000 r/m	data	data if w=1
Immediate data and accumulator	1010100w	data	data if w=1	

OR Or:				
Reg /memory and register to either	000010dw	mod reg r/m		
Immediate to register/memory	1000000w	mod001 r/m	data	data if w=1
Immediate to accumulator	0000110w	data	data if w=1	

XOR Exclusive or:				
Reg /memory and register to either	001100dw	mod reg r/m		
Immediate to register/memory	1000000w	mod110 r/m	data	data if w=1
Immediate to accumulator	0011010w	data	data if w=1	

STRING MANIPULATION

REP=Repeat	1111001z
MOVS=Move byte/word	1010010w
CMPS=Compare byte/word	1010011w
SCAS=Scan byte/word	1010111w
LODS=Load byte/wd to AL/AX	1010110w
STOS=Stor byte/wd from AL/A	1010101w

Mnemonics ©Intel, 1978

Instruction Set Summary (continued)

CONTROL TRANSFER

CALL = Call:	76543210	76543210	76543210
Direct within segment	11101000	disp-low	disp-high
Indirect within segment	11111111	mod 010 r/m	
Direct intersegment	10011010	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	11111111	mod 011 r/m	

JMP = Unconditional Jump:			
Direct within segment	11101001	disp-low	disp-high
Direct within segment-short	11101011	disp	
Indirect within segment	11111111	mod 100 r/m	
Direct intersegment	11101010	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	11111111	mod 101 r/m	

RET = Return from CALL:			
Within segment	11000011		
Within seg adding immed to SP	11000010	data-low	data-high
Intersegment	11001011		
Intersegment adding immediate to SP	11001010	data-low	data-high

	76543210	76543210
JE/JZ=Jump on equal/zero	01110100	disp
JL/JNGE=Jump on less/not greater or equal	01111100	disp
JLE/JNG=Jump on less or equal/not greater	01111110	disp
JB/JNAE=Jump on below/not above or equal	01110010	disp
JBE/JNA=Jump on below or equal/ not above	01110110	disp
JP/JPE=Jump on parity/parity even	01111010	disp
JO=Jump on overflow	01110000	disp
JS=Jump on sign	01111000	disp
JNE/JNZ=Jump on not equal/not zero	01110101	disp
JNL/JGE=Jump on not less/greater or equal	01111101	disp
JNLE/JG=Jump on not less or equal/ greater	01111111	disp

	76543210	76543210
JNB/JAE Jump on not below/above or equal	01110011	disp
JNBE/JA Jump on not below or equal/above	01110111	disp
JNP/JPO=Jump on not par/par odd	01111011	disp
JNO=Jump on not overflow	01110001	disp
JNS Jump on not sign	01111001	disp
LOOP Loop CX times	11100010	disp
LOOPZ/LOOPE Loop while zero/equal	11100001	disp
LOOPNZ/LOOPNE Loop while not zero/equal	11100000	disp
JCXZ Jump on CX zero	11100011	disp

INT Interrupt		
Type specified	11001101	type
Type 3	11001100	
INTO Interrupt on overflow	11001110	
IRET Interrupt return	11001111	

PROCESSOR CONTROL

CLC Clear carry	11111000	
CMC Complement carry	11110101	
STC Set carry	11111001	
CLD Clear direction	11111100	
STD Set direction	11111101	
CLI Clear interrupt	11111010	
STI Set interrupt	11111011	
HLT Halt	11110100	
WAIT Wait	10011011	
ESC Escape (to external device)	11011xxx	mod x x x r/m
LOCK Bus lock prefix	11110000	

Footnotes:

AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value.
Greater = more positive;
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg
if w = 1 then word instruction; if w = 0 then byte instruction

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

if s:w = 01 then 16 bits of immediate data form the operand.
if s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand.
if v = 0 then "count" = 1; if v = 1 then "count" in (CL)
x = don't care
z is used for string primitives for comparison with ZF FLAG.

SEGMENT OVERRIDE PREFIX

001 reg 110

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

Mnemonics©Intel, 1978

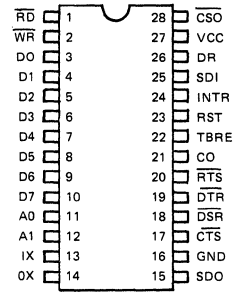
Preview

Features

- SINGLE CHIP UART/BRG
- DC TO 16MHz OPERATION
- CRYSTAL OR EXTERNAL CLOCK INPUT
- ON CHIP BAUD RATE GENERATOR
  . . . 72 SELECTABLE BAUD RATES
- INTERRUPT MODE WITH MASK CAPABILITY
- MICROPROCESSOR BUS ORIENTED INTERFACE
- 80C86 COMPATIBLE
- SCALED SAJI IV CMOS PROCESS
- SINGLE 5V POWER SUPPLY
- LOW POWER – 1mA/MHz TYPICAL
- MODEM INTERFACE
- LINE BREAK GENERATION AND DETECTION
- LOOPBACK AND ECHO MODES

Pinout

Top View



Description

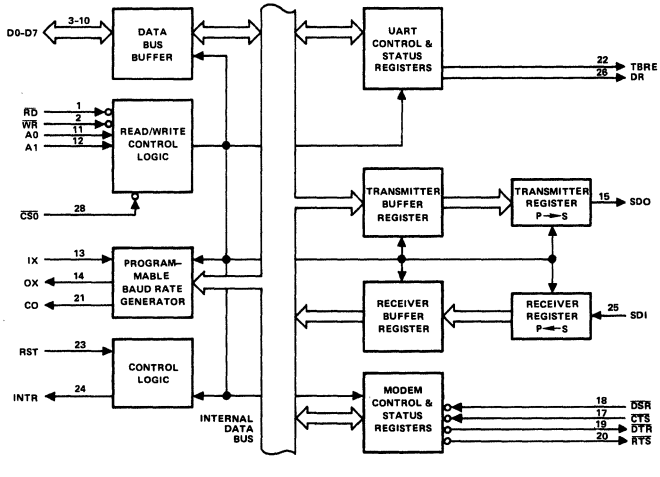
The 82C52 is a high performance programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG) on a single chip. Utilizing the Harris advanced Scaled SAJI IV CMOS process, the 82C52 will support data rates from D.C. to 1M baud asynchronously with a 16X clock (0-16 MHz clock frequency).

The on-chip Baud Rate Generator can be programmed for any one of 72 different baud rates using a single industry standard crystal or external frequency source. A unique pre-scale divide circuit has been designed to provide standard RS-232-C baud rates when using any one of three industry standard baud rate crystals (1.8432 MHz, 2.4576 MHz, or 3.072MHz).

A programmable buffered clock output (CO) is available and can be programmed to provide either a buffered oscillator or 16X baud rate clock for general purpose system usage.

Inputs and outputs have been designed with full TTL/CMOS compatibility in order to facilitate mixed TTL/NMOS/CMOS system design.

Block Diagram



√CC - PIN 27
GND - PIN 16

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow standard IC Handling Procedures.

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HARRIS

82C54

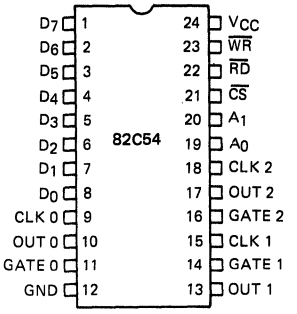
CMOS PROGRAMMABLE INTERVAL TIMER

Advance Information

Features

- COMPATIBLE WITH NMOS 8254
  - —ENHANCED VERSION OF NMOS 8253
- THREE INDEPENDENT 16 BIT COUNTERS
- SIX PROGRAMMABLE COUNTER MODES
- STATUS READ-BACK COMMAND
- BINARY OR 8CD COUNTING
- FULLY TTL COMPATIBLE
- SCALED SAJI IV CMOS PROCESS
- LOW POWER
  - —ICCSB = 10μA
  - —ICCOP = 10mA@ 8MHz COUNT FREQUENCY
- SINGLE 5V POWER SUPPLY
- COMMERCIAL, INDUSTRIAL AND MILITARY TEMPERATURE RANGES

Pinout



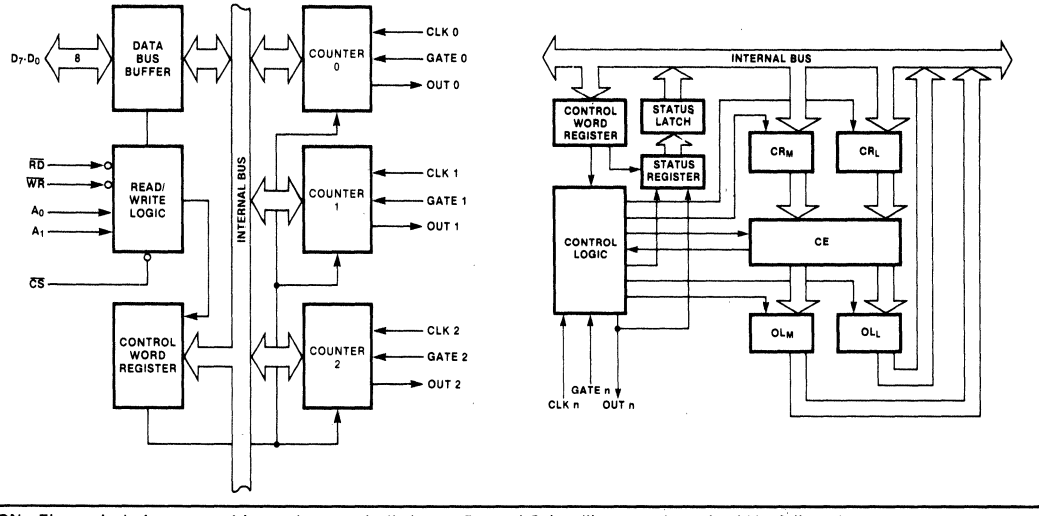
Description

The Harris 82C54 is a high performance CMOS Programmable Interval Timer manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C54 has three independently programmable and functional 16 bit counters, each capable of handling clock input frequencies of up to 8MHz. The high speed and industry standard configuration of the 82C54 make it compatible with many industry standard microprocessors.

Six programmable timer modes allow the 82C54 to be used as an event counter, elapsed time indicator, programmable one-shot along with many other applications.

Static CMOS circuit design insures low operation power Harris advanced SAJI process results in a significant reduction in power with performance equal to or greater than existing equivalent products.

Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Pin Description

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
D_7-D_0	1-8	I/O	Data: Bi-directional three state data bus lines, connected to system data bus.
CLK0	9	I	Clock 0: Clock input of Counter 0.
OUT 0	10	O	Output 0: Output of Counter 0.
GATE 0	11	I	Gate 0: Gate input of Counter 0.
GND	12		Ground: Power supply connection.
OUT 1	13	O	Out 1: Output of Counter 1.
GATE 1	14	I	Gate 1: Gate input of Counter 1.
CLK 1	15	I	Clock 1: Clock input of Counter 1.
GATE 2	16	I	Gate 2: Gate input of Counter 2.
OUT 2	17	O	Out 2: Output of Counter 2.
CLK 2	18	I	Clock 2: Clock input of Counter 2.
A0, A1	19-20	I	Address: Select inputs for one of the three counters or Control Word Register for read/write operations. Normally connected to the system address bus. A1 A0 Selects 0 0 Counter 0 0 1 Counter 1 1 0 Counter 2 1 1 Control Word Register
$\overline{CS}$	21	I	Chip Select: A low on this input enables the 82C54 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
$\overline{RD}$	22	I	Read: This input is low during CPU read operations.
$\overline{WR}$	23	I	Write: This input is low during CPU write operations.
VCC	24		Power: +5V power supply connection.

Functional Description

General

The 82C54 is a programmable interval timer/counter designed for use with microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 82C54 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the 82C54 to match his requirements and programs one of the counters for the desired delay. After the desired delay, the 82C54 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other computer/timer functions common to microcomputers which can be implemented with the 82C54 are:

- Real time clock
- Event counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the 82C54 to the system bus (see Figure 1).

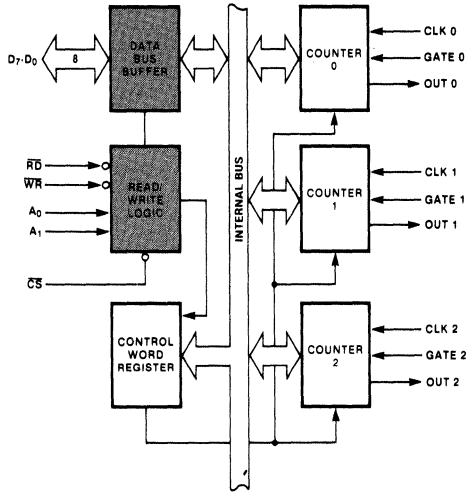


Figure 1. Data Bus Buffer and Read/Write Logic Function

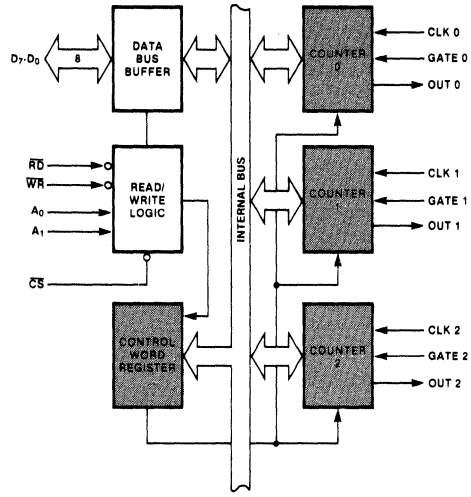


Figure 2. Control Word Register and Counter Functions

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the 82C54. A1 and A0 select one of the three counters or the Control Word Register to be read from/written into. A "low" on the $\overline{RD}$ input tells the 82C54 that the CPU is reading one of the counters. A "low" on the $\overline{WR}$ input tells the 82C54 that the CPU is writing either a Control Word or an initial count. Both $\overline{RD}$ and $\overline{WR}$ are qualified by $\overline{CS}$; $\overline{RD}$ and $\overline{WR}$ are ignored unless the 82C54 has been selected by holding $\overline{CS}$ low.

Control Word Register

The Control Word Register (Figure 2) is selected by the Read/Write Logic when A1, A0 = 11. If the CPU then does a write operation to the 82C54, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the Counter operation.

The Control Word Register can only be written to; status information is available with the Read-Back Command.

Counter 0, Counter 1, Counter 2

These three functional blocks are identical in operation, so only a single Counter will be described. The internal block diagram of a single counter is shown in Figure 3.

The Counters are fully independent. Each Counter may operate in a different Mode.

The Control Word Register is shown in the figure; it is not part of the Counter itself, but its contents determine how the Counter operates.

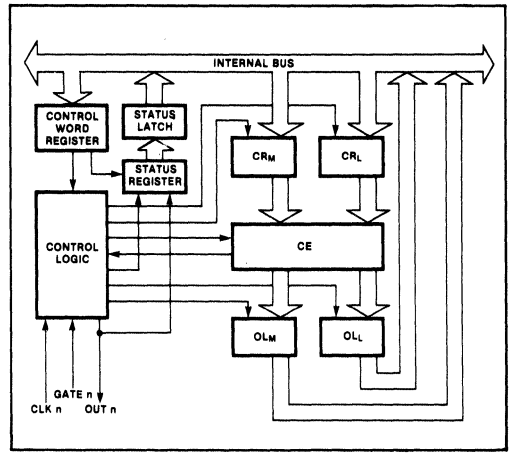


Figure 3. Counter Internal Block Diagram

The status register, shown in the Figure, when latched, contains the current contents of the Control Word Register and status of the output and null count flag. (See detailed explanation of the Read-Back command.)

The actual counter is labeled CE (for "Counting Element). It is a 16-bit presettable synchronous down counter.

OL_M and OL_L are two 8-bit latches. OL stands for "Output Latch"; the subscripts M and L for "Most significant byte" and "Least significant byte" respectively. Both are normally referred to as one unit and called just OL. These latches normally "follow" the CE, but if a suitable Counter Latch Command is sent to the 82C54, the latches "latch" the present count until read by the CPU and then return to "following" the CE. One latch at a time is enabled by the counter's Control Logic to drive the internal bus. This is how the 16-bit Counter communicated over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Similarly, there are two 8-bit registers called CR_M and CR_L (for "Count Register"). Both are normally referred to as one unit and called just CR. When a new count is written to the Counter, the count is stored in the CR and later transferred to the CE. The Control Logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously. CR_M and CR_L and cleared when the Counter is programmed for one byte counts (either most significant byte only or least significant byte only) the other byte will be zero. Note that the CE cannot be written into; whenever a count is written, it is written into the CR.

The Control Logic is also shown in the diagram. CLK n, GATE n, and OUT n are all connected to the outside world through the Control Logic.

82C54 System Interface

The 82C54 is treated by the system software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The CS can be derived directly from the address bus using a linear select method or it can be connected to the output of a decoder, such as a Harris HD-6440 for larger systems.

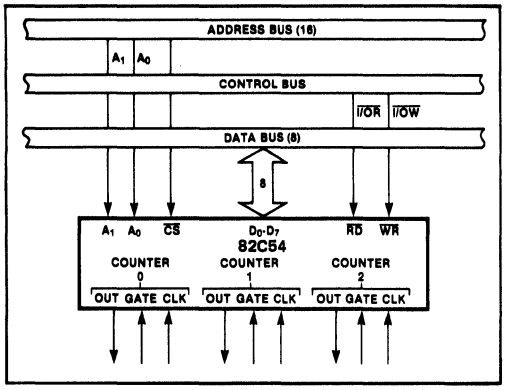


Figure 4. 82C54 System Interface

Operational Description

General

After power-up, the state of the 82C54 is undefined. The Mode, count value, and output of all Counters are undefined.

How each Counter operates is determined when it is programmed. Each Counter must be programmed before it can be used. Unused counters need not be programmed.

Programming The 82C54

Counters are programmed by writing a Control Word and then an initial count.

All Control Words are written into the Control Word Register, which is selected when A1, A0 = 11. The Control Word specifies which Counter is being programmed.

By contrast, initial counts are written into the Counters, not the Control Word Register. The A1, A0 inputs are used to select the Counter to be written. The format of the initial count is determined by the Control Word used.

Control Word Format

A1, A0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC — Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See Read Operations)

RW — Read/Write:

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only.
1	0	Read/Write most significant byte only.
1	1	Read/Write least significant byte first, then most significant byte.

M — MODE:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE: DON'T CARE BITS (X) SHOULD BE 0 TO INSURE COMPATIBILITY WITH FUTURE PRODUCTS.

Figure 5. Control Word Format

Write Operations

The programming procedure for the 82C54 is very flexible. Only two conventions need to be remembered:

1. For each Counter, the Control Word must be written before the initial count is written.

2. The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the Control Word Register and the three Counters have separate addresses (selected by the A1, A0 inputs), and each Control Word specifies the Counter it applies to (SC0, SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions above is acceptable.

A new initial count may be written to a Counter at any time without affecting the Counter's programmed Mode in any way. Counting will be affected as described in the Mode definitions. The new count must follow the programmed count format.

If a Counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same Counter. Otherwise, the Counter will be loaded with an incorrect count.

Read Operations

It is often desirable to read the value of a Counter without disturbing the count in progress. This is easily done in the 82C54.

There are three possible methods for reading the Counters. The first is through the Read-Back command, which is explained later. The second is a simple read operation of the Counter, which is selected with the A1, A0 inputs. The only requirement is that the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in process of changing when it is read, giving an undefined result.

	A_1	A_0
Control Word — Counter 0	1	1
LSB of count — Counter 0	0	0
MSB of count — Counter 0	0	0
Control Word — Counter 1	1	1
LSB of count — Counter 1	0	1
MSB of count — Counter 1	0	1
Control Word — Counter 2	1	1
LSB of count — Counter 2	1	0
MSB of count — Counter 2	1	0

	A_1	A_0
Control Word — Counter 2	1	1
Control Word — Counter 1	1	1
Control Word — Counter 0	1	1
LSB of count — Counter 2	1	0
MSB of count — Counter 2	1	0
LSB of count — Counter 1	0	1
MSB of count — Counter 1	0	1
LSB of count — Counter 0	0	0
MSB of count — Counter 0	0	0

	A_1	A_0
Control Word — Counter 0	1	1
Control Word — Counter 1	1	1
Control Word — Counter 2	1	1
LSB of count — Counter 2	1	0
LSB of count — Counter 1	0	1
LSB of count — Counter 0	0	0
MSB of count — Counter 0	0	0
MSB of count — Counter 1	0	1
MSB of count — Counter 2	1	0

	A_1	A_0
Control Word — Counter 1	1	1
Control Word — Counter 0	1	1
LSB of count — Counter 1	0	1
Control Word — Counter 2	1	1
LSB of count — Counter 0	0	0
MSB of count — Counter 1	0	1
LSB of count — Counter 2	1	0
MSB of count — Counter 0	0	0
MSB of count — Counter 2	1	0

NOTE: IN ALL FOUR EXAMPLES, ALL COUNTERS ARE PROGRAMMED TO READ/WRITE TWO-BYTE COUNTS.
THESE ARE ONLY FOUR OF MANY POSSIBLE PROGRAMMING SEQUENCES.

Figure 6. A Few Possible Programming Sequences

Counter Latch Command

The other method involves a special software command called the "Counter Latch Command". Like a Control Word, this command is written to the Control Word Register, which is selected when A1, A0 = 11. Also, like a Control Word, the SC0, SC1 bits select one of the three Counters, but two other bits, D5 and D4, distinguish this command from a Control Word.

A_1,A_0=11; CS=0; RD=1; WR=0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	0	0	X	X	X	X

SC1,SC0 — specify counter to be latched

SC1	SC0	Counter
0	0	0
0	1	1
1	0	2
1	1	Read-Back Command

D5,D4 — 00 designates Counter Latch Command

X — don't care

NOTE: DON'T CARE BITS (X) SHOULD BE 0 TO INSURE COMPATIBILITY WITH FUTURE PRODUCTS.

Figure 7. Counter Latch Command Format

The selected Counter's output latch (OL) latches the count when the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed). The count is then unlatched automatically and the OL returns to "following" reading the contents of the Counters "on the fly" without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one Counter. Each latched Counter's OL holds its count until read. Counter Latch Commands do not affect the programmed Mode of the Counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.

With either method, the count must be read according to the programmed format; specifically, if the Counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or programming operations of other Counters may be inserted between them.

Another feature of the 82C54 is that reads and writes of the same Counter may be interleaved; for example, if the Counter is programmed for two byte counts, the following sequence is valid.

1. Read least significant byte.
2. Write new least significant byte.
3. Read most significant byte.
4. Write new most significant byte.

If a Counter is programmed to read or write two-byte counts, the following precaution applies: A program MUST NOT transfer control between reading the first and second byte to another routine which also reads from that same Counter. Otherwise, an incorrect count will be read.

Read-Back Command

The read-back command allows the user to check the count value, programmed Mode, and current state of the OUT pin and Null Count flag of the selected counter(s).

The command is written into the Control Word Register and has the format shown in Figure 8. The command applies to the counters selected by setting their corresponding bits D3, D2, D1 = 1.

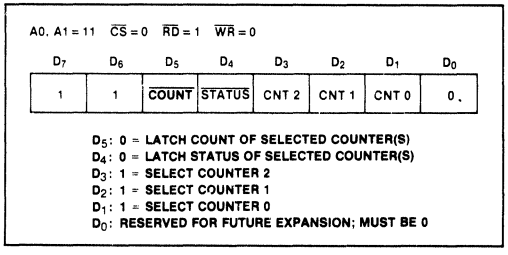


Figure 8. Read-Back Command Format

The read-back command may be used to latch multiple counter output latches (OL) by setting the COUNT bit D5 = 0 and selecting the desired counter(s). This single command is functionally equivalent to several counter latch commands, one for each counter latches. Each counter's latched count is held until it is read (or the counter is reprogrammed). That counter is automatically unlatched when read, but other counters remain latched until they are read. If multiple count read-back commands are issued to the same counter without reading the count, all but the first are ignored; i.e., the count which will be read is the count at the time the first read-back command was issued.

The read-back command may also be used to latch status information of selected counter(s) by setting STATUS bit D4 = 0. Status must be latched to be read; status of a counter is accessed by a read from that counter.

The counter status format is shown in Figure 9. Bits D5 through D0 contain the counter's programmed Mode exactly as written in the last Mode Control Word. OUTPUT bit D7 contains the current state of the OUT pin. This allows the user to monitor the counter's output via software, possibly eliminating some hardware from a system.

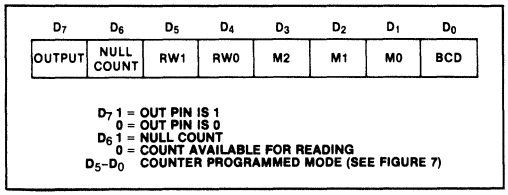


Figure 9. Status Byte

NULL COUNT bit D6 indicates when the last count written to the counter register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the Mode of the counter and is described in the Mode Definitions, but until the count is loaded into the counting element (CE), it can't be read from the counter. If the count is latched or read before this time, the count value will not reflect the new count just written. The operation of Null Count is shown in Figure 10.

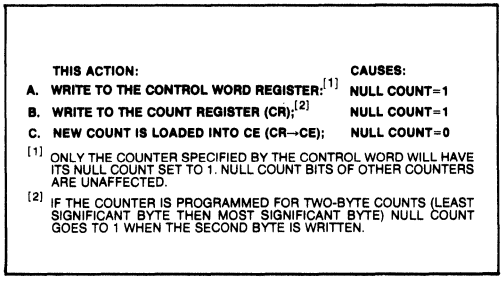


Figure 10. Null Count Operation

If multiple status latch operations of the counter(s) are performed without reading the status, all but the first are ignored; i.e., the status that will be read is the status of the counter at the time the first status read-back command was issued.

Both count and status of the selected counter(s) may be latched simultaneously by setting both COUNT and status bits D5, D4 = 0. This is functionally the same as issuing two separate read-back commands at once, and the above discussions apply here also. Specifically, if multiple count and/or status read-back commands are issued to the same counter(s) without any intervening reads, all but the first are ignored. This is illustrated in Figure 11.

If both count and status of a counter are latched, the first read operation of that counter will return latched status, regardless of which was latched first. The next one or two reads (depending on whether the counter is programmed for one or two type counts) return latched count. Subsequent reads return unlatched count.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (3-State)
1	X	X	X	X	No-Operation (3-State)
0	1	1	X	X	No-Operation (3-State)

Figure 12. Read/Write Operations Summary

Mode Definitions

The following are defined for use in describing the operation of the 82C54.

CLK PULSE: a rising edge, then a falling edge, in that order, of a Counter's CLK input.

TRIGGER: a rising edge of a Counter's Gate input.

COUNTER LOADING: the transfer of a count from the CR to the CE (See "Functional Description")

Mode 0: Interrupt on Terminal Count

Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written to the Counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an intial count of N, OUT does not go high until N + 1 CLK pulses after the initial count is written.

If a new count is written to the Counter it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1 - Writing the first byte disables counting. Out is set low immediately (no clock pulse required).

2 - Writing the second byte allows the new count to be loaded on next CLK pulse.

This allows the counting sequence to be synchronized by software. Again OUT does not go high until N + 1 CLK pulses after the new count of N is written.

If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the Counter as this has already been done.

Command								Description	Result
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	1	0	0	0	0	1	0	Read back count and status of Counter 0	Count and status latched for Counter 0
1	1	1	0	0	1	0	0	Read back status of Counter 1	Status latched for Counter 1
1	1	1	0	1	1	0	0	Read back status of Counters 2, 1	Status latched for Counter 2, but not Counter 1
1	1	0	1	1	0	0	0	Read back count of Counter 2	Count latched for Counter 2
1	1	0	0	0	1	0	0	Read back count and status of Counter 1	Count latched for Counter 1, but not status
1	1	1	0	0	0	1	0	Read back status of Counter 1	Command ignored, status already latched for Counter 1

Figure 11. Read-Back Command Example

Mode 1: Hardware Retriggerable One-Shot

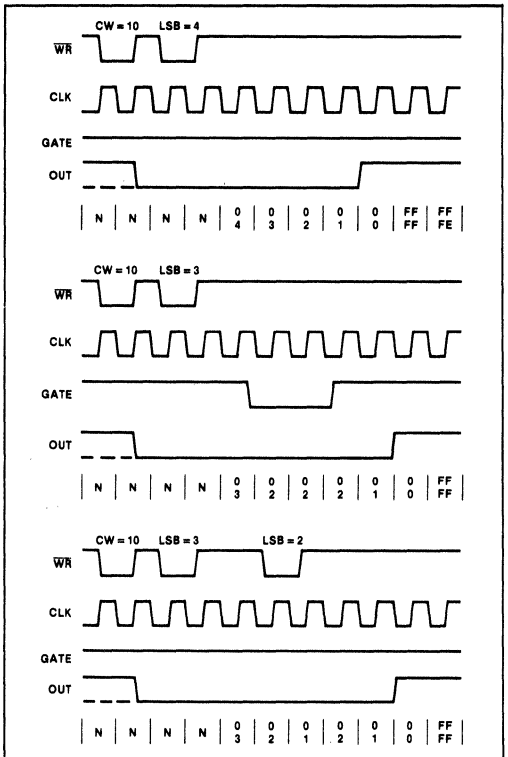
OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse N CLK cycles in duration. The one-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the Counter is retriggered. In that case, the Counter is loaded with the new count and the one-shot pulse continues until the new count expires.

Mode 2: Rate Generator

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.



NOTE: THE FOLLOWING CONVENTIONS APPLY TO ALL MODE TIMING DIAGRAMS:

1. COUNTERS ARE PROGRAMMED FOR BINARY (NOT BCD) COUNTING AND FOR READING/WRITING LEAST SIGNIFICANT BYTE (LSB) ONLY.
2. THE COUNTER IS ALWAYS SELECTED ($\overline{CS}$ ALWAYS LOW).
3. CW STANDS FOR "CONTROL WORD"; CW = 10 MEANS A CONTROL WORD OF 10, HEX IS WRITTEN TO THE COUNTER.
4. LSB STANDS FOR "LEAST SIGNIFICANT BYTE" OF COUNT.
5. NUMBERS BELOW DIAGRAMS ARE COUNT VALUES.
   THE LOWER NUMBER IS THE LEAST SIGNIFICANT BYTE.
   THE UPPER NUMBER IS THE MOST SIGNIFICANT BYTE. SINCE THE COUNTER IS PROGRAMMED TO READ/WRITE LSB ONLY, THE MOST SIGNIFICANT BYTE CANNOT BE READ.
   N STANDS FOR AN UNDEFINED COUNT.
   VERTICAL LINES SHOW TRANSITIONS BETWEEN COUNT VALUES.

Figure 13. Mode 0

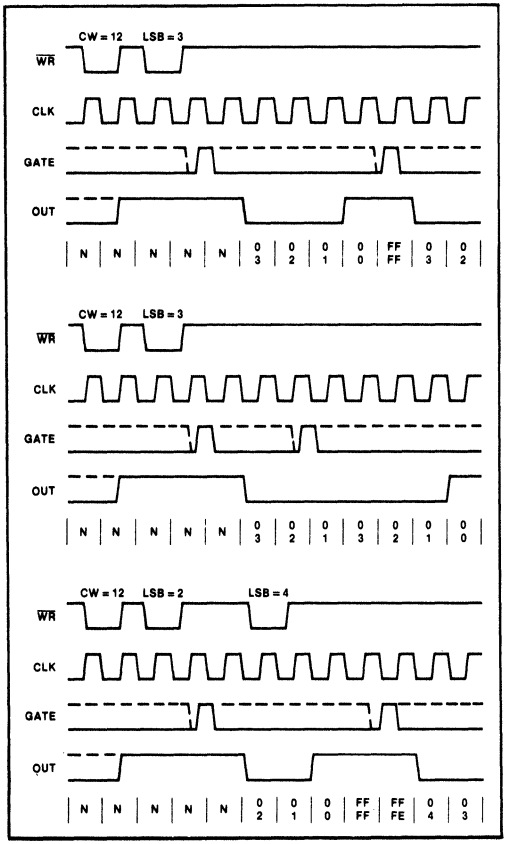


Figure 14. Mode 1

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK pulses after the initial count is written. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue form the new count. Otherwise, the new count will be loaded at the end of the current counting cycle.

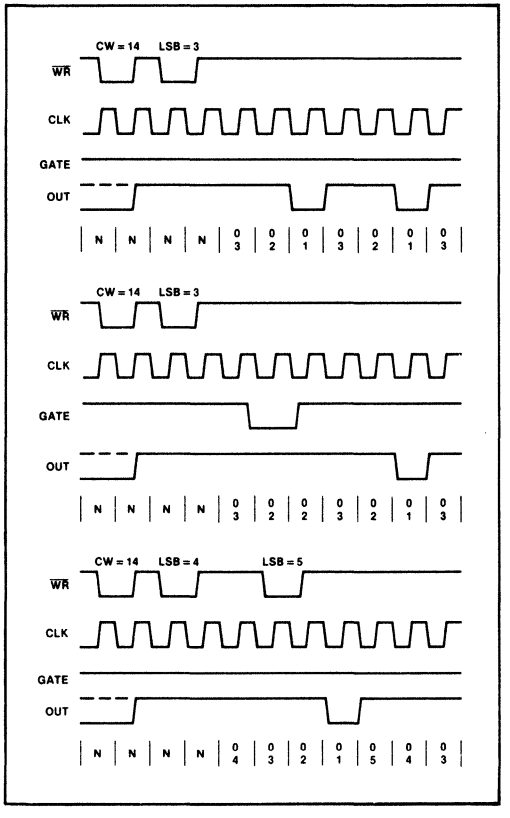


Figure 15. Mode 2

Mode 3: Square Wave Mode

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for the remainder fo the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK pulses after the initial count is written. This allows the Counter to be synchronized by software.

Writing a new count while counting does not affect the

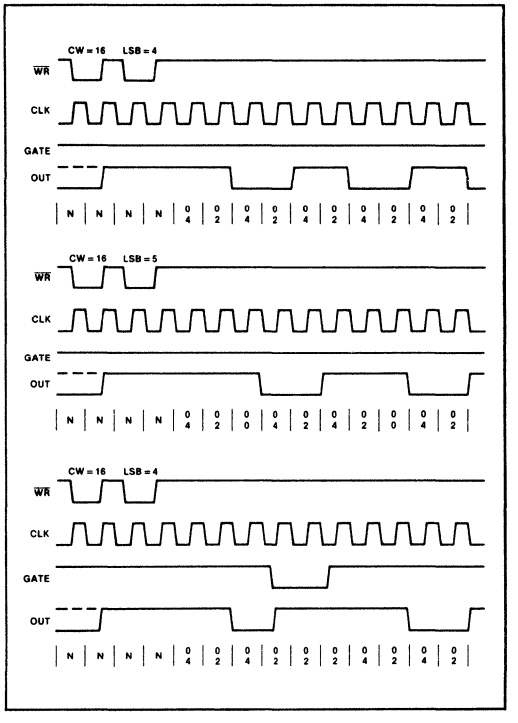


Figure 16. Mode 3

current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

EVEN COUNTS: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

ODD COUNTS: OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. One CLK pulse after the count expires, OUT goes low and the Counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the Counter is reloaded with the initial count minus one. The above process is repeated indefinitely. So for odd counts, OUT will be high for (N + 1)/2 counts and low for (N-1)/2 counts.

Mode 4: Software Triggered Mode

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse and then go high again. The counting sequence is "Triggered" by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE going low freezes OUT in current logic state.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1. Writing the first byte has no effect on counting.
2. Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be "retriggered" by software. OUT strobes low N + 1 CLK pulses after the new count of N is written.

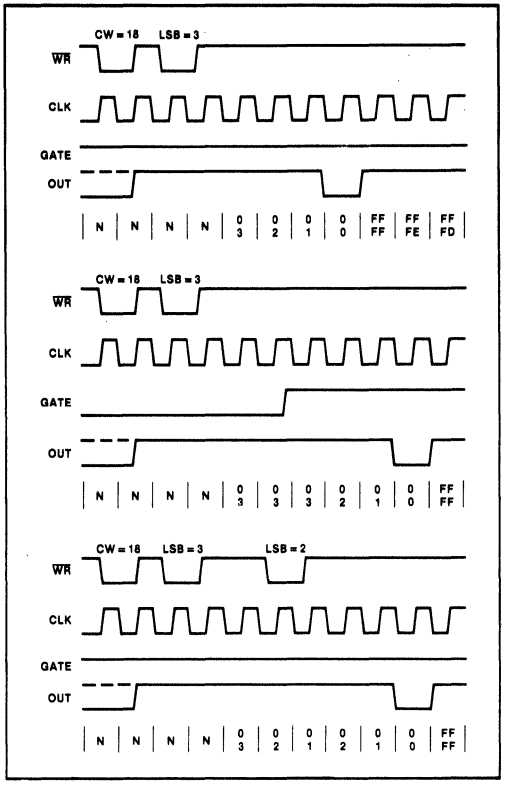


Figure 17. Mode 4

Mode 5: Hardware Triggered Strobe (Retriggerable)

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

After writing the Control Word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N+1 CLK pulses after trigger.

A trigger results in the Counter being loaded with the initial count on the next CLK pulse. The counting sequence is triggerable. OUT will not strobe low for N + 1 CLK pulses after any trigger. GATE has no effect on OUT.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count

expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

Operation Common to all Modes

Programming

When a Control Word is written to a Counter, all Control Logic is immediately reset and OUT goes to a known initial state; no CLK pulses are required for this.

Gate

The GATE input is always sampled on the rising edge of CLK. In Modes 0,2, 3, and 4 the Gate input is level sensitive, and the logic level is sampled on the rising edge of CLK. In Modes 1, 2, 3, and 5 the GATE input is rising-edge sensitive. In these Modes, a rising edge of Gate (trigger) sets an edge-sensitive flip-flop in the Counter. This flip-flop in the Counter. This flip-flop is reset immediately after it is sampled. In this way, a trigger will be detected no matter when it occurs - a high logic level does not have to be maintained until the next rising edge of CLK. Note that in Modes 2 and 3, the GATE input is both edge- and level-sensitive.

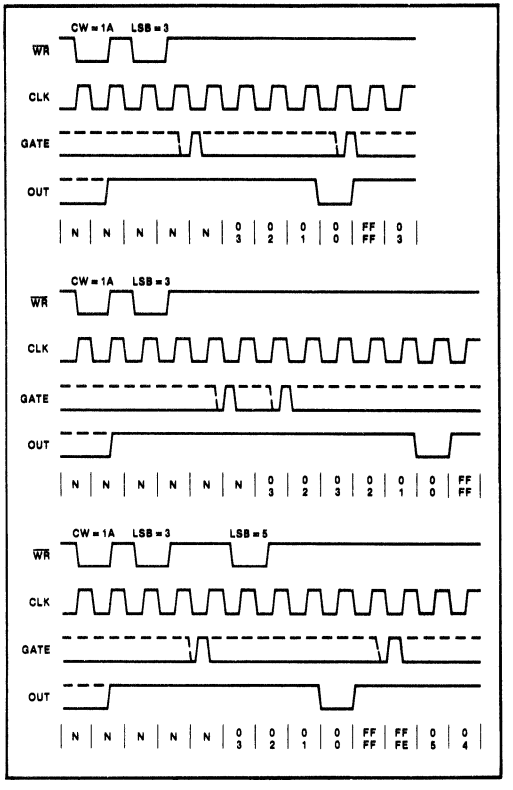


Figure 18. Mode 5

Counter

New counts are loaded and Counters are decremented on the falling edge of CLK.

The largest possible initial count is 0; this is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

The Counter does not stop when it reaches zero. In Modes 0, 1, 4, and 5 the Counter "wraps around" to the highest count, either FFFF hex for binary counting or 9999 for BCD counting, and continues counting. MOdes 2 and 3 are periodic; the Counter reloads itself with the initial count and continues counting from there.

Signal Status Modes	Low Or Going Low	Rising	High
0	Disables counting	— —	Enables counting
1	— —	1) Initiates counting 2) Resets output after next clock	— —
2	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	Disables counting	— —	Enables counting
5	— —	Initiates counting	— —

Figure 19. Gate Pin Operations Summary

Mode	Min Count	Max Count
0	1	0
1	1	0
2	2	0
3	3	0
4	1	0
5	1	0

NOTE: 0 IS EQUIVALENT TO 2^{16} FOR BINARY COUNTING AND 10^4 FOR BCD COUNTING.

Figure 20. Minimum and Maximum Initial Counts

Specifications

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0 Volts	Operating Temperature Range	
Operating Voltage Range	+4V to +7V	Commercial	0°C TO +70°C
Input Voltage Applied	GND-2.0V to +6.5V	Industrial	-40°C to +85°C
Output Voltage Applied	GND-0.5V to VCC +0.5V	Military	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C	Maximum Power Dissipation	1 Watt

CAUTION: Stresses above those listed in the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. ELECTRICAL CHARACTERISTICS

VCC = 5.0V±10%; TA = 0°C to +70°C (C82C54); TA = -40°C to +85°C (I82C54); TA = -55°C to +125°C (M82C54)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0 2.2		V V	C82C54, I82C54 M82C54
VIL	Logical Zero Input Voltage		0.8	V	
VOH	Output High Voltage	3.0 VCC -0.4		V V	IOH= -2.5mA IOH= -100μA
VOL	Output Low Voltage		0.4	V	IOL = +2.5mA
IIL	Input Leakage Current	-1.0	+1.0	μA	OV≤VIN≤VCC
IO	Output Leakage Current	-10.0	+10.0	μA	OV≤VO≤VCC
ICCSB	Standby Power Supply Current		10	μA	VCC = 5.5V VIN = VCC or GND OUTPUTS OPEN
ICCOP	Operating Power Supply Current		10	mA	VCC = 5.5V CLK FREQ = 8MHz OUTPUTS OPEN

CAPACITANCE

TA = 25°C; VCC = GND = OV; VIN = +5V or GND

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
C_{IN}*	Input Capacitance		5	pf	FREQ = 1MHz Unmeasured pins returned to GND
C_{OUT}*	Output Capacitance		15	pf	
$C_{I/O}$*	I/O Capacitance		20	pf	

*Guaranteed and sampled, but not 100% tested.

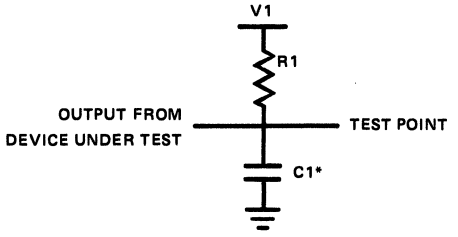
A.C. CHARACTERISTICS

VCC = +5V±10%: TA = 0°C to +70°C (C82C54);TA = -40°C to +85°C (I82C54); TA = -55°C to +125°C (M82C54)

Bus Parameters

READ CYCLE					
SYMBOL	**PARAMETER**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
TAR	Address Stable Before $\overline{RD}$	45		ns	
TSR	CS Stable Before $\overline{RD}$	0		ns	
TRA	Address Hold Time After $\overline{RD}$	0		ns	
TRR	$\overline{RD}$ Pulse Width	150		ns	
TRD	Data Delay from $\overline{RD}$		120	ns	
TAD	Data Delay from Address		220	ns	
TDF	$\overline{RD}$ to Data Floating	5	90	ns	
TRV	Command Recovery Time	200		ns	
WRITE CYCLE					
TAW	Address Stable Before $\overline{WR}$	0		ns	
TSW	CS Stable Before $\overline{WR}$	0		ns	
TWA	Address Hold Time $\overline{WR}$	0		ns	
TWW	$\overline{WR}$ Pulse Width	150		ns	
TDW	Data Setup Time Before $\overline{WR}$	140		ns	
TWD	Data Hold Time After $\overline{WR}$	10		ns	
TRV	Command Recovery Time	200		ns	
CLOCK AND GATE					
TCLK	Clock Period	125	DC	ns	
TPWH	High Pulse Width	60		ns	
TPWL	Low Pulse Width	60		ns	
TR	Clock Rise Time		100	ns	
TF	Clock Fall Time		100	ns	
TGW	Gate Width High	50		ns	
TGL	Gate Width Low	50		ns	
TGS	Gate Setup Time to CLK	50		ns	
TGH	Gate Hold Time After CLK	50		ns	
TOD	Output Delay from CLK		150	ns	
TODG	Output Delay from Gate		120	ns	

A.C. Test Circuits

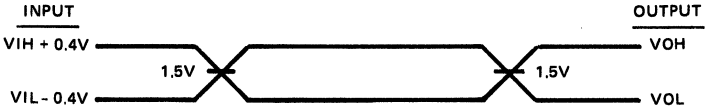


*Includes stray and jig capacitance

TEST CONDITION	V1	R1	R2	C1
1	1.7V	523	OPEN	150pf
2	5.0V	2K	1.7K	50pf
3	1.5V	750	OPEN	OPEN

TEST CONDITION DEFINITION TABLE

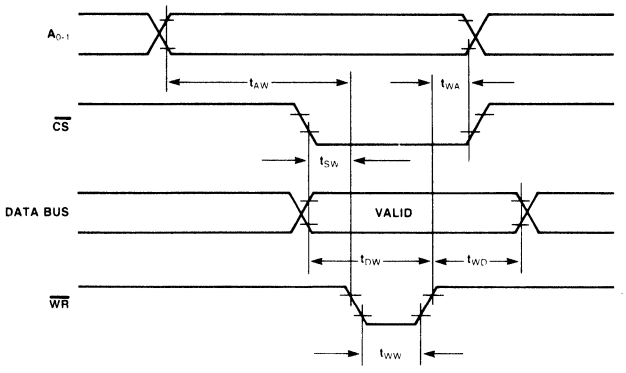
A.C. Testing Input, Output Waveform



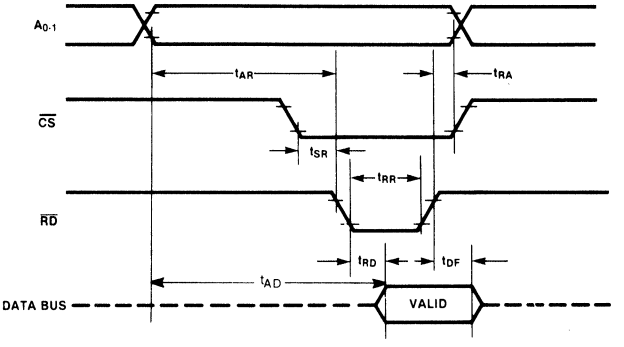
A. C. Testing: All input signals must switch between VIL -0.4V and VIH +0.4V
T_R and T_F must be less than or equal to 15ns.

Waveforms

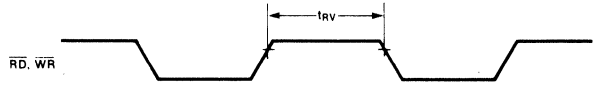
WRITE



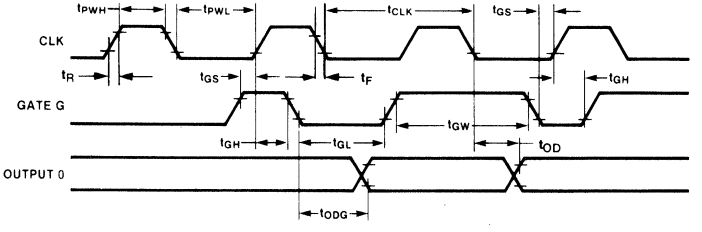
READ



RECOVERY



CLOCK AND GATE



HARRIS

82C55A

CMOS PROGRAMMABLE PERIPHERAL INTERFACE

Advance Information

Features

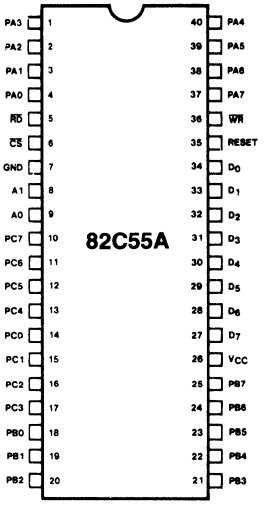
- PIN COMPATIBLE WITH NMOS 8255A
- 24 PROGRAMMABLE I/O PINS
- FULLY TTL COMPATIBLE
- BUS-HOLD CIRCUITRY ON ALL I/O PORTS ELIMINATES PULL-UP RESISTORS
- HIGH SPEED, NO "WAIT STATE" OPERATION WITH 8MHz 80C86
- DIRECT BIT SET/RESET CAPABILITY
- ENHANCED CONTROL WORD READ CAPABILITY
- SCALED SAJI IV CMOS PROCESS
- SINGLE 5V POWER SUPPLY
- 2.5 mA DRIVE CAPABILITY ON ALL I/O PORT OUTPUTS
- LOW STANDBY POWER – ICCSB = 10 μA
- COMMERCIAL, INDUSTRIAL AND MILITARY TEMPERATURE RANGES

Description

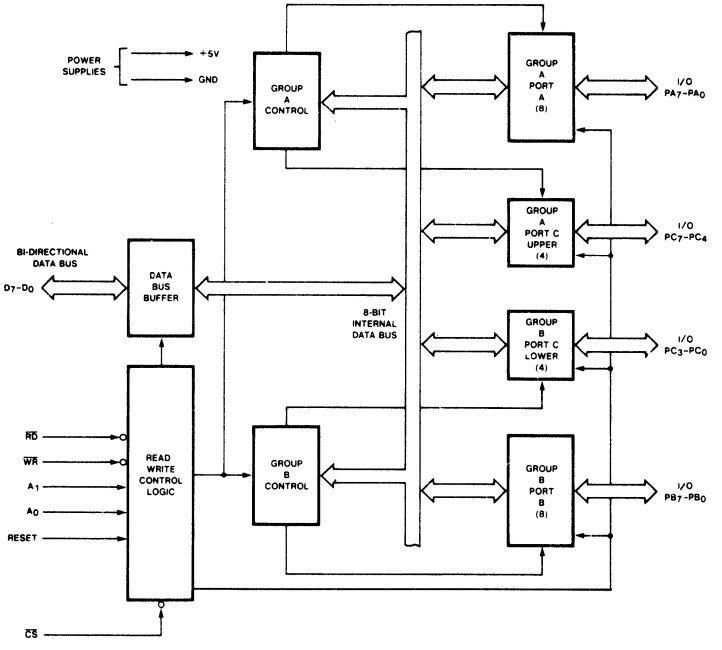
The Harris 82C55A is a high performance CMOS version of the industry standard 8255A and is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). It is a general purpose programmable I/O device which may be used with many different microprocessors. There are 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The high performance and industry standard configuration of the 82C55A make it compatible with microprocessors such as the 80C86, 8048, 8051, and NSC800.

Static CMOS circuit design insures low operating power. TTL compatibility of VIH = 2.0 volts over the industrial temperature range and bus hold circuitry eliminate the need for pull-up resistors. Harris's advanced SAJI process results in performance equal to or greater than existing equivalent products at a fraction of the power.

Pinout



Functional Diagram



PIN NAMES

D_7-D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

3 80C86 FAMILY

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

82C55A FUNCTIONAL DESCRIPTION

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select. A "low" on this input pin enables the communication between the 82C55A and the CPU.

($\overline{RD}$)

Read. A "low" on this input pin enables the 82C55A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 82C55A.

($\overline{WR}$)

Write. A "low" on this input pin enables the CPU to write data or control words into the 82C55A.

(A_0 and A_1)

Port Select 0 and Port Select 1. These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A_0 and A_1).

82C55A BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A→DATA BUS
0	1	0	1	0	PORT B→DATA BUS
1	0	0	1	0	PORT C→DATA BUS
1	1	0	1	0	CONTROL WORD→DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS→PORT A
0	1	1	0	0	DATA BUS→PORT B
1	0	1	0	0	DATA BUS→PORT C
1	1	1	0	0	DATA BUS→CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS→3-STATE
X	X	1	1	0	DATA BUS→3-STATE

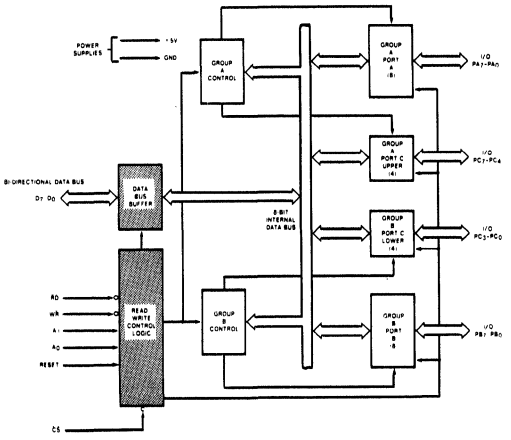


Figure 1
82C55A Block Diagram
Data Bus Buffer and Read/Write Control Logic Functions

(RESET)

Reset. A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode. "Bus hold" devices internal to the 82C55A will hold the I/O port inputs to a logic "1" state with a maximum hold current of 300 μA.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 82C55A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 82C55A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A – Port A and Port C upper (C7-C4)

Control Group B – Port B and Port C lower (C3-C0)

The control word register can be both written and read as shown in the "Basic Operation" table. Figure 4 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic "1", as this implies control word mode information.

Ports A, B and C

The 82C55A contains three 8-bit ports (A, B, and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 82C55A.

Port A One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-down" bus-hold devices are present on Port A.

Port B One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

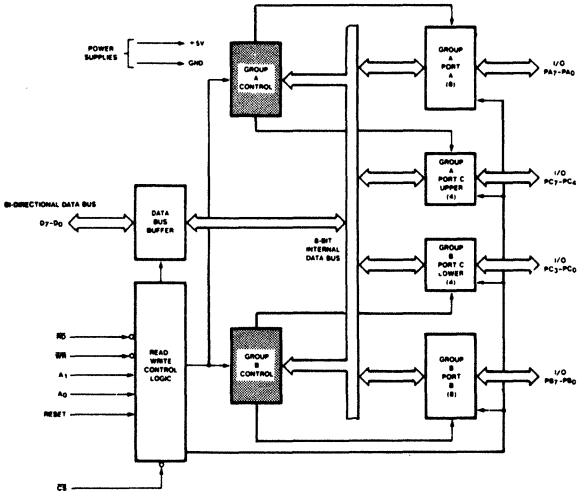


Figure 2
82C55A Block Diagram Showing Group A and Group B Control Functions

82C55A OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 – Basic Input/Output
Mode 1 – Strobed Input/Output
Mode 2 – Bi-Directional Bus

When the reset input goes "high", all ports will be set to the input mode with all 24 port lines held at a logic "one" level by internal bus hold devices. After the reset is removed, the 82C55A can remain in the input mode with no additional initialization required. This eliminates the need for pullup or pulldown resistors in all-CMOS designs. During the execution of the system program, any of the other modes may be selected using a single output instruction. This allows a single 82C55A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance: Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

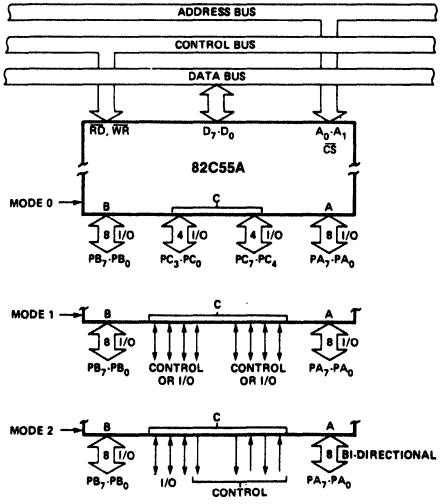


Figure 3
Basic Mode Definitions and Bus Interface

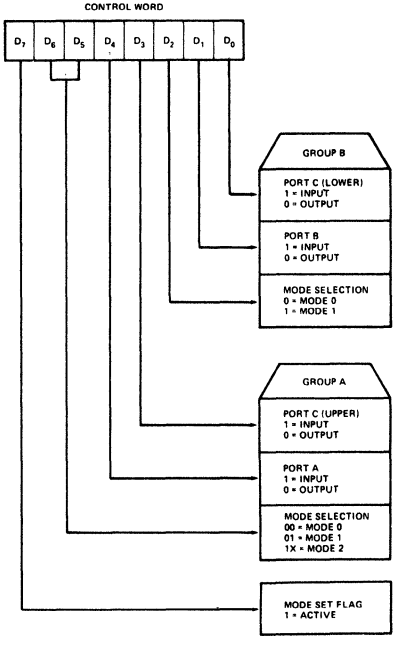


Figure 4
Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 82C55A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

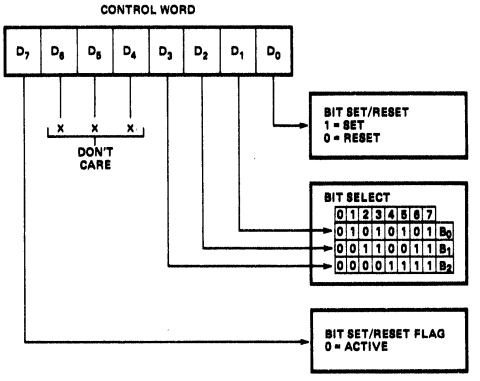


Figure 5
Bit Set/Reset Format

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 82C55A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the programmer to enable or disable a CPU interrupt by a specific I/O device without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET)—INTE is SET – Interrupt enable
(BIT-RESET)—INTE is RESET – Interrupt disable.

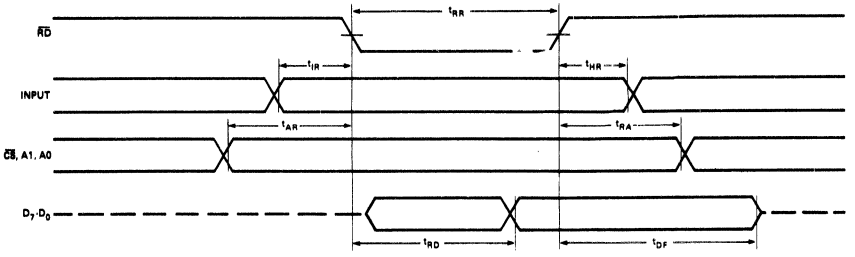
Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

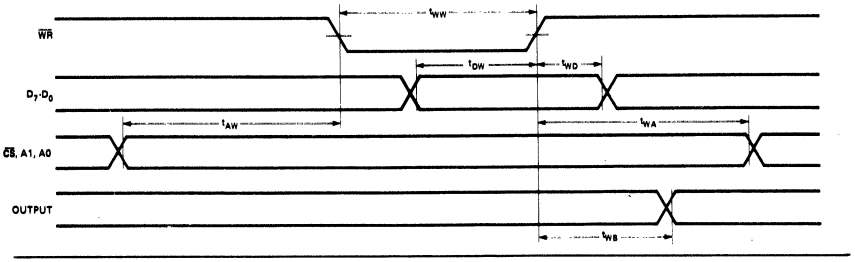
Mode O (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No handshaking is required, data is simply written to or read from a specific port.

Mode O Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports
- Any port can be input or output
- Outputs are latched
- Inputs are not latched
- 16 different Input/Output configurations possible



MODE 0 (Basic Input)



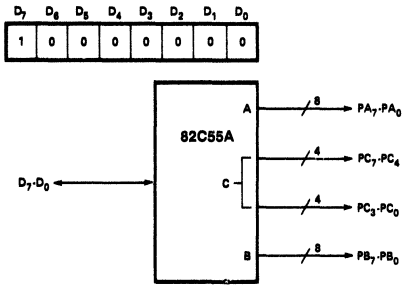
MODE 0 (Basic Output)

MODE 0 Port Definition

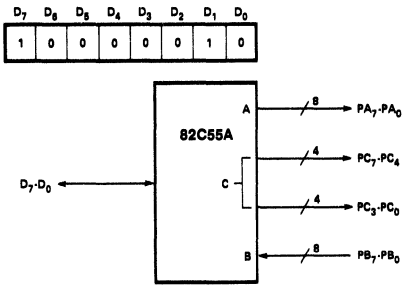
A		B		GROUP A			GROUP B	
D_4	D_3	D_1	D_0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE 0 Configurations

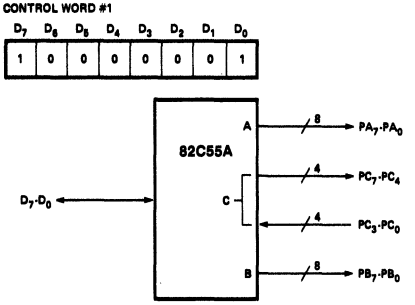
CONTROL WORD #0



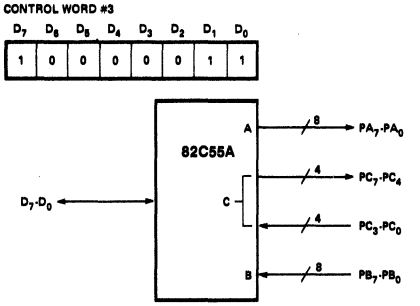
CONTROL WORD #2



CONTROL WORD #1

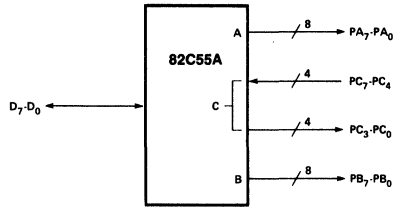


CONTROL WORD #3



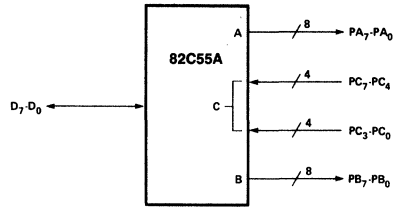
CONTROL WORD #4

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	0



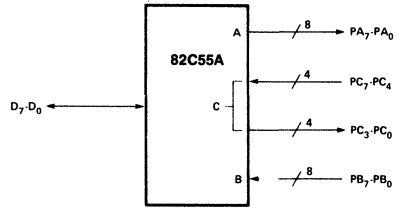
CONTROL WORD #5

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	1



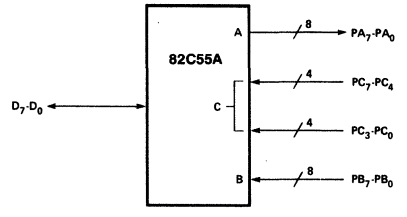
CONTROL WORD #6

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	0



CONTROL WORD #7

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	1



CONTROL WORD #8

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
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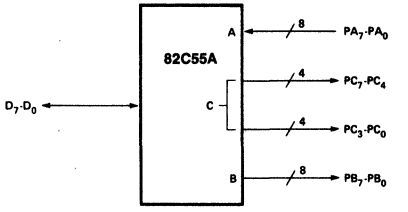
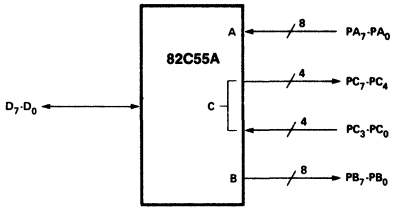


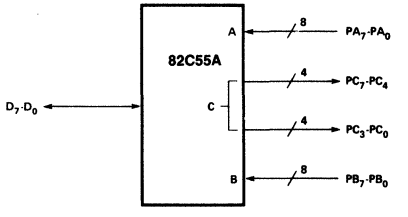
CONTROL WORD #9

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	1



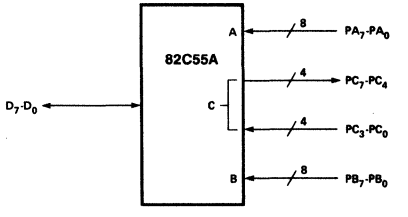
CONTROL WORD #10

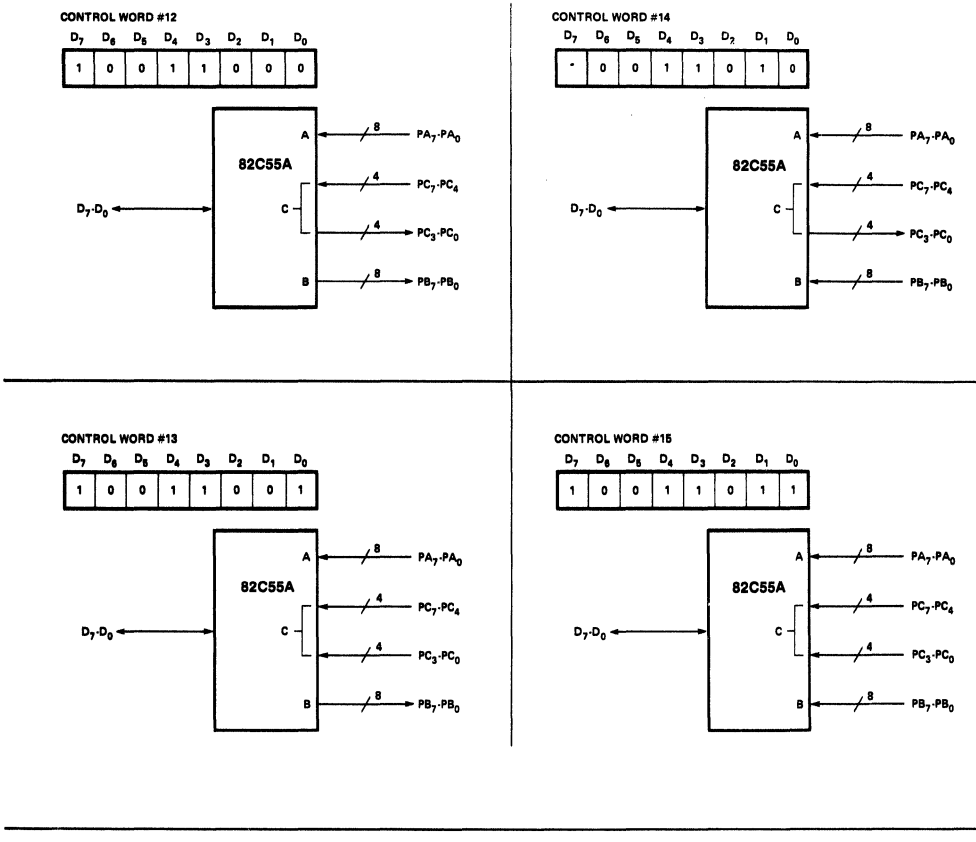
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	0



CONTROL WORD #11

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	1





Operating Modes

Mode 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and port B use the lines on port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit port.

Input Control Signal Definition

$\overline{STB}$ (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of the $\overline{RD}$ input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the condition: STB is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC_4.

INTE B

Controlled by bit set/reset of PC_2.

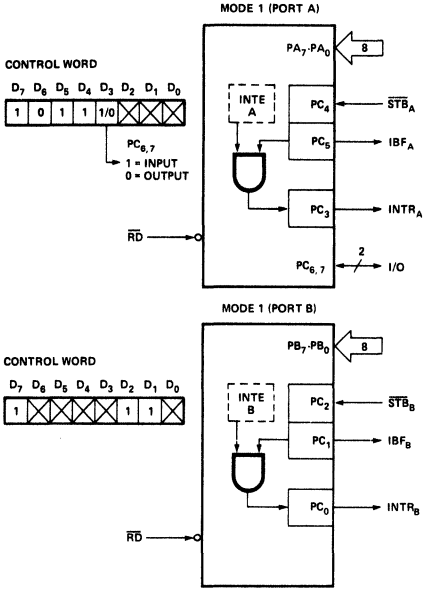


Figure 6
MODE 1 Input

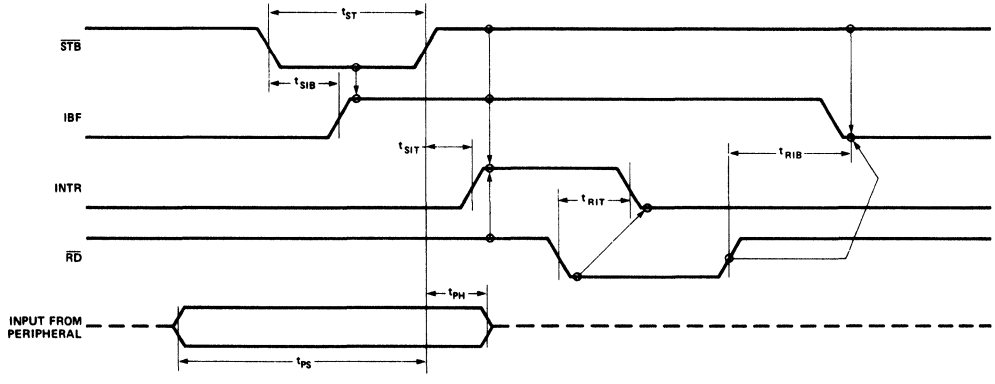


Figure 7
MODE 1 (Strobed Input)

OUTPUT CONTROL SIGNAL DEFINITION

$\overline{OBF}$ (Output Buffer Full F/F). The OBF output will go "low" to indicate that the CPU has written data out to the specified port. The $\overline{OBF}$ F/F will be set by the rising edge of the $\overline{WR}$ input and reset by $\overline{ACK}$ Input being low.

$\overline{ACK}$ (Acknowledge Input). A "low" on this input informs the 82C55A that the data from port A or port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a "one", $\overline{OBF}$ is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{WR}$.

INTE A

Controlled by Bit Set/Reset of CS_2.

INTE B

Controlled by Bit Set/Reset of PC_6.

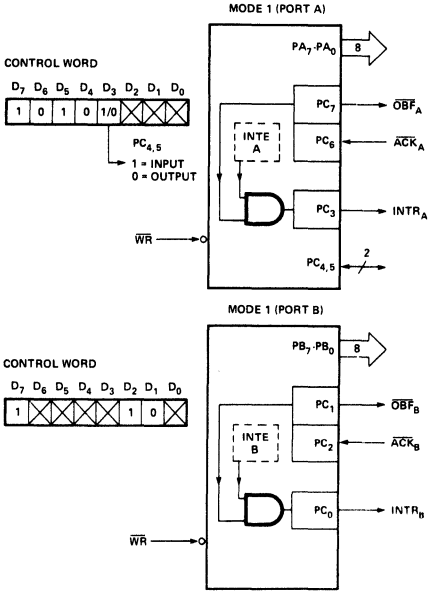


Figure 8
MODE 1 Output

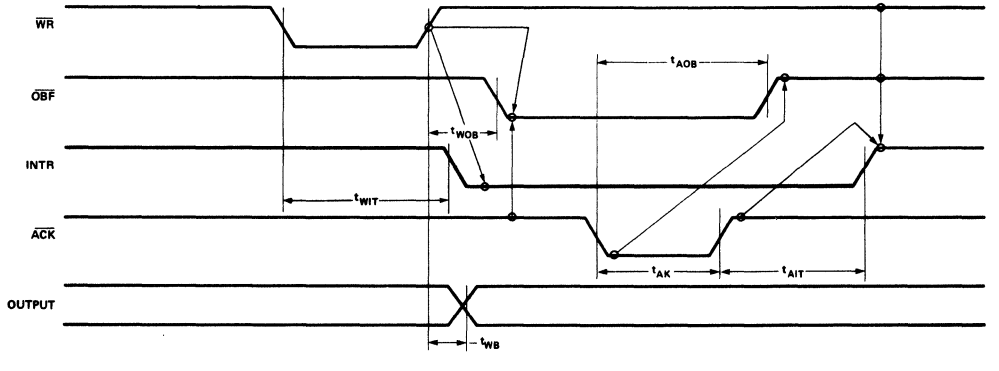


Figure 9
MODE 1 (Strobed Output)

Combinations of MODE 1: Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

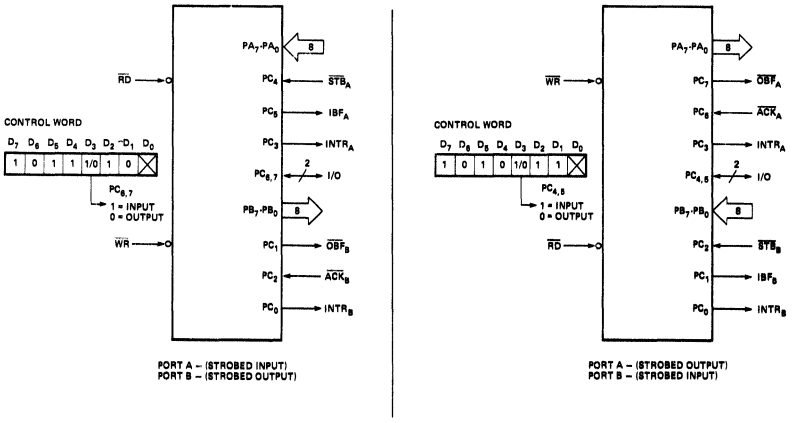


Figure 10
Combinations of MODE 1

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O)

The functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline similar to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Full). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to port A.

$\overline{ACK}$ (Acknowledge). A "low" on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with $\overline{OBF}$). Controlled by bit set/reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of PC_4.

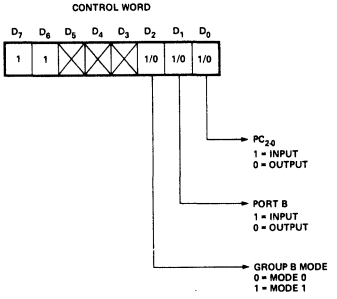


Figure 13. MODE Control Word

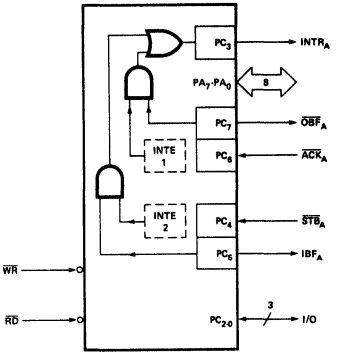


Figure 14. MODE 2

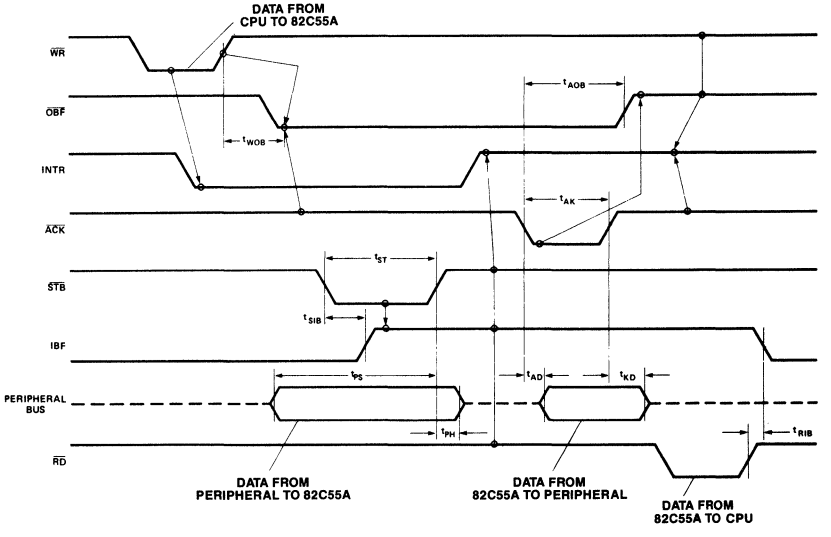


Figure 15. MODE 2 (Bidirectional)

Note: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible. ($INTR = IBF \cdot MASK \cdot \overline{STB} \cdot \overline{RD} + \overline{OBF} \cdot MASK \cdot \overline{ACK} \cdot \overline{WR}$)

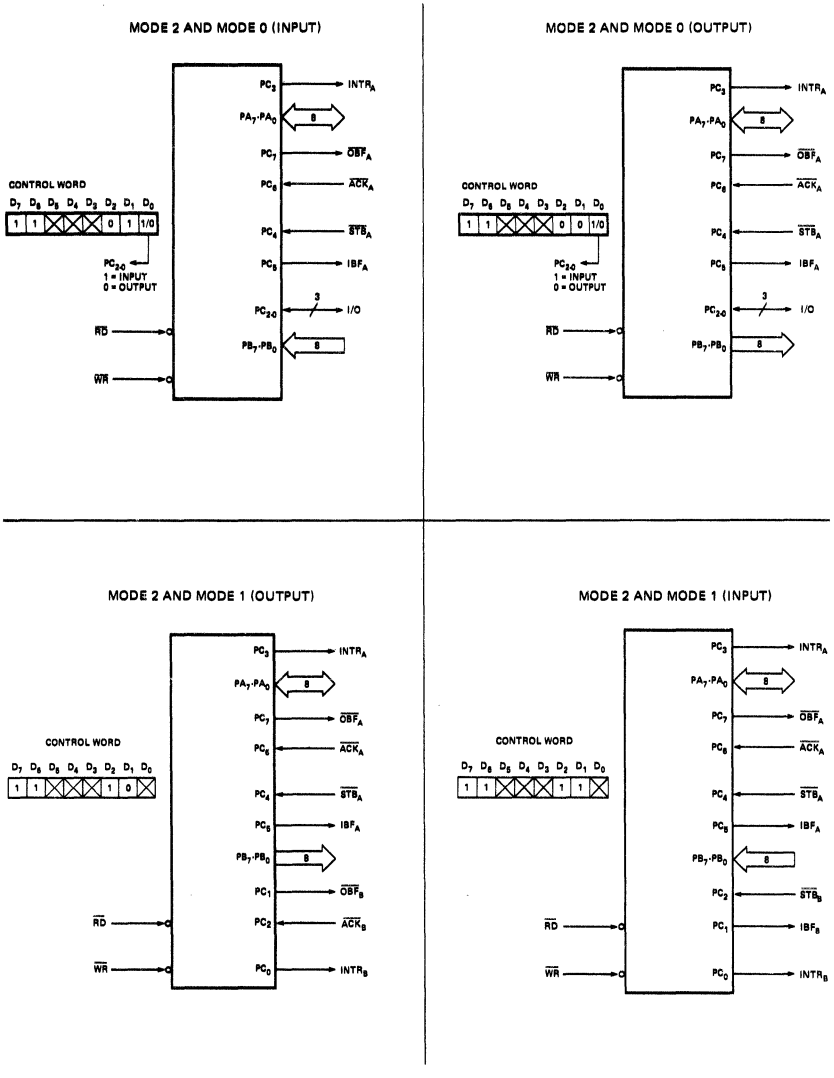


Figure 16
MODE 2 Combinations

Mode Definition Summary

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA_0	IN	OUT	IN	OUT	↔	
PA_1	IN	OUT	IN	OUT	↔	
PA_2	IN	OUT	IN	OUT	↔	
PA_3	IN	OUT	IN	OUT	↔	
PA_4	IN	OUT	IN	OUT	↔	
PA_5	IN	OUT	IN	OUT	↔	
PA_6	IN	OUT	IN	OUT	↔	
PA_7	IN	OUT	IN	OUT	↔	
PB_0	IN	OUT	IN	OUT	—	MODE 0 OR MODE 1 ONLY
PB_1	IN	OUT	IN	OUT	—	
PB_2	IN	OUT	IN	OUT	—	
PB_3	IN	OUT	IN	OUT	—	
PB_4	IN	OUT	IN	OUT	—	
PB_5	IN	OUT	IN	OUT	—	
PB_6	IN	OUT	IN	OUT	—	
PB_7	IN	OUT	IN	OUT	—	
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O	
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O	
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O	
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$	
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$	
PC_5	IN	OUT	IBF_A	I/O	IBF_A	
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$	
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$	

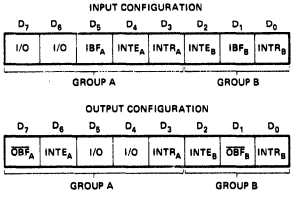


Figure 15. MODE 1 Status Word Format

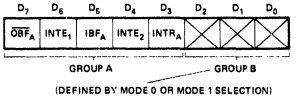


Figure 16. MODE 2 Status Word Format

Special Mode Combination Considerations:

There are several combinations of modes possible. For any combination, some or all of Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a "Set Mode" command.

During a read of Port C, the state of all the Port C lines, except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus. In place of the $\overline{ACK}$ and $\overline{STB}$ line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 17.

Through a "Write Port C" command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a "Write Port C" command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in a Mode 1 group or to change an interrupt enable flag, the "Set/Reset Port C Bit" command must be used.

With a "Set/Reset Port C Bit" command, any Port C line programmed as an output (including INTR, IBF and OBF) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, associated with Port C are not affected by a "Set/Reset Port C Bit" command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the "Set/Reset Port C Bit" command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 17.

Interrupt Enable Flag*	Position	Alternate Port C Pin Signal (Mode)
INTE B	PC2	$\overline{ACK}_B$ (Output Mode 1) or $\overline{STB}_B$ (Input Mode 1)
INTE A2	PC4	$\overline{STB}_A$ (Input Mode 1 or Mode 2)
INTE A1	PC6	$\overline{ACK}_A$ (Output Mode 1 or Mode 2)

Figure 17
Interrupt Enable Flags in Modes 1 and 2

Current Drive Capability:

Any output on Port A, B or C can sink or source 2.5mA. This feature allows the 82C55A to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 82C55A is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

APPLICATIONS OF THE 82C55A

The 82C55A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 82C55A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 82C55A to exactly "fit" the application. Figures 19 through 25 present a few examples of typical applications of the 82C55A.

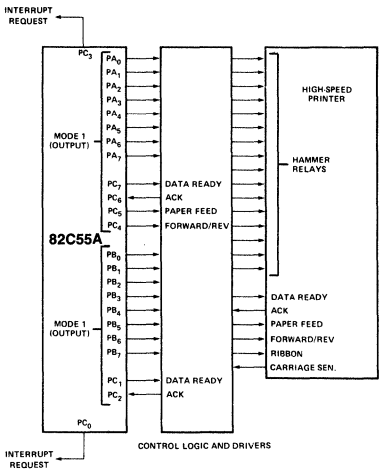


Figure 19. Printer Interface

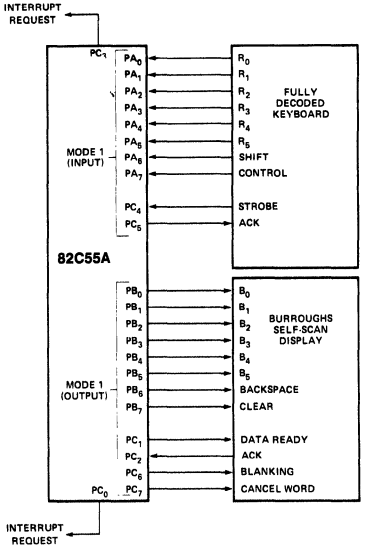


Figure 20. Keyboard and Display Interface

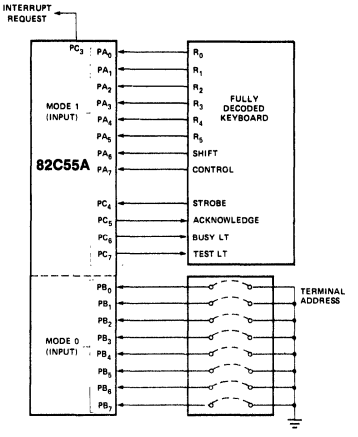


Figure 21. Keyboard and Terminal Address Interface

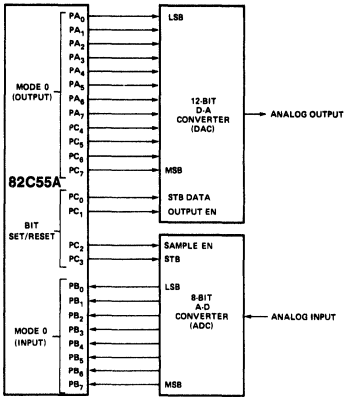


Figure 22. Digital to Analog, Analog to Digital

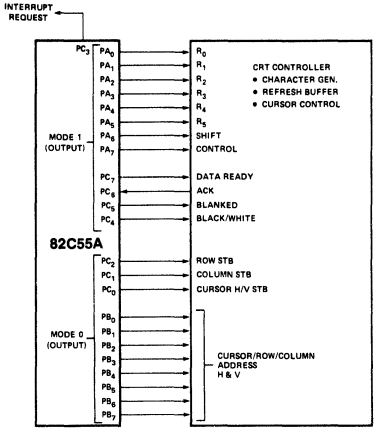


Figure 23. Basic CRT Controller Interface

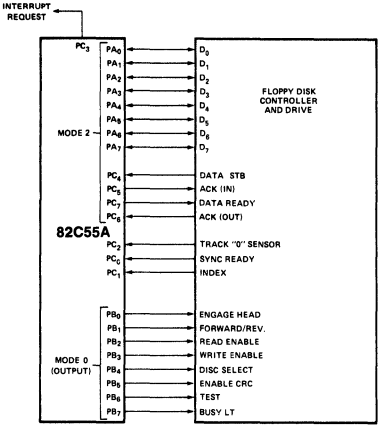


Figure 24. Basic Floppy Disc Interface

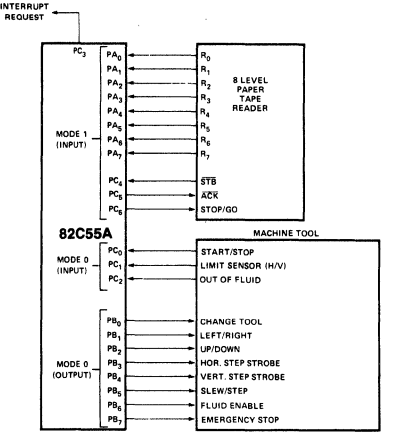


Figure 25. Machine Tool Controller Interface

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0 VOLTS	Operating Temperature Range	
Operating Voltage Range	+4V to +7V	Commercial	0°C to +70°C
Input Voltage Applied	GND−2.0V to 6.5V	Industrial	−40°C to +85°C
I/O Pin Voltage Applied	GND−0.5V to VCC+0.5V	Military	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	Maximum Power Dissipation	1 Watt

CAUTION: Stresses above those listed in the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. ELECTRICAL CHARACTERISTICS

VCC = -5.0V+/-10%; T_A = 0°C to +70°C (C82C55A); T_A = -40°C to +85°C (I82C55A); T_A = -55°C to +125°C (M82C55A)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	LOGICAL ONE INPUT VOLTAGE	2.0 2.2		V V	I82C55A M82C55A
VIL	LOGICAL ZERO INPUT VOLTAGE		0.8	V	
VOH	LOGICAL ONE OUTPUT VOLTAGE	3.0 VCC−0.4		V V	IOH = −2.5 mA IOH=−100 μA
VOL	LOGICAL ZERO OUTPUT VOLTAGE		0.4	V	IOL=+2.5 mA
IIL	INPUT LEAKAGE CURRENT	−1.0	1.0	μA	OV≤VIN≤VCC
IO	I/O PIN LEAKAGE CURRENT	−10.0	10.0	μA	OV≤VO≤VCC
IBHH	BUS HOLD HIGH CURRENT	−50	−300	μA	VO=3.0V PORTS A, B, C
IBHL	BUS HOLD LOW CURRENT	+50	+300	μA	VO=1.0V PORT A ONLY
IDAR	DARLINGTON DRIVE CURRENT	−2.0		mA	PORTS A, B, C Test Condition 3
ICC	POWER SUPPLY CURRENT		10	μA	VCC=5.5V VIN=VCC or GND OUTPUTS OPEN

CAPACITANCE T_A = 25°C; VCC = GND = 0V; VIN = +5V or GND

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
CIN*	INPUT CAPACITANCE		5	pf	FREQ = 1 MHZ Unmeasured pins returned to GND
CI/O*	I/O PIN CAPACITANCE		20	pf	

* Guaranteed and sampled, but not 100% tested

A.C. CHARACTERISTICS

VCC = +5V ±10%, GND = 0V; T_A = 0°C to +70°C (C82C55A)
VCC = +5V ±10%, GND = 0V; T_A = -40°C to +85°C (I82C55A)
VCC = +5V ±10%, GND = 0V; T_A = -55°C to +125°C (M82C55A)

Bus Parameters

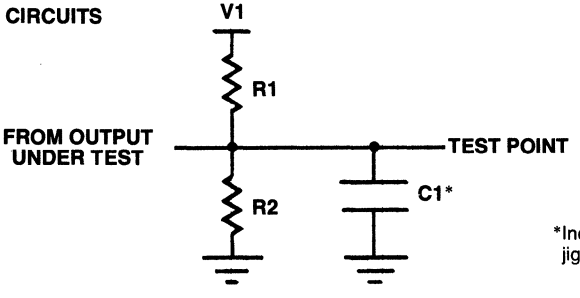
READ		I82C55A		M82C55A			TEST
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	CONDITIONS
tAR	Address Stable Before READ	0		0		ns	
tRA	Address Stable After READ	0		0		ns	
tRR	READ Pulse Width	150		150		ns	
tRD	Data Valid From READ		100		100	ns	1
tDF	Data Float After READ	10	75	10	75	ns	2
tRV	Time Between READs and/or WRITEs	300		300		ns	

WRITE		I82C55A		M82C55A			TEST
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	CONDITIONS
tAW	Address Stable Before WRITE	0		0		ns	
tWA	Address Stable After WRITE	20		20		ns	Ports A & B
		60		80		ns	Port C
tWW	WRITE Pulse Width	100		100		ns	
tDW	Data Valid to WRITE High	100		100		ns	
tWD	Data Valid After WRITE High	30		30		ns	Ports A & B
		60		80		ns	Port C

OTHER TIMINGS		I82C55A		M82C55A			TEST
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	CONDITIONS
tWB	WR = 1 to Output		350		350	ns	1
tIR	Peripheral Data Before RD	0		0		ns	
tHR	Peripheral Data After RD	0		0		ns	
tAK	ACK Pulse Width	100		100		ns	
tST	STB Pulse Width	100		100		ns	
tPS	Per. Data Before STB High	20		20		ns	
tPH	Per. Data After STB High	50		50		ns	
tAD	ACK = 0 to Output		175		175	ns	1
tKD	ACK = 1 to Output Float	20	250	20	250	ns	2
tWOB	WR = 1 to OBF = 0		150		150	ns	1
tAOB	ACK = 0 to OBF = 1		150		150	ns	1
tSIB	STB = 0 to IBF = 1		150		150	ns	1
tRIB	RD = 1 to IBF = 0		150		150	ns	1
tRIT	RD = 0 to INTR = 0		200		200	ns	1
tSIT	STB = 1 to INTR = 1		150		150	ns	1
tAIT	ACK = 1 to INTR = 1		150		150	ns	1
tWIT	WR = 0 to INTR = 0		200		200	ns	1
tRES	Reset Pulse Width	500		500		ns	see note 1

NOTE 1: Period of initial Reset pulse after power-on must be at least 50usec. Subsequent Reset pulses may be 500 ns minimum.

82C55A AC TEST CIRCUITS



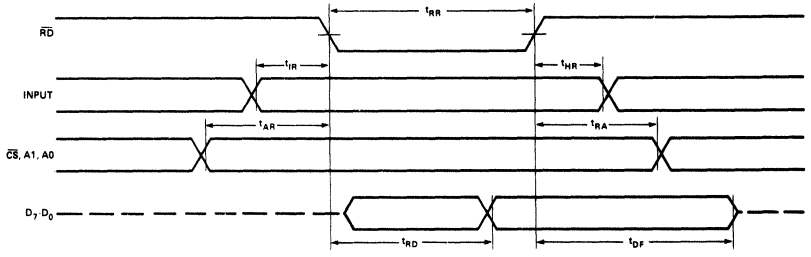
*Includes stray and jig capacitance

TEST CONDITION	V1	R1	R2	C1
1	1.7V	523Ω	OPEN	150 pf
2	5.0V	2KΩ	1.7KΩ	50 pf
3	1.5V	750Ω	OPEN	OPEN

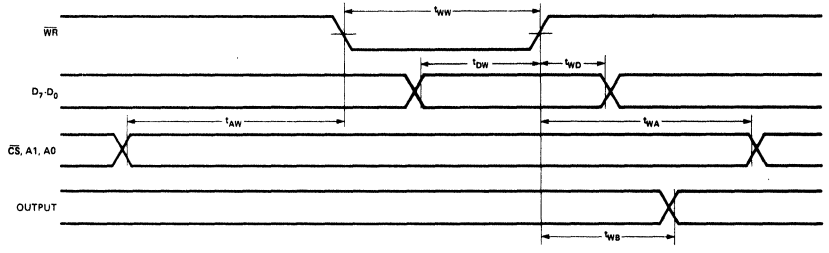
TEST CONDITION DEFINITION TABLE

WAVEFORMS

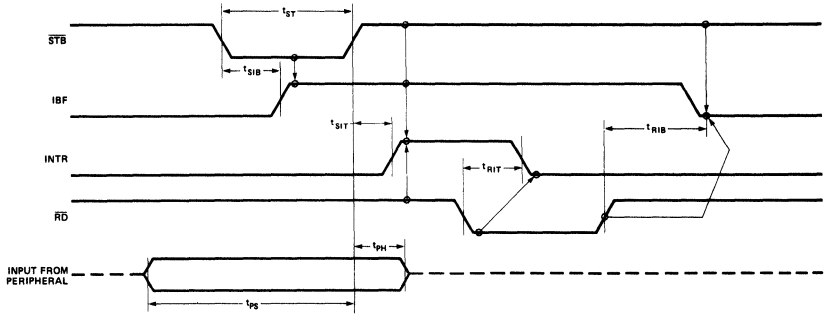
MODE 0 (BASIC INPUT)



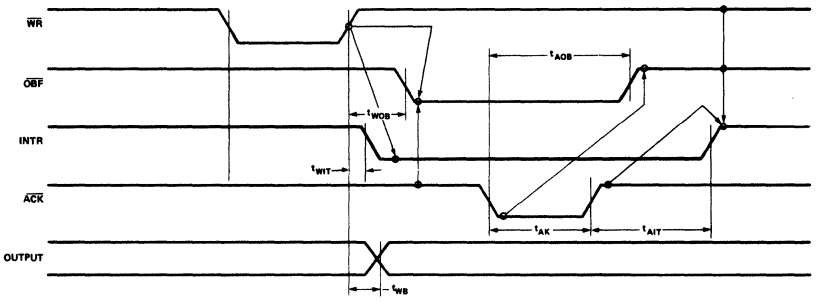
MODE 0 (BASIC OUTPUT)



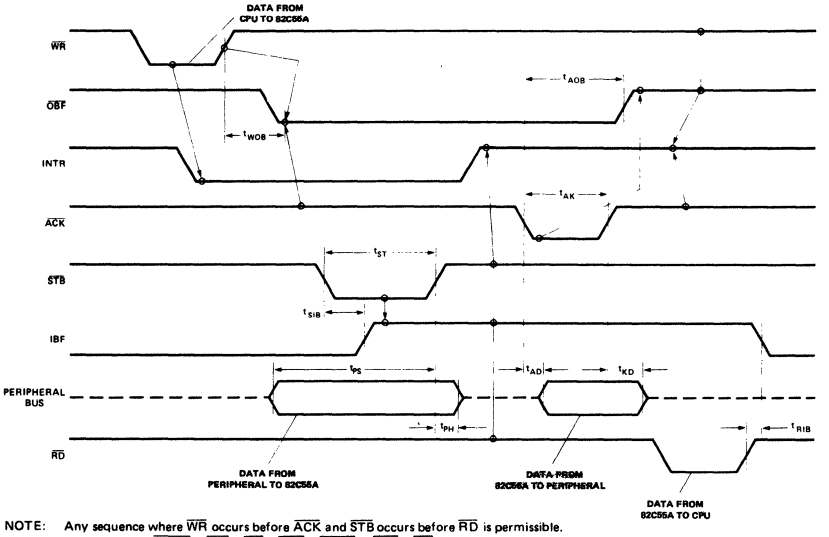
MODE 1 (STROBED INPUT)



MODE 1 (STROBED OUTPUT)

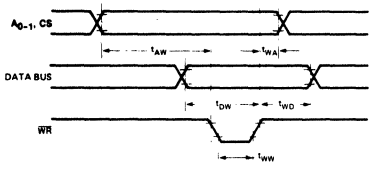


MODE 2 (BIDIRECTIONAL)

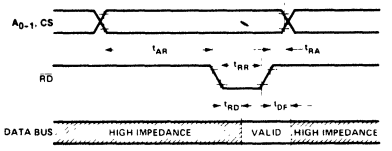


NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF • MASK • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • MASK • $\overline{ACK}$ • $\overline{WR}$)

WRITE TIMING



READ TIMING



HARRIS

82C59A

CMOS PROGRAMMABLE INTERRUPT CONTROLLER

Advance Information

Features

- PIN COMPATIBLE WITH NMOS 8259A
- EIGHT LEVEL PRIORITY CONTROLLER
- EXPANDABLE TO 64 LEVELS
- FULLY TTL COMPATIBLE
- HIGH SPEED, NO "WAIT STATE" OPERATION WITH 8 MHz 80C86
- PROGRAMMABLE INTERRUPT MODES
- 8080/8085 and 8086/80C86 COMPATIBLE OPERATION
- INDIVIDUAL REQUEST MASK CAPABILITY
- FULLY STATIC DESIGN
- SCALED SAJI IV CMOS PROCESS
- SINGLE 5V POWER SUPPLY
- LOW STANDBY POWER — 10μA
- COMMERCIAL, INDUSTRIAL and MILITARY TEMPERATURE RANGES

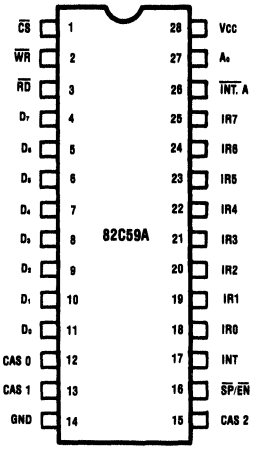
Description

The Harris 82C59A is a high performance CMOS Priority Interrupt Controller manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C59A is designed to relieve the system CPU from the task of polling in a multi-level priority interrupt system. The high speed and industry standard configuration of the 82C59A make it compatible with microprocessors such as the 80C86, 8086, 8080/85 and NSC800.

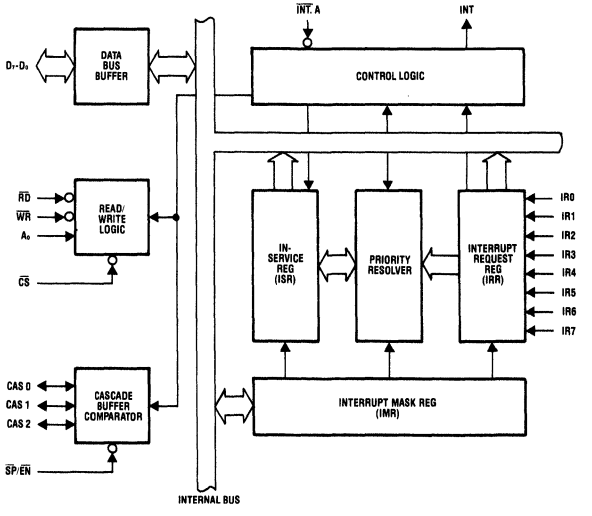
The 82C59A can handle up to eight vectored priority interrupting sources and is cascadable to 64 without additional circuitry. Individual interrupting sources can be masked or prioritized to allow custom system configuration. Two modes of operation make the 82C59A compatible with both 8080/85 and 80C86/86 formats.

Static CMOS circuit design insures low operating power. Harris advanced SAJI process results in performance equal to or greater than existing equivalent products at a fraction of the power.

Pinout



Functional Diagram



D_7-D_0	DATA BUS (BI-DIRECTIONAL)
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A_0	COMMAND SELECT ADDRESS
$\overline{CS}$	CHIP SELECT
CAS 2 - CAS 0	CASCADE LINES
$\overline{SP}/\overline{EN}$	SLAVE PROGRAM INPUT ENABLE
INT	INTERRUPT OUTPUT
$\overline{INTA}$	INTERRUPT ACKNOWLEDGE INPUT
IR0 - IR7	INTERRUPT REQUEST INPUTS

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. Pin Description

SYMBOL	PIN NO.	TYPE	NAME AND FUNCTION
V_{CC}	28	I	POWER SUPPLY: +5V Supply.
GND	14	I	GROUND.
$\overline{CS}$	1	I	CHIP SELECT: A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the 82C59A. INTA functions are independent of $\overline{CS}$.
$\overline{WR}$	2	I	WRITE: A low on this pin when $\overline{CS}$ is low enables the 82C59A to accept command words from the CPU.
$\overline{RD}$	3	I	READ: A low on this pin when $\overline{CS}$ is low enables the 82C59A to release status onto the data bus for the CPU.
D_7-D_0	4-11	I/O	BIDIRECTIONAL DATA BUS: Control, status and interrupt-vector information is transferred via this bus.
CAS 0 - CAS 2	12, 13, 15	I/O	CASCADE LINES: The CAS lines form a private 82C59A bus to control a multiple 82C59A structure. These pins are outputs for a master 82C59A and inputs for a slave 82C59A.
SP/EN	16	I/O	SLAVE PROGRAM/ENABLE BUFFER: This is a dual function pin. When in the Buffered Mode it can be used as an output to control buffer transceivers (EN). When not in the buffered mode it is used as an input to designate a master (SP=1) or slave (SP=0).
INT	17	O	INTERRUPT: This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IR0-IR7	18-25	I	INTERRUPT REQUESTS: Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode).
INTA	26	I	INTERRUPT ACKNOWLEDGE: This pin is used to enable 82C59A interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
A_0	27	I	ADDRESS LINE: This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the 82C59A to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A_0 address line (A_1 for 80C86/88).

Functional Description

INTERRUPTS IN MICROCOMPUTER SYSTEMS

Microcomputer system design requires that I/O devices such as keyboards, displays, sensors and other components receive servicing in an efficient manner so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughput.

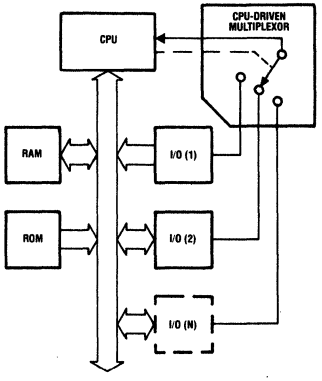
The most common method of servicing such devices is the Polled approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuous polling cycle and that such a method would have a serious, detrimental effect on system through-put, thus limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

A more desirable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete, however, the processor would resume exactly where it left off.

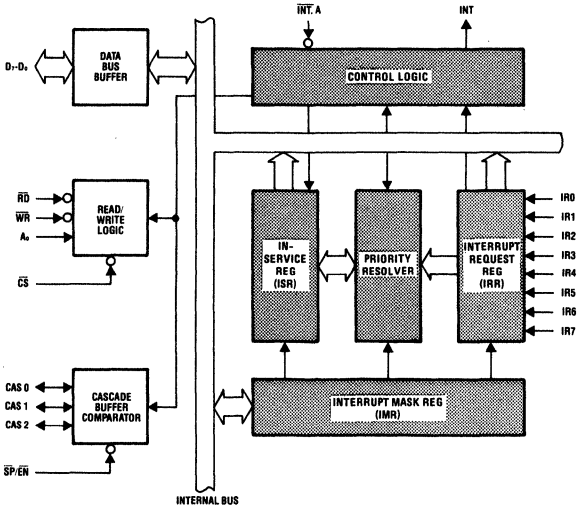
This is the interrupt-driven method. It is easy to see that system throughput would drastically increase, and thus more tasks could be assumed by the microcomputer to further enhance its cost effectiveness.

The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and issues an interrupt to the CPU based on this determination.

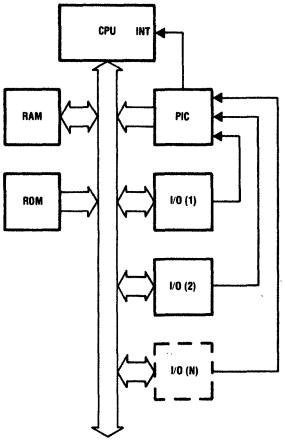
Each peripheral device or structure usually has a special program or "routine" that is associated with its specific functional or operational requirements; this is referred to as a "service routine". The PIC, after issuing an interrupt to the CPU, must somehow input information into the CPU that can "point" the Program Counter to the service routine associated with the requesting device. This "pointer" is an address in a vectoring table and will often be referred to, in this document, as vectoring data.



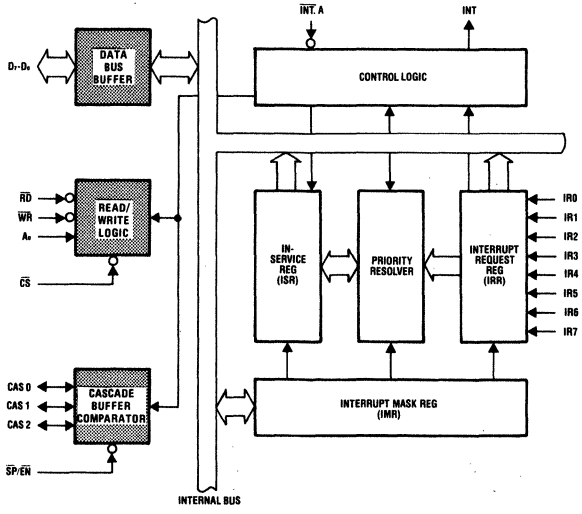
POLLED METHOD



82C59A INTERRUPT LOGIC



INTERRUPT METHOD



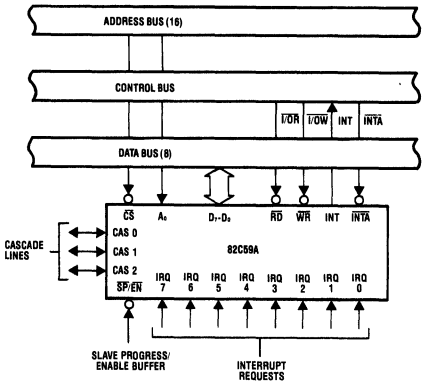
82C59A DATA AND CONTROL LOGIC

82C59A FUNCTIONAL DESCRIPTION

The 82C59A is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages eight levels of requests and has built-in features for expandability to other 82C59As (up to 64 levels). It is programmed by system software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the 82C59A can be configured to match system requirements. The priority modes can be changed or reconfigured dynamically at any time during main program operation. This means that the complete interrupt structure can be defined as required, based on the total system environment.

INTERRUPT REQUEST REGISTER (IRR) and IN-SERVICE REGISTER (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service, and the ISR is used to store all the interrupt levels which are currently being serviced.



PRIORITY RESOLVER

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during the INTA sequence.

INTERRUPT MASK REGISTER (IMR)

The IMR stores the bits which disable the interrupt lines to be masked. The IMR operates on the output of the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

INTERRUPT (INT)

This output goes directly to the CPU interrupt input. The V_{OH} level on this line is designed to be fully compatible with the 8080A, 8085A, 8086 and 80C86 input levels.

INTERRUPT ACKNOWLEDGE ($\overline{INTA}$)

$\overline{INTA}$ pulses will cause the 82C59A to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the 82C59A.

DATA BUS BUFFER

This 3-state, bidirectional 8-bit buffer is used to interface the 82C59A to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

READ/WRITE CONTROL LOGIC

The function of this block is to accept OUTput commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the 82C59A to be transferred onto the Data Bus.

CHIP SELECT ($\overline{CS}$)

A LOW on this input enables the 82C59A. No reading or writing of the device will occur unless the device is selected.

WRITE ($\overline{WR}$)

A LOW on this input enables the CPU to write control words (ICWs and OCWs) to the 82C59A.

READ ($\overline{RD}$)

A LOW on this input enables the 82C59A to send the status of the Interrupt Request Register (IRR), In Service Register (ISR), the Interrupt Mask Register (IMR), or the interrupt level (in the poll mode) onto the Data Bus.

A_0

This input signal is used in conjunction with $\overline{WR}$ and $\overline{RD}$ signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

THE CASCADE BUFFER/COMPARATOR

This function block stores and compares the IDs of all 82C59As used in the system. The associated three I/O pins (CAS0-2) are outputs when the 82C59A is used as a master and are inputs when the 82C59A is used as a slave. As a master, the 82C59A sends the ID of the interrupting slave device onto the CAS0-2 lines. The slave thus selected will send its preprogrammed subroutine address onto the Data Bus during the next one or two consecutive INTA pulses. (See section "Cascading the 82C59A".)

INTERRUPT SEQUENCE

The powerful features of the 82C59A in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specified interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

These events occur in an 8080A/8085 system:

1. One or more of the INTERRUPT REQUEST lines (I0-I7) are raised high, setting the corresponding IRR bit(s).
2. The 82C59A evaluates these requests in the priority resolver and sends an interrupt (INT) to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{INTA}$ pulse.
4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The 82C59A will also release a CALL instruction code (11001101) onto the 8-bit data bus through D_0-D_7.
5. This CALL instruction will initiate two additional $\overline{INTA}$ pulses to be sent to the 82C59A from the CPU group.
6. These two INTA pulses allow the 82C59A to release its preprogrammed subroutine address onto the data bus. The lower 8-bit address is released at the first INTA pulse and the higher 8-bit address is released at the second INTA pulse.
7. This completes the 3-byte CALL instruction released by the 82C59A. In the AEOI mode, the ISR bit is reset at the end of the third INTA pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occurring in an 80C86 system are the same until step 4.

4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The 82C59A does not drive the data bus during this cycle.
5. The 80C86 will initiate a second $\overline{INTA}$ pulse. During this pulse, the 82C59A releases an 8-bit pointer onto the data bus where it is read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode, the ISR bit is reset at the end of the second $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e.,the request was too short in duration), the 82C59A will issue an interrupt level 7. If a slave is programmed on IR bit 7, the CAS lines remain inactive and vector addresses are output from the master 82C59A.

Interrupt Sequence Outputs

8080, 8085

This sequence is timed by three $\overline{INTA}$ pulses. During the first $\overline{INTA}$ pulse, the CALL opcode is enabled onto the data bus.

First Interrupt Vector Byte Data: Hex CD

	D7	D6	D5	D4	D3	D2	D1	D0
CALL CODE	1	1	0	0	1	1	0	1

During the second $\overline{INTA}$ pulse, the lower address of the appropriate service routine is enabled onto the data bus. When interval = 4 bits, A_5-A_7 are programmed, while A_0-A_4 are automatically inserted by the 82C59A. When interval = 8, only A_6 and A_7 are programmed, while A_0-A_5 are automatically inserted.

Content of Second Interrupt Vector Byte

IR				Interval = 4				
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

IR				Interval = 8				
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

During the third $\overline{INTA}$ pulse, the higher address of the appropriate service routine, which was programmed as byte 2 of the initialization sequence (A_8-A_{15}), is enabled onto the bus.

Content of Third Interrupt Vector Byte

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

80C86, 80C88 INTERRUPT RESPONSE MODE

80C86 mode is similar to 8080/85 mode except that only two Interrupt Acknowledge cycles are issued by the processor and no CALL opcode is sent to the processor. The first interrupt acknowledge cycle is similar to that of 8080/85 systems in that the 82C59A uses it to internally freeze the state of the interrupts for priority resolution and, as a master, it issues the interrupt code on the cascade lines. On this first cycle, it does not issue any data to the processor and leaves its data bus buffers disabled. On the second interrupt acknowledge cycle in 80C86 mode, the master (or slave if so programmed) will send a byte of data to the processor with the acknowledged interrupt code composed as follows (note the state of the ADI mode control is ignored and A_5-A_{11} are unused in 80C86 mode.)

Content of Interrupt Vector Byte for 80C86 System Mode

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

PROGRAMMING THE 82C59A

The 82C59A accepts two types of command words generated by the CPU;

1. Initialization Command Words (ICWs): Before normal operation can begin, each 82C59A in the system must be brought to a starting point—by a sequence of 2 to 4 bytes timed by $\overline{WR}$ pulses.
2. Operation Command Words (OCWs): These are the command words which command the 82C59A to operate in various interrupt modes. Among these modes are:
   a. Fully nested mode
   b. Rotating priority mode
   c. Special mask mode
   d. Polled mode

The OCWs can be written into the 82C59A anytime after initialization.

Initialization Command Words (ICWS)

GENERAL

Whenever a command is issued with A0=0 and D4=1, this is interpreted as Initialization Command Word 1 (ICW1). ICW1 starts the initialization sequence during which the following automatically occur.

a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low-to-high transition to generate an interrupt.
b. The Interrupt Mask Register is cleared.
c. IR7 input is assigned priority 7.
d. Special Mask Mode is cleared and Status Read is set to IRR.
e. If IC4=0, then all functions selected in ICW4 are set to zero. (Non-Buffered mode*, no Auto-EOI, 8080/85 system).

*NOTE: Master/Slave in ICW4 is only used in the buffered mode.

INITIALIZATION COMMAND WORDS 1 and 2 (ICW1, ICW2)

A_5-A_{15}: Page starting address of service routines. In an 8080/85 system, the 8 request levels will generate CALLS to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus the 8 routines will occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes long (A_0-A_{15}). When the routine interval is 4, A_0-A_4 are automatically inserted by the 82C59A, while A_5-A_{15} are programmed externally. When the routine interval is 8, A_0-A_5 are automatically inserted by the 82C59A while A_6-A_{15} are programmed externally.

The 8-byte interval will maintain compatibility with current software, while the 4-byte interval is best for a compact jump table.

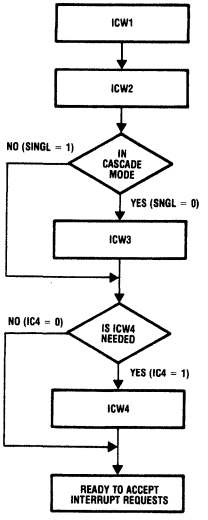
In an 80C86 system, A_{15}-A_{11} are inserted in the five most significant bits of the vectoring byte and the 82C59A sets the three least significant bits according to the interrupt level. A_{10}-A_5 are ignored and ADI (Address interval) has no effect.

LTIM: If LTIM = 1, then the 82C59A will operate in the level interrupt mode. Edge detect logic on the interrupt inputs will be disabled.

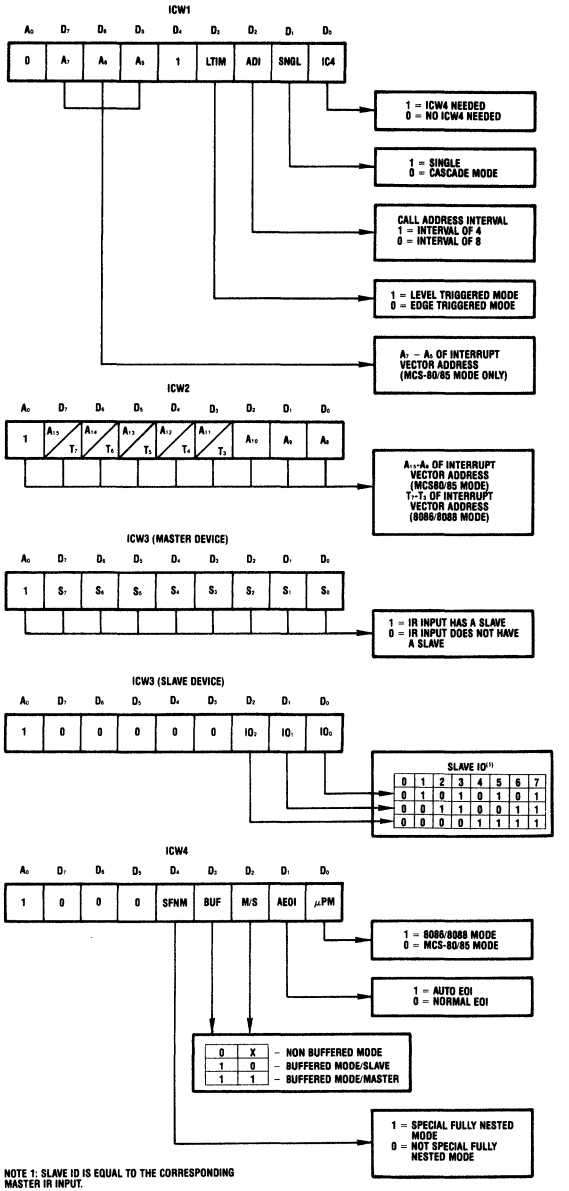
ADI: CALL address interval. ADI = 1 then interval = 4; ADI = 0 then interval = 8.

SNGL: Single. Means that this is the only 82C59A in the system. If SNGL=1, no ICW3 will be issued.

IC4: If this bit is set—ICW4 has to be issued. If ICW4 is not needed, set IC4 = 0.



82C59A INITIALIZATION SEQUENCE



82C59A INITIALIZATION COMMAND WORD FORMAT

INITIALIZATION COMMAND WORD 3 (ICW3)

This word is read only when there is more than one 82C59A in the system and cascading is used, in which case SNGL = 0. It will load the 8-bit slave register. The functions of this register are:

a. In the master mode (either when SP=1, or in buffered mode when M/S=1 in ICW4), a "1" is set for each slave in the bit corresponding to the appropriate IR line for the slave. The master then will release byte 1 of the call sequence (for 8080/85 system) and will enable the corresponding slave to release bytes 2 and 3 (for 80C86, only byte 2) through the cascade lines.

b. In the slave mode (either when SP=0, or if BUF=1 and M/S=0 in ICW4), bits 2-0 identify the slave. The slave compares its cascade input with these bits and if they are equal, bytes 2 and 3 of the call sequence (or just byte 2 for 80C86) are released by it on the Data Bus (Note: the slave address must correspond to the IR line it is connected to in the master ID).

INITIALIZATION COMMAND WORD 4 (ICW4)

SFNM: If SFNM = 1, the special fully nested mode is programmed.

BUF: If BUF = 1, the buffered mode is programmed. In buffered mode, $\overline{SP}/\overline{EN}$ becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S = 1 means the 82C59A is programmed to be a master, M/S = 0 means the 82C59A is programmed to be a slave. If BUF = 0, M/S has no function.

AEOI: If AEOI = 1, the automatic end of interrupt mode is programmed.

μPM: Microprocessor mode: μPM = 0 sets the 82C59A for 8080/85 system operation, μPM = 1 sets the 82C59A for 80C86 system operation.

OPERATION COMMAND WORDS (OCWs)

After the initialization Command Words (ICWs) are programmed into the 82C59A, the device is ready to accept interrupt requests at its input lines. However, during the 82C59A operation, a selection of algorithms can command the 82C59A to operate in various modes through the Operation Command Words (OCWs).

OPERATION CONTROL WORDS (OCWs)

	A0	D7	D6	D5	D4	D3	D2	D1	D0
OCW1	1	M7	M6	M5	M4	M3	M2	M1	M0
OCW2	0	R	SL	EOI	0	0	L2	L1	L0
OCW3	0	0	ESMM	SMM	0	1	P	RR	RIS

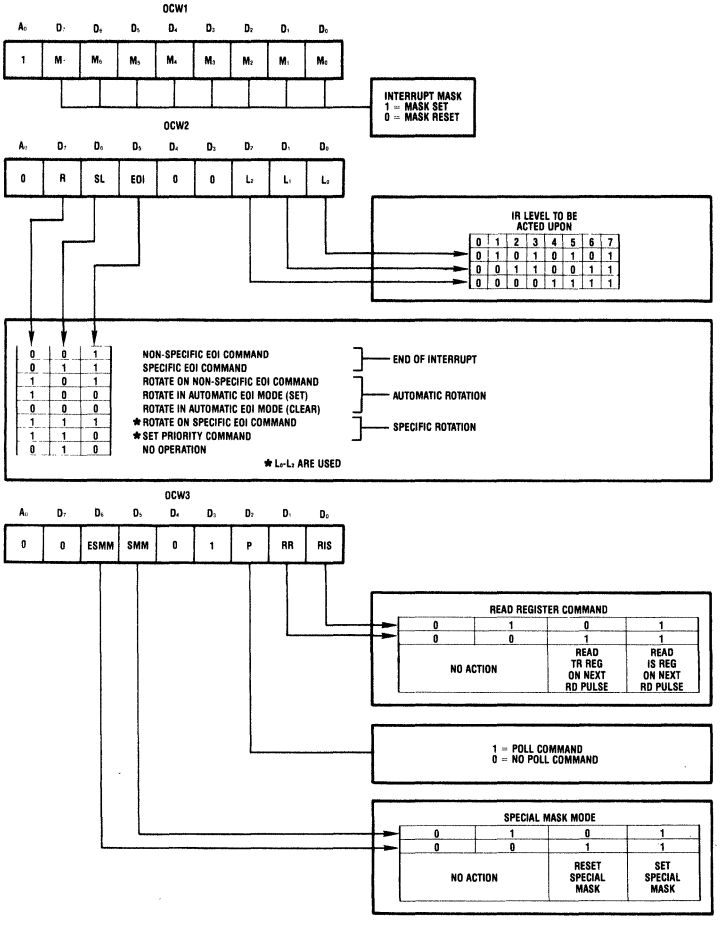
OPERATION CONTROL WORD 1 (OCW1)

OCW1 sets and clears the mask bits in the interrupt Mask Register (IMR). M_7-M_0 represent the eight mask bits. M=1 indicates the channel is masked (inhibited), M=0 indicates the channel is enabled.

OPERATION CONTROL WORD 2 (OCW2)

R, SL, EOI—These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations can be found on the Operation Command Word Format.

L_2, L_1, L_0—These bits determine the interrupt level acted upon when the SL bit is active.



82C59A OPERATION COMMAND WORD FORMAT

OPERATION CONTROL WORD 3 (OCW3)

ESMM – Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When ESMM=0,the SMM bit becomes a "don't care".

SMM – Special Mask Mode. If ESMM=1 and SMM=1,the 82C59A will enter Special Mask Mode. If ESMM=1 and SMM=0,the 82C59A will revert to normal mask mode. When ESMM=0, SMM has no effect.

FULLY NESTED MODE

This mode is entered after initialization unless another mode is programmed. The interrupt requests are ordered in priority from 0 through 7 (0 highest). When an interrupt is acknowledged the highest priority request is determined and its vector placed on the bus. Additionally, a bit of the Interrupt Service register (IS0-7) is set. This bit remains set until the microprocessor issues an End of Interrupt (EOI) command immediately before returning from the service routine, or if AEOI (Automatic End of Interrupt) bit is set, until the trailing edge of the last $\overline{\text{INTA}}$. While the IS bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels will generate an interrupt (which will be acknowledged only if the microprocessor internal interrupt enable flip-flop has been re-enabled through software).

After the initialization sequence, IR0 has the highest priority and IR7 the lowest. Priorities can be changed, as will be explained, in the rotating priority mode or via the set priority command.

END OF INTERRUPT (EOI)

The In Service (IS) bit can be reset either automatically following the trailing edge of the last in sequence $\overline{\text{INTA}}$ pulse (when AEOI bit in ICW1 is set) or by a command word that must be issued to the 82C59A before returning from a service routine (EOI Command). An EOI command must be issued twice if in the Cascade mode, once for the master and once for the corresponding slave.

There are two forms of EOI command: Specific and Non-Specific. When the 82C59A is operated in modes which preserve the fully nested structure, it can determine which IS bit to reset on EOI. When a Non-Specific EOI command is issued the 82C59A will automatically reset the highest IS bit of those that are set, since in the fully nested mode the highest IS level was necessarily the last level acknowledged and serviced. A non-specific EOI can be issued with OCW2 (EOI=1, SL=0, R=0).

When a mode is used which may disturb the fully nested structure, the 82C59A may no longer be able to determine the last level acknowledged. In this case a Specific End of Interrupt must be issued which includes as part of the command the IS level to be reset. A specific EOI can be issued with OCW2 (EOI=1, SL=1, R=0, and L0-L2 is the binary level of the IS bit to be reset).

An IRR bit that is masked by an IMR bit will not be cleared by a non-specific EOI if the 82C59A is in the Special Mask Mode.

AUTOMATIC END OF INTERRUPT (AEOI) MODE

If AEOI=1 in ICW4, then the 82C59A will operate in AEOI mode continuously until reprogrammed by ICW4. In this mode the 82C59A will automatically perform a non-specific EOI operation at the trailing edge of the last interrupt acknowledge pulse (third pulse in 8080/85, second in 80C86). Note that from a system standpoint, this mode should be used only when a nested multi-level interrupt structure is not required within a single 82C59A.

AUTOMATIC ROTATION (Equal Priority Devices)

In some applications there are a number of interrupting devices of equal priority. In this mode a device, after being serviced, receives the lowest priority, so a device requesting an interrupt will have to wait, in the worst case until each of 7 other devices are serviced at most once. For example, if the priority and "in service" status is:

Before Rotate (IR4 the highest priority requiring service)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" STATUS	0	1	0	1	0	0	0	0
PRIORITY STATUS	7 (lowest)	6	5	4	3	2	1	0 (highest)

After Rotate (IR4 was serviced, all other priorities rotated correspondingly)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" STATUS	0	1	0	0	0	0	0	0
PRIORITY STATUS	2 (highest)	1	0	7	6	5	4	3 (lowest)

There are two ways to accomplish Automatic Rotation using OCW2, the Rotation on Non-Specific EOI Command (R=1, SL=0, EOI=1) and the Rotate in Automatic EOI Mode which is set by (R=1, SL=0, EOI=0) and cleared by (R=0, SL=0, EOI=0).

SPECIFIC ROTATION (Specific Priority)

The programmer can change priorities by programming the bottom priority and thus fixing all other priorities; i.e., if IR5 is programmed as the bottom priority device, then IR6 will have the highest one.

The Set Priority command is issued in OCW2 where: R=1, SL=1; L0-L2 is the binary priority level code of the bottom priority device.

Observe that in this mode internal status is updated by software control during OCW2. However, it is independent of the End of Interrupt (EOI) command (also executed by OCW2). Priority changes can be executed during an EOI command by using the Rotate on Specific EOI command in OCW2 (R=1, SL=1, EOI=1 and L0-12=IR level to receive bottom priority).

INTERRUPT MASKS

Each Interrupt Request input can be masked individually by the Interrupt Mask Register (IMR) programmed through OCW1. Each bit in the IMR masks one interrupt channel if it is set (1). Bit 0 masks IR0, Bit 1 masks IR1 and so forth. Masking an IR channel does not affect the other channels operation.

SPECIAL MASK MODE

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The difficulty here is that if an Interrupt Request is acknowledged and an End of Interrupt command did not reset its IS bit (i.e., while executing a service routine), the 82C59A would have inhibited all lower priority requests with no easy way for the routine to enable them.

That is where the Special Mask Mode comes in. In the special Mask Mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level and enables interrupts from all other levels (lower as well as higher) that are not masked.

Thus, any interrupts may be selectively enabled by loading the mask register.

The special Mask Mode is set by OCW3 where: SSMM=1, SMM=1, and cleared where SSMM=1, SMM=0.

POLL COMMAND

In this mode, the INT output is not used or the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting P=1 in OCW3. The 82C59A treats the next $\overline{RD}$ pulse to the 82C59A (i.e. $\overline{RD}$=0, $\overline{CS}$=0) as an interrupt acknowledge, sets the appropriate IS bit if there is a request, and reads the priority level. Interrupt is frozen from $\overline{WR}$ to $\overline{RD}$.

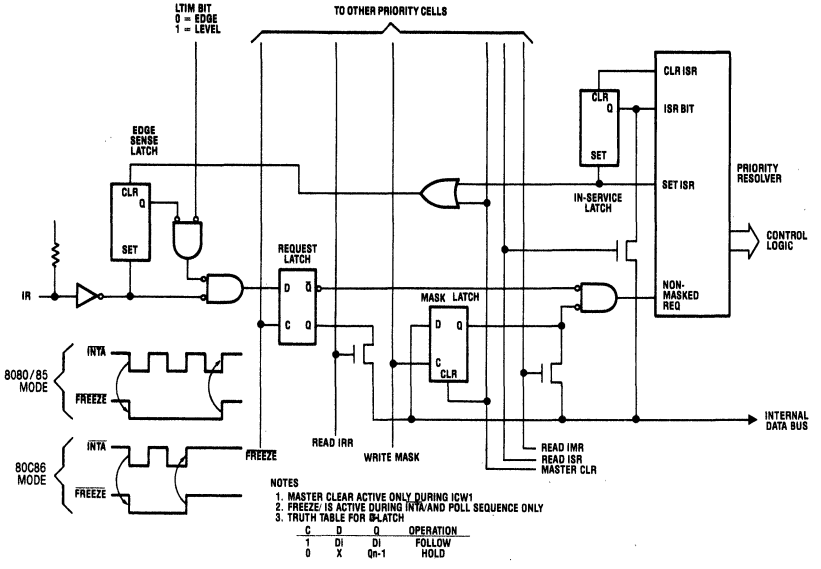
The word enabled onto the data bus during $\overline{RD}$ is:

D7	D6	D5	D4	D3	D2	D1	D0
I	—	—	—	—	W2	W1	W0

W0-W2: Binary code of the highest priority level requesting service.

I: Equal to a "1" if there is an interrupt.

This mode is useful if there is a routine command common to several levels so that the $\overline{INTA}$ sequence is not needed (saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.



PRIORITY CELL – SIMPLIFIED LOGIC DIAGRAM

READING THE 82C59A STATUS

The input status of several internal registers can be read to update the user information on the system. The following registers can be read via OCW3 (IRR and ISR or OCW1 (IMR)).

In-Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt Command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when, prior to the $\overline{RD}$ pulse, a Read Register Command is issued with OCW3 (RR=1, RIS=1).

There is no need to write an OCW3 before every status read operation, as long as the status read corresponds with the previous one; i.e., the 82C59A "remembers" whether the IRR or ISR has been previously selected by the OCW3. This is not true when poll is used. In the poll mode, the 82C59A treats the $\overline{RD}$ following a "poll write" operation as an INTA. After initialization, the 82C59A is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR whenever $\overline{RD}$ is active and A0=1 (OCW1). Polling overrides status read when P=1, RR=1 in OCW3.

EDGE AND LEVEL TRIGGERED MODES

This mode is programmed using bit 3 in ICW1.

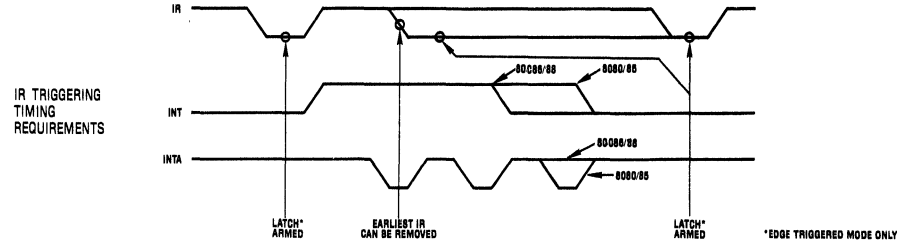
If LTIM = '0', an interrupt request will be recognized by a low to high transition on an IR input. The IR input can remain high without generating another interrupt.

If LTIM = '1', an interrupt request will be recognized by a 'high' level on IR input, and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued or the CPU interrupt is enabled to prevent a second interrupt from occurring.

The priority cell diagram shows a conceptual circuit of the level sensitive and edge sensitive input circuitry of the 82C59A. Be sure to note that the request latch is a transparent D type latch.

In both the edge and level triggered modes the IR inputs must remain high until after the falling edge of the first INTA. If the IR input goes low before this time a DEFAULT IR7 will occur when the CPU acknowledges the interrupt. This can be a useful safeguard for detecting interrupts caused by spurious noise glitches on the IR inputs. To implement this feature the IR7 routine is used for "clean up" simply executing a return instruction, thus ignoring the interrupt. If IR7 is needed for other purposes a default IR7 can still be detected by reading the ISR. A normal IR7 interrupt will set the corresponding ISR bit, a default IR7 won't. If a default IR7 routine occurs during a normal IR7 routine, however, the ISR will remain set. In this case it is necessary to keep track of whether or not the IR7 routine was previously entered. If another IR7 occurs it is a default.

In power sensitive applications, it is advisable to place the 82C59A in the edge-triggered mode. This will minimize the current through the pull-up resistors on the IR pins.



THE SPECIAL FULLY NESTED MODE

This mode will be used in the case of a big system where cascading is used, and the priority has to be conserved within each slave. In this case the fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal nested mode with the following exceptions:

a. When an interrupt request from a certain slave is in service, this slave is not locked out from the master's priority logic and further interrupt requests from higher priority IRs within the slave will be recognized by the master and will initiate interrupts to the processor. (In the normal nested mode a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.)

b. When exiting the Interrupt Service routine the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a non-specific End of Interrupt (EOI) command to the slave and then reading its In-Service register and checking for zero. If it is empty, a non-specified EOI can be sent to the master,too. If not, no EOI should be sent.

BUFFERED MODE

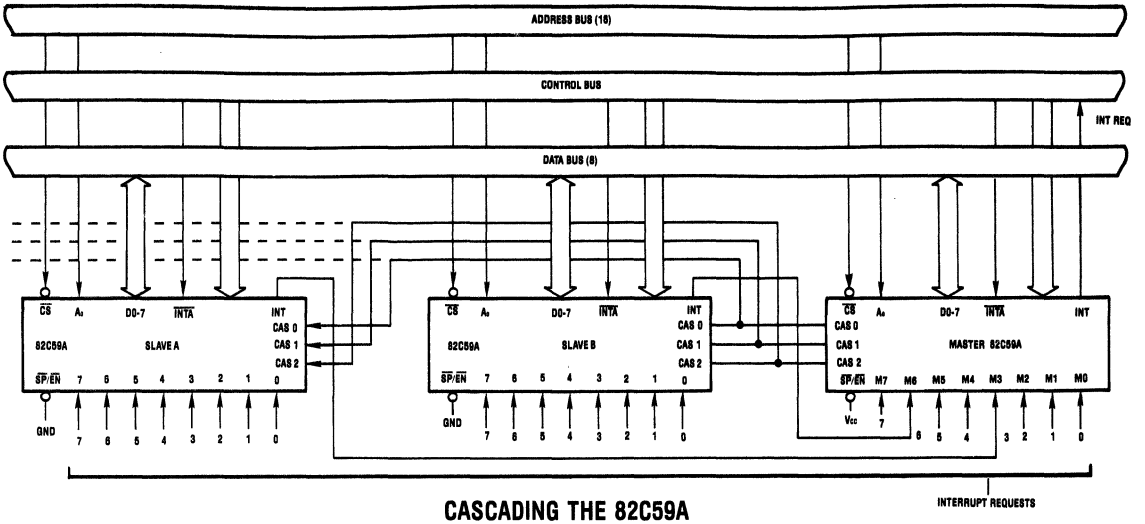
When the 82C59A is used in a large system where bus driving buffers are required on the data bus and the cascading mode is used, there exists the problem of enabling buffers.

The buffered mode will structure the 82C59A to send an enable signal of SP/EN to enable the buffers. In this mode, whenever the 82C59A's data bus outputs are enabled, the SP/EN output becomes active.

This modification forces the use of software programming to determine whether the 82C59A is a master or a slave. Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW4 determines whether it is a master or a slave.

CASCADE MODE

The 82C59A can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.



CASCADING THE 82C59A

The master controls the slaves through the 3 line cascade bus. The cascade bus acts like chip selects to the slaves during the $\overline{\text{INTA}}$ sequence.

In a cascade configuration, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will enable the corresponding slave to release the device routine address during bytes 2 and 3 of INTA. (Byte 2 only for 80C86/ 8088).

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first INTA pulse to the trailing edge of the third pulse. Each 82C59A in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. Chip select decoding is required to activate each 82C59A.

The cascade lines of the Master 82C59A are activated only for slave inputs, non-slave inputs leave the cascade line inactive (low).

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0 VOLTS
Operating Voltage Range	+4V to +7V
Input Voltage Applied	GND − 2.0V to 6.5V
Output Voltage Applied	GND − 0.5V to VCC + 0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Commercial	0°C to +70°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
Maximum Power Dissipation	1 Watt

CAUTION: Stresses above those listed in the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. ELECTRICAL CHARACTERISTICS

VCC = 5.0V ± 10%, T_A = 0°C to +70°C (C82C59A), T_A = −40°C to +85°C (I82C59A);
T_A = −55°C to +125°C (M82C59A)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	LOGICAL ONE INPUT VOLTAGE	2.0 2.2		V V	I82C59A C82C59A M82C59A
VIL	LOGICAL ZERO INPUT VOLTAGE		0.8	V	
VOH	OUTPUT HIGH VOLTAGE	3.0 VCC−0.4		V V	IOH=−2.5 mA IOH=−100 μA
VOL	OUTPUT LOW VOLTAGE		0.4	V	IOL=+2.5 mA
IIL	INPUT LEAKAGE CURRENT	−1.0	+1.0	μA	0V≤VIN≤VCC
IO	OUTPUT LEAKAGE CURRENT	−10.0	+10.0	μA	0V≤VO≤VCC
ICCSB	STANDBY POWER SUPPLY CURRENT		10	μA	VCC=5.5V VIN=VCC or GND OUTPUTS OPEN

CAPACITANCE

T_A=25°C; VCC = GND = 0V; VIN = +5V or GND

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
C_{IN}*	INPUT CAPACITANCE		5	pf	FREQ = 1 MHz Unmeasured pins returned to GND
C_{OUT}*	OUTPUT CAPACITANCE		15	pf	
$C_{I/O}$*	I/O CAPACITANCE		20	pf	

** Guaranteed and sampled, but not 100% tested*

A.C. CHARACTERISTICS

VCC = +5V±10%, GND = 0V: T_A = 0°C to +70°C (C82C59A)
: T_A = −40°C to +85°C (I82C59A)
: T_A = −55°C to +125°C (M82C59A)

Timing Requirements

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TAHRL	A0/$\overline{CS}$ Setup to $\overline{RD}$/$\overline{INTA}$	10		ns	
TRHAX	A0/$\overline{CS}$ Hold after $\overline{RD}$/$\overline{INTA}$	5		ns	
TRLRH	$\overline{RD}$ Pulse Width	160		ns	
TAHWL	A0/$\overline{CS}$ Setup to $\overline{WR}$	0		ns	
TWHAX	A0/$\overline{CS}$ Hold after $\overline{WR}$	0		ns	
TWLWH	$\overline{WR}$ Pulse Width	190		ns	
TDVWH	Data Setup to $\overline{WR}$	160		ns	
TWHDX	Data Hold after $\overline{WR}$	0		ns	
TJLJH	Interrupt Request Width (Low)	100		ns	See Note 1
TCVIAL	Cascade Setup to Second or Third $\overline{INTA}$ (Slave Only)	40		ns	
TRHRL	End of $\overline{RD}$ to next $\overline{RD}$; End of $\overline{INTA}$ to next $\overline{INTA}$ within an $\overline{INTA}$ sequence only	160		ns	
TWHWL	End of $\overline{WR}$ to next $\overline{WR}$	190		ns	
*TCHCL	End of Command to next Command (Not same command type) End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence	400		ns	

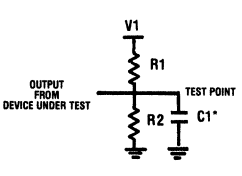
*Worst case timing for TCHCL in an actual microprocessor system is typically much greater than 400 ns (i.e. 8085A = 1.6μs, 8085A-2 = 1μs, 80C86 = 1μs).

Note: This is the low time required to clear the input latch in the edge triggered mode.

Timing Responses

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TRLDV	Data Valid from $\overline{RD}$/$\overline{INTA}$		120	ns	1
TRHDZ	Data Float after $\overline{RD}$/$\overline{INTA}$	10	85	ns	2
TJHIH	Interrupt Output Delay		300	ns	1
TIALCV	Cascade Valid from First $\overline{INTA}$ (Master Only)		360	ns	1
TRLEL	Enable Active from $\overline{RD}$ or $\overline{INTA}$		100	ns	1
TRHEH	Enable inactive from $\overline{RD}$ or $\overline{INTA}$		150	ns	1
TAHDV	Data Valid from Stable Address		200	ns	1
TCVDV	Cascade Valid to Valid Data		200	ns	1

82C59A AC TEST CIRCUITS

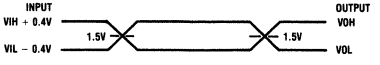


*INCLUDES STRAY AND JIG CAPACITANCE

TEST CONDITION	V1	R1	R2	C1
1	1.7V	523Ω	OPEN	100 pf
2	4.5V	1.8KΩ	1.8KΩ	30 pf

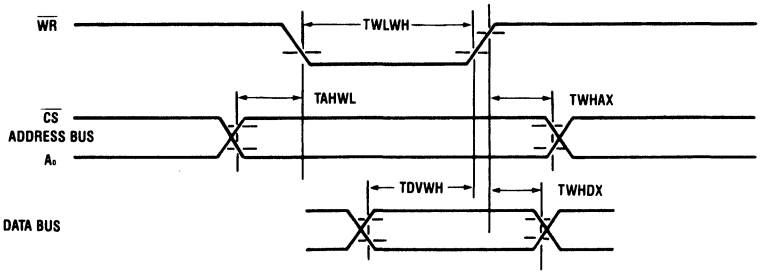
TEST CONDITION DEFINITION TABLE

A.C. TESTING INPUT, OUTPUT WAVEFORM

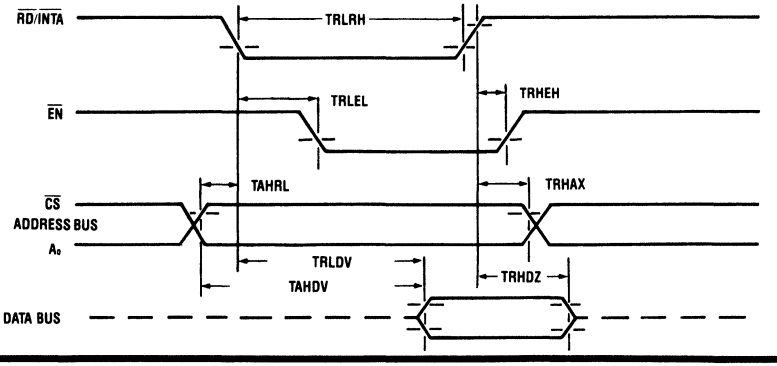


A.C. Testing: All input signals must switch between VIL−0.4V and VIH+0.4V. T_R and T_F must be less than or equal to 15 ns.

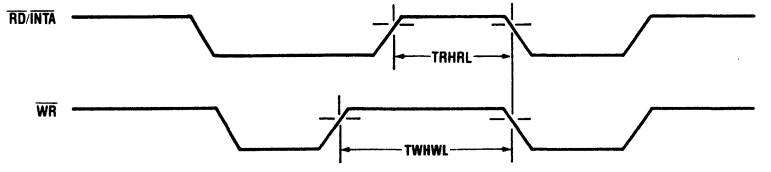
WRITE



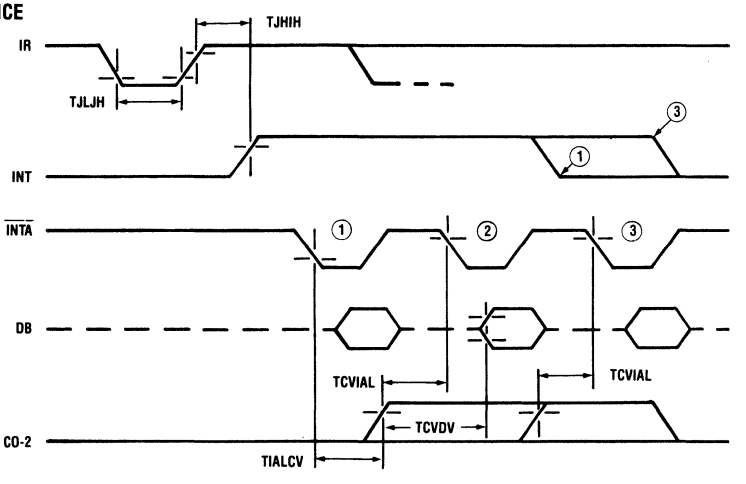
READ/INTA



OTHER TIMING



INTA SEQUENCE



NOTES: Interrupt output must remain HIGH at least until leading edge of first INTA
1. Cycle 1 in 80C86/88 systems, the Data Bus is not active.

HD-6406

CMOS Programmable Asynchronous Communication Interface

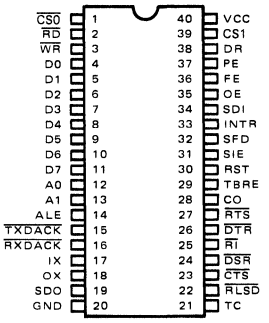
Advance Information

Features

- SINGLE CHIP UART/BRG
- DC TO 16MHz OPERATION
- CRYSTAL OR EXTERNAL CLOCK INPUT
- ON CHIP BAUD RATE GENERATOR ...72 SELECTABLE BAUD RATES
- DMA OR VECTORED INTERRUPT MODE
- MASKABLE INTERRUPTS
- MICROPROCESSOR BUS ORIENTED INTERFACE
- SCALED SAJI IV CMOS PROCESS
- SINGLE 5V POWER SUPPLY
- LOW POWER – 1mA/MHz TYPICAL
- COMPLETE MODEM INTERFACE
- LINE BREAK GENERATION AND DETECTION
- LOOPBACK AND ECHO MODES

Pinout

Top View



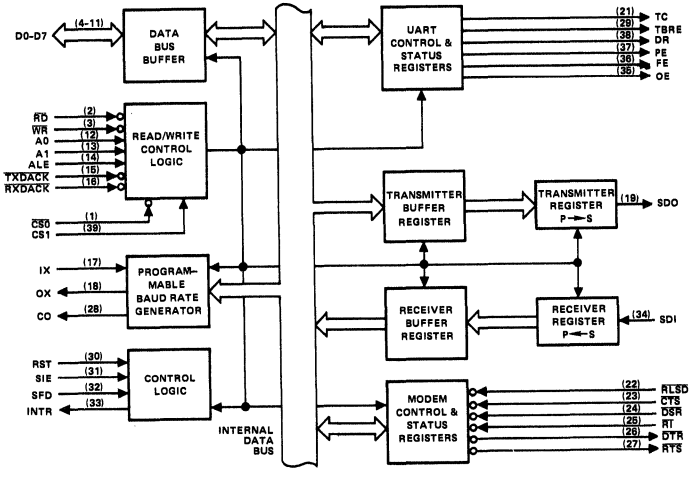
Description

The HD-6406 (PACI) is a high performance programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG) on a single chip. Utilizing Harris Semiconductor's advanced Scaled SAJI IV CMOS process, the PACI will support data rates from DC to 1Mbaud (0-16MHz clock). In addition to all standard UART functions, the PACI includes a complete Data Communications Equipment (DCE) interface.

Provision is made for DMA control of the PACI so that operation at the higher data rates is not hindered by slow microprocessor response times. An ALE control input permits direct interfacing to multiplexed data/address buses common to many microprocessors.

The interrupt structure of the PACI is user-programmable and can be configured to provide a single interrupt for any status change. A subsequent read of an internal status register will identify the source of the interrupt. If desired, the PACI can also provide separate hardware interrupt outputs for the receiver, transmitter and modem status changes. Separate error condition outputs can be used to pinpoint the exact cause of any detected error condition.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow standard IC Handling Procedures.

HARRIS

82C82

CMOS OCTAL LATCHING BUS DRIVER

Advance Information

Features

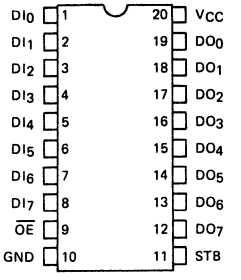
- FULL EIGHT BIT PARALLEL LATCHING BUFFER
- BIPOLAR 8282 COMPATIBLE
- THREE STATE NON-INVERTING OUTPUTS
- PROPAGATION DELAY – 35nsec MAX.
- A.C. CHARACTERISTICS GUARANTEED FOR:
  - ▶ FULL TEMPERATURE RANGE
  - ▶ 10% POWER SUPPLY TOLERANCE
  - ▶ C_L = 300pF
- SINGLE 5V POWER SUPPLY
- POWER SUPPLY CURRENT – 10μA MAX. STANDBY
- OUTPUTS GUARANTEED VALID AT V_{CC} = 2.0 VOLTS
- COMMERCIAL, INDUSTRIAL AND MILITARY TEMPERATURE RANGES
- 20 PIN PACKAGE ON 0.3" CENTERS

Description

The Harris 82C82 is an octal latching buffer manufactured using a self-aligned silicon gate CMOS process. This circuit provides an eight bit parallel latch/buffer in a 20 pin package. The active high strobe (STB) input allows transparent transfer of data and latches data on the negative transition of this signal. The active low output enable ($\overline{OE}$) permits simple interface to state-of-the-art microprocessor systems.

Pinout

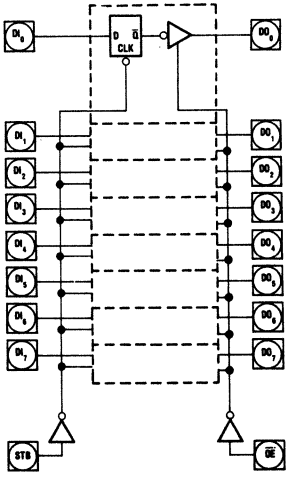
TOP VIEW



3

80C86 FAMILY

Functional Diagram



PIN NAMES

DI_0 - DI_7	Data Input Pins
DO_0 - DO_7	Data Output Pins
STB	Active High Strobe Input
$\overline{OE}$	Active Low Output Enable

Truth Table

STB	$\overline{OE}$	DI	DO
X	H	X	Hi-Z
H	L	L	L
H	L	H	H
↓	L	X	*

H = Logic One Hi-Z = High Impedance
L = Logic Zero ↓ = Negative Transition
X = Don't Care * = Latched to value of last data

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0 VOLTS	Storage Temperature Range	−65°C to +150°C
Operating Voltage Range	+4V to +7V	Operating Temperature Range	
Input Voltage Applied	GND -2.0V to +6.5V	Commercial	0°C to +70°C
Output Voltage Applied	GND -0.5V to VCC +0.5V	Industrial	−40°C to +85°C
		Maximum Power Dissipation	1 Watt

CAUTION: Stresses above those listed in the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. ELECTRICAL CHARACTERISTICS

VCC = 5.0V+/-10%; T_A = 0°C to +70°C (C82C82); T_A = -40°C to +85°C (I82C82)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0		V	See note 1
VIL	Logical Zero Input Voltage		0.8	V	
VOH	Logical One Output Voltage	2.9		V	IOH = −8mA $\overline{OE}$ = LOW
VOL	Logical Zero Output Voltage		0.4	V	IOL = 8mA $\overline{OE}$ = LOW
IIL	Input Leakage Current	−1.0	1.0	μA	0V ≤ VIN ≤ VCC
IO	Output Leakage Current	−10.0	10.0	μA	0V ≤ VO ≤ VCC $\overline{OE}$ = VCC−0.5V
ICC	Power Supply Current		10.0	μA	VIN = VCC or GND VCC = 5.5 V OUTPUTS OPEN
CIN*	Input Capacitance		5	pf	FREQ = 1 MHZ T_A = 25°C VIN = VCC or GND
COUT*	Output Capacitance		15	pf	FREQ = 1 MHZ T_A = 25°C VIN = VCC or GND

*Guaranteed and sampled, but not 100% tested.

NOTE 1: VIH is measured by applying a pulse of magnitude = VIH_{min} to one data input at a time and checking the corresponding device output for a valid logical "1" during valid input high time. Control pins (STB, OE) are tested separately with all device data input pins at VIH_{min}.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0 VOLTS	Storage Temperature Range	−65°C to +150°C
Operating Voltage Range	+4V to +7V	Operating Temperature Range	
Input Voltage Applied	GND -2.0V to +6.5V	Military	−55°C to +125°C
Output Voltage Applied	GND -0.5V to VCC +0.5V	Maximum Power Dissipation	1 Watt

CAUTION: Stresses above those listed in the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. ELECTRICAL CHARACTERISTICS; $V_{CC} = 5.0V \pm 10\%$; $T_A = -55°C$ to $+125°C$

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.2		V	See note 1
VIL	Logical Zero Input Voltage		0.8	V	
VOH	Logical One Output Voltage	2.9		V	IOH = −8mA $\overline{OE}$ = LOW
VOL	Logical Zero Output Voltage		0.4	V	IOL = 8mA $\overline{OE}$ = LOW
IIL	Input Leakage Current	−1.0	1.0	μA	$0V \leq VIN \leq VCC$
IO	Output Leakage Current	−10.0	10.0	μA	$0V \leq VO \leq VCC$ $\overline{OE}$ = VCC−0.5V
ICC	Power Supply Current		10.0	μA	VIN = VCC or GND VCC = 5.5 V OUTPUTS OPEN
CIN*	Input Capacitance		5	pf	FREQ = 1 MHZ $T_A = 25°C$ VIN = VCC or GND
COUT*	Output Capacitance		15	pf	FREQ = 1 MHZ $T_A = 25°C$ VIN = VCC or GND

*Guaranteed and sampled, but not 100% tested.

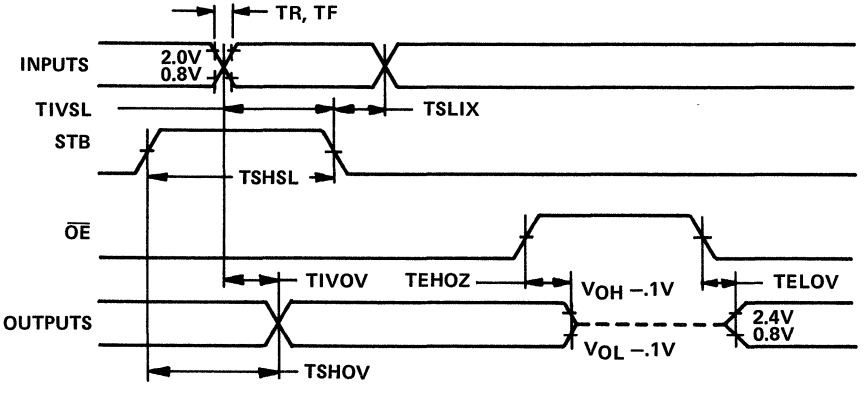
NOTE 1: VIH is measured by applying a pulse of magnitude = VIH_{min} to one data input at a time and checking the corresponding device output for a valid logical "1" during valid input high time. Control pins (STB, OE) are tested separately with all device data input pins at VIH_{min}.

A.C. ELECTRICAL CHARACTERISTICS; VCC = 5.0V ±10%; T_A = Commercial, Industrial or Military
C_L = 300 pf*, FREQ = 1 MHZ

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TIVOV	Propagation Delay Input to Output		35	ns	see notes 1, 2
TSHOV	Propagation Delay STB to Output		55	ns	see notes 1, 2
TEHOZ	Output Disable Time		35	ns	see notes 1, 2
TELOV	Output Enable Time		50	ns	see notes 1, 2
TIVSL	Input to STB Set Up Time	0		ns	see notes 1, 2
TSLIX	Input to STB Hold Time	25		ns	see notes 1, 2
TSHSL	STB High Time	25		ns	see notes 1, 2
TR, TF	Input Rise/Fall Times		20	ns	see notes 1, 2

* Output load capacitance is rated at 300 pf for ceramic and plastic packages.

NOTES: 1. All A.C. parameters tested as per test circuits and definitions in Figures 1-4.
2. Input test signals must switch between VIL−0.4V and VIH+0.4V.
Input rise and fall times must be $\leq$ 20 nsec.



All timing measurements are made at 1.5V unless otherwise noted.

Figure 1
82C82 TIMING RELATIONSHIPS

A.C. TEST CIRCUIT SPECIFICATIONS

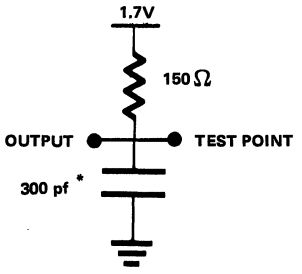


Figure 2
TIVOV, TSHOV, TELOV
Load Circuit

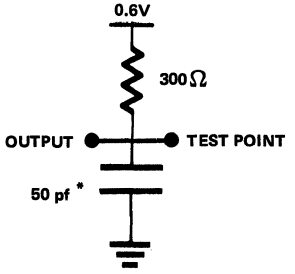


Figure 3
TEHOZ
OUTPUT HIGH DISABLE
Load Circuit

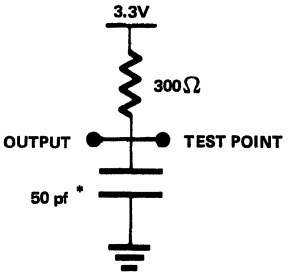


Figure 4
TEHOZ
OUTPUT LOW DISABLE
Load Circuit

*includes jig and stray capacitance

DECOUPLING CAPACITORS

The transient current required to charge and discharge the 300 pf load capacitance specified in the 82C82 data sheet is determined by

$$I = C_L \left(dv/dt\right)$$

Assuming that all outputs change state at the same time and that dv/dt is constant;

$$I = C_L \frac{(VCC \times 80\%)}{t_R/t_F}$$

where t_R = 20 ns, VCC = 5.0 volts, C_L = 300 pf on each of eight outputs.

$$I = (8 \times 300 \times 10^{-12}) \times (5.0v \times 0.8)/(20 \times 10^{-9})$$

$$= 480 \text{ mA}$$

This current spike may cause a large negative voltage spike on VCC, which could cause improper operation of the device. To filter out this noise, it is recommended that a 0.1 uF ceramic disc decoupling capacitor be placed between VCC and GND at each device, with placement being as near to the device as possible.

HARRIS

82C84A

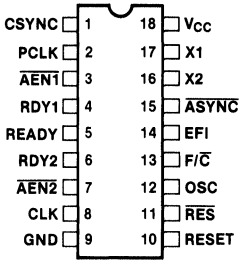
CMOS Clock Generator Driver

Advance Information

Features

- GENERATES THE SYSTEM CLOCK FOR CMOS OR NMOS MICROPROCESSORS
- UP TO 25 MHZ OPERATION
- USES A PARALLEL MODE CRYSTAL CIRCUIT OR EXTERNAL FREQUENCY SOURCE
- PROVIDES READY SYNCHRONIZATION
- GENERATES SYSTEM RESET OUTPUT FROM SCHMITT TRIGGER INPUT
- CAPABLE OF CLOCK SYNCHRONIZATION WITH OTHER 82C84As
- TTL COMPATIBLE INPUTS/OUTPUTS
- VERY LOW POWER CONSUMPTION
- 18 PIN PACKAGE
- SINGLE +5V POWER SUPPLY
- COMMERCIAL, INDUSTRIAL AND MILITARY TEMPERATURE RANGES AVAILABLE

Pinout



Description

The Harris 82C84A is a high performance CMOS clock generator-driver which is designed to service the requirements of both CMOS and NMOS microprocessors such as the 80C86, 80C88, 8086 and the 8088. The chip contains a crystal controlled oscillator, a divide-by-three counter and complete "Ready" synchronization and reset logic.

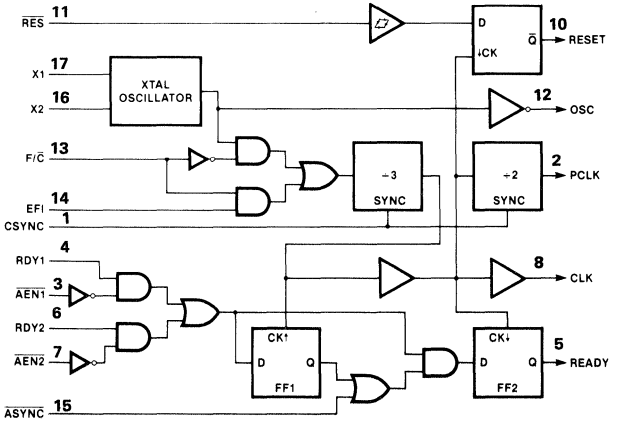
Static CMOS circuit design permits operation with an external frequency source from DC to 25MHz. Crystal controlled operation to 25MHz is guaranteed with the use of a parallel, fundamental mode crystal and two small load capacitors.

All inputs (except X1, X2 and $\overline{RES}$) are TTL compatible with a V_{IH} of 2.0 volts over the industrial temperature and voltage ranges.

Power consumption is a fraction of that of the equivalent bipolar circuits. This speed-power characteristic of CMOS permits the designer to custom tailor his system design with respect to power and/or speed requirements.

CONTROL PIN	LOGICAL 1	LOGICAL 0
F/$\overline{C}$	External Clock	Crystal Drive
$\overline{RES}$	Normal	Reset
RDY1 RDY2	Bus Ready	Bus not ready
$\overline{AEN1}$ $\overline{AEN2}$	Address Disabled	Address Enabled
ASYNC	2 Stage Ready Synchronization	1 Stage Ready Synchronization

Block Diagram



Pin	I/O	Definition
$\overline{AEN1}$, $\overline{AEN2}$	I	ADDRESS ENABLE: $\overline{AEN}$ is an active LOW signal. $\overline{AEN}$ serves to qualify its respective Bus Ready Signal (RDY1 or RDY2). $\overline{AEN1}$ validates RDY1 while $\overline{AEN2}$ validates RDY2. Two AEN signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non Multi-Master configurations, the $\overline{AEN}$ signal inputs are tied true (LOW).
RDY 1, RDY2	I	BUS READY (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by AEN1 while RDY2 is qualified by AEN2.
$\overline{ASYNC}$	I	READY SYNCHRONIZATION SELECT: $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is low, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open or HIGH a single stage of READY synchronization is provided.
READY	O	READY: READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
X1, X2	I	CRYSTAL IN: X1 and X2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency.
F/$\overline{C}$	I	FREQUENCY/CRYSTAL SELECT: F/$\overline{C}$ is a strapping option. When strapped LOW, F/$\overline{C}$ permits the processor's clock to be generated by the crystal. When F/$\overline{C}$ is strapped HIGH, CLK is generated from the EFI input.
EFI	I	EXTERNAL FREQUENCY IN: When F/$\overline{C}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output.

Pin	I/O	Definition
CLK	O	PROCESSOR CLOCK: CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus. CLK has an output frequency which is 1/3 of the crystal or EFI input frequency and a 1/3 duty cycle.
PCLK	O	PERIPHERAL CLOCK: PCLK is a peripheral clock signal whose output frequency is 1/2 that of CLK and has a 50% duty cycle.
OSC	O	OSCILLATOR OUTPUT: OSC is the output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
$\overline{RES}$	I	RESET IN: $\overline{RES}$ is an active LOW signal which is used generate RESET.The 82C84A provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.
RESET	O	RESET: RESET is an active HIGH signal which is used to reset the 80C86 family processors. Its timing characteristics are determined by $\overline{RES}$.
CSYNC	I	CLOCK SYNCHRONIZATION: CSYNC is an active HIGH signal which allows multiple 82C84As to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hardwired to ground.
GND		Ground
V_{CC}		+5V supply

TABLE 1. PIN DEFINITIONS

FUNCTIONAL DESCRIPTION

Oscillator

The oscillator circuit of the 82C84A is designed primarily for use with an external parallel resonant, fundamental mode crystal from which the basic operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input crystal connections. For the most stable operation of the oscillator (OSC) output circuit, two capacitors (C1 = C2) as shown in the waveform figures are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

Capacitors C1, C2 are chosen such that their combined capacitance:

$$CT = \frac{C1 \cdot C2}{C1 + C2} \text{ (Including stray capacitance)}$$

matches the load capacitance as specified by the crystal manufacturer. This insures operation within the frequency tolerance specified by the crystal manufacturer.

Clock Generator

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as

another 82C84A clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the 82C84A. This is accomplished with two flip-flops. (See Figure 3.) The counter output is a 33% duty cycle clock at one-third the input frequency.

* The F/C input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the ÷3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

Clock Outputs

The CLK output is a 33% duty cycle clock driver designed to drive the 80C86, 80C88 processors directly. PCLK is a peripheral clock signal whose output frequency is 1/2 that of CLK. PCLK has a 50% duty cycle.

Reset Logic

The reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the 82C84A. Waveforms for clocks and reset signals are illustrated in Figure 4.

READY Synchronization

Two READY inputs (RDY1, RDY2) are provided to accommodate two system busses. Each input has a qualifier ($\overline{AEN1}$ and $\overline{AEN2}$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals. If a Multi-Master system is not being used the $\overline{AEN}$ pin should be tied LOW.

Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY setup and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

The $\overline{ASYNC}$ input defines two modes of READY synchronization operation.

When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs will first be synchronized to flip-flop one at the rising edge of CLK (requiring a setup time t_{R1VCH}) and then synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go active (HIGH). Negative-going asynchronous READY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the READY output will go inactive.This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing, t_{R1VCL}, on each bus cycle. (Refer to Figure 5.)

When $\overline{ASYNC}$ is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time. (Refer to Figure 6.)

$\overline{ASYNC}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

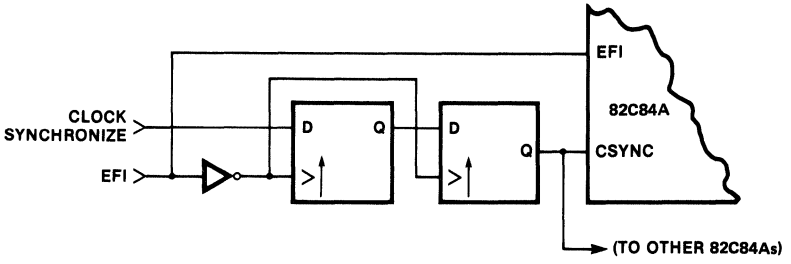


FIGURE 3. CSYNC SYNCHRONIZATION

***Note:** If EFI input is used, then crystal input X1 must be tied to VCC or GND and X2 should be left open. If the crystal inputs are used, then EFI should be tied to VCC or GND.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0 Volts	Operating Temperature Range	
Operating Voltage Range	+4V to +7V	Commercial	0°C to +70°C
Input Voltage Applied	GND-2.0V to 6.5V	Industrial	-40°C to +85°C
Output Voltage Applied	GND-0.5V to VCC + 0.5V	Military	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C	Maximum Power Dissipation	1 Watt

CAUTION: Stresses above those listed in the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D. C. ELECTRICAL CHARACTERISTICS

VCC = 5.0V ± 10%; T_A = 0°C to +70°C (C82C84A); T_A = -40°C to +85°C (I82C84A); T_A = -55°C to +125°C (M82C84A)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0 2.2		V V	I82C84A M82C84A
VIL	Logical Zero Input Voltage		0.8	V	
V_{T+}	Reset Input High Voltage	0.6 VCC	VCC -0.8	V	
$V_{T+} - V_{T-}$	Reset Input Hysteresis	0.2 VCC			
VOH	Logical One Output Voltage	VCC-0.4		V	IOH=-4.0mA for CLK output IOH = -2.5mA for all others
VOL	Logical Zero Output Voltage		0.4	V	IOL = +4.0 mA for CLK output IOL = +2.5 mA for all others
IIL	Input Leakage Current	-1.0	1.0	μA	0V<VIN<VCC except $\overline{\text{ASYNC}}$, X1-see note 1
ICC	Power Supply Current		40	mA	Crystal Frequency = 25MHz Outputs Open

NOTES:
1. ASYNC pin includes an internal 17.5KΩ nominal pull-up resistor. For $\overline{\text{ASYNC}}$ input at GND, $\overline{\text{ASYNC}}$ input leakage current = 130μA nominal.
   X1 - crystal feedback input.

CAPACITANCE

T_A = 25°C. VCC = GND = 0V; VIN = +5V or GND

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
C_{IN}*	Input Capacitance		5	pf	Freq. = 1MHz

*Guaranteed and sampled, but not 100% tested

T_A = 0°C to +70°C, V_{CC} = 5V ±10% Commercial Grade – C82C84A

A. C. CHARACTERISTICS

T_A = -40°C to +85°C, V_{CC} = 5V ±10% Industrial Grade –I82C84A

TIMING REQUIREMENTS

T_A = -55°C to +125°C, VCC = 5V ±10% Military Grade –M82C84A

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_{EHEL}	External Frequency HIGH Time	13		ns	90% - 90% V_{IN}
t_{ELEH}	External Frequency LOW Time	13		ns	10%-10% V_{IN}
t_{ELEL}	EFI Period	36		ns	
	XTAL Frequency	2.4	25	MHz	
t_{R1VCL}	RDY1, RDY2 Active Setup to CLK	35		ns	ASYNC = HIGH
t_{R1VCH}	RDY1, RD2 Active Setup to CLK	35		ns	ASYNC = LOW
t_{R1VCL}	RDY1, RDY2 Inactive Setup to CLK	35		ns	
t_{CLR1X}	RDY1, RDY2 Hold to CLK	0		ns	
t_{AYVCL}	ASYNC Setup to CLK	50		ns	
t_{CLAYX}	ASYNC Hold to CLK	0		ns	
t_{A1VR1V}	AEN1, AEN2 Setup to RDY1, RDY2	15		ns	
t_{CLA1X}	AEN1, AEN2 Hold to CLK	0		ns	
t_{YHEH}	CSYNC Setup to EFI	20		ns	
t_{EHYL}	CSYNC Hold to EFI	20		ns	
t_{YHYL}	CSYNC Width	$2 \cdot t_{ELEL}$		ns	
t_{I1HCL}	RES Setup to CLK	65		ns	(Note 2)
t_{CLI1H}	RES Hold to CLK	20		ns	(Note 2)

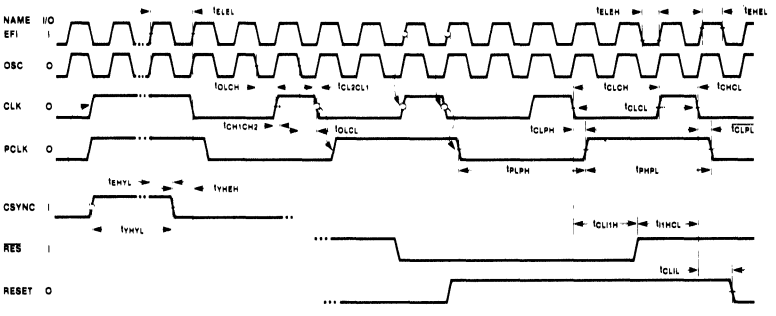
A. C. CHARACTERISTICS (cont.)

TIMING RESPONSES

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_{CLCL}	CLK Cycle Period	125		ns	
t_{CHCL}	CLK HIGH Time	(1/3 t_{CLCL}) +2.0		ns	Fig. 7 & Fig. 8
t_{CLCH}	CLK LOW Time	(2/3 t_{CLCL}) -15.0		ns	Fig. 7 & Fig. 8
t_{CH1CH2} t_{CL2CL1}	CLK Rise or Fall Time		10	ns	1.0V to 3.5V
t_{PHPL}	PCLK HIGH Time	t_{CLCL}-20		ns	
t_{PLPH}	PCLK LOW Time	t_{CLCL}-20		ns	
t_{RYLCL}	Ready Inactive to CLK (See note 4)	-8		ns	Fig. 8 & Fig. 10
t_{RYHCH}	Ready Active to CLK (See note 3)	(2/3 t_{CLCL}) -15.0		ns	Fig. 9 & Fig. 10
t_{CLIL}	CLK to Reset Delay		40	ns	
t_{CLPH}	CLK to PCLK HIGH Delay		22	ns	
t_{CLPL}	CLK to PCLK LOW Delay		22	ns	
t_{OLCH}	OSC to CLK HIGH Delay	-5	22	ns	
t_{OLCL}	OSC to CLK LOW Delay	2	35	ns	

NOTES:
1. Output signals switch between VOH and VOL unless otherwise specified.
2. Setup and hold necessary only to guarantee recognition at next clock.
3. Applies only to T3 TW states.
4. Applies only to T2 states.
5. All timing delays are measured at 1.5 volts unless otherwise noted.
6. Input signals must switch between VIL max -.4 VOH and VIH min +.4 volts in 15ns unless otherwise specified.

+Figure 11 illustrates test load measurement condition.



NOTE: ALL TIMING MEASUREMENTS ARE MADE AT 1.5 VOLTS, UNLESS OTHERWISE NOTED.

FIGURE 4. WAVEFORMS FOR CLOCKS AND RESET SIGNALS

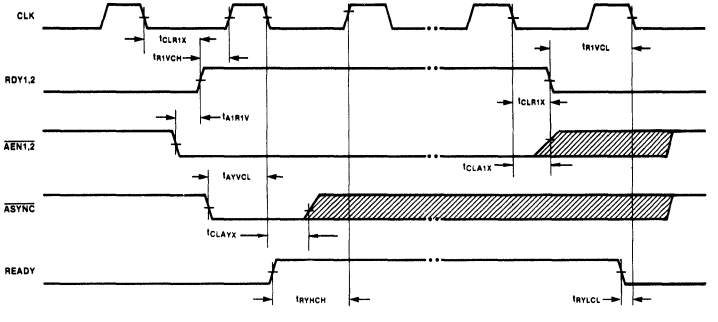


FIGURE 5. WAVEFORMS FOR READY SIGNALS (FOR ASYNCHRONOUS DEVICES)

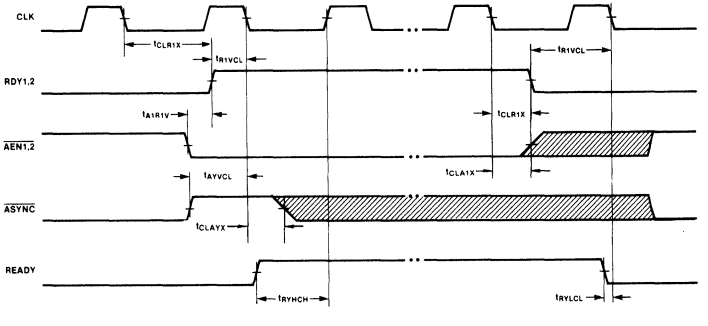


FIGURE 6. WAVEFORMS FOR READY SIGNALS (FOR SYNCHRONOUS DEVICES)

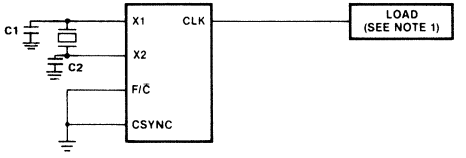


FIGURE 7. CLOCK HIGH AND LOW TIME (USING X1, X2)

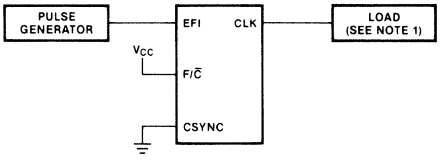


FIGURE 8. CLOCK HIGH AND LOW TIME (USING EFI)

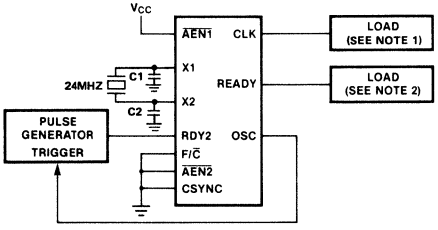


FIGURE 9. READY TO CLOCK (USING X1, X2)

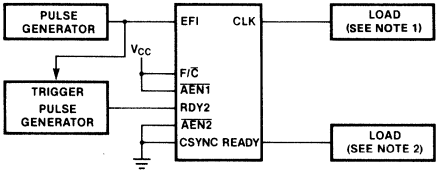


FIGURE 10. READY TO CLOCK (USING EFI)

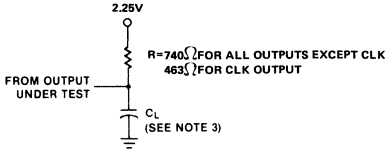


FIGURE 11. TEST LOAD MEASUREMENT CONDITIONS

NOTES:
1. C_L = 100pF
2. C_L = 30pF
3. C_L INCLUDES PROBE AND JIG CAPACITANCE

PARAMETER	TYPICAL CRYSTAL SPEC
Frequency	2.4-25MHz, Fundamental, "AT" cut
Type of Operation	Parallel
Unwanted Modes	-6db (Min)
Load Capacitance	18-32pf

TABLE 2. CRYSTAL SPECIFICATIONS

See Harris Publication TB-47 for recommended crystal specifications.

82C88

CMOS BUS CONTROLLER

Features

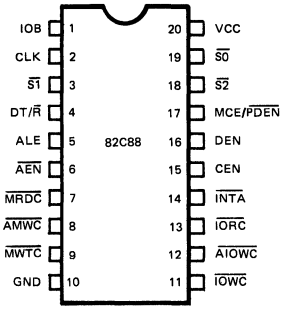
- PIN COMPATIBLE WITH BIPOLAR 8288
- PROVIDES ADVANCED COMMANDS FOR MULTI-MASTER BUSSES
- 3-STATE COMMAND OUTPUTS
- BIPOLAR DRIVE CAPABILITY
- FULLY TTL COMPATIBLE
- SCALED SAJI IV CMOS PROCESS
- SINGLE 5V POWER SUPPLY
- LOW POWER OPERATION
  - ▶ ICCSB – 10μA
  - ▶ ICCOP – 1mA/MHz
- INDUSTRIAL, MILITARY, AND COMMERCIAL TEMPERATURE RANGES

Description

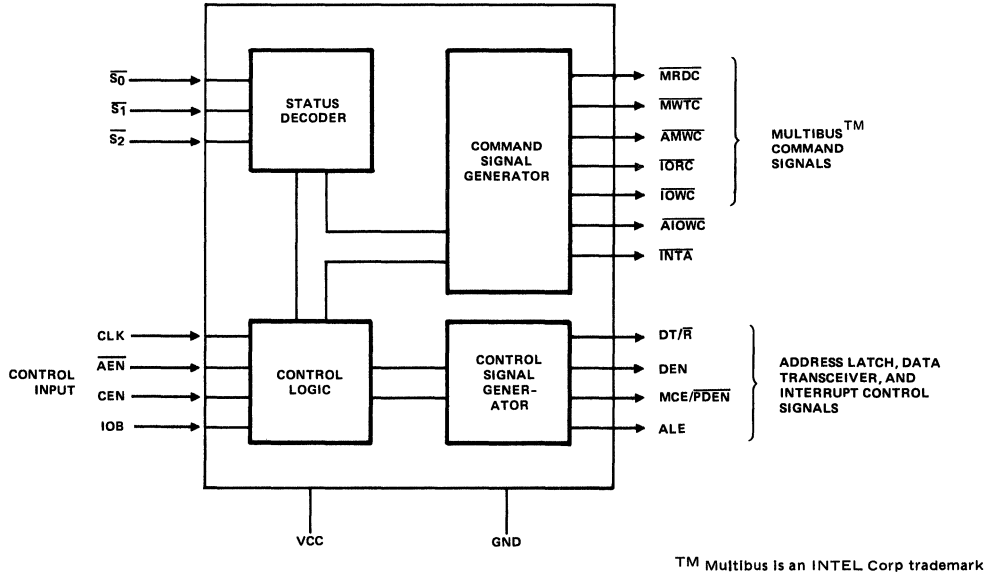
The Harris 82C88 is a high performance CMOS Bus Controller manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C88 provides the control and command timing signals for 80C86 and 8086/88 systems. The high output drive capability of the 82C88 eliminates the need for additional bus drivers. High speed and industry standard configuration make the 82C88 compatible with microprocessors such as the 80C86, 8086, 8088, 8089, 80186, and 80188.

Static CMOS circuit design insures low operating power. Harris's advanced SAJI process results in performance equal to or greater than existing equivalent products at a significant power savings.

Pinout



Functional Diagram



™ Multibus is an INTEL Corp trademark

Pin Description

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
V_{CC}	20		+5V power supply
GND	10		Ground
$\overline{S_0}, \overline{S_1}$ $\overline{S_2}$	19, 3 18	I	Status Input pins: These pins are the input pins from the 80C86, 8086/88/8089 processors. The 82C88 decodes these inputs to generate command and control signals at the appropriate time. When Status pins are not in use (passive), command outputs are held HIGH (See Table 1.)
CLK	2	I	Clock: This is a CMOS compatible input which receives a clock signal from the 82C84A clock generator and serves to establish when command/control signals are generated.
ALE	5	O	Address Latch Enable: This signal serves to strobe an address into the address latches. This signal is active HIGH and latching occurs on the falling (HIGH to LOW) transition. ALE is intended for use with transparent D type latches, such as the 82C82.
DEN	16	O	Data Enable: This signal serves to enable data transceivers onto either the local or system data bus. This signal is active HIGH.
DT/$\overline{R}$	4	O	Data Transmit/Receive: This signal establishes the direction of data flow through the transceivers. A HIGH on this line indicates Transmit (write to I/O or memory) and a LOW indicates Receive (Read).
$\overline{AEN}$	6	I	Address Enable: $\overline{AEN}$ enables command outputs of the 82C88 Bus Controller a minimum of 110ns (250ns maximum) after it becomes active (LOW). $\overline{AEN}$ going inactive immediately 3-states the command output drivers. $\overline{AEN}$ does not affect the I/O command lines if the 82C88 is in the I/O Bus mode (IOB tied HIGH).
CEN	15	I	Command Enable: When this signal LOW all 82C88 command outputs and the DEN and $\overline{PDEN}$ control outputs are forced to their Inactive state. When this signal is HIGH, these same outputs are enabled.
IOB	1	I	Input/Output Bus Mode: When the IOB is strapped HIGH the 82C88 functions in the I/O Bus mode. When it is strapped LOW, the 82C88 functions in the System Bus mode (See I/O Bus and System Bus sections).
$\overline{AIOWC}$	12	O	Advanced I/O Write Command: The $\overline{AIOWC}$ issues an I/O Write Command earlier in the machine cycle to give I/O devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AIOWC}$ is active LOW.
$\overline{IOWC}$	11	O	I/O Write Command: This command line instructs an I/O device to read the data on the data bus. The signal is active LOW.
$\overline{IORC}$	13	O	I/O Read Command: This command line instructs an I/O device to drive its data onto the data bus. This signal is active LOW.
$\overline{AMWC}$	8	O	Advanced Memory Write Command: The $\overline{AMWC}$ issues a memory write command earlier in the machine cycle to give memory devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AMWC}$ is active LOW.
$\overline{MWTC}$	9	O	Memory Write Command: This command line instructs the memory to record the data present on the data bus. This signal is active LOW.
$\overline{MRDC}$	7	O	Memory Read Command: This command line instructs the memory to drive its data onto the data bus. $\overline{MRDC}$ is active LOW.
$\overline{INTA}$	14	O	Interrupt Acknowledge: This command line tells an interrupting device that its interrupt has been acknowledged and that it should drive vectoring information onto the data bus. This signal is active LOW.
MCE/$\overline{PDEN}$	17	O	This is a dual function pin. MCE (IOB is tied LOW): Master Cascade Enable occurs during an interrupt sequence and serves to read a Cascade Address from a master 82C59A Priority Interrupt Controller onto the data bus. The MCE signal is active HIGH. $\overline{PDEN}$ (IOB is tied HIGH): Peripheral Data Enable enables the data bus transceiver for the I/O bus that DEN performs for the system bus. $\overline{PDEN}$ is active LOW.

Functional Description

Command and Control Logic

The command logic decodes the three 80C86, 8086, 8088 or 8089 status lines ($\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$) to determine what command is to be issued (see Table 1).

Table 1. Command Decode Definition

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Processor State	82C88 Command
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

I/O Bus Mode

The 82C88 is in the I/O Bus mode if the IOB pin is strapped HIGH. In the I/O Bus mode, all I/O command lines ($\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$) are always enabled (i.e., not dependent on $\overline{AEN}$). When an I/O command is initiated by the processor, the 82C88 immediately activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ to control the I/O bus transceiver. The I/O command lines should not be used to control the system bus in this configuration because no arbitration is present. This mode allows one 82C88 Bus Controller to handle two external busses. No waiting is involved when the CPU wants to gain access to the I/O bus. Normal memory access requires a "Bus Ready" signal ($\overline{AEN}$ LOW) before it will proceed. It is advantageous to use the IOB mode if I/O or peripherals dedicated to one processor exist in a multi-processor system.

System Bus Mode

The 82C88 is in the System Bus mode if the IOB pin is strapped LOW. In this mode, no command is issued until a specified time period after the $\overline{AEN}$ line is activated (LOW). This mode assumes bus arbitration logic will inform the bus controller (on the $\overline{AEN}$ line) when the bus is free for use. Both memory and I/O commands wait for bus arbitration. This mode is used when only one bus exists. Here, both I/O and memory are shared by more than one processor.

Command Outputs

The advanced write commands are made available to initiate write procedures early in the machine cycle. This signal can be used to prevent the processor from entering an unnecessary wait state.

The command outputs are:

$\overline{MRDC}$ - Memory Read Command
$\overline{MWTC}$ - Memory Write Command
$\overline{IORC}$ - I/O Read Command
$\overline{IOWC}$ - I/O Write Command
$\overline{AMWC}$ - Advanced Memory Write Command
$\overline{AIOWC}$ - Advanced I/O Write Command
$\overline{INTA}$ - Interrupt Acknowledge

$\overline{INTA}$ (Interrupt Acknowledge) acts as an I/O read during an interrupt cycle. Its purpose is to inform an interrupting device that its interrupt is being acknowledged and that it should place vectoring information onto the data bus.

Control Outputs

The control outputs of the 82C88 are Data Enable (DEN), Data Transmit/Receive (DT/$\overline{R}$) and Master Cascade Enable/Peripheral Data Enable (MCE/$\overline{PDEN}$). The DEN signal determines when the external bus should be enabled onto the local bus and the DT/$\overline{R}$ determines the direction of data transfer. These two signals usually go to the chip select and direction pins of a transceiver.

The MCE/$\overline{PDEN}$ pin changes function with the two modes of the 82C88. When the 82C88 is in the IOB mode (IOB HIGH), the $\overline{PDEN}$ signal serves as a dedicated data enable signal for the I/O or Peripheral System bus.

Interrupt Acknowledge and MCE

The MCE signal is used during an interrupt acknowledge cycle if the 82C88 is in the System Bus mode (IOB LOW). During any interrupt sequence, there are two interrupt acknowledge cycles that occur back to back. During the first interrupt cycle no data or address transfers take place. Logic should be provided to mask off MCE during this cycle. Just before the second cycle begins the MCE signal gates a master Priority Interrupt Controller's (PIC) cascade address onto the processor's local bus where ALE (Address Latch Enable) strobes it into the address latches. On the leading edge of the second interrupt cycle, the addressed slave PIC gates an interrupt vector onto the system data bus where it is read by the processor.

If the system contains only one PIC, the MCE signal is not used. In this case, the second Interrupt Acknowledge signal gates the interrupt vector onto the processor bus.

Address Latch Enable and Halt

Address Latch Enable (ALE) occurs during each machine cycle and serves to strobe the current address into the 82C82 address latches. ALE also serves to strobe the status ($\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$) into a latch for halt state decoding.

Command Enable

The Command Enable (CEN) input acts as a command qualifier for the 82C88. If the CEN pin is high, the 82C88 functions normally. If the CEN pin is pulled LOW, all command lines are held in their inactive state (not 3-state). This feature can be used to implement memory partitioning and to eliminate address conflicts between system bus devices and resident bus devices.

Specifications

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0 Volts	Operating Temperature Range	
Operating Voltage Range	+4V to +7V	Commercial	0°C to +70°C
Input Voltage Applied	GND -2.0V to +6.5V	Industrial	-40°C to +85°C
Output Voltage Applied	GND -0.5V to VCC +0.5V	Military	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C	Maximum Power Dissipation	1 Watt

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.

D. C. ELECTRICAL CHARACTERISTICS

VCC = 5.0V ±10%; T_A = 0°C to +70°C (C82C88); T_A = -40°C to +85°C (I82C88); T_A = -55°C to +125°C (M82C88)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0 2.2		V V	I82C88 M82C88
VIL	Logical Zero Input Voltage		0.8	V	
VIHC	CLK Logical One Input Voltage	0.7 VCC		V	
VILC	CLK Logical Zero Input Voltage		0.2VCC	V	
VOH	Output High Voltage Command Outputs	3.0 VCC -0.4		V V	IOH = -8.0mA IOH = -2.5mA
	Output High Voltage Control Outputs	3.0 VCC -0.4		V V	IOH = -4.0mA IOH = -2.5mA
VOL	Output Low Voltage Command Outputs		0.5	V	IOL = +20.0mA
	Output Low Voltage Control Outputs		0.4	V	IOL = +8.0mA
IIL	Input Leakage Current	-1.0	1.0	μA	$0V \leq VIN \leq VCC$ except $\overline{S_0}, \overline{S_1}, \overline{S_2}$
IBHH	Input Leakage Current-Status Bus	-50	-300	μA	VIN = 2.0V $\overline{S_0}, \overline{S_1}, \overline{S_2}$ (see Note 1)
IO	Output Leakage Current	-10.0	10.0	μA	$0V \leq VO \leq VCC$
ICCSB	Standby Power Supply		10	μA	VCC = 5.5V VIN = VCC or GND Outputs Open
ICCOP	Operating Power Supply Current		1	mA/MHz	VCC = 5.5V Outputs Open

CAPACITANCE

T_A = 25°C; VCC = GND = OV; VIN = +5V or GND

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
C_{IN}*	Input Capacitance		5	pf	FREQ = 1MHz Unmeasured pins returned to GND
C_{OUT}*	Output Capacitance		15	pf	

*Guaranteed and sampled, but not 100% tested

Note 1: IBHH should be measured after raising the VIN on $\overline{S_0}, \overline{S_1}, \overline{S_2}$ to VCC and then lowering to 2.0V.

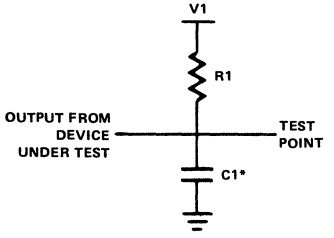
A. C. CHARACTERISTICS

VCC = +5V ±10%, GND = 0V: TA = 0°C to 70°C (C82C88)
TA = -40°C to +85°C (I82C88)
TA = -55°C to +125°C (M82C88)

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
TIMING REQUIREMENTS					
TCLCL	CLK Cycle Period	125		ns	
TCLCH	CLK Low Time	66		ns	
TCHCL	CLK High Time	40		ns	
TSVCH	Status Active Setup Time	35		ns	
TCHSV	Status Active Hold Time	10		ns	
TSHCL	Status Inactive Setup Time	35		ns	
TCLSH	Status Inactive Hold Time	10		ns	
TIMING RESPONSES					
TCVNV	Control Active Delay	5	45	ns	1
TCVNX	Control Inactive Delay	10	45	ns	1
TCLLH	ALE Active Delay (from CLK)		20	ns	1
TCLMCH	MCE Active Delay (from CLK)		25	ns	1
TSVLH	ALE Active Delay (from Status)		20	ns	1
TSVMCH	MCE Active Delay (from Status)		30	ns	1
TCHLL	ALE Inactive Delay	4	18	ns	1
TCLML	Command Active Dalay	5	35	ns	2
TCLMH	Command Inactive Delay	5	35	ns	2
TCHDTL	Direction Control Active Delay		50	ns	1
TCHDTH	Direction Control Inactive Delay		30	ns	1
TAELCH	Command Enable Time[1]		40	ns	3
TAEHCZ	Command Disable Time[2]		40	ns	4
TAELCV	Enable Delay Time	110	250	ns	2
TAEVNV	$\overline{AEN}$ to DEN		25	ns	1
TCEVNV	CEN to DEN, $\overline{PDEN}$		25	ns	1
TCELRH	CEN to Command		TCLML +10	ns	2
TLHLL	ALE High Time	TCLCH -10		ns	1

Note 1: TAELCH measurement is between 1.5V and 2.5V.
Note 2: TAEHCZ measured at 0.5V change in VO.

A. C. Test Circuits

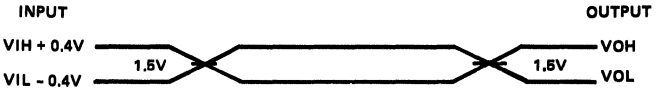


*Includes stray and jig capacitance

TEST CONDITION	IOH	IOL	V1	R1	C1
1	-4.0mA	+8.0mA	2.13V	220Ω	80pf
2	-8.0mA	+20.0mA	2.29V	91Ω	300pf
3	-8.0mA	–	1.5V	187Ω	300pf
4	-8.0mA	–	1.5V	187Ω	50pf

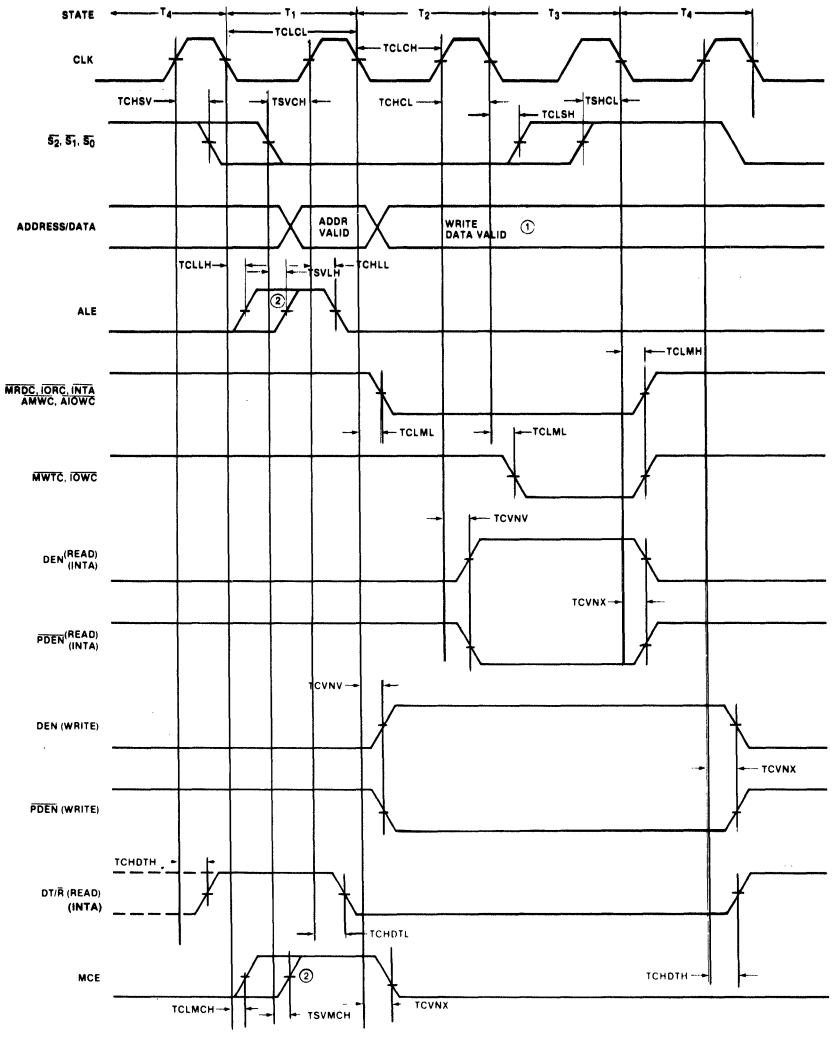
TEST CONDITION DEFINITION TABLE

A. C. Testing Input, Output Waveform



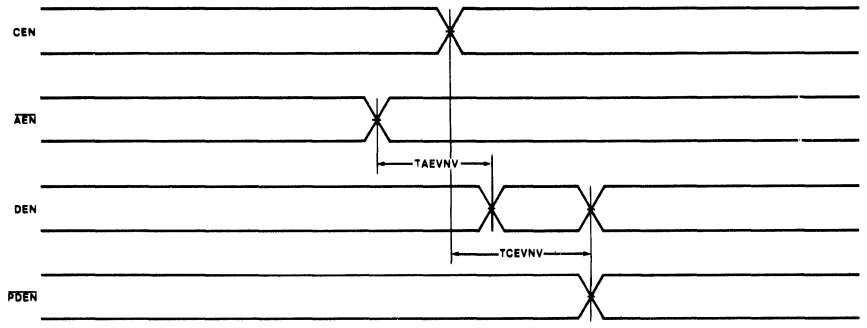
A. C. Testing: All input signals (other than CLK) must switch between VIL -0.4V and VIH +0.4V. CLK must switch between 0.4V and 3.9V. T_R and T_F must be less than or equal to 15ns.

Waveforms

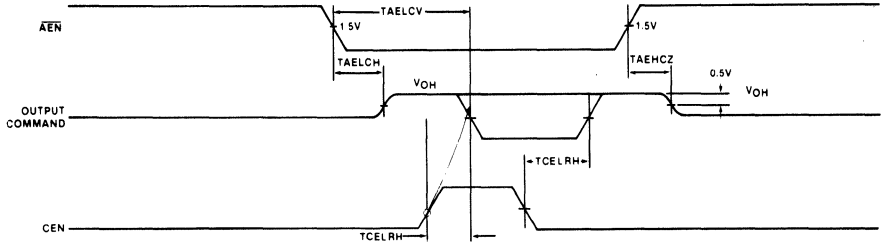


NOTES:
1. ADDRESS/DATA BUS IS SHOWN ONLY FOR REFERENCE PURPOSES
2. LEADING EDGE OF ALE AND MCE IS DETERMINED BY THE FALLING EDGE OF CLK OR STATUS GOING ACTIVE WHICHEVER OCCURS LAST
3. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS SPECIFIED OTHERWISE

Waveforms (cont.)



DEN, PDEN QUALIFICATION TIMING



NOTE: CEN must be low or valid prior to T2 to prevent the command from being generated.

ADDRESS ENABLE (AEN) TIMING (3-STATE ENABLE/DISABLE)

HARRIS

80C88
CMOS
8 BIT MICROPROCESSOR

Preview

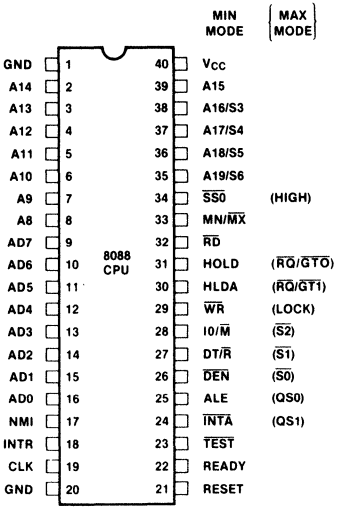
Features

- COMPATIBLE WITH NMOS 8088
- DIRECT SOFTWARE COMPATIBLITY WITH 80C86, 8086, 8088
- 8 BIT DATA BUS INTERFACE
- 16 BIT INTERNAL ARCHITECTURE
- COMPLETELY STATIC DESIGN
  - ▶ OPERATION FROM DC TO 5MHz
- LOW POWER OPERATION
  - ▶ ICCSB = 500μA MAXIMUM
  - ▶ ICCOP = 10mA/MHz TYPICAL
- 1 MBYTE OF DIRECT MEMORY ADDRESSING CAPABILITY
- 24 OPERAND ADDRESSING MODES
- BIT, BYTE, WORD, AND BLOCK MOVE OPERATIONS
- 8 and 16 BIT SIGNED/UNSIGNED ARITHMETIC
- BUS-HOLD CIRCUITRY ELIMINATES PULL-UP RESISTORS
- SCALED SAJI IV CMOS PROCESS
- SINGLE 5V POWER SUPPLY
- COMMERCIAL, INDUSTRIAL and MILITARY TEMPERATURE RANGES

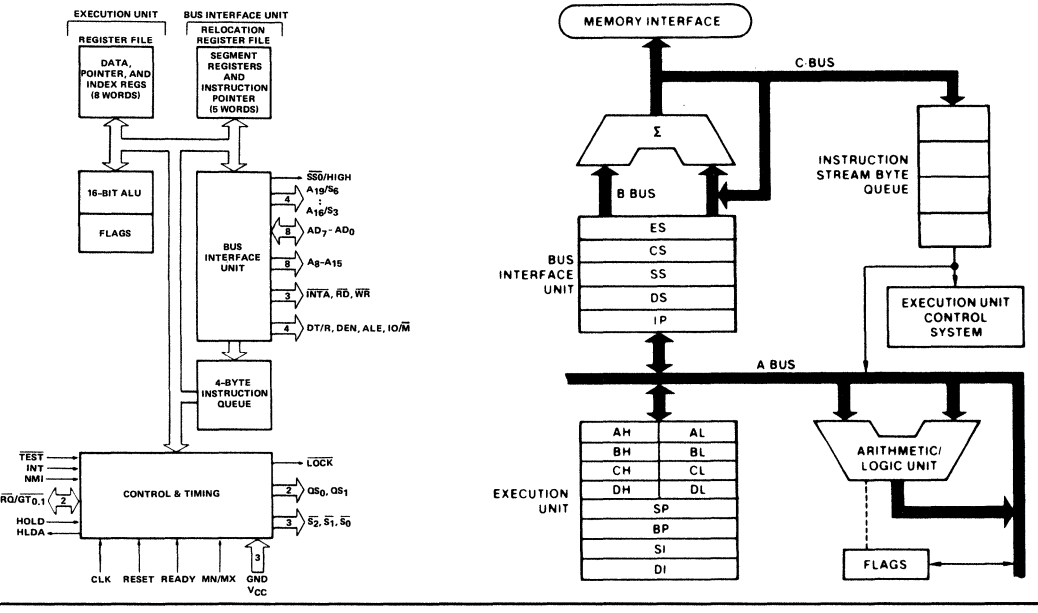
Description

The Harris 80C88 high performance 16 bit CMOS CPU is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). Two modes of operation, MINimum for small systems and MAXimum for larger applications such as multi-processing, allow user configuration to achieve the highest performance level. Full TTL compatibility and industry standard operation allow use of existing NMOS 8088 hardware and Harris CMOS 80C86 peripherals. Complete software compatibility with the 80C86, 8086 and 8088 microprocessors allows use of existing software in new designs.

Pinout



Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

82C37A

CMOS HIGH PERFORMANCE PROGRAMMABLE DMA CONTROLLER

Preview

Features

- SCALED SAJI IV CMOS PROCESS
- COMPATIBLE WITH THE NMOS 82C37A
- LOW POWER OPERATION
- COMMERCIAL, INDUSTRIAL AND MILITARY TEMPERATURE RANGES
- FULLY TTL COMPATIBLE
- FOUR INDEPENDANT DMA CHANNELS
- HIGH PERFORMANCE UP TO 1.6 MBYTES/SEC TRANSFERS
- DIRECTLY EXPANDABLE TO ANY NUMBER OF CHANNELS
- UPGRADED CAPABILITIES ALLOW SOFTWARE READ OF MOST INTERNAL REGISTERS AND STATUS BITS

Description

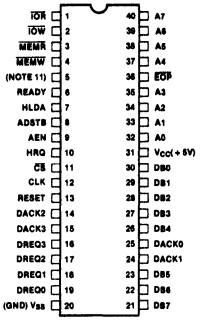
The Harris 82C37A Multimode Direct Memory Access (DMA) Controller is a peripheral interface circuit for microprocessor systems. It is designed to improve system performance by allowing external devices to directly transfer information from the system memory. Memory-to-memory transfer capability is also provided. The 82C37A offers a wide variety of programmable control features to enhance data throughput and system optimization and to allow dynamic reconfiguration under program control.

The 82C37A is designed to be used in conjunction with an external 8-bit address register such as the 82C82 and may be expanded to any number of channels by cascading additional controller chips.

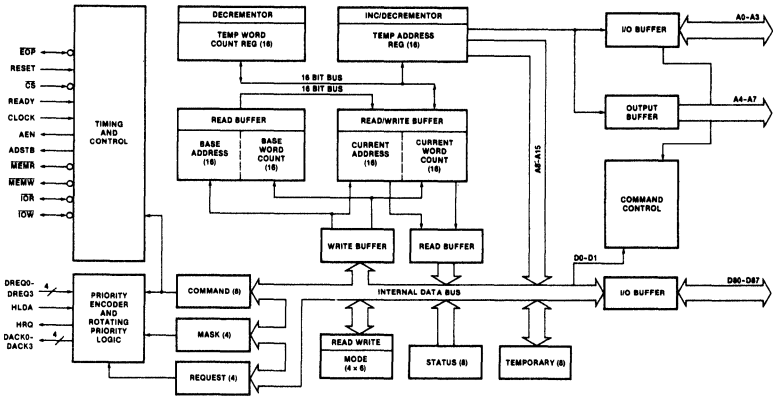
The three basic transfer modes allow programmability of the types of DMA service by the user. Each channel can be individually programmed to Auto-initialize to its original condition following an End of Process (EOP).

Each channel has a full 64K address and word count capability.

Pinout



Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow standard I.C. Handling Procedures.

HARRIS

82C83

CMOS OCTAL LATCHING INVERTING BUS DRIVER

Preview

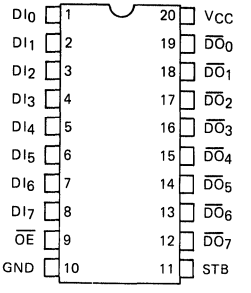
Features

- FULL EIGHT BIT PARALLEL LATCHING INVERTING BUFFER
- BIPOLAR 8283 COMPATIBLE
- THREE STATE NON-INVERTING OUTPUTS
- PROPAGATION DELAY – 35nsec MAX.
- A.C. CHARACTERISTICS GUARANTEED FOR:
  - ▶ FULL TEMPERATURE RANGE
  - ▶ 10% POWER SUPPLY TOLERANCE
  - ▶ C_L = 300pF
- SINGLE 5V POWER SUPPLY
- POWER SUPPLY CURRENT – 10μA MAX. STANDBY
- OUTPUTS GUARANTEED VALID AT V_{CC} = 2.0 VOLTS
- COMMERCIAL, INDUSTRIAL AND MILITARY TEMPERATURE RANGES
- 20 PIN PACKAGE ON 0.3" CENTERS

Description

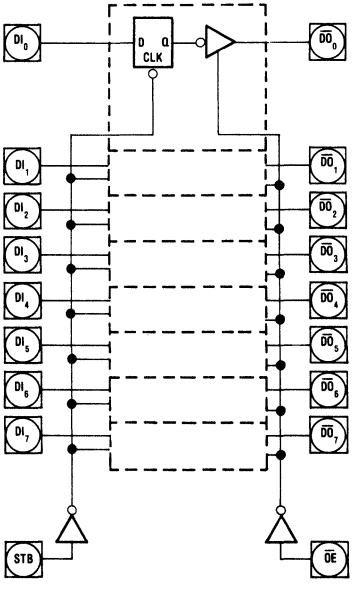
The Harris 82C83 is an octal latching buffer manufactured using a self-aligned silicon gate CMOS process. This circuit provides an eight bit parallel latch/buffer in a 20 pin package. The active high strobe (STB) input allows transparent transfer of data and latches data on the negative transition of this signal. The active low output enable ($\overline{OE}$) permits simple interface to state-of-the-art microprocessor systems. The 82C83 provides inverted data at the outputs.

Pinout



PIN NAMES	
DI_0 - DI_7	Data Input Pins
$\overline{DO}_0$ - $\overline{DO}_7$	Inverted Data Output Pins
STB	Active High Strobe Input
$\overline{OE}$	Active Low Output Enable

Functional Diagram



Truth Table

STB	$\overline{OE}$	DI	$\overline{DO}$
X	H	X	Hi-Z
H	L	L	H
H	L	H	L
↓	L	X	*

H = Logic One
L = Logic Zero
X = Don't Care
Hi-Z = High Impedance
↓ = Negative Transition
* = Latched to value of last data

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

HARRIS

82C84B

CMOS CLOCK GENERATOR DRIVER

Preview

Features

- GENERATES THE SYSTEM CLOCK FOR CMOS OR NMOS MICROPROCESSORS
- OSCILLATOR – STOP CIRCUITRY ALLOWS MINIMUM POWER STANDBY
- PIN COMPATIBLE WITH BIPOLAR 8284A AND CMOS 82C84A
- USES A PARALLEL MODE CRYSTAL CIRCUIT OR EXTERNAL FREQUENCY SOURCE
- PROVIDES READY SYNCHRONIZATION
- GENERATES SYSTEM RESET OUTPUT FROM SCHMITT TRIGGER INPUT
- CAPABLE OF CLOCK SYNCHRONIZATION WITH OTHER 82C84As or 82C84Bs
- TTL COMPATIBLE INPUTS/OUTPUTS
- VERY LOW POWER CONSUMPTION
- 18 PIN CERAMIC OR PLASTIC PACKAGE
- SINGLE +5V POWER SUPPLY
- COMMERCIAL, INDUSTRIAL AND MILITARY TEMPERATURE RANGES AVAILABLE

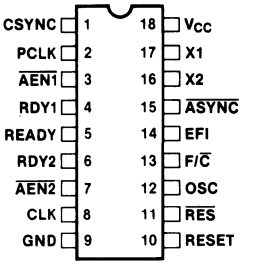
Description

The Harris 82C84B is a high performance CMOS clock generator-driver which is designed to service the requirements of both CMOS and NMOS microprocessors such as the 80C86, 80C88, 8086 and the 8088. The chip contains a crystal controlled oscillator, a divide-by-three counter and complete "Ready" synchronization and reset logic.

Static CMOS design permits operation with an external frequency source from DC to 25MHz. Crystal controlled operation to 25MHz is guaranteed with the use of a parallel, fundamental mode crystal and two small load capacitors. User controlled halt circuitry stops the internal oscillator and reduces the 82C84B and system power supply currents to standby levels.

Power consumption is a fraction of that of the equivalent bipolar circuits. This speed-power characteristic of CMOS permits the designer to custom tailor his system design with respect to power and/or speed requirements.

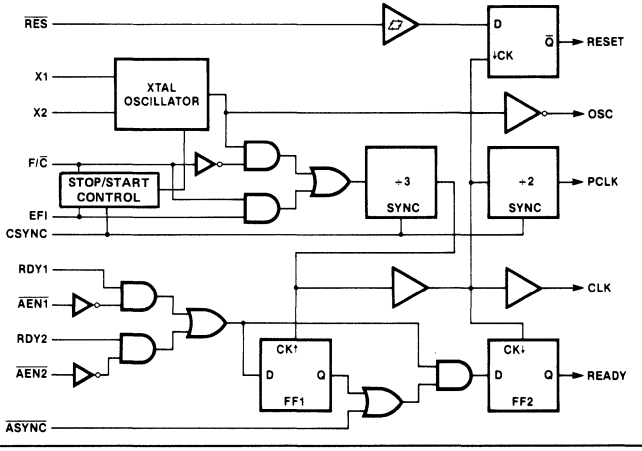
Pinout



CONTROL PIN	LOGICAL 1	LOGICAL 0
F/C	External Clock	Crystal Drive
RES	Normal	Reset
RDY1 RDY2	Bus Ready	Bus not ready
AEN1 AEN2	Address Disabled	Address Enabled
ASYNC	2 Stage Ready Synchronization	1 Stage Ready Synchronization
CSYNC*	Oscillator Stop	Oscillator Run

Note: F/C in low state

Block Diagram



3 80C86 FAMILY

HARRIS

82C86

CMOS OCTAL BUS TRANSCEIVER

Preview

Features

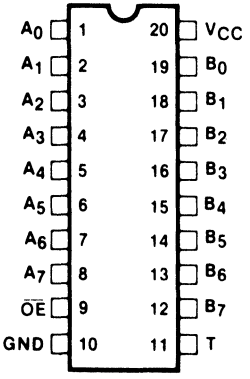
- FULL EIGHT BIT BIDIRECTIONAL BUS INTERFACE
- INDUSTRY STANDARD 8286 COMPATIBLE PINOUT
- THREE STATE NON-INVERTING OUTPUTS
- PROPAGATION DELAY 35 NSEC
- A.C. CHARACTERISTICS GUARANTEED AT RATED C_L
  - A SIDE - $C_L = 100pF$
  - B SIDE - $C_L = 300pF$
- SINGLE 5V POWER SUPPLY
- POWER SUPPLY CURRENT 10 μA MAX Standby
- 20 PIN PLASTIC OR CERAMIC PACKAGE
- COMMERCIAL, INDUSTRIAL AND MILITARY TEMPERATURE RANGES AVAILABLE

Description

The Harris 82C86 is an octal bus transceiver manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). This circuit provides a full eight bit bidirectional bus interface in a 20 pin package. The Transmit (T) control determines the data direction. The active low output enable ($\overline{OE}$) allows simple interface to the 80C86 and other microprocessors. The outputs of the 82C86 are non-inverting.

Pinout

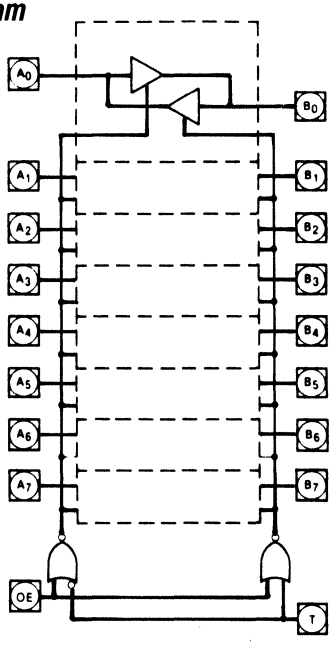
TOP VIEW



PIN NAMES

A_0-A_7	LOCAL BUS DATA I/O PINS
B_0-B_7	SYSTEM BUS DATA I/O PINS
T	TRANSMIT CONTROL INPUT
OE	ACTIVE LOW OUTPUT ENABLE

Functional Diagram



TRUTH TABLE

T	$\overline{OE}$	A	B
X	H	Hi-Z	Hi-Z
H	L	I	O
L	L	O	I

H = logical one
L = logical zero
I = input mode
O = output mode
X = don't care
Hi-Z = high impedance

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

CMOS OCTAL INVERTING BUS TRANSCEIVER

Preview

Features

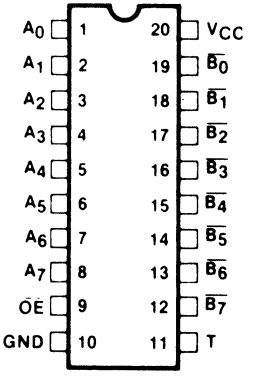
- FULL EIGHT BIT BIDIRECTIONAL BUS INTERFACE
- INDUSTRY STANDARD 8287 COMPATIBLE PINOUT
- THREE STATE INVERTING OUTPUTS
- PROPAGATION DELAY — 35 NSEC
- A.C. CHARACTERISTICS GUARANTEED AT RATED C_L
  - A SIDE - C_L = 100pF
  - B SIDE - C_L = 300pF
- SINGLE 5V POWER SUPPLY
- POWER SUPPLY CURRENT — 10 μA MAX Standby
- 20 PIN PLASTIC OR CERAMIC PACKAGE
- COMMERCIAL, INDUSTRIAL AND MILITARY TEMPERATURE RANGES AVAILABLE

Description

The Harris 82C87 is an octal bus transceiver manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). This circuit provides a full eight bit bidirectional bus interface in a 20 pin package. The Transmit (T) control determines the data direction. The active low output enable (OE) allows simple interface to state of the art microprocessors. Data at the outputs of the 82C87 are inverted.

Pinout

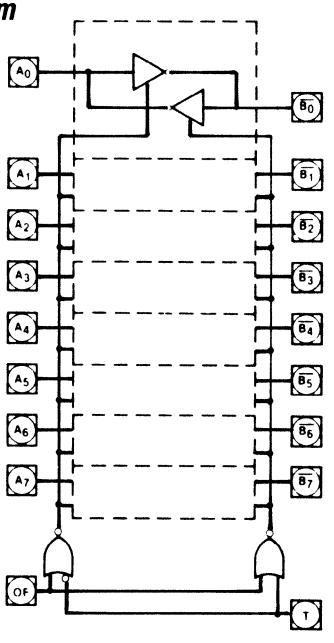
TOP VIEW



PIN NAMES

A_0-A_7	LOCAL BUS DATA I/O PINS
B_0-B_7	SYSTEM BUS DATA I/O PINS
T	TRANSMIT CONTROL INPUT
OE	ACTIVE LOW OUTPUT ENABLE

Functional Diagram



TRUTH TABLE

T	$\overline{OE}$	A	B
X	H	Hi-Z	Hi-Z
H	L	I	O
L	L	O	I

H = logical one
L = logical zero
I = input mode
O = output mode
X = don't care
Hi-Z = high impedance

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

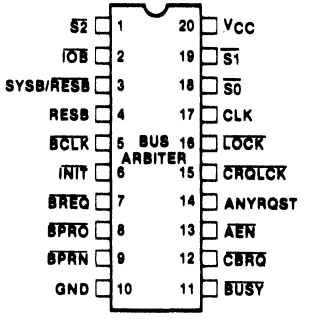
Preview

CMOS BUS ARBITER

Features

- INDUSTRY STANDARD 8289 COMPATIBLE PINOUT
- COMPATIBLE WITH 5 AND 8 MHz 80C86
- PROVIDES MULTIMASTER SYSTEM BUS CONTROL AND ARBITRATION
- COMPATIBLE WITH IEEE BUS STANDARD (MULTIBUS™)
- SINGLE 5V POWER SUPPLY
- POWER SUPPLY CURRENT
  - 10 μA MAX standby
  - 1 mA/MHz Operating
- 20 PIN PLASTIC OR CERAMIC PACKAGE
- COMMERCIAL, INDUSTRIAL AND MILITARY TEMPERATURE RANGES AVAILABLE

Pinout

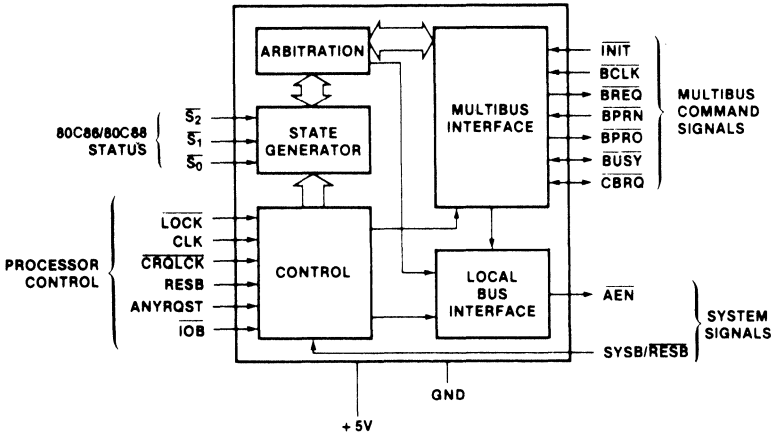


Description

The Harris 82C89 bus arbiter is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). This circuit along with the 82C88 bus controller, provides full bus arbitration and control for multi-processor systems. The 82C89 is typically used in medium to large 80C86 or 80C88 systems where access to the bus by several processors must be coordinated.

The 82C89 also provides high output current and capacitive drive to eliminate the need for additional bus buffering.

Functional Diagram



MULTIBUS IS A TRADEMARK OF INTEL CORPORATION

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

CMOS 12-Bit Microprocessors and Peripherals 4

Product Index 4-2

Product Information 4-3

CMOS Microprocessor and Peripherals Product Index

		Page
CMOS 12-BIT MICROPROCESSOR DATA SHEETS		
HD-6120	12 Bit High Performance Microprocessor	4-3
HD-6121	I/O Controller	4-22
HM-6100	12 Bit Static Microprocessor	4-30
HD-6101	Parallel Interface Element	4-51
CMOS BUS DRIVERS DATA SHEETS		
HD-6431	Hex Latching Bus Driver	4-59
HD-6432	Hex Bi-directional Bus Driver	4-62
HD-6433	Quad Bus Separator/Driver	4-65
HD-6434	Octal Resettable Latch	4-68
HD-6436	Octal Bus Buffer/Driver	4-71
HD-6440	Latch Decoder/Driver	4-74
HD-6495	Hex Bus Driver	4-78
82C82	CMOS Octal Latching Bus Driver	4-81
82C83	Octal Latching Inverting Bus Driver	4-82
82C86	Octal Bus Transceiver	4-83
82C87	Octal Bus Transceiver	4-84

HD-6120

CMOS HIGH SPEED 12 BIT MICROPROCESSOR

Features

- LOW POWER, 50 MW OPERATING, 2 MW STATIC
- SINGLE SUPPLY – 5V
- OPERATION FROM DC TO 5.1 MHZ
- INDUSTRIAL AND MILITARY TEMPERATURE RANGES
- ON-CHIP CRYSTAL OSCILLATOR CIRCUITRY
- ON-CHIP EXTENDED MEMORY ADDRESSING–32K MAIN MEMORY, 32K CONTROL PANEL
- OPTIMIZED MICRO-CODE MINIMIZES THE NUMBER OF CLOCK CYCLES REQUIRED FOR ALL INSTRUCTIONS
- TWO ON-CHIP STACK POINTERS
- SIMPLIFIED MEMORY AND I/O CONTROL SIGNALS FOR EASY HARDWARE INTERFACING
- VECTORED INTERRUPT CAPABILITY
- SOFTWARE IS PAGE RELOCATABLE

Description

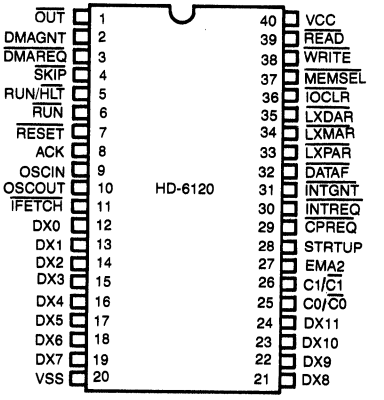
The HD-6120 is a general purpose high speed, CMOS 12 bit microprocessor. It is designed to recognize the instruction set of Digital Equipment Corporation's PDP-8/E* minicomputer.

Many architectural, functional and processing enhancements have been designed into the 6120 such that it can provide much higher system performance than its predecessor, the 6100.

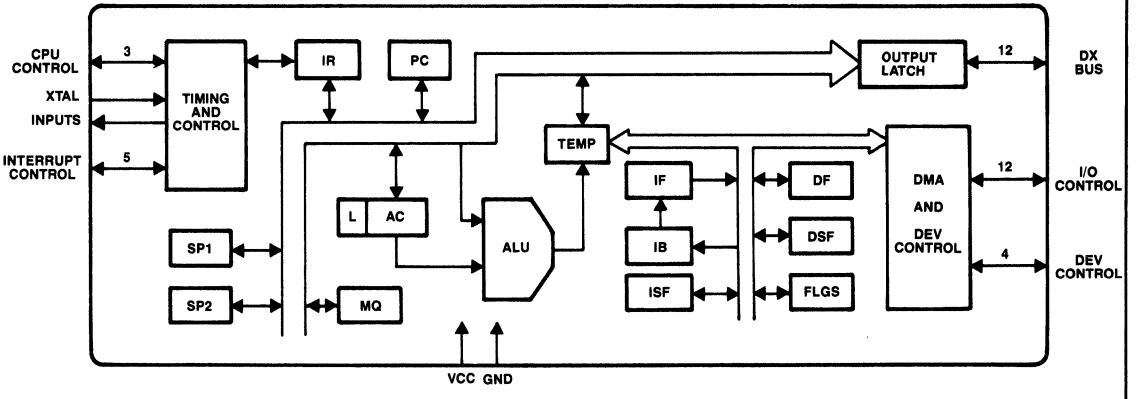
The 6120 is targeted toward the experienced PDP-8* or 6100 user. Twelve bit accuracy, rapid interrupt response, battery backup and low power (sealed enclosure) capability all equate to a processor ideally suited to real time control applications such as data acquisition, industrial control and harsh environment military systems.

* *TRADEMARK OF DIGITAL EQUIPMENT CORP.*

Pinout



Functional Diagrams



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0 VOLTS
Operating Voltage Range	+4V to +7V
Input/Output Voltage Applied	VSS−0.3V to VCC+0.3V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Industrial (−9, −9+)	−40°C to +85°C
Military (−2, −8)	−55°C to +125°C
Maximum Power Dissipation	1 Watt

CAUTION: Stresses above those listed in the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. ELECTRICAL CHARACTERISTICS; VCC=5.0V±5%; T_A = Industrial or Military

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	LOGICAL ONE INPUT VOLTAGE	70% VCC		V	
VIL	LOGICAL ZERO INPUT VOLTAGE		30% VCC	V	
VIH(CLK)	LOGICAL ONE CLOCK VOLTAGE	VCC−0.5		V	50% duty cycle $t_r, t_f \leq 20$ ns
VIL(CLK)	LOGICAL ZERO CLOCK VOLTAGE		VSS+0.5	V	50% duty cycle $t_r, t_f \leq 20$ ns
VTH+	SCHMITT TRIGGER POSITIVE THRESHOLD	50% VCC	VCC−0.5	V	$\overline{\text{RESET}}$, $\overline{\text{DMAREQ}}$, $\overline{\text{CPREQ}}$
VTH−	SCHMITT TRIGGER NEGATIVE THRESHOLD	0.5	30% VCC	V	$\overline{\text{RESET}}$, $\overline{\text{DMAREQ}}$, $\overline{\text{CPREQ}}$
VOH	LOGICAL ONE OUTPUT VOLTAGE	VCC−0.5		V	IOH = −1.6mA
VOL	LOGICAL ZERO OUTPUT VOLTAGE		0.5	V	IOL = 1.6mA
IIL	INPUT LEAKAGE CURRENT	−10	10	μA	OV≤VIN≤VCC
IO	OUTPUT LEAKAGE CURRENT	−10.0	10.0	μA	OV≤VO≤VCC
ICC	POWER SUPPLY STANDBY CURRENT		500	μA	VIN=VCC or GND VCC = 5.25 V RESET STATE OUTPUTS OPEN
ICC*	POWER SUPPLY OPERATING		10	ma	VIN=VCC or GND VCC = 5.25 V F = 5.1 Mhz OUTPUTS OPEN
IOSH	HOLD CURRENT DURING DMAGNT	−0.2	−0.6 −10.0	ma μa	Vout = VCC−1.0V Vout = OV $\overline{\text{LXMAR}}$, $\overline{\text{LXPAR}}$, $\overline{\text{READ}}$, $\overline{\text{WRITE}}$, $\overline{\text{OUT}}$ AND MEMSEL
IOSS	HOLD CURRENT DURING IOT SAMPLE TIMES	−1.6	−10.0	ma	Vout = OV C0, C1, AND $\overline{\text{SKIP}}$ OUTPUTS
IOSS	HOLD CURRENT DURING IOT SAMPLE TIMES	−50	−250	μa	Vout = OV $\overline{\text{INTREQ}}$ OUTPUT
CIN*	INPUT CAPACITANCE		5	pf	FREQ = 1 MHZ T_A=25°C VIN=VCC or GND
COUT*	OUTPUT CAPACITANCE		15	pf	FREQ = 1 MHZ T_A=25°C VIN=VCC or GND

** Guaranteed and sampled, but not 100% tested*

A.C. ELECTRICAL CHARACTERISTICS; VCC=5.0V±5%; T_A=Industrial or Military; C_L=50 pf, FREQ=5.1 MHZ

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
F	OPERATING FREQUENCY	0	5.1	Mhz	
T	MINOR CYCLE PERIOD	392		ns	T = 2/F
TL	LXMAR, LXPAR, LXDAR PULSE WIDTH	125		ns	F=5.1 Mhz
TAS	ADDRESS SET UP TIME	60		ns	
TAH	ADDRESS HOLD TIME	180		ns	
TREAD	READ ACCESS TIME	720		ns	
TRS	READ SET UP TIME	135		ns	
TRH	READ HOLD TIME	20		ns	MEMORY OPERATIONS
TRP	READ PULSE WIDTH	425		ns	
TRD	READ PULSE DELAY	40		ns	
TWPD	WRITE PULSE DELAY	200		ns	
TWS	WRITE SET UP TIME (ALL NON IOT)	375		ns	
TWP	WRITE PULSE WIDTH (ALL NON IOT)	425		ns	
TWH	WRITE HOLD TIME (ALL NON IOT)	200		ns	
TWSIO	WRITE SET UP TIME (IOT)	200		ns	
TWIO	WRITE PULSE WIDTH (IOT)	375		ns	
TWHIO	WRITE HOLD TIME (IOT)	125		ns	
TDA	READ ACK DELAY FOR NO WAIT		150	ns	
TXA	WRITE ACK DELAY FOR NO WAIT		150	ns	F=5.1 Mhz

NOTE: All measurements are taken with input rise and fall times ≤ 20 nsec.

DECOUPLING CAPACITORS

The transient current required to charge and discharge the 50 pF load capacitance specified in the 6120 data sheet is determined by

$$i = C_L\,(dv/dt)$$

Assuming that all DX outputs change state at the same time and that dv/dt is constant;

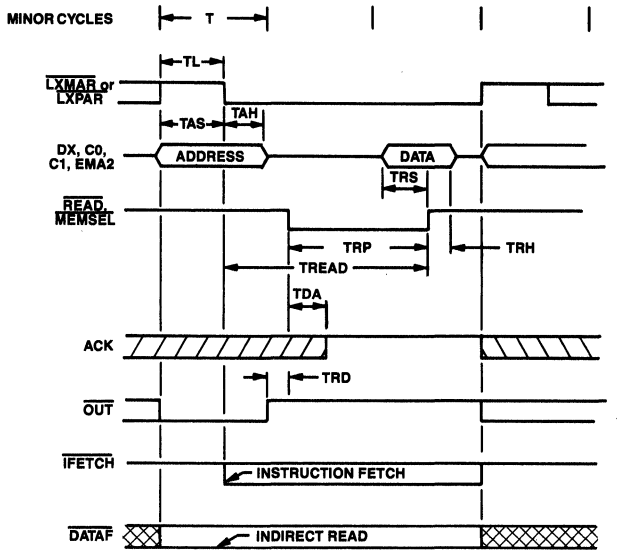
$$i \cong C_L \frac{(VCC \times 80\%)}{t_R/t_F}$$

where t_R=20 ns, VCC=5.0 volts, C_L=50 pF on each of twelve outputs.

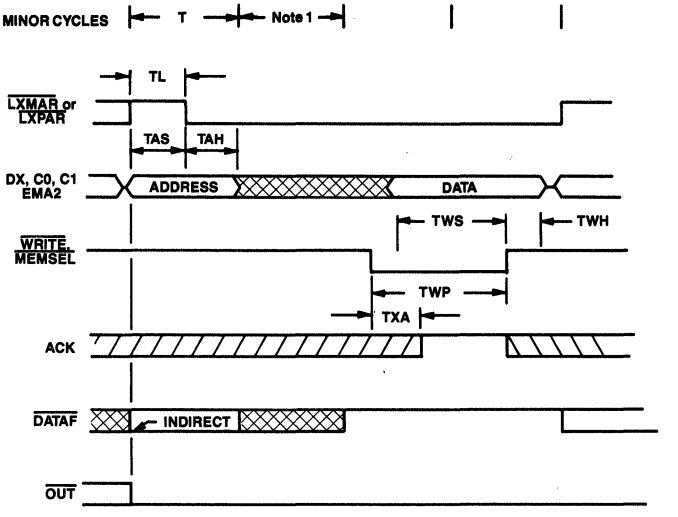
$$i \cong (12 \times 50 \times 10^{-12}) \times (5.0v \times 0.8)/(20 \times 10^{-9})$$
$$\cong 120\ mA$$

This current spike may cause a large negative voltage spike on VCC, which could cause improper operation of the device. To filter out this noise, it is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between VCC and GND at each device, with placement being as near to the device as possible.

It is recommended that for systems with greater than 50 pF loading on the DX outputs that Harris HD-6432 CMOS Hex Bi-directional bus drivers be used to buffer the 6120 from the rest of the system. The HD-6432 bus driver has guaranteed performance specifications up to a 300 pF load.

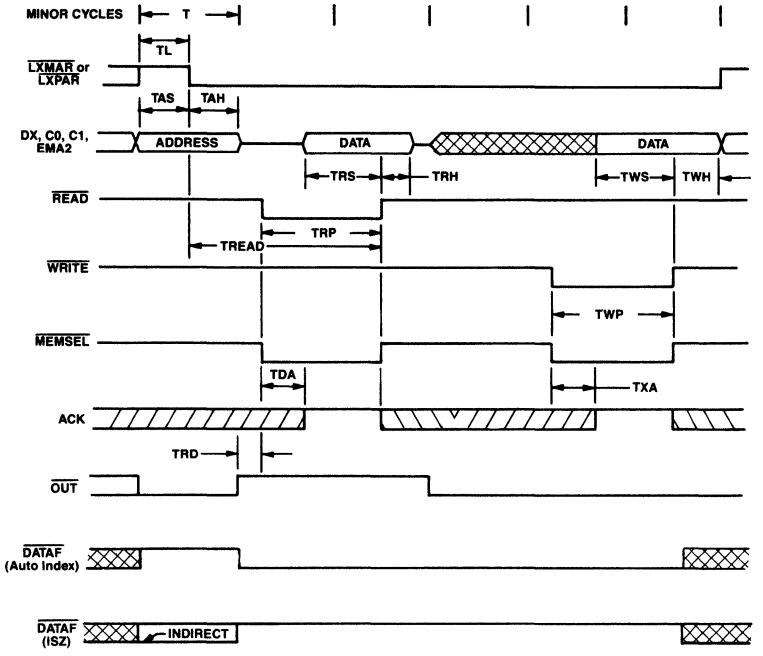


MEMORY READ OPERATION

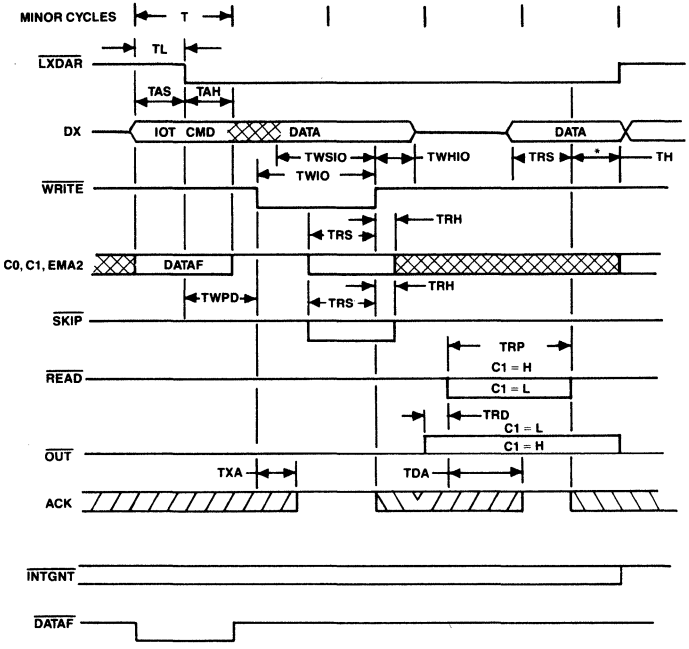


NOTE 1: This cycle is deleted on PAC1, PAC2, PPC1, PPC2 and control panel Interrupt writes.

MEMORY WRITE OPERATION



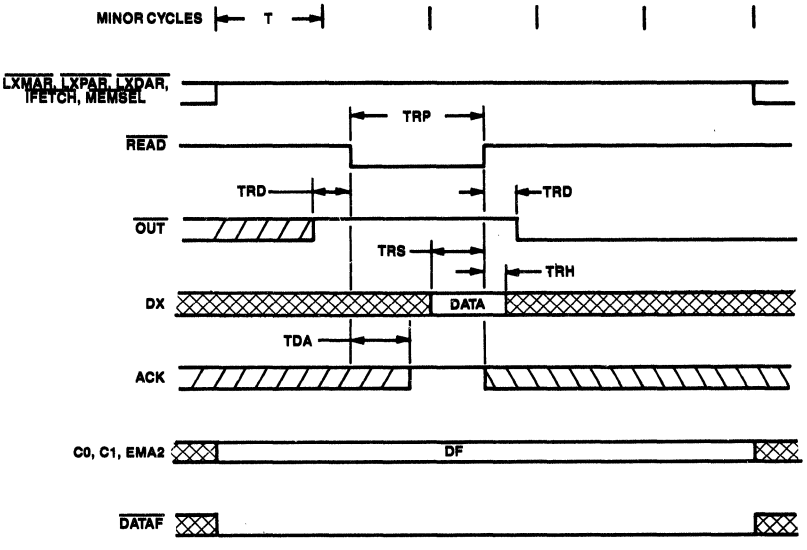
MEMORY READ-MODIFY-WRITE OPERATION



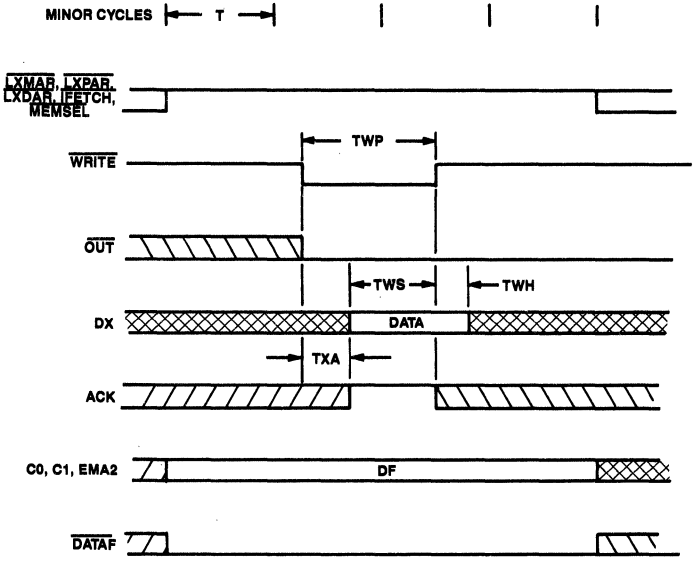
NOTES: Operation is shortened one Minor Cycle if READ is not executed.

* Read Data must be held until the rising edge of LXDAR for Read IOTs.

EXTERNAL IOT OPERATION



OR SWITCH REGISTER (OSR)



WRITE TO SWITCH REGISTER

Pin Assignments

I/O	Pin	Symbol	Active Level	Description
O	1	$\overline{OUT}$	Low	Bus timing control output which is low during all bus write or addressing operations. This signal is used to enable outbound bus drivers.
O	2	DMAGNT	High	Direct memory access grant output – DX, C0, C1, and EMA2 lines are high impedance.
I	3	$\overline{DMAREQ}$	Low	Schmitt trigger input. Direct memory access request – DMA is granted at the end of the current bus operation. Upon DMA grant, the 6120 suspends program execution until the $\overline{DMAREQ}$ line is pulled high.
I	4	$\overline{SKIP}$	Low	Input which causes the 6120 to skip the next instruction if low during an I/O instruction.
I	5	RUN/$\overline{HLT}$		Pulsing the RUN/$\overline{HLT}$ input causes the 6120 to alternately run and halt by changing the state of the internal RUNHLT flip flop on the positive transition of the RUN/$\overline{HLT}$ line.
O	6	$\overline{RUN}$	Low	This output indicates the operating state of the 6120. It is low at all times except during the reset and halt states.
I	7	$\overline{RESET}$	Low	Schmitt trigger input. Clears the AC and the memory extension registers and loads 7777 (octal) into the PC. RUNHLT is set. The STRTUP line controls whether execution starts in control panel or main memory. $\overline{RESET}$ must be held low at least 42 clock cycles after the clock starts running in order to initialize the timing generator. $\overline{LXDAR}$ is held low while $\overline{RESET}$ is low, and remains low until after the positive transition of $\overline{RESET}$ and $\overline{IOCLR}$.
I	8	ACK	High	This input indicates that peripheral or external memory is ready to transfer data. The 6120 read or write state gets extended as long as ACK is low. During this time the 6120 is in the lowest power state with clocks running.
I	9	OSCIN		Input to crystal oscillator amplifier. (Also external clock input.)
O	10	OSCOUT		Output of crystal oscillator amplifier.
O	11	$\overline{IFETCH}$	Low	Instruction fetch cycle output.
I/O	12-19, 21-24	DX0-DX11	High	Multiplexed bidirectional data in, data out and address lines. (DX0=MSB, DX11=LSB.)
	20	VSS		Most negative supply voltage.
I/O	25	C0/$\overline{C0}$		Multiplexed extended memory address (EMA) active high output MSB and peripheral device control line active low input from the peripheral device during an I/O transfer.
I/O	26	C1/$\overline{C1}$		Multiplexed EMA bit 1 and peripheral control line. See C0.
O	27	EMA2	High	Low order extended memory address output.
I	28	STRTUP		This input is tied to either VCC or VSS. If tied to VSS, the 6120 makes a panel request (caused by the PWRON flag) as soon as $\overline{RESET}$ goes to VCC. 7777 is stored in location 0000 of field 0 of panel memory. If STRTUP is tied to VCC, PWRON does not cause a panel request. Instead, the CPU starts running in location 7777 of field 0 of main memory. Location 0000 of main memory is not altered.
I	29	$\overline{CPREQ}$	Low	Schmitt trigger input. External control panel request – a dedicated interrupt which bypasses the normal device interrupt request structure. $\overline{CPREQ}$ causes a control panel interrupt request by setting the bootstrap flag with the negative going transition of $\overline{CPREQ}$. Therefore, this input is transition rather than level sensitive.
I	30	$\overline{INTREQ}$	Low	Peripheral device interrupt request input.
O	31	$\overline{INTGNT}$	Low	Peripheral device interrupt grant output.
O	32	$\overline{DATAF}$	Low	Output which is low whenever the Data Field is placed on the C0, C1 and EMA2 lines.
O	33	$\overline{LXPAR}$	Low	Output which causes control panel memory address register to be loaded. Same as $\overline{LXMAR}$, but for control panel memory operations.
O	34	$\overline{LXMAR}$	Low	Output which causes main memory address register to be loaded. Address is strobed into the main memory at the falling edge of $\overline{LXMAR}$.
O	35	$\overline{LXDAR}$	Low	Output which causes device address register to be loaded. Same as $\overline{LXMAR}$ or $\overline{LXPAR}$, except for IOT operations. Also used to distinguish between $\overline{IOCLR}$ signals. See $\overline{IOCLR}$ below.
O	36	$\overline{IOCLR}$	Low	Output which is low when $\overline{RESET}$ is low, or when CAF instruction is given. Used to clear I/O flags. If caused by $\overline{RESET}$, $\overline{LXDAR}$ is low during and after the trailing edge of $\overline{IOCLR}$.
O	37	$\overline{MEMSEL}$	Low	Memory select. During memory operations, this output pulses to VSS at bus read and write times.
O	38	$\overline{WRITE}$	Low	Write pulse. This output is low during all bus data write operations; memory, I/O, and write to switch register.
O	39	$\overline{READ}$	Low	Read pulse. This output is low during all bus read operations; memory, I/O and switch register. It also serves the function of enabling inbound bus drivers.
	40	VCC		Positive supply voltage.

Major Registers

ACCUMULATOR (AC)

The AC is a 12-bit register with which arithmetic and logical operations are performed. Data words may be fetched from memory to the AC or stored from the AC into memory. Arithmetic and logical operations involve two operands, one held in the AC and the other fetched from memory. The result of the operation is left in the AC. The AC may be cleared, complemented, tested, incremented or rotated under program control. The AC also serves as an input-output register. All programmed data transfers pass through the AC.

Link (L)

L is a 1-bit flip flop that serves as a high-order extension of the AC. It is used as a carry flip flop for 2's complement arithmetic. A carry out of the ALU complements L. L can be cleared, set, complemented and tested under program control and rotated as a part of the AC.

MQ REGISTER (MQ)

The MQ is a 12-bit temporary register which is program accessible. The contents of AC may be transferred to the MQ for temporary storage. MQ can be OR'ed with the AC and the result stored in the AC. The contents of the AC and the MQ may also be exchanged.

OUTPUT LATCH (OL)

While accessing memory or I/O, all data or addresses generated by the 6120 on the DX bus are held in the OL for the time required on the bus. This frees the 6120 internal bus for other uses during these operations. The output latch can also be read to the 6120 internal bus so that it can function as a temporary holding register for internal operations.

PROGRAM COUNTER (PC)

The 12-bit PC contains the address of the memory location from which the next instruction is fetched. During an instruction fetch, the PC is transferred to OL and the PC is then incremented by 1. When there is a branch to another address in memory, the branch address is set into the PC. Branching normally takes place under program control. A skip (SKP, SMA, SZA, SNL, etc.) instruction increments the PC by 1 (again), thus causing the next instruction to be skipped. The skip instruction may be unconditional or conditional on the state of the AC and/or LINK. During an input-output operation, a device can also cause the next instruction to be skipped.

TEMPORARY REGISTER (TEMP)

The 12-bit TEMP register latches the result of an ALU operation before it is sent to the destination register to avoid race conditions. The TEMP is also used as an internal register during instruction execution.

INSTRUCTION REGISTER (IR)

During an instruction fetch, the 12-bit IR contains the instruction that is to be executed by the 6120.

STACK POINTERS (SP1 and SP2)

The stack pointers are two twelve-bit registers which hold the address of the next stack storage location. PPCX or PACX instructions cause post-decrement of the contents of stack pointer SPX. RTNX or POPX cause a pre-increment of the contents of the stack pointer. Stack pointers are loaded from, and read into, the AC. They may also be used as program-controlled temporary registers.

Memory Extension Control Registers

INSTRUCTION FIELD (IF)

The 3-bit Instruction Field holds the memory field from which all instructions, all indirect address pointers and all directly addressed operands are obtained. It may be read into the AC, and loaded from the IB. It is cleared by $\overline{\text{RESET}}$.

INSTRUCTION BUFFER (IB)

The 3-bit Instruction Buffer serves as a holding register for instructions which change the IF. Instead of changing the IF directly, field bits are loaded into the IB, and transferred to the IF at the next JMP, JMS, RTN1 or RTN2. The IB may be loaded from instruction bits, from the AC or from the ISF. The IB is cleared by $\overline{\text{RESET}}$.

INSTRUCTION SAVE FIELD (ISF)

The 3-bit ISF is loaded with the contents of the IF upon granting of an interrupt. The ISF may be read into the AC. It is cleared by $\overline{\text{RESET}}$.

DATA FIELD (DF)

The 3-bit Data Field holds the memory field from which all indirectly addressed operands are obtained. The DF may be loaded from instruction bits, from the AC or from the DSF. It may be read into the AC. It is cleared by $\overline{\text{RESET}}$.

DATA SAVE FIELD (DSF)

The 3-bit DSF is loaded with the contents of the DF upon granting of an interrupt. The DSF may be read into the AC. It is cleared by $\overline{\text{RESET}}$.

Basic Timing and State Control

A 15-bit address is sent on the C0, C1, EMA2 and DX lines for memory reference instructions. The $\overline{\text{LXMAR}}$ or $\overline{\text{LXPAR}}$ signals cause an external register to store the address information if required. When executing an input-output instruction, $\overline{\text{LXDAR}}$ causes an external register to be loaded with device address and control information.

Memory data is read for an input transfer (READ). ACK controls the transfer duration. If ACK is low during input transfers, the 6120 waits with the $\overline{\text{READ}}$ line low. The high state of the ACK signal causes the 6120 to continue.

Output transfers are similar to input transfers. The address is defined as given above. ACK controls the length of time for which the $\overline{\text{WRITE}}$ signal is low, similar to the $\overline{\text{READ}}$ line control.

During an instruction fetch the instruction to be executed is retained internally and then executed. During the sequencing of the instruction the external request lines are sampled by the priority network. The state of this network decides whether the machine is going to fetch the next instruction in sequence or service one of the internal or external request lines.

Internal Priority Structure

GENERAL DESCRIPTION

The external request lines and the internal request flags are sampled in an internal priority network. The internal priority is RESET, DMAREQ, RUN/HLT, CPREQ, INTREQ, and IFETCH. The state of the priority network determines the next operation.

IFETCH

If no external or internal requests are pending, the 6120 fetches the next instruction pointed to by the contents of the PC. The IFETCH line is low during the cycle in which the instruction is fetched.

RESET

RESET initializes all internal flags and clears the AC, LINK and MQ. All memory extension bits (IF, IB, DF, ISF and DSF) are cleared. The interrupt enable and interrupt inhibit flip flops are cleared. RUNHLT is set to the run state. The RUN line is held high by RESET. The states of SP1 and SP2 are undefined at power up, and are unaffected by RESET.

Upon application of power, the internal timing generator is completely initialized within 42 clock pulses after power is within limits with RESET held low.

The 6120 remains in the reset state as long as the RESET line is low. LXMAR, LXPAR, READ, WRITE, MEMSEL, INTGNT and IFETCH are held high. IOCLR is held low. After RESET is changed from low to high, IOCLR is made high. LXDAR is held low for one minor cycle after IOCLR is high. DMAGNT and OUT are low. The first LXMAR or LXPAR occurs 5-1/2 minor cycles after IOCLR goes high. The PC is set to 7777 (octal) and execution commences in control panel or main memory, depending on whether the STRTUP input is low or high respectively. If execution commences in control panel memory, the FZ flag is set, the Panel Data flag is cleared, and 7777 is deposited in location 0000 of control panel memory before beginning instruction execution at location 7777. If execution commences in main memory, location 0000 of main memory is not modified.

RUN/HLT

The RUN/HLT line changes the state of the RUNHLT flip flop. This flip flop is initially placed in the run state by RESET. Pulsing RUN/HLT low causes the 6120 to alternately run and halt. This is true whether executing in main memory or control memory. The RUN/HLT line is normally high. The 6120 recognizes the positive transition of the RUN/HLT signal. The HLT instruction (7402 octal) does not cause the RUNHLT flip flop to be cleared, but causes entry into panel mode with the HLTFLG set.

Memory Organization

The 6120 has a basic addressing capacity of 4096 12-bit words. The addressing capacity is extended by the internal extended memory control hardware. The memory system is organized in 4096 word groups, called memory fields. The first 4096 words of memory are in field 0. If a full 32K block of memory is installed, the uppermost memory field will be numbered 7. Two 32K word blocks of memory may be connected to the 6120. One of these blocks is known as main memory and the other is known as panel memory.

In any given memory field, every location has a unique 4 digit octal (12 bit binary) address, 0000 to 7777 (0000 to 4095 decimal). Each memory field is subdivided into 32 pages of 128 words each. Memory pages are numbered sequentially from page 00, containing octal addresses 0000-0177, to page 37 (octal), containing octal addresses 7600-7777. The most significant 5 bits of a 12-bit memory address denote the page number and the 7 low order bits specify the address of the memory location within the given page.

During an instruction fetch cycle, the 6120 fetches the instruction pointed to by the IF, PC, and address strobes LXMAR or LXPAR. The contents of the PC are transferred to the OL. The PC is incremented by 1. The PC now contains the address of the 'next' sequential instruction. The OL now contains the address of the 'current' instruction which must be fetched from memory. Bits 0-4 of the OL identify the current page, that is, the page from which instructions are currently being fetched. Bits 5-11 of the OL identify the location within the current page. (Page zero, by definition, denotes the first 128 words of memory within a field, octal addresses 0000-0177.)

Memory Reference Instructions (MRI)

The memory reference instructions operate on the contents of a memory location or use the contents of a memory location to operate on the AC or the PC. Bits 0-2 of a memory reference instruction specify the operation code, or opcode, and the 9 low-order bits specify the operand address. Bits 5-11, the page address, identify the location of the operand on a given page, but they do not identify the page itself. The page is specified by bit 4, called the page bit. If bit 4 is a 0, the page address is interpreted as a location on page 0. If bit 4 is a 1, the page address is interpreted to be on the current page. The entire 12-bit address, consisting of the 7 low-order bits from the instruction and either 0 or the contents of the OL in the 5 high-order bits is known as the instruction address, or IA. The IF provides the 3 high-order bits of the complete 15-bit address, IA.

Other locations are addressed by utilizing bit 3. When bit 3 is a 0, the operand is directly addressed, and IA is the location of the operand. When bit 3 is a 1, the operand is indirectly addressed, and the contents of IA specify the location of the operand. To address a location that is not on page 0 or the current page, the absolute address of the desired location is stored in one of the 256 directly-addressable locations as a pointer address. The instruction addresses the operand indirectly through this pointer. Upon execution, the MRI operates on the contents of the location identified by the address contained in the pointer location. The pointer is obtained from the current Instruction Field; the data is in the current Data Field.

It should be noted that locations 0010-0017 (octal) in page 0 of any field are autoindexed. If these locations are addressed as indirect pointers, the contents are incremented by 1 and restored before they are used as the operand address. These locations may, therefore, be used for indexing applications. During the memory write operation, the DF appears on C0, C2, and EMA2. Indirect reference to auto index registers from page 0 work as defined whether the page bit is "1" or "0".

Data is represented in two's complement integer notation. In this system of notation, the negative of a number is formed by complementing each bit in the data word and adding "1" to the complemented number. The sign is indicated by the most-significant bit. In the 12-bit word used in the 6120, when bit 0 is a "0", it denotes a positive number and when bit 0 is a "1", it denotes a negative number. The number range for this system is +3777 to −4000 octal (+2047 to −2048 decimal).

Microprogramming

Group 1, 2 and 3 instructions are all microprogrammable. This means that as many as five discrete instructions can be combined into one instruction which can execute in the same amount of time required for a single discrete instruction. Instructions listed under Groups 1, 2 and 3 represent the most commonly used microcoded instructions for these groups and are not a complete listing of all possible instructions. The general rule of thumb is that if an instruction can be represented in machine code (using the "Microinstruction Format" templet), then it is a legal instruction. The logical sequence table which accompanies each "Microinstruction Format" templet shows the order in which the microcoded operations are performed. "Introduction to Programming" by Digital Equipment Corporation further explains the PDP-8* instruction set and the use of microprogramming. This handbook is also available from Harris Semiconductor.

* Trademark of Digital Equipment Corporation

HD-6120 Oscillator Requirements

The HD-6120 has been designed to work with either a parallel resonant, fundamental mode crystal or an external frequency source.

EXTERNAL CRYSTAL

When using an external crystal, two capacitors and a resistor are required to complete the oscillator circuit. Table 1 lists the required crystal characteristics and Figure 1 shows the correct circuit connections.

TABLE 1

Parameter	Typical Characteristic
Frequency	2.4 – 5.1 Mhz
Type of Operation	Parallel resonant, AT cut, Fundamental mode
Load Capacitance	C_L = 20pf or 32pf
R_{series} (Max.)	200 Ω at 5.1 Mhz

The load capacitors C1, C2 are chosen such that the total (including stray) capacitance seen by the crystal matches the specified load capacitance (C_L). For C_L = 20pf. a value of C1 = C2 = 20pf. is normally used. For C_L = 32pf. C1 and C2 would be approximately 47pf. The actual values are normally not critical unless an ultra precise frequency is desired.

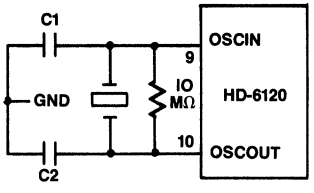


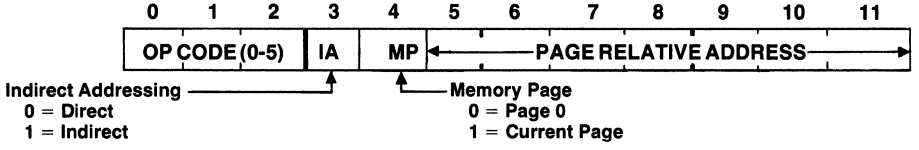
FIGURE 1

EXTERNAL FREQUENCY SOURCE

When using an external frequency source, the duty cycle should be 50/50 with rise and fall times less than 20ns. Input voltage levels should be $V_{IH} \geq VCC - 0.5V$ and $V_{IL} \leq 0.5V$. The OSCIN pin of the HD-6120 is used in this case with the OSCOUT pin left open. The Harris 82C84A CMOS Clock Generator is an excellent external frequency source which provides three outputs at different divide ratios (÷1, ÷3, ÷6).

Memory Reference Instructions

MICROINSTRUCTION FORMAT



Mnemonic	Opcode	Minor Cycles Dir	Ind	Auto	Operation
AND	0xxx	7	10	12	LOGICAL AND: Causes a bit-by-bit boolean AND between the contents of the Accumulator and the contents of the effective address (xxx) specified by the instruction. The result is left in the AC and the data word in the referenced location is not altered.
TAD	1xxx	7	10	12	TWO'S COMPLEMENT ADD: Performs a binary two's complement addition between the specified data word and the contents of the AC; the result is left in the AC. If a carry out occurs, the state of the Link is complemented. If the AC is initially cleared, this instruction acts as a load from memory.
ISZ	2xxx	9*	12*	14*	INCREMENT AND SKIP IF ZERO: The contents of the effective address is incremented by 1 and restored. If the result is zero, the next sequential instruction is skipped.
DCA	3xxx	7	10	12	DEPOSIT AND CLEAR THE ACCUMULATOR: The contents of the AC are stored in the effective address and the AC is cleared.
JMS	4xxx	7	10	12	JUMP TO SUBROUTINE: The contents of the PC is stored in the effective address and the effective address + 1 is stored in the PC. The Link, AC and MQ are unchanged.
JMP	5xxx	4	7	9	JUMP: The effective address is loaded into the PC thus causing program execution to branch to a new location.

* Add two Minor Cycles if a skip is taken.

Group 1 Operate Instructions

All group 1 instructions require 6 minor cycles, except those performing an RTR, RTL, or BSW instruction (8 minor cycles).

MICROINSTRUCTION FORMAT

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	0	CLA	CLL	CMA	CML	R1	R2	R3	IAC

Logical Sequence:
1 – CLA, CLL
2 – CMA, CML
3 – IAC
4 – RAR, RAL, RTR, RTL, BSW, R3L

Bit	R1	R2	R3	
	0	0	0	No Rotate
	0	0	1	BSW
	0	1	0	RAL
	0	1	1	RTL
	1	0	0	RAR
	1	0	1	RTR
	1	1	0	R3L
	1	1	1	Do Not Use

Mnemonic	Opcode	Logical Sequence	Operation
NOP	7000	1	No operation.
IAC	7001	3	Increment accumulator – the contents of the AC is incremented by 1. Carry out complements the LINK.
BSW	7002	4	Byte swap – AC0–5 are exchanged with AC6–11 respectively. The LINK is not changed.
RAL	7004	4	Rotate accumulator left – the contents of the AC and LINK are rotated one binary position to the left. AC0 is shifted to LINK and LINK is shifted to AC11.
RTL	7006	4	Rotate two left – equivalent to two RAL's.
RAR	7010	4	Rotate accumulator right – the contents of the AC and LINK are rotated one binary position to the right. AC11 is shifted into the LINK, and LINK is shifted to AC0.
RTR	7012	4	Rotate two right – equivalent to two RAR's.
R3L	7014	4	Rotate AC (but not LINK) left 3 places. AC0 is rotated into AC9, AC1 into AC10, etc.
CML	7020	2	Complement LINK – the contents of the LINK is complemented.
CMA	7040	2	Complement accumulator – the contents of the AC is replaced by its 1's complement.
CIA	7041	2, 3	Complement and increment accumulator – the contents of the AC is replaced by its 2's complement.
CLL	7100	1	Clear LINK – the LINK is made 0.
CLL RAL	7104	1, 4	Clear LINK, rotate left.
CLL RTL	7106	1, 4	Clear LINK, rotate two left.
CLL RAR	7110	1, 4	Clear LINK, rotate right.
CLL RTR	7112	1, 4	Clear LINK, rotate two right.
STL	7120	1, 2	Set the LINK – load binary 1 into LINK.
CLA	7200	1	Clear accumulator – load AC with 0000.
CLA IAC	7201	1, 3	Clear and increment accumulator – load AC with 0001.
GLK	7204	1, 4	Get LINK – place LINK in AC11; clear AC0-10 and LINK.
STA	7240	1, 2	Set accumulator – make AC=7777.
CLA CLL	7300	1	Clear AC and LINK.

Group 2 Operate Instructions

All group 2 instructions require 7 minor cycles, except OSR and LAS (8 minor cycles).

MICROINSTRUCTION FORMAT

0	1	2	3	4	5	6	7	8	9	10	11
					SMA	SZA	SNL	0			
1	1	1	1	CLA	SPA	SNA	SZL	1	OSR	HLT	0

Logical Sequence:
1 – (BIT 8=0) – SMA or SZA or SNL
– (BIT 8=1) – SPA and SNA and SZL
2 – CLA
3 – OSR, HLT

Mnemonic	Opcode	Logical Sequence	Operation
NOP	7400	1	No operation
HLT	7402	3	Set the HLTFLG. Causes entry into panel mode instead of executing the next instruction provided IIFF is not set. If IIFF is set, panel mode is entered after the JMP, JMS, RTN1 or RTN2 which clears IIFF. This instruction in panel mode does not cause a re-entry into panel mode, but does set HLTFLG.
OSR	7404	3	OR with switch register – the contents of an external device are "OR"ed with the contents of the AC, and the result stored in the AC. The contents of the DF are available for device selection.
SKP	7410	1	Skip – the content of the PC is incremented by 1, to skip the next instruction.
SNL	7420	1	Skip on non-zero LINK – skip if LINK one
SZL	7430	1	Skip if LINK zero
SZA	7440	1	Skip on zero accumulator – skip if AC=0000
SNA	7450	1	Skip on non-zero accumulator
SZA SNL	7460	1	Skip if AC=0000 or if LINK=1
SNA SZL	7470	1	Skip if AC not 0000 and if LINK is zero
SMA	7500	1	Skip on minus accumulator (ACO=1)
SPA	7510	1	Skip on positive accumulator (ACO=0)
SMA SNL	7520	1	Skip if AC is minus or if LINK is 1
SPA SZL	7530	1	Skip if AC is plus and if LINK is 0
SMA SZA	7540	1	Skip if AC is minus or zero
SPA SNA	7550	1	Skip if AC is positive and non-zero
SMA SZA SNL	7560	1	Skip if AC is minus or if AC is =0000 or if LINK is 1
SPA SNA SZL	7570	1	Skip if AC is positive, nonzero and if LINK is zero
CLA	7600	2	Clear accumulator
LAS	7604	2, 3	Load accumulator from switch register
SZA CLA	7640	1, 2	Skip if AC=0000, then clear AC
SNA CLA	7650	1, 2	Skip on non-zero accumulator, then clear AC
SMA CLA	7700	1, 2	Skip on minus AC, then clear AC
SPA CLA	7710	1, 2	Skip on positive AC, then clear AC

Group 3 Operate Instructions

If bits 6, 8, 9 or 10 are set to a one, instruction execution is not altered but the instruction becomes uninterruptable by either panel or normal interrupts. That is, the next instruction is guaranteed to be fetched barring a reset, $\overline{\text{DMAREQ}}$ or RUN/$\overline{\text{HLT}}$ flip flop in the HLT state.

Group 3 Operate Instructions

All group 3 instructions require 6 minor cycles.

MICROINSTRUCTION FORMAT

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	1	CLA	MQA	*	MQL	*	*	*	1

Logical Sequence:
1 – CLA
2 – MQA, MQL
3 – ALL OTHERS
* – CAUSES INSTRUCTION TO IGNORE INTERRUPTS IF A "1"

BIT 4	5	7	
0	0	0	NOP
0	0	1	AC→MQ, O→AC
0	1	0	(MQ + AC)→AC
0	1	1	MQ→AC
1	0	0	0→AC
1	0	1	0→AC: 0→MQ
1	1	0	MQ→AC
1	1	1	MQ→AC, 0→MQ

+ denotes logical OR

Mnemonic	Opcode	Logical Sequence	Operation
NOP	7401	3	No operation
MQL	7421	2	MQ register load – the MQ is loaded with the contents of the AC and the AC is cleared. The original contents of the MQ is lost.
MQA	7501	2	MQ "OR" with accumulator – the contents of the MQ is "OR"ed with the contents of the AC, and the result left in the AC. The MQ is not modified.
SWP	7521	3	Swap contents of AC and MQ – the contents of the AC and MQ are exchanged
CLA	7601	1	Clear accumulator
CAM	7621	3	Clear AC and MQ (actually a CLA MQL)
ACL	7701	3	Load AC with contents of MQ
CLA SWP	7721	3	Clear AC, then swap – the MQ is loaded into the AC; 0000 is loaded into the MQ

Stack Operation Instructions

The following IOT instructions are internally decoded to perform stack operations using internal stack pointers SP1 and SP2. These are internal IOT instructions; the $\overline{\text{LXDAR}}$ signal is not generated. If instructions are being fetched from main memory, the stacks are located in field 0 of main memory. If instructions are being fetched from panel memory, the stacks are located in field 0 of panel memory, except for the case of a ReTurN from control panel memory via a RTN1 or RTN2 instruction. In this case, the main memory stack is accessed by the instruction fetched from panel memory. Two separate stacks may be maintained – one for the PC, the second for the AC. An increment of the stack pointer is defined as a pop off the stack.

Mnemonic	Opcode	Operation
PPC1	6205	PUSH PC ON STACK. The contents of the PC are incremented by one and the result is loaded into the memory location pointed to by the contents of SP1. SP1 is then decremented by 1.
PPC2	6245	PUSH PC ON STACK. The same as PPC1 except that SP2 is used as the memory pointer.
PAC1	6215	PUSH AC ON STACK. The contents of the AC is loaded into the memory location pointed to by the contents of SP1. The contents of SP1 is then decremented by 1.
PAC2	6255	PUSH AC ON STACK. The same as PAC1 except that SP2 is used as the memory pointer.
RTN1	6225	RETURN. The contents of the stack pointer (SP1) is incremented by one. The contents of the Instruction Buffer (IB) is loaded into the Instruction Field (IF) register. If a prior PEX instruction was executed, the Control Panel Flip Flop (CTRLFF) is cleared. If the Interrupt Inhibit Flip Flop (IIFF) is set, then the Force Zero (FZ) flag is cleared. The contents of the memory location pointed to by SP1 is loaded into the PC. Prior PEX is cleared.
RTN2	6265	Same as RTN1 except that SP2 is used as the stack pointer.
POP1	6235	The contents of SP1 is incremented by 1. The contents of the memory location pointed to by SP1 is then loaded into the AC.
POP2	6275	Same as POP1 except that SP2 is used as the stack pointer.
RSP1	6207	The contents of SP1 is loaded into the AC.
RSP2	6227	The contents of SP2 is loaded into the AC.
LSP1	6217	The contents of the AC is loaded into SP1. The AC is cleared.
LSP2	6237	The contents of the AC is loaded into SP2. The AC is cleared.
CAUTION: When switching between main and control panel memory, the stack pointers must be saved and restored.		

Internal Control Instructions

Note that these instructions apply if the 6120 is executing instructions from main memory or control panel.

Mnemonic	Opcode	Operation
ION	6001	Turn on interrupt system. The Interrupt Enable Flip Flop is set. Neither $\overline{\text{INTREQ}}$ or any control panel request will be granted until after execution of the next instruction. (6 minor cycles.)
IOF	6002	Turn off interrupt. The interrupt enable flip flop is cleared immediately. If $\overline{\text{INTREQ}}$ is low while this instruction is being processed, the interrupt will not be recognized. (6 minor cycles.)
RTF	6005	Load the following from the AC: AC bit → To 0 → LINK 1 → GT 4 → IEFF 6-8 → IB 9-11 → DF The IIFF is set. The AC is cleared following the load operation. (8 minor cycles.)
SGT	6006	Skip if the GT flag is set. (7 minor cycles.)
CAF	6007	The AC, LINK and GT flag are cleared. Interrupt enable flip flop is cleared. $\overline{\text{IOCLR}}$ is generated with $\overline{\text{LXDAR}}$ high, causing peripheral devices to clear their flags. (7 minor cycles.)
WSR	6246	Write to switch register. The contents of the AC are written to an external device using a special I/O transfer. The AC is then cleared. The contents of the DF are available for device selection. DATAF is asserted. (7 minor cycles.)
GCF	6256	Get current fields. The following bits are loaded into the AC: AC bit → Function 0 → LINK 1 → GT flag 2 → 1 if $\overline{\text{INTREQ}}$ is low, 0 if $\overline{\text{INTREQ}}$ is high 3 → PWRON flag 4 → IEFF 5 → 0 6-8 → IF 0-2 9-11 → DF 0-2 (9 minor cycles.)

Main Memory Control Instructions

Note that these instructions apply only if the 6120 is executing instructions from main memory.

Mnemonic	Opcode	Operation
SKON	6000	Skip if interrupt on, and turn off interrupt system. (7 minor cycles.)
SRQ	6003	Skip if the device interrupt line is low. Note that this skip does not depend on the state of the memory extension control's interrupt inhibit flip flop. The SRQ merely tests the state of the $\overline{\text{INTREQ}}$ pin. (7 minor cycles.)
GTF	6004	Get flags. The following bits are loaded into the AC:

AC bit	Function
0	LINK
1	GT flag
2	1 if $\overline{\text{INTREQ}}$ is low 0 if $\overline{\text{INTREQ}}$ is high
3	PWRON flag
4	1
5	0
6-8	ISF 0-2
9-11	DSF 0-2

(9 minor cycles.)

PR0 PR1 PR2 PR3	6206 6216 6226 6236	These four opcodes have the same effect. The PNLTRP is set, causing the 6120 to enter panel mode instead of executing the next instruction, provided the interrupt inhibit flip flop is not set. If the interrupt inhibit flip flop is set, the panel mode will be entered following the JMP, JMS, RTN1 or RTN2 which clears the interrupt inhibit flip flop. These instructions are a NOP in panel mode. (6 minor cycles.)

Panel Memory Control Instructions

The 6120's control panel is implemented in software. The software implementation of the control panel need not use any part of the main memory or change the processor state. This is an important feature, since the final version of the system may not have a control panel and the system designer would like to use the entire capacity of the main memory for the specific system application.

Panel mode is entered because of the occurrence of any of four events. Each of these events sets a status flag, as well as causing the entry into panel mode. It should be noted that more than one event might happen simultaneously.

Flag	Set by	Cleared by
PWRON	$\overline{\text{RESET}}$ low and STRTUP low	PRS and PEX
PNLTRP	PRQ (main memory)	PRS and PEX
HLTFLG	HLT instruction (or any OPR2 instruction with bit 10 a 1)	PGO
BTSTRP	High-to-low transition of $\overline{\text{CPREQ}}$	PRS if BTSTRP was set when status read

Panel mode entry is functionally similar to the granting of an interrupt with some important differences. Entry into panel mode for any reason is inhibited by the interrupt inhibit flip flop. Note that this means that a PRQ or HLT instruction executed when the interrupt inhibit flip flop is set will not be recognized until after the interrupt inhibit flip flop is cleared on the next JMP, JMS, RTN1 or RTN2. Entry into panel mode is also inhibited immediately following the ION instruction but will be recognized after the instruction following the ION is executed.

When a panel request is granted, the PC is stored in location 0000 of the control panel memory and the 6120 resumes operation at location 7777 (octal) of the panel memory. During PC write, 0 appears on C0, C1 and EMA2. The states of the IB, IF, DF, ISF and DSF registers are not disturbed by entry into the control panel mode but execution is forced to commence in field zero. The panel memory would be organized with RAM in the lower pages and ROM or PROM in the higher pages of field zero. The control panel service routine would be stored in the nonvolatile ROMs, starting at 7777 (octal).

A ConTRoL panel Flip Flop, CTRLFF, which is internal to the 6120, is set when the $\overline{\text{CPREQ}}$ is granted. The CTRLFF prevents further $\overline{\text{CPREQ}}$s from being granted, bypasses the interrupt enable system and redefines several of the internal control instructions.

As long as the CTRLFF is set, $\overline{\text{LXPAR}}$ is used for all instruction, direct data and indirect pointer references. Also, while CTRLFF is set, the $\overline{\text{INTGNT}}$ line is held high but the interrupt grant flip flop is not cleared. IOTs executed while CTRLFF is set do not clear the interrupt grant flip flop.

Indirectly addressed data references by control panel AND, TAD, ISZ or DCA instructions reference panel memory or main memory as controlled by a Panel Data Flag (PDF) internal to the 6120. If set, this flag causes indirect references from control panel memory to address control panel memory using $\overline{\text{LXPAR}}$. If cleared, this flag causes indirect references from control panel memory to address main memory using $\overline{\text{LXMAR}}$.

The PDF is cleared unconditionally whenever the panel mode is entered for any reason. It is also cleared by an instruction called CPD (Clear Panel Data). The PDF is set by an instruction called SPD (Set Panel Data). The state of the Panel Data flag is ignored when not operating in panel mode.

Extended memory operations are implemented for panel mode instructions by a 1-bit flag in the EMA logic (the Force Zero – FZ – flag). This flag is always set when panel mode is entered and before the first panel mode memory operation (the store of the PC at control panel memory location 0000). As long as the FZ flag is set, zero appears on C0, C1 and EMA2 in place of the IF except for special C0, C1, EMA2 contents defined during write intervals, which remain undisturbed by FZ being set. The IF remains unchanged, however, and may be read by the RIF instruction. The data field is unaffected by the FZ flag and functions as defined above, using the panel data flag to determine whether operands are in main or control panel memory. In particular if FZ=0:

Control panel instruction fetch is to control panel field 0.

Control panel indirect address fetch is to control panel field 0.

Control panel current page or page zero direct data operations are to control panel field 0.

Control panel indirect data operations are specified by DF. Main or control panel memory access is specified by the panel data flag.

The FZ flag is cleared in panel mode simultaneously with the (IF)←(IB) transfer following the first panel mode instruction which may change the IF. These instructions are CIF (62X2), CDF CIF (62X3), RTF (6005), and RMF (6244). The (IF)←(IB) transfer (and hence the FZ clear) takes place during the first JMP, JMS, RTN1, or RTN2 following the instruction. Once the FZ flag is cleared, the EMA logic operates in control panel memory as it does in main memory with the exception that the panel data flag controls whether indirect data operations are to control panel or main memory. In particular:

Control panel instruction fetch is specified by IF.

Control panel indirect address fetch is specified by IF.

Control panel current page or page zero data operations are specified by IF.

Control panel indirect data operations are specified by DF. Main or control panel memory access is specified by the panel data flag.

Once the FZ flag is cleared in panel mode, it is not set until panel mode is entered again. The state of the FZ flag when not in panel mode is a "don't care".

Exiting from the control panel routine is normally achieved by executing the following sequence:

```
PEX
JMP I 0000   /location 0000 in control panel memory
```

The second instruction in this sequence may be any JMP, JMS, RTN1 or RTN2 instruction. The use of JMS is not recommended, since the programmer has no means of preserving the FZ and panel data flags.

The PEX instruction will cause the next JMP, JMS, RTN1 or RTN2 instruction to reset the CTRLFF. Location 0000 in the control panel memory contains either the original return address deposited by the 6120 when the control panel routine was entered or it may be a new starting address defined by the control panel routine. The IF and DF registers may also contain their original field designations or may have been altered by the control panel routine. If an exit is made from the control panel routine with the HLTFLG set, one instruction is executed in main memory before control panel mode is reentered due to the HLTFLG being set. Note that this allows a software-controlled single step operation of programs in main memory. Caution: Single step operation will not occur for any uninterruptable instructions or any instructions which set the IIFF. Exiting from a control panel routine can also be achieved by activating the $\overline{\text{RESET}}$ line, since reset has a higher priority than control panel request. If the RUN/$\overline{\text{HLT}}$ line is pulsed while the 6120 is in the panel mode, the 6120 will halt at the completion of the current instruction.

Panel Mode Control Instructions

Note that these instructions apply only if the 6120 is executing instructions from Control Panel Memory

<table>
<tr><th>Mnemonic</th><th>Opcode</th><th>Description</th></tr>
<tr><td>PRS</td><td>6000</td><td>Read panel status bits into AC0-4, 0 into remainder of AC.
The bits are read as follows:
<table>
<tr><th>AC bit</th><th>Function</th></tr>
<tr><td>0</td><td>BTSTRP</td></tr>
<tr><td>1</td><td>PNLTRP</td></tr>
<tr><td>2</td><td>1 if $\overline{\text{INTREQ}}$ is low
0 if $\overline{\text{INTREQ}}$ is high</td></tr>
<tr><td>3</td><td>PWRON</td></tr>
<tr><td>4</td><td>HLTFLG</td></tr>
<tr><td>5-11</td><td>0</td></tr>
</table>
Following the reading of the flags into the AC, the flags are cleared, with the exception of HLTFLG. BTSTRP is cleared only if a 1 was read into AC0. (8 minor cycles).</td></tr>
<tr><td>PG0</td><td>6003</td><td>Reset the HLTFLG flip flop. (6 minor cycles).</td></tr>
<tr><td>PEX</td><td>6004</td><td>Exit from panel mode into main memory at the end of the next JMP, JMS, RTN1 or RTN2 instruction. Clear PWRON and PNLTRP. (6 minor cycles).</td></tr>
<tr><td>CPD</td><td>6266</td><td>Clear Panel Data Flag (PDF). Clears the panel data flag so that indirect data operands of panel mode instructions are obtained from main memory. The panel data flag is also cleared upon entry into panel memory. (5 minor cycles).</td></tr>
<tr><td>SPD</td><td>6276</td><td>Set panel data flag. Sets the panel data flag so that indirect data operands of panel mode instructions are obtained from panel memory. (5 minor cycles).</td></tr>
</table>

Memory Extension Instructions

Most memory extension instructions require 6 minor cycles, except for RIB which requires 9 minor cycles.

The internal memory extension control extends the basic 4K addressing structure of the 6120 to 32K. It does so by appending three high-order bits to the memory address. These bits, which appear on C0, C1 and EMA2 lines, apply to addresses within main memory or control panel memory. The changing of memory fields is accomplished via internal control instructions.

The Instruction Field (IF) serves as an extension to the PC, providing three high-order bits during instruction fetches. Note that there is no carry from the most-significant PC bit into the IF. The IF is also used for directly-addressed operands, and for indirect address pointers.

The Data Field (DF) serves to extend the address of indirectly addressed operands, external IOTs, OSR and WSR functions.

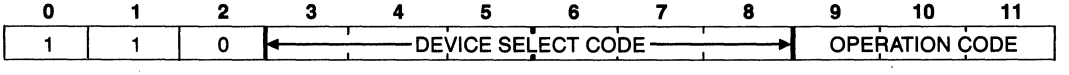
The Instruction Save Field and Data Save Field are used to retain the contents of the IF and the DF which existed prior to an interrupt.

Mnemonic	Opcode	Operation
CDF	62X1	Change Data Field to X. X is loaded into DF.
CIF	62X2	Change Instruction Field to X. X is loaded into IB, and the IIFF is set. (The set state IIFF causes the priority network to ignore interrupt requests). The contents of IB are loaded into the IF at the end of the next JMP, JMS, RTN1 or RTN2 instruction. At the same time the interrupt inhibit flip flop is cleared.
CDF CIF	62X3	A microprogrammed combination of CDF and CIF. Both fields are set to X.
RDF	6214	Load the contents of the Data Field register into bits 6-8 of the AC. DF0-2 goes to AC6-8 respectively. AC0-5 and 9-11 are unchanged.
RIF	6224	Load the contents of the Instruction Field register into bits 6-8 of the AC. IF0-2 goes to AC6-8 respectively. AC0-5 and 9-11 are unchanged.
RIB	6234	Load the contents of the ISF and DSF into bits 6-11 of the AC. ISF0-2 goes to AC6-8 and DSF0-2 goes to AC9-11 respectively. AC0-5 are unchanged.
RMF	6244	Load the contents of ISF into IB, DSF into DF, and set the interrupt inhibit flip flop. This instruction is used to restore the contents of the memory field registers to their values before an interrupt occurred.

Input/Output Instructions

Input/output transfer instructions, which have an opcode of 6, are used to initiate the operation of peripheral devices and to transfer data between peripherals and the 6120. Three types of data transfer may be used to receive or transmit information between the 6120 and one or more peripheral I/O devices. Programmed data transfer provides a straight-forward means of communicating with relatively slow I/O devices, such as teletypes, cassettes, card readers and CRT displays. Interrupt transfers use the interrupt system to service several peripheral devices simultaneously, on an intermittent basis, permitting computational operations to be performed concurrently with I/O operations. Both programmed data transfers and program interrupt transfers use the accumulator as a buffer, or storage area, for all data transfers.

IOT INSTRUCTION FORMAT



Bits 0-2 are always set to 6 (110) to specify an IOT instruction. The next six bits, 3-8, contain the device selection code that determines the specific I/O device for which the IOT instruction is intended. Device selection codes 00 and 2X specify internal operations, and may not be used by external devices. Up to 55 I/O devices can be specified. The last three bits, 9-11, contain the operation specification code that determines the specific operation to be performed. The nature of this operation for any given IOT instruction depends entirely upon the circuitry designed into the I/O device interface (see the 6121 specification).

Programmed data transfer begins when the 6120 fetches an instruction from the memory and recognizes that the current instruction is an external IOT. The 6120 sequences the IOT instruction through an execute phase. Bits 0-11 of the IOT instruction are placed on DX0-11; the data field is placed on C0, C1 and EMA2; and $\overline{\text{DATAF}}$ is asserted. $\overline{\text{LXDAR}}$ then falls, signalling the beginning of the IOT execute phase. These bits must be latched in an external register, since they are then removed to free the DX bus for I/O data exchanges. Following the fall of $\overline{\text{LXDAR}}$, the 6120 generates a write signal. During the $\overline{\text{WRITE}}$, the 6120 reads the $\overline{\text{SKIP}}$, C0 and C1 lines. $\overline{\text{SKIP}}$, C0, and C1 define the type of I/O operation. If C1 is pulled low during the write signal, then the 6120 adds one minor cycle and performs a read operation after the write.

The control line $\overline{\text{SKIP}}$, when low during the write portion of an IOT, causes the 6120 to skip the next instruction. This feature is used to sense the status of various signals in the device interface. The C0 and C1 lines are treated independently of the $\overline{\text{SKIP}}$ line.

Programmed I/O Control Lines

External programmed data transfers require 10 minor cycles if there is a read, 9 if not.

Control Lines C0	C1	Operation	Description
High	High	(Device)←(AC)	The contents of the AC is sent to the device.
Low	High	(Device)←(AC), CLA	The contents of the AC is sent to the device; then the AC is cleared.
High	Low	(AC)←(AC)V(Device)	Data is received from a device, "OR"ed with the data in the AC, and the result is stored in the AC.
Low	Low	(AC)←(Device)	Data is received from a device and loaded into the AC.

Interrupt Transfer

The program interrupt system may be used to initiate programmed data transfers in such a way that the time spent waiting for device status is greatly reduced. It also provides a means of performing programmed data transfers between the 6120 and peripheral devices while executing another program. This is accomplished by isolating the I/O handling routines from the mainline program and using the interrupt system to ensure that these routines are entered only when an I/O device is set, indicating that the device is actually ready to perform the next data transfer.

The interrupt system allows external conditions to interrupt the computer program (which must be in main memory) by driving INTREQ low. If no internal higher priority requests are outstanding and the interrupt system is enabled, the 6120 grants the device interrupt at the end of the current instruction. After an interrupt has been granted, the interrupt enable flip flop in the 6120 is reset so that no more interrupts are acknowledged until the interrupt system is re-enabled under program control.

The interrupt inhibit flip flop prevents interrupts (both device and control panel) from occurring when there is a possibility that the IF is not equal to the IB. More specifically, the interrupt inhibit flip flop is set whenever the IB is loaded (i.e., by the instructions CIF, CDF CIF, RMF or RTF), and cleared whenever the IF is loaded from the IB (i.e., at the proper phase of JMP, JMS, RTN1 or RTN2 instructions). Device interrupts are recognized only if the interrupt system is enabled, the interrupt inhibit flip flop is cleared and INTREQ is low.

Upon recognition of an interrupt, the 6120 stores the PC in location 0000 of field 0 and clears the interrupt enable flip flop. Zero appears on C0, C1 and EMA2 when the PC is stored. At the same time, INTGNT goes low. During the interrupt grant sequence, IF is loaded into ISF and DF is loaded into DSF. IF, IB and DF are then cleared. The next instruction is fetched from location 0001 of main memory field 0. INTGNT remains low until the trailing edge of the first LXDAR generated by a main memory IOT following the recognition of the interrupt. The granting of an interrupt requires 4 minor cycles. If a control panel interrupt is granted while INTGNT is low, INTGNT will be forced high as long as CTRLFF is set but will return to the low state when CTRLFF is cleared.

Direct Memory Access

Direct memory access, sometimes called data break, is the preferred form of data transfer to use with high-speed storage devices such as magnetic disk or tape units. The DMA mechanism transfers data directly between memory and peripheral devices. The 6120 is involved only in setting up the transfer; the transfers take place with no 6120 intervention on a "cycle stealing" basis. The DMA transfer rate is limited only by the bandwidth of the memory and the data transfer characteristics of the device.

The external device generates a DMA request when it is ready to transfer data. The 6120 grants the DMAREQ by pulling the DMAGNT signal high at any point in any of the instructions, or between instructions, when the 6120 is not using the DX bus in performing a bus read, write or read-modify-write operation. The 6120 suspends its internal timing until the DMAREQ line is high. The DX lines, EMA2, C0 and C1 lines are tristated. LXPAR, LXMAR, MEMSEL, OUT, READ and WRITE are all held high by a device on each of these lines which only has a very small pull-up drive. These lines can then be pulled down by an external device. In this way, these control lines are stable until the external device can gain control of them. IFETCH and LXDAR are both held high. RUN is held low. The states of DATAF and INTGNT are undisturbed.

The external DMA device must not drive the bus until DMAGNT is high. The DMA device must:

a. Drive all signals with three-state devices.
b. Provide all address, data, LXPAR, LXMAR, and other control signals with the proper timing.
c. Return all control lines to the high state before relinquishing the bus.
d. Three-state all drivers at or before DMAREQ is pulled high by the device.

After the DMAREQ line is pulled high, the 6120 negates DMAGNT and re-establishes proper timing before proceeding.

Internal Flags

Name	Set Conditions	Clear Conditions	Load Conditions	Comments
IEFF	ION inst.	1. RESET=low 2. IOF inst. 3. During INTGNT sequence 4. SKON inst.	RTF inst.	INTERRUPT ENABLE FLIP FLOP: Tested by the SKON instruction. GCF inst. loads state of IEFF into AC4. INTREQ is honored only if IEFF is set (1).
IIFF	1. CIF inst. 2. CIF CDF 3. RMF 4. RTF	1. RESET=low 2. JMP, JMS, RTN inst.	none	INTERRUPT INHIBIT FLIP FLOP: Suppresses any INTREQ or Control Panel mode request.
CTRLFF	Upon entry into panel mode	1. RESET=low 2. Next JMP, JMS or RTN after PEX inst.	none	CONTROL PANEL FLIP FLOP: Indicates control panel operation. Interrupts are not honored when set.
FZ	Upon entry into panel mode	First JMP, JMS or RTN inst. executed with IIFF set.	none	FORCE ZERO FLAG: Forces control panel instruction field access to field zero. Indirect data accesses are not affected.
PDF	SPD inst.	1. Panel mode entry 2. CPD inst.	none	PANEL DATA FLAG: When set causes indirect data operations executed in control panel to access CP memory. Otherwise they are to main memory. PDF is ignored when executing in main memory.
RUNHLT	RESET=low	none	On the low to high transition of the RUN/HLT line	RUN HALT FLIP FLOP: When cleared the 6120 will halt after the first instruction in which this state is detected. The 6120 will respond to DMAREQ in this state.
HLTFLG	HLT inst.	1. RESET=low 2. PG0 inst.	none	HALT FLAG: When set, panel mode will be entered unless the IIFF is set or RESET is low. IIFF can be cleared on the next JMP, JMS or RTN instruction at which point panel mode will be entered.
PNLTRP	PR0, PR1, PR2, PR3 inst. (main only)	1. RESET=low 2. PRS inst. 3. PEX inst.	none	PANEL TRAP FLAG: Same result as defined for HLTFLG.
BTSTRP	High to low transition of CPREQ	1. RESET=low 2. PRS inst.	none	BOOTSTRAP FLAG: Same result as defined for HLTFLG.
PWRON	RESET and STRTUP=low	1. RESET and STRTUP=high 2. PRS inst. 3. PEX inst.	none	POWER-ON FLAG: Causes entry into panel mode when RESET is released and this flag is set.
GT	none	RESET=low	RTF inst.	GREATER THAN FLAG: General purpose flag which has no arithmetic significance.

HARRIS

HD-6121

CMOS I/O CONTROLLER

Features

- LOW POWER, TYP. < 2 mW
- SINGLE SUPPLY – 5V
- INDUSTRIAL AND MILITARY TEMPERATURE RANGES
- 6120 COMPATIBLE INTERFACE
- CONTROLS ANY COMBINATION OF FIVE INPUT OR OUTPUT PORTS WITH HANDSHAKING
- ELIMINATES GATED READ AND WRITE SIGNALS THROUGH THE CONTROLLER
- CONFORMS TO DEC* CONVENTIONS REGARDING DEVICE ADDRESSING AND COMMANDS
- INDEPENDENT PROGRAMMING OF EACH DEVICE'S ADDRESS AND DATA DIRECTION
- COMPLETE INTERRUPT AND SKIP LOGIC FOR EACH DEVICE INCLUDING PRIORITY INTERRUPT VECTORING
- STROBE OUTPUTS ARE PROGRAMMABLE HIGH OR LOW TRUE
- SENSE INPUTS ARE PROGRAMMABLE FOR LEVEL OR EDGE SENSITIVITY
- ENABLE OUTPUTS FUNCTION AS USER PROGRAMMABLE CHIP SELECTS

Description

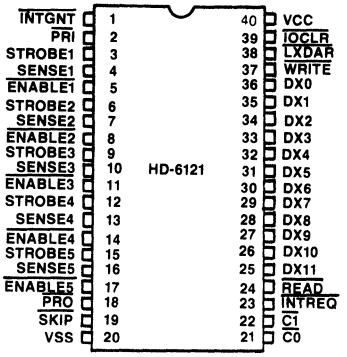
The HD-6121 Input/Output Controller (IOC) is a high performance, CMOS support circuit for the 6120 microprocessor. Fully programmable, this device offers independent control of any combination of five, 12 bit input or output ports.

Used in conjunction with the 6120 microprocessor, the 6121 provides user programmable chip select decoding, priority vectored interrupt control, software readable status and I/O port handshaking signals.

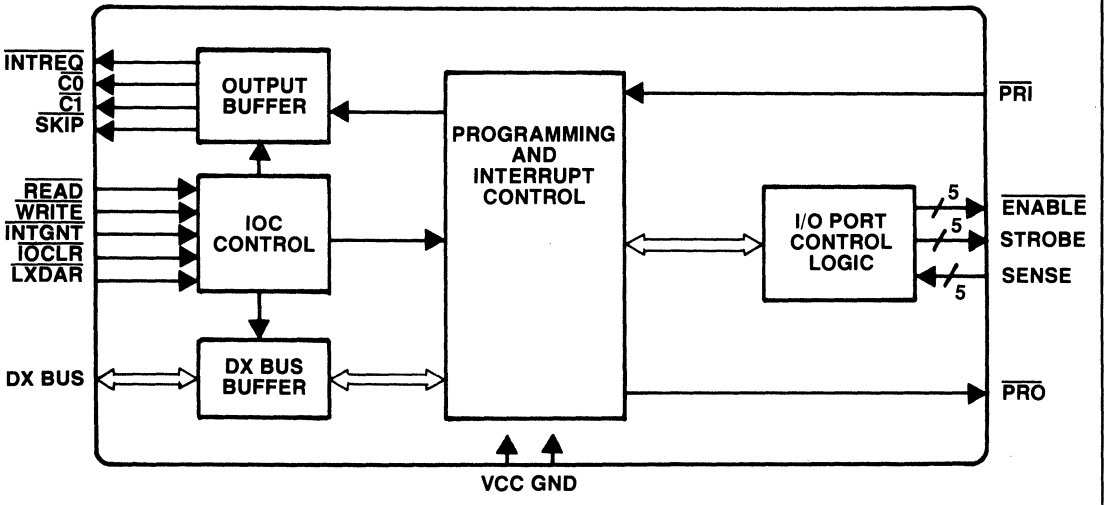
The Priority In ($\overline{PRI}$) and Priority Out ($\overline{PRO}$) control signals permit up to eleven 6121s to be used without any additional hardware. Industrial control and other I/O intensive systems can profit greatly from the highly hardware/software efficient capability provided by the 6120/6121 chip set.

* *TRADEMARK of Digital Equipment Corp.*

Pinout



Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0 VOLTS	Operating Temperature Range	
Operating Voltage Range	+4V to +7V	Industrial (−9, −9+)	−40°C to +85°C
Input/Output Voltage Applied	VSS−0.3V to VCC+0.3V	Military (−2, −8)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	Maximum Power Dissipation	1 Watt

CAUTION: Stresses above those listed in the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. ELECTRICAL CHARACTERISTICS; VCC=5.0V±5%; T_A = Industrial or Military

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	LOGICAL ONE INPUT VOLTAGE	70% VCC		V	
VIL	LOGICAL ZERO INPUT VOLTAGE		30% VCC	V	
VOH	LOGICAL ONE OUTPUT VOLTAGE	VCC−0.5		V	IOH = −1.6mA Except for SKIP, $\overline{\text{INTREQ}}$, $\overline{\text{C0}}$ and $\overline{\text{C1}}$ which are open drain.
VOL	LOGICAL ZERO OUTPUT VOLTAGE		0.5	V	IOL = 1.6mA Except for $\overline{\text{SKIP}}$, $\overline{\text{INTREQ}}$, $\overline{\text{C0}}$ and $\overline{\text{C1}}$.
VOL	LOGICAL ZERO OUTPUT VOLTAGE		0.5	V	IOL = 15 mA $\overline{\text{SKIP}}$, $\overline{\text{INTREQ}}$, $\overline{\text{C0}}$, $\overline{\text{C1}}$ OUTPUTS
IIL	INPUT LEAKAGE CURRENT	−10	10	μA	OV≤VIN≤VCC
IO	I/O, OUTPUT LEAKAGE CURRENT	−10	10	μA	OV≤VO≤VCC NOTE 1
ICC	POWER SUPPLY CURRENT		100	μA	VIN=VCC or GND VCC = 5.25 V OUTPUTS OPEN
CIN*	INPUT CAPACITANCE		5	pF	FREQ = 1 MHZ TA=25°C VIN=VCC or GND
COUT*	OUTPUT CAPACITANCE		15	pF	FREQ = 1 MHZ TA=25°C VIN=VCC or GND

** Guaranteed and sampled, but not 100% tested*

NOTE 1: APPLIES ONLY TO DX0 THROUGH DX11, $\overline{\text{C0}}$, $\overline{\text{C1}}$, $\overline{\text{SKIP}}$, AND $\overline{\text{INTREQ}}$ WITH THE OUTPUT DRIVERS DISABLED OR OPEN DRAIN OUTPUTS OFF.

A.C. ELECTRICAL CHARACTERISTICS; VCC=5.0V±5%; T_A=Industrial or Military; C_L=50 pf,

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TAS	ADDRESS SET UP TIME	30		ns	
TAH	ADDRESS HOLD TIME	70		ns	
TRWE	WRITE ENABLE DELAY		100	ns	
TRWD	WRITE DISABLE DELAY		100	ns	
TWS	WRITE SET UP TIME	50		ns	
TWH	WRITE HOLD TIME	50		ns	
TPDE	ENABLE OUTPUT DELAY		125	ns	
TPDD	ENABLE OUTPUT DISABLE DELAY		200	ns	
TRE	READ VECTOR ENABLE		100	ns	
TRD	READ VECTOR DISABLE		100	ns	
TWPD	WRITE PULSE DELAY	100		ns	
TLXH	RESET DELAY, IOCLR TO LXDAR	100		ns	

NOTE: ALL MEASUREMENTS ARE TAKEN WITH INPUT RISE AND FALL TIMES ≤ 20 NSEC

DECOUPLING CAPACITORS

The transient current required to charge and discharge the 50 pf load capacitance specified in the 6121 data sheet is determined by

$$i = C_L (dv/dt)$$

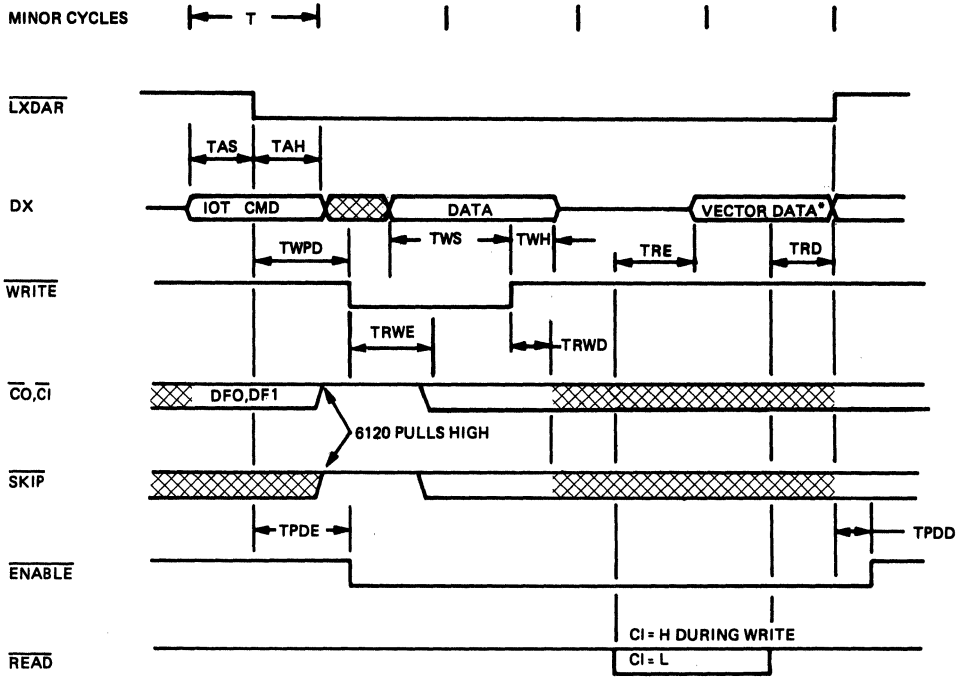
Assuming that all DX outputs change state at the same time and that dv/dt is constant;

$$i \cong C_L \frac{(VCC \times 80\%)}{t_R/t_F}$$

where t_R=20 ns, VCC=5.0 volts, C_L=50 pF on each of twelve outputs.

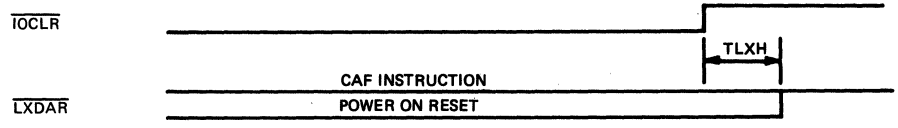
$$i \cong (12 \times 50 \times 10^{-12}) \times (5.0v \times 0.8)/(20 \times 10^{-9})$$
$$\cong 120 \text{ mA}$$

This current spike may cause a large negative voltage spike on VCC, which could cause improper operation of the device. To filter out this noise, it is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between VCC and GND at each device, with placement being as near to the device as possible.



** Vector Operation Only*

EXTERNAL IOT and VECTORED INTERRUPT OPERATION



RESET TIMING

I/O	PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
I	1	$\overline{\text{INTGNT}}$	Low	Interrupt grant signal from the 6120.
I	2	$\overline{\text{PRI}}$	Low	Input for priority string. Low implies no higher priority up the string. Device #1 internally is the highest priority device.
O	3, 6, 9, 12, 15	STROBE 1-5	High or Low	Output strobes set true by a transfer command. Cleared by a Set Flag command or by the corresponding sense input going true. Programmable polarity.
I	4, 7, 10, 13, 16	SENSE 1-5	High or Low	Status inputs from an external device. Can cause IOT skips or interrupts. Programmable edge or level sense and polarity.
O	5, 8, 11, 14, 17	$\overline{\text{ENABLE}}$ 1-5	Low	Bus transfer enable pulses for external devices. True during $\overline{\text{LXDAR}}$.
O	18	$\overline{\text{PRO}}$	Low	Output for priority string. Low implies enable for next device down the string. Device #5 internally is the lowest priority device and drives this output.
O	19	$\overline{\text{SKIP}}$	Low	True during $\overline{\text{LXDAR}}$ and $\overline{\text{WRITE}}$ to indicate to the 6120 that a skip is to occur on the current IOT. N-Channel open drain.
	20	VSS		Power supply ground.
O	21, 22	$\overline{\text{C0}}$, $\overline{\text{C1}}$	Low	Control signals to the 6120 which specify the type of transfer required for an I/O instruction. See Table 1. N-Channel open drain.
O	23	$\overline{\text{INTREQ}}$	Low	Interrupt request to the 6120. N-Channel open drain output.
I	24	$\overline{\text{READ}}$	Low	6120 bus read pulse.
I/O	25-36	DX11-0	High	6120 data/address bus. (DXO=MSB, DX11=LSB)
I	37	$\overline{\text{WRITE}}$	Low	6120 bus write pulse.
I	38	$\overline{\text{LXDAR}}$	Low	6120 I/O transfer enable signal. True during the execute phase of external IOT instruction. Also true during power on reset.
I	39	$\overline{\text{IOCLR}}$	Low	Reset from the 6120 generated by power on reset or CAF instruction.
	40	VCC		Positive supply voltage.

CONCEPT:

The concept of the IOC is to provide basic control and enable signals for the devices which it controls but not be involved in the critical speed timing of the DX bus transfers to and from these devices. Each input or output port still has its own output latch or input driver interface which results in maximum flexibility with regard to I/O device characteristics. Because these latches and input drivers are not included in the 6121, this 40 pin device is able to provide complete handshaking for five I/O ports.

Software programmable chip select decoding ($\overline{\text{ENABLE}}$ outputs) provides a means whereby I/O device addressing is readily changed with no change to the users PC board. This on-chip feature replaces the 2-5 IC's normally associated with chip select decoding.

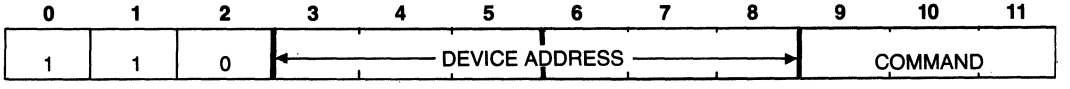
Another feature of the 6121 IOC is an on-chip priority interrupt controller. The interrupt logic includes software programmable vectors and complete interrupt request/grant handshaking for the 6120 microprocessor. This on-chip feature of the 6121 eliminates a separate interrupt controller IC. Up to eleven 6121 IOCs can be daisy chained without the need for any interfacing logic. This results in vectored interrupt control of up to 55 I/O ports. The Priority In ($\overline{\text{PRI}}$) and Priority Out ($\overline{\text{PRO}}$) control signals are used for this I/O expansion capability.

Another major on-chip feature of the 6121 IOC is the inclusion of I/O port handshaking signals. These signals provide the capability of polling the status of an Input port (SENSE inputs) and that of signaling an Output port that it has received data (STROBE outputs). These signals can be thought of as "Input Buffer Full" and "Output Buffer Full" status lines. The characteristics of these signals are software programmable which greatly increases their flexibility.

6120 IOT INSTRUCTION SEQUENCING:

The 6121 is designed to interface with the 6120 external IOT sequence. This sequence begins when the 6120 fetches an instruction from the memory and recognizes that the current instruction is an external IOT. An external IOT is any IOT (Bits 0−2=6) whose device code (Bits 3-8) is not 00 or 2X.

EXTERNAL IOT COMMAND FORMAT



The 6120 sequences the IOT instruction through an execute phase. Bits 0-11 of the IOT instruction are available on DX0-11 as $\overline{\text{LXDAR}}$ falls near the start of the execute phase. The 6121 IOC accepts the IOT command on the falling edge of $\overline{\text{LXDAR}}$ and latches this information into an internal command latch. $\overline{\text{WRITE}}$ or $\overline{\text{READ}}$ is active low to enable data transfers between the 6120 and the peripheral device(s). The 6121 communicates with the 6120 through 3 control lines... $\overline{\text{C0}}$, $\overline{\text{C1}}$ and $\overline{\text{SKIP}}$. The type of data transfer during an IOT instruction is specified by the peripheral device by asserting the control lines as shown in Table 1.

The control line $\overline{\text{SKIP}}$, when low during an IOT, causes the 6120 to skip the next instruction. This feature is used to sense the status of various signals in the device interface. The $\overline{\text{C0}}$ and $\overline{\text{C1}}$ lines are treated independently of the $\overline{\text{SKIP}}$ line. The input command signals, $\overline{\text{C0}}$, $\overline{\text{C1}}$ and $\overline{\text{SKIP}}$, are sampled during $\overline{\text{LXDAR}}$ low • $\overline{\text{WRITE}}$ low. The data from the 6120 is available to the device(s) during $\overline{\text{LXDAR}}$ low • $\overline{\text{WRITE}}$ low. If $\overline{\text{C1}}$ is low at $\overline{\text{LXDAR}}$ low • $\overline{\text{WRITE}}$ low, a read is also performed and data is read from the peripheral into the 6120 during $\overline{\text{LXDAR}}$ low • $\overline{\text{READ}}$ low.

TABLE 1 – PROGRAMMED I/O CONTROL LINES

CONTROL LINES $\overline{\text{C0}}$	$\overline{\text{C1}}$	OPERATION	DESCRIPTION
High	High	(Device)◄—(AC)	The contents of the AC is sent to the device.
Low	High	(Device)◄—(AC), Clear (AC)	The contents of the AC is sent to the device, then the AC is cleared.
High	Low	(AC)◄—(AC)V(Device)	Data is received from a device,"OR'ed" with the data in the AC and the result stored in the AC.
Low	Low	(AC)◄—(Device)	Data is received from a device and loaded into the AC.

INTERNAL DEVICE CONTROLLER FLIP FLOP DEFINITIONS:

There are five device controllers within the 6121 IOC. Each controller has a set of control and status flip flops which are defined below:

FLAG FLIP FLOP – Internal device control status flip flop which only has meaning if the IS programming bit is a 1. It is set by a SET FLAG IOT or by true going edge of sense input. It is cleared by the SKIP ON FLAG instruction only if it was sampled by that instruction as being set; by the interrupt vector operation; or by $\overline{\text{IOCLR}}$. If the flag is set, interrupts can be generated if otherwise enabled. If the IS programming bit is 0, the flag flip flop is held in the cleared state.

FLAG SAMPLE FLIP FLOP – Internal device control flip flop which samples the state of the flag flip flop at the falling edge of $\overline{\text{LXDAR}}$. The set state of this flip flop causes the skip line to be pulled and the flag flip flop to be cleared during $\overline{\text{WRITE}}$ pulses of a skip IOT.

STROBE FLIP FLOP – Internal device control flip flop which controls strobe output line. It is set by a transfer IOT at the trailing edge of the $\overline{\text{LXDAR}}$ pulse. It is cleared by $\overline{\text{IOCLR}}$, the true going edge of the sense input (if the IS programming bit set) or the SET FLAG IOT command. The STROBE output reflects the state of this flip flop any time the strobe flip flop is cleared or at the end of $\overline{\text{LXDAR}}$ if the strobe flip flop is set.

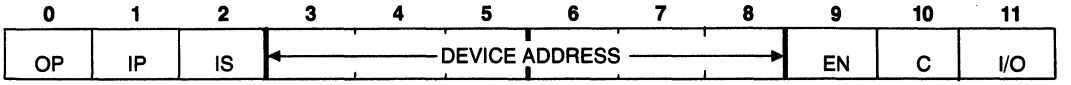
INTERRUPT ENABLE FLIP FLOP – Internal device control flip flop which allows program enable of interrupts. This bit is set by $\overline{\text{IOCLR}}$. This bit is loaded by DX11 during $\overline{\text{WRITE}}$ of LOAD INTERRUPT ENABLE IOT. If this flip flop and the flag flip flop are both set, then the $\overline{\text{INTREQ}}$ pin is pulled low.

INTERRUPT SAMPLE FLIP FLOP – Internal device control flip flop which samples the state of the interrupt condition at the falling edge of $\overline{\text{INTGNT}}$. The falling edge of $\overline{\text{INTGNT}}$ sets the interrupt sample flip flop if the flag flip flop and interrupt enable flip flop are set and the priority input is true. If the flag flip flop is clear or the priority input is false at the fall of $\overline{\text{INTGNT}}$, the state of the interrupt sample flip flop is not changed. The interrupt sample flip flop is cleared by the SKIP ON FLAG IOT, by the reset state of the interrupt enable flip flop or by $\overline{\text{IOCLR}}$. If this flip flop is set, the device's priority output is false (high).

PROGRAMMING:

Immediately after power on reset, the five device controllers within the IOC are set to a state such that the first IOT command received with $\overline{\text{PRI}}$ low will be interpreted as a programming command to set up various IOC parameters. This is true only for power on reset and is *not* true for the reset generated by the 6120 CAF instruction. Power on reset from the 6120 is distinguished by $\overline{\text{LXDAR}}$ being low at the end of the $\overline{\text{IOCLR}}$ pulse. During the reset caused by the CAF instruction, $\overline{\text{LXDAR}}$ is high throughout the $\overline{\text{IOCLR}}$ pulse. Each of the five device controllers within the IOC are programmed independently by separate IOT commands. If PRI is low, the first IOT programs the highest priority device (Device #1). The second IOT programs the second highest priority device (Device #2). This continues until all the devices in the IOC are programmed, at which time $\overline{\text{PRO}}$ is made low so that programming can commence on the next IOC (if any) down the priority chain. The IOC will not accept any operational IOT commands to any of the five devices until all five devices have been programmed. The programming IOT writes data from the 6120 accumulator. The lower 9 bits of the IOT instruction itself perform no programming function. The IOT instruction must be an external IOT, not device #00 or 2X. The programming format from the accumulator is shown below:

PROGRAMMING COMMAND FORMAT



OP Output polarity
1=High true strobe output
0=Low true strobe output

IP Input polarity
1=High true sense polarity
0=Low true sense polarity

IS Input edge sensitivity
1=Set flag flip flop and interrupt (if interrupts enabled) on true-going edge of sense input. Skip on flag flip flop set.
0=Skip on sense line input level true. (No interrupt on sense true.)

DEVICE ADDRESS The 6 bit device address assigned to the device controller.

EN Enable output control select.
1=Enable output is true (low) whenever the device is addressed. (Except for programming and vector operations.)
0=Enable is true only when a transfer command (4_8 or 6_8) is given.

C C line control.
0=Transfer commands do not cause C lines to be controlled.
1=Transfer commands cause C lines to be controlled.

I/O Input or output port select. This programming bit has no meaning if the "C" programming bit is set to a "0".
1=Transfer commands cause outputs to the device. ($\overline{C1}$ is not pulled low.)
0=Transfer commands cause inputs from the device. ($\overline{C1}$ is pulled low.)

After all five devices of the IOC are programmed, they are ready to respond to IOT commands with their programmed addresses. Because of this, no operational IOT commands can be used until all system IOC's have been programmed. An additional constraint is that each device must have its own unique address.

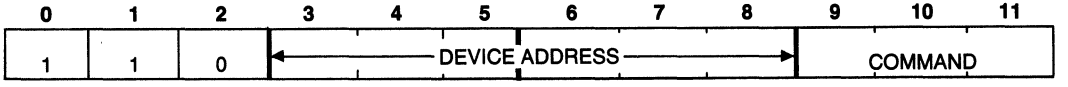
Note that unused devices must be turned off during programming simply by programming them with an internal IOT address (00 or 2X), and with the IS programming bit set to "0" to prevent interrupts. Also, sense inputs must be tied to ground. Internal 6120 IOT's do not generate $\overline{LXDAR}$. The IOT controller is therefore made insensitive to all external IOT commands when programmed with an internal IOT address. Whenever a device controller within the IOC responds to its programming IOT, it pulls the $\overline{C0}$ line low so that the 6120 will perform an output operation from the AC followed by clearing the AC.

IOC COMMANDS:

Power on reset– This is indicated by the $\overline{IOCLR}$ input low and $\overline{LXDAR}$ low at the end of the $\overline{IOCLR}$ pulse. This operation sets up the IOC to be programmed as discussed above. Also, all five flag flip flops are cleared as are the flag sample and interrupt sample flip flops. The interrupt enable flip flops are all set. The strobe flip flops are cleared, the STROBE outputs are set low and the $\overline{ENABLE}$ outputs are set high. Note that if a controller is programmed for a low true STROBE output, then there will be a low to high transition on the strobe output when this device is programmed. Also, care must be taken to assure that the state of the flag, flag sample, interrupt sample, interrupt inhibit and strobe flip flops are *not* disturbed by the programming function.

The 6120 Clear All Flags (CAF) Instruction – This instruction is indicated to the IOC by $\overline{IOCLR}$ going low and $\overline{LXDAR}$ staying high during the $\overline{IOCLR}$ pulse. This operation performs exactly the same operation as power on reset on the device flag, flag sample, interrupt sample, interrupt enable and strobe flip flops. It does not set up the IOC for programming, nor does it disturb the state of any of the programming information stored within the IOC.

EXTERNAL IOT COMMAND FORMAT



	Bit 9	10	11
SET FLAG, CLEAR STROBE	0	0	0
SKIP ON FLAG, CLEAR FLAG	0	0	1
CLEAR ACCUMULATOR (If programmed for input)	0	1	0
NOP	0	1	1
DATA TRANSFER ($\overline{C0}$ not pulled low)	1	0	0
LOAD INTERRUPT ENABLE (From DX11)	1	0	1
DATA TRANSFER ($\overline{C0}$ pulled low)	1	1	0
NOP	1	1	1

Each IOT is discussed below:

SET FLAG, CLEAR STROBE – If the device is programmed for edge sensitive SENSE input, this IOT command causes the internal flag flip flop to be set and also clears the STROBE output to the programmed false state. If the device is programmed for level sensitive SENSE input, then the flag flip flop is not set by this instruction, but the STROBE output is cleared.

SKIP ON FLAG, CLEAR FLAG – The skip on flag operation depends on whether the device is programmed for edge or level sensitivity. If programmed for level sensitivity and the SENSE input is logic true, then the $\overline{SKIP}$ line is pulled low during the IOT $\overline{WRITE}$ pulse; the clear flag operation has no meaning. If programmed for edge sensitivity, then the state of the flag flip flop is sampled to the flag sample flip flop at the falling edge of $\overline{LXDAR}$. During the IOT $\overline{WRITE}$ pulse, the $\overline{SKIP}$ line will be pulled low if the flag sample flip flop is true. If the flag sample flip flop is set, then the flag flip flop will be cleared some time before or at the trailing edge of $\overline{LXDAR}$.

CLEAR ACCUMULATOR – This command only functions if the C line control programming bit (bit 10=1) has been programmed for the device to control the C lines and the device has been programmed as an input device (bit 11=0). When enabled by the above two programming conditions, this command will cause $\overline{C0}$ to be pulled low during the IOT $\overline{WRITE}$ pulse. This will cause the 6120 accumulator to be cleared.

DATA TRANSFER (4_8 or 6_8) – Either transfer command will unconditionally set the STROBE output to its true state. If the "C" programming bit is set, the transfer commands will also cause the "C" lines to be controlled to specify the type of I/O transfer to be performed. If not, then the IOC device does not control the "C" lines. If the device "I/O" programming bit is 1, then $\overline{C1}$ is not pulled low and an output transfer is specified by either 4_8 or 6_8. If the I/O programming bit is 0, then an input transfer is specified by pulling $\overline{C1}$ low during the $\overline{WRITE}$ pulse. Command 4_8 does not pull $\overline{C0}$ low. For an output, this corresponds to not clearing the AC after the output. For an input, this corresponds to "OR'ing" the input data with the AC. Command 6_8 always pulls $\overline{C0}$ low. For an output, this causes the AC to be cleared following the output. For an input, this corresponds to the input data being loaded into the AC. The STROBE output is cleared when the flag flip flop is set by the SENSE transition or by a SET FLAG command.

LOAD INTERRUPT ENABLE – This command causes a write of 6120 AC bit 11 to the addressed device's interrupt enable flip flop. This write holds neither $\overline{C0}$ nor $\overline{C1}$ low so that a write without a clear of the AC is performed. The device is incapable of generating interrupts if the interrupt enable flip flop is cleared.

INTERRUPT LOGIC:

A device controller within the IOC is capable of generating an interrupt by pulling the $\overline{INTREQ}$ line low if all of the following conditions are true:

1. The device is programmed for edge sensitive SENSE input, and
2. The device flag flip flop has been set, and
3. The device interrupt enable flip flop is set, and
4. The priority string input for that device is true.

Normally, with no system interrupts outstanding, all device priority inputs and outputs are low. At the highest priority IOC, the $\overline{PRI}$ input must be tied to V_{SS}.

Whenever the interrupt conditions are met at any device on the IOC, the $\overline{INTREQ}$ line is pulled low and the following sequence of events occurs:

1. The 6120 $\overline{INTREQ}$ being low causes $\overline{INTGNT}$ low. All IOC driving device controllers which have the interrupt condition met set their interrupt sample flip flops. Note that this is an edge triggered *set* and is *not* a "load". All device controllers which have their interrupt sample flip flops set will hold their respective priority outputs high. All device controllers with a high priority input hold their priority outputs high and also are inhibited from driving the $\overline{INTREQ}$ bus low.
2. When the first IOT is executed with $\overline{INTGNT}$ low, one of two events occurs, depending on the IOT command:

a. If the command issued is a SKIP ON FLAG (1_8) command, then the normal operation of the IOT command occurs in the addressed device. A SKIP ON FLAG (1_8) instruction will clear the interrupt sample flip flop of the addressed device and will clear the flag flip flop if it is set.

b. If the command is not a SKIP ON FLAG (1_8) command, then the fact that $\overline{INTGNT}$ is low causes special action. During the $\overline{WRITE}$ pulse $\overline{C0}$ and $\overline{C1}$ are both pulled low by the highest priority device with its interrupt sample flip flop set. No other device (not even the addressed device) will respond on this IOT. This IOT specifies a JAM read cycle. The 6120 then generates a $\overline{READ}$ pulse which causes the device address of the highest priority device with its interrupt sample flip flop set to put its device address on DX6-11 and all zeros on DX0-5. Also, the flag flip flop of that device is cleared, causing it to remove the $\overline{INTREQ}$ drive. The interrupt sample flip flop is not cleared at this time so that the priority output of that device continues to be held false (high).

c. Near the end of the interrupt service routine of that particular device, the software should (with the 6120 interrupts disabled) execute a SKIP ON FLAG IOT to the device. This will clear the interrupt sample flip flop of the device, which in turn will set the priority output of that device true, enabling interrupts from devices lower in the chain.

SOFTWARE NOTES:

1. When performing the interrupt vector operation from the 6120, the accumulator must be loaded with a "no interrupt" vector address (such as zero) before the vector IOT is issued. This vector is left in the accumulator if no internal vector is returned by a device controller.
2. Before a device's interrupts are turned off by resetting its interrupt enable flip flop with a 6XX5 command the 6120's interrupts must be turned off. Failure to do so can result in an unidentifiable interrupt from the device.
3. When turning on a device's interrupt with a 6XX5 command, an immediate interrupt will result if the device's flag is set and the 6120 interrupts are turned on.
4. Because the IOC programming sequence relies on an exact sequence of IOT instructions to be executed and $\overline{IOCLR}$ enables interrupts, the programming instructions must be executed with the 6120's interrupts off.
5. Use of the level sensitive "Skip on Flag, Clear Flag" operation (6xx1), requires that a redundant skip instruction followed by a NOP be used to guarantee that the "Flag Sample Flip Flop" is reset.

TESTING NOTE:

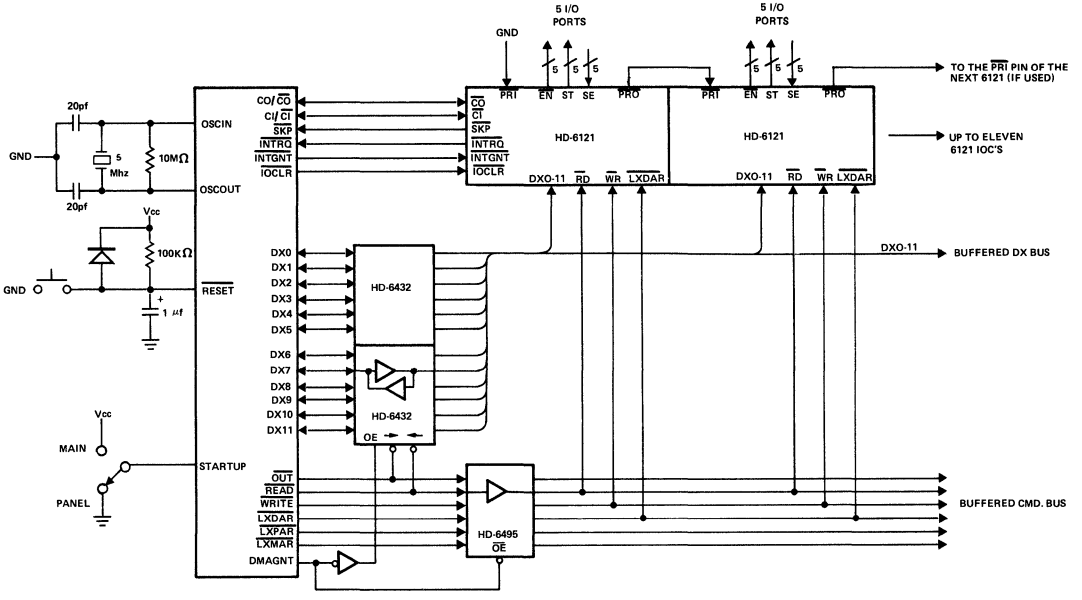
The $\overline{PRO}$ line cannot go true after any $\overline{IOCLR}$ true pulse (either in programming or in a CAF) until there is at least one $\overline{READ}$ pulse. In addition, no external IOT commands can be executed during an $\overline{IOCLR}$ true pulse.

SUMMARY OF 6120, 6121 CONDITIONS:

The following table provides a brief summary of all the 6120 and 6121 Operations.

IOT COMMANDS BIT 9	BIT 10	BIT 11	PROGRAMMING BITS C	I/O	OUTPUTS $\overline{C0}$	$\overline{C1}$	6120 OPERATION	6121 OPERATION
0	1	0	1	1	HiZ	HiZ	Output (AC)	NOP
1	0	0	1	1	HiZ	HiZ	Output (AC)	Generate $\overline{\text{ENABLE}}$. (Output to device.) Set STROBE output.
1	1	0	1	1	Low	HiZ	Output (AC) then (AC)◄— 0	Generate $\overline{\text{ENABLE}}$. (Output to device.) Set STROBE output.
0	1	0	1	0	Low	HiZ	Output (AC) then (AC)◄—0	NOP except for low $\overline{C0}$ output. Result is only to clear 6120 AC.
1	0	0	1	0	HiZ	Low	(AC)◄— Input V(AC)	Generate $\overline{\text{ENABLE}}$. (Input from device.) Set STROBE output.
1	1	0	1	0	Low	Low	(AC)◄— Input	Generate $\overline{\text{ENABLE}}$. (Input from device.) Set STROBE output.
1	0	1	X	X	HiZ	HiZ	Output (AC)	Load interrupt enable flip flop from DX11.
0	0	0	X	X	HiZ	HiZ	Output (AC)	Set flag flip flop if its prog. bit is set. Clear STROBE output.
0	0	1	X	X	HiZ	HiZ	Output (AC)	Pull $\overline{\text{SKIP}}$ low and clear Flag F.F. if flag sample flip flop is a 1 during the write pulse.
X	1	1	X	X	HiZ	HiZ	Output (AC)	No operation.
Vector Read			X	X	Low	Low	(AC)◄— Input	Place interrupt vector on DX bus, clear Flag F.F.
Programming IOT			X	X	Low	HiZ	Output (AC) then (AC)◄— 0	Load programming information to device programming register from the DX bus during write.

BUFFERED BUS 6120/6121 INTERFACING EXAMPLE



NOTE: This simplified example does not show the extended Memory Addressing and other features of the 6120.

HM-6100
CMOS 12 BIT MICROPROCESSOR (CPU)

Features

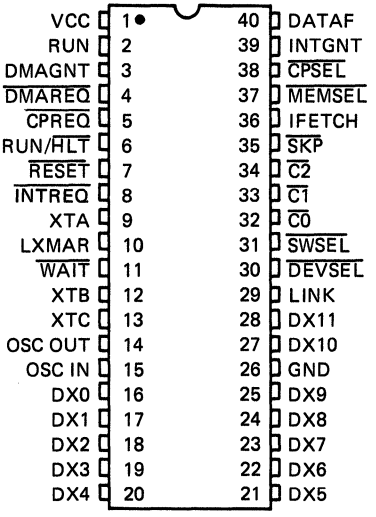
- LOW POWER - TYP.< 5.0μW
- SINGLE +5V POWER SUPPLY
- FULL TEMPERATURE RANGE -55°C TO +125°C
- STATIC OPERATION
- SINGLE PHASE CLOCK, ON CHIP CRYSTAL OSC.
- SOFTWARE COMPATIBLE WITH PDP-8/E
- 12-BIT DATA WORD
- OVER 90 SINGLE WORD INSTRUCTIONS
- RELOCATABLE MEMORY ORGANIZATION
- BASIC ADDRESSING TO 4K 12 BIT WORDS
- PROVISION FOR DEDICATED CONTROL PANEL
- 128 GENERAL PURPOSE REGISTERS
- 8 AUTOINDEXING REGISTERS
- FLEXIBLE PROGRAMMED I/O TRANSFERS
- VECTORED INTERRUPT CAPABILITY

Description

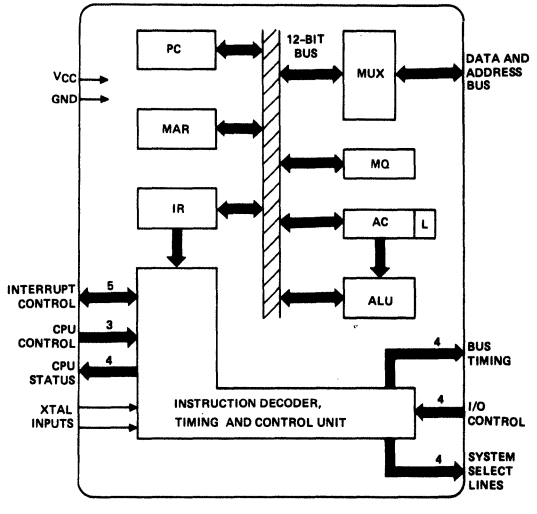
The HM-6100 is a single address, fixed word length, parallel transfer microprocessor using 12-bit two's complement arithmetic. It is a general purpose processor which recognizes the instruction set of Digital Equipment Corporation's PDP-8/E Minicomputer.

Standard features include indirect addressing and facilities for instruction skipping, program interrupts as a function of input/output device conditions, and auto-restart. Five 12-bit registers are used to control microprocessor operations, address memory, perform arithmetic or logical operations, and store data. The device design is optimized to minimize the number of external components required for interfacing with standard memory and peripheral devices.

Pinout



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND - 0.3V) to (VCC +0.3V)
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	
Industrial HM-6100-9	-40°C to +85°C
Military HM-6100-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

VCC = 5.0 ± 10% Volts, T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIHC	Logical "1" Osc. Input Voltage	VCC-.5			V	
VIL	Logical "0" Input Voltage			20% VCC	V	
VILC	Logical "0" Osc. Input Voltage			GND +.5	V	
IIL	Input Leakage (1)	-1.0		+1.0	μA	$0V \leq VIN \leq VCC$
VOH	Logical "1" Output Volt. (2)	2.4			V	IOH = -0.2mA
VOL	Logical "0" Output Volt. (2)			0.45	V	IOL = 2.0mA
IO	Output Leakage	-1.0		+1.0	μA	$0V \leq VO \leq VCC$
ICC1	Supply Current (Static)			400	μA	VIN = VCC, Freq. = 0
ICC2	Supply Current (Operating)			2.5	mA	VCC=5.5V, Freq=2.0MHz
CI	Input Capacitance (3)		5	7	pF	
CO	Output Capacitance (3)		8	10	pF	
CIO	Input/Output Capacitance (3)		8	10	pF	
COSC	Oscillator IN/OUT CAP. (3)		30		pF	

Notes: (1) Except pin 14 and 15
(2) Except pin 14
(3) Guaranteed and sampled, but not 100% tested.

A.C.

		TA = 25°C VCC = 5.0V (1)		TA = Indust. VCC = 5.0 ± 10%V		TA = Military VCC = 5.0 ± 10%V			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
fMAX	Max Operating Frequency		4.0		3.33		2.5	MHz	CL = 50pF
TS	Major State Time	500		600		800		ns	See Timing Diagram
TLX	LXMAR Pulse Width	220		230		355		ns	
TAS	Address Setup Time	80		85		200		ns	
TAH	Address Hold Time	150		125		175		ns	
TAL	Access Time from LXMAR		450		520		745	ns	
TEN	Output Enable (Memory)		250		300		470	ns	
TEND	Output Enable (I/O)		300		470		655	ns	
TWP	Write Pulse Width	200		235		330		ns	
TDS	Data Setup (Memory)	160		135		250		ns	
TDSD	Data Setup (I/O)	185		225		350		ns	
TDH	Data Hold Time	125		125		170		ns	
TST	Status Signals Valid		250		300		325	ns	
TRS	Request Inputs Setup	0		0		0		ns	
TRH	Request Inputs Hold	200		250		300		ns	
TWS	Wait Setup Time	0		50		50		ns	
TWH	Wait Hold Time	100		100		150		ns	
TRHS	Run Halt Setup Time	0		50		50		ns	
TRHP	Run Halt Pulse Width	100		100		150		ns	

NOTE 1: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information - not guaranteed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	8.0V
Input or Output Voltage Applied	Gnd -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	
Industrial HM-6100C-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

VCC = 5.0 ± 5% Volts, T_A = Industrial

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIHC	Logical "1" Osc. Input Voltage	VCC-.5			V	
VIL	Logical "0" Input Voltage			.8	V	
VILC	Logical "0" Osc. Input Voltage			GND +.5	V	
IIL	Input Leakage (1)	-10		+10	µA	$0V \leq VIN \leq VCC$
VOH	Logical "1" Output Volt. (2)	2.4			V	IOH = -0.2mA
VOL	Logical "0" Output Volt. (2)			0.45	V	IOL = 1.6mA
IO	Output Leakage	-10		+10	µA	$0V \leq VO \leq VCC$
ICC1	Supply Current (Static)			600	µA	VIN = VCC, Freq. = 0
ICC2	Supply Current (Operating)			5.0	mA	VCC=5.5V, Freq=2.0MHz
CI	Input Capacitance (3)		5	7	pF	
CO	Output Capacitance (3)		8	10	pF	
CIO	Input/Output Capacitance (3)		8	10	pF	
COSC	Oscillator IN/OUT CAP. (3)		30		pF	

Notes: (1) Except pin 14 and 15
(2) Except pin 14
(3) Guaranteed and sampled, but not 100% tested.

A.C.

		TA = 25°C VCC=5.0V(1)		TA = Indust. VCC = 5.0 ± 5%			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNIT	TEST CONDITION
fMAX	Max operating Freq.		3.33		2.5	MHz	CL = 50pF
TS	Major State Time	600		800		ns	See Timing Diagram
TLX	LXMAR Pulse Width	270		335		ns	
TAS	Address Setup Time	100		120		ns	
TAH	Address Hold Time	150		175		ns	
TAL	Access Time from LXMAR		500		650	ns	
TEN	Output Enable (Memory)		300		400	ns	
TEND	Output Enable (I/O)		350		575	ns	
TWP	Write Pulse Width	250		320		ns	
TDS	Data Setup (Memory)	180		240		ns	
TDSD	Data Setup (I/O)	200		275		ns	
TDH	Data Hold Time	130		175		ns	
TST	Status Signals Valid		300		350	ns	
TRS	Request Inputs Setup	0		0		ns	
TRH	Request Inputs Hold	100		130		ns	
TWS	Wait Setup Time	0		0		ns	
TWH	Wait Hold Time	100		130		ns	
TRHS	Run Halt Setup Time	0		70		ns	
TRHP	Run Halt Pulse Width	100		130		ns	

Note 1: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information - not guaranteed.

Timing and State Control

The HM-6100 generates all the timing and state signals internally. A crystal is used to control the CPU operating frequency. The CPU divides the crystal frequency by two. With a 4MHz crystal, the internal states will be of 500ns duration. The major timing states are described in Figure 1.

T1 For memory reference instructions, a 12-bit address is sent on the DataX, DX, lines. The Load External Address Register, LXMAR, is used to clock an external register to store the address information externally, if required. When executing an Input-Output I/O instruction, the instruction being executed is sent on the DX lines to be stored externally. The external address register then contains the device address and control information.

Various CPU request lines are priority sampled if the next cycle is an Instruction Fetch cycle. Current state of the CPU is available externally.

T2 Memory/Peripheral data is read for an input transfer (READ). $\overline{\text{WAIT}}$ controls the transfer duration. If $\overline{\text{WAIT}}$ is active during input transfers, the CPU waits in the T2 state. The wait duration is an integral multiple of the crystal frequency - 250ns for 4MHz.

For Memory reference instructions, the Memory Select, $\overline{\text{MEMSEL}}$, lines are active. For I/O instruction the $\overline{\text{DEVSEL}}$, line is active. Control lines, therefore, distinguish the contents of the external register as memory or device address.

External device sense lines $\overline{\text{C0}}$, $\overline{\text{C1}}$, $\overline{\text{C2}}$, and SKP are sampled if the instruction being executed is an I/O instruction.

Control Panel Memory Select, $\overline{\text{CPSEL}}$, and Switch Register Select, $\overline{\text{SWSEL}}$, become active low for data transfers between the HM-6100 and Control Panel Memory and the Switch Register, respectively.

T3, T4, T5
ALU operation and internal register transfers.

T6 This state is entered for an output transfer (WRITE). The address is defined during T1. $\overline{\text{WAIT}}$ controls the time for which the WRITE data must be maintained.

The following illustrates the timing of the CPU when its operating frequency is low enough that propagation delays can be ignored. It effectively shows the timing of the CPU when it is single clocked.

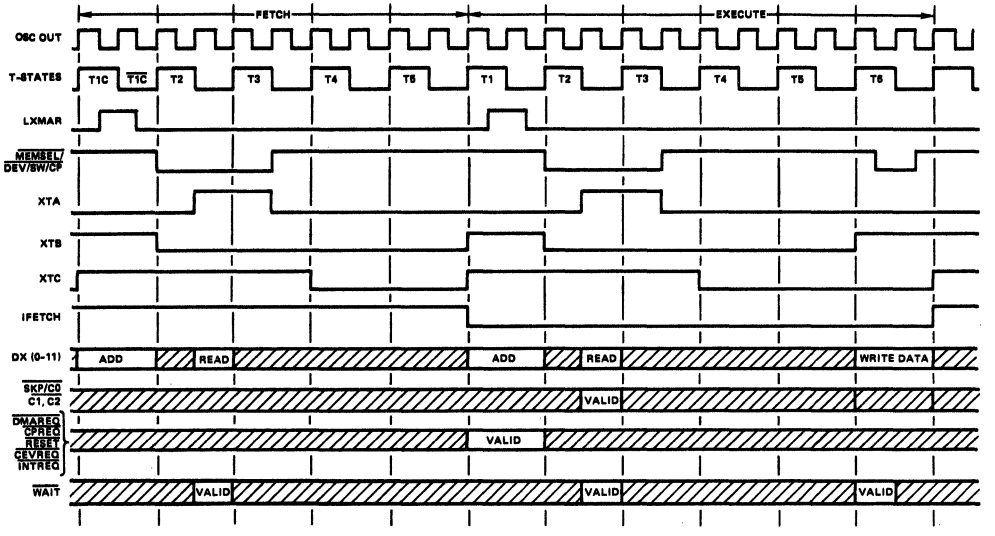


FIGURE 1 – Static Timing

The dynamic or high frequency timing illustrates the propagation delays at specified operating frequencies. (Refer to specifications) It defines the interface requirements for memory and I/O devices on the bus.

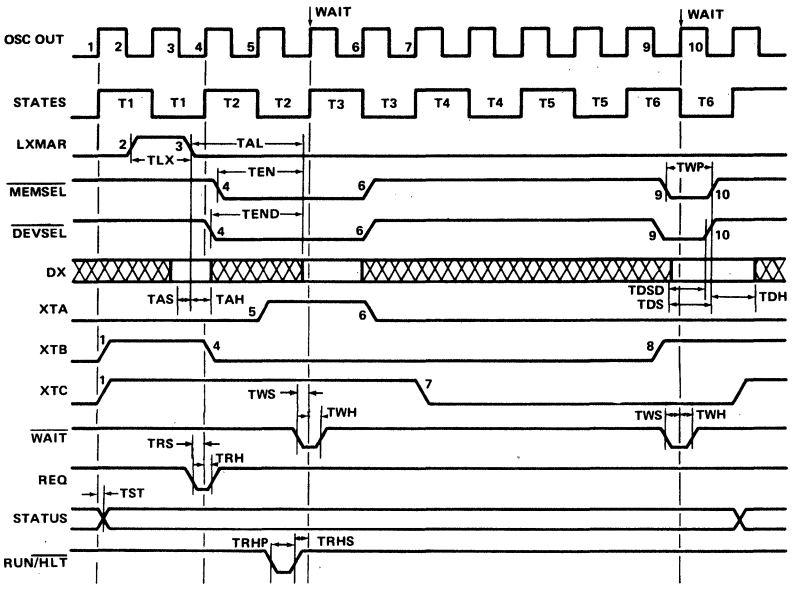


FIGURE 2 – Dynamic Timing

Microprocessor Architecture

The block diagram of the CPU architecture, shown on the front page, consists of the following major functional segments:

- CPU Registers
- Arithmetic and Logic Unit
- Dx-Bus Multiplexer
- Timing and Control Unit

Each one is briefly described below.

CPU REGISTERS

The CPU consists of five, 12-bit registers, of which three are user programmable; 1) Accumulator (AC), 2) Program Counter (PC), and 3) Multiply Quotient (MQ). The remaining two registers are the Instruction Register (IR) and the Memory Address Register (MAR) which are used exclusively for internal operations. The CPU registers are defined as follows.

ACCUMULATOR AND LINK (AC/L)

All arithmetic and logical operations are performed in the AC. For any arithmetic operation, the AC data and memory data are combined in the ALU and the result is temporarily stored in the AC. Under software control, the AC can be cleared, set, complemented, incremented, tested or rotated. Using the Operate Microinstructions, a variety of register operate instructions can be derived.

The link is a one-bit extension of the AC. It can be complemented with a carry out of the ALU or cleared, set, complemented, tested and rotated along with the rest of the AC. It also serves as the carry output for two's complement arithmetic.

MULTIPLY QUOTIENT (MQ)

The MQ register can be used as a temporary storage for the AC. The MQ may be OR'ed with the AC and the result stored in the AC or the contents of the AC and MQ may be swapped. The MQ is used in conjunction with the AC to perform multiplication, division, and double-precision operations.

PROGRAM COUNTER (PC)

The PC supports both memory and input-output device operations. For memory operations, the PC is controlled exclusively by internal logic and instructions fetched from memory. During an instruction fetch cycle the contents of the PC are transferred to the memory address register (MAR) while the current instruction is being decoded. The PC is then loaded with a new address or simply incremented for the next instruction depending upon the type of instruction. The next instruction obtained from memory is then loaded into the Instruction Register. For example, if the instruction is a JMP X, then the branch address X is loaded into the PC for program controlled branching.

Branching can also be controlled by an external device during input-output operations. This feature allows I/O controlled vectored interrupts.

MEMORY ADDRESS REGISTER (MAR)

The MAR contains the address of the memory location that is currently selected for memory or I/O read-write operations. It is also used for microprogram control during data transfers to and from memory and peripherals.

INSTRUCTION REGISTER (IR)

The instruction fetched from memory is held in the IR while being interpreted by the Instruction Decoder. The IR specifies the initial step of the microprogram sequence for each instruction and is also used to store temporary data for microprogram control.

ARITHMETIC AND LOGIC UNIT (ALU)

The ALU performs 12-bit arithmetic, logical and rotate operations. Its input is derived from the AC and any one of the other CPU registers. The type of operations performed by the ALU include:

ADD	Left-right shifts and rotates
Logical AND	Increment
Logical OR	Complement
Test AC	Set/Clear

DX-BUS MULTIPLEXER

To keep the CPU pin count to a reasonable 40 and still maintain a 12-bit word structure, the address and data paths are multiplexed by the DX-Bus Multiplexer. It handles data, address and instruction transfers between the CPU and memory or peripheral devices on a time-multiplexed basis.

TIMING AND CONTROL UNIT

The Timing and Control Unit generates the state and cycle timing signals from a single-phase clock and maintains the proper sequences of events required for any processing task. It also decodes the instruction obtained from the IR and combines the result with various timing signals and external control inputs to provide control and gating signals required by other functional units (both internal and external to the CPU).

Memory Organization

The HM-6100 has a basic addressing capacity of 4096 12-bit words. The addressing capacity may be extended to 32K words by Extended Memory Control hardware. Every location has a unique 4 digit octal (12 bit binary) address, 0000_8 to 7777_8 (0000_{10} to 4095_{10}). The Memory is subdivided into 32 PAGES of 128 words each. Memory Pages are numbered sequentially from Page 00_8, containing addresses 0000-0177_8, to Page 37_8, containing addresses 7600_8-7777_8. The first 5 bits of a 12-bit MEMORY ADDRESS denote the PAGE NUMBER and the low order 7 bits specify the PAGE ADDRESS of the memory location within the given Page.

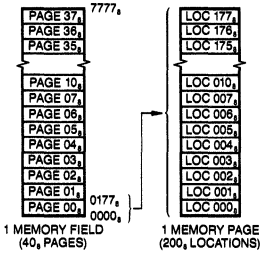


FIGURE 3 – Memory Organization

Memory and Processor Instructions

The HM-6100 instructions are 12-bit words stored in memory. The HM-6100 makes no distinction between instruction and data; it can manipulate instructions as stored variables or execute data as instructions. There are three general classes of HM-6100 instructions. They are Memory Reference Instructions (MRI), Operate Instructions (OPR), and Input/Output Transfer Instructions (IOT).

During an instruction fetch cycle, the HM-6100 fetches the instruction pointed to by the PC. The contents of the PC are transferred to the MAR. The PC is incremented by 1. The PC now contains the address of the "current" instruction which must be fetched from memory. Bits 0-4 of the MAR identify the CURRENT PAGE, that is, the Page from which instructions are currently being fetched and bits 5-11 of the MAR identify the location within the Current Page. (PAGE ZERO (0), 0000_8-0177_8, by definition, denotes the first 128 words of memory and is called the Register Page.)

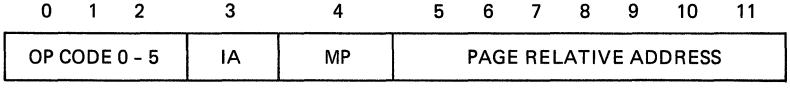
Since the HM-6100 is a static design it can operate at any crystal frequency from 0 to 8MHz. State times required for execution are given for each instruction. Execution time can be calculated from the equation:

$$T = N*(2*(1/F))$$

where N is the number of state times and F is the crystal or input clock frequency.

MEMORY REFERENCE INSTRUCTIONS (MRI)

The Memory Reference Instructions operate on the contents of a memory location or use the contents of a memory location to operate on the AC or the PC. The first 3 bits of a Memory Reference Instruction specify the operation code, or OPCODE, and the low order 9 bits, the OPERAND address, as shown in Figure 4.



IA: Indirect Addressing 0 = Direct; 1 = Indirect
MP: Memory Page 0 = Register Page; 1 = Current Page

FIGURE 4 – Memory Reference Instruction Format

Bits 5 through 11, the PAGE ADDRESS, identify the location of the OPERAND on a given page, but they do not identify the page itself. The page is specified by bit 4, called the CURRENT PAGE OR REGISTER PAGE BIT. If bit 4 is a 0, the page address is interpreted as a location on the Register Page. If bit 4 is a 1, the page address specified is interpreted to be on the Current Page.

By this Method, 256 locations may be directly addressed, 128 on the REGISTER PAGE and 128 on the CURRENT PAGE. Other locations are addressed by using bit 3. When bit 3 is a 0, the operand address is a DIRECT ADDRESS. An INDIRECT ADDRESS (pointer address) identifies the location that contains the desired address (effective address). To address a location that is not directly addressable, not in the REGISTER PAGE or in the CURRENT PAGE, the absolute address of the desired location is stored in one of the 256 directly addressable locations (pointer address). Upon execution, the MRI will operate on the contents of the location identified by the address contained in the pointer location. Note that locations 0010_8-0017_8 in the Register Page are AUTOINDEXED. When these locations are used for index registers their contents are incremented by 1 and restored before they are used as the operand address. These locations are therefore convenient for indexing applications.

Combinations of mode and page bits yield four (4) addressing modes:

- Current Page, Direct
- Current Page, Indirect
- Register Page, Direct
- Register Page, Indirect

A fifth addressing mode results from use of the AUTOINDEX registers:

- Register Page, Autoindexed

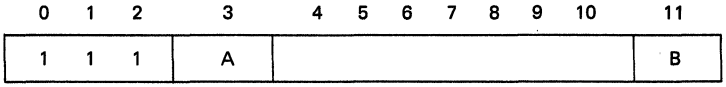
TABLE 1

MNE-MONIC	OP CODE	NUMBER OF STATES			OPERATION
		DIRECT	INDIRECT	AUTO-INDEXED	
AND	0XXX	10	15	16	LOGICAL AND: Causes a bit-by-bit boolean AND between the contents of the Accumulator and the contents of the effective address (XXX) specified by the instruction. The result is left in the AC and the data word in the referenced location is not altered.
TAD	1XXX	10	15	16	TWO'S COMPLEMENT ADD: Performs a binary two's complement addition between the specified data word and the contents of the AC; the result is left in the AC. If a carry out occurs, the state of the Link is complemented. If the AC is initially cleared, this instruction acts as a LOAD from memory.
ISZ	2XXX	16	21	22	INCREMENT AND SKIP IF ZERO: The contents of the effective address are incremented by 1 and restored. If the result is zero, the next sequential instruction is skipped.
DCA	3XXX	11	16	17	DEPOSIT AND CLEAR THE ACCUMULATOR: The contents of the AC are stored in the effective address and the AC is cleared.
JMS	4XXX	11	16	17	JUMP TO SUBROUTINE: The contents of the PC are stored in the effective address and the effective address + 1 is stored in the PC. The link, AC, and MQ are unchanged.
JMP	5XXX	10	15	16	JUMP: The effective address is loaded into the PC thus causing program execution to branch to a new location.
IOT	6XXX	17			INPUT/OUTPUT TRANSFER: Used to initiate the operation of peripheral devices and to transfer data between the peripherals and the CPU.
OPI	7XXX				OPERATE Instructions: Used to perform logical operations on the contents of the major registers.
		10			2 - Cycle OPERATE
		15			3 - Cycle OPERATE

Operate Instructions

The Operate Instructions, which have an OPCODE of 7_8(111), consist of 3 groups of microinstructions. Group 1 microinstructions, which are identified by the presence of a 0 in bit 3, are used to perform logical operations on the contents of the accumulator and link. Group 2 micro instructions, which are identified by the presence of a 1 in bit 3 and a 0 in bit 11, are used primarily to test the contents of the accumulator and then conditionally skip the next sequential instruction. Group 3 microinstructions have a 1 in bit 3 and a 1 in bit 11 and are used to perform logical operations on the contents of the AC and MQ.

The basic OPR instruction format is shown in Figure 5. Operate microinstructions from any group may be microprogrammed with other operate microinstructions of the same group. The actual code for a microprogrammed combination of two, or more, microinstructions is the bitwise logical OR of the octal codes for the individual microinstructions. When more than one operation is microprogrammed into a single instruction, the operations are performed in a prescribed sequence, with logical sequence number 1 microinstructions performed first, logical sequence number 2 microinstructions performed second, logical sequence number 3 microinstructions performed third, and so on. Two operations with the same logical sequence number, within a given group of microinstructions, are performed simultaneously.

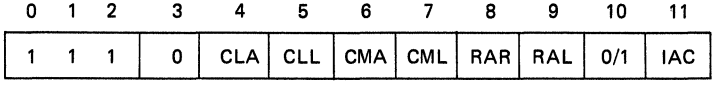


MICROINSTRUCTION	A	B
Group 1	0	0/1
Group 2	1	0
Group 3	1	1

FIGURE 5 – Basic OPR Instruction Format

GROUP 1 MICROINSTRUCTIONS

Figure 6 shows the instruction format of a group 1 microinstruction. Any one of bits 4 to 11 may be set, loaded with a binary 1, to indicate a specific group 1 microinstruction. If more than one of these bits is set, the instruction is a microprogrammed combination of group 1 microinstructions, which will be executed according to the logical sequence shown in Figure 6.



Logical Sequences:
1- CLA CLL
2 - CMA CML
3 - IAC
4 - RAR RAL RTR RTL BSW

BIT 8	BIT 9	BIT 10	FUNCTION
0	0	1	BSW
0	1	0	RAL
0	1	1	RTL
1	0	0	RAR
1	0	1	RTR

FIGURE 6 – Group 1 Microinstruction Format

Table 2-1 lists commonly used group 1 microinstructions, their assigned mnemonics, octal number, instruction format, logical sequence, the operation they perform, and the number of states. The same format is followed in Table 3 and 4 which corresponds to group 2 and 3 microinstructions, respectively.

There are several commonly used microprogrammed combinations of group 1 microinstructions. These are listed in Table 2-2. When writing programs it is necessary to load various constants into the AC for such purposes as initiallizing counters and to provide comparisons. Table 2-3 lists those constants which can be loaded directly via microprogrammed combinations of group 1 instructions.

TABLE 2 - 1

MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
NOP	7000	1	10	NO OPERATION - This instruction causes a 10 state delay in program execution, without affecting the state of the HM-6100. It may be used for timing synchronization or as a convenient means of deleting an instruction from a program.
CLA	7200	1	10	CLEAR ACCUMULATOR - The accumulator is loaded with binary 0's.

FIGURE 2 - 1 Continued

MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
CLL	7100	1	10	CLEAR LINK - The link is loaded with a binary 0.
CMA	7040	2	10	COMPLEMENT ACCUMULATOR - The content of each bit of the AC is complemented. This has the effect of replacing the contents of the AC with its one's complement.
CML	7020	2	10	COMPLEMENT LINK - The content of the link is complemented.
IAC	7001	3	10	INCREMENT ACCUMULATOR - The content of the AC is incremented by one (1) and the carry out componments the Link (L).
BSW	7002	4	15	BYTE SWAP - The right six (6) bits of the AC are exchanged or SWAPPED with the left six bits. AC(0) is swapped with AC(6), AC(1) with AC(7), etc. The link is not affected.
RAL	7004	4	15	ROTATE ACCUMULATOR LEFT - The content of the AC and L are rotated one binary position to the left. AC(0) is shifted to L and L is shifted to AC(11). The ROTATE instructions use what is commonly called a circular shift, meaning that any bit rotated off one end of the accumulator will reappear at the other end.
RTL	7006	4	15	ROTATE TWO LEFT - The contents of the AC and L are rotated two binary positions to the left. AC(1) is shifted to L and L is shifted to AC(10).
RAR	7010	4	15	ROTATE ACCUMULATOR RIGHT - The contents of the AC and L are rotated one binary position to the right. AC(11) is shifted to L and L is shifted to AC(0).
RTR	7012	4	15	ROTATE TWO RIGHT - The contents of the AC and L are rotated two binary positions to the right. AC(10) is shifted to L and L is shifted to AC(1).

TABLE 2 - 2

MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
CLA CLL	7300	1	10	CLEAR ACCUMULATOR - CLEAR LINK
CIA	7041	2, 3	10	COMPLEMENT AND INCREMENT ACCUMULATOR - The content of the AC is replaced with its two's complement. The carry out complements the link. This is a microprogrammed combination of CMA and IAC.
STL	7120	1, 2	10	SET THE LINK - The LINK is loaded with a binary 1 corresponding with a microprogrammed combination of CLL and CML.
STA	7240	1, 2	10	SET THE ACCUMULATOR - Each bit of the AC is set to 1 corresponding to a microprogrammed combination of CLA and CMA.
CLA IAC	7201	1, 3	10	Sets the accumulator to a 1.

TABLE 2 - 2 Continued

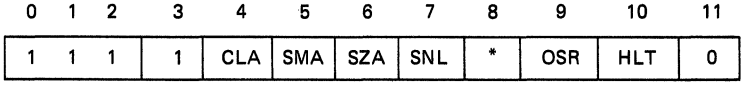
MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
GLK	7204	1, 4	15	GET LINK - The AC is cleared and the content of the link is shifted into AC(11) while a 0 is shifted into the link. This is a microprogrammed combination of CLA and RAL.
CLL RAL	7104	1, 4	15	CLEAR LINK - ROTATE ACCUMULATOR LEFT
CLL RTL	7106	1, 4	15	CLEAR LINK - ROTATE TWO LEFT
CLL RAR	7110	1, 4	15	CLEAR LINK - ROTATE ACCUMULATOR RIGHT
CLL RTR	7112	1, 4	15	CLEAR LINK - ROTATE TWO RIGHT

TABLE 2 - 3

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	DECIMAL CONSTANT	INSTRUCTIONS COMBINED
NL0000	7300	1	10	0	CLA CLL
NL0001	7301	1, 3	10	1	CLA CLL IAC
NL0002	7305	1, 3, 4	15	2	CLA CLL IAC RAL
NL0003	7325	1, 2, 3, 4	15	3	CLA CLL CML IAC RAL
NL0004	7307	1, 3, 4	15	4	CLA CLL IAC RTL
NL0006	7327	1, 2, 3, 4	15	6	CLA CLL CML IAC RTL
NL0100	7303	1, 3, 4	15	64	CLA IAC BSW
NL2000	7332	1, 2, 4	15	1024	CLA CLL CML RTR
NL3777	7350	1, 2, 4	15	2047	CLA CLL CMA RAR
NL4000	7330	1, 2, 4	15	-0	CLA CLL CML RAR
NL5777	7352	1, 2, 4	15	-1025	CLA CLL CMA RTL
NL6000	7333	1, 2, 3, 4	15	-1024	CLA CLL CML IAC RTR
NL7775	7346	1, 2, 4	15	-3	CLA CLL CMA RTL
NL7776	7344	1, 2, 4	15	-2	CLA CLL CMA RAL
NL7777	7340	1, 2	10	-1	CLA CLL CMA

GROUP 2 MICROINSTRUCTIONS

Figure 7 shows the instruction format of group 2 microinstructions, Bits 4 - 10 may be set to indicate a specific group 2 microinstruction. If more than one of bits 4 - 7 or 9 - 10 is set, the instruction is a microprogrammed combination group 2 microinstructions, which will be executed according to the logical sequence shown in Figure 7.



Logical Sequences:
1 (BIT 8 = 0) -SMA or SZA or SNL
(BIT 8 = 1) -SPA or SNA or SZL
2 -CLA
3 -OSR, HLT

* Reverse sensing BIT:
Unconditional SKIP when
BITS 5, 6, & 7 are 0's

FIGURE 7 — Group 2 Microinstruction Format

Skip microinstructions may be microprogrammed with CLA, OSR, or HLT microinstructions. Skip microinstructions which have a 0 in bit 8, however, may not be microprogrammed with skip microinstructions which have a 1 in bit 8. When two or more skip microinstructions are microprogrammed into a single instruction, the resulting condition on which the decision will be based is the logical OR of the individual conditions when bit 8 is 0, or when bit 8 is 1, the decision will be based on the logical AND.

TABLE 3 -1

MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
NOP	7400	1	10	NO OPERATION - See Group 1 microinstructions.
CLA	7600	2	10	CLEAR ACCUMULATOR - The accumulator is loaded with binary O's.
HLT	7402	3	10	HALT - Program stops at the conclusion of the current machine cycle. If HLT is combined with others in OPR 2, the other operations are completed before the end of the cycle.
SKP	7410	1	10	SKIP - The content of the PC is incremented by 1, to skip the next instruction.
SNL	7420	1	10	SKIP ON NON-ZERO LINK - The content of L is sampled; the next sequential instruction is skipped if L contains a 1. If L contains a 0, the next instruction is executed.
SZL	7430	1	10	SKIP ON ZERO LINK - The instruction is skipped if the link contains a 0.
SZA	7440	1	10	SKIP ON ZERO ACCUMULATOR - The content of the AC is sampled; the next sequential instruction is skipped if all AC bits are 0. If any bit in the AC is a 1, the next instruction is executed.
SNA	7450	1	10	SKIP ON NON-ZERO ACCUMULATOR - The next instruction is skipped if any one bit of the AC contains a 1. If every bit in the AC is 0, the next instruction is executed.
SMA	7500	1	10	SKIP ON MINUS ACCUMULATOR - If the content of AC(0) contains a negative two's complement number, the next sequential instruction is skipped. If AC(0) contains a 0, the next instruction is executed.
SPA	7510	1	10	SKIP ON POSITIVE ACCUMULATOR - If the content of AC(0) contains a 0, indicating a positive two's complement number, the next sequential instruction is skipped.
OSR	7404	3	15	OR WITH SWITCH REGISTER - The content of the Switch Register is inclusively OR'ed with the content of the AC and the result stored in the AC. The HM-6100 sequences the OSR instruction through a 2-cycle execute phase referred to as OPR 2A and OPR 2B. This instruction provides the simplest way to input data to the HM-6100 from peripherals.
LAS	7604	1, 3	15	LOAD ACCUMULATOR WITH SWITCH REGISTER - The content of the AC is loaded with the content of the SR, bit for bit. This is equivalent to a microprogrammed combination of CLA and OSR.

Table 3 - 2 lists every legal combination of skip microinstructions, along with the resulting condition upon which the decision to skip or execute the next sequential instruction is based. When these combinations include a CLA, the accumulator is cleared after the decision is made. This is a useful trick to save code when a new value will be TAD'ed into the AC.

TABLE 3 - 2

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
SZA SNL	7460	1	10	Skip if AC = 0 or L = 1 or both.
SNA SZL	7470	1	10	Skip if AC $\neq$ 0 and L = 0.
SMA SNL	7520	1	10	Skip if AC $<$ 0 or L = 1 or both.
SPA SZL	7530	1	10	Skip if AC $\geq$ 0 and L = 0.
SMA SZA	7540	1	10	Skip if AC $\leq$ 0.
SPA SNA	7550	1	10	Skip if AC $>$ 0.
SMA SZA SNL	7560	1	10	Skip if AC $\leq$ 0 or L = 1 or both.
SPA SNA SZL	7570	1	10	Skip if AC $>$ 0 and L = 0.

When writing an actual program, it is useful to think in terms of the FORTRAN relational operators - .LT., .EQ., etc.- when trying to compare numbers. The following method along with Table 3 - 3 will provide this.

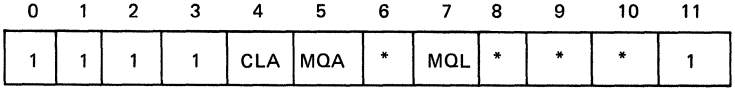
```
CLA CLL          / Initialize AC and Link
TAD B            /Fetch 2nd number
CML CMA IAC      /Create "-B" (AC & L act like a 13 bit accumulator)
TAD A            /Fetch 1st number
Test  CLA        /Use instructions from Table 3 - 3 to provide test
                 /The CLA is optional to provide a clear AC after test
JMP FAIL         /Branch to FAIL routine if test failed
...              /Test passed, continue with program
...
```

TABLE 3 - 3

SKIP IF	UNSIGNED COMPARE	SIGNED COMPARE
A. NE. B	SNA	SNA
A. LT. B	SNL	SMA
A. LE. B	SNL SZA	SMA SZA
A. EQ. B	SZA	SZA
A. GE. B	SZL	SPA
A. GT. B	SZL SNA	SPA SAN

GROUP 3 MICROINSTRUCTIONS

Figure 8 shows the instruction format of group 3 microinstructions which requires bits 3 and 11 to contain a 1. Bits 4, 5 or 7 may be set to indicate a specific group 3 microinstruction. If more than one of the bits is set, the instruction is a microprogrammed combination of group 3 microinstructions following the logical sequence listed in Figure 8.



Logical Sequences:
1 - CLA
2 - MQA, MQL
3 - NOP

*Don't care

FIGURE 8 - Group 3 Microinstruction Format

TABLE 4

MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
NOP	7401	3	10	NO OPERATION - See group 1 microinstructions.
CLA	7600	1	10	CLEAR ACCUMULATOR
MQA	7501	2	10	MQ REGISTER INTO ACCUMULATOR - The content of the MQ is logical OR'ed with the content of the AC and the result is loaded into the AC. The original content of the AC is lost but the original content of the MQ is retained. This instruction provides the programmer with an inclusive OR operation.
MQL	7421	2	10	MQ REGISTER LOAD - The content of the AC is loaded into the MQ, the AC is cleared and the original content of the MQ is lost. This is similar to a DCA instruction.
ACL	7701	1, 2	10	CLEAR ACCUMULATOR AND LOAD MQ REGISTER INTO ACCUMULATOR - This is equivalent to a microprogrammed combination of CLA and MQA. It is similar to the two instruction combination of CLA and TAD.
CAM	7621	1, 2	10	CLEAR ACCUMULATOR AND MQ REGISTER - The content of the AC and MQ are loaded with binary 0's. This is equivalent to a microprogram combination of CLA and MQL.
SWP	7521	2	10	SWAP ACCUMULATOR AND MQ REGISTER - The content of the AC and MQ are interchanged by accomplishing a microprogrammed combination of MQA and MQL.
CLA SWP	7721	1, 2	10	CLEAR ACCUMULATOR AND SWAP ACCUMULATOR AND MQ REGISTER - The content of the AC is cleared. The content of the MQ is loaded into the AC and the MQ is cleared.

Input Output Transfer Instructions (IOT)

The input/output transfer instructions, which have an OPCODE of 6_8 are used to initiate the operation of peripheral devices and to transfer data between peripherals and the HM-6100. Three types of data transfer may be used to receive or transmit information between the HM-6100 and one or more peripheral I/O devices. PROGRAMMED DATA TRANSFER provides a straightforward means of communicating with relatively slow I/O devices, such as Teletypes, cassettes, card readers and CRT displays. INTERRUPT TRANSFERS use the interrupt system to service several peripheral devices simultaneously, on an intermittent basis, permitting computational operations to be performed concurrently with the data I/O operations. Both Programmed Data Transfers and Program Interrupt Transfers use the accumulator as a buffer, or storage area, for all data transfers. Since data may be transferred only between the accumulator and the peripheral, only one 12 bit word at a time may be transferred. DIRECT MEMORY ACCESS, DMA, Transfers variable-size blocks of data between high-speed peripherals and the memory with minimum of program control required by the HM-6100.

IOT INSTRUCTION FORMAT

The Input/Output Transfer instruction format is represented in Figure 9.

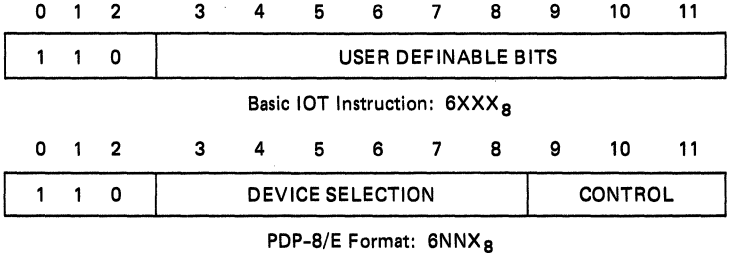


FIGURE 9 – IOT Instruction Format

The first three bits, 0 - 2, are always set to 6_8 (110) to specify an IOT instruction. The next 9 bits, 3 - 11, are user definable and can provide a minimal implementation when each bit controls one operation. When following PDP-8/E format, the next six bits, 3 - 8, contain the device selection code that determines the specific I/O device for which the IOT instruction is intended and, therefore, permit interface with up to 64 I/O devices. The last three bits, 9 - 11, contain the operation specification code that determines the specific operation to be performed. The nature of this operation for any given IOT instruction depends entirely upon the circuitry designed into the I/O device interface.

PROGRAMMED DATA TRANSFER

Programmed Data Transfer is the easiest, simplest, most convenient and most common means of performing data I/O. For microprocessor applications, it may also be the most cost effective approach. The data transfer begins when the HM-6100 fetches an instruction from the memory and recognizes that the current instruction is an IOT (2). This is referred to an IFETCH and consists of five (5) internal states. The HM-6100 sequences the IOT instruction through a 2-cycle execute phase referred to as IOTA and IOTB. Bits 0 - 11 of the IOT instruction are available on DX0 - 11 at IOTA ^ LXMAR (3). These bits must be latched in an external address register. $\overline{\text{DEVSEL}}$ is active low to enalbe data transfers between the HM-6100 and the peripheral device (4) & (5). Input-Output Instruction Timing is shown in Figure 10. The selected peripheral device communicates with the HM-6100 through 4 control lines - $\overline{\text{C0}}$, $\overline{\text{C1}}$, $\overline{\text{C2}}$ and $\overline{\text{SKP}}$. In the HM-6100 the type of data transfer, during an IOT instruction, is specified by the peripheral device(s) by asserting the control lines as shown in Tables 5-1 and 5-2.

The control line $\overline{\text{SKP}}$, when low during an IOT, causes the HM-6100 to skip the next sequential instruction. This feature is used to sense the status of various signals in the device interface. The C0, C1, and C2 lines are treated independently of the $\overline{\text{SKP}}$ line. In the case of a RELATIVE or ABSOLUTE JUMP, the skip operation is performed after the jump. The input signals to the HM-6100, DX0 - 11, $\overline{\text{C0}}$, $\overline{\text{C1}}$, $\overline{\text{C2}}$ and $\overline{\text{SKP}}$, are sampled during IOTA on the rising edge of time state 3 (4). The data from the HM-6100 is available to the device during $\overline{\text{DEVSEL}}$ ^ $\overline{\text{XTC}}$ (5). The IOTB cycle is internal to the HM-6100 to perform the operations requested during IOTA. Both IOTA and IOTB consists of six (6) internal states.

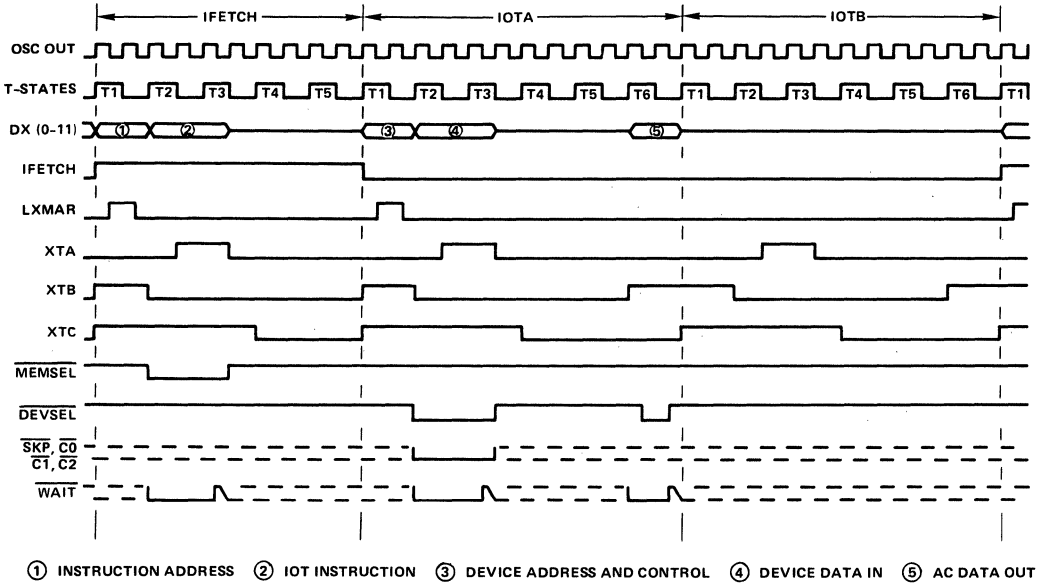


FIGURE 10 – Input-output instruction timing

TABLE 5 - 1
AC DATA TRANSFERS

CONTROL LINES					
$\overline{SKP}$	$\overline{C0}$	$\overline{C1}$	$\overline{C2}$	OPERATION	DESCRIPTION
H	H	H	H	DEV ← AC	The content of the AC is sent to the device.
H	L	H	H	DEV ← AC; CLA	The content of the AC is sent to a device and then the AC is cleared.
H	H	L	H	AC ← AC V DEV; DEV ← AC	Data is received from a device OR'ed with the data in the AC and the result is stored in the AC. The new AC content is sent to the device.
H	L	L	H	AC ← DEV; DEV ← AC	Data is received from a device and loaded into the AC. The new AC content is sent to the device.
L	H	H	H	DEV ← AC; PC ← PC + 1	The content of the AC is sent to the device and the microprocessor skips the next sequential instruction.
L	L	H	H	DEV ← AC; CLA; PC ← PC + 1	The content of the AC is sent to a device, the AC is cleared, and the microprocessor skips the next sequential instruction.
L	H	L	H	AC ← AC V DEV; DEV ← AC; PC ← PC + 1	Data is OR'ed into the AC, the new AC sent to the device, and the microprocessor skips the next sequential instruction.
L	L	L	H	AC ← DEV; DEV ← AC PC ← PC + 1	Data is loaded into the AC, the new AC contents sent to the device, and the next sequential instruction skipped.

TABLE 5 - 2
PC VECTOR TRANSFERS

CONTROL LINES					
$\overline{SKP}$	$\overline{C0}$	$\overline{C1}$	$\overline{C2}$	OPERATION	DESCRIPTION
H	*	H	L	PC ← PC + DEV	Data from the device is added to the contents of the PC. This is referred to as a RELATIVE JUMP.
H	*	L	L	PC ← DEV	Data is received from a device and loaded into the PC. This is referred to as an ABSOLUTE JUMP.
L	*	H	L	PC ← PC + DEV; PC ← PC + 1	The RELATIVE JUMP is performed and then the microprocessor skips the next sequential instruction.
L	*	L	L	PC ← DEV; PC ← PC + 1	The ABSOLUTE JUMP is executed and then the next sequential instruction is skipped.

* Don't Care

PROGRAM INTERRUPT TRANSFERS

The program interrupt system may be used to initiate programmed data transfers in such a way that the time spent waiting for device status is greatly reduced or eliminated altogether. It also provides a means of performing concurrent programmed data transfers between the HM-6100 and the peripheral devices. This is accomplished by isolating the I/O handling routines from the mainline program and using the interrupt system to ensure that these routines are entered only when an I/O device status is set, indicating that the device is actually ready to perform the next data transfer, or that is requires some sort of intervention from the running program.

TABLE 6
PROCESSOR IOT INSTRUCTIONS

MNE-MONIC	OCTAL CODE	OPERATION
SKON	6000	SKIP IF INTERRUPT ON - If Interrupt system is enabled, the next sequential instruction is skipped. The Interrupt system is disabled.
ION	6001	INTERRUPT TURN ON - The internal interrupt acknowledge system is enabled. The interrupt system is enabled after the CPU executes the next sequential instruction.
IOF	6002	INTERRUPT TURN OFF - The interrupt system is disabled. Note that the interrupt system is automatically disabled when the CPU acknowledges an INT request.
SRQ	6003	SKIP IF INT REQUEST - The next sequential instruction is skipped if the INT request bus is low.
GTF	6004	GET FLAGS - The following machines states are read into the indicated bits of AC. bit 0 - Link bit 1 - Greater than flag* bit 4 - Interrupt Enable FF* bit 2 - INT request bus bit 5 - User flag* bit 3 - Interrupt Inhibit FF* bit 6 - 11 - Save Field Register* * These bits are modified by external devices driving the DX bus and the $\overline{C}$-lines ($\overline{C0}$ = L, $\overline{C1}$ = L). For example, bits 1 and 6 - 11 are part of the Extended Memory Control.
RTF	6005	RETURN FLAGS - Link is restored from AC (0). Interrupt system is enabled after the next sequential instruction is executed. All AC bits are available externally to restore external states. (ex. Extended memory control). ($\overline{C0}$ = H, $\overline{C1}$ = H)
SGT	6006	SKIP ON GREATER THAN FLAG - Operation is determined by external devices, if any. This flag is external and must control the skip line.
CAF	6007	CLEAR ALL FLAGS - AC and link are cleared. Interrupt system is disabled.

The interrupt system allows certain external conditions to interrupt the computer program by driving the $\overline{\text{INTREQ}}$ input to the HM-6100 low. If no higher priority requests are outstanding and the interrupt system is enabled, the HM-6100 grants the device interrupt at the end of the current instruction. After an interrupt has been granted, the Interrupt Enable Flip-Flop in the HM-6100 is reset so that no more interrupts are acknowledged until the interrupt system is re-enabled under program control.

The current content of the Program Counter, PC, is deposited in location 0000_8 of the memory and the program fetches the instruction from location 0001_8. The return address is available in location 0000_8. This address must be saved, possibly in a software stack, if nested interrupts are permitted. The INTGNT signal is activated by the HM-6100 when a device interrupt is acknowledged. This signal is reset by executing any IOT instruction. The INTGNT is also useful in implementing an External Vectored Priority Interrupt network.

The user program controls the interrupt mechanism of the HM-6100 by executing the processor IOT instructions listed in Table 6. Several of these interrupt IOT instructions are also used if the memory is extended beyond 4K words.

DIRECT MEMORY ACCESS (DMA)

Direct Memory Access, sometimes called data break, is the perferred form of data transfer for use with high-speed storage devices such as magnetic disk or tape units. The DMA mechanism transfers data directly between memory and peripheral devices. The HM-6100 is involved only is setting up the transfer; the transfers take place with no processor intervention on a "cycle stealing" basis. The DMA transfer rate is limited only by the bandwidth of the memory and the data transfer characteristics of the device.

The device generates a DMA Request when it is ready to transfer data. The HM-6100 grants the $\overline{\text{DMAREQ}}$ by activating the DMAGNT signal at the end of the current instruction. The HM-6100 suspends any further instruction fetches until the $\overline{\text{DMAREQ}}$ line is released. The DX lines are tri-stated, all SEL lines are high, and the external timing signals XTA, XTB, and XTC are active. The device which generated the $\overline{\text{DMAREQ}}$ must provide the address and necessary control signals to the memory for data transfers. The $\overline{\text{DMAREQ}}$ line can also be used as a level sensitive "pause" line.

Control Panel Interrupt Transfer

The HM-6100 CPU provides a unique Control Panel (CP) feature through its $\overline{\text{CPREQ}}$ input and $\overline{\text{CPSEL}}$ output lines. After acknowledging the control panel request, the CPU generates the necessary timing to execute program code in CP memory while also providing the capability to transfer data between CP memory and the user memory using the AC as a buffer. This allows the user memory to be examined and/or modified by the CP software. The CPU will output the $\overline{\text{MEMSEL}}$ signal for all user memory references while the $\overline{\text{CPSEL}}$ signal is generated for CP memory references as shown in Figure 11.

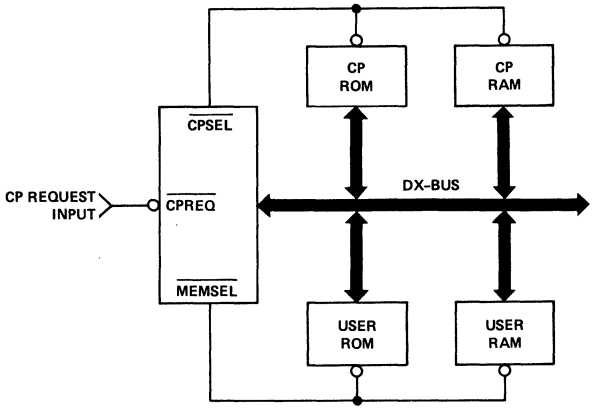


FIGURE 11 – Control Panel Block Diagram

The designer can make use of the control panel features to implement various functions that will be "transparent" to the user's (main) memory. Some of the more common functions include:

- Binary Loader and Punch
- Register Examination and Modification
- Single Cycle
- Octal Debug with Breakpoints
- Octal listing
- Auto Bootstrap

When a $\overline{\text{CPREQ}}$ is granted the PC is stored in location 0000 of Panel Memory and the HM-6100 resumes operation at location 7777 of the Panel Memory. The $\overline{\text{CPREQ}}$ bypasses the interrupt enable system and the processor IOT instruction, ION and IOF, are ignored while the HM-6100 is in the Control Panel Mode. Once a $\overline{\text{CPREQ}}$ is granted, the HM-6100 will not recognize any $\overline{\text{DMAREQ}}$ or $\overline{\text{INTREQ}}$ until the CPREQ has been fully serviced.

During Control Panel program execution access to the user memory is gained through use of indirect TAD, AND, DCA and ISZ instructions. The CPU will transfer control from $\overline{\text{CPSEL}}$ to $\overline{\text{MEMSEL}}$ during the execute phase of these instructions. The instructions are always fetched from control panel memory.

Exiting from the control panel routine is achieved by executing the following sequence:

- ION
- JMP I 0000 /Exit via location 0000 in Panel Memory

Location 0000 contains either the original return address deposited by the HM-6100 when the CP routine was entered, or it may be a new starting address defined by the CP routine.

Internal Priority Structure

After an instruction is completely sequenced, the major state generator scans the internal priority network as shown in in Figure 12. The state of the priority network decides the next sequence of the HM-6100.

The CPU samples the $\overline{\text{RESET}}$ line, the request lines $\overline{\text{CPREQ}}$, $\overline{\text{DMAREQ}}$, and $\overline{\text{INTREQ}}$, and the state of its internal RUN flip-flop during the last execute cycle of each instruction. The worst case response time of the HM-6100 to an external request is, therefore the time required to execute the longest instruction preceded by any 6-state execution cycle. For the HM-6100, this is an autoindexed ISZ, 22 states, preceded by any 6-state execution cycle instruction. The worst case response time is, therefore, 28 states, 14 μs at 4MHz clock frequency.

When the HM-6100 is initially powered up, the state of the timing generator is undefined. The generator is automatically initialized with a maximum of 34 clock pulses. The request inputs, as the HM-6100 is powered on, must span at least 58 clock pulses to be recognized, 34 clocks for the counter to initialize and a maximum of two HM-6100 cycles (20 to 24 clocks) for the state generator to sample the request lines. A positive transition of RUN/$\overline{\text{HLT}}$ should occur at least 10 clock pulses after $\overline{\text{RESET}}$ to be recognized.

The priority hierarchy is:

- $\overline{\text{RESET}}$ - If the $\overline{\text{RESET}}$ line is asserted at the sample time, the processor immediately sets its program counter to 7777, clears the Accumulator and Link, and puts the processor in the $\overline{\text{HALT}}$ state. While halted, the processor continues to cycle and generate the timing signals XTA, XTB, and XTC. During reset the DX line is tri-stated and the SEL lines are high.
- $\overline{\text{CPREQ}}$ - If the $\overline{\text{RESET}}$ line is not found to be asserted, but the $\overline{\text{CPREQ}}$ line is, the processor grants the control panel interrupt request at the end of the current cycle.
- RUN/$\overline{\text{HLT}}$ - If neither of the foregoing lines are asserted, but the processor finds its internal RUN FF in the halt state, it enters the HALT cycle at the end of the last execute cycle. Pulsing the RUN/$\overline{\text{HLT}}$ line low causes the HM-6100 to alternately run and halt. The internal RUN FF changes state on the rising edge of the RUN/$\overline{\text{HLT}}$ line. While halted the processor continues to generate the timing signals XTA, XTB, and XTC.
- $\overline{\text{DMAREQ}}$ - DMA requests are granted at the end of the current cycle only if none of the above actions are pending.
- $\overline{\text{INTREQ}}$ - An interrupt request is granted at the end of the current cycle only if none of the higher priority lines preempts it.
- IFETCH - If none of the above actions are indicated, the processor will fetch the next sequential instruction in the next cycle.

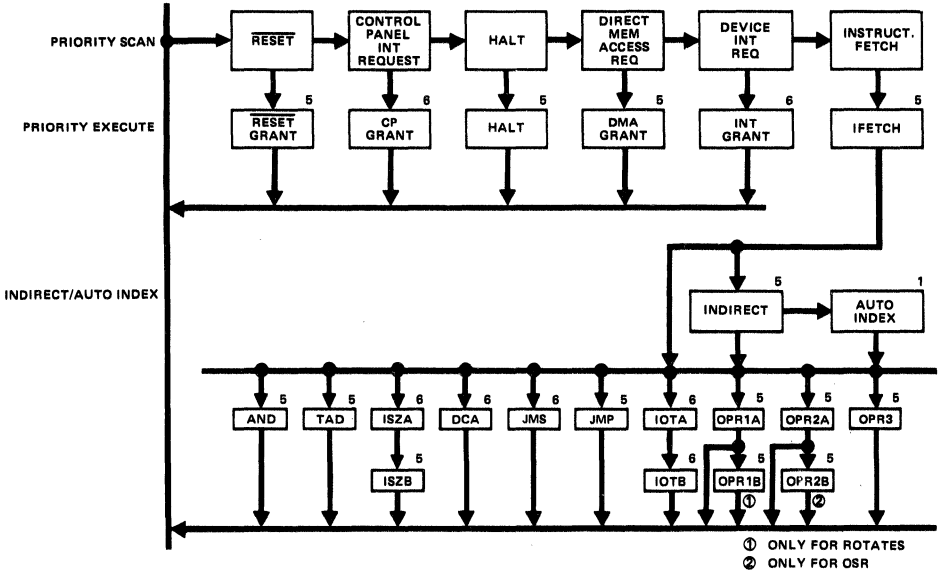


FIGURE 12 – Major processor states and number of clock cycles in each state.

Use of Wait Input

The HM-6100 samples the $\overline{\text{WAIT}}$ line during input-output data transfers. The $\overline{\text{WAIT}}$ line, if active low, controls the transfer duration. If $\overline{\text{WAIT}}$ is active during input transfers (READ), the CPU waits in the T2 state. For an output transfer (WRITE), $\overline{\text{WAIT}}$ controls the time for which the write data is maintained on the DX lines by extending the T6 state. When operating at the max frequency, the internal delay of the HM-6100 causes the falling edge select lines to be past the $\overline{\text{WAIT}}$ setup time for WRITE. The rising edge of the select line for READ can be used to activate $\overline{\text{WAIT}}$ for a WRITE. The wait duration is an integral multiple of the oscillator time period (Figure 13).

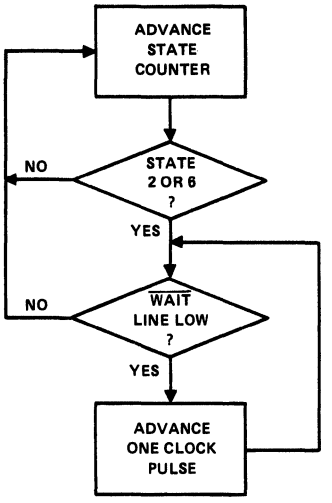


FIGURE 13 – WAIT sequencing steps.

HM-6100 Oscillator Requirements

USING AN EXTERNAL CRYSTAL

An inexpensive crystal can be used thereby eliminating the need for a clock generator. The crystal operates at parallel resonance, and thus is looks inductive in the circuit. An "AT" cut crystal should be used because it has a low temperature coefficient and can be used over a wide temperature range. The Feedback resistor and shunt capacitance are included internally. The crystal parameters needed are:

- Frequency
- Mod of Resonance - Parallel (anti-resonant)
- Maximum Power level - 1 milliwatt
- Load Capacitance - 32pF
- Series Resistance (max) - 250Ω

For precise frequency determination the effect of the stray circuit capacitance and internal 30pF capacitance must be taken into account.

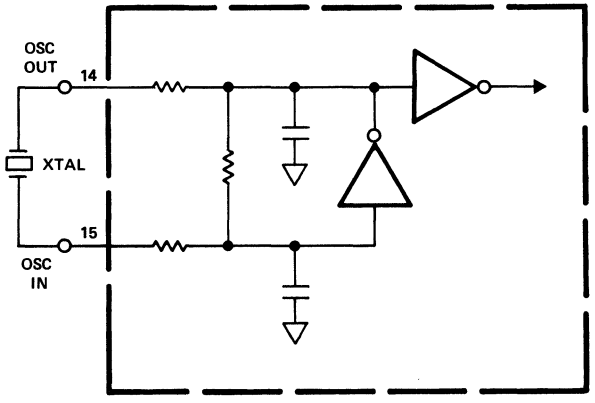


FIGURE 14 – Oscillator input schematic

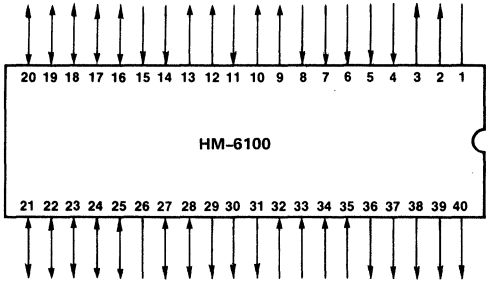
USING AN EXTERNAL CLOCK GENERATOR

When a system clock is needed, eg. for a baud rate generator for UARTs, the HM-6100 can be externally clocked, thus eliminating the need for separate crystals. The external clock can be connected to the oscillator output pin while grounding oscillator input. This has the effect of over driving the small internal oscillator inverter causing an increase in supply current.

Duty cycle - 50/50
T_{rise}, T_{fall} - 20ns

PIN DEFINITIONS

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1	VCC		Supply voltage.
2	RUN	H	The signal indicates the run state of the CPU and may be used to power down the external circuitry
3	DMAGNT	H	Direct Memory Access Grant—DX lines are three-state.
4	$\overline{\text{DMAREQ}}$	L	Direct Memory Access Request—DMA is granted at the end of the current instruction. Upon DMA grant, the CPU suspends program execution until the $\overline{\text{DMAREQ}}$ line is released.
5	$\overline{\text{CPREQ}}$	L	Control Panel Request—a dedicated interrupt which bypasses the normal device interrupt request structure.
6	RUN/$\overline{\text{HLT}}$	L	Pulsing the Run/Halt line causes the CPU to alternately run and halt by changing the state of the internal RUN/$\overline{\text{HLT}}$ flip flop.
7	$\overline{\text{RESET}}$	L	Clears the AC and loads 7777_8 into the PC. CPU is halted.
8	$\overline{\text{INTREQ}}$	L	Peripheral device interrupt request.
9	XTA	H	External coded minor cycle timing—signifies input transfers to the HM-6100.
10	LXMAR	H	The Load External Address Register is used to store memory and peripheral address externally.
11	$\overline{\text{WAIT}}$	L	Indicates that peripherals or external memory is not ready to transfer data. The CPU state gets extended as long as $\overline{\text{WAIT}}$ is active. The CPU is in the lowest power state with clocks running.
12	XTB	H	External coded minor cycle timing—signifies output transfers from the HM-6100.
13	XTC	H	External coded minor cycle timing—used in conjunction with the Select Lines to specify read or write operations.
14	OSC OUT		Crystal input to generate the internal timing (also external clock input).
15	OSC IN		See Pin 14—OSC OUT (also external clock ground)
16	DX0		DataX—multiplexed data in, data out and address lines.
17	DX1		See Pin 16—DX0.
18	DX2		See Pin 16—DX0.
19	DX3		See Pin 16—DX0.
20	DX4		See Pin 16—DX0.



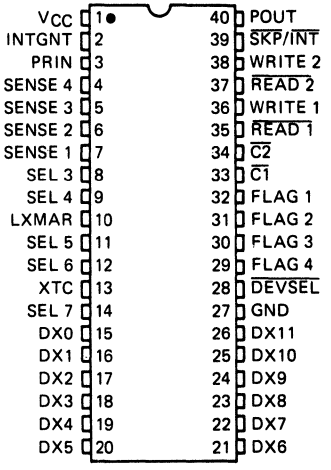
PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
21	DX5		See Pin 16—DX0.
22	DX6		See Pin 16—DX0.
23	DX7		See Pin 16—DX0.
24	DX8		See Pin 16—DX0.
25	DX9		See Pin 16—DX0.
26	GND		Ground
27	DX10		See Pin 16—DX0.
28	DX11		See Pin 16—DX0.
29	LINK	H	Link flip flop.
30	$\overline{\text{DEVSEL}}$	L	Device Select for I/O transfers.
31	$\overline{\text{SWSEL}}$	L	Switch Register Select for the OR THE SWITCH REGISTER INSTRUCTION (OSR). OSR is a Group 2 Operate Instruction which reads a 12 bit external switch register and OR's it with the contents of the AC.
32	$\overline{\text{C0}}$	L	Control line inputs from the peripheral device during an I/O transfer (Table 5).
33	$\overline{\text{C1}}$	L	See Pin 32—C0.
34	$\overline{\text{C2}}$	L	See Pin 32—C0.
35	$\overline{\text{SKP}}$	L	Skips the next sequential instruction if active during an I/O instruction. (Table 5)
36	IFETCH	H	Instruction Fetch Cycle
37	$\overline{\text{MEMSEL}}$	L	Memory Select for memory transfers.
38	$\overline{\text{CPSEL}}$	L	The Control Panel Memory Select becomes active, instead of the $\overline{\text{MEMSEL}}$, for control panel routines. Signal may be used to distinguish between control panel and main memories.
39	INTGNT	H	Peripheral device Interrupt Grant
40	DATAF	H	Data Field pin indicates the execute phase of indirectly addressed AND, TAD, ISZ and DCA instructions so that the data transfers are controlled by the Data Field, DF, and not the Instruction Field, IF, if Extended Memory Control hardware is used to extend the addressing space from 4K to 32K words.

HD-6101
CMOS PARALLEL INTERFACE ELEMENT (PIE)

Features

- HM-6100 COMPATIBLE
- LOW POWER STANDBY -500μW MAX
- SINGLE SUPPLY 4–11 VOLTS
- FULL TEMPERATURE RANGE -55°C TO +125°C
- STATIC OPERATION
- 4 PROGRAMMABLE OUTPUTS (FLAGS)
- 4 PROGRAMMABLE SENSE INPUTS
- CONTROL FOR TWO 12 BIT INPUT PORTS
- CONTROL FOR TWO 12 BIT OUTPUT PORTS
- PRIORITY VECTORED INTERRUPTS
- UP TO 31 PIE'S PER SYSTEM
- 16 INSTRUCTIONS FOR PIE CONTROL

Pinout

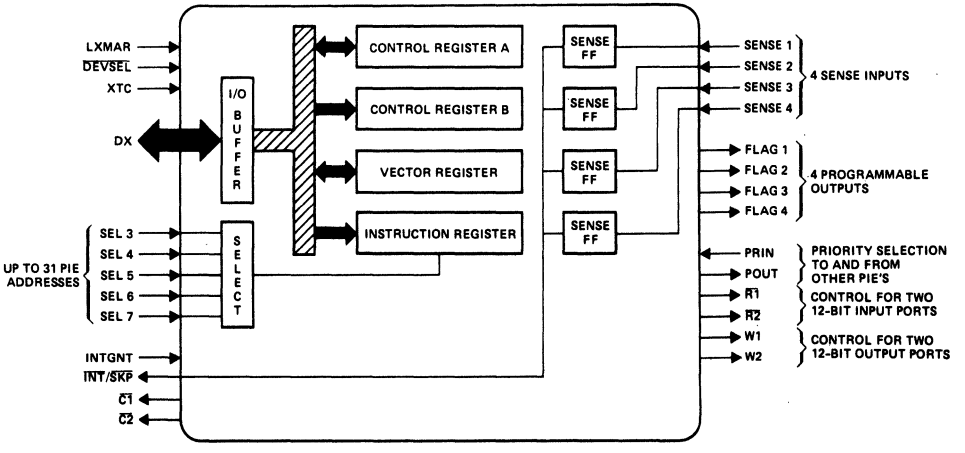


Description

The HD-6101 Parallel Interface Elements (PIE) are high speed, low power, silicon gate CMOS general purpose devices which provide addressing interrupt and control for a variety of peripheral functions, such as UARTs, FIFOs, Keyboards, etc. Data transfers between the HM-6100 CMOS Microprocessor and the HD-6101 are via Input-Output Transfer (IOT) instructions, control lines and DX bus.

Data transfers between peripheral devices and the DX bus are controlled by the PIE via 2 read, 2 write, 4 sense and 4 flag functions. Internal PIE registers are programmed under software control for write polarities, sense levels or edges, flag values and interrupt enables. Another software controlled register stores the address for vectored interrupt operation.

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND - 0.3V) to (VCC + 0.3V)
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6101-9	-40°C to +85°C
Military HD-6101-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0		+1.0	μA	$0V \leqslant V_{IN} \leqslant V_{CC}$
V_{OH}	Logical "1" Output Voltage(1)	2.4			V	I_{OH} = -0.2mA
V_{OL}	Logical "0" Output Voltage			0.45	V	I_{OL} = 2.0mA
I_O	Output Leakage	-1.0		+1.0	μA	$0V \leqslant V_O \leqslant V_{CC}$
I_{CC}	Supply Current (Static)		1.0	100	μA	$V_{IN} = V_{CC}$, Freq. = 0
C_I	Input Capacitance(2)		5	7	pF	
C_O	Output Capacitance(2)		8	10	pF	
C_{IO}	Input/Output Capacitance(2)		8	10	pF	

NOTE: (1) Except pins 33, 34, 39
(2) Guaranteed and sampled, but not 100% tested.

A.C.

		T_A = 25°C V_{CC} = 5.0V(1)		T_A = INDUSTRIAL V_{CC} = 5V ±10%		T_A = MILITARY V_{CC} = 5V ±10%			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
tDR	Delay: $\overline{DEVSEL}$ to $\overline{READ}$		200		300		330	ns	C_L = 50pF
tDW	Delay: $\overline{DEVSEL}$ to WRITE	100	220	140	300	150	330	ns	See Timing
tDF	Delay: $\overline{DEVSEL}$ to FLAG		200		375		415	ns	Diagram
tDC	Delay: $\overline{DEVSEL}$ to $\overline{C1}$, $\overline{C2}$		160		460		510	ns	
tDI	Delay: $\overline{DEVSEL}$ to $\overline{SKP}/\overline{INT}$		210		460		510	ns	
tDA	Delay: $\overline{DEVSEL}$ to DX		350		460		510	ns	
tLX	LXMAR Pulse Width	200		240		265		ns	
tAS	Address Set-Up Time	60		80		90		ns	
tAH	Address Hold Time	100		125		140		ns	
tDS	Data Set-Up Time	50		80		80		ns	
tDH	Data Hold Time	100		100		110		ns	

NOTE (1): All devices guaranteed at worst case limits. Room temperature, 5V data provided for information — not guaranteed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND - 0.3V) to (VCC +0.3V)
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6101C-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±5%; T_A = Industrial

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
D.C.	VIH	Logical "1" Input Voltage	70% VCC			V	
	VIL	Logical "0" Input Voltage			.8	V	
	IIL	Input Leakage	-10		+10	μA	0V ≤ VIN ≤ VCC
	VOH	Logical "1" Output Voltage(1)	2.4			V	IOH = -0.2mA
	VOL	Logical "0" Output Voltage			0.45	V	IOL = 1.6mA
	IO	Output Leakage	-10		+10	μA	0V ≤ VO ≤ VCC
	ICC	Supply Current (Static)		1.0	800	μA	VIN = VCC, Freq. = 0
	CI	Input Capacitance(2)		5	7	pF	
	CO	Output Capacitance(2)		8	10	pF	
	CIO	Input/Output Capacitance(2)		8	10	pF	

NOTES: (1) Except pins 33, 34, 39
(2) Guaranteed and sampled, but not 100% tested.

			T_A = 25°C V_{CC} = 5.0V(1)		T_A = INDUSTRIAL V_{CC} = 5V ±5%			
	SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
A.C.	tDR	Delay: $\overline{DEVSEL}$ to $\overline{READ}$		230		375	ns	C_L = 50pF
	tDW	Delay: $\overline{DEVSEL}$ to WRITE	100	240	125	375	ns	See Timing
	tDF	Delay: $\overline{DEVSEL}$ to FLAG		230		475	ns	Diagram
	tDC	Delay: $\overline{DEVSEL}$ to $\overline{C1}$, $\overline{C2}$		190		560	ns	
	tDI	Delay: $\overline{DEVSEL}$ to $\overline{SKP}/\overline{INT}$		250		560	ns	
	tDA	Delay: $\overline{DEVSEL}$ to DX		400		560	ns	
	tLX	LXMAR Pulse Width	230		300		ns	
	tAS	Address Set-Up Time	80		100		ns	
	tAH	Address Hold Time	120		150		ns	
	tDS	Data Set-Up Time	60		90		ns	
	tDH	Data Hold Time	120		150		ns	

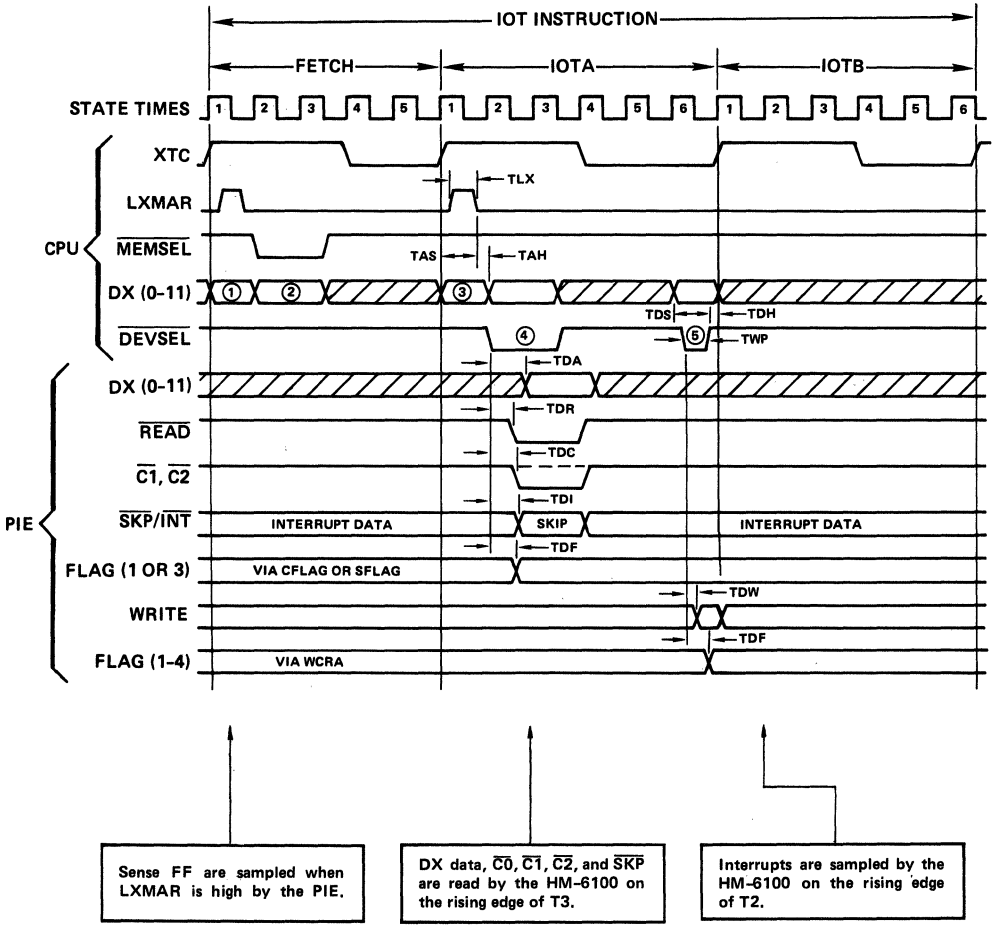
NOTE (1): All devices guaranteed at worst case limits. Room temperature, 5V data provided for information — not guaranteed.

Timing Diagram

Timing for a typical transfer is shown below. During an instruction fetch the processor places the contents of the PC on the bus (1) and obtains from memory an IOT instruction of the form 6XXX (2). During IOTA of the execute phase the processor places that instruction back on the DX lines (3) and pulses LXMAR transferring address and control information for the IOT transfer to all peripheral devices. A low going pulse on $\overline{\text{DEVSEL}}$ while XTC is high (4) is used by the addressed PIE along with the decoded control information to generate CPU control signals $\overline{\text{C1}}$, $\overline{\text{C2}}$, and $\overline{\text{SKP}}$. Also at this time either the Control Register A or the Interrupt Vector Register are outputed on the DX lines, or control outputs $\overline{\text{READ1}}$ and $\overline{\text{READ2}}$ are generated to gate peripheral data to the DX lines. A low going pulse on $\overline{\text{DEVSEL}}$ while XTC is low (5) is used to generate WRITE 1 and WRITE 2 controls. These signals are used to latch accumulator data into peripheral devices.

All PIE timing is generated from HM-6100 signals LXMAR, $\overline{\text{DEVSEL}}$, and XTC. No additional timing signals, clocks, or one shots are required.

Propagation delays, pulse width, data setup and hold times are specified for direct interfacing with the HM-6100.

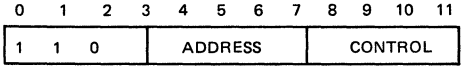


Pie Address and Instructions

The HM-6100 communicates with the PIE and with peripherals through the PIE via IOT commands. During the IOTA cycle an instruction of the form 6XXX is loaded into all PIE instruction registers. The bits are interpreted as shown below.

The 5 address bits (3-7) are compared with the pin programmable select inputs SEL3, SEL4, SEL5, SEL6, SEL7 to address 1 of 31 possible PIEs. Address zero is reserved for IOT's internal to the HM-6100. The four control bits are decoded by the PIE to select one of 16 instructions which are described below.

PIE INSTRUCTION FORMAT



CONTROL	MNEMONICS	ACTION
0000 1000	READ1 READ2	The READ instructions generate a pulse on the appropriate read outputs. This signal is used by the peripheral device to gate onto the DX bus to be "OR'ed" with the HM-6100 accumulator data. The HM-6100 accumulator is cleared prior to reading peripheral data when $\overline{CO}$ is asserted low.
0001 1001	WRITE1 WRITE2	The WRITE instructions generate a pulse on the appropriate write output. This signal is used by peripherals to load the HM-6100 accumulator data on the DX lines into peripheral data registers. The HM-6100 AC is cleared after the write operation when the $\overline{CO}$ input is asserted low.
0010 0011 1010 1011	SKIP1 SKIP2 SKIP3 SKIP4	The SKIP instructions test the state of the sense flip flops. If the input conditions have set the sense flip flop, the PIE will assert the $\overline{SKP}/\overline{INT}$ output causing the HM-6100 to skip the next program instruction. The sense flip flop is then cleared. If the sense flip flop is not set, the PIE not assert the $\overline{SKP}/\overline{INT}$ output and the HM-6100 will execute the next instruction.
0100	RCRA	The Read Control Register A instruction gates the contents of CRA onto the DX lines during time 4 to be "OR" transferred to the HM-6100 AC.
0101 1101 1100	WCRA WCRB WVR	The Write Control Register A, Write Control Register B and Write Vector Register instructions transfer HM-6100 AC data on the DX lines during time 5 of IOTA into the appropriate register.
0110 1110	SFLAG1 SFLAG3	The SET FLAG instructions set the bits FL1 and FL3 in control register A to a high level. PIE outputs FLAG1 and FLAG3 follow the data stored in bits FL1 and FL3 of CRA.
0111 1111	CFLAG1 CFLAG3	The CLEAR FLAG instructions clear the bits FL1 and FL3 in control register A to a low level.
$(6007)_8$	CAF	HM-6100 internal IOT instruction CLEAR ALL FLAGS clears the interrupt requests by clearing the sense flip flops.

Programmable Outputs

FLAGs (1-4) - The FLAGs are general purpose outputs that can be set and cleared under program control. GLAG1 follows bit FL1 in Control Register A and etc. FLAGs can be changed by loading new data into CRA via the WCRA commands. In addition, FLAG1 and FLAG3 can be set and cleared directly by the commands SFLAG1, CFLAG1, SFLAG3 and CFLAG3.

Programmable Sense Inputs

The sense inputs are used to set sense flip flops (SENSE FF) inside the PIE. For each sense input there are two FF's, one for skip and one for interrupt. Conditions for setting each SENSE FF, levels or edges and positive or negative polarities, are set by control bits SL and SP in CRB.

The SENSE FF's are sampled when LXMAR is high. Interrupt requests are generated only when the sense flip flops are set by an edge and interrupts are enabled by writing to control reg A. Sense flip flops are reset on the following conditions.

CONDITION	SENSE FLIP FLOPS	
	SKIP FF	INTERRUPT FF
CAF Instruction (6007$_8$)	Clears All	Clears All
SKIP Instruction	Clears Corresponding FF	Clears Corresponding FF
Vectored Interrupt	Not Cleared	Clears Highest Priority FF on Selected PIE After Vectoring
Interrupt Disabled (IE = "0")	Not Cleared	Disables Interrupt by Holding Corresponding FF in Reset State

Controls for Input and Output Ports

READ (1-2) – The $\overline{\text{READ}}$ outputs are activated by the read instructions and are used by peripheral devices to get data onto the DX lines for transfer to the HM-6100. Read lines are active low.

WRITE (1-2) – The WRITE outputs are activated by the write instructions and are used by peripheral devices to load HM-6100 AC data from the DX lines into peripheral data registers. Output polarity is controlled by the WRITE POLARITY bits of CRA. A logic one causes pulses to be positive while a logic zero causes pulses to be negative.

I/O CONTROL LINES – There are three I/O control lines from the PIE to the microprocessor – $\overline{C1}$, $\overline{C2}$, and $\overline{INT}/\overline{SKP}$. The type of data transfer, during an IOT instruction, is specified by the PIE's assertion of the $\overline{C1}$ and $\overline{C2}$ control lines as shown below.

Interrupt and skip information are time multiplexed on the same line ($\overline{SKP}/\overline{INT}$). Since the HM-6100 samples skip and interrupt data at separate times there is no degradation in system performance. The PIE samples the sense flip flops and generates an interrupt request for enabled bits (IE1-4) when LXMAR is high. Interrupt requests are asserted by the PIE driving the $\overline{INT}/\overline{SKP}$ line low. During IOTA of SKIP instructions the $\overline{INT}/\overline{SKP}$ reflects the SENSE FF data when $\overline{DEVSEL}$ is low and XTC is high. If the SENSE flip flop is set, the $\overline{INT}/\overline{SKP}$ line is driven low to cause the HM-6100 to skip the next instruction. All these outputs are open drain.

CONTROL LINES				OPERATION	DESCRIPTION
$\overline{SKP}$	$\overline{C0}$*	$\overline{C1}$	$\overline{C2}$		
H	H	H	H	PIE ← AC	The contents of the AC is sent to the PIE.
H	H	L	H	AC ← AC V PIE	Data is received from the PIE, OR'ed with the data in the AC and the result stored in the AC.
H	H	L	L	PC ← Vector Address	Vector address received from PIE and loaded into PC. This is referred to as an absolute jump.
L	H	H	H	PC ← PC + 1	Forces Microprocessor to skip next sequential instruction.

NOTE: *The $\overline{C0}$ line must be connected to V_{CC} using a pull-up resistor.

CONTROL REGISTER A (CRA)

The CRA can be read and written by the HM-6100 via the RCRA and WCRA commands.

The format and meaning of control bits are shown below.

FL (1-4) – Data on FLAG outputs corresponds to data in FL (1-4). Changing the FL bits under software control changes the corresponding FLAG outputs.

IE (1-4) – A high level on INTERRUPT ENABLE enables interrupts for the SENSE inputs.

Otherwise these inputs provide conditional skip testing as defined by the SKIP1-4 instructions.

WP (1-2) – A high level on WRITE POLARITY bits causes positive pulses at the WRITE outputs.

0	1	2	3	4	5	6	7	8	9	10	11
FL4	FL3	FL2	FL1	WP2	*	WP1	*	IE4	IE3	IE2	IE1

* = Don't Care

CONTROL REGISTER B (CRB)

The CRB can be written by the HM-6100 via the WCRB instruction. It has no read back capability. The format and meaning of control bits are shown.

SL (1-4) – A high level on the SENSE LEVEL bits causes the SENSE inputs to be level sensitive. A low level in the SL bits causes the SENSE inputs to be edge sensitive. An interrupt request is generated only if a sense line is set up to be edge sensitive and interrupts are enabled via the IE bits of CRA.

SP (1-4) – A high level on the SENSE POLARITY bits causes the flip flop to be set by high level or positive going edge. A low level causes the flip flop to be set by a low level or negative going edge.

0	1	2	3	4	5	6	7	8	9	10	11
SL4	SL3	SL2	SL1	SP4	SP3	SP2	SP1	*	*	*	*

* = Don't Care

VECTOR REGISTER

A hardware priority network uniquely selects a PIE to provide a vectored address. The first IOT command of any type, after the HM-6100 signal INTERRUPT GRANT goes high, resets the INTGNT line to a low level. The INTGNT signal is used to freeze the priority network and enable vector generation. The highest priority PIE has PIN tied to V_{CC}. The lowest priority PIE is the last one on the chain. Within the PIE, SENSE1 has the highest priority and SENSE 4 has the lowest. The vector address generated by the PIE consists of 10 bits from the vector register and two bits that indicate the sense input within the highest priority PIE that generated the interrupt. If PIN is tied to GND, then the PIE will respond as a non-vectored interrupt device.

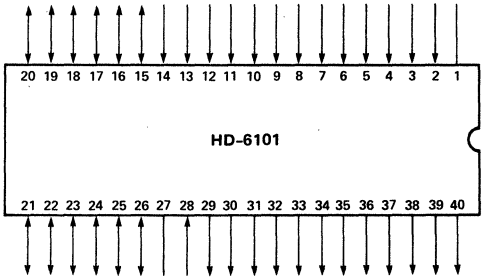
0	1	2	3	4	5	6	7	8	9	10	11
VECTOR REGISTER										VPRI	

VPRI	CONDITIONS
00	SENSE 1
01	SENSE 2
10	SENSE 3
11	SENSE 4

Pin Definitions

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1	V_{CC}		Positive voltage
2	INTGNT	H	A high level on INTERRUPT GRANT inhibits recognition of new interrupt requests and allows the priority chain time to uniquely specify a PIE.
3	PRIN	H	A high level ON PRIORITY IN and an interrupt request will select a PIE for vectored interrupt.
4	SENSE 4	PROG	The SENSE input is controlled by the SL (sense level) and SP (sense polarity) bits of control register B. A high SL level will cause the sense flip flop to be set by a level while a low SL level causes then sense flip flop to be set by an edge. A high SP level will cause the sense flip flop to be set by a positive going edge or high level. A high IE (interrupt enable) level generates an interrupt request whenever the sense flip flop is set by an edge.
5	SENSE 3	PROG	See pin 4 – SENSE 4
6	SENSE 2	PROG	See pin 4 – SENSE 4
7	SENSE 1	PROG	See pin 4 – SENSE 4

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
8	SEL 3	TRUE	Matching SELECT(3-7) inputs with PIE addressing on DX(3-7) during IOTA selects a PIE for programmed input output transfers.
9	SEL 4	TRUE	See Pin 8 – SEL 3
10	LXMAR	H	A positive pulse on LOAD EXTERNAL ADDRESS REGISTER loads address and control data from DX(3-11) into the address register.
11	SEL 5	TRUE	See Pin 8 – SEL 3
12	SEL 6	TRUE	See Pin 8 – SEL 3
13	XTC	H	The XTC input is a timing signal produced by the microprocessor. When XTC is high a low going pulse on $\overline{\text{DEVSEL}}$ initiates a "read" operation. When XTC is low, a low going pulse on $\overline{\text{DEVSEL}}$ initiates a write operation.
14	SEL 7	TRUE	See Pin 8 – SEL 3
15	DX 0	TRUE	Data transfers between the microprocessor and PIE take place via these input/output pins.
16	DX 1	TRUE	See Pin 15 – DX 0
17	DX 2	TRUE	See Pin 15 – DX 0
18	DX 3	TRUE	See Pin 15 – DX 0
19	DX 4	TRUE	See Pin 15 – DX 0
20	DX 5	TRUE	See Pin 15 – DX 0



PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
21	DX 6	TRUE	See Pin 15 – DX 0
22	DX 7	TRUE	See Pin 15 – DX 0
23	DX 8	TRUE	See Pin 15 – DX 0
24	DX 9	TRUE	See Pin 15 – DX 0
25	DX 10	TRUE	See Pin 15 – DX 0
26	DX 11	TRUE	See Pin 15 – DX 0
27	GND		
28	$\overline{\text{DEVSEL}}$	L	The $\overline{\text{DEVSEL}}$ input is a timing signal produced by the microprocessor during IOT instructions. It is used by the PIE to generate timing for controlling PIE registers and "read" and "write" operations.
29	FLAG 4	PROG	The FLAG outputs reflect the data stored in control register A. Flags (1-4) can be set or reset by changing data in CRA via a WRA (write control register A) command. FLAG1 and FLAG3 can be controlled directly by PIE commands SFLAG1, CFLAG1, SFLAG3 and CFLAG3.
30	FLAG 3	PROG	See Pin 29 – FLAG 4
31	FLAG 2	PROG	See Pin 29 – FLAG 4
32	FLAG 1	PROG	See Pin 29 – FLAG 4
33	$\overline{\text{C1}}$	L	The PIE decodes address, control and priority information and asserts outputs $\overline{\text{C1}}$ and $\overline{\text{C2}}$ during the IOTA cycle to control the type of data transfer. These outputs are open drain for bussing and require a pullup register to V_{CC}. $\overline{\text{C1}}$(L), $\overline{\text{C2}}$(L) - vectored interrupt $\overline{\text{C1}}$(L), $\overline{\text{C2}}$(H) - $\overline{\text{READ1}}$, $\overline{\text{READ2}}$ or RRA commands $\overline{\text{C1}}$(H), $\overline{\text{C2}}$(H) - all other instructions

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
34	$\overline{\text{C2}}$	L	See Pin 33 – $\overline{\text{C1}}$
35	$\overline{\text{READ1}}$	PROG	Outputs $\overline{\text{READ1}}$ and $\overline{\text{READ2}}$ are used to gate data from peripheral devices onto the DX bus for input to the **HM-6100** Note the data does not pass through the PIE.
36	WRITE1	PROG	Outputs WRITE1 and WRITE2 are used to gate data from the **HM-6100** DX bus into peripheral devices. Data does not pass through the PIE.
37	$\overline{\text{READ2}}$	PROG	See Pin 35 – $\overline{\text{READ1}}$
38	WRITE2	PROG	See Pin 36 – WRITE1
39	$\overline{\text{SKP/INT}}$	L	The PIE asserts this line low to generate interrupt requests and to signal the **HM-6100** when sense flip flops are set during SKIP instructions. This output is open drain.
40	POUT	H	A high level on priority out indicates no higher priority PIE interrupt requests are outstanding. This output is tied to the PIN input of the next lower priority PIE in the chain.

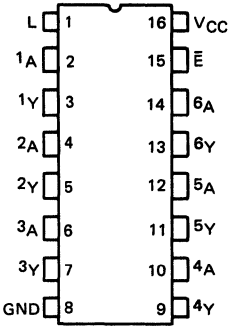
HD-6431
CMOS HEX LATCHING BUS DRIVER

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY — 300pF
- SOURCE CURRENT — 4mA
- SINK CURRENT — 6mA
- PROPAGATION DELAY — 75nsec MAX.

Pinout

TOP VIEW



Truth Table

CONTROL INPUTS		DATA PORT STATUS	
Ē	L	A	Y
H	L	X	HI-Z*
H	H	X	HI-Z
L	↓	X	*
L	H	L	L
L	H	H	H

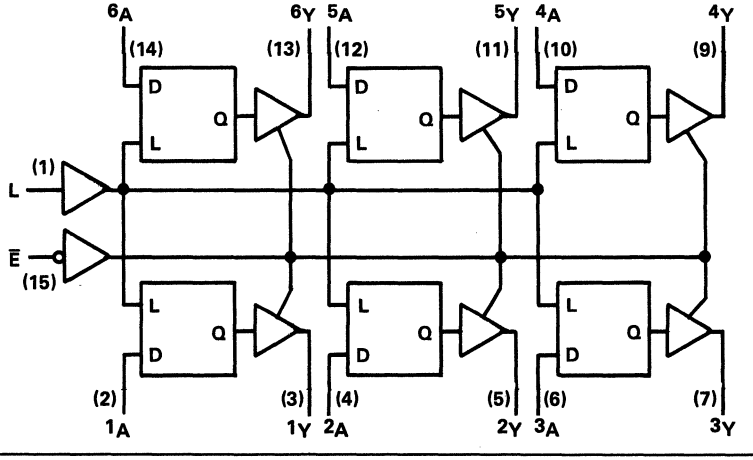
* Data is latched to the value of the last input
X = Don't Care
HI-Z = High Impedance
↓ = Transition from High to Low level

Description

The HD-6431 is a self-aligned silicon gate CMOS Latching Three-State Bus Driver. This circuit consists of 6 non-inverting latching drivers with separate input and output. A high on the strobe line L allows data to go through the latches and a transition to low latches the data. A high on the Three-State control Ē forces the buffers to the high impedance mode without disturbing the latched data. New data may be latched in while the buffers are in the high impedance mode.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6431-9	-40°C to +85°C
Military HD-6431-2/8	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA, $\overline{E}$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA $\overline{E}$ = Low
I_O	Output Leakage	-1.0	1.0	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}$ = High
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

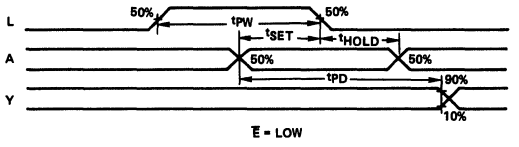
C_L = 300pF

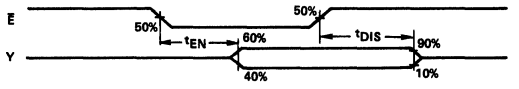
A.C.

		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% T_A = Indus. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		65		75	ns
t_{EN}	Enable Time		80		90	ns
t_{DIS}	Disable Time		80		90	ns
t_{SET}	Input Setup Time	15		15		ns
t_{HOLD}	Input Hold Time	15		15		ns
t_{PW}	Pulse Width	25		30		ns
t_R	Output Rise Time		80		90	ns
t_F	Output Fall Time		70		80	ns

NOTE ① All devices guaranteed at worst case limits. Room temperature, 5V data provided for information-not guaranteed.

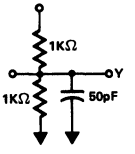
Switching Waveforms





All inputs have t_R, $t_F \leq$ 20ns.

OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS

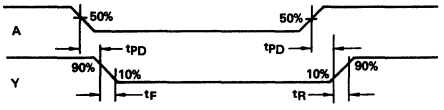


OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. $\left[t_R = 80ns, V_{CC} = 5.0V, \text{each } C_L = 300pF, I_T = (4)\left(300 \times 10^{-12}\right)\frac{5.0 \times 0.8}{80 \times 10^{-9}} = 90mA.\right]$ This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS



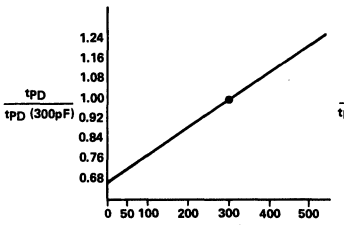


FIGURE 1

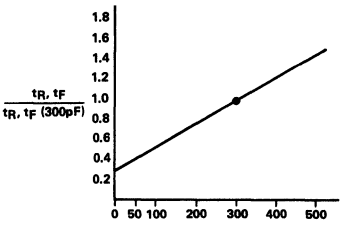


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of ± 10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6431-2. The table of A.C. specs shows the t_{PD} at 4.5V and 125°C is 75nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 75 x 0.84 or 63nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 90nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 90 x 0.65 or 58nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 92nsec. The rise time was used here because it is always the worst case.

HARRIS

HD-6432

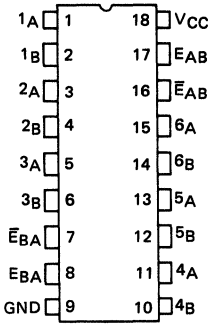
CMOS HEX BI-DIRECTIONAL BUS DRIVER

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY — 300pF
- SOURCE CURRENT — 4mA
- SINK CURRENT — 6mA
- PROPAGATION DELAY — 55nsec MAX.

Pinout

TOP VIEW



Description

The HD-6432 is a self-aligned silicon gate CMOS bi-directional bus driver. This circuit consists of 12 drivers organized as 6 bi-directional pairs. Four enable lines select drive direction or Three-State mode.

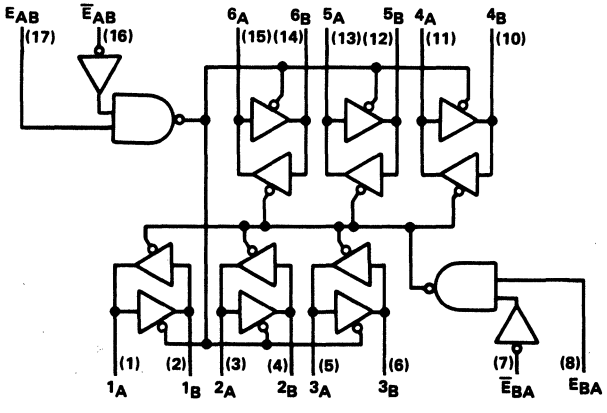
Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Truth Table

CONTROL INPUTS				DATA PORT STATUS	
E_{AB}	$\overline{E}_{AB}$	E_{BA}	$\overline{E}_{BA}$	A	B
L	X	H	L	O	I
X	H	H	L	O	I
H	L	X	H	I	O
H	L	L	X	I	O
L	X	L	X	ISOLATED	
X	H	X	H	ISOLATED	
L	X	X	H	ISOLATED	
X	H	L	X	ISOLATED	
H	L	H	L	NOT ALLOWED	

I = Input, O = Output, X = Don't Care

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6432-9	-40°C to +85°C
Military HD-6432-2/8	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA
I_O	Output Leakage	-1.0	1.0	μA	$0V \leq V_O \leq V_{CC}$, $E_{AB} = E_{BA}$ = Low
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
$C_{I/O}$	I/O Capacitance*		20	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

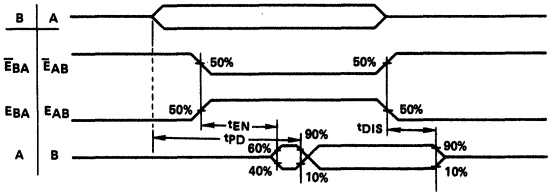
C_L = 300pF

A.C.

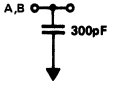
		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% T_A = Indus. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		45		55	ns
t_{EN}	Enable Time		65		75	ns
t_{DIS}	Disable Time		100		110	ns
t_R	Output Rise Time		100		110	ns
t_F	Output Fall Time		70		80	ns

NOTE ①: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information–not guaranteed.

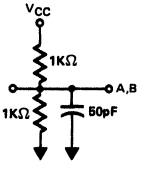
Switching Waveforms



All inputs have t_R, $t_F \leq$ 20ns.



OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS

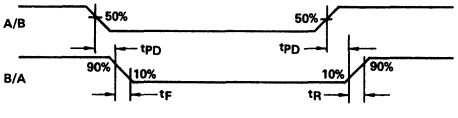


OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The Transient current required to charge the load capacitance is given by $I_T = C \frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = (\Sigma C_L)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. $\left[t_R = 100ns \quad V_{CC} = 5.0V \quad \text{each } C_L = 300pF \quad I_T = (6)\,(300 \times 10^{-12})\frac{5.0 \times 0.8}{100 \times 10^{-9}} = 72mA.\right]$ This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS



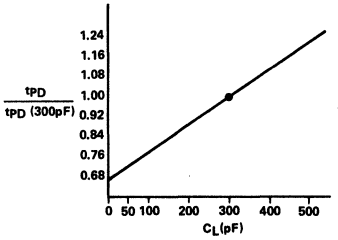


FIGURE 1

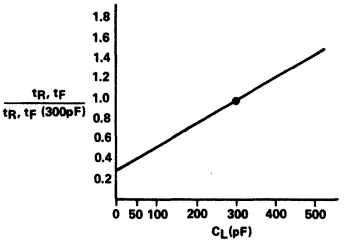


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of ± 10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6432-2. The table of A.C. specs shows the t_{PD} at 4.5V and 125°C is 55nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 55 x 0.84 or 46nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 110nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 110 x 0.65 or 72nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 82nsec. The rise time was used here because it is always the worst case.

HD-6433

CMOS QUAD BUS SEPARATOR/DRIVER

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY — 300pF
- SOURCE CURRENT — 4mA
- SINK CURRENT — 6mA
- PROPAGATION DELAY — 50nsec MAX.

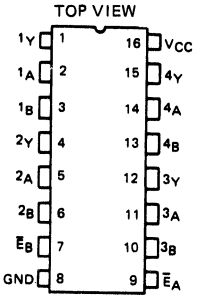
Description

The HD-6433 is a self-aligned silicon gate CMOS bus separator/driver. This circuit consists of 8 drivers organized as 4 pairs of bus separators which allow a unidirectional input bus and a unidirectional output bus to be interfaced with a bi-directional bus.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Pinout

TOP VIEW

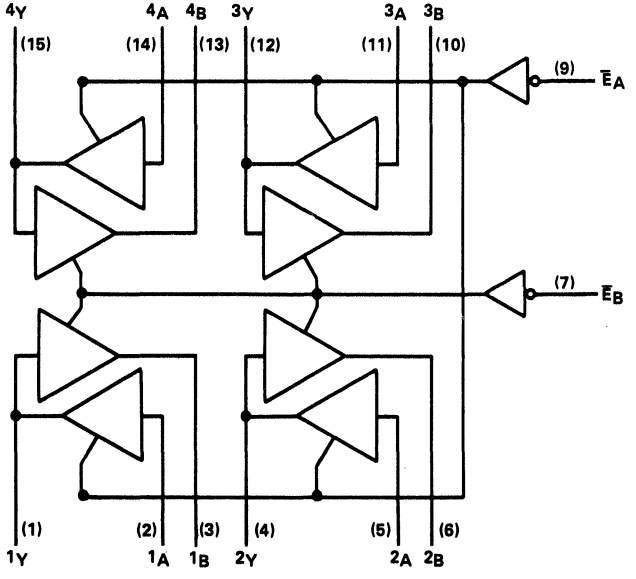


Truth Table

CONTROL INPUTS		FUNCTION		
$\overline{E}_A$	$\overline{E}_B$	A	B	Y
L	L	I	O	O
L	H	I	D	O
H	L	D	O	I
H	H	ISOLATED		

I = Input, O = Output,
D = Disconnected

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6433-9	-40°C to +85°C
Military HD-6433-2/8	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA
I_O	Output Leakage	-1.0	1.0	μA	$0V \leq V_O \leq V_{CC}$ $\overline{E}_A = \overline{E}_B$ = High
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
$C_{I/O}$	I/O Capacitance*		20	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

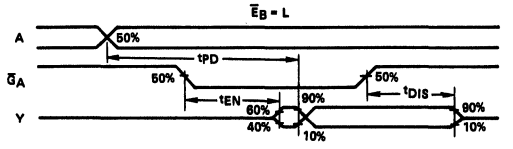
C_L = 300pF

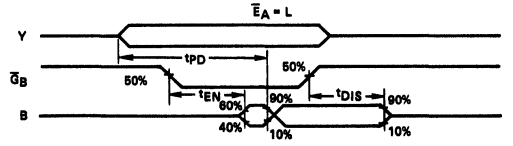
A.C.

		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% TA = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		40		50	ns
t_{EN}	Enable Time		60		70	ns
t_{DIS}	Disable Time		90		100	ns
t_R	Output Rise Time		85		95	ns
t_F	Output Fall Time		70		80	ns

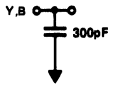
NOTE ① All devices guaranteed at worst case limits. Room temperature, 5V data provided for information-not guaranteed.

Switching Waveforms

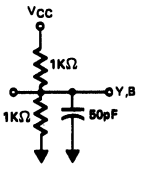




All inputs have t_R, $t_F \leq$ 20ns.



OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS

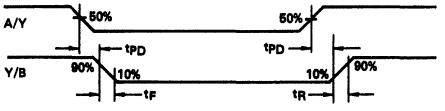


OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. $\left[t_R = 85\text{ns}, V_{CC} = 5.0\text{V}, \text{each } C_L = 300\text{pF}, I_T = (4)\left(300 \times 10^{-12}\right)\frac{5.0 \times 0.8}{85 \times 10^{-9}} = 56.5\text{mA}.\right]$ This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS



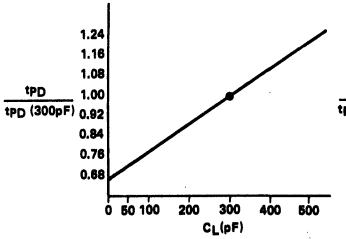


FIGURE 1

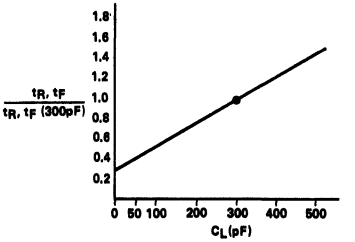


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of ± 10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6433-2. The table of A.C. specs shows the t_{PD} at 4.5V and 125°C is 50nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 50 x 0.84 or 42nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 95nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 95 x 0.65 or 62nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 73nsec. The rise time was used here because it is always the worst case.

HARRIS

HD-6434

CMOS OCTAL RESETTABLE LATCHED BUS DRIVER

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY — 300pF
- SOURCE CURRENT — 6mA
- SINK CURRENT — 9mA
- PROPAGATION DELAY — 50nsec MAX.

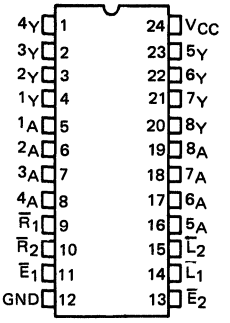
Description

The HD-6434 is a self-aligned silicon gate CMOS latching Three State bus driver. This circuit consists of 8 non-inverting latching drivers with separate input and output. A low on both strobe lines ($\overline{L}$) allows data to go through the latches and a transition to high latches the data. A high on either Three State control ($\overline{E}$) forces the buffers to the high impedance mode without disturbing the latched data. A low on either reset line ($\overline{R}$) forces each of the latches to a low level. New data may be latched in while the buffers are in the high impedance mode.

Qutputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Pinout

TOP VIEW

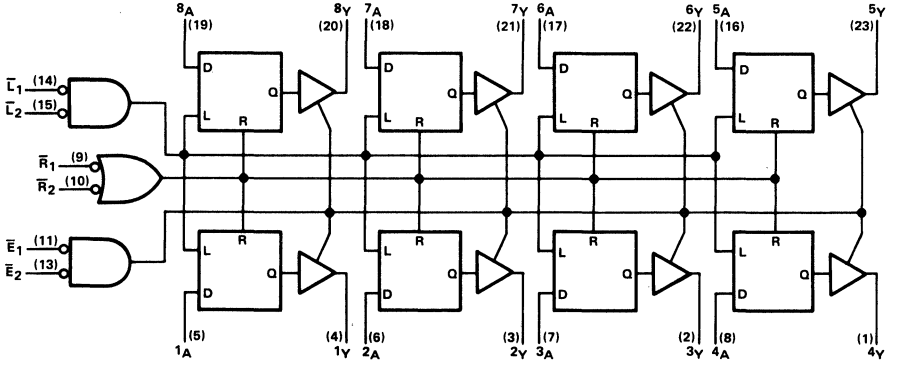


Truth Table

CONTROL INPUTS						DATA	
$\overline{R}_1$	$\overline{R}_2$	$\overline{E}_1$	$\overline{E}_2$	$\overline{L}_1$	$\overline{L}_2$	A	Y
X	X	H	X	X	X	X	Hi-Z
X	X	X	H	X	X	X	Hi-Z
L	X	L	L	X	X	X	L
X	L	L	L	X	X	X	L
H	H	L	L	L	L	L	L
H	H	L	L	L	L	H	H
H	H	L	L	↑	L	X	*
H	H	L	L	L	↑	X	*

X = Don't Care Hi-Z = High Impedance L = Low
H = High * = Data is latched to the value of the last input
↑ = Transition from a Low to High level

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6434-9	-40°C to +85°C
Military HD-6434-2/8	-55°C to +125°C
Operating Voltage Range	+4V to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -6.0mA, $\overline{E}_1 = \overline{E}_2$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 9.0mA $\overline{E}_1 = \overline{E}_2$ = Low
I_O	Output Leakage	-10	10	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}_1 = \overline{E}_2$ = High
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

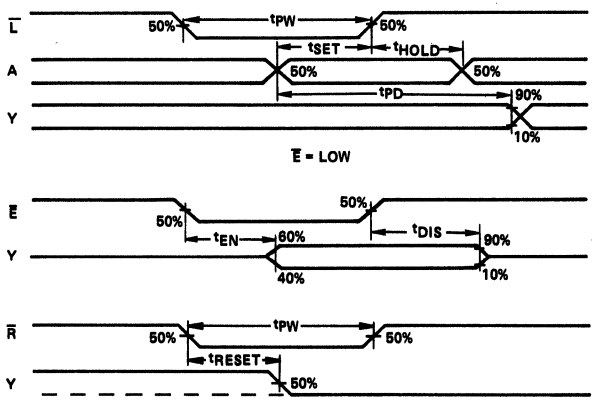
* Guaranteed and sampled, but not 100% tested.

A.C.

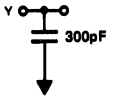
		VCC = 5.0V TEMP = 25°C C_L = 50pF ①	VCC ±5.0V ±10% TEMP = IND OR MIL C_L = 300pF		
SYMBOL	PARAMETER	TYP	MIN	MAX	UNITS
tPD	Propagation Delay	40		50	ns
tEN	Enable Time	45		50	ns
tDIS	Disable Time	45		50	ns
tSET	Input Setup Time	25	35		ns
tHOLD	Input Hold Time	40	45		ns
tPW	Pulse Width	45	65		ns
tR	Output Rise Time	45		50	ns
tF	Output Fall Time	30		50	ns
tRESET	Reset Delay Time	75		125	ns

① All devices guaranteed at worst case limits. Room temperature, 5V, C_L = 50pF data provided for information only - not guaranteed.

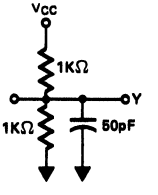
Switching Waveforms



All inputs have t_R, $t_F \leq$ 20ns.



OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS



OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The instantaneous current required to switch a large capacitance load may cause a voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS

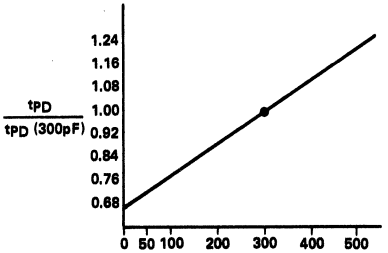


FIGURE 1

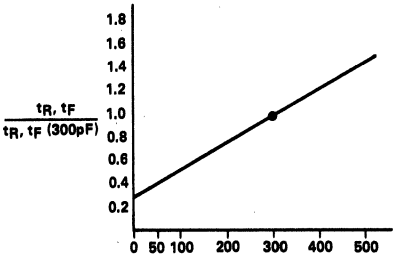


FIGURE 2

TYPICAL CURVES

HD-6436

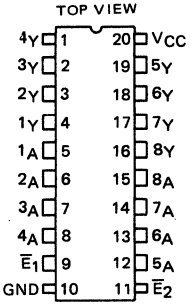
CMOS OCTAL BUS BUFFER/DRIVER

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY — 300pF
- SOURCE CURRENT — 6mA
- SINK CURRENT — 9mA
- PROPAGATION DELAY — 55nsec MAX.

Pinout

TOP VIEW



Description

The HD-6436 is a self-aligned silicon gate CMOS Three State buffer driver. The circuit consists of 8 noninverting buffers with separate inputs and outputs which permit this driver to be used for bi-directional or uni-directional busing. A high on either Three State control line $\overline{E}_1$ or $\overline{E}_2$ will force the drivers to the high impedance mode.

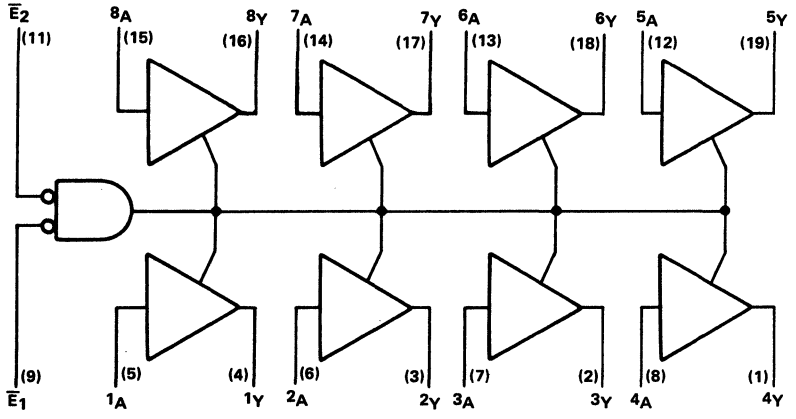
Outputs guaranteed valid at V_{CC} = 2.0V for Battery Backup Applications.

Truth Table

CONTROL INPUTS		INPUT	OUTPUT
$\overline{E}_1$	$\overline{E}_2$	A	Y
L	L	L	L
L	L	H	H
L	H	X	Hi-Z
H	L	X	Hi-Z
H	H	X	Hi-Z

L = Low, H = High
X = Don't Care
Hi-Z = High Impedance

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6436-9	-40°C to +85°C
Military HD-6436-2/8	-55°C to +125°C
Operating Voltage Range	+4V to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	µA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -6.0mA, $\overline{E}_1 = \overline{E}_2$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 9.0mA $\overline{E}_1 = \overline{E}_2$ = Low
I_O	Output Leakage	-10	10	µA	$0V \leq V_O \leq V_{CC}$, $\overline{E}_1 = \overline{E}_2$ = High
I_{CC}	Supply Current		10	µA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

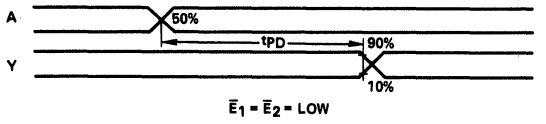
* Guaranteed and sampled, but not 100% tested.

A.C.

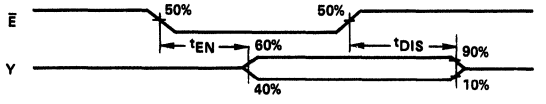
		V_{CC} = 5.0V TEMP = 25°C C_L = 50pF ①	V_{CC} = 5.0V ±10% TEMP = IND OR MIL C_L = 300pF	
SYMBOL	PARAMETER	TYP	MAX	UNITS
tPD	Propagation Delay	35	55	ns
tEN	Enable Time	50	65	ns
tDIS	Disable Time	50	55	ns
tR	Output Rise Time	30	55	ns
tF	Output Fall Time	25	55	ns

① All Devices guaranteed at worst case limits. Room temperature, 5V, C_L = 50pF data provided for information only - not guaranteed.

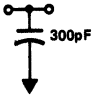
Switching Waveforms



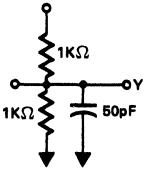
$\overline{E}_1 = \overline{E}_2 = LOW$



All inputs have t_R, $t_F \leq 20ns$.



OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS



OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The instantaneous current required to switch a large capacitance load may cause a voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS

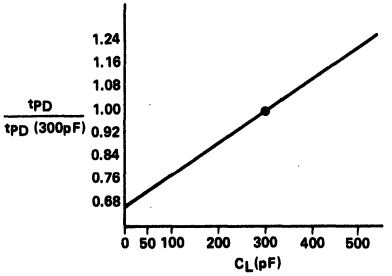


FIGURE 1

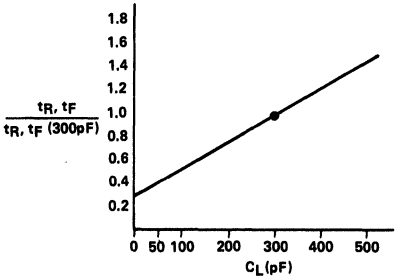


FIGURE 2

TYPICAL CURVES

HD-6440

CMOS LATCHED 3 TO 8 LINE DECODER-DRIVER

Features

- HIGH SPEED DECODING FOR MEMORY ARRAYS
- INCORPORATES 3 ENABLE INPUTS TO SIMPLIFY EXPANSION
- LOW POWER . . . . . TYPICALLY<50μW @ 5V STANBDY
- HIGH NOISE IMMUNITY
- AVAILABLE IN BOTH MILITARY AND INDUSTRIAL TEMPERATURE RANGE
- HIGH CAPACITANCE DRIVE 200pF
- HIGH OUTPUT DRIVE . . . . . I_{OH} = -2mA, I_{OL} = 2.4mA
- SINGLE POWER SUPPLY

Description

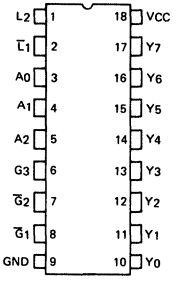
The HD-6440 is a self aligned silicon CMOS gate latched decoder. One of 8 output lines is decoded, and brought to a low state, from the 3 input lines. There are two latch enables ($\overline{L_1}$, L_2), one complemented and one not, to eliminate the need for external gates. The output is enabled by three different output enables ($\overline{G_1}$, $\overline{G_2}$, G_3), two of them complemented and one not. Each output remains in a high state until it is selected, at which time it will go low.

When using high speed CMOS memories, the delay time of the HD-6440 and the enable time of the memory is usually less than the access time of the memory. This assures that memory access time will not be lengthened by the use of the HD-6440 latched decoder driver. The latch is useful for memory mapping or for systems which use a multiplexed bus.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Pinout

TOP VIEW



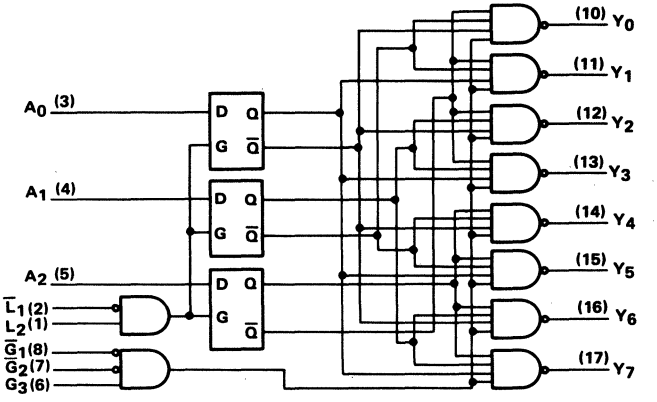
Truth Table

INPUTS																OUTPUTS								
ENABLE						ADDRESS																		
$\overline{G_1}$	$\overline{G_2}$	G_3	$\overline{L_1}$	L_2		A_2	A_1	A_0								Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	FUNCTION
X	X	L	X	X		X	X	X								H	H	H	H	H	H	H	H	DISABLE
X	H	X	X	X		X	X	X								H	H	H	H	H	H	H	H	
H	X	X	X	X		X	X	X								H	H	H	H	H	H	H	H	
L	L	H	L	H		L	L	L								L	H	H	H	H	H	H	H	DECODE
L	L	H	L	H		L	L	H								H	L	H	H	H	H	H	H	
L	L	H	L	H		L	H	L								H	H	L	H	H	H	H	H	
L	L	H	L	H		L	H	H								H	H	H	L	H	H	H	H	
L	L	H	L	H		H	L	L								H	H	H	H	L	H	H	H	
L	L	H	L	H		H	L	H								H	H	H	H	H	L	H	H	
L	L	H	L	H		H	H	L								H	H	H	H	H	H	L	H	
L	L	H	L	H		H	H	H								H	H	H	H	H	H	H	L	
L	L	H	X	L		X	X	X								Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	LATCHED
L	L	H	H	X		X	X	X								Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	

L = Low, H = High, X = Don't Care

Y_n = Data is latched to the value of the last input

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6440-9	-40°C to +85°C
Military HD-6440-2/8	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} - 0.4		V	I_{OH} = -2.0mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 2.4mA
I_{CC}	Supply Current		10	μA	V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

*Guaranteed and sampled, but not 100% tested.

CL = 200pF

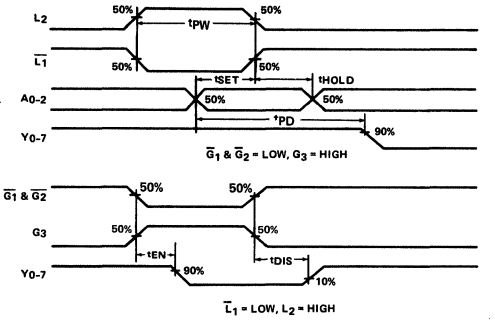
A.C.

		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% T_A = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{SET}	Input Setup Time	20		20		ns
t_{HOLD}	Input Hold Time	20		20		ns
t_{PD}	Propagation Delay		65		100	ns
t_{EN}	Enable Time		50		90	ns
t_{DIS}	Disable Time		50		90	ns
t_{PW}	Pulse Width	30		30		ns
t_R	Output Rise Time		60		90	ns
t_F	Output Fall Time		50		80	ns

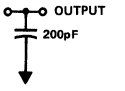
NOTE:

① All devices guaranteed at worse case limits. Room temperature, 5V data provided for information - not guaranteed.

Switching Waveforms



All Inputs have t_R, $t_F \leq 20$ns

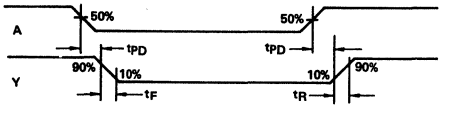


OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS

DECOUPLING CAPACITORS

The Transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. [t_R = 60ns, V_{CC} = 5.0V, each C_L = 200pF, $I_T = (2)(200 \times 10^{-12})\frac{5.0 \times 0.8}{60 \times 10^{-9}} = 26.7$mA.] This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAY



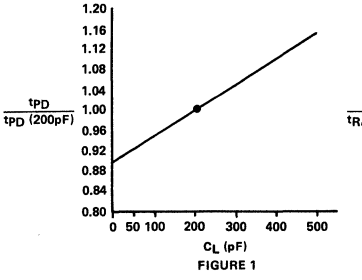


FIGURE 1

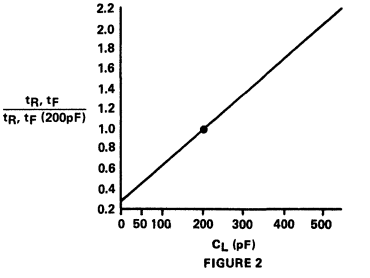


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of ± 10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6440-2. The table of A.C. specs shows the t_{PD} at 4.5V and 125°C is 100nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.97. The adjusted propagation delay, to the 10% or 90% point, is therefore 100 x 0.97 or 97nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 90nsec. Use Figure 2 to find it's degradation multiple to be 0.85. The adjusted rise time is, therefore, 90 x 0.85 or 76.5nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 135nsec. The rise time was used here because it is always the worst case.

Battery Backup Applications

The HD-6440 is especially well suited for use in battery backup systems in conjunction with low power CMOS RAM arrays. When designing a RAM array in conjunction with the HD-6440, the following criteria should be met:

1. As RAM VCC drops, the inputs logical one voltages should follow so as not to exceed VCC +0.3V and logical zero voltages do not go below GND -0.3V.

2. $\overline{G}_1$ or $\overline{G}_2$ must be held high at CMOS VCC, or G_3 held low. $\overline{L}_1$, L_2 and address inputs should be held at either GND or CMOS VCC.

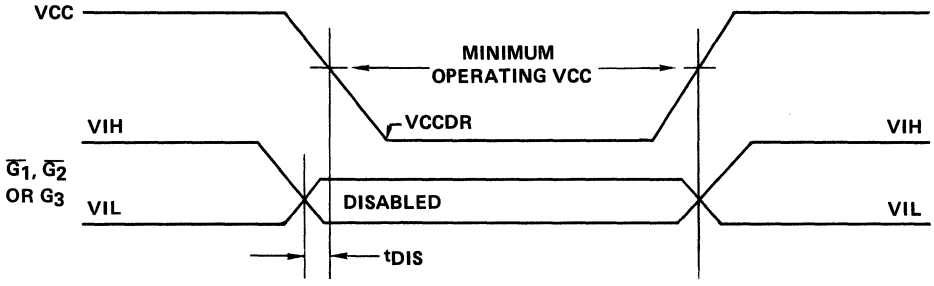
3. Y_0 - Y_7 will maintain a VOH of VCC -0.3 or greater at IOH of 100μA provided the HD-6440 VCC is $\geq$2.0V.

4. When exiting from the battery backup mode, VCC should ramp without ring on discontinuities.

5. The HD-6440 can begin operation when VCC reaches the minimum operating voltage.

6. The HD-6440 should be disabled one t_{DIS} before VCC reaches the minimum operating voltage.

TIMING DIAGRAM



HARRIS

HD-6495

CMOS HEX BUS DRIVER

Features

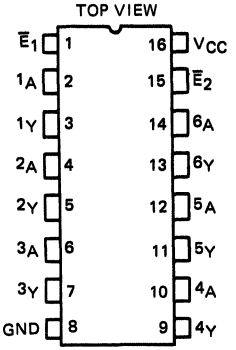
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY — 300pF
- SOURCE CURRENT — 4mA
- SINK CURRENT — 6mA
- PROPAGATION DELAY — 45nsec MAX.

Description

The HD-6495 is a self aligned silicon gate CMOS Three-State buffer driver. The circuit consists of 6 non-inverting buffers with separate inputs and outputs which permit this driver to be used for bi-directional or uni-directional busing. A high on either Three-State control line $\overline{E}_1$ or $\overline{E}_2$ will force the drivers to the high impedance mode.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Pinout

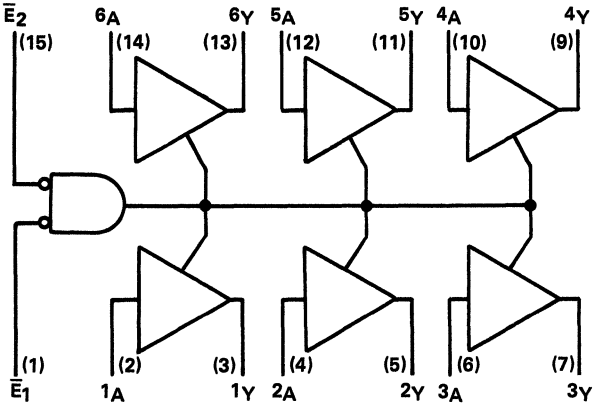


Truth Table

CONTROL INPUTS		INPUT	OUTPUT
$\overline{E}_1$	$\overline{E}_2$	A	Y
L	L	L	L
L	L	H	H
L	H	X	HI-Z
H	L	X	HI-Z
H	H	X	HI-Z

X = DON'T CARE
HI-Z = HIGH IMPEDANCE

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6495-9	-40°C to +85°C
Military HD-6495-2/8	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	µA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA, $\overline{E}_1 = \overline{E}_2$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA $\overline{E}_1 = \overline{E}_2$ = Low
I_O	Output Leakage	-1.0	1.0	µA	$0V \leq V_O \leq V_{CC}$, $\overline{E}_1 = \overline{E}_2$ = High
I_{CC}	Supply Current		10	µA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

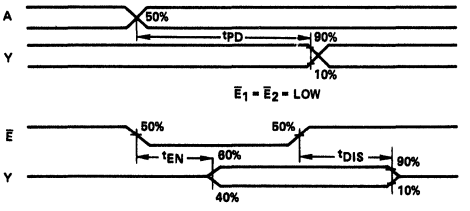
C_L = 300pF

A.C.

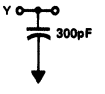
		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ±10% T_A = Indus. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		35		45	ns
t_{EN}	Enable Time		90		100	ns
t_{DIS}	Disable Time		90		100	ns
t_R	Output Rise Time		85		95	ns
t_F	Output Fall Time		65		75	ns

NOTE ① All devices guaranteed at worst case limits. Room temperature, 5V data provided for information–not guaranteed.

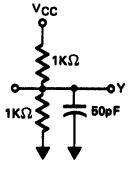
Switching Waveforms



All inputs have t_R, $t_F \leq$ 20ns.



OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS

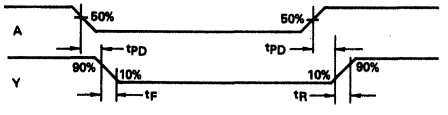


OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. $\left[t_R = 85\text{ns}, V_{CC} = 5.0\text{V}, \text{each } C_L = 300\text{pF}, I_T = (6)\left(300 \times 10^{-12}\right)\frac{5.0 \times 0.8}{85 \times 10^{-9}} = 84.7\text{mA.}\right]$ This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS



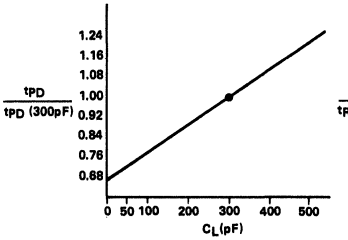


FIGURE 1

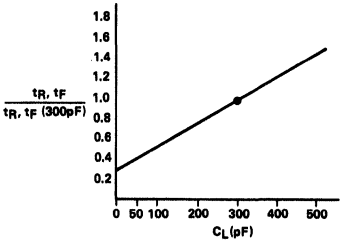


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of ± 10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6495-2. The table of A.C. specs shows the t_{PD} at 4.5V and 125°C is 45nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 45 x 0.84 or 38nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 95nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 95 x 0.65 or 62nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 69nsec. The rise time was used here because it is always the worst case.

82C82

CMOS OCTAL LATCHING BUS DRIVER

Advance Information

Features

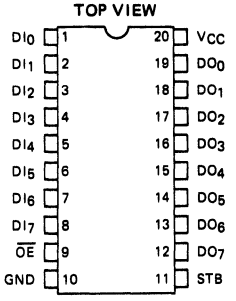
- FULL EIGHT BIT PARALLEL LATCHING BUFFER
- BIPOLAR 8282 COMPATIBLE
- THREE STATE NON-INVERTING OUTPUTS
- PROPAGATION DELAY – 35nsec MAX.
- A.C. CHARACTERISTICS GUARANTEED FOR:
  - ► FULL TEMPERATURE RANGE
  - ► 10% POWER SUPPLY TOLERANCE
  - ► C_L = 300pF
- SINGLE 5V POWER SUPPLY
- POWER SUPPLY CURRENT – 10μA MAX. STANDBY
- OUTPUTS GUARANTEED VALID AT V_{CC} = 2.0 VOLTS
- COMMERCIAL, INDUSTRIAL AND MILITARY TEMPERATURE RANGES
- 20 PIN PACKAGE ON 0.3" CENTERS

Description

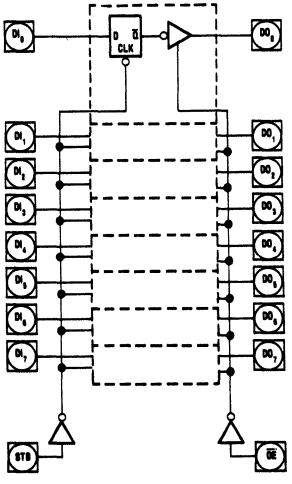
The Harris 82C82 is an octal latching buffer manufactured using a self-aligned silicon gate CMOS process. This circuit provides an eight bit parallel latch/buffer in a 20 pin package. The active high strobe (STB) input allows transparent transfer of data and latches data on the negative transition of this signal. The active low output enable ($\overline{OE}$) permits simple interface to state-of-the-art microprocessor systems.

Pinout

TOP VIEW



Functional Diagram



PIN NAMES

DI_0 - DI_7	Data Input Pins
DO_0 - DO_7	Data Output Pins
STB	Active High Strobe Input
$\overline{OE}$	Active Low Output Enable

Truth Table

STB	$\overline{OE}$	DI	DO
X	H	X	Hi-Z
H	L	L	L
H	L	H	H
↓	L	X	*

H = Logic One Hi-Z = High Impedance
L = Logic Zero ↓ = Negative Transition
X = Don't Care * = Latched to value of last data

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

HARRIS

82C83

CMOS OCTAL LATCHING INVERTING BUS DRIVER

Preview

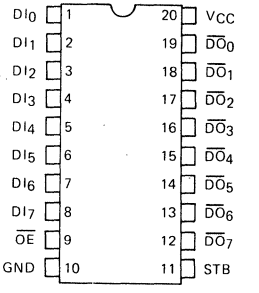
Features

- FULL EIGHT BIT PARALLEL LATCHING INVERTING BUFFER
- BIPOLAR 8283 COMPATIBLE
- THREE STATE NON-INVERTING OUTPUTS
- PROPAGATION DELAY – 35nsec MAX.
- A.C. CHARACTERISTICS GUARANTEED FOR:
  - ▶ FULL TEMPERATURE RANGE
  - ▶ 10% POWER SUPPLY TOLERANCE
  - ▶ C_L = 300pF
- SINGLE 5V POWER SUPPLY
- POWER SUPPLY CURRENT – 10μA MAX. STANDBY
- OUTPUTS GUARANTEED VALID AT V_{CC} = 2.0 VOLTS
- COMMERCIAL, INDUSTRIAL AND MILITARY TEMPERATURE RANGES
- 20 PIN PACKAGE ON 0.3" CENTERS

Description

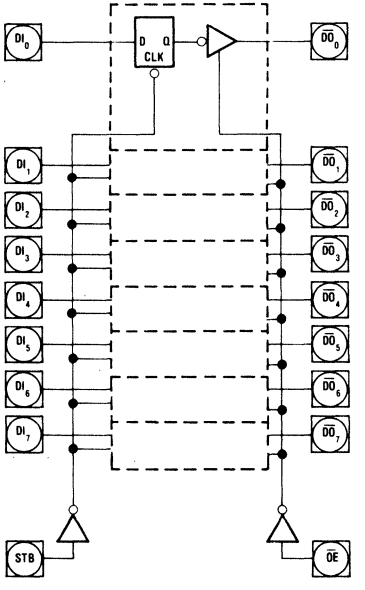
The Harris 82C83 is an octal latching buffer manufactured using a self-aligned silicon gate CMOS process. This circuit provides an eight bit parallel latch/buffer in a 20 pin package. The active high strobe (STB) input allows transparent transfer of data and latches data on the negative transition of this signal. The active low output enable ($\overline{OE}$) permits simple interface to state-of-the-art microprocessor systems. The 82C83 provides inverted data at the outputs.

Pinout



PIN NAMES	
DI_0 - DI_7	Data Input Pins
$\overline{DO}_0$ - $\overline{DO}_7$	Inverted Data Output Pins
STB	Active High Strobe Input
$\overline{OE}$	Active Low Output Enable

Functional Diagram



Truth Table

STB	$\overline{OE}$	DI	$\overline{DO}$
X	H	X	Hi-Z
H	L	L	H
H	L	H	L
↓	L	X	*

H = Logic One
L = Logic Zero
X = Don't Care
Hi-Z = High Impedance
↓ = Negative Transition
* = Latched to value of last data

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

HARRIS

82C86

CMOS OCTAL BUS TRANSCIEVER

Preview

Features

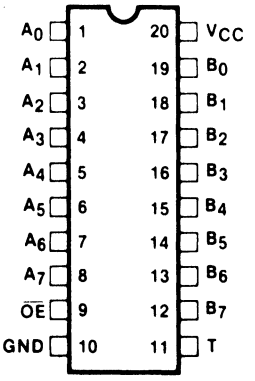
- FULL EIGHT BIT BIDIRECTIONAL BUS INTERFACE
- INDUSTRY STANDARD 8286 COMPATIBLE PINOUT
- THREE STATE NON-INVERTING OUTPUTS
- PROPAGATION DELAY — 35 NSEC
- A.C. CHARACTERISTICS GUARANTEED AT RATED C_L
  - A SIDE - C_L=100pF
  - B SIDE - C_L=300pF
- SINGLE 5V POWER SUPPLY
- POWER SUPPLY CURRENT — 10 μA MAX Standby
- 20 PIN PLASTIC OR CERAMIC PACKAGE
- COMMERCIAL, INDUSTRIAL AND MILITARY TEMPERATURE RANGES AVAILABLE

Description

The Harris 82C86 is an octal bus transceiver manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). This circuit provides a full eight bit bidirectional bus interface in a 20 pin package. The Transmit (T) control determines the data direction. The active low output enable ($\overline{OE}$) allows simple interface to the 80C86 and other microprocessors. The outputs of the 82C86 are non-inverting.

Pinout

TOP VIEW

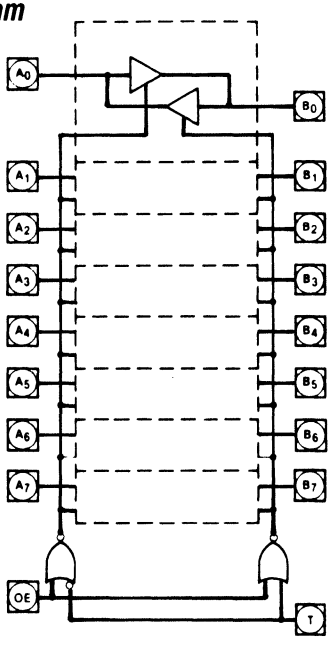


PIN NAMES

A_0-A_7	LOCAL BUS DATA I/O PINS
B_0-B_7	SYSTEM BUS DATA I/O PINS
T	TRANSMIT CONTROL INPUT
OE	ACTIVE LOW OUTPUT ENABLE

4 µP & PERIPHERALS

Functional Diagram



TRUTH TABLE

T	$\overline{OE}$	A	B
X	H	Hi-Z	Hi-Z
H	L	I	O
L	L	O	I

H = logical one
L = logical zero
I = input mode
O = output mode
X = don't care
Hi-Z = high impedance

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

HARRIS

82C87

CMOS OCTAL INVERTING BUS TRANSCEIVER

Preview

Features

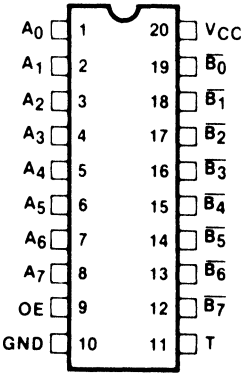
- FULL EIGHT BIT BIDIRECTIONAL BUS INTERFACE
- INDUSTRY STANDARD 8287 COMPATIBLE PINOUT
- THREE STATE INVERTING OUTPUTS
- PROPAGATION DELAY 35 NSEC
- A.C. CHARACTERISTICS GUARANTEED AT RATED C_L
  - A SIDE - $C_L = 100pF$
  - B SIDE - $C_L = 300pF$
- SINGLE 5V POWER SUPPLY
- POWER SUPPLY CURRENT 10 μA MAX Standby
- 20 PIN PLASTIC OR CERAMIC PACKAGE
- COMMERCIAL, INDUSTRIAL AND MILITARY TEMPERATURE RANGES AVAILABLE

Description

The Harris 82C87 is an octal bus transceiver manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). This circuit provides a full eight bit bidirectional bus interface in a 20 pin package. The Transmit (T) control determines the data direction. The active low output enable ($\overline{OE}$) allows simple interface to state of the art microprocessors. Data at the outputs of the 82C87 are inverted.

Pinout

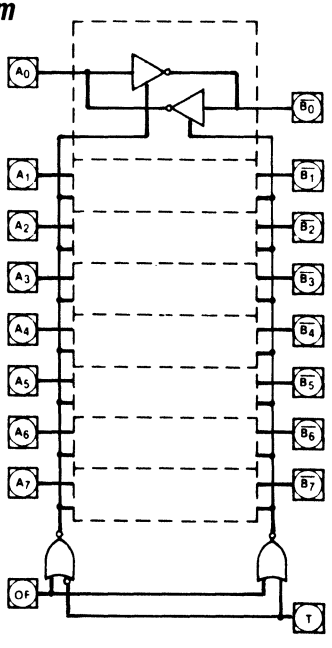
TOP VIEW



PIN NAMES

A_0-A_7	LOCAL BUS DATA I/O PINS
$\overline{B_0}$-$\overline{B_7}$	SYSTEM BUS DATA I/O PINS
T	TRANSMIT CONTROL INPUT
OE	ACTIVE LOW OUTPUT ENABLE

Functional Diagram



TRUTH TABLE

T	$\overline{OE}$	A	$\overline{B}$
X	H	Hi-Z	Hi-Z
H	L	I	0
L	L	0	I

H = logical one
L = logical zero
I = input mode
O = output mode
X = don't care
Hi-Z = high impedance

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

CMOS Data Communications 5

Product Index 5-2

Product Information 5-3

CMOS Data Communication Product Index

		Page
CMOS DATA COMMUNICATION DATA SHEETS		
HD-15530	Manchester Encoder-Decoder	5-3
HD-15531	Manchester Encoder-Decoder	5-10
HD-15531B	Programmable Manchester Encoder-Decoder	5-18
HD-6408	Asynchronous Serial Manchester Adapter	5-25
HD-6409	Manchester Encoder-Decoder	5-30
HD-6406	Programmable Asynchronous Communication Interface	5-39
82C52	Serial Controller Interface	5-50
HD-6402	LSI Universal Asynchronous Receiver Transmitter	5-51
HD-4702	Programmable Bit Rate Generator	5-56

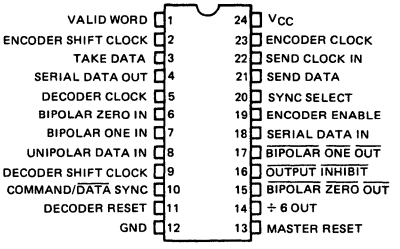
HD-15530

CMOS Manchester Encoder-Decoder

Features

- SUPPORT OF MIL-STD-1553
- 1.25 MEGABIT/SEC DATA RATE
- SYNC IDENTIFICATION AND LOCK-IN
- CLOCK RECOVERY
- MANCHESTER II ENCODE, DECODE
- SEPARATE ENCODE AND DECODE
- LOW OPERATING POWER: 50mW AT 5 VOLTS
- FULL MILITARY TEMPERATURE RANGE

Pinout



Description

The Harris HD-15530 is a high performance CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocals. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate completely independent of each other, except for the Master Reset function.

This circuit meets many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

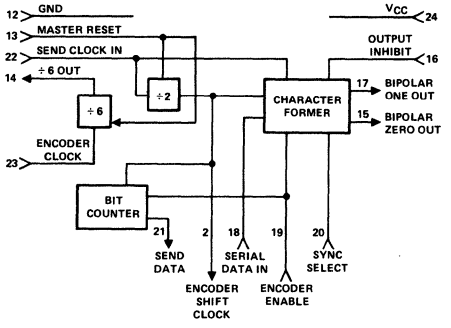
This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over both temperature and voltage. It interfaces with CMOS, TTL or N channel support circuitry, and uses a standard 5 volt supply.

The HD-15530 can also be used in many party line digital data communications applications, such as an environmental control system driven from a single twisted pair cable or fiber optic cable throughout the building.

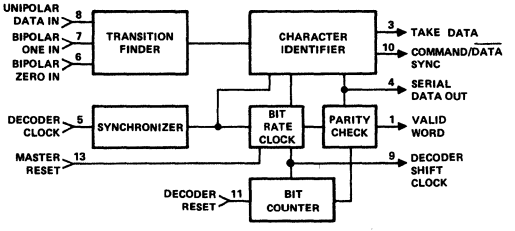
5 DATA COMMUNICATION

Block Diagrams

ENCODER



DECODER



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} + 0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-15530-9	-40°C to +85°C
Military HD-15530-2/8	-55°C to +125°C

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±10% T_A = Industrial or Military

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
	V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
	V_{IHC}	Logical "1" Input Voltage (Clock)	V_{CC} -0.5			V	
	V_{ILC}	Logical "0" Input Voltage (Clock)			GND +0.5	V	
	I_{IL}	Input Leakage	-1.0		+1.0	µA	$0V \leqslant V_{IN} \leqslant V_{CC}$
	V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -3mA
	V_{OL}	Logical "0" Output Voltage			0.4	V	I_{OL} = 1.8mA
	I_{CCSB}	Supply Current Standby		0.5	2	mA	$V_{IN} = V_{CC} = 5.5V$ Outputs Open
	I_{CCOP}	Supply Current Operating*		8.0	10.0	mA	V_{CC} = 5.5V, f = 1MHz
	C_{IN}	Input Capacitance*		5.0	7.0	pF	
	C_O	Output Capacitance*		8.0	10.0	pF	

*Guaranteed and sampled but not 100% tested.

ENCODER TIMING V_{CC} = 5.0V ±10% T_A = Industrial or Military

A.C.	FEC	Encoder Clock Frequency	0		15	MHz	C_L = 50pF
	FESC	Send Clock Frequency	0		2.5	MHz	
	TECR	Encoder Clock Rise Time			8	ns	
	TECF	Encoder Clock Fall Time			8	ns	
	FED	Data Rate	0		1.25	MHz	
	TMR	Master Reset Pulse Width	150			ns	
	TE1	Shift Clock Delay			125	ns	
	TE2	Serial Data Setup	75			ns	
	TE3	Serial Data Hold	75			ns	
	TE4	Enable Setup	90			ns	
	TE5	Enable Pulse Width	100			ns	
	TE6	Sync Setup	55			ns	
	TE7	Sync Pulse Width	150			ns	
	TE8	Send Data Delay	0		50	ns	
	TE9	Bipolar Output Delay			130	ns	

DECODER TIMING V_{CC} = 5.0V ±10% T_A = Industrial or Military

A.C.	FDC	Decoder Clock Frequency	0		15	MHz	C_L = 50pF
	TDCR	Decoder Clock Rise Time			8	ns	
	TDCF	Decoder Clock Fall Time			8	ns	
	FDD	Data Rate	0		1.25	MHz	
	TDR	Decoder Reset Pulse Width	150			ns	
	TDRS	Decoder Reset Setup Time	75			ns	
	TMR	Master Reset Pulse Width	150			ns	
	TD1	Bipolar Data Pulse Width	TDC +10			ns	
	TD2	Sync Transition Span		18TDC		ns	
	TD3	One Zero Overlap			TDC -10	ns	
	TD4	Short Data Transition Span		6TDC		ns	
	TD5	Long Data Transition Span		12TDC		ns	
	TD6	Sync Delay (ON)	-20		110	ns	
	TD7	Take Data Delay (ON)	0		110	ns	
	TD8	Serial Data Out Delay			80	ns	
	TD9	Sync Delay (OFF)	0		110	ns	
	TD10	Take Data Delay (OFF)	0		110	ns	
	TD11	Valid Word Delay	0		110	ns	

NOTE ①: T_{DC} = Decoder Clock Period = $\frac{1}{F_{DC}}$

These parameters are guaranteed but not 100% tested.

Pin Assignments

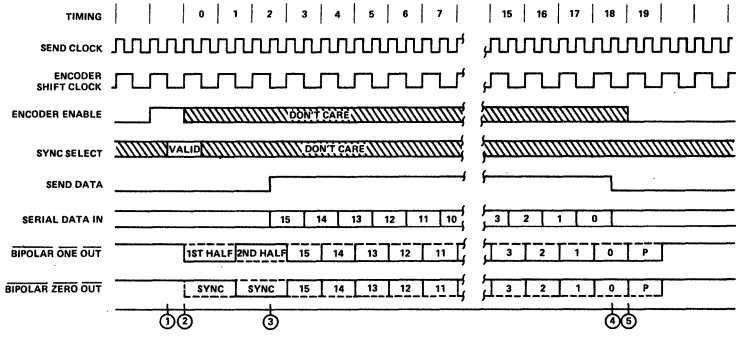
PIN	SECTION	NAME	DESCRIPTION
1	Decoder	VALID WORD	Output high indicates receipt of a valid word.
2	Encoder	ENCODER SHIFT CLOCK	Output for shifting data into the Encoder. This clock shifts data on a low-to-high transition.
3	Decoder	TAKE DATA	Output is high during receipt of data after identification fo a sync pulse.
4	Decoder	SERIAL DATA OUT	Delivers received data in correct NRZ format.
5	Decoder	DECODER CLOCK	Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the Decoder.
6	Decoder	BIPOLAR ZERO IN	A high input should be applied when the bus is in its negative state. This pin must be held high when the Unipolar input is used.
7	Decoder	BIPOLAR ONE IN	A high input should be applied when the bus is in its positive state, this pin must be held low when the Unipolar input is used.
8	Decoder	UNIPOLAR DATA IN	With pin 6 high and pin 7 low, this pin enters unipolar data into the transition finder circuit. If not used this input must be held low.
9	Decoder	DECODER SHIFT CLOCK	Output which delivers a frequency (Decoder Clock ÷ 12), synchronized by the recovered serial data stream.
10	Decoder	COMMAND SYNC	Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character. A low output indicates a Data synchronizing character.
11	Decoder	DECODER RESET	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
12	Both	GROUND	Ground supply pin.
13	Both	MASTER RESET	A high on this pin clears 2:1 counters in both the Encoder and Decoder.
14	Encoder	÷ 6 OUT	Output from 6:1 divider which is driven by the ENCODER CLOCK.
15	Encoder	$\overline{\text{BIPOLAR ZERO OUT}}$	An active low output designed to drive the zero or negative sense of a bipolar line driver.
16	Encoder	$\overline{\text{OUTPUT INHIBIT}}$	A low on this input forces pin 15 and pin 17 high, the inactive states.
17	Encoder	$\overline{\text{BIPOLAR ONE OUT}}$	An active low output designed to drive the one or positive sense of a bipolar line driver.
18	Encoder	SERIAL DATA IN	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
19	Encoder	ENCODER ENABLE	A high on this input initiates the encode cycle. (Subject to the preceding cycle being complete.)
20	Encoder	SYNC SELECT	Actuates command sync for an input high and data sync for an input low.
21	Encoder	SEND DATA	Is an active high output which enables the external source of serial data.
22	Encoder	SEND CLOCK IN	Clock input at a frequency equal to the data rate X2.
23	Encoder	ENCODER CLOCK	Input to the 6:1 divider.
24	Both	V_{CC}	Positive supply pin.

Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxillary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the DECODER CLOCK.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK ①. This cycle lasts for one word length or twenty ENCODER SHIFT CLOCK periods. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high at SYNC SELECT input actuates a command sync or a low will produce a data sync for that word ② . When the Encoder is ready to accept data, the SEND DATA output will go high and remain high for sixteen ENCODER SHIFT CLOCK periods ③ . During these sixteen periods the data should be clocked into the SERIAL DATA input with every low-to-high transition of the ENCODER SHIFT CLOCK ③ – ④ . After the sync and the Manchester II coded data are transmitted through the $\overline{\text{BIPOLAR ONE}}$ and $\overline{\text{BIPOLAR ZERO}}$ outputs, the Encoder adds on an additional bit which is the parity for that word ⑤ . At any time a low on $\overline{\text{OUTPUT INHIBIT}}$ input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Anytime after or during this pulse, a low to high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.



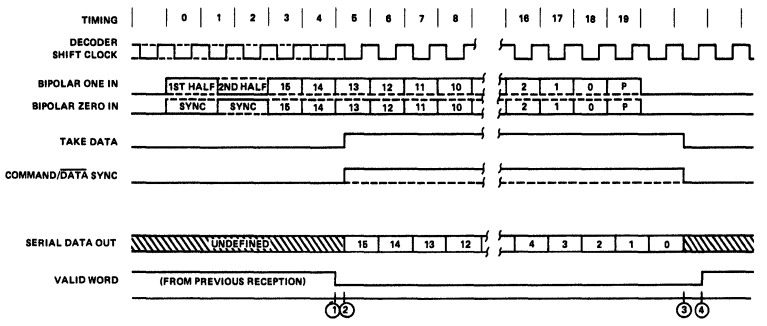
Decoder Operation

The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept non-inverted Manchester II coded data. (e.g. from $\overline{\text{BIPOLAR ZERO OUT}}$ of an Encoder.)

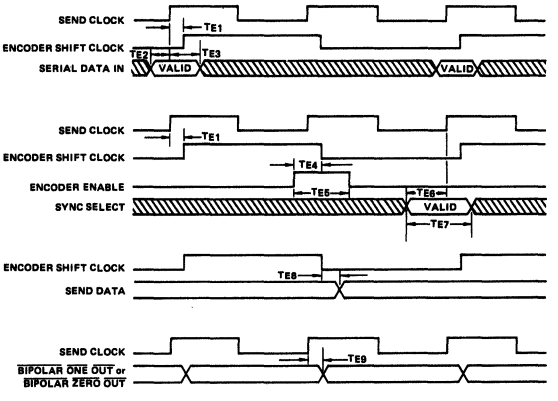
The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ① , the type of sync is indicated on COMMAND/$\overline{\text{DATA}}$ SYNC output. If the sync character was a command sync, this output will go high ② and remain high for sixteen DECODER SHIFT CLOCK periods ③ , otherwise it will remain low. The TAKE DATA output will go high and remain high ② – ③ while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in a NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can get shifted into an external register on every low-to-high transition of this clock ② – ③ .

After all sixteen decoded bits have been transmitted ③ the data is checked for odd parity. A high on VALID WORD output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence.

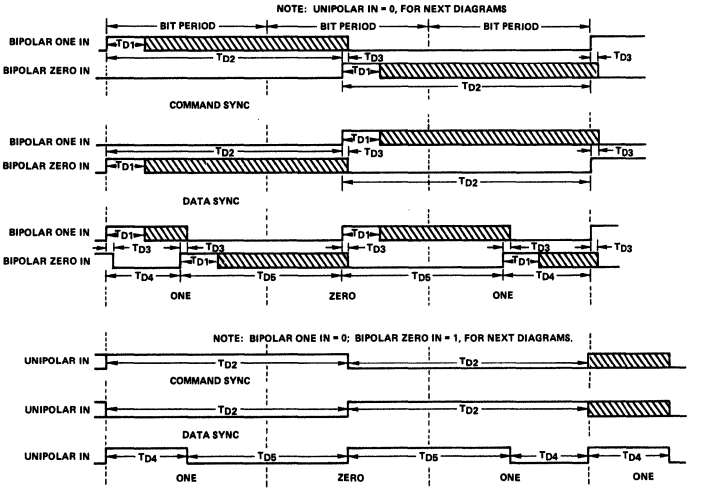
At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.

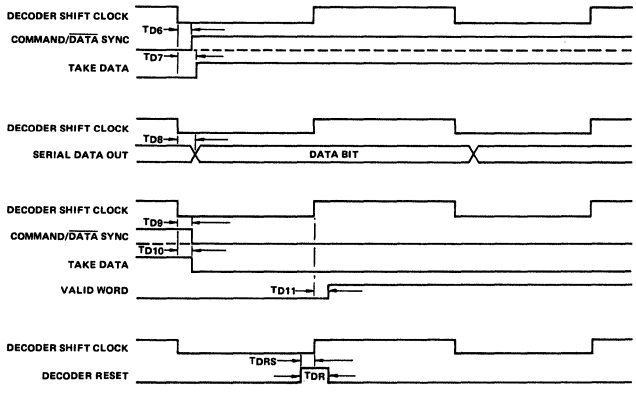


Encoder Timing



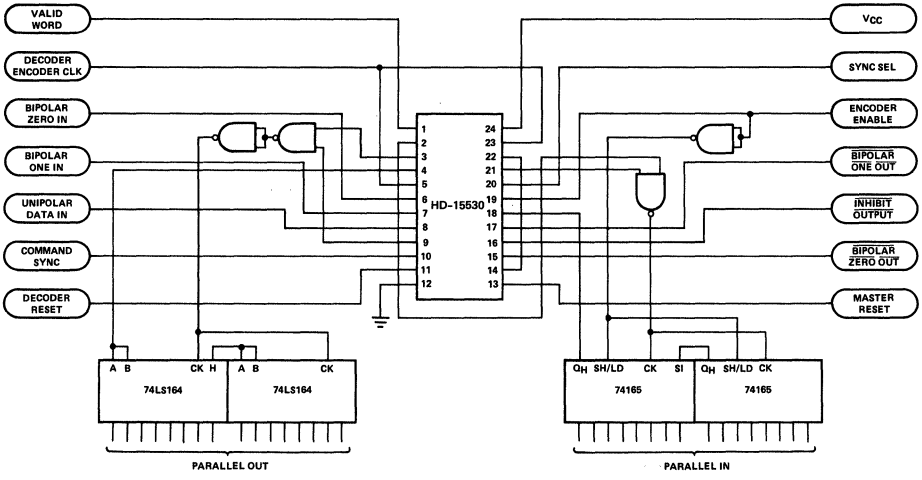
Decoder Timing



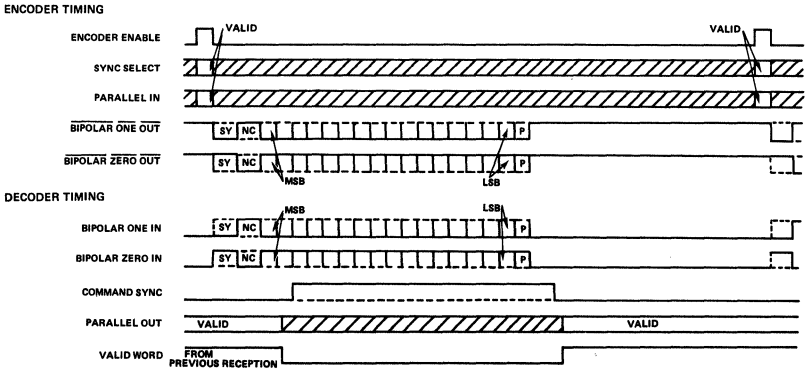


Applications

How to Make Our MTU Look Like a Manchester Encoded UART



Typical Timing Diagrams for a Manchester Encoded UART



The 1553 standard defines a time division multiplexed data bus for application within aircraft. The bus is defined to be bipolar, and encoded in a Manchester II format, so no DC component appears on the bus. This allows transformer coupling and excellent isolation among systems and their environment.

The HD-15530 supports the full bipolar configuration, assuming a bus driver configuration similar to that in Figure 1. Bipolar inputs from the bus, like Figure 2, are also accommodated.

The signaling format in MIL-STD-1553 is specified on the assumption that the network of 32 or fewer terminals are controlled by a central control unit by means of Command Words. Terminals respond with Status Words. These control words reference Data Words. Each word is preceded by a synchronizing pulse, and followed by parity bit, occupying a total of 20μsec. The word formats are shown in Figure 4. The special abbreviations are as follows:

- P — Parity, which is defined to be odd, taken across all 17 bits.
- R/T — Receive on logical zero, transmit on ONE.
- ME — Message Error if logical 1.
- TF — Terminal Flag, if set, calls for controller to request self-test data.

The paragraphs above are intended only to suggest the content of MIL-STD-1553 and do not completely describe its bus requirements, timing or protocols.

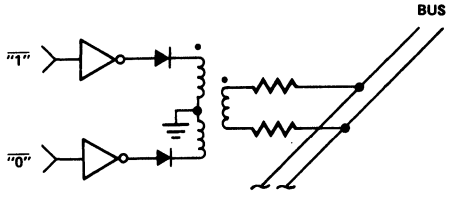


FIGURE 1 – Simplified MIL-STD- 1553 Driver

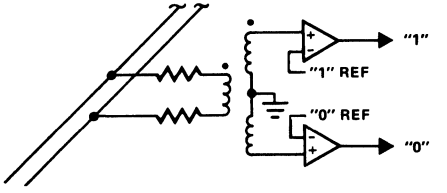


FIGURE 2 – Simplified MIL-STD-1553 Receiver

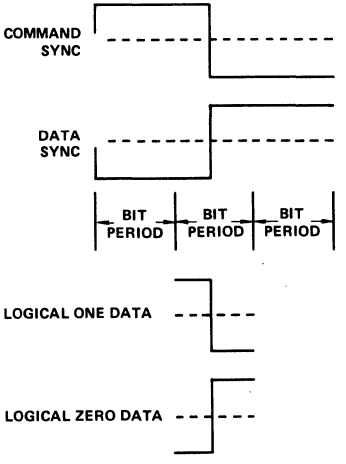


FIGURE 3 – MIL-STD-1553 Character Formats

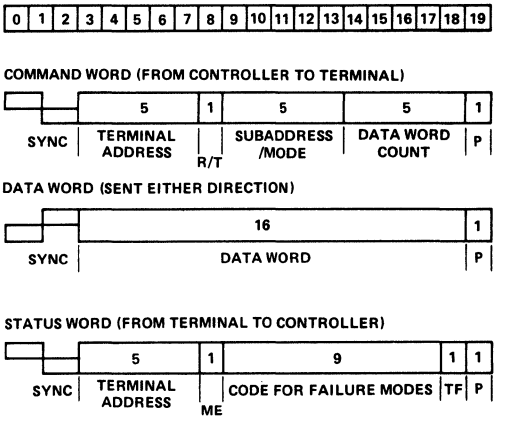


FIGURE 4 – MIL-STD-1553 Word Formats

NOTE: This page is a summary of MIL-STD-1553 and is not intended to describe the operation of the HD-15530.

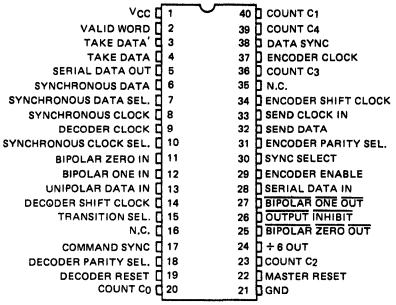
HARRIS HD-15531

CMOS Manchester Encoder-Decoder

Features

- SUPPORT OF MIL-STD-1553
- 1.25 MEGABIT/SEC DATA RATE
- SYNC IDENTIFICATION AND LOCK-IN
- CLOCK RECOVERY
- VARIABLE FRAME LENGTH TO 32 BITS
- MANCHESTER II ENCODE, DECODE
- SEPARATE ENCODE AND DECODE
- LOW OPERATING POWER: 50mW @ 5 VOLTS
- FULL MILITARY TEMPERATURE RANGE

Pinout



Description

The Harris HD-15531 is a high performance CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocals. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate independently of each other, except for the Master Reset and frame length functions.

This circuit provides many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

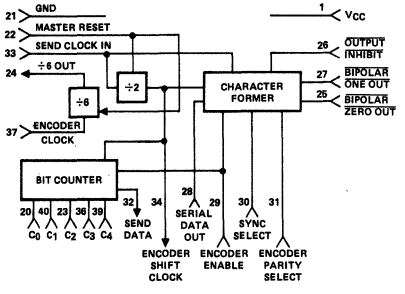
The HD-15531 also surpasses the requirements of MIL-STD-1553 by allowing the frame length to be programmable. The frame length may be programmed from 2 to 28 data bits plus sync and parity. This chip also allows selection of either even or odd parity for the Encoder and Decoder separately.

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over both temperature and voltage. It interfaces with CMOS, TTL or N channel support circuitry, and uses a standard 5 volt supply.

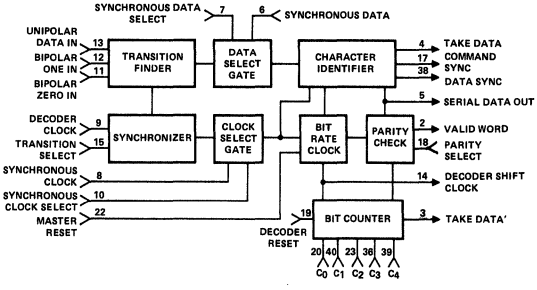
The HD-15531 can also be used in many party line digital data communications applications, such as an environmental control system driven from a single twisted pair of fiber optic cable throughout a building.

Block Diagrams

ENCODER



DECODER



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow standard I.C. Handling Procedures.

The 1553 standard defines a time division multiplexed data bus for application within aircraft. The bus is defined to be bipolar, and encoded in a Manchester II format, so no DC component appears on the bus. This allows transformer coupling and excellent isolation among systems and their environment.

The HD-15531 supports the full bipolar configuration, assuming a bus driver configuration similar to that in Figure 1. Bipolar inputs from the bus, like Figure 2, are also accommodated.

The signaling format in MIL-STD-1553 is specified on the assumption that the network of 32 or fewer terminals are controlled by a central control unit by means of Command Words, and Data. Terminals respond with Status Words, and Data. Each word is preceded by a synchronizing pulse, and followed by parity bit, occupying a total of 20 μ sec. The word formats are shown in Figure 4. The special abbreviations are as follows:

P	Parity, which is defined to be odd, taken across all 17 bits.
R/T	Receive on logical zero, transmit on ONE.
ME	Message Error if logical 1.
TF	Terminal Flag, if set, calls for controller to request self-test data.

The paragraphs above are intended only to suggest the content of MIL-STD-1553, and do not completely describe its bus requirements, timing or protocols.

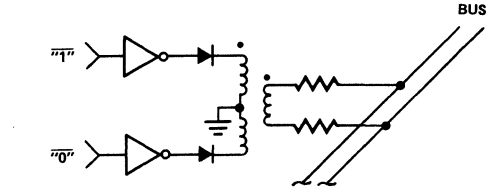


FIGURE 1 – Simplified MIL-STD-1553 Driver

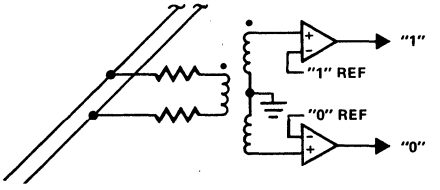


FIGURE 2 – Simplified MIL-STD-1553 Receiver

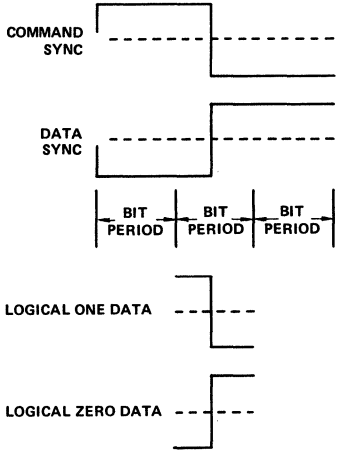


FIGURE 3 – MIL-STD-1553 Character Formats

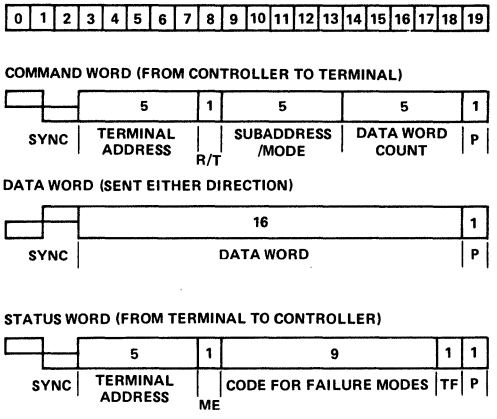


FIGURE 4 – MIL-STD-1553 Word Formats

NOTE: This page is a summary of MIL-STD-1553 and is not intended to describe the operation of the HD-15531.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-15531-9	-40°C to +85°C
Military HD-15531-2/8	-55°C to +125°C

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±10% T_A = Industrial or Military

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
D.C.	VIH	Logical "1" Input Voltage	70% VCC			V	
	VIL	Logical "0" Input Voltage			20% VCC	V	
	VIHC	Logical "1" Input Voltage (Clock)	VCC -0.5			V	
	VILC	Logical "0" Input Voltage (Clock)			GND +0.5	V	
	IIL	Input Leakage	-1.0		+1.0	µA	0V ≤ VIN ≤ VCC
	VOH	Logical "1" Output Voltage	2.4			V	IOH = -3mA
	VOL	Logical "0" Output Voltage			0.4	V	IOL = 1.8mA
	ICCSB	Supply Current Standby		0.5	2.0	mA	VIN = VCC = 5.5V Outputs Open
	ICCOP	Supply Current Operating*		8.0	10.0	mA	VCC = 5.5V, f = 15MHz
	CIN	Input Capacitance*		5.0	7.0	pF	
	CO	Output Capacitance*		8.0	10.0	pF	
		*Guaranteed and sampled but not 100% tested.					
	ENCODER TIMING						
A.C.	FEC	Encoder Clock Frequency	0		15	MHz	CL = 50pF
	FESC	Send Clock Frequency	0		2.5	MHz	
	TECR	Encoder Clock Rise Time			8	ns	
	TECF	Encoder Clock Fall Time			8	ns	
	FED	Data Rate	0		1.25	MHz	
	TMR	Master Reset Pulse Width	150			ns	
	TE1	Shift Clock Delay			125	ns	
	TE2	Serial Data Setup	75			ns	
	TE3	Serial Data Hold	75			ns	
	TE4	Enable Setup	90			ns	
	TE5	Enable Pulse Width	100			ns	
	TE6	Sync Setup	55			ns	
	TE7	Sync Pulse Width	150			ns	
	TE8	Send Data Delay	0		50	ns	
	TE9	Bipolar Output Delay			130	ns	
	DECODER TIMING						
A.C.	FDC	Decoder Clock Frequency	0		15	MHz	CL = 50pF
	FDS	Decoder Synchronous Clock	0		2.5	MHz	
	TDCR	Decoder Clock Rise Time			8	ns	
	TDCF	Decoder Clock Fall Time			8	ns	
	FDD	Data Rate	0		1.25	MHz	
	TDR	Decoder Reset Pulse Width	150			ns	
	TDRS	Decoder Reset Setup Time	75			ns	
	TMR	Master Reset Pulse Width	150			ns	
	TD1	Bipolar Data Pulse Width	TDC +10			ns	①
	TD2	Sync Transition Span		18TDC		ns	①
	TD3	One Zero Overlap			TDC -10	ns	①
	TD4	Short Data Transition Span		6TDC		ns	①
	TD5	Long Data Transition Span		12TDC		ns	①
	TD6	Sync Delay (ON)	-20		110	ns	
	TD7	Take Data Delay (ON)	0		110	ns	
	TD8	Serial Data Out Delay			80	ns	
	TD9	Sync Delay (OFF)	0		110	ns	
	TD10	Take Data Delay (OFF)	0		110	ns	
	TD11	Valid Word Delay	0		110	ns	
	TD12	Synchronous Clock To Shift Clock Delay			75	ns	
	TD13	Synchronous Data Setup	75			ns	

NOTE ①: T_{DC} = Decoder Clock Period = $\frac{1}{F_{DC}}$

These parameters are guaranteed but not 100% tested.

Pin Assignments

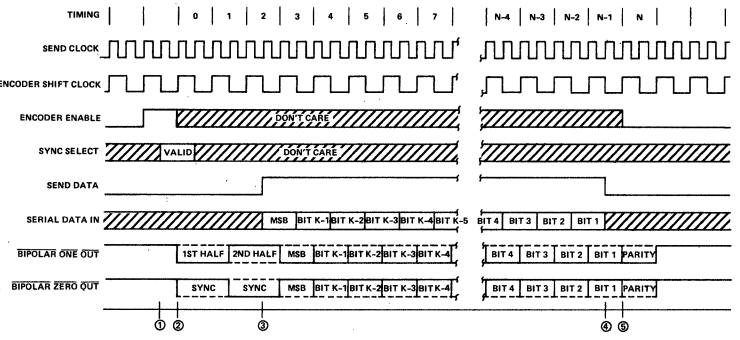
PIN	SECTION	NAME	DESCRIPTION
1	Both	VCC	Positive supply pin.
2	Decoder	VALID WORD	Output high indicates receipt of a valid word.
3	Decoder	TAKE DATA'	A continuous, free running signal provided for host timing or data handling. When data is present on the bus, this signal will be synchronized to the incoming data and will be identical to take data.
4	Decoder	TAKE DATA	Output is high during receipt of data after identification of a sync pulse
5	Decoder	SERIAL DATA OUT	Delivers received data in correct NRZ format.
6	Decoder	SYNCHRONOUS DATA	Input presents Manchester data directly to character identification logic. SYNCHRONOUS DATA SELECT must be held high to use this input. If not used this pin should be held high.
7	Decoder	SYNCHRONOUS DATA SELECT	In high state allows the synchronous data to enter the character identification logic.
8	Decoder	SYNCHRONOUS CLOCK	Input provides externally synchronized clock to the decoder. This input should be tied high when not in use.
9	Decoder	DECODER CLOCK	Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the decoder.
10	Decoder	SYNCHRONOUS CLOCK SELECT	In high state directs the SYNCHRONOUS CLOCK to control the decoder character identification logic. A low state selects the DECODER CLOCK
11	Decoder	BIPOLAR ZERO IN	A high input should be applied when the bus is in its negative state. This pin must be held high when the unipolar input is used.
12	Decoder	BIPOLAR ONE IN	A high input should be applied when the bus is in its positive state. This pin must be held low when the unipolar input is used.
13	Decoder	UNIPOLAR DATA IN	With pin 11 high and pin 12 low, this pin enters unipolar data into the transition finder circuit. If not used this input must be held low.
14	Decoder	DECODER SHIFT CLOCK	Output which delivers a frequency (DECODER CLOCK ÷ 12), synchronized by the recovered serial data stream.
15	Decoder	TRANSITION SELECT	A high input to this pin causes the transition finder to synchronize on every transition of input data. A low input causes the transition finder to synchronize only on mid-bit transitions.
16	Blank	N.C.	Not connected.
17	Decoder	COMMAND SYNC	Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character
18	Decoder	DECODER PARITY SELECT	An input for parity sense, calling for even parity with input high and odd parity with input low.
19	Decoder	DECODER RESET	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
20	Both	COUNT C_0	One of five binary inputs which establish the total bit count to be encoded or decoded.
21	Both	GROUND	Supply pin.
22	Both	MASTER RESET	A high on this pin clears 2:1 counters in both the encoder and decoder.
23	Both	COUNT C_2	See pin 20.
24	Encoder	÷ 6 OUT	Output from 6:1 divider which is driven by the ENCODER CLOCK.
25	Encoder	$\overline{\text{BIPOLAR ZERO OUT}}$	An active low output designed to drive the zero or negative sense of a bipolar line driver.
26	Encoder	$\overline{\text{OUTPUT INHIBIT}}$	A low on this pin forces pin 25 and 27 high, the inactive states.
27	Encoder	$\overline{\text{BIPOLAR ONE OUT}}$	An active low output designed to drive the one or positive sense of a bipolar line driver.
28	Encoder	SERIAL DATA IN	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
29	Encoder	ENCODER ENABLE	A high on this pin initiates the encode cycle. (Subject to the preceeding cycle being complete.)
30	Encoder	SYNC SELECT	Actuates a Command sync for an input high and Data sync for an input low.
31	Encoder	ENCODER PARITY SELECT	Sets transmit parity odd for a high input, even for a low input.
32	Encoder	SEND DATA	Is an active high output which enables the external source of serial data
33	Encoder	SEND CLOCK IN	Clock input at a frequency equal to the data rate X2.
34	Encoder	ENCODER SHIFT CLOCK	Output for shifting data into the Encoder. This shift clock shifts data on a low-to-high transition.
35	Blank	N.C.	Not connected.
36	Both	COUNT C_3	See pin 20.
37	Encoder	ENCODER CLOCK	Input to the 6:1 divider.
38	Decoder	DATA SYNC	Output of a high from this pin occurs during output of decoded data which was preceded by a Data synchronizing character.
39	Both	COUNT C_4	See pin 20.
40	Both	COUNT C_1	See pin 20.

Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the DECODER CLOCK. The frame length is set by programming the COUNT inputs. Parity is selected by programming ENCODER PARITY SELECT high for odd parity or low for even parity.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK ① . This cycle lasts for one word length or K + 4 ENCODER SHIFT CLOCK periods, where K is the number of bits to be sent. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high at SYNC SELECT input actuates a Command sync or a low will produce a Data sync for that word ② . When the Encoder is ready to accept data, the SEND DATA output will go high for K ENCODER SHIFT CLOCK periods ④ . During these K periods the data should be clocked into the SERIAL DATA input with every low-to-high transition of the ENCODER SHIFT CLOCK ③ - ④ . After the sync and Manchester II encoded data are transmitted through the BIPOLAR ONE and BIPOLAR ZERO outputs, the Encoder adds on an additional bit with is the parity for that word ⑤ . At any time a low on OUTPUT INHIBIT input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Any time after or during this pulse, a low-to-high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.



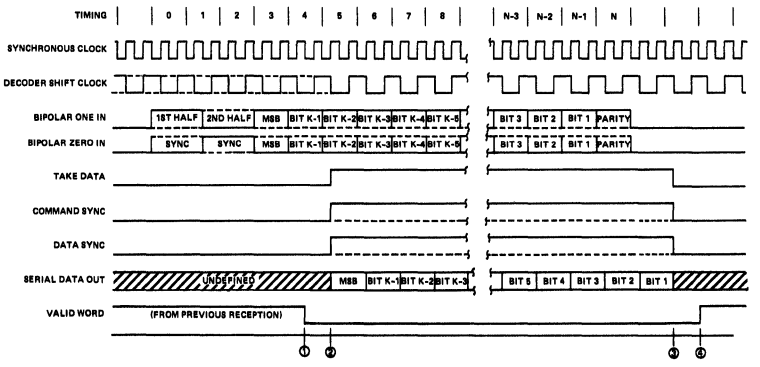
Decoder Operation

To operate the Decoder asynchronously requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. To operate the Decoder synchronously requires a SYNCHRONOUS CLOCK at a frequency 2 times the data rate which is synchronized with the data at every high-to-low transition applied to the SYNCHRONOUS DATA input. The Manchester II coded data can be presented to the Decoder asynchronously in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept noninverted Manchester II coded data. (e.g. from BIPOLAR ZERO OUT on an Encoder).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ① , the type of sync is indicated by a high level at either COMMAND SYNC or DATA SYNC output. If the sync character was a command sync the COMMAND SYNC output will go high ② and remain high for K SHIFT CLOCK periods ③ , where K is the number of bits to be received. If the sync character was a data sync the DATA SYNC output will go high and remain high ② - ③ while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can get shifted into an external register on every low-to-high transition of this clock ② - ③ .

After all K decoded bits have been transmitted ③ the data is checked for parity. A high input on DECODER PARITY SELECT will set the Decoder to check for even parity or a low input will set the Decoder to check for odd parity. A high on VALID WORD output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence.

At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.

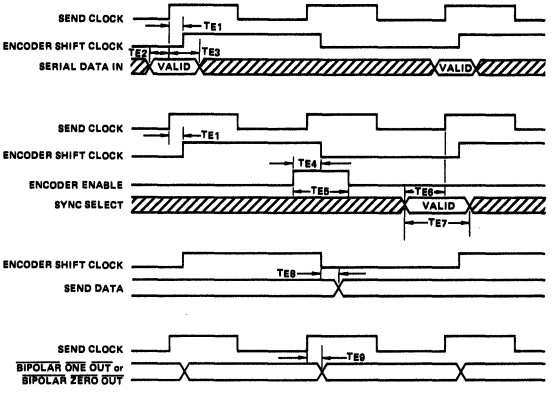


Frame Count

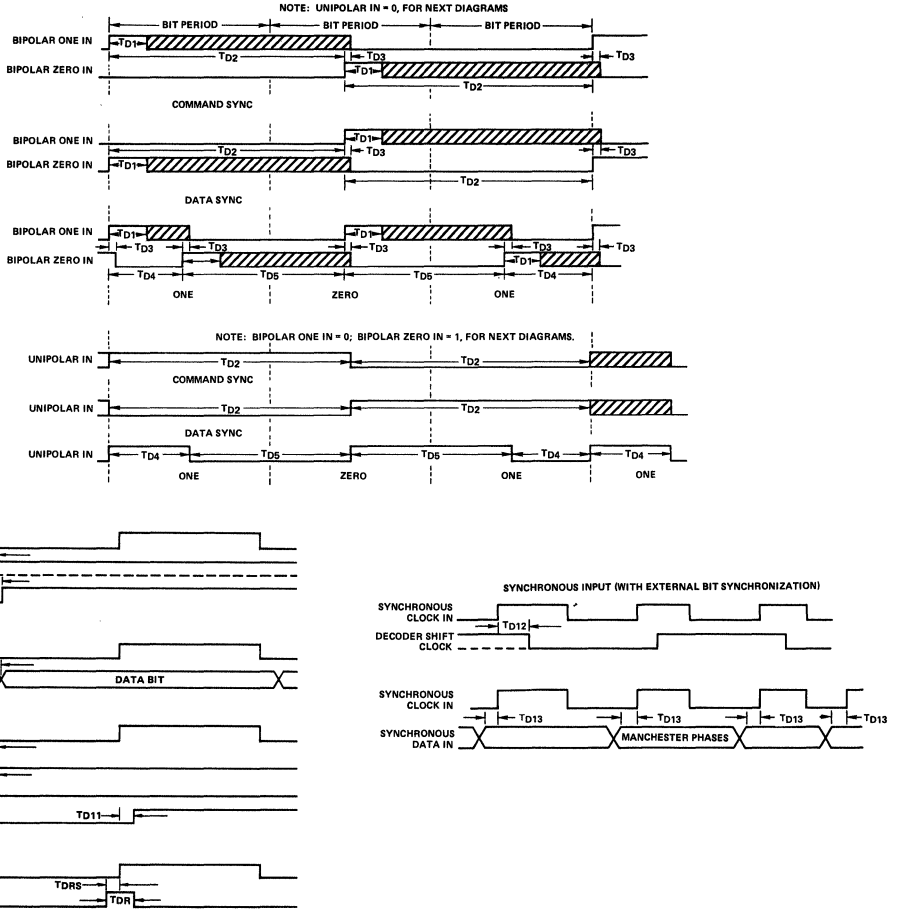
DATA BITS	FRAME LENGTH (BIT PERIODS)	PIN WORD				
		C_4	C_3	C_2	C_1	C_0
2	6	L	L	H	L	H
3	7	L	L	H	H	L
4	8	L	L	H	H	H
5	9	L	H	L	L	L
6	10	L	H	L	L	H
7	11	L	H	L	H	L
8	12	L	H	L	H	H
9	13	L	H	H	L	L
10	14	L	H	H	L	H
11	15	L	H	H	H	L
12	16	L	H	H	H	H
13	17	H	L	L	L	L
14	18	H	L	L	L	H
15	19	H	L	L	H	L
16	20	H	L	L	H	H
17	21	H	L	H	L	L
18	22	H	L	H	L	H
19	23	H	L	H	H	L
20	24	H	L	H	H	H
21	25	H	H	L	L	L
22	26	H	H	L	L	H
23	27	H	H	L	H	L
24	28	H	H	L	H	H
25	29	H	H	H	L	L
26	30	H	H	H	L	H
27	31	H	H	H	H	L
28	32	H	H	H	H	H

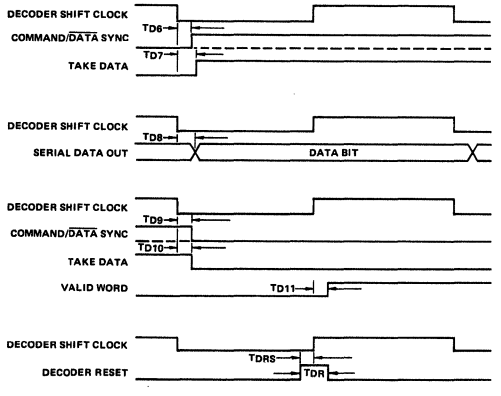
The above Table demonstrates all possible combinations of frame lengths ranging from 6 to 32 bits. The pin word described here is common to both the Encoder and Decoder.

Encoder Timing



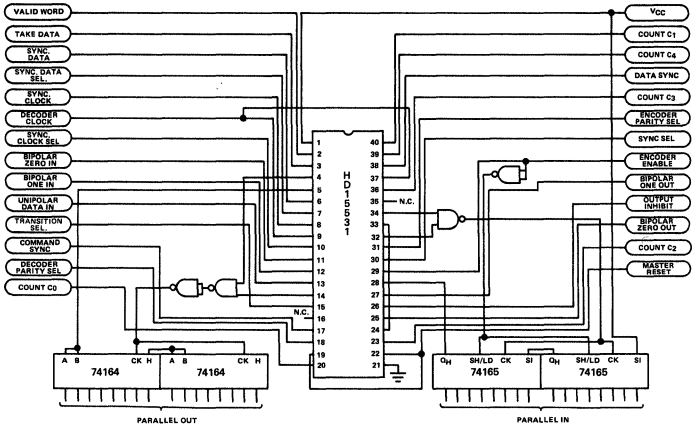
Decoder Timing





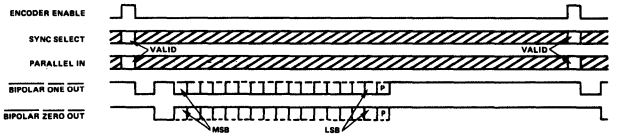
Applications

How to Make Our MTU Look Like a Manchester Encoded UART

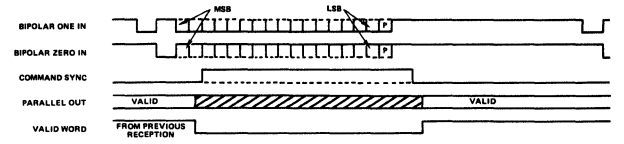


Typical Timing Diagrams for a Manchester Encoded UART

ENCODER TIMING



DECODER TIMING



HARRIS

HD-15531B

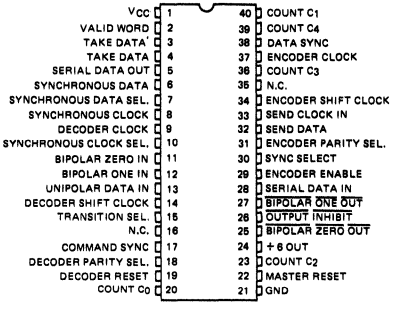
CMOS Programmable Manchester Encoder-Decoder

Preliminary

Features

- 2.5 MEGABIT/SEC DATA RATE
- SYNC IDENTIFICATION AND LOCK-IN
- CLOCK RECOVERY
- VARIABLE FRAME LENGTH TO 32 BITS
- MANCHESTER II ENCODE AND DECODE
- HALF OR FULL DUPLEX OPERATION
- FULL MILITARY OR INDUSTRIAL TEMPERATURE RANGES
- WORD TYPE SELECT AND RECOGNITION
- DETECTS ALL SINGLE, DOUBLE, OR TRIPLE SAMPLING ERRORS

Pinout



Description

The Harris HD-15531B Programmable Manchester Encoder-Decoder (MED) is intended to be used as a high speed, low power, serial data link controller in applications where data integrity combined with low overhead is important. It is manufactured using Harris' Self Aligned Junction Isolated (SAJI) CMOS process.

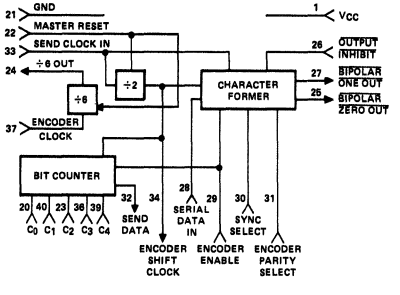
This LSI chip is divided into two sections, an encoder and a decoder. These sections operate independently of each other except for the Master Reset and frame length select function. In addition to encoding/decoding of NRZ data the HD-15531B frames variable length data (2-28 bits) with one of two types of synchronization characters and a parity bit. Independent selection of even or odd parity for the encoder and decoder is included.

An internal error detection algorithm will detect all single, double or triple sampling errors. In addition, this algorithm will typically detect better than 99% of four or more errors in any one word.

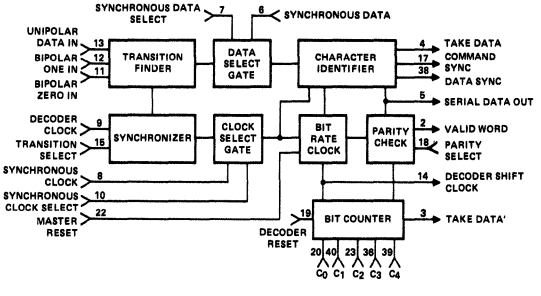
Ideal applications include party line Local Area Networks as well as data acquisition systems where 8, 12 or 16 bit A/D converters are typically used for the digital transmission of data.

Block Diagrams

ENCODER



DECODER



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow standard IC Handling Procedures.

ABSOLUTE MAXUMUM RATINGS

Supply Voltage	+7.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-15531B-9	-40°C to +85°C
Military HD-15531B-2/8	-55°C to +125°C

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±10% T_A = Industrial or Military

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
	V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
	V_{IHC}	Logical "1" Input Voltage (Clock)	V_{CC} -0.5			V	
	V_{ILC}	Logical "0" Input Voltage (Clock)			GND +0.5	V	
	I_{IL}	Input Leakage	-1.0		+1.0	μA	$0V \leqslant V_{IN} \leqslant V_{CC}$
	V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -3mA
	V_{OL}	Logical "0" Output Voltage			0.4	V	I_{OL} = 1.8mA
	I_{CCSB}	Supply Current Standby		0.5	2.0	mA	$V_{IN} = V_{CC} = 5.5V$ Outputs Open
	I_{CCOP}	Supply Current Operating*		16.0	20.0	mA	V_{CC} = 5.5V f = 30MHz
	C_{IN}	Input Capacitance*		5.0	7.0	pF	
	C_O	Output Capacitance*		8.0	10.0	pF	
	*Guaranteed and sampled but not 100% tested.						
	ENCODER TIMING						
A.C.	FEC	Encoder Clock Frequency	0		30	MHz	C_L = 50pF
	FESC	Send Clock Frequency	0		5	MHz	
	TECR	Encoder Clock Rise Time			8	ns	
	TECF	Encoder Clock Fall Time			8	ns	
	FED	Data Rate	0		2.5	MHz	
	TMR	Master Reset Pulse Width	150			ns	
	TE1	Shift Clock Delay			80	ns	
	TE2	Serial Data Setup	50			ns	
	TE3	Serial Data Hold	50			ns	
	TE4	Enable Setup	90			ns	
	TE5	Enable Pulse Width	100			ns	
	TE6	Sync Setup	55			ns	
	TE7	Sync Pulse Width	150			ns	
	TE8	Send Data Delay	0		50	ns	
	TE9	Bipolar Output Delay			130	ns	
	DECODER TIMING						
A.C.	FDC	Decoder Clock Frequency	0		30	MHz	C_L = 50pF
	FDS	Decoder Synchronous Clock	0		5	MHz	
	TDCR	Decoder Clock Rise Time			8	ns	
	TDCF	Decoder Clock Fall Time			8	ns	
	FDD	Data Rate	0		2.5	MHz	
	TDR	Decoder Reset Pulse Width	150			ns	
	TDRS	Decoder Reset Setup Time	75			ns	
	TMR	Master Reset Pulse Width	150			ns	
	TD1	Bipolar Data Pulse Width	T_{DC} +10			ns	①
	TD2	Sync Transition Span		18T_{DC}		ns	①
	TD3	One Zero Overlap			T_{DC} -10	ns	①
	TD4	Short Data Transition Span		6T_{DC}		ns	①
	TD5	Long Data Transition Span		12T_{DC}		ns	①
	TD6	Sync Delay (ON)	-20		110	ns	
	TD7	Take Data Delay (ON)	0		110	ns	
	TD8	Serial Data Out Delay			80	ns	
	TD9	Sync Delay (OFF)	0		110	ns	
	TD10	Take Data Delay (OFF)	0		110	ns	
	TD11	Valid Word Delay	0		110	ns	
	*TD12	Synchronous Clock To Shift Clock Delay			75	ns	
	TD13	Synchronous Data Setup	75			ns	

NOTE ①: T_{DC} = Decoder Clock Period = $\frac{1}{F_{DC}}$
These parameters are guaranteed but not 100% tested.

5 DATA COMMUNICATION

Pin Assignments

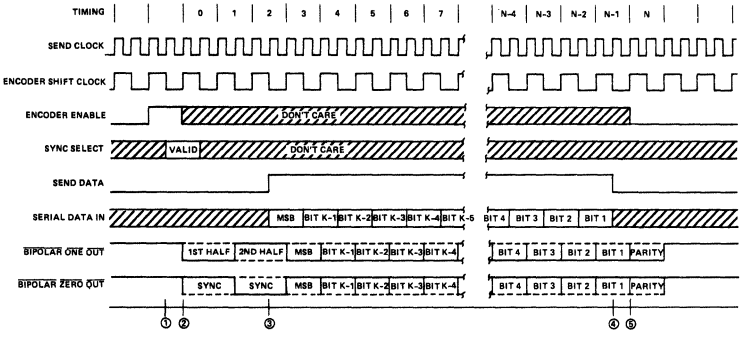
PIN	SECTION	NAME	DESCRIPTION
1	Both	VCC	Positive supply pin.
2	Decoder	VALID WORD	Output high indicates receipt of a valid word.
3	Decoder	TAKE DATA'	A continuous, free running signal provided for host timing or data handling. When data is present on the bus, this signal will be synchronized to the incoming data and will be identical to take data.
4	Decoder	TAKE DATA	Output is high during receipt of data after identification of a sync pulse
5	Decoder	SERIAL DATA OUT	Delivers received data in correct NRZ format.
6	Decoder	SYNCHRONOUS DATA	Input presents Manchester data directly to character identification logic. SYNCHRONOUS DATA SELECT must be held high to use this input. If not used this pin should be held high.
7	Decoder	SYNCHRONOUS DATA SELECT	In high state allows the synchronous data to enter the character identification logic.
8	Decoder	SYNCHRONOUS CLOCK	Input provides externally synchronized clock to the decoder. This input should be tied high when not in use.
9	Decoder	DECODER CLOCK	Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the decoder.
10	Decoder	SYNCHRONOUS CLOCK SELECT	In high state directs the SYNCHRONOUS CLOCK to control the decoder character identification logic. A low state selects the DECODER CLOCK
11	Decoder	BIPOLAR ZERO IN	A high input should be applied when the bus is in its negative state. This pin must be held high when the unipolar input is used.
12	Decoder	BIPOLAR ONE IN	A high input should be applied when the bus is in its positive state. This pin must be held low when the unipolar input is used.
13	Decoder	UNIPOLAR DATA IN	With pin 11 high and pin 12 low, this pin enters unipolar data into the transition finder circuit. If not used this input must be held low.
14	Decoder	DECODER SHIFT CLOCK	Output which delivers a frequency (DECODER CLOCK ÷ 12), synchronized by the recovered serial data stream.
15	Decoder	TRANSITION SELECT	A high input to this pin causes the transition finder to synchronize on every transition of input data. A low input causes the transition finder to synchronize only on mid-bit transitions.
16	Blank	N.C.	Not connected.
17	Decoder	COMMAND SYNC	Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character
18	Decoder	DECODER PARITY SELECT	An input for parity sense, calling for even parity with input high and odd parity with input low.
19	Decoder	DECODER RESET	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
20	Both	COUNT C_0	One of five binary inputs which establish the total bit count to be encoded or decoded.
21	Both	GROUND	Supply pin.
22	Both	MASTER RESET	A high on this pin clears 2:1 counters in both the encoder and decoder.
23	Both	COUNT C_2	See pin 20.
24	Encoder	÷ 6 OUT	Output from 6:1 divider which is driven by the ENCODER CLOCK.
25	Encoder	$\overline{\text{BIPOLAR ZERO OUT}}$	An active low output designed to drive the zero or negative sense of a bipolar line driver.
26	Encoder	$\overline{\text{OUTPUT INHIBIT}}$	A low on this pin forces pin 25 and 27 high, the inactive states.
27	Encoder	$\overline{\text{BIPOLAR ONE OUT}}$	An active low output designed to drive the one or positive sense of a bipolar line driver.
28	Encoder	SERIAL DATA IN	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
29	Encoder	ENCODER ENABLE	A high on this pin initiates the encode cycle. (Subject to the preceeding cycle being complete.)
30	Encoder	SYNC SELECT	Actuates a Command sync for an input high and Data sync for an input low.
31	Encoder	ENCODER PARITY SELECT	Sets transmit parity odd for a high input, even for a low input.
32	Encoder	SEND DATA	Is an active high output which enables the external source of serial data
33	Encoder	SEND CLOCK IN	Clock input at a frequency equal to the data rate X2.
34	Encoder	ENCODER SHIFT CLOCK	Output for shifting data into the Encoder. This shift clock shifts data on a low-to-high transition.
35	Blank	N.C.	Not connected.
36	Both	COUNT C_3	See pin 20.
37	Encoder	ENCODER CLOCK	Input to the 6:1 divider.
38	Decoder	DATA SYNC	Output of a high from this pin occurs during output of decoded data which was preceded by a Data synchronizing character.
39	Both	COUNT C_4	See pin 20.
40	Both	COUNT C_1	See pin 20.

Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the DECODER CLOCK. The frame length is set by programming the COUNT inputs. Parity is selected by programming ENCODER PARITY SELECT high for odd parity or low for even parity.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK ① . This cycle lasts for one word length or K + 4 ENCODER SHIFT CLOCK periods, where K is the number of bits to be sent. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high at SYNC SELECT input actuates a Command sync or a low will produce a Data sync for that word ② . When the Encoder is ready to accept data, the SEND DATA output will go high for K ENCODER SHIFT CLOCK periods ④ . During these K periods the data should be clocked into the SERIAL DATA input with every low-to-high transition of the ENCODER SHIFT CLOCK ③ - ④ . After the sync and Manchester II encoded data are transmitted through the $\overline{\text{BIPOLAR ONE}}$ and $\overline{\text{BIPOLAR ZERO}}$ outputs, the Encoder adds on an additional bit with is the parity for that word ⑤ . At any time a low on $\overline{\text{OUTPUT INHIBIT}}$ input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Any time after or during this pulse, a low-to-high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.



Decoder Operation

To operate the Decoder asynchronously requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. To operate the Decoder synchronously requires a SYNCHRONOUS CLOCK at a frequency 2 times the data rate which is synchronized with the data at every high-to-low transition applied to the SYNCHRONOUS DATA input. The Manchester II coded data can be presented to the Decoder asynchronously in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept noninverted Manchester II coded data. (e.g. from $\overline{\text{BIPOLAR ZERO OUT}}$ on an Encoder).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ① , the type of sync is indicated by a high level at either COMMAND SYNC or DATA SYNC output. If the sync character was a command sync the COMMAND SYNC output will go high ② and remain high for K SHIFT CLOCK periods ③ , where K is the number of bits to be received. If the sync character was a data sync the DATA SYNC output will go high. The TAKE DATA output will go high and remain high ② - ③ while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can get shifted into an external register on every low-to-high transition of this clock ② - ③ .

After all K decoded bits have been transmitted ③ the data is checked for parity. A high input on DECODER PARITY SELECT will set the Decoder to check for even parity or a low input will set the Decoder to check for odd parity. A high on VALID WORD output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence.

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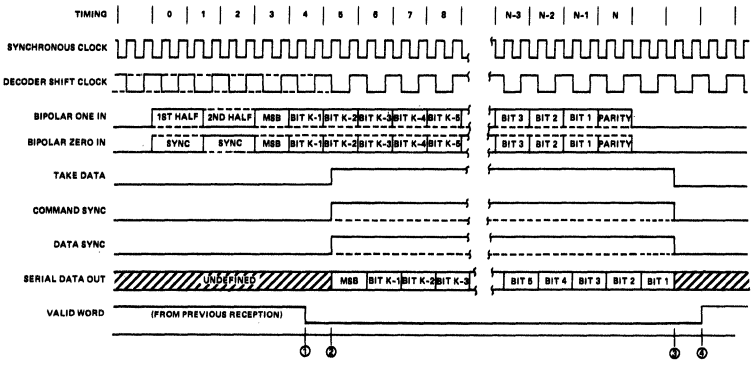

Frame Count

DATA BITS	FRAME LENGTH (BIT PERIODS)	PIN WORD				
		C4	C3	C2	C1	C0
2	6	L	L	H	L	H
3	7	L	L	H	H	L
4	8	L	L	H	H	H
5	9	L	H	L	L	L
6	10	L	H	L	L	H
7	11	L	H	L	H	L
8	12	L	H	L	H	H
9	13	L	H	H	L	L
10	14	L	H	H	L	H
11	15	L	H	H	H	L
12	16	L	H	H	H	H
13	17	H	L	L	L	L
14	18	H	L	L	L	H
15	19	H	L	L	H	L
16	20	H	L	L	H	H
17	21	H	L	H	L	L
18	22	H	L	H	L	H
19	23	H	L	H	H	L
20	24	H	L	H	H	H
21	25	H	H	L	L	L
22	26	H	H	L	L	H
23	27	H	H	L	H	L
24	28	H	H	L	H	H
25	29	H	H	H	L	L
26	30	H	H	H	L	H
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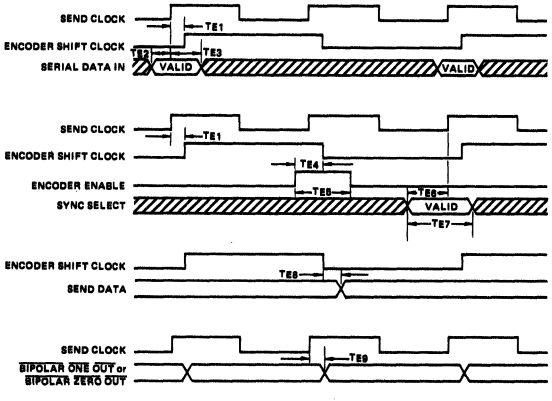
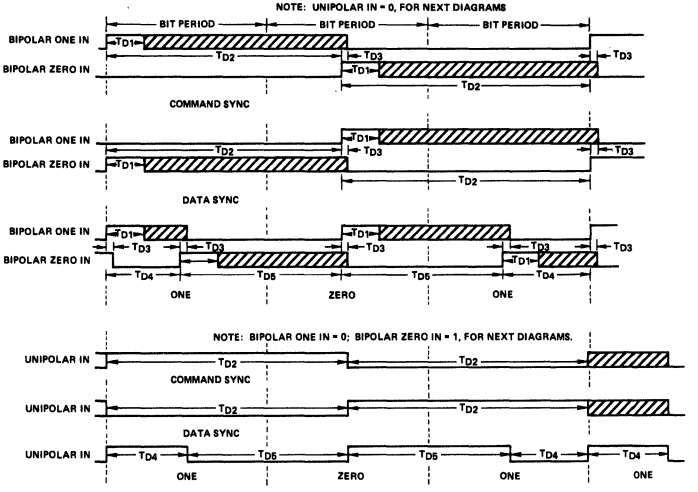
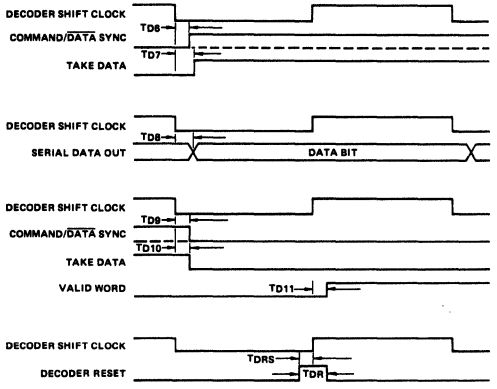
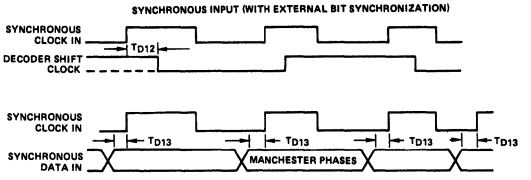


Decoder Timing

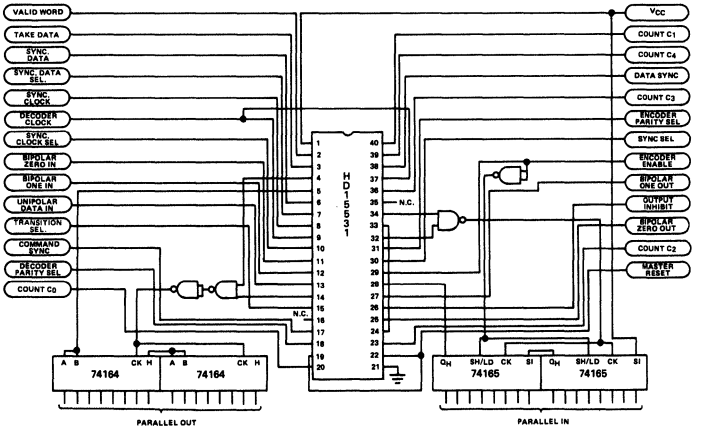






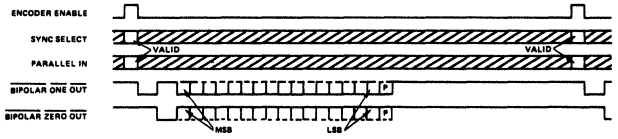
Applications

How to Make Our MTU Look Like a Manchester Encoded UART

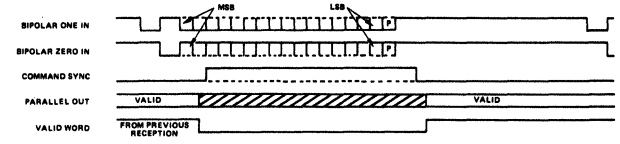


Typical Timing Diagrams for a Manchester Encoded UART

ENCODER TIMING



DECODER TIMING



The following is a partial listing of technical articles that have been published which discuss Harris Semiconductors line of Manchester Encoder-Decoders.

- "Manchester Terminal Unit in CMOS LSI", Military Electronics, April 1979
- "Manchester II Transfers Data with Integrity, Speed" Electronic Design, March 19, 1981
- "Encoding Schemes in Serial Data Communiations", Electronic Engineering, July 1981
- "Pulse Codes in Serial Data Communications", Computer Design, January 1982
- "Improve Datacomm Links by Using Manchester Code", Electric Design News, February17, 1982
- "For Data-Comm Links, Manchester Chip Could be the Best", Electronic Design, August 5, 1982

Additional literature is available from Harris in the form of Technical Briefs (TB-15, 20, 28, 29, 43) and Article Reprints of published articles.

HD-6408

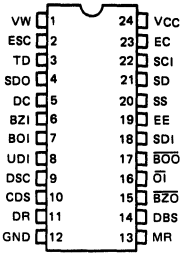
CMOS Asynchronous Serial Manchester Adapter (ASMA)

Features

- LOW BIT ERROR RATE
- ONE MEGABIT/SEC DATA RATE
- SYNC IDENTIFICATION AND LOCK-IN
- CLOCK RECOVERY
- MANCHESTER II ENCODE, DECODE
- SEPARATE ENCODE AND DECODE
- LOW OPERATING POWER: 50mW AT 5 VOLTS
- SINGLE POWER SUPPLY
- 24 PIN PACKAGE

Pinout

TOP VIEW



Description

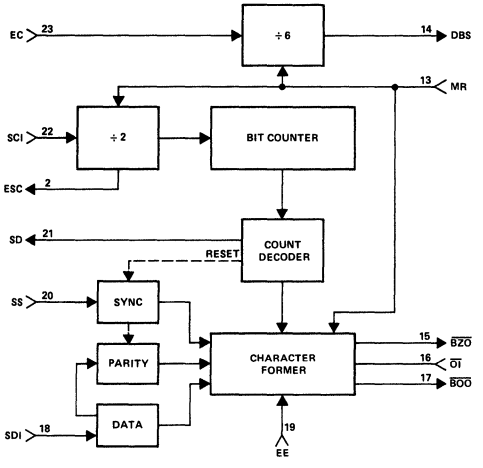
The HD-6408 is a CMOS/LSI Manchester Encoder/Decoder for creating a very high speed asynchronous serial data bus. The Encoder converts serial NRZ data (typically from a shift register) to Manchester II encoded data adding a sync pulse and parity bit. The Decoder recognizes this sync pulse and identifies it as a Command Sync or a Data Sync. The data is then decoded and shifted out in the NRZ code (typically into a shift register). Finally, the parity bit is checked. If there were no Manchester or parity errors the Decoder responds with a valid word signal. This Decoder puts the Manchester code to full use to provide clock recovery and excellent noise immunity at these very high speeds.

The HD-6408 can be used in many commercial applications such as, security systems, environmental control systems, serial data links and many others. It utilizes a single 12X clock and achieves data rates of up to one million bits per second with a very minimum overhead of only 4 bits out of 20, leaving 16 bits for data.

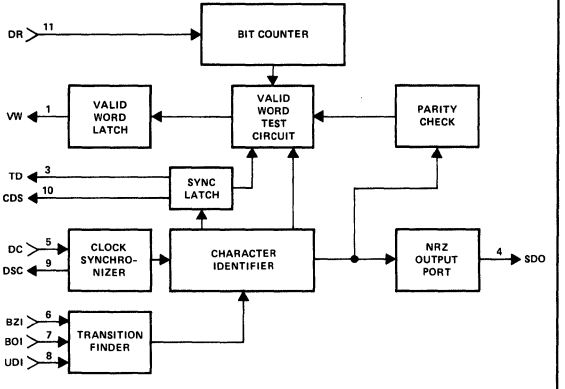
5 DATA COMMUNICATION

Block Diagrams

ENCODER



DECODER



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±10% T_A = -40°C to +85°C

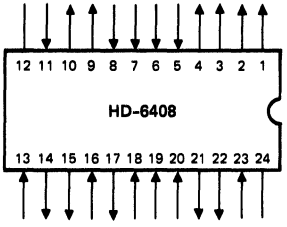
	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
	V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
	V_{IHC}	Logical "1" Input Voltage (Clock)	V_{CC} -0.5			V	
	V_{ILC}	Logical "0" Input Voltage (Clock)			GND +0.5	V	
	I_{IL}	Input Leakage	-1.0		+1.0	µA	$0V \leqslant V_{IN} \leqslant V_{CC}$
	V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -3mA
	V_{OL}	Logical "0" Output Voltage			0.4	V	I_{OL} = 1.8mA
	I_{CCSB}	Supply Current Standby		0.5	2	mA	$V_{IN} = V_{CC}$ = 5.5V Outputs Open
	I_{CCOP}	Supply Current Operating*		8.0	10.0	mA	V_{CC} = 5.5V, f = 1MHz
	C_{IN}	Input Capacitance*		5.0	7.0	pF	
	C_O	Output Capacitance*		8.0	10.0	pF	
		*Guaranteed and sampled but not 100% tested.					
ENCODER TIMING V_{CC} = 5.0V ±5% T_A = -40°C to +85°C							
A.C.	F_{EC}	Encoder Clock Frequency	0		12	MHz	C_L = 50pF
	F_{ESC}	Send Clock Frequency	0		2.0	MHz	
	T_{ECR}	Encoder Clock Rise Time			8	ns	
	T_{ECF}	Encoder Clock Fall Time			8	ns	
	F_{ED}	Data Rate	0		1.0	MHz	
	T_{MR}	Master Reset Pulse Width	150			ns	
	T_{E1}	Shift Clock Delay			125	ns	
	T_{E2}	Serial Data Setup	75			ns	
	T_{E3}	Serial Data Hold	75			ns	
	T_{E4}	Enable Setup	90			ns	
	T_{E5}	Enable Pulse Width	100			ns	
	T_{E6}	Sync Setup	55			ns	
	T_{E7}	Sync Pulse Width	150			ns	
	T_{E8}	Send Data Delay	0		50	ns	
	T_{E9}	Bipolar Output Delay			130	ns	
DECODER TIMING V_{CC} = 5.0V ±5% T_A = -40°C to +85°C							
A.C.	F_{DC}	Decoder Clock Frequency	0		12	MHz	C_L = 50pF
	T_{DCR}	Decoder Clock Rise Time			8	ns	
	T_{DCF}	Decoder Clock Fall Time			8	ns	
	F_{DD}	Data Rate	0		1.0	MHz	
	T_{DR}	Decoder Reset Pulse Width	150			ns	
	T_{DRS}	Decoder Reset Setup Time	75			ns	
	T_{MR}	Master Reset Pulse Width	150			ns	
	T_{D1}	Bipolar Data Pulse Width	T_{DC} +10			ns	①
	T_{D2}	Sync Transition Span		18T_{DC}		ns	①
	T_{D3}	One Zero Overlap			T_{DC} -10	ns	①
	T_{D4}	Short Data Transition Span		6T_{DC}		ns	①
	T_{D5}	Long Data Transition Span		12T_{DC}		ns	①
	T_{D6}	Sync Delay (ON)	-20		110	ns	
	T_{D7}	Take Data Delay (ON)	0		110	ns	
	T_{D8}	Serial Data Out Delay			80	ns	
	T_{D9}	Sync Delay (OFF)	0		110	ns	
	T_{D10}	Take Data Delay (OFF)	0		110	ns	
	T_{D11}	Valid Word Delay	0		110	ns	

NOTE ①: T_{DC} = Decoder Clock Period = $\frac{1}{F_{DC}}$

These parameters are guaranteed but not 100% tested.

Pin Assignment and Functions

PIN	SYMBOL	SECTION	DESCRIPTION
1	VW	Decoder	Output high indicates receipt of a VALID WORD.
2	ESC	Encoder	ENCODER SHIFT CLOCK is an output for shifting data into the Encoder. This clock shifts data on a low-to-high transition.
3	TD	Decoder	TAKE DATA output is high during receipt of data after identification of a sync pulse.
4	SDO	Decoder	SERIAL DATA OUT delivers received data in correct NRZ format.
5	DC	Decoder	DECODER CLOCK input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the Decoder.
6	BZI	Decoder	A high input should be applied to BIPOLAR ZERO IN when the bus is in its negative state. This pin must be held high when the Unipolar input is used.
7	BOI	Decoder	A high input should be applied to BIPOLAR ONE IN when the bus is in its positive state, this pin must be held low when the Unipolar input is used.
8	UDI	Decoder	With pin 6 high and pin 7 low, this pin enters UNIPOLAR DATA IN to the transition finder circuit. If not used this input must be held low.
9	DSC	Decoder	DECODER SHIFT CLOCK output delivers a frequency (DECODER CLOCK ÷ 12), synchronized by the recovered serial data stream.
10	CDS	Decoder	COMMAND/DATA SYNC output high occurs during output of decoded data which was preceded by a Command synchronizing character. A low output indicates a Data synchronizing character.
11	DR	Decoder	A high input to DECODER RESET during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
12	GND	Both	GROUND supply pin.



PIN	SYMBOL	SECTION	DESCRIPTION
13	MR	Both	A high on MASTER RESET clears the 2:1 counters in both the encoder and decoder and the ÷ 12 counter.
14	DBS	Encoder	DIVIDE BY SIX is an output from 6:1 divider which is driven by the ENCODER CLOCK.
15	$\overline{\text{BZO}}$	Encoder	$\overline{\text{BIPOLAR ZERO OUT}}$ is an active low output designed to drive the zero or negative sense of a bipolar line driver.
16	$\overline{\text{OI}}$	Encoder	A low on $\overline{\text{OUTPUT INHIBIT}}$ forces pin 15 and 17 high, their inactive states.
17	$\overline{\text{BOO}}$	Encoder	$\overline{\text{BIPOLAR ONE OUT}}$ is an active low output designed to drive the one or positive sense of a bipolar line driver.
18	SDI	Encoder	SERIAL DATA IN accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
19	EE	Encoder	A high on ENCODER ENABLE initiates the encode cycle. (Subject to the preceding cycle being completé.)
20	SS	Encoder	SYNC SELECT actuates a Command sync for an input high and Data sync for an input low.
21	SD	Encoder	SEND DATA is an active high output which enables the external source of serial data.
22	SCI	Encoder	SEND CLOCK IN is 2X the Encoder data rate.
23	EC	Encoder	ENCODER CLOCK is the input to the 6:1 divider.
24	VCC	Both	Positive supply pin.

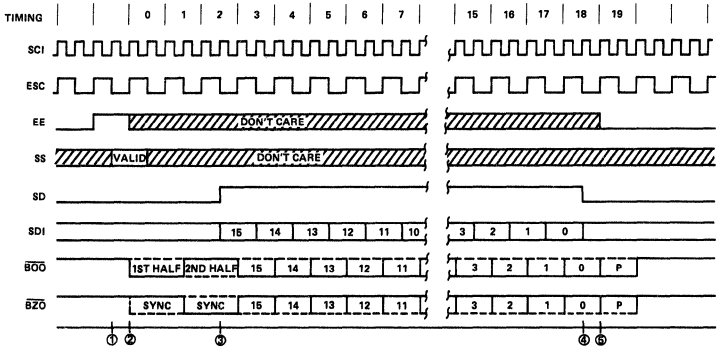
Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SClock input. An auxiliary divide by six counter is provided on chip which can be utilized to produce the SClock by dividing the DClock.

The Encoder's cycle begins when EE is high during a falling edge of ESC ①. This cycle lasts for one word length or twenty ESC periods. At the next low-to-high transition of the ESC, a high at SS input actuates a Command sync or a low will produce a Data sync for that word ②. When the Encoder is ready to accept data, the SD output will go high and remain high for sixteen ESC periods ③ – ④.

During these sixteen periods the data should be clocked into the SDInput with every high-to-low transition of the ESC ③ – ④. After the sync and Manchester II encoded data are transmitted through the $\overline{BOO}$ and $\overline{BZO}$ outputs, the Encoder adds on an additional bit which is the (odd) parity for that word ⑤. At any time a low on $\overline{OI}$ will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MR. Any time after or during this pulse, a low-to-high transition on SCI clears the internal counters an initializes the Encoder for a new word.



Decoder Operation

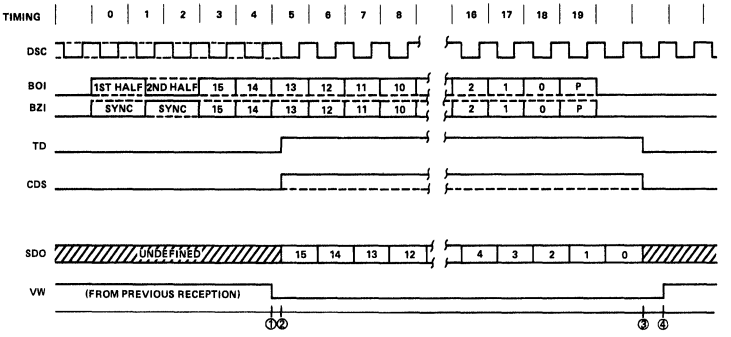
The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DClock input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BOI and BZI inputs will accept data from a differential output comparator. The UDI input can only accept noninverted Manchester II coded data (e.g. from $\overline{BZO}$ of an Encoder).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ①, the type of sync is indicated by the CDS output. If the sync character was a command, this output will go high ② and remain high for sixteen DSC periods ③, otherwise it will remain low. The TD output will go high and remain high ② – ③ while the Decoder is transmitting the decoded data through SDO.

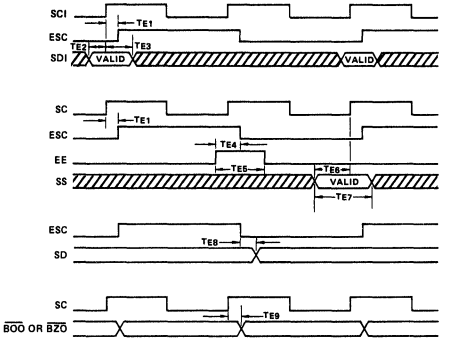
The decoded data available at SDO is in a NRZ format. The DSC is provided so that the decoded bits can get shifted into an external register on every low-to-high transition for this clock ② – ③.

After all sixteen decoded bits have been transmitted ③ the data is checked for odd parity. A high on VW output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence.

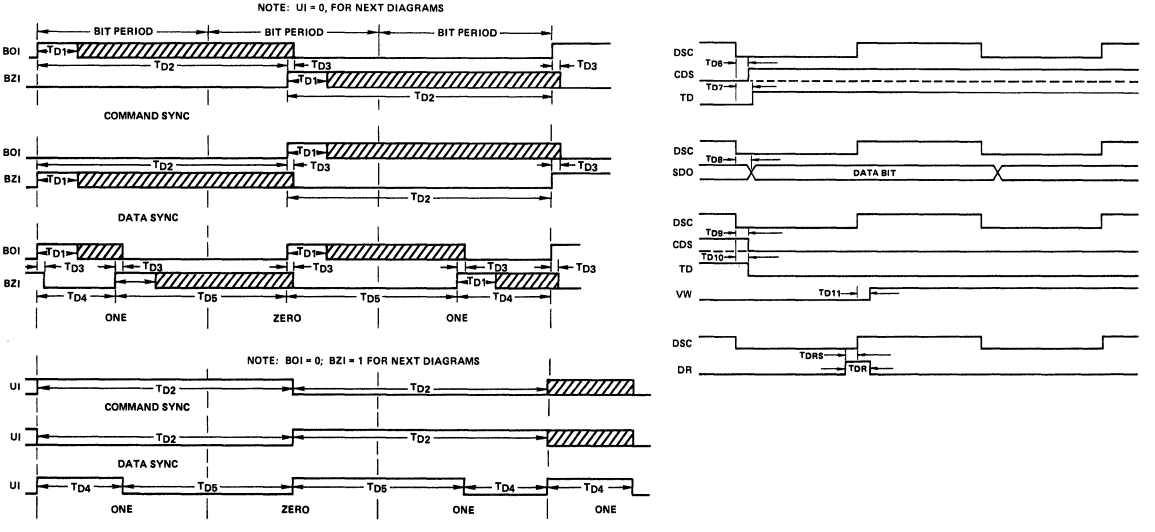
At any time in the above sequence a high input on DR during a low-to-high transition of DSC will abort transmission and initialize the Decoder to start looking for a new sync character.



Encoder Timing



Decoder Timing



HARRIS

HD-6409

CMOS Manchester Encoder-Decoder (MED)

Features

- CONVERTER OR REPEATER MODE
- INDEPENDENT MANCHESTER ENCODER AND DECODER OPERATION
- STATIC TO ONE MEGABIT/SEC DATA RATE GUARANTEED
- LOW BIT ERROR RATE
- DIGITAL PLL CLOCK RECOVERY
- ON CHIP OSCILLATOR
- SINGLE POWER SUPPLY
- LOW OPERATING POWER: 50mW AT 5 VOLTS
- INDUSTRIAL OR MILITARY TEMPERATURE RANGE
- 20 PIN PACKAGE

Description

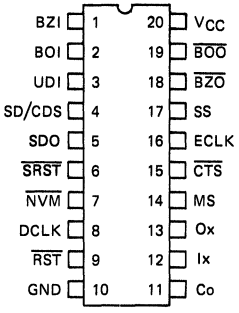
The HD-6409 Manchester Encoder-Decoder (MED) is a high speed, low power device manufactured using self-aligned silicon gate technology. The device is intended for use in serial data communication, and can be operated in either of two modes. In the converter mode, the MED converts Nonreturn-to-Zero code (NRZ) into Manchester code and decodes Manchester code into Nonreturn-to-Zero code. For serial data communication, Manchester code does not have some of the deficiencies inherent in Nonreturn-to-Zero code. For instance, use of the MED on a serial line eliminates DC components, provides clock recovery, and gives a relatively high degree of noise immunity. Because the MED converts the most commonly used code (NRZ) to Manchester code, the advantages of using Manchester code are easily realized in a serial data link.

In the Repeater mode, the MED accepts Manchester code input and reconstructs it with a recovered clock. This minimizes the effects of noise on a serial data link. A digital phase lock loop generates the recovered clock. A maximum data rate of 1MHz requires only 50mW of power.

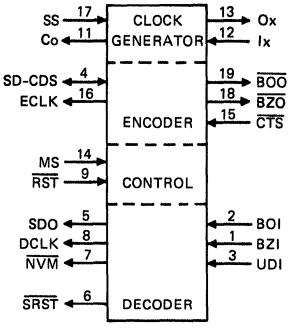
Manchester code is used in magnetic tape recording and in fiber optic communication, and generally is used where data accuracy is imperative. Because it frames blocks of data, the HD-6409 easily interfaces to protocol controllers.

Pinout

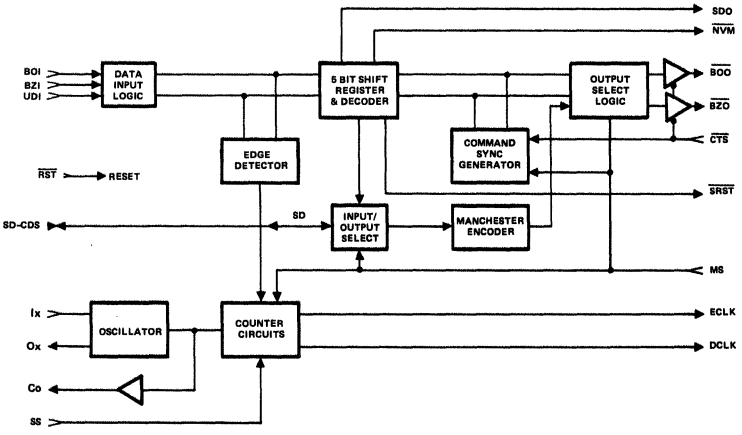
TOP VIEW



Logic Symbol



Functional Diagram



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

Pin Assignment And Functions

PIN	MNEMONIC NAME		DESCRIPTION
1 (I)	BZI	Bipolar Zero Input	Used in conjunction with pin 2, Bipolar One Input (BOI), to input Manchester II encoded data to the decoder. BZI and BOI are logical complements. When using pin 3, Unipolar Data Input (UDI) for data input, BZI must be held high.
2 (I)	BOI	Bipolar One Input	Used in conjunction with pin 1, Bipolar Zero Input (BZI), to input Manchester II encoded data to the decoder. BOI and BZI are logical complements. When using pin 3, Unipolar Data Input (UDI) for data input, BOI must be held low.
3 (I)	UDI	Unipolar Data Input	An alternate to bipolar input (BZI, BOI), Unipolar Data Input (UDI) is used to input Manchester II encoded data to the decoder. When using pin 1 (BZI) and pin 2 (BOI) for data input, UDI must be held low.
4 (I/O)	SD/CDS	Serial Data/Command Data Sync	In the converter mode, SD/CDS is an input used to receive serial NRZ data. NRZ data is accepted synchronously on the falling edge of encoder clock output (ECLK). In the repeater mode, SD/CDS is an output indicating the status of last valid sync pattern received. A high indicates a command sync and a low indicates a data sync pattern.
5 (O)	SDO	Serial Data Out	The decoded serial NRZ data is transmitted out synchronously with the decoder clock (DCLK). SDO is forced low when $\overline{RST}$ is low.
6 (O)	$\overline{SRST}$	$\overline{Serial\ Reset}$	In the converter mode, $\overline{SRST}$ follows $\overline{RST}$. In the repeater mode, when $\overline{RST}$ goes low, $\overline{SRST}$ goes low and remains low after $\overline{RST}$ goes high. $\overline{SRST}$ goes high only when RST is high, the reset bit is zero, and a valid synchronization sequence is received.
7 (O)	$\overline{NVM}$	$\overline{Nonvalid\ Manchester}$	A low on $\overline{NVM}$ indicates that the decoder has received invalid Manchester data and present data on Serial Data Out (SDO) is invalid. A high indicates that the sync pulse and data were valid and SDO is valid. $\overline{NVM}$ is set low by a low on $\overline{RST}$, and remains low after $\overline{RST}$ goes high until valid sync pulse followed by two valid Manchester bits is received.
8 (O)	DCLK	Decoder Clock	The decoder clock is a 1X clock recovered from BZI and BOI to synchronously output received NRZ data (SDO).
9 (I)	$\overline{RST}$	$\overline{Reset}$	In the converter mode, a low on $\overline{RST}$ forces SDO, DCLK, $\overline{NVM}$, and $\overline{SRST}$ low. A high on $\overline{RST}$ enables SDO and DCLK, and forces $\overline{SRST}$ high. $\overline{NVM}$ remains low after $\overline{RST}$ goes high until a valid sync pulse followed by two Manchester bits is received, after which it goes high. In the repeater mode, $\overline{RST}$ has the same effect on SDO, DCLK and $\overline{NVM}$ as in the converter mode. When $\overline{RST}$ goes low, $\overline{SRST}$ goes low and remains low after $\overline{RST}$ goes high. $\overline{SRST}$ goes high only when $\overline{RST}$ is high, the reset bit is zero and a valid synchronization sequence is received.

(I) - Input

(O) - Output

Pin Assignment And Functions (Continued)

PIN	MNEMONIC NAME		DESCRIPTION
10 (I)	GND	Ground	Ground
11 (O)	Co	Clock Output	Buffered output of clock input Ix. May be used as clock signal for other peripherals.
12 (I)	Ix	Clock Input	Ix is the input for an external clock or, if the internal oscillator is used, Ix and Ox are used for the connection of the crystal.
13 (I)	Ox	Clock Drive	If the internal oscillator is used, Ox and Ix are used for the connection of the crystal.
14 (I)	MS	Mode Select	MS must be held low for operation in the converter mode, and high for operation in the repeater mode.
15 (I)	$\overline{CTS}$	Clear to Send	In the converter mode, a high disables the encoder, forcing outputs $\overline{BOO}$, $\overline{BZO}$ high and ECLK low. A high to low transition of $\overline{CTS}$ initiates transmission of a Command sync pulse. A low on $\overline{CTS}$ enables $\overline{BOO}$, $\overline{BZO}$, and ECLK. In the repeater mode, the function of $\overline{CTS}$ is identical to that of the converter mode with the exception that a transition of $\overline{CTS}$ does not initiate a synchronization sequence.
16 (O)	ECLK	Encoder Clock	In the converter mode, ECLK is a 1X clock output used to receive serial NRZ data to SD/CDS. In the repeater mode, ECLK is a 2X clock which is recovered from BZI and BOI data by the digital phase locked loop.
17 (I)	SS	Speed Select	A logic high on SS sets the data rate at 1/32 times the clock frequency while a low sets the data rate at 1/16 times the clock frequency.
18 (O)	$\overline{BZO}$	$\overline{\text{Bipolar Zero Output}}$	$\overline{BZO}$ and its logical complement $\overline{BOO}$ are the Manchester data outputs of the encoder. The inactive state for these outputs is in the high state.
19 (0)	$\overline{BOO}$	$\overline{\text{Bipolar One Out}}$	see pin 18
20 (I)	V_{CC}	V_{CC}	Positive Power Supply

(I) - Input
(O) - Output

ABSOLUTE MAXIMUM RATINGS *	
Supply Voltage	+7.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE		
Operating Temperature Range		
Industrial	HD-6409-9	-40°C to +85°C
Military	HD-6409-2/8	-55°C to +125°C
Operating Voltage Range		
Industrial	HD-6409-9	4.5V to 5.5V
Military	HD-6409-2/8	4.5V to 5.5V

* *CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	MIN	TYPICAL	MAX	UNITS	TEST CONDITIONS
DC	VIH	Logic-1 Input Voltage	70% VCC	–		V	
	VIL	Logic-0 Input Voltage			20% VCC	V	
	VIHR	Logic-1 Input Voltage ($\overline{\text{Reset}}$)	VCC -0.5			V	
	VILR	Logic-0 Input Voltage ($\overline{\text{Reset}}$)			GND +0.5	V	
	VIHC	Logic-1 Input Voltage (Clock)	VCC -0.5			V	
	VILC	Logic-0 Input Voltage (Clock)			GND +0.5	V	
	IIL	Input Leakage	-1.0		+1.0	μA	$0V \leqslant V_{IN} \leqslant V_{CC}$
	VOH	Logic-1 Output Voltage	VCC -0.4			V	I_{OH} = -2.0mA
	VOL	Logic-0 Output Voltage			0.4	V	I_{OL} = 2.0mA
	ICCQ	Supply Current Quiescent		1.0	100	μA	$V_{IN} = V_{CC} = 5.5V$,
	ICCOP	Supply Current Operating*		7.0	12.0	mA	$V_{CC} = 5.5V$, f_{co} = 16MHz
	CIN	Input Capacitance*		6.0	8.0	pF	
	COUT	Output Capacitance*		8.0	15.0	pF	
AC	fc	Clock Frequency		16		MHz	I_X or X_{tal}
	tc	Clock Period		1/fc		s	
	t1	Bipolar Pulse Width	tc -10			ns	
	t2	Sync Transition Span		1.5 x CR x tc ①②		ns	
	t3	One-Zero Overlap			tc -10	ns	
	t4	Short Data Transition Span		0.5 x CR x tc ①②		ns	
	t5	Long Data Transition Span		CR x tc		ns	
	t6	Output Rise & Fall Time			50	ns	CL = 20pF for Co,
		Clock Out Co Rise & Fall Time			1/(5 x fc)	s	50pF Otherwise
	t7	Input Rise & Fall Time			1/(5 x fc)	s	50ns Max.
	t8	Clock High Duty Cycle	20			ns	TCYCLE = 62ns Fig. 5
	t9	Clock Low Duty Cycle	20			ns	TCYCLE = 62ns Fig. 5

CONVERTER MODE

	SYMBOL	PARAMETER	MIN	TYPICAL	MAX	UNITS	TEST CONDITIONS
	ENCODER SECTION						
AC	tCE1	SD Setup Time	70			ns	
	tCE2	SD Hold Time	0			ns	
	tCE3	SD to $\overline{\text{BZO}}$, $\overline{\text{BOO}}$ Prop Delay		1	1.5	DBP	
	tCE4	$\overline{\text{CTS}}$ Low to $\overline{\text{BZO}}$, $\overline{\text{BOO}}$ Enabled		1	1.5	DBP	
	tCE5	$\overline{\text{CTS}}$ Low to ECLK Enabled		10.5		DBP	
	tCE6	$\overline{\text{CTS}}$ High to ECLK Disabled		1.0	1.5	DBP	
	tCE7	$\overline{\text{CTS}}$ High to $\overline{\text{BZO}}$, $\overline{\text{BOO}}$ Disabled		2.0	2.5	DBP	
	DECODER SECTION						
	tCD1	UDI to SDO, $\overline{\text{NVM}}$	2.5		3	DBP ③	
	tCD2	DCLK to SDO, $\overline{\text{NVM}}$			40	ns	
	tCD3	$\overline{\text{RST}}$ Low to DCLK, SDO, $\overline{\text{NVM}}$ Low		0.5	1.5	DBP ③	CL = 50pF
	tCD4	$\overline{\text{RST}}$ High to DCLK Enabled		0.5	1.5	DBP ③	CL = 50pF

REPEATER MODE

	SYMBOL	PARAMETER	MIN	TYPICAL	MAX	UNITS	TEST CONDITIONS
AC	tR1	UDI to $\overline{\text{BOO}}$, $\overline{\text{BZO}}$		1		DBP ③	
	tR2	ECLK to $\overline{\text{BZO}}$			40	ns	
	tR3	UDI to SDO, $\overline{\text{NVM}}$	2.5		3	DBP ③	

NOTES: ① CR – Clock Rate, either 16X or 32X
② $t_c = 1/f_c$
③ DBP – Data Bit Period, CR = 16X, one DBP = 16 Clock cycles; CR = 32X, one DBP = 32 clock cycles
* Guaranteed and sampled but not 100% tested.

ENCODER OPERATION

The encoder uses free running clocks at 1X and 2X the data rate derived from the system clock 1_X for internal timing. $\overline{CTS}$ is used to control the encoder outputs, ECLK, $\overline{BOO}$ and $\overline{BZO}$. A free running 1X ECLK is transmitted out of the encoder to drive the external circuits which supply the NRZ data to the MED at pin SD/CDS.

A low on $\overline{CTS}$ enables encoder outputs ECLK, $\overline{BOO}$ and $\overline{BZO}$, while a high on $\overline{CTS}$ forces $\overline{BZO}$, $\overline{BOO}$ high and holds ECLK low. When $\overline{CTS}$ goes from high to low ①, a synchronization sequence is transmitted out on $\overline{BOO}$ and $\overline{BZO}$. A synchronization sequence consists of eight Manchester "0" bits followed by a command sync pulse. ② A command sync pulse is a three bit wide pulse with the first 1½ bits high followed by 1½ bits low. ③ Serial NRZ data is clocked into the encoder at SD/CDS on the high to low transition of ECLK during the command sync pulse. The NRZ data received is encoded into Manchester II data and transmitted out on $\overline{BOO}$ and $\overline{BZO}$ following the command sync pulse. ④ Following the synchronization sequence, input data is encoded and transmitted out continuously without parity check or word framing. The length of the data block encoded is defined by $\overline{CTS}$. Manchester data out is inverted.

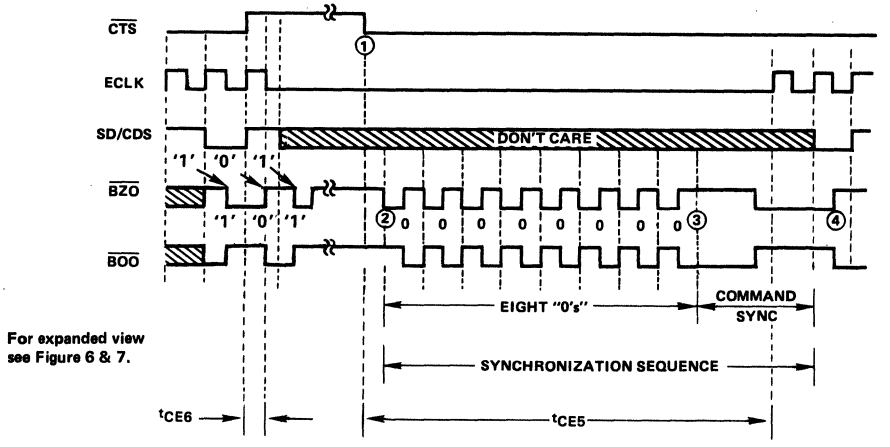


FIGURE 1

DECODER OPERATION

The decoder requires a single clock with a frequency 16X or 32X the desired data rate. The rate is selected on the speed select with SS low producing a 16X clock and high a 32X clock. For long data links the 32X mode should be used as this permits a wider timing jitter margin. The internal operation of the decoder utilizes a free running clock synchronized with incoming data for its clocking.

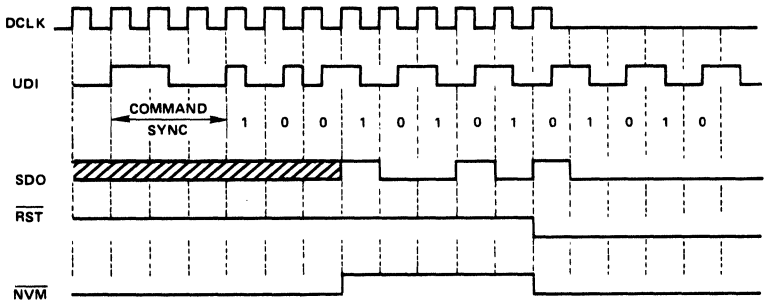
The Manchester II encoded data can be presented to the decoder in either of two ways. The Bipolar One and Bipolar Zero inputs will accept data from differential inputs such as a comparator sensed transformer coupled bus. The Unipolar Data input can only accept noninverted Manchester II encoded data, i.e. Bipolar Zero Out of an encoder. The decoder continuously monitors this data input for a valid sync pattern. Note that while the MED encoder section can generate only a command sync pattern, the decoder can recognize either a command or data sync pattern. A data sync is a logically inverted command sync.

There is a three bit delay between UDI, BOI or BZI input and the decoded NRZ data transmitted out of SDO.

Control of the decoder outputs is provided by the $\overline{RST}$ pin. When $\overline{RST}$ is low, SDO, DCLK and $\overline{NVM}$ are forced low. When $\overline{RST}$ is high, SDO is transmitted out synchronously with the recovered clock DCLK. The $\overline{NVM}$ output remains low after a low to high transition on $\overline{RST}$ until a valid sync pattern is received.

The decoded data at SDO is in NRZ format. DCLK is provided so that the decoded bits can be shifted into an external register on every high to low transition of this clock.

Three bit periods after an invalid Manchester bit is received on UDI, or BOI and BZI, $\overline{NVM}$ goes low synchronously with the questionable data output on SDO. Further, the decoder does not reestablish proper data decoding until another sync pattern is recognized.



For expanded view see Figure 8.

FIGURE 2

Repeater Mode

Manchester II data can be presented to the repeater in either of two ways. The inputs Bipolar One In and Bipolar Zero In will accept data from differential inputs such as a comparator or sensed transformer coupled bus. The input Unipolar Data In accepts only non-inverted Manchester II coded data. The decoder requires a single clock with a frequency 16X or 32X the desired data rate. This clock is selected to 16X with Speed Select low and 32X with Speed Select high. For long data links the 32X mode should be used as this permits a wider timing jitter margin.

The inputs UDI, or BOI, BZI are delayed approximately 1/2 bit period and repeated as outputs $\overline{BOO}$ and $\overline{BZO}$. The 2X ECLK is transmitted out of the repeater synchronously with $\overline{BOO}$ and $\overline{BZO}$.

A low on $\overline{CTS}$ enables ECLK, $\overline{BOO}$, and $\overline{BZO}$. In contrast to the converter mode, a transition on $\overline{CTS}$ does not initiate a synchronization sequence of eight 0's and a command sync. The repeater mode does recognize a command or data sync pulse. SD/CDS is an output which reflects the state of the most recent sync pulse received, with high indicating a command sync and low indicating a data sync.

When $\overline{RST}$ is low, the outputs SDO, DCLK, and $\overline{NVM}$ are low, and $\overline{SRST}$ is set low. $\overline{SRST}$ remains low after $\overline{RST}$ goes high and is not reset until a sync pulse and two valid manchester bits are received with the reset bit low. With $\overline{RST}$ high, NRZ Data is transmitted out of Serial Data Out synchronously with the 1X DCLK.

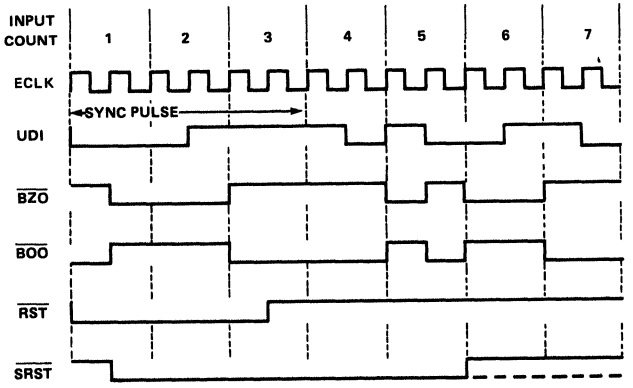


FIGURE 3

Switching Waveforms

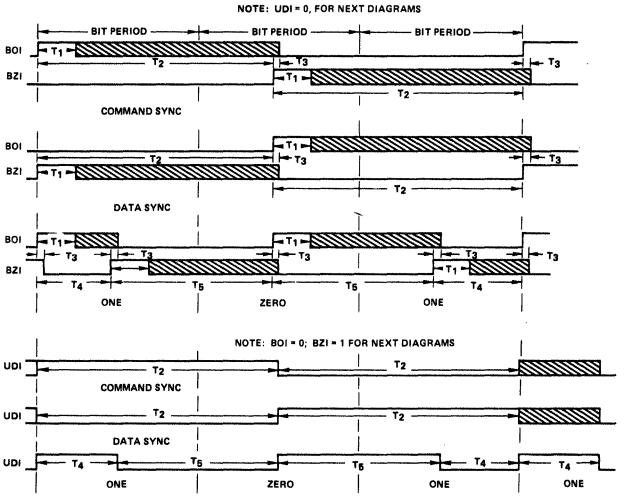


FIGURE 4

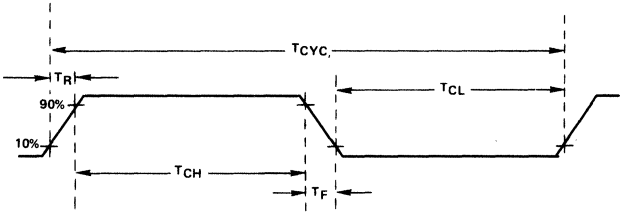


FIGURE 5

NOTE: Reference parameters t6, t7, t8, t9

Encoder Timing

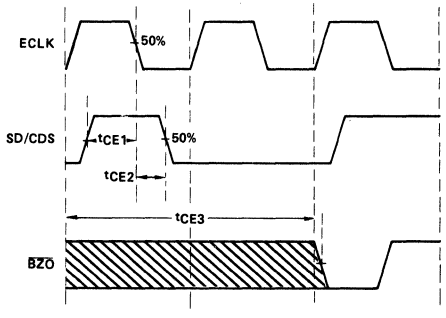
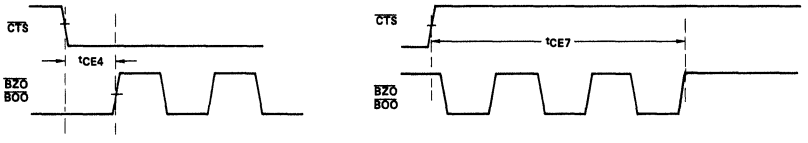


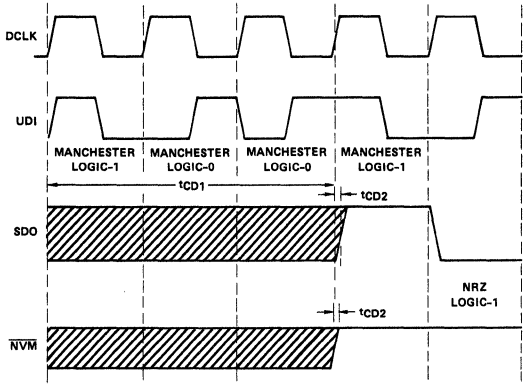
FIGURE 6



NOTE: t_{CE5} – See Figure 1
t_{CE6} – See Figure 1

FIGURE 7

Decoder Timing



NOTE: Manchester Data In is not synchronous with Decoder Clock. Decoder Clock is synchronous with decoded NRZ out of SDO.

FIGURE 8

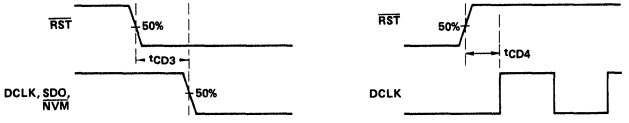


FIGURE 9

Repeater Timing

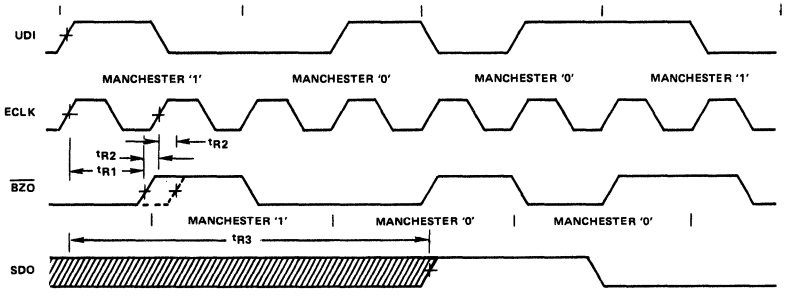


FIGURE 10

MANCHESTER CODE

Nonreturn to Zero (NRZ) code represents the binary values logic-0 and logic-1 with a static level maintained throughout the data cell. In contrast, Manchester code represents data with a level transition in the middle of the data cell. Manchester has bandwidth, error detection, and synchronization advantages over NRZ code.

The Manchester II code Bipolar One and Bipolar Zero shown below are logical complements. The direction of the transition indicates the binary value of data. A logic-0 in Bipolar One is defined as a low to high transition in the middle of the data cell, and a logic-1 as a high to low mid bit transition. Manchester I code is not properly decoded by the HD-6409. Manchester II is also known as Biphase-L code.

The bandwidth of NRZ is from DC to the clock frequency fc/2, while that of Manchester is from fc/2 to fc. Thus, Manchester can be AC or transformer coupled, which has considerable advantages over DC coupling. Also, the ratio of maximum to minimum frequency of Manchester extends one octave, while the ratio for NRZ is the range of 5-10 octaves. It is much easier to design a narrow band than a wideband amp.

Secondly, the mid bit transition in each data cell provides the code with an effective error detection scheme. If noise produces a logic inversion in the data cell such that there is no transition, an error indiction is given, and synchronization must be re-established. This places relatively stringent requirements on the incoming data.

The synchronization advantages of using the HD-6409 and Manchester code are several fold. One is that Manchester is a self clocking code. The clock in serial data communication defines the position of each data cell. Non self clocking codes, as NRZ, often require an extra clock wire or clock track (in magnetic recording). Further, there can be a phase variation between the clock and data track. Crosstalk between the two may be a problem. In Manchester, the serial data stream contains both the clock and the data, with the position of the mid bit transition representing the clock, and the direction of the transition representing data. There is no phase variation between the clock and the data.

A second synchronization advantage is a result of the number of transitions in the data. The decoder resynchronizes on each transition, or at least once every data cell. In contrast, receivers using NRZ, which does not necessarily have transitions, must resynchronize on frame bit transitions, which occur far less often, usually on a character basis. This more frequent resynchronization eliminates the cumulative effect of errors over sucessive data cells. A final synchronization advantage concerns the HD-6409's sync pulse used to initiate synchronization. This three bit wide pattern is sufficiently distinct from Manchester data that a false start by the receiver is unlikely.

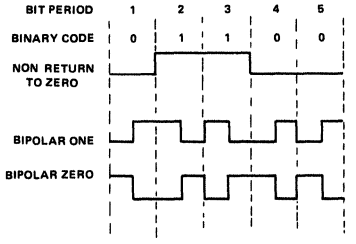
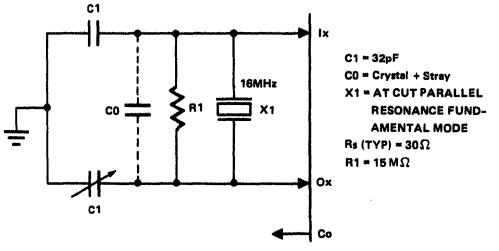
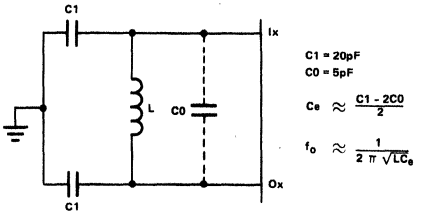


FIGURE 11

Crystal Oscillator Mode



LC Oscillator Mode



HD-6406

CMOS Programmable Asynchronous Communication Interface

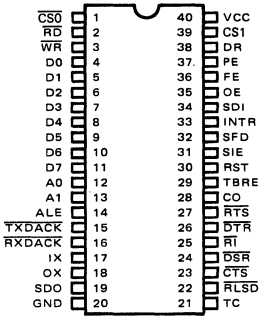
Advance Information

Features

- SINGLE CHIP UART/BRG
- DC TO 16MHz OPERATION
- CRYSTAL OR EXTERNAL CLOCK INPUT
- ON CHIP BAUD RATE GENERATOR ...72 SELECTABLE BAUD RATES
- DMA OR VECTORED INTERRUPT MODE
- MASKABLE INTERRUPTS
- MICROPROCESSOR BUS ORIENTED INTERFACE
- SCALED SAJI IV CMOS PROCESS
- SINGLE 5V POWER SUPPLY
- LOW POWER – 1mA/MHz TYPICAL
- COMPLETE MODEM INTERFACE
- LINE BREAK GENERATION AND DETECTION
- LOOPBACK AND ECHO MODES

Pinout

Top View



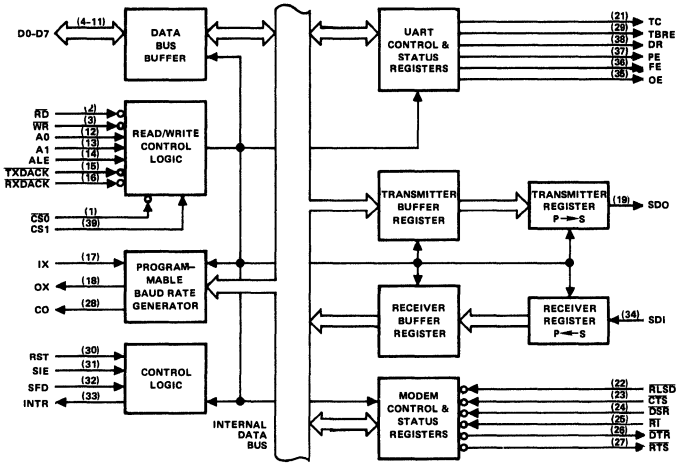
Description

The HD-6406 (PACI) is a high performance programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG) on a single chip. Utilizing Harris Semiconductor's advanced Scaled SAJI IV CMOS process, the PACI will support data rates from DC to 1Mbaud (0-16MHz clock). In addition to all standard UART functions, the PACI includes a complete Data Communications Equipment (DCE) interface.

Provision is made for DMA control of the PACI so that operation at the higher data rates is not hindered by slow microprocessor response times. An ALE control input permits direct interfacing to multiplexed data/address buses common to many microprocessors.

The interrupt structure of the PACI is user-programmable and can be configured to provide a single interrupt for any status change. A subsequent read of an internal status register will identify the source of the interrupt. If desired, the PACI can also provide separate hardware interrupt outputs for the receiver, transmitter and modem status changes. Separate error condition outputs can be used to pinpoint the exact cause of any detected error condition.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow standard IC Handling Procedures.

Pin Description

I/O	PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
I	1, 39	$\overline{CS0}$, CS1	Low, High	CHIP SELECTS: The chip select inputs act as enable signals for the $\overline{RD}$ and $\overline{WR}$ input signals during all non-DMA bus operations.
I	2	$\overline{RD}$	Low	READ: The $\overline{RD}$ input causes data to be output to the data bus (D0-D7). The data output depends upon the state of the address inputs (A0, A1) during non-DMA operations. During DMA read operations ($\overline{RXDACK}$ true) the address inputs are ignored and the contents of the Receiver Buffer Register is output providing the DR bit in the Modem Status Register (MSR) is true.
I	3	$\overline{WR}$	Low	WRITE: The $\overline{WR}$ input causes data from the data bus (D0-D7) to be input to the PACI. Addressing and chip select action is the same as for read operations with the exception that $\overline{TXDACK}$ provides the select qualifier for DMA write operations providing the TBRE bit in the MSR is true.
I/O	4-11	D0-D7	High	DATA BITS 0-7: The Data Bus provides eight, 3-state input/output lines for the transfer of data, control and status information between the PACI and the CPU. For character formats of less than 8 bits, the corresponding D7, D6 and D5 are considered "don't cares" for data writes and are 0 for data reads. These lines are normally at their high impedance state except during read operations. D0 is the LSB and is the first serial data bit received or transmitted.
I	12, 13	A0, A1	High	ADDRESS 0, 1: The address lines select the various internal registers during CPU bus operations. Qualified DMA operations ignore the address inputs and access the appropriate receive or transmit buffer register.
I	14	ALE	High	ADDRESS LATCH ENABLE: ALE true enables the internal transparent address latches for the A0, A1 inputs. The address is latched when ALE goes false (low).
I	15	$\overline{TXDACK}$	Low	TRANSMIT DMA ACKNOWLEDGE: A true $\overline{TXDACK}$ notifies the PACI that a transmit DMA cycle has been granted. It acts as a chip select which enables the $\overline{WR}$ input to access the Transmitter Buffer Buffer Register when the TBRE bit in the MSR is true.
I	16	$\overline{RXDACK}$	Low	RECEIVE DMA ACKNOWLEDGE: A true $\overline{RXDACK}$ notifies the PACI that a receive DMA cycle has been granted. It acts as a chip select which enables the $\overline{RD}$ input to access the Receiver Buffer Register when the DR bit in the MSR is true.
I,O	17, 18	IX, OX		CRYSTAL/CLOCK: Crystal connections for the internal Baud Rate Generator. IX can also be used as an external clock input in which case OX should be left open.
O	19	SDO	High	SERIAL DATA OUTPUT: Serial data output from the PACI transmitter circuitry. A Mark (1) is high and a Space (0) is low. SDO is held in the Mark condition when the transmitter is disabled with $\overline{CTS}$ false, RST true, when the Transmitter Register is empty, or when in the Loop Mode.
	20	GND	Low	GROUND: Power supply ground connection.
O	21	TC	High	TRANSMISSION COMPLETE: TC goes true when a complete character, including stop bits, has been been transmitted and TBRE is true. TC is reset with a data write to TBR. RST will set TC true.
I	22	$\overline{RLSD}$	Low	RECEIVE LINE SIGNAL DETECT: The logical state of this input is reflected in the $\overline{RLSD}$ bit of the Modem Status Register. Any change of state will cause an interrupt on INTR if INTEN and MIEN are true.
I	23	$\overline{CTS}$	Low	CLEAR TO SEND: The logical state of the $\overline{CTS}$ line is reflected in the CTS bit of the Modem Status Register. Any change of state of $\overline{CTS}$ causes INTR to be set true when INTEN and MIEN are true. A false level on $\overline{CTS}$ will inhibit transmission of data on the SDO output and will hold SDO in the Mark (high) state. If $\overline{CTS}$ goes false during transmission, the current character being transmitted will be completed. $\overline{CTS}$ does not affect the Loop mode of operation.
I	24	$\overline{DSR}$	Low	DATA SET READY: The logical state of the $\overline{DSR}$ line is reflected in the Modem Status Register. Any change of state of $\overline{DSR}$ will cause INTR to be set if INTEN and MIEN are true. The state of this signal does not affect any other circuitry within the PACI.
I	25	$\overline{RI}$	Low	RING INDICATOR: The logical state of the $\overline{RI}$ line is reflected in the Modem Status Register. Any change of state of $\overline{RI}$ will cause INTR to be set if INTEN and MIEN are true. The state of this signal does not affect any other circuitry within the PACI.
O	26	$\overline{DTR}$	Low	DATA TERMINAL READY: The $\overline{DTR}$ signal can be set (low) by writing a logic 1 to the appropriate bit in the Modem Control Register (MCR). This signal is cleared (high) by writing a logic 0 to the same bit in the MCR or whenever a RST (High) is applied to the PACI.

Pin Description

I/O	PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
0	27	$\overline{RTS}$	Low	REQUEST TO SEND: The $\overline{RTS}$ signal can be set (low) by writing a logic 1 to the appropriate bit in the MCR. This signal is cleared (High) by writing a logic 0 to the same bit in the MCR or whenever a RST (High) is applied to the PACI.
0	28	CO		CLOCK OUT: This output is user programmable to provide either buffered IX output or a buffered Baud Rate Generator (16x) clock output. The buffered Ix (Crystal or external clock source) output is provided when the BRSR bit 7 is set to a zero. Writing a logic one to BRSR bit 7 causes the CO output to provide a buffered version of the internal Baud Rate Generator clock which operates at sixteen times the programmed baud rate.
0	29	TBRE	High	TRANSMITTER BUFFER REGISTER EMPTY: The TBRE output is set (high) whenever the Transmitter Buffer Register (TBR) has transferred its data to the Transmit Register. Application of a RST to the PACI will also set the TBRE output. TBRE is cleared (Low) whenever data is written to the TBR.
I	30	RST	High	RESET: The RST input forces the PACI into an "Idle" mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The UART Status Register (USR) is cleared except for the TBRE and TC bits which are set. The PACI remains in an "Idle" state until programmed to resume serial data activities. The RST input is a Schmitt trigger input.
I	31	SIE	High	SINGLE INTERRUPT ENABLE: A true (high) level on the SIE input enables interrupts caused by the DR and TBRE status bits. This enables the user to utilize a single hardware interrupt signal (INTR) for any status change within the PACI.
I	32	SFD	High	STATUS FLAGS DISABLE: Holding the SFD input true (high) prevents the true state of the USR bits PE, OE, FE and TC from causing an interrupt. This control input, like the SIE input, enables the user to define what status changes will effect the INTR output.
0	33	INTR	High	INTERRUPT REQUEST: The INTR output is enabled by the INTEN bit in the Modem Control Register (MCR). The MIEN bit and the SIE and SFD control inputs selectively enable various status changes to provide an input to the INTR logic. Figure 9 shows an overall view of the relationship of these interrupt control signals.
I	34	SDI	High	SERIAL DATA INPUT: Serial data input to the PACI receiver circuits. A Mark (1) is high, and a Space (0) is low. Data inputs on SDI are disabled when operating in the loop mode, when RST is true or when the Receiver Enable (REN) bit in the MCR register is false.
0	35	OE	High	OVERRUN ERROR: A true level on the OE output indicates that the Receiver Buffer Register (RBR) was full when a character was received. Transfer to the RBR will not occur. OE is updated each time a character is transferred to the RBR. RST high will set OE low.
0	36	FE	High	FRAMING ERROR: A true level on the FE output indicates that there were invalid stop bits in the last received character. The FE output is updated each time a character is transferred to the RBR. RST high will reset FE.
0	37	PE	High	PARITY ERROR: PE is set true whenever the parity of a received character does not match the programmed parity. The PE output is updated each time a character is transferred to the RBR. PE is reset whenever RST is true or when no parity check is programmed.
0	38	DR	High	DATA READY: A true level indicates that a character has been received, transferred to the RBR and is ready for transfer to the CPU. DR is reset on a data read of the RBR or when RST is true.
	40	VCC	High	+5 VOLT SUPPLY: Positive power supply connection.

Functional Description

RESET

During and after power-up, the PACI should be given a RST high for at least two IX clock cycles in order to initialize and drive the PACI's circuits to an idle mode until proper programming can be done. A high on RST causes the following events to occur:

- Resets the internal BRG circuits, clock counters and bit counters. The Baud Rate Select Register (BRSR) is not affected.
- Clears the UART Status Register (USR) except for TC and TBRE which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. Note that the UART Control Register (UCR) is not affected.

Following removal of the reset condition (RST low), the PACI remains in the idle mode until programmed to its desired system configuration.

PROGRAMMING THE HD-6406 PACI

The complete functional definition of the PACI is programmed by the systems software. A set of control words (UCR, BRSR and MCR) must be sent out by the CPU to initialize the PACI to support the desired communication format. These control words will program the character length, number of stop bits, even/odd/no parity, baud rate etc. Once programmed, the PACI is ready to perform its communication functions.

The control registers can be written to in any order, however the MCR should be written to last because it controls the interrupt enables, modem control outputs and the receiver enable bit. Once the PACI is programmed and operational these registers can be updated any time that the PACI is not immediately transmitting or receiving data.

Table 1 shows the required control signals to access the PACI's internal registers.

ALE	$\overline{CS0}$	CS1	A1	A0	$\overline{WR}$	$\overline{RD}$	OPERATION
1 or ↓	0	1	0	0	↓	1	Data bus → TBR
1 or ↓	0	1	0	0	1	↓	RBR → Data bus
1 or ↓	0	1	0	1	↓	1	Data bus → UCR
1 or ↓	0	1	0	1	1	↓	USR → Data bus
1 or ↓	0	1	1	0	↓	1	Data bus → MCR
1 or ↓	0	1	1	0	1	↓	MCR → Data bus
1 or ↓	0	1	1	1	↓	1	Data bus → BRSR
1 or ↓	0	1	1	1	1	↓	MSR → Data bus

TABLE 1

The Address Latch Enable (ALE) input acts as an address latch control signal during these operations. If ALE is left high, the address inputs A0, A1 must be held true during the entire bus operation (demultiplexed bus operation). For multiplexed bus applications the address inputs A0, A1 are latched when ALE goes low. In this case A0 and A1 are not required to be held true for the entire bus cycle.

DMA control of the PACI is discussed in a later section of this data sheet and involves reading and writing of the Receiver and Transmitter Buffer Registers (RBR and TBR).

The following descriptions discuss the control registers in detail.

UART CONTROL REGISTER (UCR)

The UCR is a write only register which configures the UART transmitter and receiver circuits. Data bits D7 and D6 are not used but should always be set to a zero in order to insure software compatability with future product upgrades. During the Echo Mode, the transmitter always repeats the received word and parity, even when the UCR is programmed with different or no parity.

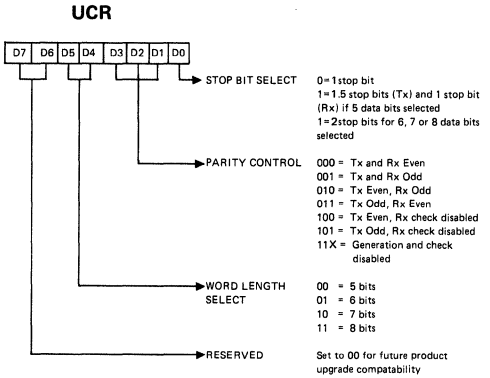


FIGURE 1

BAUD RATE SELECT REGISTER (BRSR)

The PACI is designed to operate with a single crystal or external clock driving the IX input pin. The Baud Rate Select Register is used to select which divide ratio (one of 72) the internal Baud Rate Generator circuitry will use. The internal circuitry is seperated into two separate counters, a Prescaler and a Divisor Select. The Prescaler can be set to any one of four division rates, ÷1, ÷3, ÷4 or ÷5. This Prescaler design has been optimized to provide standard baud rates using any one of three popular crystal frequencies. By using one of these common system clock frequencies, 1.8432 MHz, 2.4576 MHz or 3.072 MHz and a Prescaler of ÷3, ÷4 or ÷5 respectively, the Prescaler output will provide a constant 614,400 Hz. When this frequency is further divided by the Divisor Select counter, any of the standard baud rates from 50 to 38.4 KBaud can be selected (see Table 2). Non-standard baud rates up to 1 Mbaud can be selected by using different input frequencies (up to 16 MHz) and/or different Prescaler and Divisor Select ratios. The baud rate generator provides a clock which is 16 times the desired baud rate. For example, in order to operate at a 1 Mbaud data rate a 16 MHz crystal, a Prescale rate of ÷1, and a Divisor Select rate of "external" would be used to provide a 16 MHz clock as the output of the Baud Rate Generator to the Transmitter and Receiver Circuts.

The C0 select bit in the BRSR selects whether a buffered version of the external frequency input (IX input) or the Baud Rate Generator output (16X baud rate clock) will be output on the C0 output (pin 28). The Baud Rate Generator output will always be a 50% nominal duty cycle except when "external" is selected and the Prescaler is set to ÷3 or ÷5.

BRSR

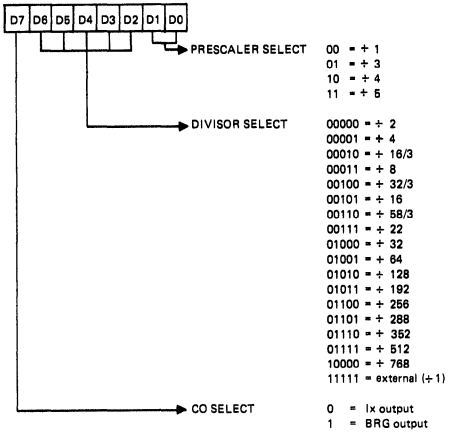


FIGURE 2

BAUD RATE	DIVISOR
38.4K	external
19.2K	2
9600	4
7200	16/3
4800	8
3600	32/3
2400	16
2000*	58/3
1800	22
1200	32
600	64
300	128
200	192
150	256
134.5*	288
110*	352
75	512
50	768

TABLE 2

Note: These baud rates are based upon the following input frequency/Prescale divisor combinations.
1.8432MHz and Prescale = ÷3
2.4576MHz and Prescale = ÷4
3.072MHz and Prescale = ÷5

*All baud rates are exact except for:

BAUD RATE	ACTUAL	PERCENT ERROR
2000	1986.2	0.69%
134.5	133.33	0.87%
110	109.71	0.26%

MODEM CONTROL REGISTER

The MCR is a general purpose control register which can be written to and read from. The $\overline{RTS}$ and $\overline{DTR}$ outputs are directly controlled by their associated bits in this register. Note that a logic one asserts a true logic level (low) at these output pins. The Interrupt Enable (INTEN) bit is the overall control for the INTR output pin. When INTEN is false, INTR is held false (low). The Operating Mode bits configure the PACI into one of four possible modes. "Normal" configures the PACI for normal full or half duplex communications. "Transmit Break" enables the transmitter to only transmit break characters (Start, Data and Stop bits all are logic zero). The Echo Mode causes any data that is received on the SDI input pin to be re-transmitted on the SDO output pin. Note that this output is a buffered version of the data seen on the SDI input and is not a re-synchronized output (see Figure 4). The Loop Test Mode internally routes transmitted data to the receiver circuitry for the purpose of self test. The transmit data is disabled from the SDO output pin. The Receiver Enable bit gates off the input to the receiver circuitry when in the false state. Modem Interrupt Enable will permit any change in modem status line inputs ($\overline{CTS}$, $\overline{RI}$, $\overline{RLSD}$, $\overline{DSR}$) to cause an interrupt when this bit is enabled. Bit D7 must always be written to with a logic zero to insure correct PACI operation.

MCR

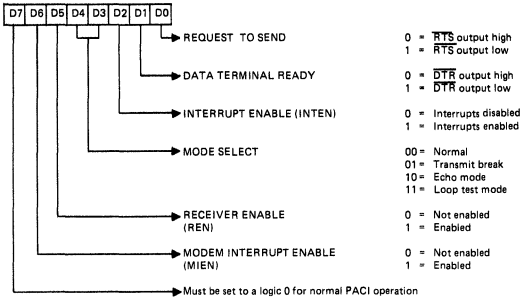


FIGURE 3

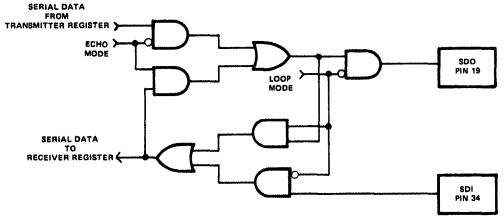


FIGURE 4 – Loop and Echo Mode Functionality

5 DATA COMMUNICATION

UART STATUS REGISTER (USR)

The USR provides a single register that the controlling system can examine to ascertain if errors have occured or if other status changes in the PACI require the system's attention. For this reason, the USR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the PACI. Three error flags OE, FE and PE report the status of any error conditions detected in the receiver circuitry. These error flags are updated with every character received during reception of the stop bits. The Overrun Error (OE) indicates that a character in the Receiver Register has been received and cannot be transferred to the Receiver Buffer Register (RBR) because the RBR was not read by the CPU. Framing Error (FE) indicates that the last character received contained improper stop bits. This could be caused by the total absence of the required stop bit(s) or by a stop bit(s) that was too short to be properly detected. Parity Error (PE) indicates that the last character received contained a parity error based on the programmed parity of the receiver and the calculated parity of the received characters data and parity bits.

The Received Break (RBRK) status bit indicates that the last character received was a break character. A break character would be considered to be an invalid data character in that the entire character including parity and stop bits are a logic zero.

The Modem Status bit is set whenever a transition is detected on any of the Modem input lines ($\overline{RI}$, $\overline{RLSD}$, $\overline{CTS}$ or $\overline{DSR}$). A subsequent read of the Modem Status Register will show the state of these four signals. Assertion of this bit will cause an interrupt (INTR) to be generated if the MIEN and INTEN bits in the MCR register are enabled.

The Transmission Complete (TC) bit indicates that both the TBR and Transmitter Registers are empty and the PACI has completed transmission of the last character it was commanded to transmit. The assertion of this bit will cause an interrupt (INTR) if the SFD (pin 32) input is low and the INTEN bit in the MCR register is true.

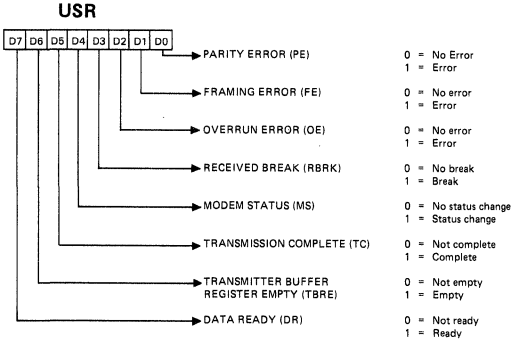


FIGURE 5

The Transmitter Buffer Register Empty (TBRE) bit indicates that the TBR register is empty and ready to receive another character. Assertion of this bit will cause an interrupt if the SIE (pin 31) input is high and the INTEN bit in the MCR is enabled.

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character and that the CPU may access this data. An interrupt will be generated (INTR) if SIE input is high and the INTEN bit is enabled.

MODEM STATUS REGISTER (MSR)

The MSR provides a means whereby the CPU can read the modem signal inputs by accessing the data bus interface of the PACI. Like all of the register images of external pins in the PACI, true logic levels are represented by a high (1) signal level. By following this consistent definition the system software need not be concerned with whether external signals are high or low true. In particular the modem signal inputs are low true, thus a 0 (true assertion) at a modem input pin is represented by a 1 (true) in the MSR.

Any change of state of any of the modem input signals will set the Modem Status (MS) bit in the USR register. When this happens an interrupt (INTR) will be generated if the MIEN and INTEN bits of the MCR are enabled.

The Ring Indicator ($\overline{RI}$) input indicates to the PACI that the modem is receiving a ringing signal.

The Receive Line Signal Detect ($\overline{RLSD}$) input is used to notify the PACI that the signal quality received by the modem is within acceptable limits.

The Data Set Ready ($\overline{DSR}$) input is a status indicator from the modem to the PACI which indicates that the modem is ready to provide received data to the PACI receiver circuitry.

Clear to Send ($\overline{CTS}$) is both a status and control signal from the modem that tells the PACI that the modem is ready to receive transmit data from the PACI transmitter output (SDO). A high (false) level on this input will inhibit the PACI from beginning transmission and if asserted in the middle of a transmission will only permit the PACI to finish transmission of the current character.

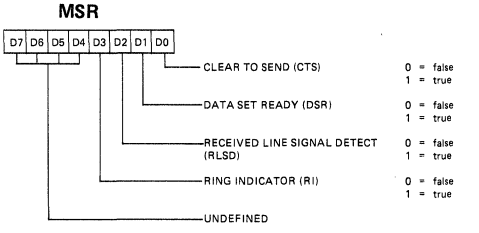
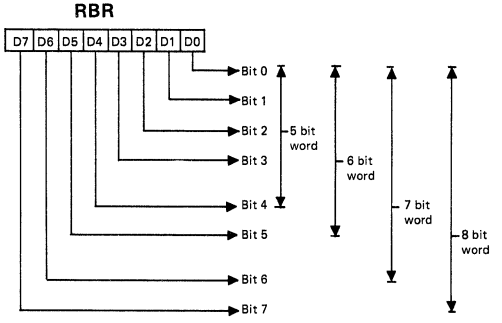


FIGURE 6

RECEIVER BUFFER REGISTER (RBR)

The receiver circuitry in the PACI is programmable for 5, 6, 7 or 8 data bits per character. For words of less than 8 bits, the data is right justified to the LSB (D0). Bit D0 of a data word is always the first data bit received. The unused bits in a less than 8 bit word, at the parallel interface, are set to 0 by the PACI. Received data at the SDI input pin is shifted into the Receiver Register by an internal 1X clock

which has been synchronized to the incoming data based on the position of the start bit. When a complete character has been shifted into the Receiver Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. Both the DR output pin and DR flag in the USR register are set. This double buffering of the received data permits continuous reception of data without losing any of the received data. While the Receiver Register is shifting a new character into the PACI, the Receiver Buffer Register is holding a previously received character for the system CPU to read. Failure to read the data in the RBR before complete reception of the next character can result in the loss of the data in the Receiver Register. The OE flag in the USR register indicates the overrun condition.

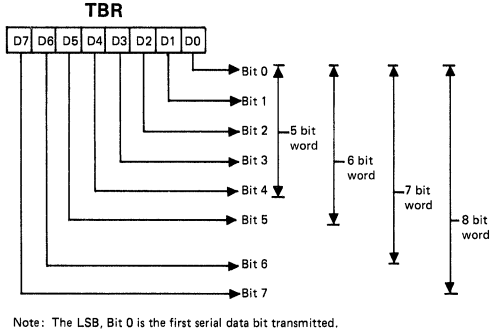


Note: The LSB, Bit 0 is the first serial data bit received.

FIGURE 7

TRANSMITTER BUFFER REGISTER (TBR)

The Transmitter Buffer Register (TBR) accepts parallel data from the microprocessor data bus (D0-D7) and holds it until the Transmitter Register is empty and ready to accept a new character for transmission. The transmitter always has the same word length and number of stop bits as the receiver. For words of less than 8 bits the unused bits at the microprocessor data bus are ignored by the transmitter. Bit 0, which corresponds to D0 at the data bus, is always the first serial data bit transmitted. Provision is made for the transmitter parity to be the same or different from the receiver. The TBRE output pin and flag (USR register) reflect the status of the TBR. The TC output pin and flag (USR register) indicates when both the TBR and TR are empty.



Note: The LSB, Bit 0 is the first serial data bit transmitted.

FIGURE 8

PACI INTERRUPT STRUCTURE

The PACI has provision for both software and hardware masking of interrupts generated for the INTR output pin. The two input pins, SIE and SFD, provide the mask control for the receiver and transmitter status interrupts. Two control bits in the MCR register, MIEN and INTEN, control modem status interrupts and overall PACI interrupts respectively. Figure 9 illustrates the logical control function provided by these signals.

The modem status inputs ($\overline{RLSD}$, $\overline{RI}$, $\overline{DSR}$ and $\overline{CTS}$) will trigger the edge detection circuitry with any change of status. Reading the MSR register will clear the detect circuit but has no effect on the status bits themselves. These status bits always reflect the state of the input pins regardless of the mask control signals. Note that the state (high or low) of the status bits are inverted versions of the actual input pins.

The edge detection circuits for the USR register signals will trigger only for a positive edge (true assertion) of these status bits. Reading the USR register not only clears the edge detect circuit but also clears (sets to 0) all of the status bits. The output pins associated with these status bits are not affected by reading the USR register.

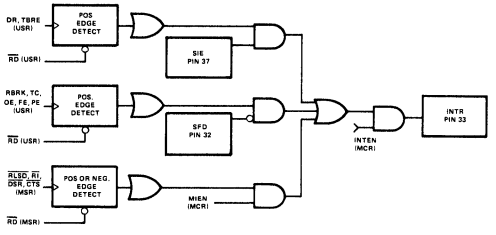


FIGURE 9

DMA CONTROL OF THE PACI

Because of the high data rates possible with the PACI, provision for DMA control of the transmitter and receiver buffer registers has been included in the design. The $\overline{RXDACK}$ and $\overline{TXDACK}$ inputs in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs are driven by the system DMA controller to access the RBR and TBR registers respectively.

Reading of the RBR via the $\overline{RXDACK}$ control signal requires that the DR bit in the USR is set (high) and that the $\overline{RD}$ input be driven low. When these conditions are

met the address logic overrides the address inputs (A0, A1) and forces a read of the RBR. Similarly, a DMA write to the TBR requires that the TBRE bit in the USR register is set (high) and that $\overline{TXDACK}$ and $\overline{WR}$ are asserted by the DMA controller. Once again the address logic overrides the address inputs and forces a write to the TBR register.

The $\overline{CS0}$ and CS1 inputs would normally be in their inactive state during DMA accesses. The A0, A1, and ALE inputs are overridden during DMA operations and as such their logical state is a don't care.

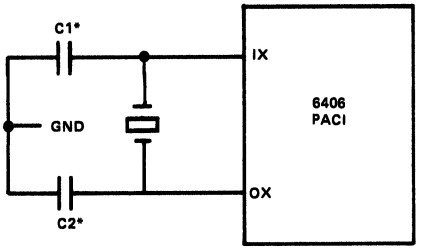
CRYSTAL OPERATIONS

The PACI crystal oscillator circuitry is designed to operate with a fundamental, parallel resonent crystal. This circuit is the same as used in the Harris 82C84A clock generator/driver and as such the general applications information contained in Tech Brief TB-47 that applies to the oscillator operation will be pertinent to the PACI. To summarize Table 3 and Figure 10 show the required crystal parameters and crystal circuit configuration respectively.

When using an external clock source the Ix input is driven and the Ox output is left open. Power consumption when using an external clock is typically 2 times lower than when using a crystal. This is due to the sinusoidal nature of the drive circuitry when using a crystal.

PARAMETER	TYPICAL CRYSTAL SPECIFICATION
Frequency	1.0 to 16MHz
Type of Operation	Parallel resonent, Fund. mode
Load Capacitance (CL)	20 or 32 pf. (typ.)
R_{series}(Max.)	100 ohms (f=16 MHz, CL = 32pf.) 200 ohms (f=16 MHz, CL = 20pf.)

TABLE 3



*** C1 = C2 ≈ 20pf for CL = 20pf.**
C1 = C2 ≈ 47pf for CL = 32pf.

FIGURE 10

REGISTER BIT ASSIGNMENT SUMMARY

REGISTER NAME	MNEMONIC	BIT ASSIGNMENT							
		LSB 0	1	2	3	4	5	6	MSB 7
Receiver Buffer	RBR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Transmitter Buffer	TBR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
UART Status	USR	Parity Error (PE)	Framing Error (FE)	Overrun Error (OE)	Received Break (RBRK)	Modem Status (MS)	Transmission Complete (TC)	Transmitter Buffer Reg. empty (TBRE)	Data Ready (DR)
UART Control	UCR	Stop Bit Select	Parity Control 0	Parity Control 1	Parity Control 2	Word Length 0	Word Length 1	Reserved*	Reserved *
Modem Control	MCR	Request To Send (RTS)	Data Terminal Ready (DTR)	Interrupt Enable (INTEN)	Mode Select 0	Mode Select 1	Receiver Enable (REN)	Modem Interrupt enable (MIEN)	0
Modem Status	MSR	Clear to Send (CTS)	Data Set Ready (DSR)	Received Line Signal Detect (RLSD)	Ring Indicator (RI)	Not Used	Not Used	Not Used	Not Used
Bit Rate Select	BRSR	Prescaler Select 0	Prescaler Select 1	Divisor Select 0	Divisor Select 1	Divisor Select 2	Divisor Select 3	Divisor Select 4	Co Select

* Reserved for future use. Always set to zero (0) to maintain future software compatibility.

Specifications

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0 Volts	Operating Temperature Range	
Operating Voltage Range	+4V to +7V	Industrial	-40°C to +85°C
Input Voltage Applied	GND -2.0V to +6.5V	Military	-55°C to +125°C
Output Voltage Applied	GND -0.5V to VCC +0.5V	Maximum Power Dissipation	1 Watt
Storage Temperature Range	-65°C to +150°C		

CAUTION: Stresses above those listed in the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D. C. CHARACTERISTICS

VCC = 5.0V ±10%; T_A = -40°C to +85°C (-9); T_A = -55°C to +125°C (-2, -8)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0		V	
VIL	Logical Zero Input Voltage		0.8	V	
VTH	Schmidt Trigger Logical One Input Voltage	VCC -0.5		V	Reset Input
VTL	Schmidt Trigger Logical One Input Voltage		GND +0.5	V	Reset Input
VIH (CLK)	Logical One Clock Voltage	VCC -0.5		V	External Clock
VIL (CLK)	Logical Zero Clock Voltage		GND +0.5	V	External Clock
VOH	Output High Voltage	3.0 VCC -0.4		V V	IOH = -2.5mA IOH = -400μA
VOL	Output Low Voltage		0.4	V	IOL = +2.5mA
IIL	Input Leakage Current	-1.0	+1.0	μA	$0V \leq VIN \leq VCC$
IOL	Output Leakage Current	-10.0	+10.0	μA	$0V \leq V0 \leq VCC$
ICCOP*	Operating Power Supply Current		3	ma	External Clock F = 2.4576 MHz VCC = 5.5V VIN = VCC or GND Outputs Open

*Guaranteed and sampled, but not 100% tested. ICCOP is typically $\leq$1mA/MHz

CAPACITANCE

T_A = 25°C; VCC = GND = 0V; VIN = +5V or GND

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
CIN*	Input Capacitance		10	pf	FREQ = 1 MHz Unmeasured pins returned to GND
C_{OUT}*	Output Capacitance		15	pf	
$C_{I/O}$*	I/O Capacitance		20	pf	

*Guaranteed and sampled, but not 100% tested

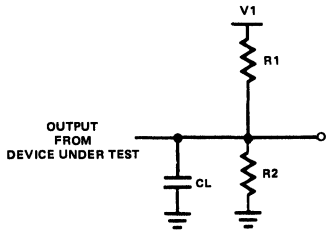
A. C. CHARACTERISTICS

VCC = +5V ±10%, GND = 0V: TA = -40°C to +85°C (-9)
TA = -55°C to +125°C (-2, -8)

TIMING REQUIREMENTS

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TLHLL	ALE Pulse Width	50		ns	
TAVLL	Address Setup	20		ns	
TLLAX	Address Hold	20		ns	
TSVCTL	Select Setup to Control leading edge	30		ns	
TCTHSX	Select Hold from Control Trailing Edge	50		ns	
TCTLCTH	Control Pulse Width	150		ns	Control Consists of $\overline{RD}$ or $\overline{WR}$
TCTHCTL	Control Disable to Control Enable	100		ns	
TRLDV	Read low to Data Valid		120	ns	1
TRHDZ	Read Disable	0	60	ns	2
TCTHLH	Control Inactive to ALE High	20		ns	
TDVWH	Data Setup Time	50		ns	
TWHDX	Data Hold Time	20		ns	
FC	Clock Frequency	0	16	MHz	TCHCL + TCLCH must be ≥ 62.5ns
TCHCL	Clock High Time	25		ns	
TCLCH	Clock Low Time	25		ns	
TR/TF	IX Input Rise/Fall Time (10% - 90%) (External Clock)		tx	ns	tx ≤1/(6FC) or 50ns whichever is smaller
TFCO	Clock Output Fall Time		15	ns	CL = 50pf
TRCO	Clock Output Rise Time		15	ns	CL = 50pf

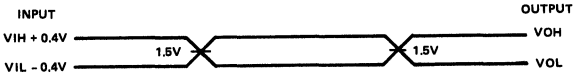
A.C. Test Circuits



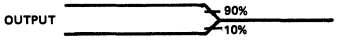
TEST CONDITION	V1	R1	R2	CL
1 Propagation Delay	1.7V	520	∞	100pF
2 Disable Delay	VCC	5K	5K	50pF

A. C. Testing Input, Output Waveform

PROPAGATION DELAY



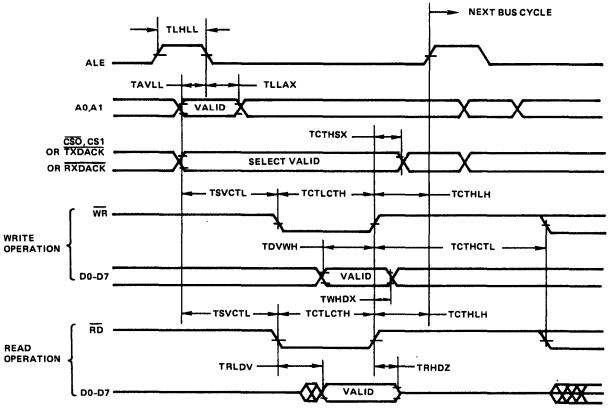
ENABLE/DISABLE DELAY



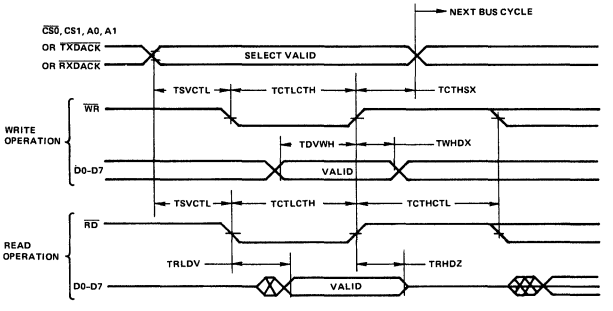
A. C. Testing: All input signals must switch between VIL -0.4V and VIH +0.4V. TR and TF must be less than or equal to 15ns.

Timing Diagrams

MULTIPLEXED BUS OPERATION



DEMULTIPLEXED BUS OPERATION (ALE HIGH)



82C52

CMOS Serial Controller Interface

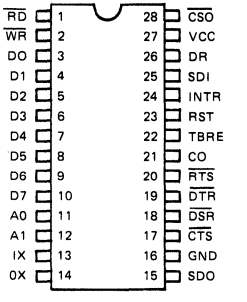
Preview

Features

- SINGLE CHIP UART/BRG
- DC TO 16MHz OPERATION
- CRYSTAL OR EXTERNAL CLOCK INPUT
- ON CHIP BAUD RATE GENERATOR
  ...72 SELECTABLE BAUD RATES
- INTERRUPT MODE WITH MASK CAPABILITY
- MICROPROCESSOR BUS ORIENTED INTERFACE
- 80C86 COMPATIBLE
- SCALED SAJI IV CMOS PROCESS
- SINGLE 5V POWER SUPPLY
- LOW POWER – 1mA/MHz TYPICAL
- MODEM INTERFACE
- LINE BREAK GENERATION AND DETECTION
- LOOPBACK AND ECHO MODES

Pinout

Top View



Description

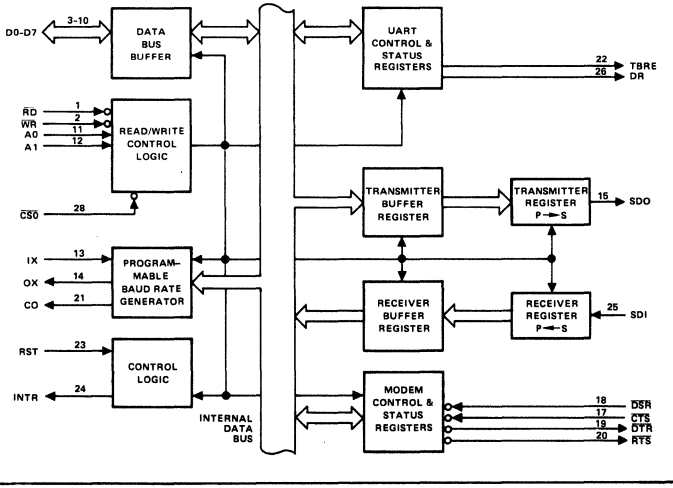
The 82C52 is a high performance programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG) on a single chip. Utilizing the Harris advanced Scaled SAJI IV CMOS process, the 82C52 will support data rates from D.C. to 1M baud asynchronously with a 16X clock (0-16 MHz clock frequency).

The on-chip Baud Rate Generator can be programmed for any one of 72 different baud rates using a single industry standard crystal or external frequency source. A unique pre-scale divide circuit has been designed to provide standard RS-232-C baud rates when using any one of three industry standard baud rate crystals (1.8432 MHz, 2.4576 MHz, or 3.072MHz).

A programmable buffered clock output (CO) is available and can be programmed to provide either a buffered oscillator or 16X baud rate clock for general purpose system usage.

Inputs and outputs have been designed with full TTL/CMOS compatibility in order to facilitate mixed TTL/NMOS/CMOS system design.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow standard IC Handling Procedures.

HARRIS

HD-6402

CMOS/LSI Universal Asynchronous Receiver Transmitter (UART)

Features

- OPERATION FROM D. C TO 2.0MHz @ 5.0 VOLTS
- LOW POWER-TYP. 10mW @ 2.0MHz AND 5.0 VOLTS
- PROGRAMMABLE WORD LENGTH, STOP BITS AND PARITY
- AUTOMATIC DATA FORMATTING AND STATUS GENERATION
- COMPATIBLE WITH INDUSTRY STANDARD UART'S
- SINGLE POWER SUPPLY

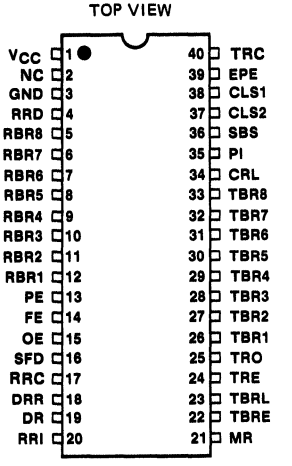
Description

The HD-6402 is a CMOS/LSI subsystem for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits. The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two or one and one-half when transmitting 5 bit code.

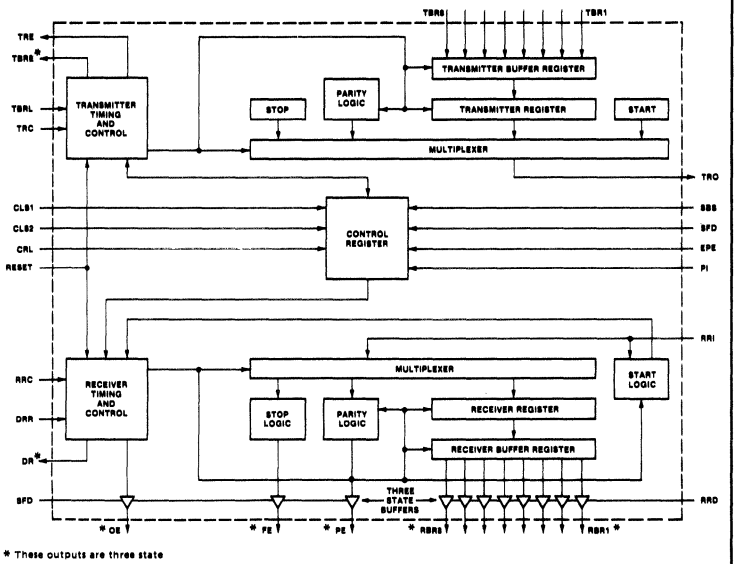
The HD-6402 can be used in a wide range of applications including modems, printers, peripherals and remote data aquisition systems. CMOS/LSI technology permits operation clock frequencies up to 2.0MHz (125K Baud) an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 300mW to 10mW. Status logic increases flexibility and simplifies the user interface.

Pinout

TOP VIEW



Functional Diagram



* These outputs are three state

Control Definition

CONTROL WORD					CHARACTER FORMAT			
CLS2	CLS1	PI	EPE	SBS	START BIT	DATA BITS	PARITY BIT	STOP BITS
0	0	0	0	0	1	5	ODD	1
0	0	0	0	1	1	5	ODD	1.5
0	0	0	1	0	1	5	EVEN	1
0	0	0	1	1	1	5	EVEN	1.5
0	0	1	X	0	1	5	NONE	1
0	0	1	X	1	1	5	NONE	1.5
0	1	0	0	0	1	6	ODD	1
0	1	0	0	1	1	6	ODD	2
0	1	0	1	0	1	6	EVEN	1
0	1	0	1	1	1	6	EVEN	2
0	1	1	X	0	1	6	NONE	1
0	1	1	X	1	1	6	NONE	2
1	0	0	0	0	1	7	ODD	1
1	0	0	0	1	1	7	ODD	2
1	0	0	1	0	1	7	EVEN	1
1	0	0	1	1	1	7	EVEN	2
1	0	1	X	0	1	7	NONE	1
1	0	1	X	1	1	7	NONE	2
1	1	0	0	0	1	8	ODD	1
1	1	0	0	1	1	8	ODD	2
1	1	0	1	0	1	8	EVEN	1
1	1	0	1	1	1	8	EVEN	2
1	1	1	X	0	1	8	NONE	1
1	1	1	X	1	1	8	NONE	2

5 DATA COMMUNICATION

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6402-9	-40°C to +85°C
Military HD-6402-2/8	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%. T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0		1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	2.4			V	$I_{OH} = -0.2mA$
V_{OL}	Logical "0" Output Voltage			0.45	V	$I_{OL} = 2.0mA$
I_O	Output Leakage	-1.0		1.0	μA	$0V \leq V_O \leq V_{CC}$
I_{CC}	Supply Current		1.0	100	μA	V_{IN} = GND or V_{CC}; V_{CC} = 5.5V, Output Open
C_{IN}	Input Capacitance*		7.0	8.0	pF	
C_O	Output Capacitance*		8.0	10.0	pF	

*Guaranteed but not 100% tested

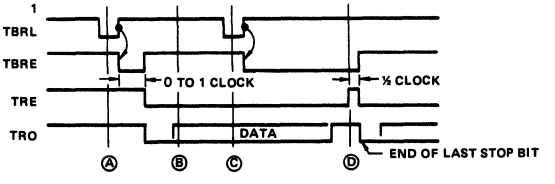
A.C.

		V_{CC} = 5.0V ① T_A = 25°C			V_{CC} = 5.0V ± 10% T_A = Indust. or Mil.				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	CONDITIONS
f_{clock}	Clock Frequency	D.C.		3.0	D.C.		2.0	MHz	
t_{pw}	Pulse Widths CRL, DRR, TBRL	150			150			ns	C_L = 50pF
t_{MR}	Pulse Width MR	350			400			ns	See Switching Time
t_{SET}	Input Data Setup Time	50			50			ns	Waveforms 1, 2, 3
t_{HOLD}	Input Data Hold Time	60			60			ns	
t_{EN}	Output Enable Time			125			160	ns	

NOTE ① All devices guaranteed at worst case limits. Room temperature, 5V data provided for information-not guaranteed.

Transmitter Operation

The transmitter section accepts parallel data, formats it and transmits it in serial form on the TROutput terminal. Ⓐ Data is loaded into the transmitter buffer register from the inputs TR1 through TR8 by a logic low on the TBRLoad input. Valid data must be present at least t_{SET} prior to and t_{HOLD} following the rising edge of TBRL. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TR1. Ⓑ The rising edge of TBRL clears TBREmpty. 0 to 1 clock cycles later, data is transferred to the transmitter register, TREmpty is cleared, TBREmpty is set high, and serial data transmission is started. Output data is clocked by TRClock. The clock rate is 16 times the data rate. Ⓒ A second pulse on TBRLoad loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. Ⓓ Data is automatically transferred to the transmitter register and transmission of that character begins one clock cycle later.



TRANSMITTER TIMING (NOT TO SCALE)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range (Industrial -9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V \pm 10\%$. T_A = Industrial

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	CONDITIONS
D.C.	V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
	V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
	I_{IL}	Input Leakage	-10.0		+10.0	μA	$0V \leq V_{IN} \leq V_{CC}$
	V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -0.2mA
	V_{OL}	Logical "0" Output Voltage			0.45	V	I_{OL} = 2.0mA
	I_O	Output Leakage	-10.0		+10.0	μA	$0V \leq V_O \leq V_{CC}$
	I_{CC}	Supply Current		1.0	800	μA	V_{IN} = GND or V_{CC}, V_{CC} = 5.5V, Output Open
	C_{IN}	Input Capacitance*		7.0	8.0	pF	
	C_O	Output Capacitance*		8.0	10.0	pF	

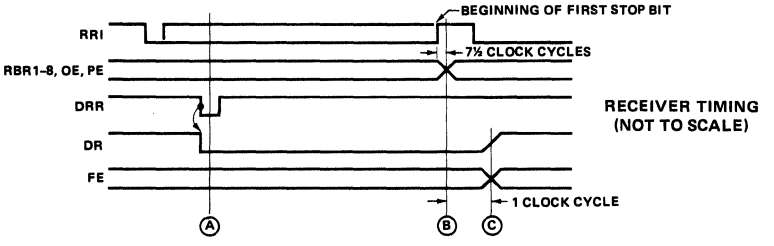
*Guaranteed but not 100% tested.

			$V_{CC} = 5.0V$ ① $T_A = 25°C$			$V_{CC} = 5.0V \pm 10\%$ T_A = Industrial				
	SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	CONDITIONS
A.C.	f_{clock}	Clock Frequency	D.C.		2.0	D.C.		1.0	MHz	
	t_{pw}	Pulse Widths CRL, DRR, TBRL	200			225			ns	C_L = 50pF
	t_{MR}	Pulse Width MR	500			600			ns	See Switching Time
	t_{SET}	Input Data Setup Time	60			75			ns	Waveforms 1, 2, 3
	t_{HOLD}	Input Data Hold Time	75			90			ns	
	t_{EN}	Output Enable Time			150			190	ns	

NOTE ①: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information-not guaranteed.

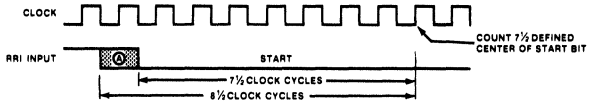
Receiver Operation

Data is received in serial form at the RInput. When no data is being received, RInput must remain high. The data is clocked through the RRClock. The clock rate is 16 times the data rate. Ⓐ A low level on DRReset clears the DReady line. Ⓑ During the first stop bit data is transferred from the receiver register to the RBRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OError indicates overruns. An overrun occurs when DReady has not been cleared before the present character was transferred to the RBRegister. Ⓒ 1 clock cycle later DReady is reset to a logic high, and FError is evaluated. A logic high on FError indicates an invalid stop bit was received, a framing error. A logic high on PError indicates a parity error.



Start Bit Detection

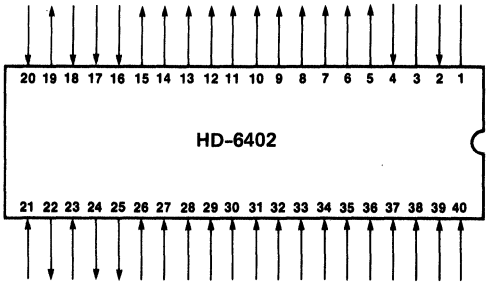
The receiver uses a 16X clock for timing. Ⓐ The start bit could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7½. If the receiver clock is a symetrical square wave, the center of the start bit will be located within ±½ clock cycle, $\pm\frac{1}{32}$ bit or 3.125% giving a receiver margin of 46.875%. The receiver begins searching for the next start bit at the center of the first stop bit.



Pin Assignment And Functions

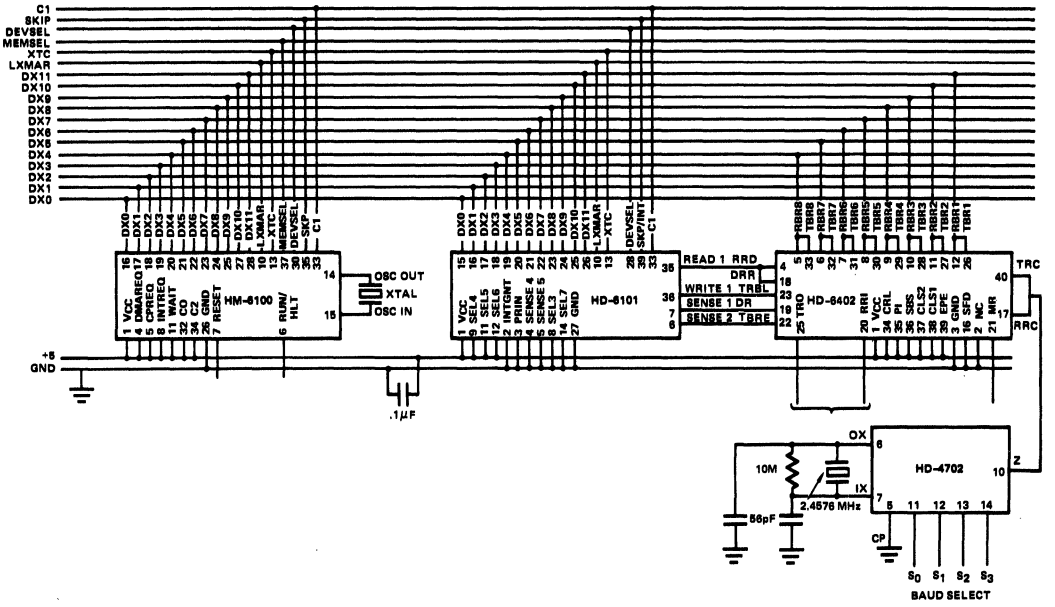
PIN	SYMBOL	DESCRIPTION
1	VCC	Positive Voltage Supply
2	NC	No Connection
3	GND	Ground
4	RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding outputs RBR1-RBR8 to a high impedance state.
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	RBR7	See Pin 5 - RBR8
7	RBR6	See Pin 5 - RBR8
8	RBR5	See Pin 5 - RBR8
9	RBR4	See Pin 5 - RBR8
10	RBR3	See Pin 5 - RBR8
11	RBR2	See Pin 5 - RBR8
12	RBR1	See Pin 5 - RBR8
13	PE	A high level on PARITY ERROR indicates received parity does not match parity programmed by control bits. When parity is inhibited this output is low.

PIN	SYMBOL	DESCRIPTION
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid.
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the received buffer register.
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.
17	RRC	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	DRR	A low level on DATA RECEIVED RESET clears the data received output DR to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
21	MR	A high level on MASTER RESET clears PE, FE, OE, and DR to a low level and sets the transmitter output to a high level after 18 clock cycles. MR does not clear the receiver buffer register. **This input must be pulsed at least once after power up.**

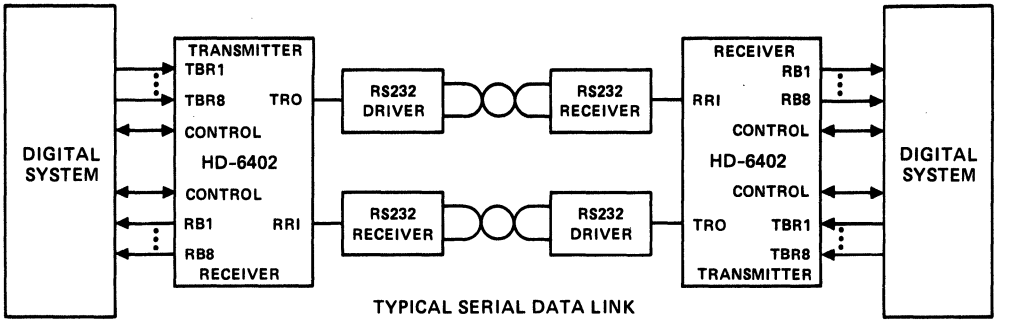


PIN	SYMBOL	DESCRIPTION
22	TBRE	A high level on TRANMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	TBRL	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on TBRL indicates data transfer to the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end.
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
26	TBR1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8 bits the TBR8, 7, and 6 inputs are ignored corresponding to the programmed word length.
27	TBR2	See Pin 26 - TBR1
28	TBR3	See Pin 26 - TBR1

PIN	SYMBOL	DESCRIPTION
29	TBR4	See Pin 26 - TBR1
30	TBR5	See Pin 26 - TBR1
31	TBR6	See Pin 26 - TBR1
32	TBR7	See Pin 26 - TBR1
33	TBR8	See Pin 26 - TBR1
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register.
35	PI	A high level on PARITY INHIBIT inhibits parity generation. Parity checking and forces PE output low.
36	SBS	A high level on STOP BIT SELECT selects 1.5 stop bits for 5 character format and 2 stop bits for other lengths.
37	CLS2	These inputs program the CHARACTER LENGTH SELECTED (CLS1 low CLS2 low 5 bits) (CLS1 high CLS2 low 6 bits) (CLS1 low CLS2 high 7 bits) (CLS1 high CLS2 high 8 bits)
38	CLS1	See Pin 37 - CLS2
39	EPE	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	TRC	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.



The bit rate generator is shown supplying the transmit and receive clocks for the UART.



TYPICAL SERIAL DATA LINK

Switching Waveforms

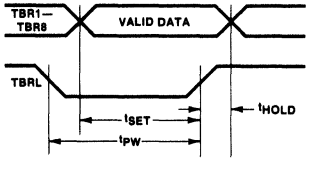


FIGURE 1
Data Input Cycle

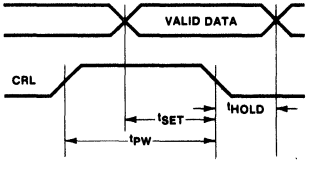


FIGURE 2
Control Register Load Cycle

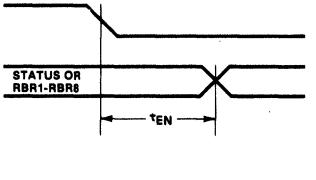


FIGURE 3
Status Flag Output Enable Time or Data Output Enable Time

HARRIS

HD-4702

CMOS PROGRAMMABLE BIT RATE GENERATOR

Features

- HD-4702 – PROVIDES 13 COMMONLY USED BIT RATES
- USES A 2.4576MHz CRYSTAL/INPUT FOR STANDARD FREQUENCY OUTPUT (16 TIMES BIT RATE)
- TTL COMPATIBLE – OUTPUT WILL SINK 1.6mA
- LOW POWER DISSIPATION 4.5mW TYP. @ 2.4576MHz
- CONFORMS TO EIA RS-404
- ONE HD-4702 CONTROLS UP TO EIGHT TRANSMISSION CHANNELS
- INITIALIZATION CIRCUIT FACILITATES DIAGNOSTIC FAULT ISOLATION
- ON-CHIP INPUT PULL-UP CIRCUIT

Description

The HD-4702 Bit Rate Generator provides the necessary clock signals for digital data transmission systems, such as a UART. It generates 13 commonly used bit rates using an on-chip crystal oscillator or an external input. For conventional operation generating 16 output clock pulses per bit period,the input clock frequency must be 2.4576MHz (i.e. 9600 Baud x 16 x 16, since there is an internal ÷16 prescaler). A lower input frequency will result in a proportionally lower output frequency.

The HD-4702 can provide multi-channel operation with a minimum of external logic by having the clock frequency CO and the ÷8 prescaler outputs Q_0, Q_1, Q_2 available externally. All signals have a 50% duty cycle except 1800 Baud, which has less than 0.39% distortion and 3600 Baud, which has less than 0.78% distortion.

The four rate select inputs (S_0-S_3) select which bit rate is at the output (Z). The table lists select code and output bit rate. Two of the 16 for the HD-4702 do not select an internally generated frequency, but select an input into which the user can feed either a different frequency, or a static level (High or Low) to generate "ZERO BAUD".

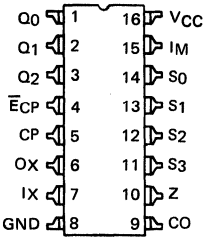
The bit rate most commonly used in modern data terminals (110, 150, 300, 1200, 2400 Baud) require that no more than one input be grounded for the HD-4702, which is easily achieved with a single 5-position switch.

The HD-4702 has an initialization circuit which generates a common master reset for all flip-flops. This signal is derived from a digital differentiator that senses the first high level on the CP input after the $\overline{E}_{CP}$ input goes low. When $\overline{E}_{CP}$ is high, selecting the crystal input, CP must be low. A high level on CP would apply a continuous reset.

For the HD-4702, all inputs except I_X have on-chip pull-up circuits which provide TTL compatibility and eliminate the need to tie a permanently high input to V_{CC}.

Pinout

TOP VIEW



PIN NAMES

$\overline{CP}$	External Clock Input
$\overline{E}_{CP}$	External Clock Enable Input (Active Low)
I_X	Crystal Input
I_M	Multiplexed Input
S_0 - S_3	Rate Select Inputs
CO	Clock Output
O_X	Crystal Drive Output
Q_0 - Q_2	Scan Counter Outputs
Z	Bit Rate Output

Truth Tables

TABLE 1
CLOCK MODES AND INITIALIZATION

I_X	E_{CP}	CP	OPERATION
⎍⎍	H	L	Clocked from I_X
X	L	⎍⎍	Clocked from CP
X	H	H	Continuous Reset
X	L	⎍	Reset During 1st CP = HIGH Time

NOTE: Actual output frequency is 16 times the indicated Output Rate, assuming a clock frequency of 2.4576MHz.

H = HIGH Level
L = LOW Level
X = Don't care
⎍ = 1st HIGH Level Clock Pulse after E_{CP} goes LOW
⎍⎍ = Clock Pulse

TABLE 2
TRUTH TABLE FOR RATE SELECT INPUTS

S_3 S_2 S_1 S_0	OUTPUT RATE (Z)
L L L L	MUX INPUT (I_M) ①
L L L H	MUX INPUT (I_M)
L L H L	50 BAUD
L L H H	75 BAUD
L H L L	134.5 BAUD
L H L H	200 BAUD
L H H L	600 BAUD
L H H H	2400 BAUD
H L L L	9600 BAUD
H L L H	4800 BAUD
H L H L	1800 BAUD
H L H H	1200 BAUD
H H L L	2400 BAUD
H H L H	300 BAUD
H H H L	150 BAUD
H H H H	110 BAUD

NOTE:
① 19200 BAUD by connecting Q_2 to I_M.

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		+8.0V
Input or Output Voltage Applied		(GND -0.3V) to (V_{CC} +0.3V)
Storage Temperature Range		-65°C to +150°C
Operating Temperature Range		
Industrial	HD-4702-9	-40°C to +85°C
Military	HD-4702-2/8	-55°C to +125°C
Operating Voltage Range		+4 to +7V

ELECTRICAL CHARACTERISTICS

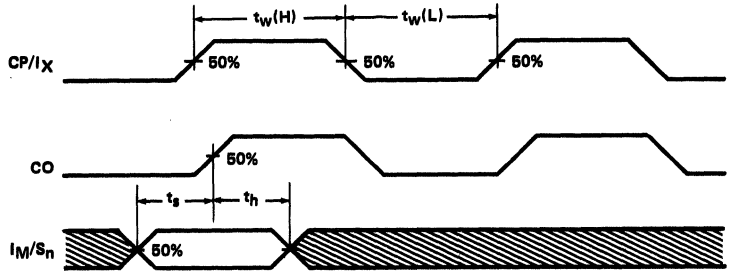
D.C.: V_{CC} = 5V ± 10%; T_A = Industrial or Military.
A.C.: V_{CC} = 5V; T_A = 25°C.

	SYMBOL	PARAMETER	HD-4702-2 MIN	HD-4702-2 TYP	HD-4702-2 MAX	HD-4702-9 MIN	HD-4702-9 TYP	HD-4702-9 MAX	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Input High Voltage	V_{CC} 70%			V_{CC} 70%			V	
	V_{IL}	Input Low Voltage			V_{CC} 30%			V_{CC} 30%	V	
	V_{OH1}	Output High Voltage	V_{CC} -.05			V_{CC} -.05			V	$I_{OH} \leq -1\mu A$
	V_{OL1}	Output Low Voltage			0.05			0.05	V	$I_{OL} \leq +1\mu A$
	I_{IH}	Input High Current	-1		+1	-1		+1	μA	$V_I = V_{CC}$, All other pins = 0V
	I_{IL}	INPUT ① (all other inputs) LOW		-30	-100		-30	-100	μA	
	I_{ILX}	CURRENT (I_X inputs)	-1		+1	-1		+1	μA	V_I = 0, All other pins = V_{CC}
	I_{OHX}	OUTPUT (O_X)	-0.1			-0.1			mA	$V_{OUT} = V_{CC}$ -.5
	I_{OH1}	HIGH (all other outputs)	-1.0			-1.0			mA	V_{OUT} = 2.5V
	I_{OH2}	CURRENT (all other outputs)	-0.3			-0.3			mA	$V_{OUT} = V_{CC}$ -.5
										Input at 0 or V_{CC} per Logic Function or Truth Table
	I_{OLX}	OUTPUT (O_X) LOW	0.1			0.1			mA	V_{OUT} = .4V
	I_{OL}	CURRENT (all other outputs)	1.6			1.6			mA	V_{OUT} = .4V
	I_{CC}	SUPPLY ① CURRENT (STATIC)			1500 1000			1500 1000	μA μA	$\overline{E}_{CP} = V_{CC}$, CP = 0, All other inputs = GND $\overline{E}_{CP} = V_{CC}$, CP = 0, All other inputs = V_{CC}
A.C.	t_{PLH} t_{PHL}	Propagation Delay, I_X to CO			300 250			300 250	ns ns	$C_L \leq$ 7pF on O_X ②
	t_{PLH} t_{PHL}	Propagation Delay, CP to CO			215 195			215 195	ns ns	C_L = 15pF, Input Transition Times ≤ 20ns
	t_{PLH} t_{PHL}	Propagation Delay, CO to Q_n			⑤			⑤	ns ns	
	t_{PLH} t_{PHL}	Propagation Delay, CO to Z			75 65			75 65	ns ns	
	t_{TLH} t_{THL}	Output Transition Time (except OX)			80 40			80 40	ns ns	
	t_{PLH} t_{PHL}	Propagation Delay, I_X to CO			350 275			350 275	ns ns	$C_L \leq$ 7pF on O_X ②
	t_{PLH} t_{PHL}	Propagation Delay, CP to CO			260 220			260 220	ns ns	C_L = 50pF, Input Transition Times ≤ 20ns
	t_{PLH} t_{PHL}	Propagation Delay, CO to Q_n			⑤			⑤	ns ns	
	t_{PLH} t_{PHL}	Propagation Delay, CO to Z			85 75			85 75	ns ns	
	t_{TLH} t_{THL}	Output Transition Time (except OX)			160 75			160 75	ns ns	
	t_s t_h	Set-Up Time, Select to CO Hold Time, Select to CO	350 0			350 0			ns ns	$C_L \leq$ 7pF on O_X ②
	t_s t_h	Set-Up Time, I_M to CO Hold Time, I_M to CO	350 0			350 0			ns ns	C_L = 15pF, Input Transition Times ≤ 20ns
	$t_{WCP(L)}$ $t_{WCP(H)}$	Minimum Clock Pulse-Width Low and High ③ ④	120 120			120 120			ns ns	
	$t_{WCP(L)}$ $t_{WCP(H)}$	Minimum I_X Pulse Width, Low and High ④	160 160			160 160			ns ns	

NOTES:

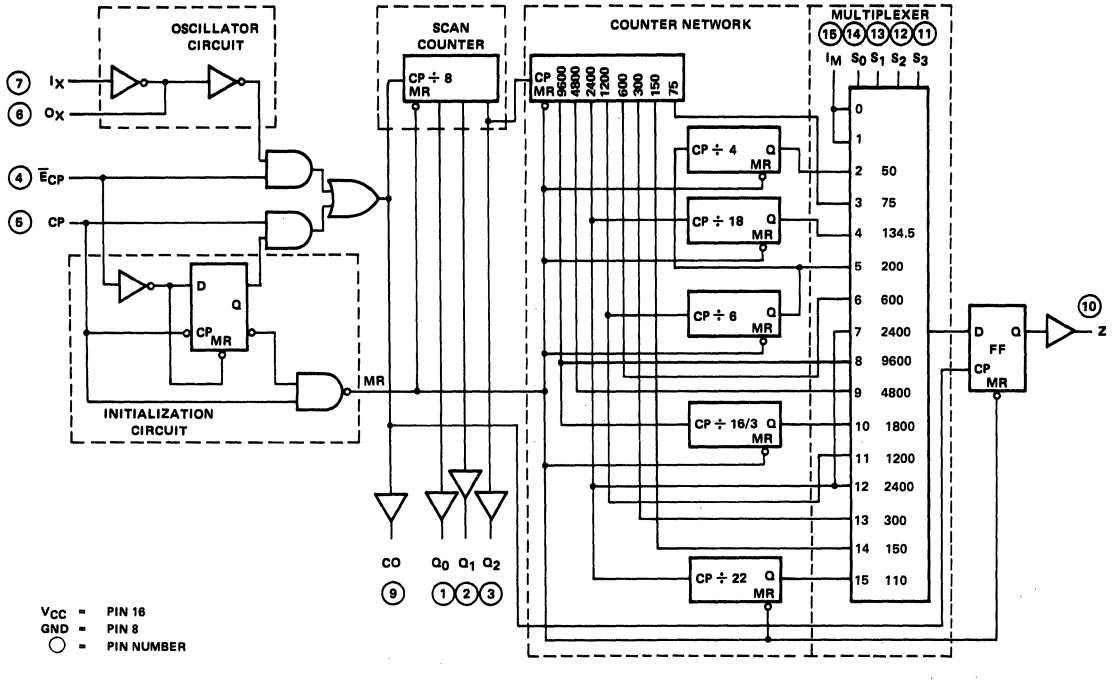
① Input Current and Quiescent Power Supply Current are relatively higher for this device because of active pull-up circuits on all inputs except I_X. This is done for TTL compatibility.
② Propagation Delays (t_{PLH} and t_{PHL}) and Output Transistion Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-Up Times (t_s), Hold Times (t_h), and Mininum Pulse Widths (t_W) do not vary with load capacitance.
③ The first High Level Clock Pulse after $\overline{E}_{CP}$ goes Low and must be at least 350ns long to guarantee reset of all Counters.
④ It is recommended that input rise and fall times to the Clock Inputs (CP, I_X) be less than 15μs.
⑤ For multichannel operation, Propagation Delay (CO to Q_n) plus Set-Up Time, Select to CO, is guaranteed to be ≤ 367ns.

Switching Waveforms



NOTE: Set-Up and Hold Times are shown as positive values but may be specified as negative values.

Block Diagram



SINGLE CHANNEL BIT RATE GENERATOR

Figure 1 shows the simplest application of the HD-4702. This circuit generates one of five possible bit rates as determined by the setting of a single pole, 5-position switch. The Bit Rate Output (Z) drives one standard TTL load or four low power Schottky loads over the full temperature range. The possible output frequencies correspond to 110, 150, 300, 1200, and 2400 or 3600 Baud. For many low cost terminals, these five bit rates are adequate.

SIMULTANEOUS GENERATION OF SEVERAL BIT RATES

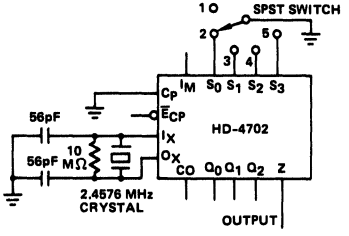
Figure 2 shows a simple scheme that generates eight bit rates on eight output lines, using one HD-4702 and one 93L34 Bit Addressable Latch. This and the following applications take advantage of the built-in scan counter (prescaler) outputs, As shown in the block diagram, these outputs (Q_0 to Q_2) go through a complete sequence of eight states for every half-period of the highest output frequency (9600 Baud). Feeding these Scan Counter Outputs back to the Select Inputs of the multiplexer causes the HD-4702 to interrogate sequentially the state of eight different frequency signals. The 93L34 8 Bit Addressable Latch, addressed by the same Scan Counter Outputs, re-converts the multiplexed single Output (Z) of the HD-4702 into eight parallel output frequency signals. In the simple scheme of Figure 2, input S_3 is left open (HIGH) and the following bit rates are generated:

Q_0: 110 Baud Q_1: 9600 Baud Q_2: 4800 Baud
Q_3: 1800 Baud Q_4: 1200 Baud Q_5: 2400 Baud
Q_6: 300 Baud Q_7: 150 Baud

Other bit rate combinations can be generated by changing the Scan Counter to Selector interconnection or by inserting logic gates into this path.

19200 BAUD OPERATION

Though a 19200 Baud signal is not internally routed to the multiplexer, the HD-4702 can be used to generate this bit rate by connecting the Q_2 output to the I_M input and applying select code. An additional 2-input NOR gate can be used to retain the "Zero Baud" feature on select code 1 for the HD-4702 (See Figure 3).



SWITCH POSITION	HD-4702 BIT RATE
1	110 Baud
2	150 Baud
3	300 Baud
4	1200 Baud
5	2400 Baud

FIGURE 1
Switch selectable bit rate generator configuration providing five bit rates.

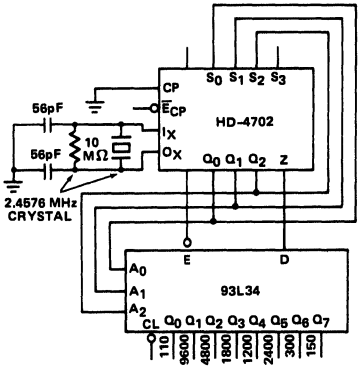


FIGURE 2
Bit rate generator configuration with eight simultaneous frequencies

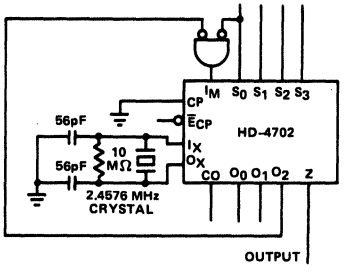


FIGURE 3
19200 Baud Operation

TABLE 3
CRYSTAL SPECIFICATIONS

PARAMETERS	TYPICAL CRYSTAL SPEC
Frequency	2.4576 MHz "AT" Cut
Series Resistance (Max)	250
Unwanted Modes	-6.0dB (Min)
Type of Operation	Parallel
Load Capacitance	32pF +0.5

CMOS

Harris Reliability and Quality

6

Introduction	6-2
Quality Control	6-2
Quality Assurance	6-4
Reliability	6-4
Harris SAJI Process Overview	6-8
CMOS Design Considerations	6-10

Harris Reliability & Quality

Introduction

The Product Assurance Department at Harris Semiconductor Products Group is responsible for assuring that the quality and reliability of all products shipped to customers meet their requirements. During all phases of product fabrication, there are many independent visual and electrical checks performed by Product Assurance personnel.

Prior to shipment, a final inspection is performed at Quality Assurance Plant Clearance to insure that all requirements of the purchase order and customer specifications are met.

The following military documents provide the foundation for HARRIS Product Assurance Program.

MIL-M-38510D	"General Specification of Microcircuits"
MIL-Q-9858A	"Quality Program Requirements"
MIL-STD-883B	"Test Methods and Procedures for Microelectronics"
NASA Publication 200-3	"Inspection System Provisions"
MIL-C-45662A	"Calibration System Requirements"
MIL-I-4508A	"Inspection System Requirements"

The Harris Semiconductor Reliability and Quality Manual, which is available upon request, describes the total function and policies of the organization to assure product reliability and quality. All customers are encouraged to visit the Harris Semiconductor facilities and survey the deployment of the Product Assurance function.

Quality Control

The Quality Control Department consists of Process Control with Chemical Mix as an available supporting service.

Process Quality Control is responsible for quality engineering and controls in the wafer processing modules, assembly, mask and materials production areas, and electrical wafer probe.

The primary responsibilities of Process Quality Control are:

a. To establish and maintain effective controls for monitoring manufacturing processes and equipment

b. to provide rapid feedback of information concerning the state of control

c. to initiate, design, and develop statistically controlled experiments to further improve product reliability and quality levels.

Statistical control charts on processes and operating procedures are used in the manufacturing areas and in the evaluation of process and product parameters utilized to qualify new processes.

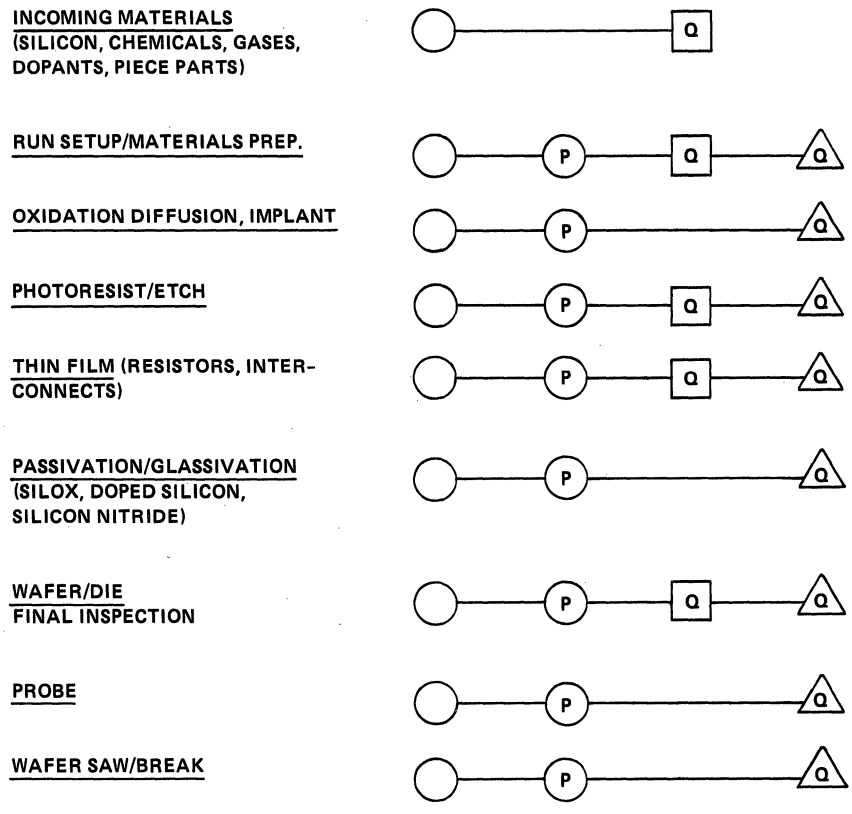
When necessary, fixed gate inspections are permanently employed to assure specified quality levels.

On a regular basis, process audits are performed to verify conformance to operating procedures.

Statistical control charts are maintained on processes and workmanship for all phases of assembly and environmental testing.

PROCESS CONTROL

WAFER FABRICATION - GENERAL PROCESS FLOW



Quality Assurance

The primary responsibility of the Quality Assurance Department is to assure that all delivered products meet the rigid standard of reliability and quality of Harris Semiconductor Products Group. The Quality Assurance department is responsible for process control and product quality from product test to shipment. Random sampling of products at specified points and intervals is used to ensure quality. This includes performance and analysis of sample electrical testing (Group A) and environmental and life testing (Groups B, C and D). In addition, mechanical and visual inspections specified by the Quality Assurance Test Plans, as well as customer and military specifications are performed. The random selection and distribution of samples, the routing of devices through specified testing and adherence to inspection programs are controlled and implemented by Quality Assurance.

All packaged microcircuits are marked by a code indicating the date the lot was sealed. This code provides product traceability and meets customer date coding requirements. Traceability is maintained through lot acceptance, testing and shipment to the customer.

Reliability

RELIABILITY PROCEDURES

Harris Semiconductor Products Group employs a comprehensive approach to reliability evaluation to ensure that reliability is designed and built into all products. This approach is referred to as the Reliability Evaluation Procedures and outlines the basic guidelines for evaluation of the total inherent reliability capability of all products types. The Reliability Evaluation Procedures are applied as an overlay during the early product development phase, subsequent prove-in via preproduction and final maturity in the manufacturing of all new product types. They also provide guidelines for evaluation of new process technologies deployed in all applicable products. The Reliability Evaluation Procedures also encompass a package qualification procedure, and the "Add-on" program which is a quarterly reliability monitor of all process groups. These documents are available upon request. The following test matrix (Table 1) outlines the minimum requirements necessary for product qualification.

TABLE 1. TEST MATRIX

Design Package Process	New New New	New New Est.	New Exist New	New Exist Est.	Exist New New	Exist New Est.	Exist Exist New	Exist Exist Est.
Abuse Tests 20 Units	X	X	X	X	X		X	X
Max. Ratings 20 Units: No Failures	X		X	X	X		X	X
86/86 or Autoclave 50 Units: No Failures	X	X	X		X	X	X	
Constr. Analysis 5 Units: No Failures	X	X	X	X	X	X	X	X
Centrifuge 50 Units: No Failures	X	X			X	X		
Ele. Charac. 20 Units: No Failures	X	X	X	X	X		X	X
ESD Immunity 20 Units: No Failures	X	X	X	X	X		X	X
Fig. Test 20 Units: No Failures	X	X	X	X	X		X	
HTOL Sample Groups	200 (min)	200 (min)	200 (min)	200 (min)	200 (min)	200 (min)	200 (min)	200 (min)
Latch-up 20 Units: No Failures	X	X	X	X	X			
Lead Integrity 20 Units: No Failures	X	X			X	X	X	X
Mech. Charac. 20 Units: No Failures	X	X			X	X		
Mech. Schock 50 Units: No Failures	X	X			X	X		
Moisture Resist 50 Units: No Failures	X	X			X	X		
Oja/Ojc 20 Units	X	X			X	X		
Solvent Resistance 4 Units: No Failures	X	X			X	X		
Solderability 20 Units: No Failures	X	X			X	X		
Temperature Cycling 50 Units: No Failures	X	X			X	X		
Thermal Shock 50 Units: No Failures	X	X			X	X		
Vibration 50 Units: No Failures	X	X			X	X		

The HARRIS CMOS product line has had a continual evolution of new and enhanced processes. From SAJI I (Self Aligned Junction Isolated) to the most recent SAJI V process. There has been an ongoing effort to increase performance, density and reliability. The current RAM products (4K and up) along with the microprocessors and peripheral families utilize the SAJI IV, scaled SAJI IV, and SAJI V processes. Table II is a summary of recent reliability data taken on the various SAJI processes. Table III lists the activation energies of the most common defects associated with the CMOS products. Table IV gives a breakdown of field returns by failure mechanism.

At Harris, accelerated life Tests are utilized to estimate the field failure rate of our product. A typical life test consists of 200 devices tested at +125°C to +150°C ambient, dynamic operation, 5.5V to 6.5V, for 1000 hours. All failures are carefully analyzed to determine the failure mechanism and associated activation energy (EA) utilizing the arrehnius equation derating factors back to +55°C ambient, 5.5volts operation are determined.

Derating factor = $D.F. = e^{-\left(\frac{E_A}{K}\right)\left(\frac{1}{T_2} - \frac{1}{T_1}\right)}$ where E_A = Activation Energy
K = Boltzman's Constant
T_2 = Life Test Junction Temp.
T_1 = Junction Temp. at +55°C Ambient

Projected field failure rates are calculated at 60% and 95% confidence levels. This means that either 60% or 95% of the product will meet or exceed the reliability demonstrated in the test. We also ensure that the failure rate is decreasing with time to prevent any wear-out mechanism from reaching our customers.

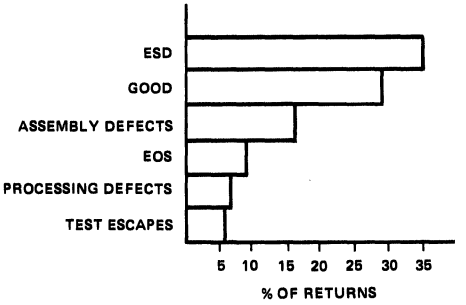
TABLE II. SUMMARY OF RELIABILITY DATA

SAJI Process Type	No. of Devices	Device Hours (+125°C)	No. of Failures	E_A (ev)	Failure Rate (%/K Hours) @ T_A = +55°C		
					Observed	60% Confidence	95% Confidence
I	2,046	4,019,046	1 4 6	1.0ev .6 ev .5ev	.0007	.001	.002
II	1,515	1,791,668	2 1 2 2	1.0ev .7ev .6ev .5ev	.004	.013	.028
III	440	938,844	0	–	.002	.005	.015
IV	687	740,464	1 2	.6ev .5ev	.020	.025	.044
Scaled IV	1740	3,387,860	21 2 3 6	1.0ev .7ev .6ev .5ev	.012	.015	.025

TABLE III CMOS PRODUCTS - ACTIVATION ENERGY

Failure Mechanism	Activation Energy (E_A)
Oxide Defects	0.5ev
Defective Apertures	0.6ev
Photoresist Flaws	0.7ev
Assembly Defects	0.8ev
Ionic Contamination	1.0ev

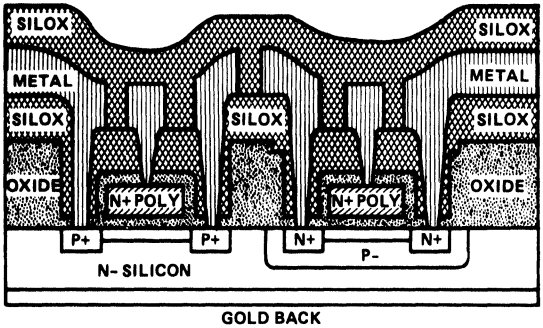
TABLE IV. FIELD RETURNS BY FAILURE MECHANISM



NOTE: Returned units are approximately 1% of the total shipped.

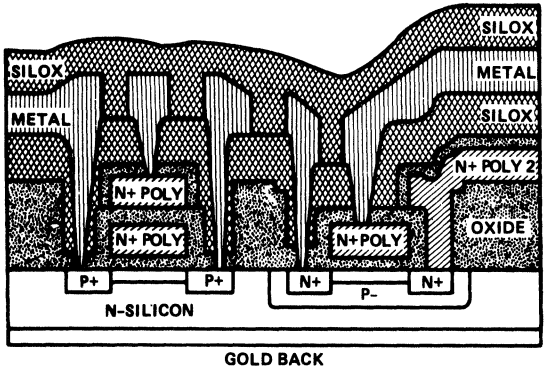
Harris SAJI Process Overview

SAJI I - Self Aligned Junction Isolation



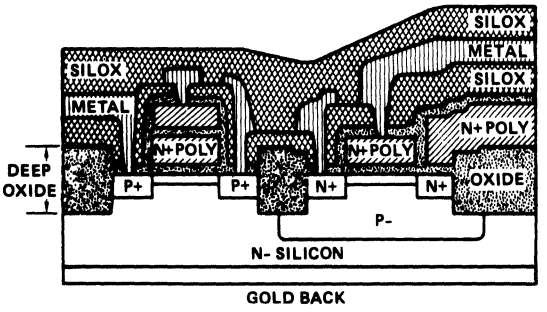
In 1972 Harris Semiconductor began development of a SAJI CMOS process that would become the basis for all Harris CMOS devices. In 1973, Harris perfected the SAJI I process and proved its potential for high speed, low power and high packing density. By 1975, the SAJI I process had proved to be successful in volume production of high density CMOS components as evidenced by the reliability of the 1K CMOS RAMs. SAJI I utilizes a single level of polysilicon and a single level of metal interconnect.

SAJI II



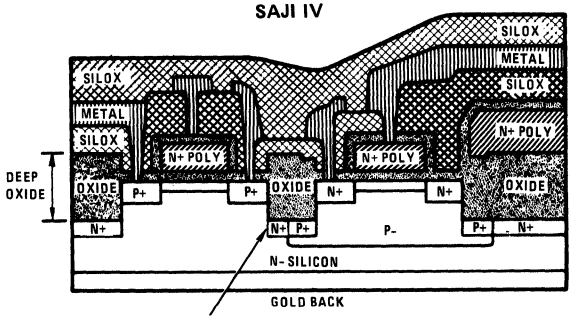
To achieve higher packing density, SAJI II was implemented in the 4K CMOS RAMs in 1978. SAJI II represents the evolution of SAJI processes into a second generation, incorporating smaller (scaled) devices and a second level of polysilicon interconnect, labeled N + POLY 2. Buried contacts allow the interface of multiple interconnect levels. This process relies upon the thick oxide for device isolation and guardbanding.

SAJI III



In 1980, SAJI III was introduced with the redesigned (2nd generation) 4K CMOS RAMs. SAJI III advances include device scaling for increased packing density and die size reductions, and selective oxidation processing, which exhibits more planar device surface structures improving step coverage and device reliability. The selective oxidation process involves the deposition of a nitride layer in the gate region of each device. This nitride layer prohibits the growth of oxide in the gate region. As a result, thick oxide is not grown across the entire face of the die but only in areas not inhibited by the nitride layer. Thick oxide growth now occurs between devices and below the surface of the die. The lower inherent capacitance in the gate area due to a thinner gate oxide results in increased device speed. Previous SAJI processes are easily retrofitted to this process.

SAJI IV



The next generation process was SAJI IV. SAJI IV features the selection oxidation and planar surface characteristics of SAJI III while adding further device scaling with the option of high resistivity substrates which reduces internal junction capacitances and increases speed. Self-aligned implanted P+ and N+ guardbands were also added, which increased the isolation between devices and reduced adjacent device interaction and increased packing density.

CMOS Design Considerations

ESD (ELECTROSTATIC DISCHARGE)

Since the introduction of MOS, manufacturers have searched for effective and safe ways of handling this voltage sensitive device. High input impedance of CMOS, coupled with gate-oxide breakdown characteristics, result in susceptibility to electrostatic charge damage.

Figure 2 shows a cross-section of a silicon gate MOS structure. Note the very thin oxide layer (≈500-1000Å) present under the gate material. Actual breakdown voltage for this insulating layer ranges from 70V to 100V.

Handling equipment and personnel, by simply moving, can generate in excess of 10kV of static potential in a low humidity environment. Thus, static voltages, in magnitudes sufficient to damage delicate MOS input gate structures, are generated in most handling environments.

A failure occurs when a voltage of sufficient magnitude is applied across the gate oxide causing it to breakdown and destruct. Molten material then flows into the void creating a short from the gate to the underlying silicon. Such shorts occur either at a discontinuity in doping concentration, or at a defect site in the thin oxide. If no problems appear in the oxide, breakdown would most likely occur at gate/source, or gate/drain intersection coincidence due to the doping concentration gradient.

Noncatastrophic degradation may result due to overstressing a CMOS input. Sometimes an input may be damaged, but not shorted. Most of these failures relate to damage of the protection network, not the gate, and show up as increased input leakage.

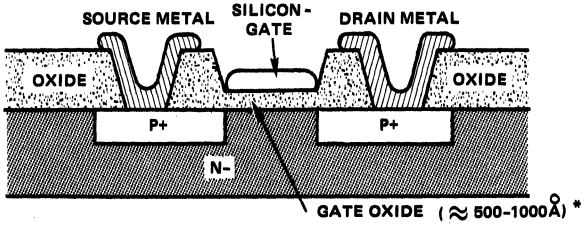


Figure 2 — Silicon-gate PFET structure cross-section shows the heavily doped source and drain region. They are separated by a narrow gap over which lies a thin-gate oxide and gate material.

*NOTE: 1Å (Angstrom = 10^{-8} cm)

Voltage Limiting Input Protection

During the evolution of monolithic MOS, manufacturers developed various protection mechanisms that are an integral part of the circuit. However, several of these earlier techniques have been replaced by improved methods now in use. The object of most of these schemes is to prevent damage to input-gate structures by limiting applied voltages.

Recent CMOS designs employ a dual-diode concept in their input protection networks. Figure 3 illustrates such a protection circuit.

One characteristic of junction-isolated CMOS protection circuits is the ≈ 200Ω current limiting resistor. Cross sectional area of the metallization leading to the resistor, and the area of the resistor are, therefore, designed to absorb discharge energy without sustaining permanent damage. This dual-diode protection has proved very effective and is the most commonly used method in production today.

HARRIS INPUT GATE PROTECTION

To protect input device gates against destructive overstress by static electricity accumulating during handling and insertion of CMOS products, Harris provides a protection circuit on all inputs. The general configuration of this protection circuit is shown in Figure 3.

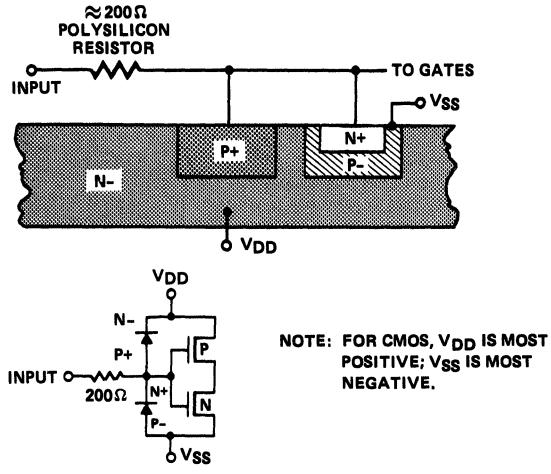


Figure 3 — Junction isolated dual-diode protection networks are most commonly used in today's CMOS circuits.

Both diodes to the V_{DD} and V_{SS} lines have breakdown voltages averaging between 35 and 40 volts. Excessive static charge accumulated on the input pin is thus effectively discharged through these diodes which limit the voltage applied from gate to drain and source. The 200 ohm resistor provides current limiting during discharge. Depending on the polarity of the input static charge and on which of the supply pins are grounded, the protective diodes may either conduct in the forward direction or breakdown in the reverse direction.

In order to test this concept, step stress tests have been performed at Harris using an approximate equivalent circuit to simulate the static charge encountered in handling operations. The equivalent circuit consists of a 100pF capacitor in series with a 1.5K ohm resistor and is considered the rough equivalent of a human body. Step stressing takes the form of charging the capacitor to a given voltage and then discharging it into an input pin of the CMOS device under test according to the sequence given in MIL-M-38510.

Stress Voltage	Cumulative Failures
500	0
700	0
1000	0
1400	1
1600	3
1800	4

These results indicate that the input protection used for Harris CMOS products provides adequate protection against static electricity based on the limits specified in MIL-M-38510.

There are two trade-offs to consider when fabricating an input protection scheme, namely effectiveness of the overvoltage protection and performance of the overall circuit. It is obvious that increasing the series resistance and capacitance at an input limits current and this, in turn, increases the input protection's ability to absorb the shock of a static discharge. However, such an approach to protection can have a significant effect on circuit speed and input leakage. The input protection selected must therefore provide a useful performance level and adequate static-charge protection.

Commonly used MOS-input protection circuits all have basic characteristics that limit their effectiveness. The zener diodes, or forward-biased pn-junctions, employed have finite turn-on times too long to be effective for fast rise-time conditions. A static discharge of 1.5kV into a MOS input may bring the gate past its breakdown level before the protection diodes or zener becomes conductive.

Actual turn-on times of zeners and pn-diodes are difficult to determine. It is estimated that they are a few nanoseconds and a few tens of picoseconds, respectively. A low-impedance static source can easily produce rise times equal to or faster than these turn-on times. Obviously the input time constant required to delay buildup of voltage at the gate must be much higher for zener diodes or other schemes having longer turn-on times.

Consider an example. Figure 4 shows a test circuit that simulates the discharge of a 1.5kV static charge into a CMOS input. Body capacitance and resistance of the average person is represented by a 100pF capacitor through 1.5kΩ . Switch A is initially closed, charging 100pF to 1.5kV with switch B open. Switch A is opened, then B is closed, starting the discharge. With the 1.5KΩ x 5pF time constant to limit the charge rate at the DUT input, it would take approximately 350psec to charge to 70V above V_{DD}. Diode turn-on time is much shorter than 350psec, hence the gate node would be clamped before any damage could be sustained.

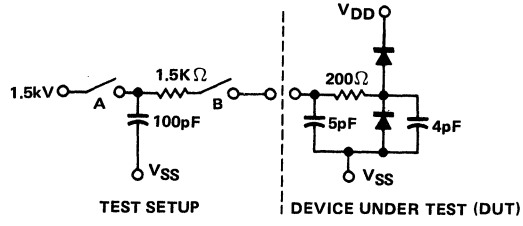


Figure 4 — Input protection network test setup illustrates how diode clamping prevents excessive voltages from damaging the CMOS device.

HANDLING RULES

There is no completely foolproof system of chip-input protection presently in production. If static discharge is of high enough magnitude, or of sufficiently short rise-time, some damage or degradation may occur. It is evident, therefore, that proper handling procedures should be adopted at all times.

Elimination or reduction of static charge can be accomplished as follows:

- Use conductive work stations. Metallic or conductive plastic tops on work benches connected to ground help eliminate static build-up.
- Ground all handling equipment.
- Ground all handling personnel with a conductive bracelet through 1MΩ to ground.
- The 1MΩ resistor will prevent injury.
- Smocks, clothing, and especially shoes of certain insulating materials (notably nylon) should not be worn in areas where devices are handled. These materials, highly dielectric in nature, will hold or aid in the generation of a static charge.
- Control relative humidity to as high a level as practical. A higher level of humidity helps bleed away any static charge as it collects.
- Ionized air blowers reduce charge build-up in areas where grounding is not possible or desirable.
- Devices should be in antistatic conductive carriers during all phases of transport. If antistatic carriers are used the devices and carriers should be in a static shielding bag.
- In automated handling equipment, the belts, chutes or other surfaces the leads contact should be of a conducting nature. If this is not possible, ionized air blowers may be a good alternative.

Harris currently ships all CMOS products in Benstat ™ tubes placed inside static shielding bags. Packing materials are all antistatic.

THE FORWARD-BIAS PHENOMENON

Monolithic CMOS integrated circuits employ a single-crystal silicon wafer into which FET sources and drains are implanted. For complex functions many thousands of transistors may be required and each must be electrically isolated for proper operation.

Junction techniques are commonly used to provide the required isolation – each switching node operating reverse-biased to its respective substrate material. Additionally, as previously mentioned, protection diodes are provided to prevent static-charge related damage where inputs interface to package pins. Forward-biasing any of these junctions with or without power applied may result in malfunction, parametric degradation, or damage to the circuit.

High currents resulting from an excessive forward-bias can cause severe overheating localized to the area of a junction. Damage to the silicon, overlying oxide and metallization can result.

BIPOLAR PARASITICS

Care must always be exercised not to forward-bias junctions from input or output pads.

A complex and potential defect phenomenon is the interaction of a npn/pnp combination a la SCR (Figure 5). Forward-biasing the base-emitter junction of either bipolar component can cause the pair to latch up if βnpn x βpnp ≥ 1. The resultant low impedance between supply pins can cause fusing of metallization or over-dissipation of the chip.

Figure 5 shows how an SCR might be formed. The p+ diffusion labeled INPUT is connected to aluminum metallization and bonded to a package pin. Biasing this point positive with respect to V_{DD} supplies base drive to the pnp through R2. Although gain of these lateral devices is normally very low, sufficient collector current may be generated to forward-bias and supply substantial base current to the vertical npn parasitic. Once the pair has been activated, each member provides the base current required to sustain the other. A latched condition will be maintained until power is removed or circuit damage disables further operation.

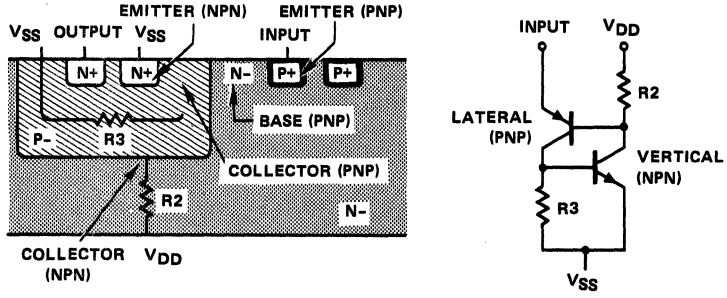


Figure 5 — Improper biasing can latch-up this SCR configuration. A p+ guard ring is commonly used to kill lateral pnp action. This ring is diffused into the surface at the junction of p- and n- silicon.

DESIGN RULES EQUALLY IMPORTANT AS HANDLING RULES

A system using CMOS devices must have reliability designed in. No amount of testing can guarantee long term reliability when poor design practices are evident.

- Never apply signals which exceed maximum ratings to a CMOS circuit before or after power has been turned on (to prevent latch-up)
- Supply filter capacitance should be distributed such that some filtering is in close proximity to the supply pins of each package. Testing has shown 0.01 μF/package to be effective in filtering noise generated by most CMOS functions.
- CMOS signal lines are terminated at the driving end by a relatively high impedance when operating at the low end of the supply voltage range. This high-impedance termination results in vulnerability to high-energy or high-frequency noise generated by bipolar or other non-CMOS components. Such noise must be held down to manageable levels on both CMOS power and signal lines.
- Where CMOS must interface between logic frames or between different equipments, ground differences must be controlled in order to maintain operation within absolute maximum ratings.

- Capacitance on a CMOS input or output will result in a forward-bias condition when power is turned off. This capacitance must discharge through forward-biased input or output to substrate junctions as the bus voltage collapses. Excessive capacitance (thousands of pF) should be avoided as discharging the stored energy may generate excessive current densities during power-down.
- Where forward-biasing is inevitable, current limiting should be provided. Current should not be permitted to exceed 1mA on any package pin excluding supply pins.

All CMOS is susceptible to damage due to electrical overstress. It is the user's responsibility to follow a few simple rules in order to minimize device losses.

First, select a source for the CMOS device that employs an effective input protection scheme. This will allow a greater margin of safety at all levels of device handling since the devices will not be quite so prone to static charge damage. Next, he should apply a sound set of handling and design rules. At minimum, this will eliminate electrical stresing or hold it to manageable levels.

With an effective on-chip protection scheme, good handling procedures and sound design, users should not lose any CMOS devices to electrical overstress.

CMOS

Harris Hi-Rel and Military

7

Introduction	7-3
Advantages of Standard Flows	7-3
Standard Manufacturing Flows	7-3
CMOS Military Product Description	7-4

Harris Hi-Rel and Military Products

Introduction

High reliability, the Military and Harris Semiconductor have enjoyed a cooperative relationship for more than a decade. Over ten years ago, Harris was the first to manufacture and, subsequently, JAN-qualify bipolar PROMS. Harris currently has government certified manufacturing lines producing a variety of high-rel products.

Early commitment to CMOS technology has made Harris the premier manufacturer of high performance CMOS VLSI devices. HARRIS fast, low power components are designed to offer significant power reduction, lower operating temperatures, improved reliability, reduced packaging costs and improved performance for extended temperature range applications. For the military/hi-rel market, Harris also has standard CMOS hi-rel grades which accommodate the requirements of virtually all applications.

Advantages of Standard Flows

Wherever feasible, and in accordance with good value engineering practice, it is beneficial to the IC user to specify Hi-Rel device grades based on one of the five standard Harris manufacturing flows. These generally meet or exceed the requirements of the majority of applications.

Advantages gained by basing designs on the standard data book or slash sheet (as applicable) electrical limits and calling out standard as opposed to custom flows include:

- LOWER COST than the same or an equivalent flow executed on a custom basis. This results from the higher efficiency achieved with a constant product flow and the elimination of such extra cost items as special fixturing, test programs, additional handling, and added documentation.
- FASTER DELIVERY since the manufacturer often can supply many items from inventory and, in any case, can establish and maintain a better product flow when there is no need to restructure process and/or test procedures.
- INCREASED CONFIDENCE in the Hi-Rel devices, as a continuing flow of a given Hi-Rel product permits the manufacturer to monitor trends which may influence end-product performance or reliability and to effect necessary corrective action.

Standard Manufacturing Flows

Harris has developed standard flows which should satisfy most requirements. Produced in accordance with established manufacturing flows, the standard Harris Hi-Rel grades and their indicated areas of application are as follows:

- DASH-9+ [PLUS] products are processed to Harris high reliability test conditions and are designed for industrial use. Performance is guaranteed over a temperature range of -40°C to +85°C. For added reliability, devices packaged in ceramic (CERDIP) are burned-in for 160 hours at +125°C, while the burn-in requirement for epoxy packaged parts is 96 hours at +125°C.
- DASH-8 products are designed for general use in the military environment, with performance guaranteed over a temperature range of -55°C to +125°C. Included in Harris DASH-8 processing is 160 hours of burn-in at 125°C.
- DESC drawing parts are manufactured in accordance with drawings provided by the Defense Electronic Supply Center which call out full military screening and lot acceptance testing requirements.

CMOS MICROPROCESSOR AND SUPPORT CIRCUITS

MILITARY PART NUMBER	FUNCTION	PIN COUNT	PAGE REF
8/16-BIT MICROPROCESSORS			
MD80C86/B	16 BIT CMOS MICROPROCESSOR (5MHz)	40	3-4
MD80C86-2/B	16 BIT CMOS MICROPROCESSOR (8MHz)	40	3-4
MD80C88/B	8 BIT CMOS MICROPROCESSOR (5MHz)	40	3-96
MD80C88-2/B	8 BIT CMOS MICROPROCESSOR (8MHz)	40	3-96
80C86/88 PERIPHERAL CIRCUITS			
MD82C52/B	CMOS SERIAL COMMUNICATION INTERFACE	28	3-27
MD82C54/B	CMOS PROGRAMMABLE INTERVAL TIMER	24	3-28
MD82C55A/B	CMOS PROGRAMMABLE PERIPHERAL INTERFACE	40	3-43
MD82C59A/B	CMOS PRIORITY INTERRUPT CONTROLLER	28	3-62
MD82C37A/B	CMOS DMA CONTROLLER	40	3-97
80C86/88 BUS SUPPORT CIRCUITS			
MD82C82/B	CMOS OCTAL LATCHING BUS DRIVER	20	3-77
MD82C83/B	CMOS OCTAL LATCHING INVERTING BUS DRIVER	20	3-98
MD82C84A/B	CMOS CLOCK GENERATOR/DRIVER	18	3-82
MD82C86/B	CMOS OCTAL BUS TRANSCEIVER	20	3-100
MD82C87/B	CMOS OCTAL INVERTING BUS TRANSCEIVER	20	3-101
MD82C88/B	CMOS BUS CONTROLLER	20	3-89
MD82C89/B	CMOS BUS ARBITER	20	3-102
12-BIT MICROPROCESSORS			
HM-6100-8	CMOS 12 BIT MICROPROCESSOR	40	4-30
HD-6120-8	CMOS HIGH PERFORMANCE 12 BIT MICRO	40	4-3
12-BIT PERIPHERAL CONTROLLERS			
HD-6101-8	CMOS PARALLEL INTERFACE ELEMENT (PIE)	40	4-51
HD-6121-8	CMOS I/O CONTROLLER (IOC)	40	4-22
BUS SUPPORT CIRCUITS			
HD-6431-8	CMOS HEX LATCHING BUS DRIVER	16	4-59
HD-6432-8	CMOS HEX BIDIRECTIONAL BUS DRIVER	18	4-62
HD-6433-8	CMOS QUAD BUS SEPARATOR/DRIVER	16	4-65
HD-6434-8	CMOS OCTAL LATCH BUS DRIVER W/RESET	24	4-68
HD-6436-8	CMOS OCTAL BUS BUFFER/DRIVER	20	4-71
HD-6440-8	CMOS LATCHED 3 TO 8 LINE DECODER/DRIVER	18	4-74
HD-6495-8	CMOS HEX BUS DRIVER	16	4-78
SERIAL COMMUNICATION CIRCUITS			
HD-4702-8	CMOS BIT RATE GENERATOR	16	5-56
HD-6402-8	CMOS UART	40	5-51
HD-6406-8	CMOS PROG. ASYNC. COMMUNICATION INTERFACE	40	5-39
HD-6409-8	CMOS MANCHESTER ENCODER-DECODER	20	5-30
HD-15530-8	CMOS MANCHESTER ENCODER-DECODER	24	5-3
HS-15530RH	CMOS MANCHESTER ENCODER-DECODER (RADIATION RESISTANT)	24	9-17
HD-15531-8	CMOS MANCHESTER ENCODER-DECODER	40	5-10
HD-15531B-8	CMOS MANCHESTER ENCODER-DECODER	40	5-10
HS-3182	CMOS ARINC 429 BUS INTERFACE LINE DRIVER CIRCUIT	16	9-28
HS-3282	CMOS ARINC 429 BUS INTERFACE CIRCUIT	40	9-29

CMOS STATIC RAMS

MILITARY PART NUMBER	CONFIG-URATION	PIN COUNT	ACCESS TIME	STANDBY CURRENT-ICCSB	DATA RET. CURRENT-ICCDR	OPERATING CURRENT-ICCOP	PAGE REF
1K - SYNCHRONOUS							
HM-6508-8	1K x 1	16	250ns	10μA	10μA	4mA/MHz	2-5
HM-6508B-8	1K x 1	16	180ns	10μA	5μA	4mA/MHz	2-5
HM-6518-8	1K x 1	18	250ns	10μA	10μA	4mA/MHz	2-11
HM-6518B-8	1K x 1	18	180ns	10μA	5μA	4mA/MHz	2-11
HM-6551-8	256 x 4	22	300ns	10μA	10μA	4mA/MHz	2-17
HM-6551B-8	256 x 4	22	220ns	10μA	10μA	4mA/MHz	2-17
HM-6561-8	256 x 4	18	300ns	10μA	10μA	4mA/MHz	2-25
HM-6561B-8	256 x 4	18	220ns	10μA	10μA	4mA/MHz	2-25
4K - SYNCHRONOUS							
HM-6504-8	4K x 1	18	300ns	50μA	25μA	7mA/MHz	2-29
HM-6504B-8	4K x 1	18	200ns	50μA	25μA	7mA/MHz	2-29
HM-6504S-8	4K x 1	18	120ns	50μA	25μA	7mA/MHz	2-29
HM-6514-8	1K x 4	18	300ns	50μA	25μA	7mA/MHz	2-40
HM-6514B-8	1K x 4	18	200ns	50μA	25μA	7mA/MHz	2-40
HM-6514S-8	1K x 4	18	120ns	50μA	25μA	7mA/MHz	2-40
16K - SYNCHRONOUS							
HM-6516-8	2K x 8	24	200ns	100μA	50μA	10mA/MHz	2-51
HM-6516B-8	2K x 8	24	120ns	50μA	25μA	10mA/MHz	2-51
16K - ASYNCHRONOUS							
HM-65162-8	2K x 8	24	90ns	100μA	40μA	70mA	2-57
HM-65162B-8	2K x 8	24	70ns	50μA	20μA	70mA	2-57
HM-65172-8	2K x 8	24	90ns	100μA	40μA	70mA	2-70
HM-65172B-8	2K x 8	24	70ns	50μA	20μA	70mA	2-70
CMOS RAM MODULES							
HM-6564-8	64K	40	350ns	800μA	400μA	28/56mA/MHz	2-85
HM-92560-8	256K	48	150ns	500μA	350μA	15/30mA/MHz	2-96
HM-92570-8	BUFFERED 256K	48	250ns	600μA	450μA	15/30mA/MHz	2-104

CMOS RADIATION HARDENED RAMS							
PART NUMBER	CONFIG-URATION	PIN COUNT	ACCESS TIME	STANDBY CURRENT-ICCSB	DATA RET. CURRENT-ICCDR	OPERATING CURRENT-ICCOP	PAGE REF
HS-6504RH	4K x 1	18	300ns	100μA	50μA	7mA/MHz	9-18
HS-6508RH	1K x 1	16	300ns	100μA	—	4mA/MHz	9-19
HS-6514RH	1K x 4	18	200ns	250μA	50μA	7mA/MHZ	9-20
HS-6551RH	256 x 4	22	300ns	100μA	—	4mA/MHz	9-21
HS-6564RH RAM MODULE	16K x 4 or 8K x 8	40	350ns	800μA	—	32mA/MHz	9-22

CMOS FUSE LINK PROMS

PART NUMBER	CONFIG-URATION	PIN COUNT	ACCESS TIME	STANDBY CURRENT-ICCSB	DATA RET. CURRENT-ICCDR	OPERATING CURRENT-ICCOP	PAGE REF
HM-6641-8	512 x 8	24	250ns	100μA	—	10mA/MHz	2-113
HM-6616-8	2K x 8	24	120ns	100μA	—	13mA/MHz	2-118

CMOS Article Reprints 8

Article Reprints Table of Contents 8-2

Article Reprints 8-3

Article Reprints Table of Contents

	Page
Defense Electronics	
Part 1 Microprocessor Family Turns to Low Power	8-3
Part 2 High Density LCC Packages	8-10
Computer Design	
Providing CMOS Benefits to Peripheral Chips	8-17
Electronics	
Custom Microprocessor Powers Portable Workstation	8-23
Electronic Design	
For Data Communication, Manchester Chip Could be the Best	8-27
Electronic Design	
Industrial Controller Joins MIL-STD-1553 Bus	8-37
EDN	
Take a Total System Approach with CMOS Memories	8-44
EDN	
LCC Implementation Procedures Enhance a Valuable Technology	8-51

Microprocessor Family Turns to Low-Power CMOS

The 80C86 microprocessor adds a proven design and low power to high performance defense systems.

By Walter J. Niewierski

Next Month, Part II in this two-part series on microprocessors will examine the transition of the low-power 80C86 family to industry standard leadless chip carrier packages.

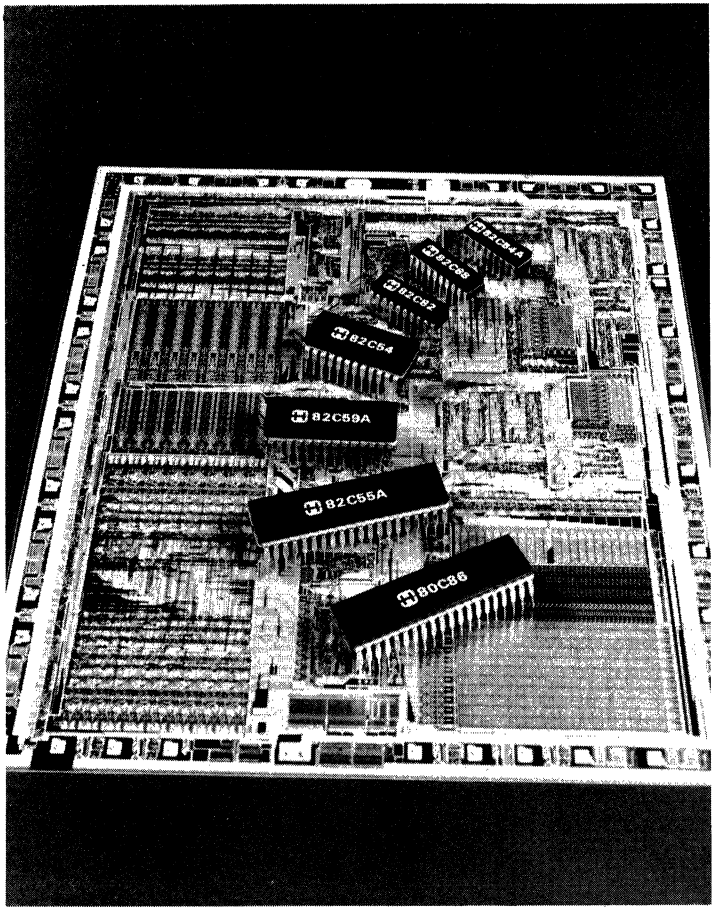
Walter Niewierski is a technical marketing engineer with Harris Corporation's Semiconductor Group, CMOS Digital Products Division, P.O. Box 883, MS 54-130, Melbourne, FL 32901.

CMOS equivalents of existing high performance circuits offer obvious advantages to the military system designer—allowing immediate reductions in critical system operating power, reduced power supply requirements, sealable enclosures, and lighter, higher density packaging. System reliability is improved due to lower ambient and junction temperatures and the high radiation tolerance of the CMOS process. In the past, however, this power reduction usually came at the expense of lower system performance.

The new 80C86 products from Harris Semiconductor have been designed especially for high performance military systems. Initial device specifications for the product line include 5 MHz operation over the full −55°C to +125°C temperature range, with selected products available in 8 MHz versions. Upgrades of all circuits to 8 MHz compatibility are planned. MIL-STD-883B processing allows full implementation of CMOS products in military designs.

80C86 Functional Compatibility

Full functional compatibility with existing 8086 NMOS/bipolar equivalents is provided in the 80C86 family. Programs that test original source



Harris Semiconductor will begin delivering *the 80C86 mil-spec CMOS microprocessor and the six support chips by August. Additional parts will follow into fourth quarter 1983 to complete the family. The 80C86 is an exact replica of the NMOS 8086 processor, and takes advantage of existing software and support tools.*

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devices are being used to verify functionality and compatibility. In-system testing has been done by both the Harris Semiconductor CMOS Applications Group and selected external customer sites to verify functionality in a real system, real time environment providing an additional level of compatibility assurance.

Product compatibility with existing industry standard devices and development systems can immediately improve system performance with respect to power and reliability. Life spans of existing hardware and software designs can be extended by providing direct low-power, high performance upgrades for existing 8086-based systems.

The unit's hardware interface and instruction set are compatible with proven design and development tools. Software developed for projects using the 8086 can be used directly with the 80C86 family, reducing the manpower investment and resulting in decreased development time and cost. With standard software (Ada, Jovial, etc.) for military, defense, and aerospace applications, this software compatibility can result in significant savings in new and existing projects.

CMOS 80C86 Microprocessor Family

Part Type	Description	Scheduled Availability
80C86	CMOS 16-Bit CPU	Aug '83
82C54	CMOS Programmable Interval Timer	Now
82C55A	CMOS Programmable Peripheral Interface	Now
82C59A	CMOS Priority Interrupt Controller	Now
82C82	CMOS Octal Latch	Now
82C84A	CMOS Clock Generator/Driver	Now
82C88	CMOS Bus Controller	Now
HD-6406	CMOS PACI (UART/BRG)	Q3CY83
82C89	CMOS Bus Arbiter	Q4CY83
82C83 82C86 82C87	CMOS Inverting Octal Latch CMOS Bus Transceiver CMOS Inverting Bus Transceiver	Q4CY83

Worst Case Design for Defense Applications

As with all system components, CMOS devices best perform within their specified operating conditions. The problem facing the designer is one of insuring these system operating conditions will not degrade device performance beyond the limits imposed by the design. Devices guaranteed to operate to specifications over "worst case ranges" make this task easier (for example, parameter limits guaranteed over the full temperature range and propagation delays guaranteed at realistic 100 to 300 pF capacitive loads as opposed to 15 to 45 pF). All AC parameters are tested and guaranteed with worst case specified loads on the appropriate outputs.

The 80C86 product line has been designed for military applications; specific operation goals over the military temperature range were established and maintained throughout the design process. Performance is also guaranteed at worst case conditions, including operation over the power supply voltage range and at the maximum rated loads. These worst case specifications insure reliable operation under adverse conditions such as extreme temperature variations, fluctuating power supply level, and heavy output load.

Limits specified for the 80C86 family AC and DC parameters reflect maximums and minimums over the entire military (−55°C to +125°C) temperature range. Capacitive loads are 100 to 150 pF for standard peripherals and 300 pF for the 82C82 and 82C88 bus interface devices, which interface directly with the system bus. These guarantees insure a system is designed to worst case specifications; no performance degradation calculations for guaranteed parameters will be needed during initial design; and, the system will operate properly over the full specified operating ranges.

Low-Power System Application

The 80C86 CPU, operating in the maximum mode, is the focal point in the control module for flight navigation. Non-inverting octal latches (82C82) and transceivers (82C86) provide the address/data latching and buffering for the local bus. The 82C88 CMOS bus controller provides the control signals for the on-board memory, both CMOS RAM and non-volatile CMOS PROM, and for the peripheral circuits.

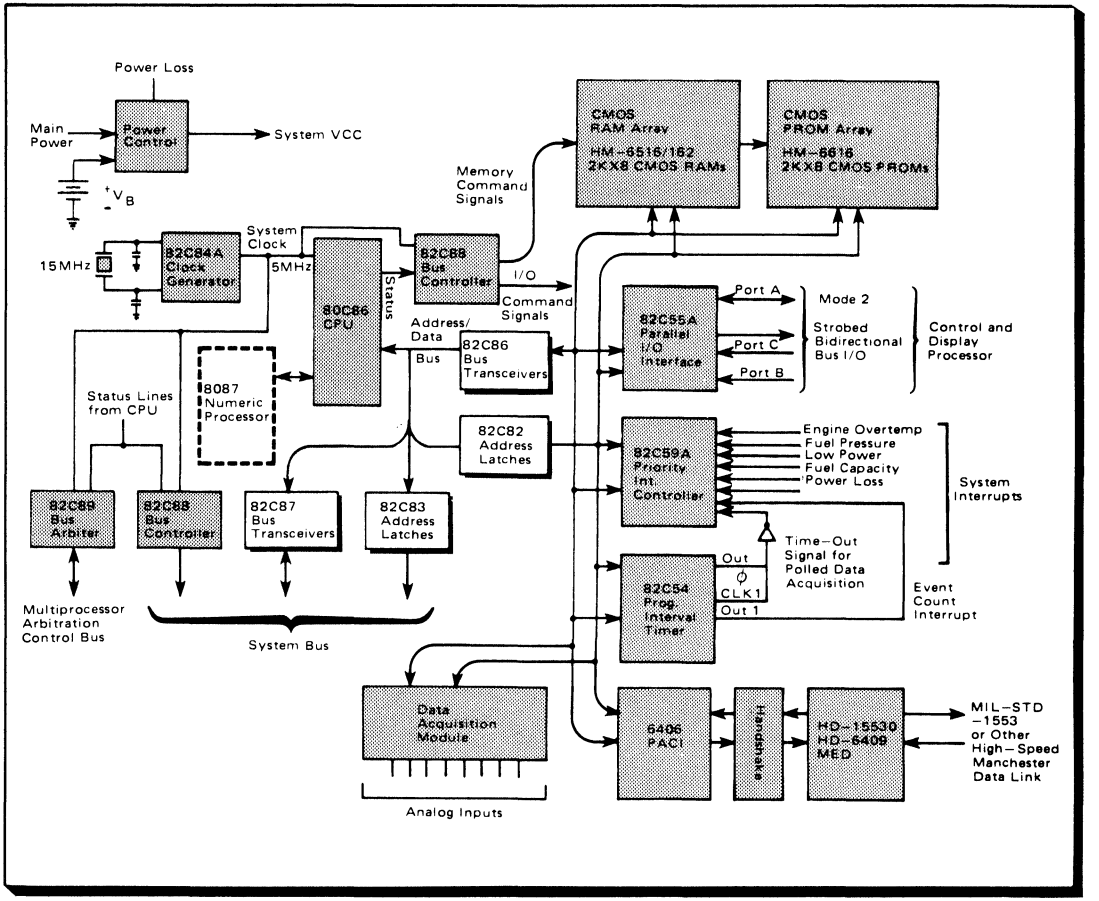
CMOS Memory Options

CMOS memory circuits offer the designer several options. The HM-6516, a 2K x 8 CMOS static RAM, offers a low operating power of 10 mA/MHz, maximum, for military applications. Access times as low as 120 ns make this device compatible with many high-speed applications. Where increased performance is necessary, the HM-65162 asynchronous 16K CMOS RAM can be used with an access time of 70 ns, maximum.

CMOS fuse link PROMS are used in this application because of the high reliability requirements of military systems. The long-term data retention characteristics of polysilicon fuses insure reliable operation in extreme environments. The low power (13 mA/MHz for the 16K density CMOS PROM) and 150 ns access time provide the performance needed for this generation of CMOS systems.

Multiple CPUs

Expanding system capabilities beyond the level available with a single



A typical flight control computer configuration *based on the 80C86 microprocessor family is a full 5 MHz design. The device can also operate at lower speeds to provide even greater power savings. The 80C86 can directly replace the NMOS 8086 in existing designs.*

processor can be accomplished in several ways. The addition of another CPU subsystem, along with the appropriate interface to allow common access to data, significantly improves system throughput. To accommodate this multiprocessing scheme, the 82C88 bus controller and the 82C89 bus arbiter provide the control and arbitration for the system bus. Inverting latches (82C83) and transceivers (82C87) meet the necessary functional compatibility for existing industry standard multiprocessor bus systems.

If there is no need to expand beyond a single board or enlarge to a multiprocessor system, the 80C86 can run in the Minimum mode, where decoded memory and I/O signals are available from the processor. This type of configuration eliminates the need for the 82C88 bus controllers and the additional multiprocessor interface circuitry.

Mixing Technologies

Another way to increase system throughput, especially in cases where arithmetic functions and numeric data manipulation are critical, is to add an 8087 numeric coprocessor to the system. Although not available in CMOS, the device can be used in a CMOS 80C86 system, providing the increase in power dissipation is acceptable.

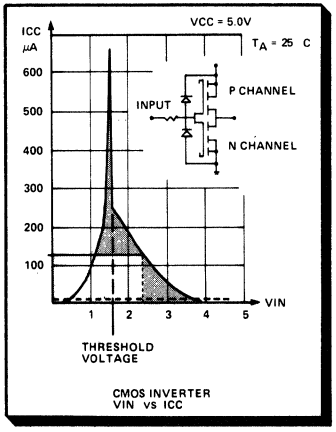
The addition of the NMOS 8087 to the otherwise all-CMOS 80C86 system and the subsequent mixing of technologies is possible with the full TTL compatibility present on the 80C86 products. This compatibility on both inputs and outputs eases interfacing to NMOS and bipolar circuits. CMOS output drivers, along with the dual V_{OH} specification, guarantee operation at CMOS and TTL logic levels.

Mil-Std Bus

When data communication between subsystems is desired, but not necessarily at parallel bus speeds, a MIL-STD-1553 or alternate protocol Manchester-based serial bus can be used. The addition of an HD-6406 programmable asynchronous communication interface (PACI) and an HD-15530 Manchester encoder-decoder

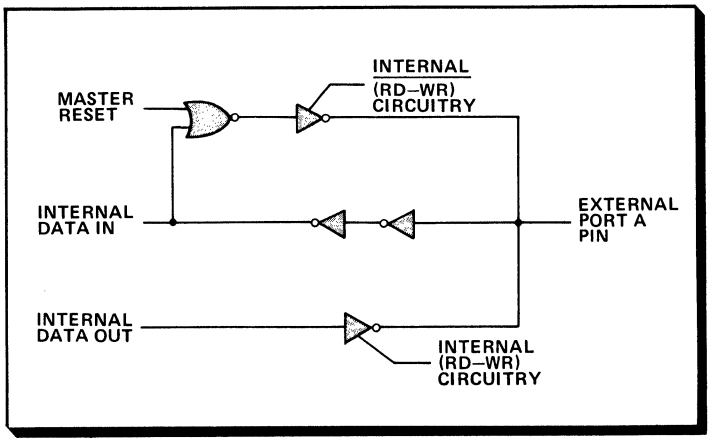
(MED) form a high-speed serial link between several remote systems. Standard eight-bit data transfers can be accomplished in the non-1553 bus applications by using the military version of the HD-6409 Manchester encoder-decoder—which allows more freedom than the MIL-STD-1553 bus for formatting the serial data.

The HD-6406 provides the UART parallel-to-serial/serial-to-parallel conversion function and bit rate generator in a single 40-pin package. A 28-pin version (82C52) will also be available for higher packing density applications. The HD-6406 functions are fully programmable through a microprocessor-compatible bidirectional bus, which has a maximum serial data rate of one megabaud (asynchronous transmission with a 16X clock). The HD-15530 (1.25 M-bit/sec) and the HD-6409's (1 M-bit/sec) maximum data rates can fully support a one M-bit serial bus interface for military applications.



Peripheral Monitor and Control Functions

Several peripheral functions monitor system I/O and timing control. The 82C55A programmable peripheral interface can be used for display control or for information passing between subsystems, using the bidirectional handshaking mode. Upon RESET, the 82C55A port pins become defined as inputs. If these inputs are not used or will eventually become outputs, they have no driving source and are in an undefined, or "float," condition.



Both the 80C86 and the 82C55A *use this on-chip "bus-hold" circuitry to provide valid input voltages to specific inputs without using external resistors.*

Undefined input voltage levels are forbidden in CMOS system design. Undefined input states allow the input circuitry to "float" within the devices' active regions. Unfortunately, floating CMOS inputs tend to migrate toward the threshold voltage and increase ICC substantially. All CMOS inputs, if unused, must be tied to VCC or GND to avoid oscillation and high ICC conditions.

Pull-up/pull-down resistors are the most common method for defining CMOS inputs when no driving source is present. But, this technique has several disadvantages. Additional components (resistors) are necessary, which increase production costs and reduce overall reliability. Higher power operation can actually occur when using pull-up/down resistors. Since the driving circuit must supply the current needed when switched to the opposite state of the pull-up/down resistor, the result can be a significant increase over normal CMOS input leakage current levels of 1 μA.

Bus-Hold Circuitry

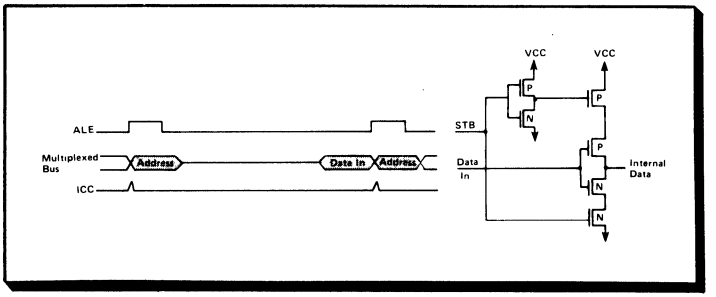
To avoid the need for external resistors and eliminate the high power effects of floating inputs, the 82C55A, along with the 80C86 CPU, uses on-chip "bus-hold" circuitry to provide valid input voltages to specific inputs; this is important when there is no driving source (i.e., a no-connect or a driving input that goes to a high impedance state). The bus-hold circuits maintain these pins at a Logic One level internally and externally until they are defined as outputs or are overdriven by an external source.

An external driver must be capable of supplying 300 μA minimum sink or source current at valid input voltage levels in order to overdrive the bus-hold circuits. Since this circuitry is active and not a passive pull-up resistive-type element, the 82C55A, standby current is kept to 10 μA, maximum.

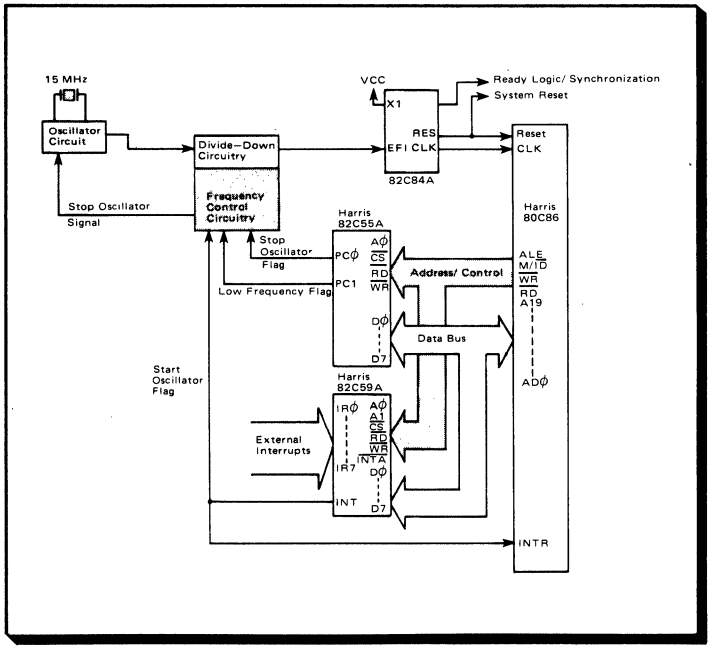
System needs and overall compatibility dictated the placing of bus-hold circuits on specific devices. The 80C86 CPU has bus-hold devices on selected pins (AD0 AD15, etc.), which are common to the local bus. This eliminates the compounding of the overdrive current necessary if all 80C86 family members had bus-hold circuitry, and keeps all current requirements within TTL LSTTL capabilities.

Gated Inputs

The 82C82 octal latch also has specialized input circuitry to minimize power dissipation and help eliminate the need for external resistors. Gated inputs minimize the effects on the ICC from switching and undefined inputs. This gating function, initiated by the falling edge of the strobe (STB) input, disconnects the input inverter from the VCC by turning off the upper P-channel (Q1) and lower N-channel (Q2). Thus, there is no current path, other than leakage, between VCC and



Gated inputs on the 82C82 octal latch *eliminate extraneous current spikes due to input conditions unrelated to latch operation. While data is latched, floating inputs can be directly connected to the 82C82 inputs without using pull-up resistors.*



For power critical applications *where power is reduced to the point that even full-time operation at reduced frequency is not desirable, the 80C86's static circuitry allows the clock to be stopped.*

GND during input transitions when data is latched in the 82C82. Internally, logic states are held valid by the feedback logic signal in the circuit's latch section.

Input gating also isolates the driving source from the internal circuitry. Invalid logic states from floating inputs cannot be transmitted to succeeding stages when the inputs are turned off, eliminating the need for pull-up resistors when data is latched.

In an 80C86 system, the STB input is driven by an ALE (address latch enable). At 5 MHz, the high pulse width of the ALE is 98 ns or approximately 15 to 20 percent of the bus cycle period. Therefore, 82C82 inputs are disabled 80 percent of the time. During this time, ICC transients from input switching are eliminated, resulting in a lower operating current.

Polled or On-Demand Data Sensing

The 82C59A priority interrupt controller and the 82C54 programmable interval timer manage system interrupt and polling control functions. Two methods, used either separately or concurrently, are available for controlling the system sequencing of data acquisition. Polled acquisition or interrupt-driven data taking can be accomplished with the circuit described.

The 82C54 timer can be programmed, using single or multiple 16-bit timers (three per package), to provide an input to the 82C59A interrupt controller and cause execution of a data acquisition software routine. This procedure can be repeated by using the 82C54 in the rate generator mode (Mode 2), inverting the signal, and inputting it to the 82C59A programmed for edge-triggered inputs.

If certain functions must be executed only every Nth cycle, the 82C54 Timer 0 output (OUT 0) can be fed into the clock of Timer 1 (CLK 1). Timer 1 can be programmed to operate as an event counter (Mode 0 interrupt on terminal count) and interrupt the 82C59A every Nth count.

The 82C59A is also used for control of other external interrupts such as emergency conditions like engine over-temperature, pressure high low, and other on-demand situations. If desirable, the repeated interrupt for polling purposes can be disabled by using the 82C59A's interrupt masking ability, which only allows generation of critical situation interrupts.

The 82C59A interrupt inputs can be prioritized. When both polled and on-demand sequences are used concurrently, the on-demand emergency situations would be considered highest priority.

Tailoring Low-Power System Operation

Several circuit design techniques can be valuable in examining low-power operation at the system level. CMOS is only a first step. Significant reductions in system-level power consumption can be realized if proper design approaches are taken.

In an aircraft situation, power is not normally a problem. If, however, the microsystem power fails independent of the main aircraft power, full

navigation controls can remain intact and operational with the 80C86 CMOS control system. With a backup battery power supply, the power sensing unit can transfer the system from main power operation to battery supply. With system power levels approximately 10 percent of equivalent NMOS bipolar circuits, full 5 MHz operation can be maintained.

As primary power is diminished (battery discharging) or removed (power interruption battery backup operation) in portable or remote battery-powered applications, running at a lower frequency to conserve power becomes important. Operating power is critical in low-power applications, and CMOS operating power is directly related to frequency.

With the 80C86 family's static design, power requirements can be user controlled; lowering the frequency reduces power. Static design (i.e., no internal dynamic registers needing constant clocking or refresh) allows operation from DC to the individual device's maximum rated frequencies.

The CMOS 80C86 static design allows the system clock to drop to a lower frequency (100 kHz, for example), making full computational and data manipulation powers available while significantly reducing system power consumption. This low frequency operation is not available with most NMOS processors, including the NMOS 8086 where 2 MHz is the minimum allowed clock frequency. Dynamic register designs in the NMOS CPUs need to be refreshed at a minimum rate and do not allow low operating frequencies.

Typical operating power for the 80C86 CPU at 5 MHz is 40 mA, derated linearly as frequency drops (approximately 2 mA at 100 kHz). Similar deratings are also valid for the power dissipations of the peripheral, support, and memory circuits.

Finally, given a power critical situation where power is diminished to the point that even low frequency, full-time operation is undesirable, the 80C86's static internal circuitry allows clocks to be stopped. This capability eliminates the power dissipation associated with switching, and reduces device currents to standby levels. With static DC operation, individual peripheral device standby currents are guaranteed to be less than 10 μA, with the 80C86 CPU typically less than 500 μA.

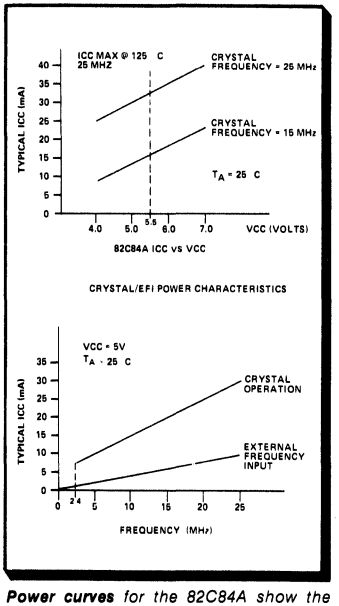
Static design can also stop and single-step the system clock during system prototyping. This debug method allows the designer to inspect the system bus and examine specific operations. The real time complications of 5 MHz bus transfers are eliminated and system debug is simplified.

Stopped Clock Power Savings

Although the 82C84A clock generator's 40 mA ICC limit is significantly lower than the bipolar 8284A's 162 mA limit, it is still the largest, single power user in a CMOS 80C86 system; this is due to the high frequency of

CMOS/NMOS/Bipolar Parametric Comparison

	CMOS 80C86	NMOS 8086	CMOS 82C54	NMOS 8254	CMOS 82C55A	NMOS 8255A	CMOS 82C59A	NMOS 8259A	CMOS 82C82	Bipolar 8282	CMOS 82C84A	Bipolar 8284A	CMOS 82C88	Bipolar 8288
VIH	2.2V	2.0V	2.2V	2.0V	2.2V	2.0V	2.2V	2.0V	2.2V	2.0V	2.2V	2.0V	2.2V	2.0V
VIL	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V
VOH	3.0V/ VCC 0.4V	2.4V	3.0V/ VCC 0.4V	2.4V	3.0V/ VCC 0.4V	2.4V	3.0V/ VCC 0.4V	2.4V	2.9V	2.4V	VCC 0.4V	2.4V	3.0V/ VCC 0.4V	2.4V
IOH	-2.5mA/ -100μA	-400μA	-2.5MA/ -100μA	-400μA	-2.5mA/ -100μA	-400μA	-2.5mA/ -100μA	-400μA	-8mA	-5mA	-2.5mA	-1mA	-8mA/ -2.5mA	-5mA
VOL	0.4V	0.45V	0.4V	0.45V	0.4V	0.45V	0.4V	0.45V	0.4V	0.45V	0.4V	0.45V	0.5V/ 0.4V	0.5V
IOL	+2.5mA	+2.5mA	+2.5mA	+2mA	+2.5mA	+2.5mA	+2.5mA	+2.2mA	+8mA	+32mA	+2.5mA	+5mA	+20mA/ +8mA	+32mA/ +16mA
ICCSB	500μA Typical	Not Applicable	10μA	140mA	10μA	120mA	10μA	85mA	10μA	160mA	10 μA Typical	162mA	10μA	230mA
ICCOP	40mA @ 5 MHz Typical	340mA	1mA/ MHz Typical	140mA	1mA/ MHz Typical	120mA	1mA/ MHz Typical	85mA	1mA/ MHz Typical	160mA	40mA @ 25 MHz	162mA @ 25 MHz	1mA/ MHz	230mA
C_L	100 pF	100 pF	150 pF	150 pF	150 pF	150 pF	100 pF	100 pF	300 pF	300 pF	100 pF/ 30 pF	100 pF/ 30 pF	300 pF/ 80 pF	300 pF/ 80 pF



***Power curves** for the 82C84A show the effects of both frequency and voltage decreases on the ICC.*

operation (15 24 MHz crystal frequency for ⅓ MHz system frequency) and the non-ideal waveform of the crystal signal.

When using the 82C84A in a stop-clock application, the external frequency input (EFI) mode of operation must be used. The 82C84A clock generator has a minimum crystal frequency of 2.4 MHz (corresponding to 800 kHz system frequency) for internal oscillator operation. The EFI input allows use of an external clock to provide the main timing. This external clock is processed through the same internal 82C84A circuitry as the crystal oscillator input, so timing within the system remains the same.

An additional benefit, critical to the successful design of a stop-clock circuit, is the 82C84A's reduced operating power when using an external frequency source to drive the EFI input.

With X1 and X2 crystal operation, the input transistors spend a greater percentage of time in the active region due to the sinusoidal nature of the crystal circuit. Driving the EFI input to VCC and GND levels with an external source more effectively turns internal circuitry on and off, resulting in decreased operating power.

The clock frequency reduction must be properly timed to meet minimum 80C86 clock high- and low-time requirements. Therefore, along with the appropriate divide-down circuitry needed to provide the proper lower frequency, synchronization between the low frequency signal line and the control circuitry is necessary. Care must be taken to avoid cases of asynchronous timing errors caused by irregular clocks that are outside the CPU specification limits.

The 82C55A PPI provides the parallel CPU interface to the control circuitry. An interrupt from the 82C59A priority interrupt controller can provide the start-up signal for the system clock control circuitry. The 82C59A allows prioritizing and masking of interrupting sources so that; during the time the system is stopped, only the most critical signals may restart the processor. ■

High Density Leadless Chip Carrier Packages Increase Reliability, Save Weight

A military CMOS 16-bit microprocessor packaged in LCCs reduces operating temperatures, size, and weight, adding to that family's low-power advantages.

By Walter J. Niewierski and Jeffrey M. Wilkinson

Last month, DE *looked at the 80C86 family, which adds low-power CMOS to a proven design for high performance defense systems. This month, Part II in this two-part series on microprocessors will examine that family's transition to industry standard leadless chip carrier packages.*

Just as critical as power consumption is packaging technique. The low-power operation of the CMOS 80C86 family, along with memory and support chips, allows for design of sealed, portable system enclosures. In turn, this type of packaging reduces operating temperatures and minimizes hostile external environment effects, increasing system reliability.

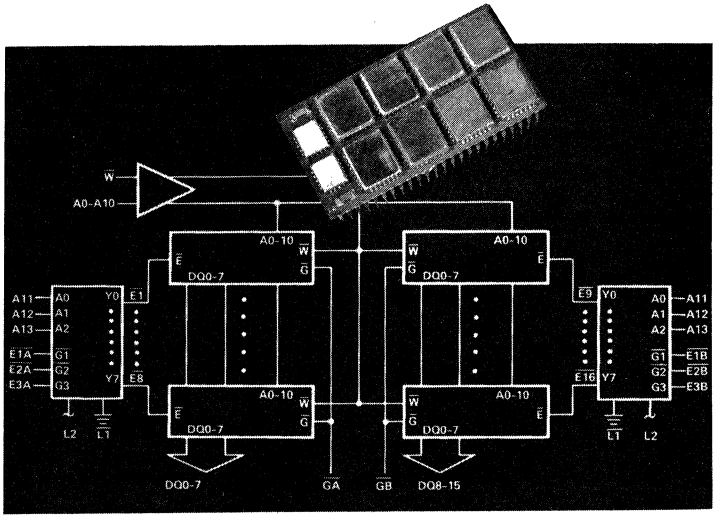
System Level Reductions

Replacing higher power devices with their CMOS equivalents can reduce system "hot spots" caused by localized high dissipation circuits. A direct replacement with low-power CMOS components will significantly reduce system ambient temperatures. Using the power supply current requirements of the CMOS 82C88 and bipolar 8288 bus controller, along with a typical θjA (junction to ambient temperature rise with respect to power dissipation) of 50°C/W, the following device temperature comparison can be made:

$T = \theta jA \times \text{power dissipation} + T_A$

For bipolar
= 50°C/W x (230 mA) x 5.5V + 125°C
= 50°C/W x 1.265W + 125°C
= 63.25°C + 125°C
= 188.25°C, typical

For CMOS
= 50°C/W x (5 mA) x 5.5V + 125°C
= 50°C/W x .0275 mW + 125°C
= 1.375°C + 125°C
= 126.375°C, typical



Leadless chip carriers *attached to a ceramic dual-in-line substrate allow Harris Semiconductor to package the complete 16-bit CMOS microprocessor as a single unit. Harris has already used this packaging concept to produce 64K- and 256K-bit RAM arrays based on 16K and 64K chips. All these LCC packaged products are military qualified.*

The rise in the die surface temperature of CMOS is approximately two percent of the increase seen in NMOS products. This lower CMOS die temperature results in a significant in-

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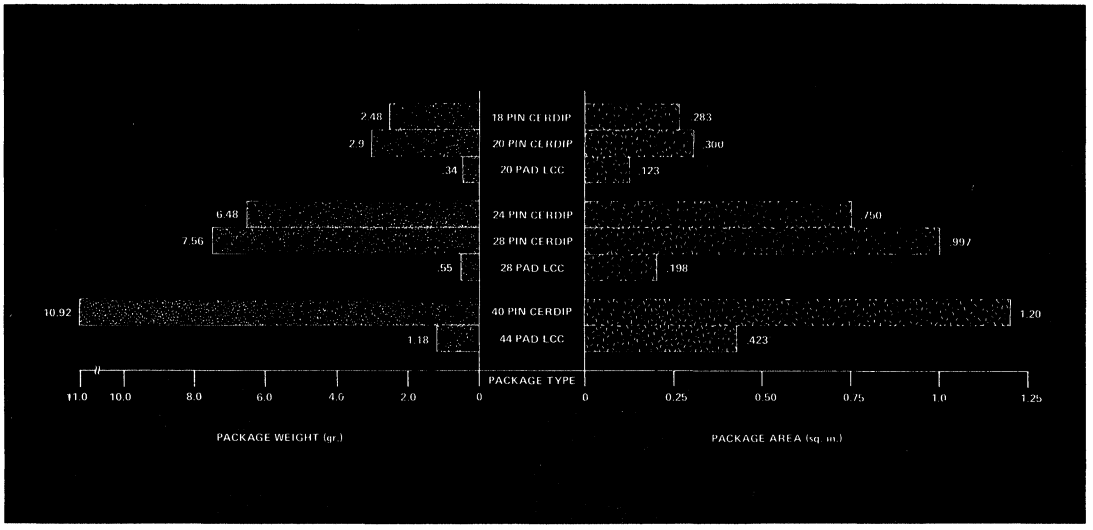


Package weights and area *for LCCs are compared to equivalent ceramic dual-in-line packages.*

crease in the mean time between failure (MTBF). The MTBF equation shows the direct relationship of the failure rate and temperature:

$$MTBF_T = e^{EA/KT}$$

where $MTBF_T$ = MTBF at temperature T

EA = activation energy (ev)

K = Boltzman's constant

T = absolute temperature (°K)

Similar increased MTBF numbers can be estimated for system operation when system ambient temperatures are reduced by CMOS circuits.

With decreased system temperatures, the need for special cooling equipment and enclosure openings can be eliminated or reduced. The use of cooling techniques such as heat pipes, liquid coolants, heat sinks, and louver assemblies can add weight and volume to systems. Besides these physical disadvantages, the lower reliability of electromechanical operation and the system's exposure to hostile environments adds an additional risk factor to system reliability. CMOS systems can keep the system operating temperature to lower levels, enabling the use of sealed enclosures with a minimum of cooling.

Temperature also affects circuit and system performance. CMOS leakage currents and, therefore, standby power dissipation increase at the high end of the temperature range. Performance also degrades because of increased channel resistances on the P- and N-channel transistors. Keeping the system ambient temperature low results in an improved overall performance.

Replacing existing circuits with low-power CMOS offers many benefits. However, the system environment remains constant—that is, compatible with NMOS/bipolar operation. Power supplies, cooling equipment, and enclosure size and weight all remain the same.

In order to optimize the reductions possible in weight and cost and increase reliability, the system must be designed with low power in mind. Smaller system power supply requirements and lower temperatures eliminate the need for cooling components.

Device Level Miniaturization

Decreasing an individual device's package can lead to miniaturization and portability. Flatpacks and DIPs are the main packages used in military system designs. However, leadless chip carriers (LCC) have recently become popular because of their small size and light weight.

The trend toward using dual-in-line packages has proven sufficient in most applications. But, where very light and small, complex electrical functions are required, LCCs offer space and flexibility. DIPs occupy approximately three times the space an LCC package uses for the same pin count. And unlike an LCC package, the DIP has leads that can bend or break, adding a parasitic resistance and capacitance.

The introduction of flatpacks to military applications proved an alternative to the DIP package in reducing board space requirements. But, flatpack costs are high because of the large amounts of gold used in the package plating. Long lead length and narrow spacing also require special carriers for handling. And, when soldering to printed circuit boards, the long lead length permits package vibration, which could affect the reliability of the leads or their solder connections.

Leadless chip carriers offer small package sizes, no leads to bend or break, and premium electrical performance due to full parametric testing allowed at the package level. For critical military applications, MIL-STD-883B, group A, B, C, and D can be applied to leadless chip carriers in a method

similar to those applied to dice packaged in a size-brazed DIP.

Many devices cannot be manufactured in LCCs or must be placed in larger pad count carriers because of bipolar and NMOS technologies' excessive power dissipations. But with CMOS, power dissipation is reduced—optimizing package size and pin count.

The leadless chip carrier pinout definitions for the CMOS 80C86 family follows, for the most part, predefined pinout and package assignments as established by the original NMOS source. With certain device types, specifically the original source products, larger than necessary packages were used. For example, the 8282 octal latch, 8284A clock generator, and 8288 bus controller are packaged in 28-pad LCCs, while 20-pad LCC packages are standard for the 82CXX CMOS equivalents. One of the main reasons for using this enlarged package for bipolar devices is its higher-than-CMOS power dissipation. With CMOS' lower power characteristics, however, minimum package sizes can be achieved. Using 20-pad LCCs for the CMOS versions of the above devices allows for maximum system packing density.

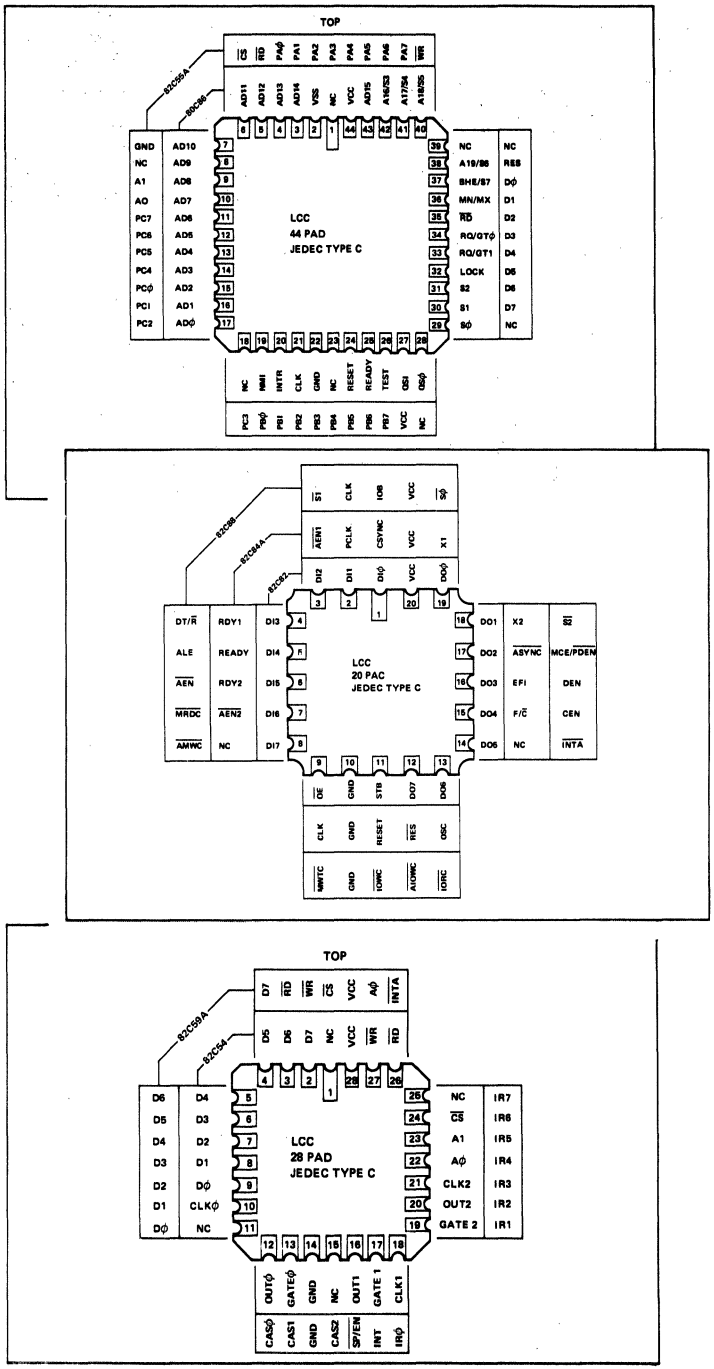
Leadless chip carriers for high density packaging and minimized pad counts further reduce board space and weight in high density systems. In addition, LCC packages' reduced package lead lengths and interconnect lower the parasitic inductance of the circuitry. Parasitic inductance is a major contributing factor to noise in high-speed CMOS system designs (See sidebar, "System Noise Reduction in High-Speed CMOS Design").

LCC Assembly Techniques

The relatively recent revival of the LCC package, along with the advantages of implementing these packages on printed circuit boards and substrates, allows designers a high-density packaging option. To ease the transition from conventional DIP/PCB assemblies to the LCC/PCB packaging option, the designer must understand the differences between the two packaging technologies.

Substrate Material Selection

The basic concern for selection of the substrate material is matching the



***Pinouts** for the 80C86 CMOS microprocessor family are similar to the more familiar pinouts used for conventional flatpacks.*

CMOS vs NMOS Power Requirements

Part Type	Description	CMOS Operating Power Supply Current	NMOS/Bipolar Equiv. Power Supply Current
80C86	CMOS 16-Bit CPU	40 mA	340 mA
82C54	CMOS Interval Timer	5 mA	140 mA
82C55A	CMOS Parallel Interface	1 mA	120 mA
82C59A	CMOS Interrupt Controller	1 mA	85 mA
HD-6406	CMOS UART/BRG	3 mA	100 mA
82C82	CMOS Octal Latch	1 mA	160 mA
82C83	CMOS Octal Latch (Inv)	1 mA	160 mA
82C84A	CMOS Clock Generator	25 mA	162 mA
82C86	CMOS Bus Transceiver	1 mA	160 mA
82C87	CMOS Bus Transceiver (Inv)	1 mA	130 mA
82C88	CMOS Bus Controller	5 mA	230 mA
82C89	CMOS Bus Arbiter	5 mA	165 mA
Approx. System Power Supply Current		**89 mA**	**1,952 mA**

80C86 Family Package Comparisons

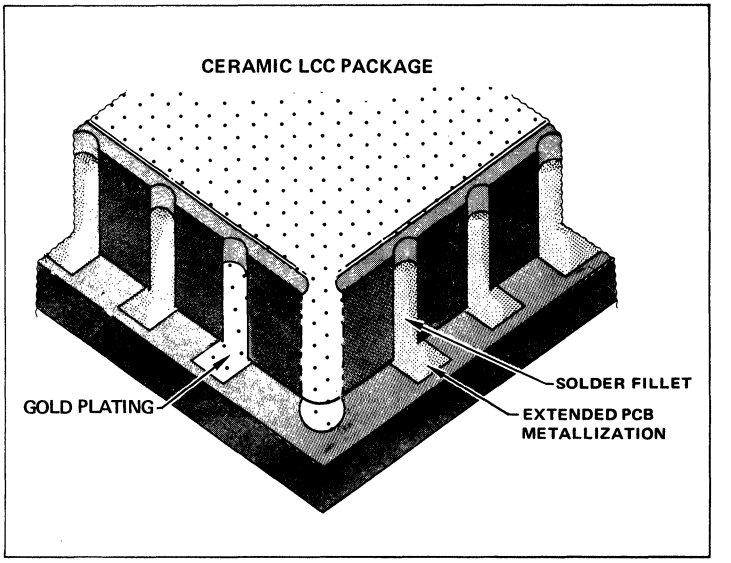
Part Type	DIP Pin Count	LCC Pad Count	DIP Area (Sq. In.)	LCC Area (Sq. In.)	DIP Weight (Gr.)	LCC Weight (Gr.)
80C86	40	44	1.2	0.423	10.92	1.18
82C54	24	28	0.75	0.198	6.48	0.55
82C55A	40	44	1.2	0.423	10.92	1.18
82C59A	28	28	0.997	0.198	7.56	0.55
HD-6406	40	44	1.2	0.423	10.92	1.18
82C82	20	20	0.3	0.123	2.9	0.34
82C83	20	20	0.3	0.123	2.9	0.34
82C84A	18	20	0.283	0.123	2.48	0.34
82C86	20	20	0.3	0.123	2.9	0.34
82C87	20	20	0.3	0.123	2.9	0.34
82C88	20	20	0.3	0.123	2.9	0.34
82C89	20	20	0.3	0.123	2.9	0.34
System Area/Weight Summary			**7.43 Sq. In.**	**2.526 Sq. In.**	**66.68 Gr.**	**7.02 Gr.**

Material Thermal Properties

Substrate Material	TCE (In./In./°C x 10^{-6})	Comments
Alloy 42	5.3	42% Ni, Balance Fe
96% Alumina	6.3	Industry Standard
94% Alumina	6.4	Industry Standard
92% Alumina	6.4	
Copper Clad Invar	6.4	
99.5% BeO	6.4	Expensive
Low Carbon Steel	12.0	Porcelanized
Polyimide G30	14.3	Industry Standard
Epoxy/Glass G10	15.8	Industry Standard
Triazine G40	16.0	Industry Standard
CDA 101 Copper	17.3	Very High TCE
6061 Aluminum	23.6	Very High TCE

linear thermal coefficient of expansion (TCE). Matching the TCEs is critical to attaching an LCC to a substrate when the assembly must be able to survive the number of thermal cycles typical of military applications and testing. When the LCC is soldered on a board, the solder interface is not only the electrical contact but the mechanical connection as well.

When the TCEs of both the package and mounting substrate are not properly matched, thermostatic deflection (warp) can occur during temperature cycles. When these two materials warp, torque is directed to the solder joints, which results in a fatigued mechanical/electrical connection. This problem becomes even more apparent as the LCC pin count increases. Larger package and substrate sizes result in higher stress levels. The selection and use of board material should follow this general rule: The larger the difference between the TCEs of the two materials used (the LCC and the substrate material), the smaller the substrate surface area should be. Available materials range widely in cost and TCE characteristics.



Printed circuit board metallization *should extend beyond the LCCs outer edge. This extension permits molten solder to flow up the castellated regions, and to form a fillet of solder to complete the electrical connection while strengthening the mechanical bond.*

Printed Circuit Considerations

After selecting the substrate material, the printed circuit trace geometries should be investigated. The circuit traces for LCC foot pads should be the same size as the metallization on the bottom of the LCC and slightly longer to the outer edge of the package. This metallization allows the solder, when heated to the reflow temperature, to wet both the base contacts and the LCC package's castellations.

The outer surface of the solder deposit forms a fillet where it extends over the metallization pad on the substrate's surface, strengthening the mechanical bond. This type of bond raises the LCC away from the board's mounting surface to facilitate cleaning the residual flux and debris under the package.

To optimize packaging density, relatively tight geometries in layout are of concern. Leadless package layouts often require .010-in. lines, 010-in. spaces between lines, and .020-in. or smaller feed-through holes. The pads that connect to the LCCs are typically .020-in. wide, and are .050-in. center to center. This spacing allows one .010-in. line at .010-in. spacing to be run between the LCC mounting pads.

If lines are run close to other metallization, a solder mask should be used on the board to prevent solder bridging during the reflow process. When using multilayer boards or substrates, a clean layout can be made by allocating the surface layer metallization exclusively to LCC mounting pads—eliminating the need for a solder mask and reducing the concern for solder bridging. Electrical noise problems can be diminished by power gridding the supply buses on a unique layer while routing signal lines on other layers of the substrate.

LCC Mounting Techniques

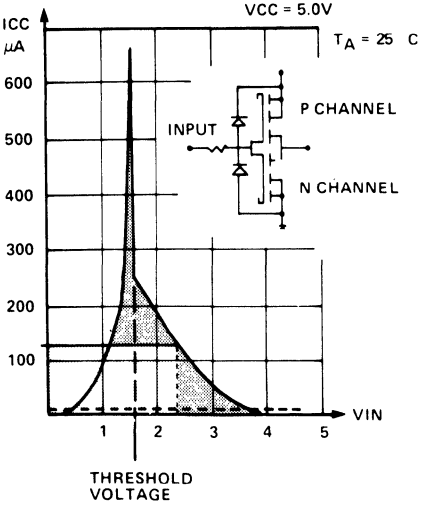
Socketing and soldering directly to the board are the two methods possible for mounting LCCs on circuit boards. In military applications, socketing becomes a disappointing compromise for LCC mounting because of the socket's bulky size. An LCC socket has its place in less critical applications, but can severely sacrifice packing density, and falls short of the stringent environmental testing required by most military applications. Direct LCC to substrate mounting is the most reliable method for assembly.

The basic principle for attaching LCCs to boards and substrates is reflow soldering. Both the leadless package I/O metallization and the interconnecting substrate metallization are pretinned with solder; the two are then mated and heated by one of a number of means. Surface tension and the cohesive properties of the molten solder align the package over the substrate metallization. The assembly is then cooled, making complete the electrical/mechanical bond.

The best results are usually obtained from reflow soldering, and when both the LCC and the metallization on the substrate it is to be attached to are pre-tinned. The LCC package pads can be pre-tinned by fluxing and dipping. The substrate pads are usually tinned by wave soldering or screening on a solder paste.

When using a wave solder tinning approach, and after the substrate has been tinned, an adhesive must be applied temporarily to hold the LCC in place over the substrate metallization during the reflow process.

In implementing the screened on solder paste technique, the paste is



CMOS INVERTER
VIN vs ICC

System Noise Reduction in High-Speed CMOS

The majority of current flow in an all CMOS system is transient by nature, occurring on the waveform edges or transitions where instantaneous demand for current occurs. These current transients result from:

- charging and discharging of output load capacitance
- simultaneous P-channel and N-channel switching

The currents generated by these switching conditions can be large and cause noise on the power supply lines. However, the current's magnitude is not the only factor in determining the size of VCC/GND variations—The time period over which this current is switched is also critical. If this time period is relatively long, the current can be categorized as steady or bulk current, and the transient effect on the power supply voltage is minimal.

However, as the time period decreases, these inductance effects begin to play a more important role. The relationship of time and inductance are given by:

$$V=L\,{}^{di}/_{dt}$$

Switching the same amount of current more quickly will have as great an effect on the VCC as an increase in the magnitude of the current change in the same time period. As propagation delays and output rise/fall times decrease, the effect of the related inductance becomes more significant.

The parasitic inductance is a result of system interconnect, socket, decoupling capacitor, and device package contributions. The inductance must be minimized to reduce this transient effect. The main sources of inductance are lead lengths (both IC and decoupling capacitor), PC board interconnect (VCC to capacitor to GND), and the capacitor, itself.

Although the designer can do little about standard IC packaging and lead length, manufacturers can employ several techniques for controlling the IC's parasitic inductance. Matching device size to package cavity area allows minimum bond wire lengths in assembly. Doubling the VCC and GND bond wire interconnect also reduces parasitic inductance effects within the package.

Printed circuit board runs should be kept to minimum lengths with VCC and GND lines 3/16-in. to 5/16-in. wide to reduce power line inductance. In prototype circuits, extra care should be taken in limiting wire length and including sufficient decoupling since the wire and socket lead length add inductance beyond that normally found in PC boards. Low inductance capacitors and socket elimination will help control system related inductance. —*W.J.N. & J.M.W.* ■

applied to the substrate contacts using a screen printing technique. Normally, a layer of "wet" paste, eight to nine mils thick, is deposited on the substrate contacts. Then the contact area, covered with paste, is air dried until tacky before the LCC is attached. The LCC is then mounted to the corresponding contacts manually or by automatic placement.

One important step in the LCC assembly process is baking the populated substrates dry before soldering, which allows the air and flux pockets in the paste to evacuate, minimizing the volatility effects in a vapor phase soldering operation. This process is vital because unevacuated flux pockets will cause the package to float during the reflow operation. Floating affects the package's positioning properties, and an unacceptable package alignment can occur. Also, the liquid vehicle of the solder paste is evaporated and the LCC is temporarily held to the substrate by the paste, which is now dry.

LCC placement on the substrate is not as critical as it might appear. During the reflow process, the dried solder paste holds the LCC in place while the paste reaches the reflow temperature. During this process, the surface tension of the solder will pull the LCC into alignment over the substrate contacts. The placement must be accurate enough to insure the LCC solder pads do not overlap the adjacent interconnect on the metallization below.

Heat must be applied to melt the solder and connect the LCC and the substrate. Methods such as belt furnaces, heated air chambers, and infrared radiated heat techniques can be used, but are not finding widespread acceptance. The most popular heating method for high-volume production is the vapor phase reflow technique.

In vapor phase reflow, the populated substrate to be soldered is lowered into a saturated vapor above a pool of high boiling point, flourinated hydrocarbons. Usually, vapor phase soldering systems have two operation zones. The primary zone is used for heating; the secondary zone is used as an intermediate cooling and cleansing zone before the assembly is removed from the soldering operation.

As the board is lowered into the primary zone, the solder joints are reflowed uniformly by the vapor, condensing over the surface of the substrate, which gives up its latent heat from vaporization. This thermal exchange heats the board quickly and evenly. When the substrate is raised into the secondary zone, the now condensed fluid from the primary zone drips off the board into the boiling liquid below. The substrate assembly exits from the process, uniformly oldered, dry, and relatively clean.

Cleaning the soldered assembly should be performed immediately after the vapor phase reflow process while the boards are still hot. Uncongealed residue can be easily removed at this time, resulting in thorough cleaning.

Another reflow technique employs hot solder oil. The substrate with positioned LCCs are fully immersed in a hot oil bath to bring the solder and parts up to the reflow temperature quickly. The assembly is then removed from the oil and allowed to cool. Rinsing the assembly afterwards removes residual oil and excess flux. This technique is useful for experimentation and low-volume production because of its relatively small capital investment.

LCC Assembly Rework

The repair and replacement of a failed device packaged in an LCC is important in chip carrier assembly processes. The advantages in rework stem from the ease of reflow soldering. Since there are no leads on LCCs and usually no holes in the substrate to deform, many rework cycles are allowed. Of course, rework is dependent on the reflow technique, type of solder, reflow temperature, and the thickness of the metallization used in a particular application. During a rework situation, LCC removal can be accomplished using several techniques.

One method is to use the same hot solder oil immersion technique for applying the LCCs to a board. After the immersion and subsequent reflow of the solder, a pair of tweezers, or a similar tool, can be used to remove the defective LCC from the board. Other removal methods are possible, such as using a soldering iron with a specially shaped tip to heat the contacts or by heating the defective package and its surrounding area with a forced hot air gun.

The heat gun method is usually the most convenient, inexpensive, and practical for rework. When the LCC is heated by the gun, the package should be removed with tweezers—the now exposed substrate contacts can be tinned, if necessary, as could the LCC contacts on the replacement device. The LCC is manually replaced in close proximity to its final position. The repair area or entire board is then heated to the solder reflow temperature to complete the operation.

System on a Substrate Concept

When the appropriate LCC system components are assembled on a ceramic substrate with dual-in-line pins, the space, weight, and reliability advantages of LCCs are made more accessible. This "system on a substrate" technique allows LCCs to be used in more traditional system configurations such as those using standard DIP packaging.

One of the first movements in this concept direction has been the development of memory arrays on ceramic substrates. The HM-6564, a 64K CMOS RAM module, was first introduced in 1979, and uses sixteen 4K x 1 CMOS RAMs mounted on both the substrate's top and bottom. This packaging technique further increases an LCC's functional density on the RAM module. Other products available in module form include the Texas Instruments TMS4164, a 64K dynamic RAM assembly, and a 64K EEPROM assembly from National Semiconductor, the NMH2864.

With the introduction of the 16K CMOS RAM, a step-up in module density is also seen. The HM-92560 uses sixteen HM-6516 RAMs, and has a total capacity of 256K bits of static CMOS memory. The HM-92560 can be configured as a 16K x 16 or 32K x 8 static RAM array.

The HM-6564 and HM-92560, along with the other such modules, provide only the memory circuitry—This approach increases the system packing density when large amounts of memory are necessary. Maximum reduction, however, is not accomplished because bus drivers and decoders must be added externally to the module assembly. To achieve a greater reduction in size, as many functions as possible must be placed on high density assemblies.

The Harris HM-92570 is a beginning to the "system on a substrate" development. By providing LCC-packaged CMOS bus drivers and decoders on the substrate, all the functions of a 256K-bit memory board are contained in one high density assembly. The HM-92570 address inputs are buffered and have an input current leakage limit of 10μA so direct connection to the CPU address bus is possible without additional buffering. The HD-6440 CMOS decoders on the substrate meet the memory array decoding needs.

The Digital Equipment Corporation Micro/J-11, a CMOS module assembly, which is a two-chip set equivalent of the PDP-11 minicomputer, has adapted this concept to the microprocessor area. Two CMOS devices manufactured by Harris, the control chip and the data chip, are packaged in 64-pad LCCs and are mounted on a 60-pin ceramic DIP substrate, compatible with the PDP-11's full instruction set. Compared to the original PDP-11 assembly, which consisted of several boards, this transition to a 60-pin substrate offers significant size and power reduction advantages.

The next step will be the combination of CPU, I/O, and a significant amount of memory onto a single substrate assembly. The development of more highly integrated processor, such as the 80C186, that include I/O and control functions on-chip will make the logistics of providing all capabilities in a single high-density unit easier to handle. With all functions available in one unit, systems can be implemented with one assembly connected to the outside world, or additional assemblies added to provide greater amounts of memory or high-density multiprocessing capabilities. ■

PROVIDING CMOS BENEFITS TO PERIPHERAL CHIPS

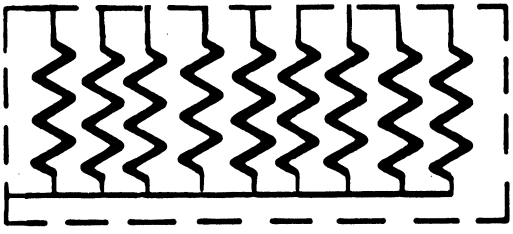
CMOS technology is finally being extended beyond processors to peripheral support chips. An era of low power, high performance designs may result.

by Walter J. Niewierski

Today's complementary metal oxide semiconductor microprocessors have evolved in differing ways—some through direct hardware/software emulation of existing N-channel metal oxide semiconductor microprocessors, others by the merging of several architectures and instruction sets. In both cases, performance improvement and low power operation result.

In order to take advantage of these microprocessor advancements, logic and memory also had to improve. For example, an entire second generation of high speed small scale integration/medium scale integration (SSI/MSI) logic appeared in the 74HCXX/74SCXX products. These logic devices offered low power Schottky transistor-transistor logic (LS/TTL) equivalent propagation delays at complementary metal oxide semiconductor (CMOS) operating power levels and provided the necessary high speed "glue" for advanced CMOS microprocessor systems.

Similarly, higher density CMOS memories are now available at much greater speeds. Functional options include both synchronous and asynchronous memory



operation to meet specific system requirements. Synchronous 16k CMOS random access memories (RAMs), for example, have a guaranteed operating current of 10 mA/MHz maximum for low power or battery operated systems. In addition, asynchronous 16k CMOS RAMs, with the same configuration, have access times as low as 70 ns.

CMOS nonvolatile memory support is available with both erasable programmable read only memory (EPROM) and fuse link programmable read only memories (PROMs). CMOS PROMs offer the greatest benefits in nonvolatile applications where low power and reliable data retention are critical. Present CMOS fuse link PROMs store data in programmed polysilicon fuses. Fuse link technology yields permanent, stable storage characteristics for the life of the device. Polysilicon fuses, combined with the low power of CMOS, provide an excellent alternative to EPROMs or bipolar PROMs for battery operated and other low power systems.

For high performance, low power 2716-type memory applications, 16k CMOS synchronous fuse link PROMs

Walter J. Niewierski is a technical marketing engineer at Harris Corp, Semiconductor CMOS Digital Products Div, Melbourne, FL 32901, where he is responsible for technical support of CMOS digital products. Mr Niewierski has a BSEE from the University of Michigan.

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TABLE 1

CMOS 80C86 Family Peripheral Support Chips

Part	CMOS device type/function	Comments
82C82	octal latch	T_{PD} = 35 ns max at C_L = 300 pf
82C84A	clock generator/driver	8-MHz system clock frequency
82C88	bus controller	Status decode function
82C54	programmable interval timer	10-MHz count frequency
82C55A	programmable peripheral interface	Control word read capability
82C59A	priority interrupt controller	8 user defined priority interrupt requests

provide a low 13-mA/MHz operating current with 175-ns access times. Moreover, performance upgrades to 125-ns access times will soon be possible. In nonvolatile memory, CMOS has a significant speed advantage over N-channel MOS (NMOS), while showing a large power reduction.

Improving peripheral support

Although sophisticated CMOS microprocessors have brought high performance to low power designs, they cannot reach their full potential without equally high performance, low power consumption support chips. For the most part, CMOS peripheral circuit design efforts have lagged. This has limited the development of systems attempting to use CMOS devices exclusively. A new family of microprocessor peripheral circuits fills this void by providing increased performance and functionality without sacrificing low power consumption.

Because the Harris 80C86 peripheral product line (see Table 1) has a wide functional range, complex, high performance systems for low power applications can be designed. The peripherals are TTL compatible CMOS versions of industry standard NMOS devices. In addition, they incorporate improvements that eliminate traditional problems in hardware, software, and power consumption. With the peripheral circuit family, cost-effective, low power designs can be implemented at superior performance levels.

Drop-in replacements for their NMOS equivalents (see Table 2), the 80C86 peripheral family offers equal or greater performance. The peripheral family's architecture is fully compatible with 80C85- and 80C86-type microprocessors. However, the popular 2-line control method for data movement, using read (RD) and write (WR) lines, allows interface to almost any recent generation microprocessor.

In addition, consistent family specifications make system design easier. All peripheral product ac and dc specifications are guaranteed over the industrial (−40 °C to 85 °C) or military (−55 °C to 125 °C) temperature range and 5-V ±10% voltage range. Timing specifications for peripheral circuits allow full speed operation with a CMOS 80C86 central processing unit (CPU) at 5 MHz, with no wait states.

Dual specifications for the logical 1 output voltage (VOH) ensure interface compatibility of the peripherals with both CMOS and TTL devices. Even in an all-CMOS design, there may be the need for circuit functions available only in NMOS or bipolar. In this case, the peripherals allow direct interface without pullup resistors or additional buffers. For future system enhancements with circuits of other technologies, the retrofit problems that occur with non-TTL compatible devices are eliminated.

Several techniques used to design the peripherals improve CMOS's natural low power operation. During normal system operation, bus signals at the latch inputs can exhibit high impedance or make transitions unrelated to latch operation. These voltage transitions cause an increase in power dissipation due to the low resistance path between V_{CC} and ground created when the input circuitry switches.

In Harris' 82C82 octal latching bus driver, gated inputs eliminate input switching current transients by turning off the inputs when data are latched (strobe pin = low). See Fig 1. The strobe pin (STB) disconnects the input inverter from the power supply by turning off the upper P-channel (Q1) and lower N-channel (Q2). No current flow from V_{CC} to ground occurs during input transitions. Invalid logic states from floating inputs are not transmitted to succeeding circuitry, thereby eliminating the need for pullup resistors.

Steering clear of high current conditions

Bus-hold circuitry used on specific pins avoids high current conditions caused by floating inputs to CMOS devices. These circuits maintain a valid logic state when

TABLE 2

Peripheral Interface Compatibility

	Logical 1 Input voltage (VIH)	Logical 0 Input voltage (VIL)	Logical 1 Output voltage (VOH)	Logical 1 Output current (IOH)	Logical 0 Output voltage (VOL)	Logical 0 Output current (IOL)
80C86 Peripherals	2.0 V/2.2 V Ind/Mil	0.8 V	3.0 V V_{CC} − 0.4 V	−2.5 mA −100 μA	0.4 V	2.5 mA
NMOS 8086 Family	2.0 V	0.8 V	2.4 V	−400 μA	0.45 V	2.5 mA
CMOS	70% V_{CC}	30% V_{CC}	V_{CC} − 0.5 V	−10 μA	0.4 V	2.0 mA
LS/TTL	2.0 V	0.8 V	2.5 V 2.7 V	−400 μA −400 μA	0.4 V 0.5 V	4.0 mA − Military 8.0 mA − Commercial

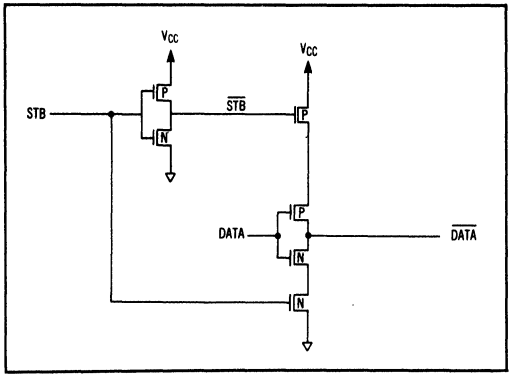

Fig 1 Gated inputs of 82C82 octal latching bus drivers. Such internal circuitry eliminates need for external pullup resistors.

no driving source is present (ie, an unconnected pin or a driving input that goes to a high impedance state). In the 82C55A programmable peripheral interface (PPI), all port pins have bus-hold circuitry (Fig 2). Port pins are defined as inputs at reset. If they are either open or will eventually become outputs, they have no driving source and are floating. With normal CMOS input circuitry, this could cause a high current situation. On the PPI port pins, however, bus-hold circuits maintain a logic 1 level internally and externally until the ports are either defined as outputs or overdriven by an external source.

To overdrive the bus-hold circuits, an external driver must supply 300-μA minimum sink or source current at valid input voltage levels. Since this bus-hold circuitry is active and not a resistive-type element, the associated power supply current is negligible. The PPI standby current specification is 10 μA maximum.

All 80C86 peripheral family devices are designed with fully static circuitry. This allows the devices to be operated from dc to their individual maximum rated frequencies. Since operating power is critical in low power applications, the user can control this parameter,

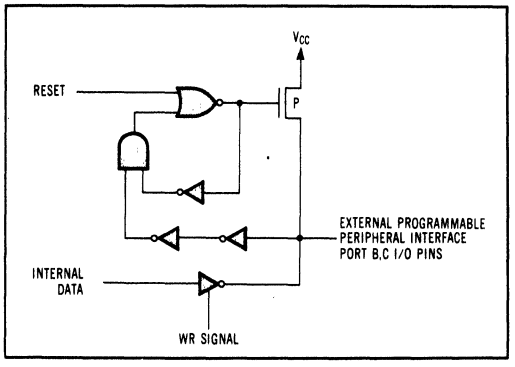

Fig 2 Bus-hold circuitry used on the 82C55A programmable peripheral interface CMOS peripheral. Logic 1 level is maintained internally on undefined port pins to keep power consumption to a minimum.

based on system operating frequencies. CMOS operating power is directly related to frequency; the lower the frequency, the lower the operating power dissipation. At a dc frequency, device standby currents are typically less than 10 μA.

Where voltage is concerned, the peripheral family maximum input voltage limit (ground $-$ 2.0 V$\leq V_{IN} \leq$6.5 V) essentially eliminates the problem of device latch-up. Latch-up results from an overvoltage condition on the inputs or outputs that causes a parasitic silicon controlled rectifier on the die to become active. This creates a high power supply current (ICC) condition. The increased input/output (I/O) voltage range on the peripherals offers greater protection from system-induced noise, as well as increased noise immunity.

Expanding parallel ports

Adding parallel I/O ports to an 80C48 family microcomputer using a PPI is well documented. However, designing this system in CMOS (see Fig 3) requires additional attention to the port reset condition and the state of unused port inputs. The CMOS PPI eliminates these concerns and, in conjunction with a unique feature of the 82C82 octal latch, keeps power dissipation low enough for battery operation. An extremely low standby power supply current of 10 μA maximum is guaranteed over the full operating temperature range for both the PPI and the octal latch. This is especially desirable in idle or low power modes of operation. Since these devices see mostly static operation, the standby current level is the dominant factor in overall power dissipation.

With the use of bus-hold devices on all port inputs, the PPI eliminates the need for pullup resistors to prevent undefined signal states. Upon being reset, all port (A, B, and C) pins are pulled high by internal bus-hold devices instead of the standard NMOS PPI procedure of putting all port pins into the high impedance state. The bus-hold devices also provide valid logic levels to CMOS inputs connected to the port pins prior to port initialization. Shaded areas in Fig 3 indicate where pullup resistors, normally needed for CMOS systems, are eliminated.

A low level external drive input (I_O = 300 μA) can overcome the bus-hold function. If the port input is unused, the bus-hold device maintains a high logic level and provides a valid logic input to the port pin. Since the bus-hold device is an active component on the chip and the PPI standby current is specified as 10 μA maximum, dc standby current is decreased by a factor of 1000 from the levels seen with pullup resistors.

Functional update is simplified by a readable control word on the PPI. Status of this device can be obtained by a control-word read operation. Data are transferred from the PPI control register, eliminating the need to store port configurations in system memory or internal registers.

Used in this application for address/data bus demultiplexing, the octal latch keeps power at a minimum with a specialized input circuit design. Gated inputs on the octal latch prohibit the passing of invalid input states to octal latch internal circuitry during the time data are latched. This prevents undefined logic states and high current transients due to input switching.

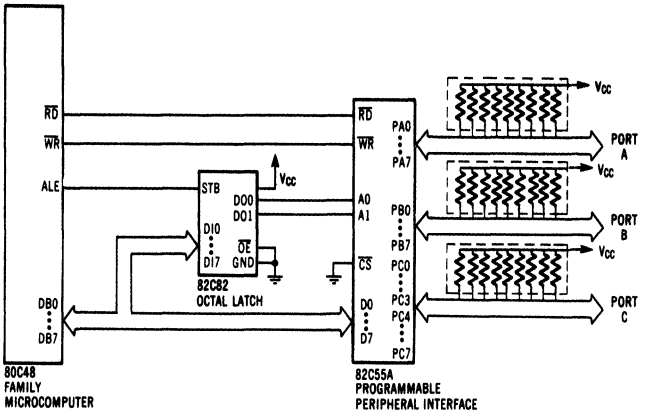

Fig 3 Parallel I/O port expansion with CMOS peripheral low power consumption and elimination of external pullup resistors (shaded areas) are benefits of CMOS techniques.

Waking up the processor

One of the most appealing features in many CMOS microprocessors is the interrupt wake-up from power-down mode. In this operation, the CPU is brought back from a low power idle mode by an external interrupt. Typically, simple interrupt schemes must be implemented since only a single external interrupt is available at the processor itself. With the 82C59A CMOS priority interrupt controller (PIC), eight separate interrupting sources can wake up the processor on a priority basis. For complex systems, 64 interrupts can be serviced via the cascaded connection of up to eight PICs.

Fig 4 shows how the PIC accommodates several interrupts in a single-chip CMOS microcomputer system. Addressing for the 82C59A PIC takes a 2-level approach—standard read/write operations and interrupt vector transfer. Since there is no interrupt acknowledge (INTA) signal available from the processor (this line is needed to transfer the interrupt vector information from the PIC), the necessary decoding for these two sets of operations must be handled elsewhere. A single HD-6440 CMOS line decoder and one 74HC00 quad 2-input NAND gate will do the job. A single bit from port B (PB1) is used to gate the microcomputer RD signal to the 82C59A PIC RD input for standard data transfers (PB1 = logic 0), or to the INTA input for vector information (PB1 = logic 1).

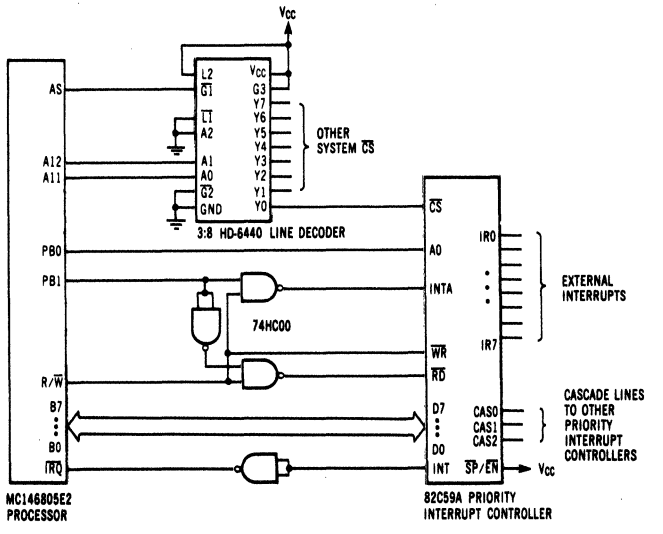

Fig 4 Multiple interrupt handling in priority interrupt controller CMOS chip. Up to eight levels of interrupts are possible, with a single 82C59A priority interrupt controller.

TABLE 3

Priority Interrupt Controller Chip Interrupts

Interrupt Request Inputs	Interrupt Bit Assignments							
	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

A PIC response can occur in either of two user programmable modes. The first mode is the classic 8080/85 format where a call opcode is transmitted with two bytes of additional vector information. For the most efficient interrupt response in this system, however, the 8086 compatible mode should be used. This mode needs only two INTA pulses instead of the three required for mode 1 operation. During the initial INTA cycle in the 8086 compatible mode, the PIC freezes the state of the interrupts, resolves priority, and issues the master interrupt codes on the cascade lines. No data are transmitted on the data bus during the first cycle. On the second INTA cycle, a byte of interrupt code is sent to the CPU. This acknowledgment byte is defined in Table 3. The host CPU programs the upper five bits (D3 through D7) at initialization. They provide the base address for interrupt vectoring. The lower three bits (D0 through D2) provide the offset based on the interrupting source.

INTA signals are generated by decoding specific addresses' output during load accumulator (LDA) instructions. The vector information transferred during the last INTA cycle can be used in an interrupt service routine using an indexed jump to locate the specific service program.

The timing diagram in Fig 5 shows a 146805 microcomputer's response to a wake-up interrupt, along with the necessary INTA generation and vector information retrieval from the PIC. The ability to wake up an idle CMOS microcomputer with any of several interrupting sources greatly increases single-chip system flexibility.

High resolution timing

Although the increased speeds of CMOS microprocessors meet the timing requirements of many applications, some demand a more precise reflection of time. In these situations, the 82C54 CMOS programmable interval timer (PIT) provides high frequency count capability while the 82C84A CMOS clock generator/driver (CGD) delivers, from a single input frequency, both a high frequency timer input and a lower frequency CPU clock. High resolution timing is thus accomplished with relatively low system clock frequencies.

In the system depicted in Fig 6, an 8-MHz timer frequency is used with a 4-MHz CPU clock. The CGD generates three output signals: OSC is the crystal frequency; CLK is the crystal frequency divided by three; and PCLK is the clock frequency divided by two. A 24-MHz parallel resonant, fundamental mode, AT cut crystal on the CGD results in a 24-MHz OSC frequency, 8-MHz CLK

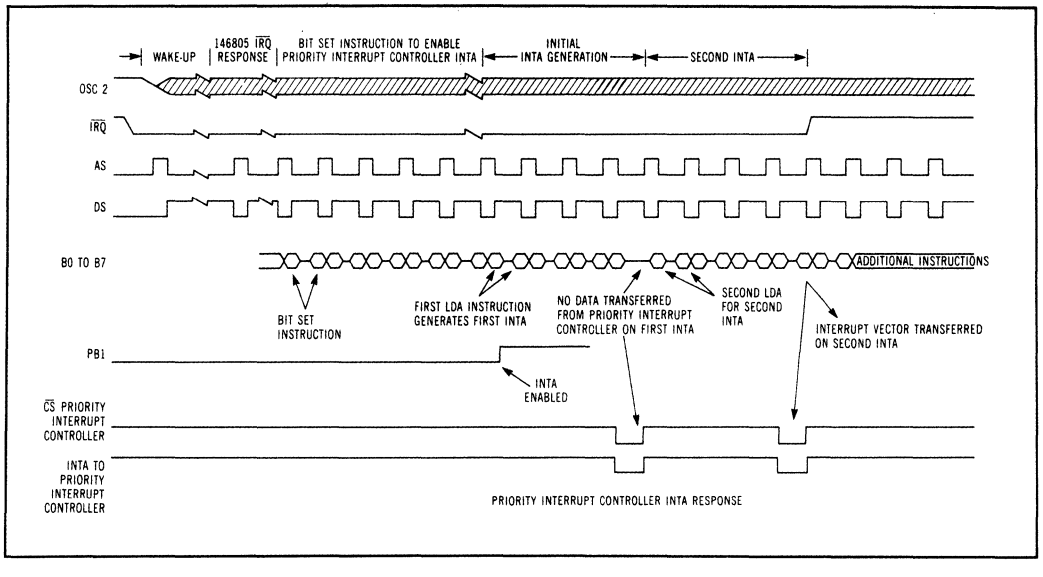

Fig 5 Timing diagram of microprocessor response to a wake-up interrupt. Any of several interrupts can initiate the wake-up response.

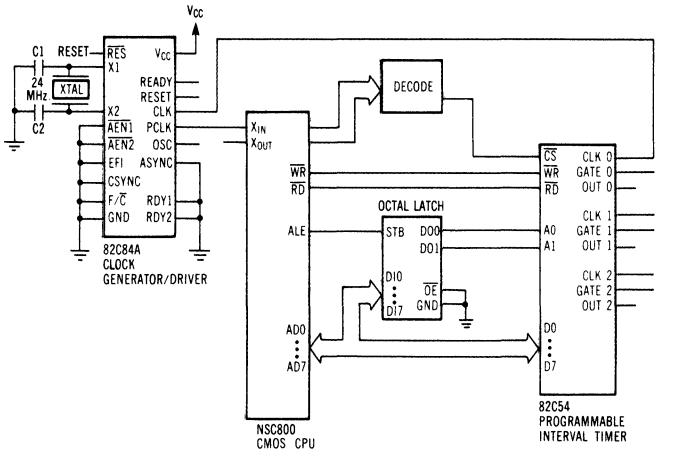

Fig 6 CMOS programmable interval timer and clock generator. Such a system provides high timing resolution from low system clock frequencies.

frequency, and 4-MHz PCLK frequency. The system thus has an 8-MHz count frequency and 2-MHz NSC800 operation. If an upgrade to 4-MHz operation is desired, the 8-MHz CLK output from the PIT can clock both the processor and the PIT. The guaranteed maximum count frequency for the PIT is 10 MHz minimum. The 8-MHz output from the CGD meets the minimum pulse width requirements for the PIT clock input. This high count frequency allows resolution of time increments down to 125 ns, even with processor T-state periods of 500 ns.

Two software features—a readable status word and realtime count indication—allow full 82C54 PIT control in high frequency applications. The status-word read capability enables the processor to get an accurate indication of device status and reconfigures the counter when necessary. For accurate realtime count readings, the PIT can be read while still incrementing. When a read count operation is initiated, the current count is held in a count register until the read is completed. The count register is then updated to the new elapsed count status. If lower system operating power is desired, or if a slower CPU speed is needed, the 82C84A CGD base frequency can be reduced. Since CMOS operating power is directly related to frequency, both CGD and PIT operating power will be lower at these reduced frequencies.

The advent of a diverse group of CMOS peripheral chips heralds a new era in system design. Applications demanding low power consumption, high performance, and portability can now be served by an entirely CMOS oriented approach. Broadening CMOS applications into areas hitherto restricted to the realm of other technologies will allow designers more flexibility in creating tomorrow's systems.

CUSTOM MICROPROCESSOR POWERS OFFICE WORK STATION

by Carl P. Gerstle and Donald A. White, *Digital Equipment Corp., Small Systems Engineering Group, Maynard, Mass.*

☐ Generous use of complementary-MOS semiconductor technology in a new processor chip and in many other circuit components imparts high performance and outstanding reliability to a combined small-business computer and office-automation work station. Beneficiary of the C-MOS magic is the DECmate Work Processor, the newest member of the fully compatible family of word- and data-processing systems based on the 12-bit PDP-8 architecture. Its new integrated-circuit processor, called the 6120, runs an extended PDP-8/A instruction set, including memory-address expansion on chip.

For both the 6120 processor and the 6121 input/output controller, C-MOS was deemed superior to less-power-efficient static n-channel MOS technology and also to more complex dynamic n-MOS technology. Although dynamic n-MOS could have reduced the amount of power required, as compared with static parts, a dynamic design would not have been as clean to work with for the logic functions needed.

In the asynchronous environment of static logic, chip designers need not be as precise in planning timing tolerances as is necessary to maintain two-phase clock synchronization in dynamic logic. Moreover, single-step design debugging in static logic allows the designer to see individual problems as they happen at slow clock speeds. The system clock may be brought down to dc if desired, there being no minimum cycling rate required.

C-MOS is superior

The 6120 chip (Fig. 1) was a joint development project between DEC's Small Systems Engineering group and the Harris Semiconductor division of Harris Corp., Melbourne, Fla. It is about three times faster than the predecessor 6100 C-MOS processor used in the earlier WS78 computer.

The speed improvement was measured executing a representative mix of instructions. In fact, the 6120 is even a little faster than a PDP-8/A minicomputer running the software of the WS200 multiterminal word-processing system.

Two differences between the 6100 and 6120 are chiefly responsible for the speed hike. First, the 6120 was designed to perform some operations in parallel, but the 6100 processes all functions serially. For example, the page addresses in memory are calculated at the I/O pins while data is being computed in the arithmetic and logic unit. Secondly, the shrink from 6-micrometer geometry in the 6100 to 4-μm features in the 6120 reduced on-chip capacitance, boosting transfer speeds with little increase in power dissipation.

A significant jump in transistor density on the 6120 owes much to the move to 4-μm technology, but it is also due in part to enhanced on-chip interconnection techniques. The die size of the 6120 is 230 mils by 210 mils—only a 20% increase in die area for a 175% increase in transistor count as compared with the 6100.

Old reliable

The high reliability experienced with the 6100 C-MOS chip in more than four years in the field, as well as the low power consumption and other design benefits of this technology, made it an easy decision to use such logic in the 6120 processor chip. Furthermore, there were many good reasons to extend the use of C-MOS in preference to n-MOS and TTL logic wherever possible among support functions surrounding the central processor.

C-MOS was also chosen for the 6121 custom I/O controller chips designed for this product—two of them on the processor board and one on the optional communications-controller board. C-MOS is used, as well, for the read-only and random-access memories in the control store of the processor board and for the universal asynchronous receiver-transmitters in the serial printer and keyboard control circuitry, also on board. The control memory is used for such functions as self-testing, terminal I/O emulation, floppy-disk control, and a buffer memory and control registers for the video display.

Altogether, there are 27 static C-MOS ICs on the microcomputer board and 14 more on the communications-controller board. However, dynamic n-MOS was chosen for main memory to achieve the maximum storage capacity per dollar. These RAMs are the only dynamic circuitry on the processor board.

Memory control

On-chip memory-extension control in the 6120 boosts its addressing capability over previous family members from 4-K 12-bit words to 32-K words in each of two separate memory spaces. In addition, the new chip executes the memory-extension instructions faster. It also contains 12 special-purpose registers and control logic, along with the arithmetic and logic unit.

Extensions to the PDP-8/A instruction set include stack-command macroinstructions that permit more efficient encoding of the ROM-based firmware. Another benefit from the expanded instruction set is the addition of power-up self-test diagnostics. The 6120 costs about the same as the 6100, but by taking over memory-extension control, it reduces total system cost.

The mostly C-MOS, cool-running single-board micro-

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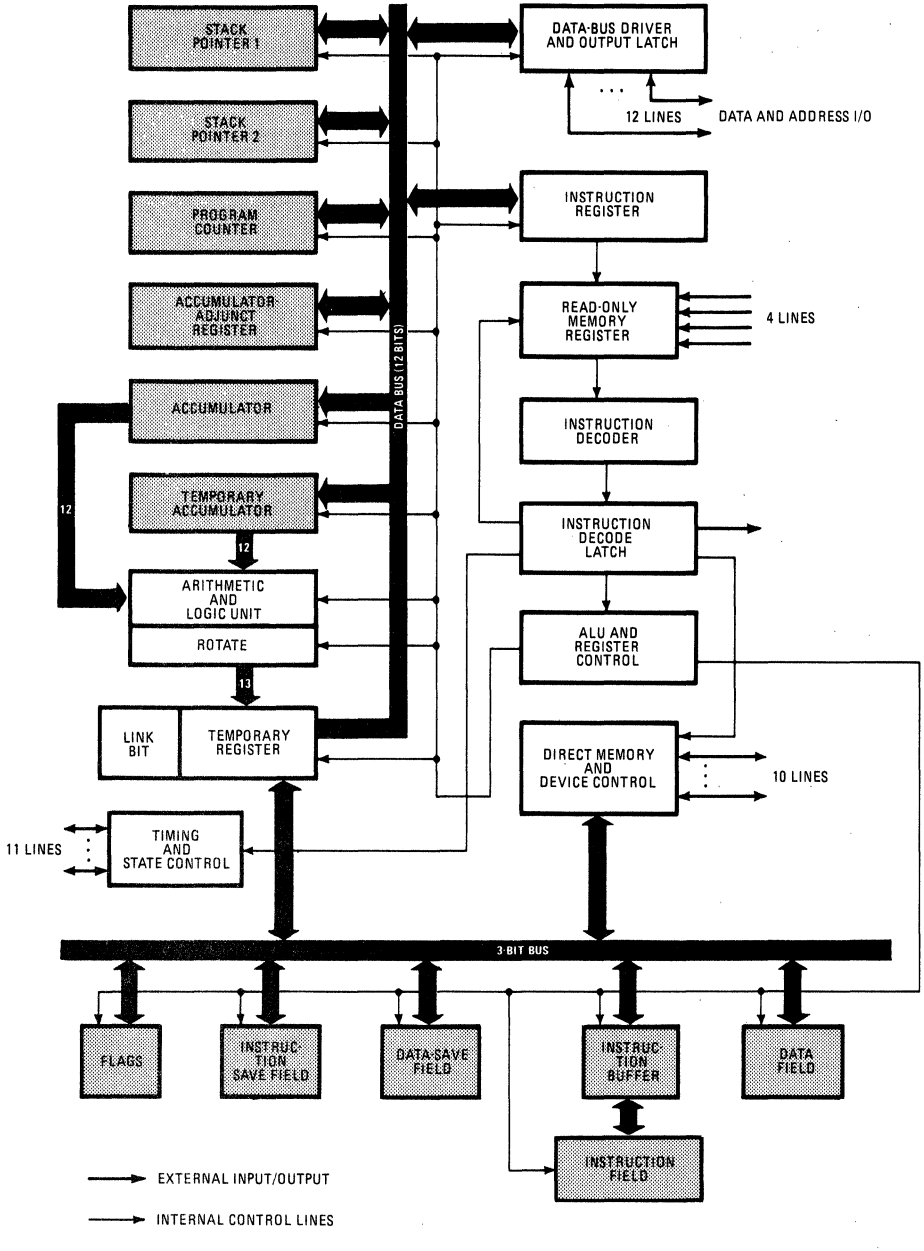
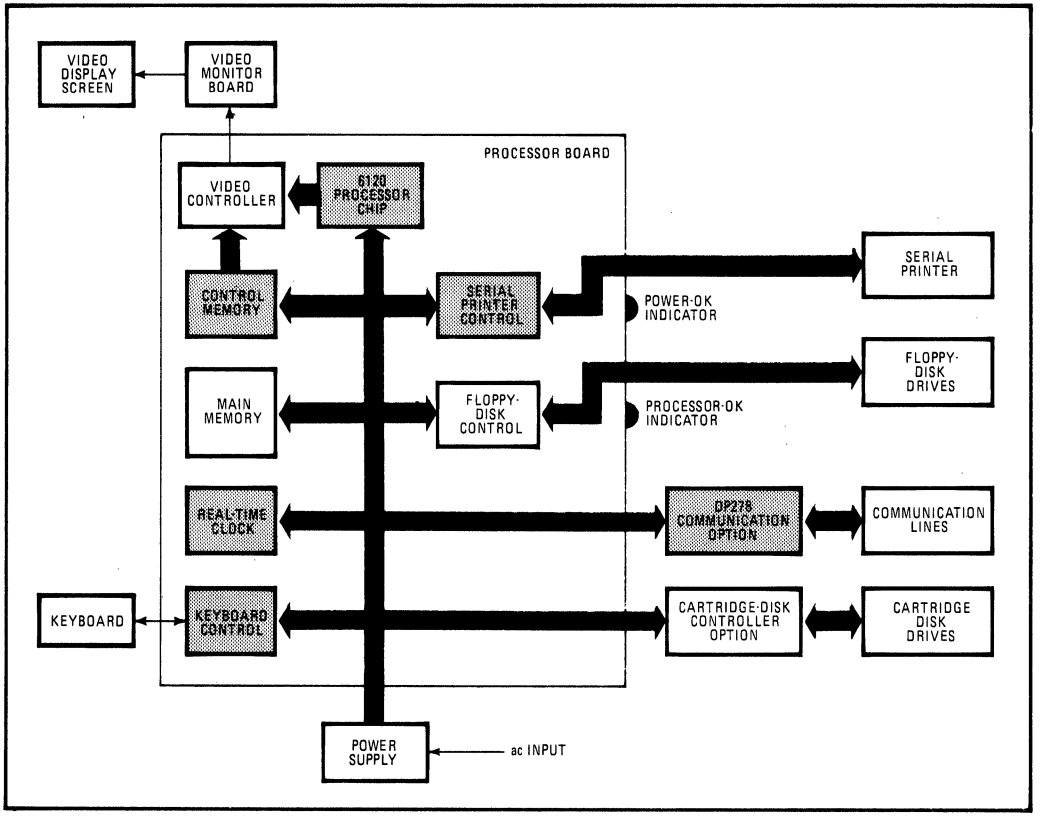


1. Chip off the old block. The 6120 C-MOS processor chip implements the much-used PDP-8 architecture, executing an extended PDP-8/A instructions set. The design uses two system buses—the data and address I/O bus and the C-bus—and 12 special-purpose registers (tinted).



2. Energy-efficient worker. The C-MOS–intensive DECmate desktop system packs a lot of function onto a small number of low-power boards. The processor board alone handles eight functions. The building blocks implemented totally or partly in C-MOS are shaded.

computer (Fig. 2), requiring a mere 15 watts, is the controller of all functions in the computer. The 11.1-by-10.5-inch DEC-standard extended quad board contains eight major functional units: the processor, the 32-K 12-bit–word main memory, address space for as much as 32-K words of control memory, a real-time clock, and four control circuits.

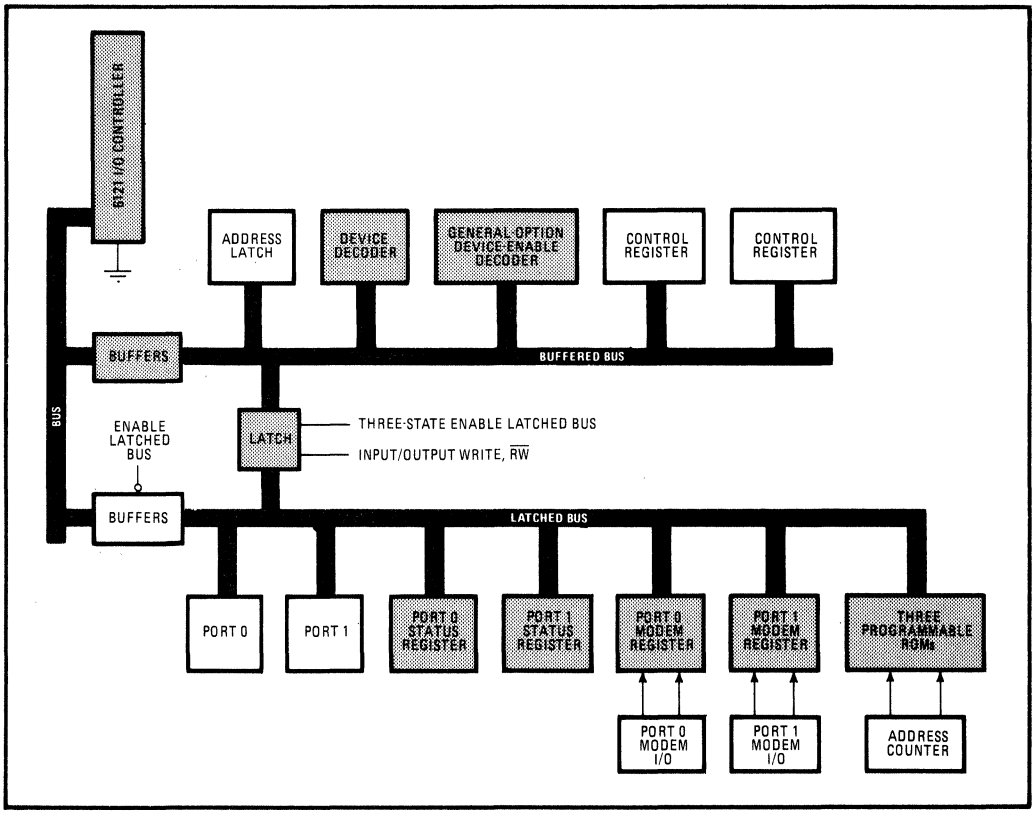
Smaller package

The new chips allow the microprocessor and its main memory to fit on a single board. The equivalent ICs including the 6100 processor in the older WS78 occupy three larger boards and one slightly smaller one. The number of 14-pin–chip equivalents was reduced from 375 in the WS78 to 200 in the DECmate. The 80% net reduction in board area stems in part from the use of large-scale integrated circuits, the other factors being the combining of the terminal and central processors that were separate in the WS78 and the tighter board layout possible with improved printed-circuit boards.

The almost 50% reduction in chip population increases long-term reliability because it reduces the total number of gold-wire bonds subject to temperature cycling and possible failure. Equally important is the massive switch to cool-running, low-power C-MOS. The temperature rise on such a die is only about 25% above the ambient temperature, while the rise on a similarly sized TTL or n-MOS die is roughly 100%. In the latter case, then, a much greater temperature strain is imposed on wire bonds and metal lines, as well as on the IC devices themselves.

Like any MOS part, a C-MOS IC is self-limiting—circuit currents drop as temperature rises. In TTL parts, higher temperatures result in increased currents—which can ultimately lead to cyclic degeneration or thermal runaway. Since C-MOS runs cooler than other MOS technologies, the resultant parts offer a more generous temperature safety margin.

Through the use of static C-MOS logic in the 6121 I/O controller, board space and power were saved again. Because the 6121 spends much of real time in an inactive state, dynamic logic would have required a good deal of refresh circuitry either on the chip or in discrete logic. The three 40-pin 6121s perform I/O control for five



3. C-MOS to the rescue. When the DP278 communications controller for the DECmate was using too much power, consumption was cut from 6 to 4 watts by using the C-MOS 6121 I/O controller chip and replacing 16 TTL chips with 14 C-MOS chips (tinted).

channels each. They are programmable, so the board designer has more flexibility in establishing channel characteristics.

C-MOS logic also offers reduced ringing and overshoot—a cleaner signal that is especially valuable on a bus. There tend to be fewer difficulties with electromagnetic and radio-frequency interference—a point that has increased importance today in view of the new Government emissions regulations on office equipment. The noise margins offered by C-MOS are superior to those of TTL, there being a wider tolerance for noise introduced between the maximum input and output low voltages: 1.4 V versus 0.4 V. Similarly, a C-MOS receiver has a high-voltage margin of 1.4 V versus 0.4 V.

Little watts

Low power consumption, chiefly as a means of optimizing reliability, was, from the beginning of the design effort, a principal reason for specifying C-MOS in both custom and off-the-shelf parts. Whenever off-the-shelf C-MOS chips were available, they were used in preference to their TTL counterparts for bus buffering, special hardware registers, and dedicated address decoding. In general, this reduced system bus noise and power requirements.

The system power requirements were set at a low enough level so as to ensure reliability within a convection-cooled terminal housing. An important design goal was as small a power supply as possible, while maintaining the ability of adding options. A 60-W supply is used, requiring 75 W from a wall outlet. As a comparison, the WS78 used somewhat over 200 W.

Well into the design effort, the small power supply, coupled with a fixed power allotment for the processor board and any further options, necessitated a very limited power allotment for the DP278 communications-control optional board. The DP278 was originally designed in n-MOS (four ICs) and 7400-series TTL parts to minimize cost. The TTL, however, caused the module's power requirement to be 50% over its allotment. So in the 10 functions shaded in Fig. 3, C-MOS parts were used to cut the projected power to 4 W at 5 V dc. Replacing 16 TTL chips were 14 C-MOS equivalents—about 19% of the module. □

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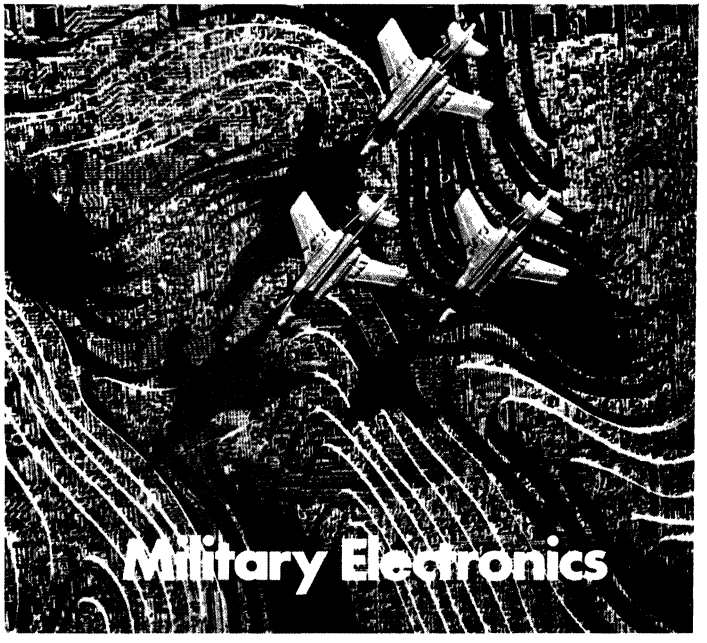
For many data-communication tasks, commercial or military, a programmable Manchester encoder-decoder circuit has the edge over UARTs or protocol controllers.

For data-comm links, Manchester chip could be best



Although there are many LSI chips for interfacing computers, terminals, and other subsystems with serial data-communication links, in many applications the programmable Manchester encoder-decoder offers significant advantages over the other chips. These advantages become apparent when comparisons are made at the system level.

The list of competing circuits includes universal asynchronous receiver-transmitters (UARTs), multiprotocol controllers (such as those for various levels of data-link control), and several types of encoders and decoders. But it is often difficult to compare capabilities at the chip level because of the chips' different natures. Performance must therefore be compared at the system level, taking into account the required throughput, accuracy, and communication protocols.

In many situations, such analysis shows that programmable Manchester encoder-decoder circuits have higher data rates, overhead efficiency, and accuracy. Unlike other controller chips, however, these devices do not perform serial-to-parallel or parallel-to-serial data conversion. Also, additional circuitry is needed to implement some standard data protocols, thereby making them less cost-effective in those applications.

The Harris HD-15531 aptly illustrates the capabilities of systems built with a Manchester encoder-decoder chip. Originally aimed at military applications (see "Interfacing with a Military Data-Comm Bus"), the 15531 is sufficiently versatile, thanks to its programmability, to compete with UARTs and multiprotocol controllers in a wide range of commercial applications as well.

It is built with CMOS technology and comes in a 40-pin package. Capable of data rates up to 2.5 Mbits/s, the 15531 has power dissipation of only 50 mW. As a transmitter, it encodes nonreturn-to-zero code into Manchester code; as a receiver, it decodes the Manchester back into NRZ. The data word length is programmable from 2 to 28 bits.

Other programmable characteristics include parity polarity and synchronous/asynchronous clock operation. Independent encoder and decoder sections on the chip allow full-duplex data communication.

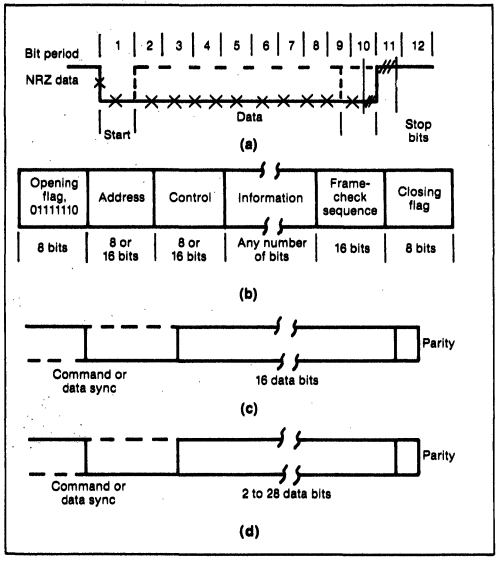
Lester Sanders, Member of the Technical Staff
Harris Corp., Semiconductor Digital Products Division
P.O. Box 883, Melbourne, Fla. 32901

Also available are lower-cost preprogrammed versions (the HD-15530 and HD-6408) in 24-pin packages.

Speed without sacrificing accuracy

The goal in data-communication systems is maximum throughput combined with maximum accuracy. But there are several conflicting tradeoffs. First, a need for extreme accuracy tends to restrict the throughput. Then, too, throughput depends on both the data rate and the overhead efficiency. Finally, overhead efficiency relates directly to the communication protocol employed.

Therefore protocol and data rate are used to measure the effectiveness of data-communication ICs. The most popular LSI circuits for data communications are UARTs and data-link control chips. Some UARTs operate at up to 500 kbits/s, but most work in the 40-to-50-kbaud range. Similarly, some data-link controllers operate at up to 2 Mbits/s, but 1 Mbit/s is more typical. With a maximum data rate of 2.5 Mbits/s, the 15531 clearly outpaces both UARTs and data-link controllers on the basis of data rate alone. However, the questions of communication protocol and overhead efficiency remain to be resolved. In many cases the 15531 will offer further advantages in those areas.



1. The data formats of UARTS (a), protocol controllers (b), and Manchester encoder-decoders (c and d) differ vastly, each offering advantages for different applications. The HD-6408 and HD-15530 (c) have a fixed, 16-bit word length, whereas the HD-15531 (d) has a programmable word length.

Since accuracy should not be sacrificed to achieve throughput, the synchronization schemes used by the various data-communication circuits must be considered. Synchronization is the key to accurate reception of incoming data. Because they transmit data in Manchester code rather than NRZ, Manchester circuits are better at synchronization than UARTs and DLCs. Also, the 15531 establishes synchronization by recognizing a 5-bit sequence, and its relatively powerful error detection circuitry further enhances accuracy.

Manchester code offers other useful advantages in addition to reliable synchronization (see "Manchester Code Gaining on NRZ"). For one, it is self-clocking, so that a wire for the clock signal is not needed, thus reducing transmission-line costs. In addition the Manchester code has no dc or low-frequency components in the waveform; therefore signals can be ac-coupled with transformers or capacitors, thereby lowering system costs, and in some applications avoiding errors or failure caused by interference.

Protocols and data formats

Usually, system designers select data-communication ICs primarily on the basis of the data structure used in a particular application. For example, UARTs and programmable Manchester circuits transmit data asynchronously (though synchronous operation is possible with the 15531), whereas data-link controllers send data synchronously.

A data-communication protocol is the implied set of rules that establishes communication between a transmitting and receiving station. The information structure in any serial data-communication scheme includes both control information and data. The control information performs such functions as delineating data, defining the amount of data to be transmitted, providing the addresses of the transmitting and receiving stations, and error handling. Figure 1 compares the data formats of UARTs, the DLC circuits and the 15531.

UARTs have programmable data formats. They frame from 5 to 8 data bits with 2 to 4 frame bits, using start and stop frame bits to define the beginning and end of a character. A programmed parity bit can provide error detection.

In data transmission, those bits that are not data are considered to be overhead, and overhead efficiency is a measure of the amount of data contained in a message. To calculate the typical overhead efficien-

cy of a UART, assume that a 7-bit ASCII character is transmitted and that the UART is programmed for a parity bit and one stop bit. Thus, including the start bit, 3 control bits are used in a 10-bit frame, for an overhead efficiency of 70%.

With the 15531, the length of the transmitted character is also programmable—in this case, from 2 to 28 data bits. A 3-bit synchronization pulse and a parity bit frame the data word. The 3-bit sync pulse is an invalid Manchester pattern generated by the encoder and recognized by the decoder. The sync pattern consists of 1½ bits in one state followed by 1½ bits in the opposite state. (As will be shown later, this particular pattern has definite advantages for synchronization.) The use of 3 bits plus parity means that 4 overhead bits are required to send as many as 28 data bits—yielding an overhead efficiency of 87.5%.

Data-link, or multiprotocol, controllers typically generate such bit-oriented protocols as Synchronous Data Link Control (SDLC), High-level Data Link Control (HDLC), and Advanced Data Communications Control Procedure (ADCCP). These protocols frame blocks of data with byte-wide or multibyte-wide fields like preframe sync, address, control, cyclic redundancy check (two bytes), and post-frame sync so that six control bytes are required to send a data field of 0 to 256 bytes (extended with HDLC and ADCCP). Therefore the overhead efficiency of multiprotocol controllers ranges from zero to nearly 98%. Table 1 compares the overhead efficiencies and other important characteristics of all three types of data-communication circuits.

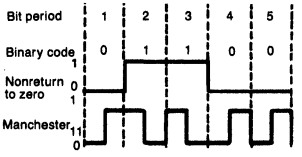
Arbitrarily sized gaps between characters occur

Manchester code gaining on NRZ

Although nonreturn-to-zero (NRZ) code is still the most widely used in data-communication systems, Manchester code is gaining ground rapidly. Already it is extremely common in magnetic tape recording and fiber-optic communication systems. More recently, it has gained support for serial data communications. The Ethernet office network—supported by Xerox, Digital Equipment Corp., Intel, Hewlett-Packard, and others—specifies Manchester phase encoding. Also, MIL-STD-1553 specifies Manchester code for an avionics data bus (see "Interfacing with a Military Data-Comm Bus").

Strictly speaking, the coding scheme referred to as "Manchester" should be called "Manchester II," as it differs from the original Manchester code, which is almost never used today. Also known as biphase-L, Manchester code is distinguished from NRZ and others by a transition at the center of each data cell.

The diagram compares NRZ and Manchester codes for the binary expression 01100. Note that the NRZ version represents the binary value with a static level throughout a bit period—where a binary 0 is a low logic level and a binary 1 is a logic high. Manchester code, on the other hand, has a logic



transition at the middle of each bit period. The binary value of data is represented by the direction of the transition: a high-to-low midbit transition represents a logic 1, and a low-to-high represents logic 0. The midbit transition represents both the data and the clock. Because the clock and data are included in a single serial data stream, Manchester is known as a self-clocking code.

Note that with NRZ code, only one symbol (1 or 0) is required to represent a data cell. Therefore the data transfer rate is the same as the information rate. With Manchester, however, two symbols are needed for each cell. That means that a modulation rate twice that of NRZ is needed to transmit the same amount of data—a possible drawback in bandwidth-limited communication channels.

The advantages of Manchester code include self-clocking, inherent error detection, and the absence of a dc component—which allows ac coupling. NRZ, however, requires no additional encoding or decoding, and it makes the most efficient use of a communication channel's bandwidth. Another advantage of NRZ is that it is supported by a wide range of ICs. However, the introduction of Manchester LSI chips, such as the HD-15531, signals increasing support of Manchester code by semiconductor companies.

with asynchronous data transfer. Typically such transfer occurs when a human-operated peripheral, such as a keyboard, interfaces with a computer; the interval between characters is arbitrary. In contrast, with synchonous data transfer the characters are transmitted contiguously. Synchronous data transfer occurs typically in computer-to-computer interfaces. Although there are exceptions, UARTs are traditionally used for asynchronous data transfers, and protocol controllers for synchronous data. Usually—but not necessarily—synchonous data transfer is faster than asynchronous.

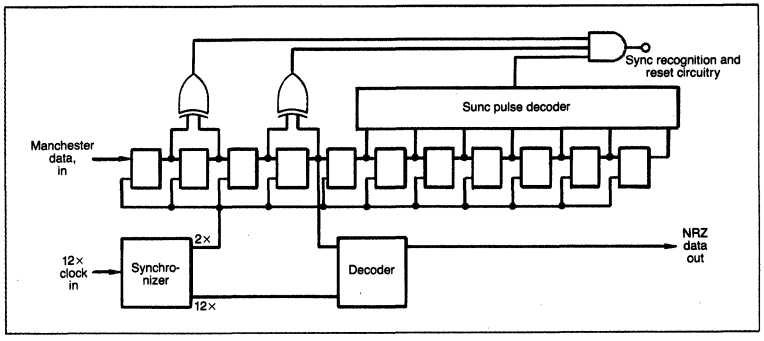
In many situations, however, both UARTs and data-link chips are limited in speed, overhead efficiency, or both. UARTs, especially, lack the throughput needed for the more demanding data networks. Data-link controllers, on the other hand, have excessive overhead when single characters are transmitted, because, as explained, each frame has an overhead of six bytes, even if the frame length is only one or a few bytes.

As an example of the limitations of protocol controllers, consider systems for process control or data acquisition. Typically, such systems have many remote stations sending data to a primary computer. At the remote stations, input or output devices (such as temperature sensors) communicate a single 8-, 10-, or 12-bit word through analog-to-digital or digital-to-analog converters. With a protocol controller, however, the fixed-format frame would require the opening and closing flags and the address, control, and CRC fields—clearly inefficient for transmission of a single character.

A programmable Manchester circuit like the 15531 is much better suited to process-control applications. In addition to providing high data rates, it has a programmable data format, which can be useful for interfacing with a-d and d-a converters. For example, the programmable character length makes it easy to upgrade an 8-bit conversion system to, say, 10- or 12-bit resolution. In contrast, UARTs are limited to 8-bit characters and are therefore difficult to operate with 10- or 12-bit converters.

Protocol requirements are satisfied with various degrees of completeness by available data-communication circuits. UARTs merely provide a frame for the character, plus bits for framing and parity error checking. Protocol controllers provide somewhat more, using established fields to facilitate data communication. For example, the address field defines the address of the remote station for which the data is intended, and the control field defines the nature of the transfer. Both types, UARTs and protocol controllers, perform the parallel-to-serial and serial-to-parallel conversions needed for computer interfacing. In addition, most protocol controllers provide address recognition.

Several of the 15531's functions prove useful in generating a protocol. The Sync Select input, for instance, allows the polarity of the synchronization pulse to be selected at the encoder. Since this polarity is subsequently recognized by the decoder, it provides



2. Two sections of the 15531 decoder circuitry play a role in synchronization. The synchronizer detects signal edges and operates at 12 times the data rate, and the synchronization-pulse recognizer detects specific patterns.

Interfacing with a military data-comm bus

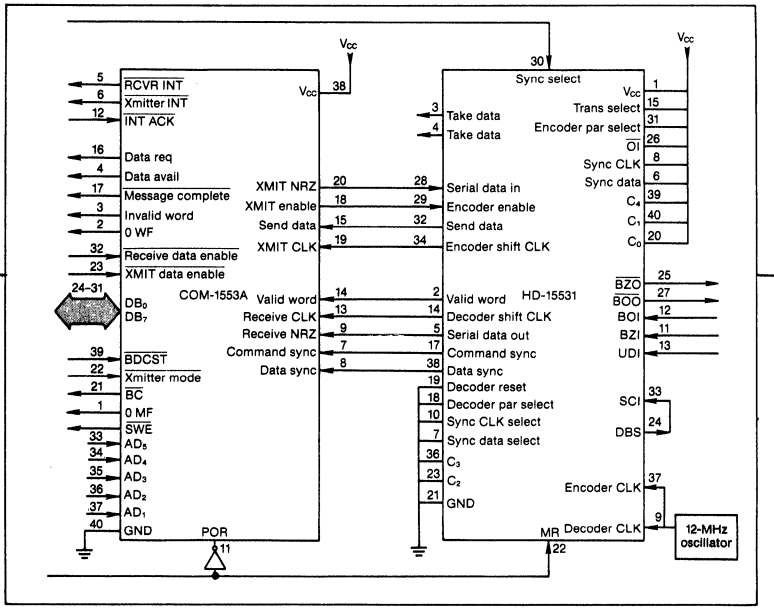
The HD-15531 Manchester encoder-decoder was developed originally for military applications. Specifically, it was designed to meet MIL-STD-1553A, a time-division–multiplexed bus for military aircraft.

Manchester code brings several important benefits to military avionics. For example, because it is self-clocking, it allows serial data transmission over a single twisted-wire pair, thus minimizing weight and space requirements. Also, accurate synchronization and simplified error detection enhance system reliability, so that the technique can safely be used for aircraft instrumentation and control signals. In addition, unlike signals resulting from other coding schemes, Manchester signals can be ac-coupled, allowing the use of transformers and simplifying the design of fiber-optic transmission systems. In turn, the isolation provided by transformers or fiber-optic cables minimizes interference from other electrical systems.

Of course, the 15531 and other ICs designed for MIL-STD-1553B meet the temperature and other environmental requirements of military systems. The military standard provides a 1-MHz data-communication channel, so that real-time control is achieved even when many signals are multiplexed.

Companion ICs for the 15531 are available from Standard Microsystems Corp., Circuit Technology Inc., and ILC Data Device Corp. The figure shows the connections when the 15531 is used with a UART from Standard Microsystems. The COM-1553A SMART (synchronous-mode avionics receiver-transmitter) converts parallel data into serial form and vice versa, recognizes addresses, and counts words for error detection. Also, it provides a convenient interface with a microcomputer or other controller via an 8-bit data bus. As can be seen, in the figure, the two chips are extremely compatible.

To read or transmit the control and data words, two read or write pulses must be generated to the Read Data Enable or the Write Data Enable pin respectively. Connections to the data-communication bus are from $\overline{BZO}$ and $\overline{BOO}$.



a way to distinguish between two types of words in the communication between the transmitting and receiving stations. Then, for example, the transmitter can generate a command sync pulse to indicate to the receiver that a particular word contains address and control information. Similarly, a data sync denotes a data word.

Techniques for synchronization

To compare the accuracy of a UART and the 15531, it is necessary to understand how the two circuits synchronize with data. Typically, a UART employs a clock rate of 16 times the data frequency to synchronize with incoming data. The stop bit from the transmitter has a high logic level, and the gap between words (known as the idle state of the line) also is high. The start bit is a low level for one bit cell. To detect this bit, the receiver recognizes a high-to-low-level transition of the input (from the stop bit or idle state). The receiver then verifies the start bit in two steps: by counting eight cycles of the 16× clock to reach the center of the start bit and by checking to make certan that the start bit is still low. If the sample yields a high logic level, the receiver knows that the start bit is false. It then continues to look for a high-to-low transition. Thus synchronization with a character is initiated on the basis of two states.

Two sections of the 15531's decoder are involved in the synchronization: the synchronizer and the sync-pulse recognizer (Fig. 2). The former includes edge-detection circuitry, and its clock frequency is 12 times the data rate. The latter can detect a particular type of data pattern that is 5 bits wide. The pattern consists of 1½ data cells at one logic level, followed by 1½ data cells at the opposite level, followed by two valid Manchester bits (Fig. 3). A valid Manchester bit is defined as one with a midbit transition, and it is detected by the Exclusive-OR gates shown in Fig. 2.

Although the synchronization scheme of the 15531 requires three bits of preframe sync, as opposed to a UART's single bit, it checks a total of 10 states for synchronization. Therefore synchronization is much more reliable with the 15531 than with a UART.

Manchester code has a transition in the center of a data cell, and depending upon the data pattern, it also may have a transition at the beginning of the data cell. Transitions not only determine whether the data is a logic 0 or a logic 1, they also provide references to which the decoder can synchronize. Unlike UARTs, which synchronize only at the beginning of each character, the 15531 synchronizes with each transition. After it has been reset, the decoder needs to know when to sample the logic state of the data. The optimum time to do that is midway between the data transitions, because this allows time for the signal waveform to settle from the rise and fall times.

Since transitions in Manchester code occur at the beginning and center of the data cells, the sample points should be one-quarter and three-quarters of the way through the data cell. A transition detector, a counter, and logic circuitry team up to locate the required sampling points. With a clock of 12 times the data rate, the decoder counts to 3 to find the one-quarter data-cell point and to 9 for the three-quarters data-cell point. For resynchronization, the algorithm is reset at each transition—which occurs once or twice in each data cell. Thus synchronization of the 15531 is far superior to that of a UART, which synchronizes only once per character. With the 15531, sampling error does not accumulate over adjacent data-bit cells, whereas it does with UARTs.

Interfacing with a serial data bus

The 15531 performs word framing, error checking, and Manchester encoding and decoding for a serial interface. It interfaces with a serial bus in either a single-ended or a differential format. Because the circuit receives and sends NRZ serial data, parallel-to-serial and serial-to-parallel shift registers are needed to communicate with computers, which operate on parallel data.

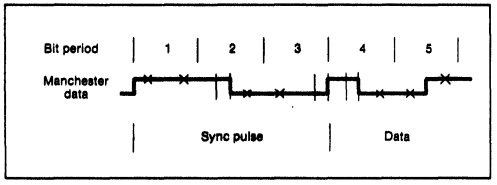
To interface with a 16-bit parallel data bus, two

Table 1. Comparing data-comm circuits

	UART	Protocol controller	Manchester encoder-decoder
Maximum data rate	50 kbaud	1–2 Mbaud	2.5 Mbaud
Overhead efficiency	70%	0–97%	80%
Error detection	Parity, framing	Cyclical redundancy check	Bit count, parity, valid Manchester
Code	NRZ	NRZ, NRZ-1	Manchester
Disad-vantages	Poor throughput for large blocks of data	Inefficient overhead for character transmission	Requires shift registers

74C165 shift registers can be used (Fig. 4). The 15531 strobes the CLK inputs of the shift registers with the NAND product of the Send Data and Encoder Shift Clock outputs. The parallel inputs are loaded just before Send Data goes high, which happens after the sync pulse has been shifted out of the encoder (it returns low before the parity bit is generated). When Send Data is high, NRZ data is shifted into the chip.

To transmit a word, the controller or microcomputer must apply a high logic level to the Encoder Enable input of the 15531. If this line stays high, so that contiguous words are transmitted out of the encoder, the only gap in the NRZ data is the 3-bit sync pulse and the parity bit. As noted, the type of word transmitted (control or data) is selected with the Sync Select input.



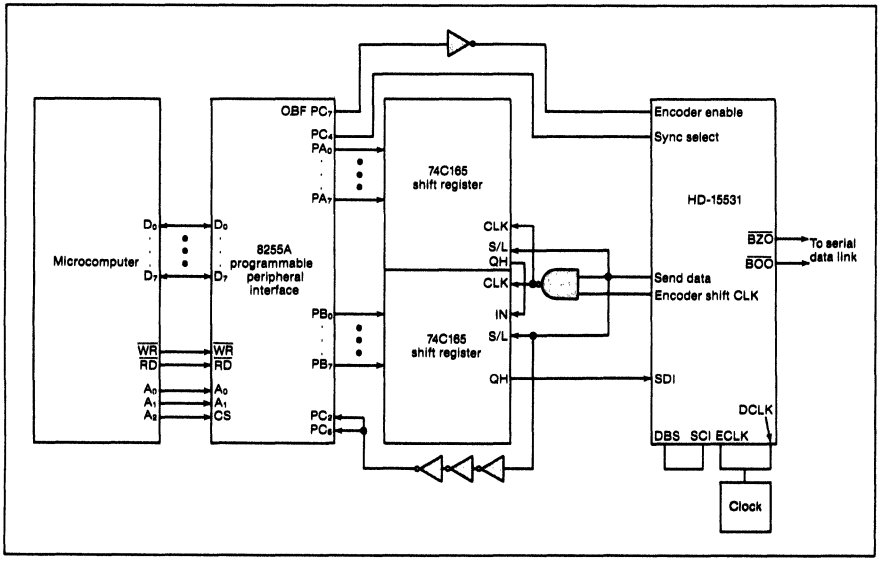
3. For synchronization, the decoder section of the 15531 samples at 10 points to recognize a pattern that has a total length of 5 bits. The pattern has 1½ bits at one logic level, followed by 1½ bits at the opposite level, and culminates with two valid Manchester bits.

An example of how the 15531 interfaces with a controller for use as a transmitter, with the help of an Intel 8255A programmable peripheral interface (PPI) chip, is shown in Fig. 4. A general-purpose I/O device, the 8255A has 24 I/O pins that can be configured for any of three modes of operation. An 8-bit data bus allows it to be connected directly to a microcomputer. The microcomputer selects the operating mode and defines the port directions with commands via the data bus.

In Mode 1, used in this example, the 24 I/O pins of the 8255A are configured as two 8-bit data ports and one 8-bit control and status port for handshaking operations. The data ports, Port A and Port B, interface directly with the two parallel-to-serial shift registers.

Operation as a transmitter

To transmit, the microcomputer generates a write signal to the 8255A, which then sends an Output Buffer Full (OBF) signal to the Encoder Enable input of the 15531. One of the two programmable I/O pins (PC_4 in this case) controls the polarity of the sync pulse to define the type of word transmitted. If desired, the Send Data output of the 15531 can be used to acknowledge the transmission of a word. When Send Data returns low, the microcomputer can generate another word. The 15531 transmits Manchester code onto the serial bus as logical complements at the Bipolar Zero Out ($\overline{BZO}$) and Bipolar



4. The transmitter section of a terminal based on the 15531 includes 74C165 shift registers to convert parallel signals from the controller into serial data for the Manchester encoder. An 8255A programmable peripheral interface buffers the processor to minimize system overhead.

One Out ($\overline{BOO}$) outputs.

To provide a 16-bit parallel word when the 15531 is operated as a receiver, the Serial Data Out (SDO) pin of the 15531 is connected to a pair of cascaded 74C164 serial-to-parallel shift registers (Fig. 5). The Take Data (TD) and Decoder Shift Clock (DSC) outputs of the 15531 are ANDed and used to strobe the shift registers. The Valid Word (VW) signal goes high approximately half a clock cycle after the final bit in a word is shifted out, and the latter action is indicated when TD returns low. The parallel data from the 74C164s must be latched to define the beginning and end of the word.

To operate the 15531 as a receiver, a second 8255A is used, as shown in Fig. 5. As with the transmitter subsystem, the 8255A is configured in Mode 1. Once again, Port A and Port B serve as the interface with the data bus, and Port C provides the necessary handshaking signals between the 15531 and the microcomputer. A signal into the $\overline{STB}$ pin latches the data word into the 8255A. The 8255A subsequently outputs an Input Buffer Full (IBF) signal and follows with an Interrupt (INT) signal.

Depending on the required functions, the receiver interface has a variety of possible forms. Many of the functions can be provided by either hardware or software. One hardware/software tradeoff concerns address recognition. If no external address-recognition circuitry is provided, the 15531 must interrupt the 8255A with the reception of every control and data word on the data bus. That will require that the microcomputer read each control word to find the terminal for which the message is intended. Of course, regardless of the address-recognition scheme used, the data words following another station's message should be ignored.

The system shown in Fig. 5 includes hardware that provides address recognition for one of 16 terminals. The VW output of the 15531 latches data into the 82C82 CMOS octal latching bus drivers. Hard-wired inputs, b_0-b_3, of a 7485 magnitude comparator define the station's address. The receiving terminal's corresponding address on the data bus is input a_0-a_3. If these inputs match the hardwired inputs, the signal a = b goes high.

The 7485 has no way of distinguishing between control and data words. Therefore, since a data word may contain a pattern that arbitrarily reproduces a terminal's address, the a = b output is NANDed with the VW and CMD SYNC outputs from the 15531. The CMD SYNC output must be latched, because it returns low before VW goes high. For a serial bus

Table 2. Control codes for a network protocol

Control field	From	To	Control command
0 0 0	Primary	Remote terminal	Transmit a character to the primary; message poll
0 0 1	Remote terminal	Primary	Transmit character feedback; remote terminal has message to transmit
0 0 1	Primary or remote terminal	Remote terminal or primary	Receive the following message
1 0 0	Primary or remote terminal	Remote terminal or primary	End of message—from originating to receiving remote terminal
1 0 1	Primary or remote terminal	Remote terminal or primary	Message error; retransmit—from originating to receiving remote terminal
1 1 0	Primary or remote terminal	Remote terminal or primary	Acknowledge valid message—from receiving to originating remote terminal
1 1 1	Originating remote terminal	Primary	Message transfer is complete; bus is free

with more than 16 terminals, 7485s can be cascaded to provide the expanded address recognition.

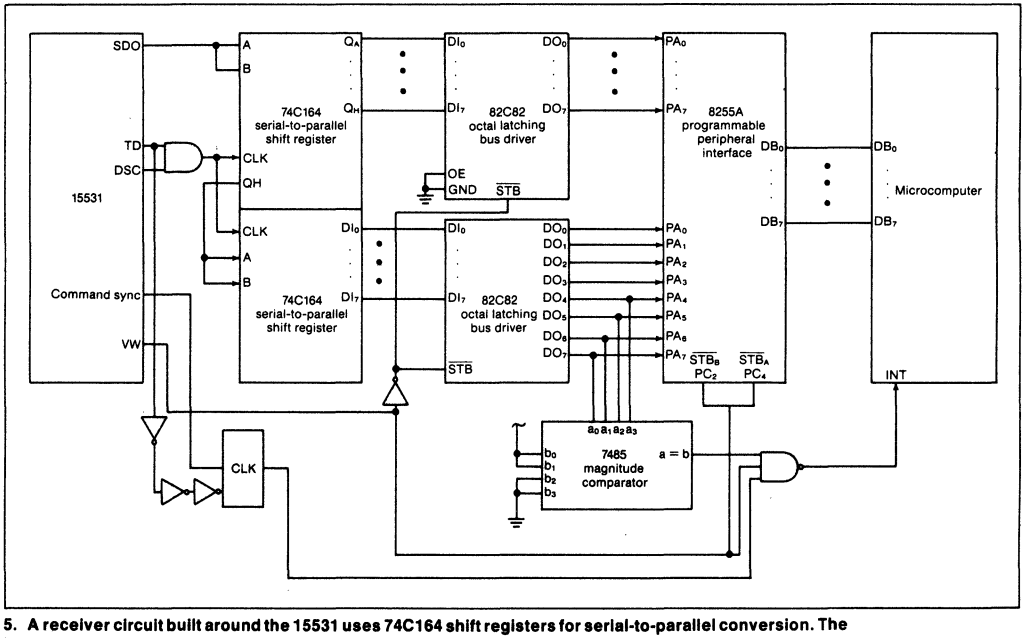
Some functions, however, are usually better served by software than by hardware. One such function is the word count of the message length. The transmitting station generates a word that contains the message length—that is, number of words in the message. To ensure that the message is transmitted and received accurately, the receiving station counts the Data Sync outputs and matches the total with the transmitted word count. (If the 24-pin Manchester chip, the HD-6408, is used, the Data Sync output is multiplexed with the Command Sync output. Therefore Take Data can be Exclusive-ORed with the Command/Data Sync output to provide the word count.)

For interfacing with a microcomputer or controller with a 16-bit data bus, a different design is appropriate. This scheme, too, uses two 8255As in Mode 1. But instead of dedicating one 8255A to transmission and the other to reception, it uses the A ports of both 8255As to transmit and the B ports to receive. As before, the C ports provide the control and status functions for handshaking between devices. The modified bus structure allows reading or writing of the 16 data bits in a single operation.

Distinguishing control information

As shown earlier, the 15531 generates and detects programmable sync pulses that can be used to tag different types of information. Thus the chip generates and recognizes two types of words: control and data. To communicate control information between transmitting and receiving stations, specific meanings must be preassigned to various bit combinations. That, of course, must be done as part of the system design.

To illustrate the design procedure, consider a multidrop serial data communication network. The system will handle both asynchronous character transfers (such as instrumentation data) and block messages. Basically, the system consists of a single primary station and a user-definable number of remote terminals. For simplicity, just one primary



5. A receiver circuit built around the 15531 uses 74C164 shift registers for serial-to-parallel conversion. The 82C82 latching bus drivers and the 7485 magnitude comparator provide hard-wired address recognition. As with the receiver, an 8255A acts as the interface to the controller.

and two remote stations will be used as a design example. In an actual system, of course, the programmable word length of the 15531 specifies the number of stations addressed and the control messages. For the initial design, the length of a control word will be fixed at 16 bits.

Assume now that the control word is divided into three fields, each of which plays a role in the protocol of the data-communication network. For this example, the first six bits of the control word give the address of the station transmitting the control word, the next four bits form the control field, and the last six bits provide the address of the intended receiving station. With such an arrangement, the number of possible stations that can be addressed is 2^6, or 64, and the number of control commands that can be issued is 2^4, or 16.

The system uses a primary terminal to poll remote terminals for a character feedback—such as a temperature reading for an energy control system. At the same time, it provides for block data transfers, such as messages. Actually blocks are not transferred synchronously, as with a protocol controller. However, the higher data rate and overhead efficiency of the 15531-based system yield higher overall throughput than is possible with systems with conventional block transfers.

The system has the following protocol: First, the primary station polls the first remote terminal, requesting a character feedback. The control field contains a control code that indicates the type of data transfer. Then the remote terminal responds with a control word, which verifies its address, and a control field, which indicates whether or not it has a message to transmit. In either case, the terminal subsequently transmits a data word—which is the single-character feedback. The primary terminal receives this character and stores it in memory. Depending upon the response of the remote terminal to the message poll, the primary performs one of two options. If the remote terminal did not have a message, the primary proceeds to poll the next station, for the character feedback and message flag. If, on the other hand, the remote terminal indicates in its control-word response that it has a message to transmit, the primary idles and relinquishes control of the bus.

Control codes give commands

The primary terminal's receiver remains active because it, as well as remote stations, can receive messages. Message transfer can take place from any terminal, primary or remote to any other terminal. The message need not go through the primary. To transfer a message, the first remote terminal generates a control word with the same format as a primary's control word.

The control code in the control field instructs the receiving station to "receive the following message." A list of control code commands is given in Table 2.

The receiving station identifies the source of a message by reading the address field of the control word. The originating remote terminal then transmits a special data word (the only data word that is used as a control word). Since in all other instances data words contain only data, this exception must be recognized by the controller software of the receiving terminal. This data word gives the number of words in the message. Were a control word used here instead of a data word, the arbitrary data pattern indicating the message length could trigger the address-recognition circuitry of another terminal on the bus. The address and control fields could be repeated, but this would mean that the message length, as defined by the word, would be limited to 2^6 characters—which is too short.

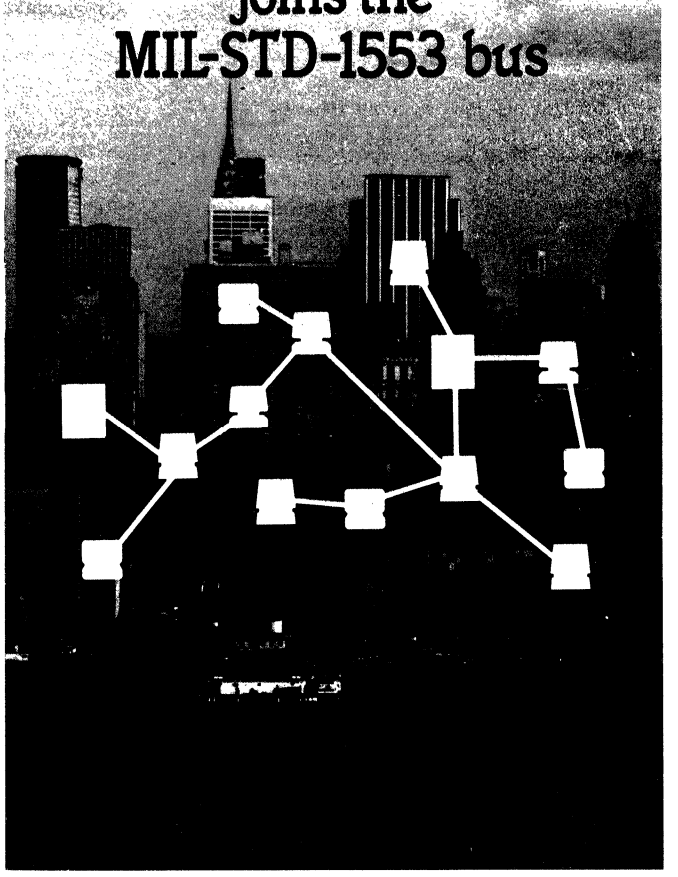
If there is a message, the first remote terminal transmits the message continuously. After completing the message, it transmits a control word in which the control code indicates "end of message." Upon receiving this word, the receiving terminal checks to see if the correct number of data words were received. Then it responds to the originating remote terminal with a control word indicating one of two responses.

If the receiving terminal did not receive the message properly (the number of data words does not equal the number indicated by the sending terminal), the receiving terminal indicates this with a "message error, retransmit" control code. When the originating remote terminal receives this code, it can go back several steps and begin retransmitting the message with the original control word. The number of retries should be limited by the sender's controller software.

If the message was received properly, the receiving terminal indicates that fact to the sender with the appropriate control code. When the latter receives the indication, it transmits a control word to the primary with a control code signifying that the message transfer is complete and the bus is free. Even if there is repeated failure to acknowledge the message, the originating terminal must indicate after the retries that the bus is free. The primary can then poll the next remote terminal.□

LOCAL NETWORKS

Industrial controller joins the MIL-STD-1553 bus



Based on low-cost, low-power CMOS circuitry, an industrial-grade local-area network controller brings high-speed data communications to the 1553 data bus.

David G. Williams, Member of the Technical Staff
Harris Corp., Semiconductor Group
P.O. Box 883, Melbourne, Fla. 32901

Protecting the integrity of information is the most important function of a data-communications system. One way to ensure secure data communications is to design the system's local-area network similar to the specifications defined in MIL-STD-1553. Originally intended for the high-noise environment of military aircraft, 1553's provisions are applicable to a variety of industrial and commercial systems that must provide high performance under adverse conditions (see "Riding the 1553 Bus").

To bring 1553's data integrity to nonmilitary applications, the network design must cost-effectively meet space, power consumption, and data-rate requirements. With these factors in mind, a CMOS network controller can be designed with the following features:

- A 1-Mbit/s data rate, upgradable to 2.5 Mbits/s
- An extremely low bit-error rate
- An operating power consumption of just 150 mW, including line drivers and receivers
- A bus length of 1000 ft (expandable)
- The use of low-cost, shielded-twisted-pair cable (15¢/ft per pair)
- A component cost of $60 per controller
- The use of multidrop topology
- Low chip count, using LSI technology

The block diagram of the controller is shown in Fig. 1. Its principal component is Harris Semiconductor CMOS HD-6408 Manchester encoder-decoder chip, which operates at data rates of up to 1 Mbit/s (ELECTRONIC DESIGN, Aug. 5, p.201). To obtain higher data rates—up to 1.25 Mbits/s—and

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Electronic Design • October 14, 1982

operation over the full military temperature range, the HD-6408 can be replaced by the pin-compatible HD-15530-8, which conforms to MIL-STD-883 specifications. If the application warrents the highest data rates—up to 2.5 Mbits/s—the HD-15531B can be substituted for the HD-15530-8.

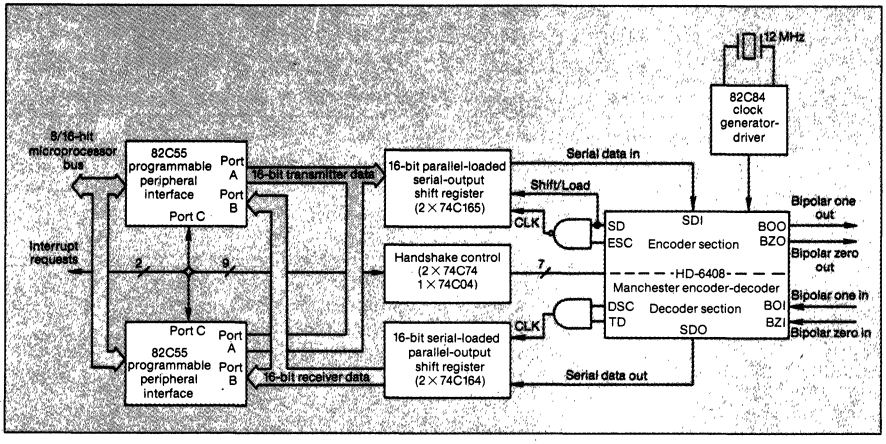
To interface the controller with virtually any 8- or 16-bit microprocessor, the design uses two 82C55A programmable peripheral interface chips. A CMOS functional equivalent of an original Intel part, it operates at much lower power levels and with far greater speed, thanks to circuit and technology improvements.

Selecting a suitable clock generator was one of the more difficult tasks in designing the controller. The HD-6408 requires a 12-MHz clock input which switches within 0.5 V of the power supply rails, and has both rise and fall times of 8 ns or less. An 82C84A CMOS clock generator-driver was chosen because it supplies a buffered clock output of up to 30 MHz when running from a fundamental, parallel-mode crystal and two capacitors. This device is another functional equivalent of an original Intel bipolar device, but being CMOS, it operates at a much lower power-supply current—about 1 mA/MHz.

Components that interface with the serial data bus play an extremely important role in the overall design. No matter how well the controller itself performs, the line driver-receiver and cable combination can create a bottleneck through which all data must flow. Consequently, deficiencies in interface design become a limiting factor in the controller's data throughput and integrity.

High data rates, long cable lengths, and low power consumption present a designer with conflicting requirements. Most conventional line drivers and receivers handle larger amounts of power than CMOS. To accommodate CMOS technology, the controller uses a so-called current-mode transmission system (see "Why Current-Mode Transmission").

Current-mode transmission was developed for space satellites, in which low-power drains and very low levels of radiated and conducted electromagnetic interference are mandatory. Basically, the technique



1. A self-contained local-area network controller for driving a data bus similar to the MIL-STD-1553 data bus with Manchester II data, this system runs at data rates of up to 2.5 Mbit/s and interfaces with most 8- and 16-bit microprocessors.

switches a constant current between each of two conductors in a twisted-pair transmission line. The total current in the pair remains constant and flows in the same direction for any transmission. Current flows through line-termination resistors and returns to the transmitter as a steady dc current on the transmission-line shield. The net effect is near-zero current through the complete shielded twisted pair, resulting in very low levels of EMI.

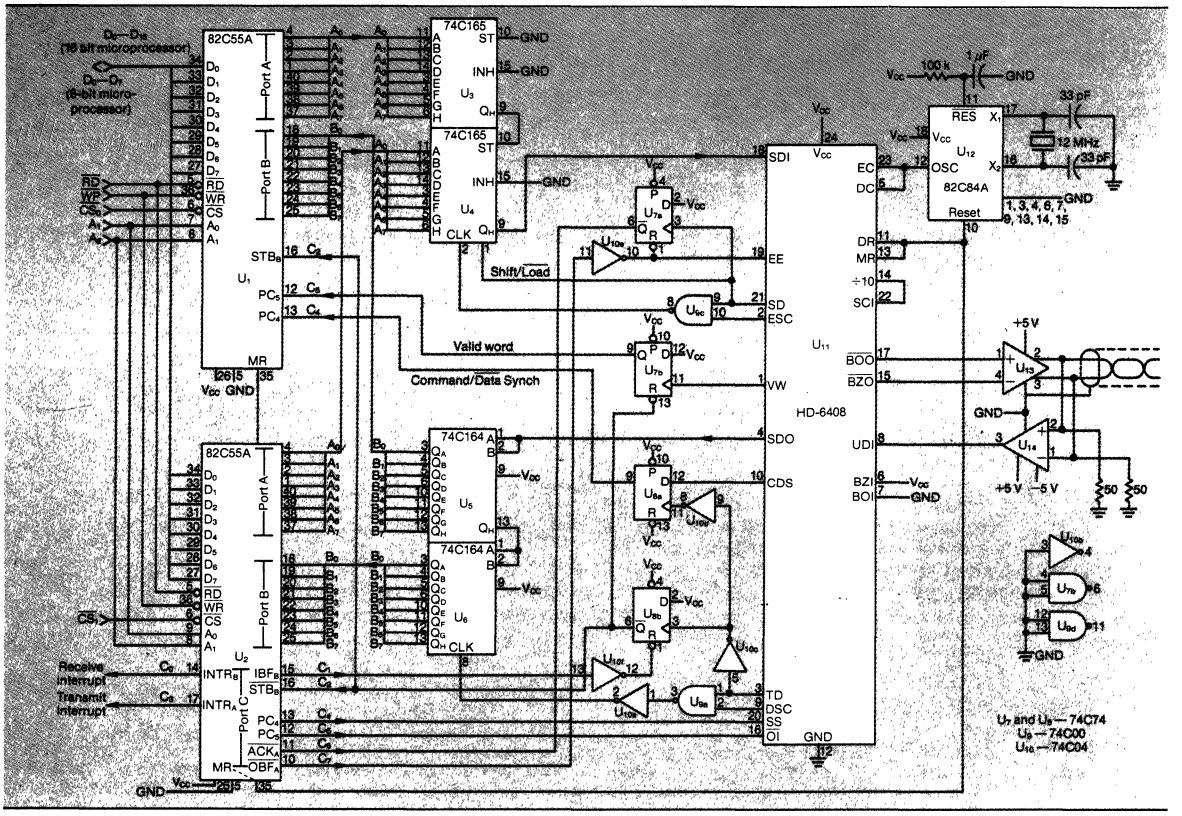
The major advantages of current-mode transmission are very low system power levels: typical dissipation is 25 mW when the system is active and 100 μW on standby, for a transmitter operating at a 1-Mbit/s data rate over a transmission line of 1000 feet or longer. Moreover, using multiple twisted pairs within the same shield is possible, since there are no high crosstalk levels like those common to differential-voltage switching systems.

As for CMOS, besides all the obvious advantages, there is another reason for its use. Because of CMOS's low power consumption, a sealed enclosure often becomes feasible. With strict FCC regulations governing allowable RFI emissions, sealing the box becomes important. Moreover, sealed enclosures are more suitable for the extremely hostile environments encountered in most military and some industrial applications.

Getting down to details

Figure 2 shows a complete schematic of the controller. The system interfaces with an 8-bit microprocessor by tying together the D_0–D_7 inputs of the 82C55As to form an 8-bit bus. These devices must be programmed individually to their mode 1, strobed I/O, configuration. A double-buffered interrupt-driven interface can then be achieved.

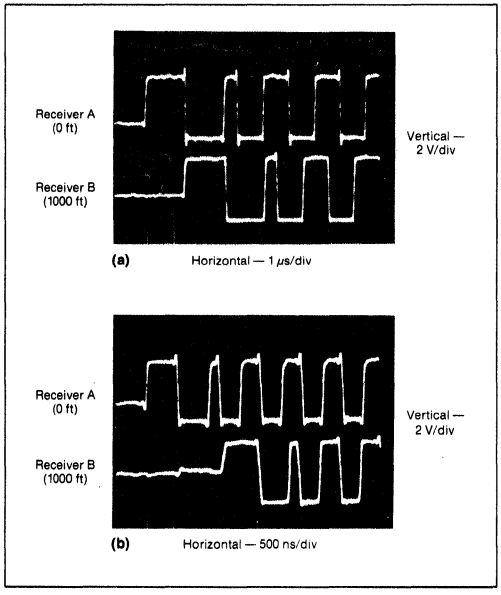
Port A of each 82C55A is programmed as an output port to supply data to the HD-6408 for subsequent



2. The complete schematic of the network controller shows a data-communications system designed around the HD-6408 Manchester encoder-decoder chip (U_{11}) and a pair of 82C55A programmable peripheral interface devices (U_1 and U_2). The system operates as both transmitter and receiver, and because the two functions are independent, it can be configured for either half- or full-duplex operation.

transmission. A pair of 74C165s (8-bit parallel-loading, serial-output shift registers) convert 16-bit transmission data from parallel into serial form. Bits 3, 6, and 7 of port C provide the handshaking signals for port A data.

When data is written by the microprocessor to port A, bit 7 of port C (C_7) goes low, producing an Output Buffer Full ($\overline{OBF}$) signal. Although this signal appears at the output of each 82C55A when data is written to them, only the $\overline{OBF}$ signal from the device containing the most significant byte of data is used —in this case, U_2. The reason is that all 16 bits of transmitted data must be available to the network controller before transmission starts. When data is written to the 82C55As, the least significant byte is written first, followed by the most significant byte.



3. Oscilloscope photos of the network controller's receiver output show waveforms taken at data rates of 1 Mbit/s (a) and 2.5 Mbits/s (b). Although distortion is slightly greater at the higher data rate, the difference is virtually insignificant.

The $\overline{OBF}$ signal controls the Encoder Enable (EE) input on the 6408. This signal prompts the 6408 to start transmission. Once transmission begins, the 6408 responds with a Send Data (SD) signal, which forms an acknowledgment (ACK) to C_6. The response resets $\overline{OBF}$ and prompts the 82C55A to issue a Transmit Interrupt signal from line C_3 to the processor's CPU. This signal informs the CPU that the transmitter is ready to receive another word for transmission. A double-buffered transmitter results that permits continuous data transmissions without interword gaps or idle time.

At a 1-Mbyte/s data rate, the CPU has about 16 μs in which to send a new data word without having any idle time. This is a relatively short response time for an 8-bit processor. An upgraded version of the controller would use a faster 16-bit microprocessor such as an Intel 8086 or a Harris CMOS 80C86. Under this condition, the D_0–D_7 inputs must be connected as a 16-bit bus (D_0–D_{15}) and simultaneous chip-selection signals (CS_0–CS_1) must be applied to both 82C55As.

The system can be upgraded further with a DMA controller, which lets the CPU spend more time on other processing tasks. But this addition is necessary only for high data-rate systems—lower data-rate systems operate satisfactorily without DMA or interrupt-driven schemes. In slower controllers, the interrupt outputs (C_0 and C_3) are unused, and the CPU can poll the status word of port C by reading the port.

The receiver operates much as does the transmitter and is likewise double-buffered. Since the receiver and transmitter are independent, the controller can be set up for either half- or full-duplex operation. The receiver circuitry ignores spurious data on the bus and begins its response sequence only on receipt of a valid sync character, followed by two valid Manchester II bits. This procedure is implemented with circuitry internal to the 6408.

After a validation sequence has occurred, the 6408 generates a Take Data (TD) signal, enabling the 74C164-based shift register to accept the Serial Data Output (SDO) of the 6408. The trailing edge of TD indicates that all 16 data bits have been transferred to the shift register and also serves to generate a strobe signal ($\overline{STB}$) for the 82C55As. $\overline{STB}$, C_2 causes the devices to load the received data into their port B inputs. Then the 82C55A responds with an Input Buffer Full (IBF) signal, which resets the $\overline{STB}$ line. The shift register is available immediately to receive the next 16-bit word. Since there is always a minimum time of four bit periods between data words—because of the parity bit and sync character —the design guarantees successful reception of so-called back-to-back data words.

$\overline{STB}$ also causes the 82C55A to generate a Receive Interrupt on the C_0 output. As in the transmitter, this interrupt can be either used directly or polled under software control.

The 6408 indicates acceptance of an error-free word by generating a Valid Word (VW) signal. VW is latched and presented to a spare input at C_5, and the microprocessor reads the bit to validate correct data. With a slight hardware modification, VW can be used to enable $\overline{STB}$, thereby reducing the required software and its overhead.

The 6408's error-detection circuitry checks every data bit for correct Manchester II encoding and also verifies correct parity. As a result of its composite error-detection algorithm, the chip detects 100% of three or fewer sampling errors in any data word. When more than three errors occur, the 6408 will correctly detect—on a statistical basis—better than 99.99% of all possible errors. Thus, at a system level, undetected errors occur five or six orders of magnitude less frequently than detected errors.

Two types of synchronization characters can be supplied by the 6408 to differentiate between command and data words. The Command/Data Sync (CDS) output reflects the reception of a command or data word based on the sync character. The signal is latched and presented to the spare input at C_4 of U1 and can be read under software control. Since the use of CDS depends on the application, it is employed at the designer's option.

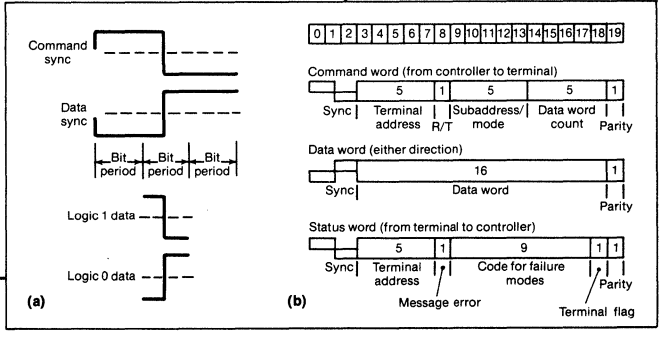
The 6408's transmitter section has two control signal inputs which connect to the spare port C outputs on U_2. Sync Select (SS) determines whether a command or data sync character is to be transmitted, and Output Inhibit ($\overline{OI}$) is a low-true signal used to put the $\overline{BOO}$ and $\overline{BZO}$ transmit-data

Riding the 1553 bus

MIL-STD-1553 defines a time-division–multiplexed data bus for use in military aircraft. The bus carries bipolar signals and uses a single twisted-pair shielded cable. Data going out on the bus is encoded in the Manchester II format. Under this system, no dc signal components appear on the bus. Thus transformer coupling is permitted, resulting in excellent isolation between data-handling systems and their environment.

The signaling format of 1553 is specified assuming that 32 or fewer terminals are managed by a central control unit that uses command words. Provision is made for dynamic reassignment of the control unit using the token-passing technique. Each word transmitted is preceded by a synchronizing pulse and followed by a parity bit, resulting in a total word time of 20 μs. The character and word formats of the MIL-STD 1553 bus are shown in Figs. A and B, respectively.

The HD-6408 Manchester encoder-decoder, which is the key component of the network controller, is designed to meet the requirements of 1553. At the same time, the CMOS device is flexible enough to implement other signaling protocols. The 16 data bits in both the 1553's command and data words are defined by the user and can be generated by the hardware-software combination in the network controller. For example, expanding the system to any number of terminals is possible by redefining the meaning of bit assignments within command words. Additionally, error codes can be deleted or expanded. By substituting the HD-15531 Manchester encoder-decoder for the HD-6408, additional user-defined features can be incorporated, such as expanding the word length of the bus to 28 data bits, if desired.



outputs in their inactive states (high). These signals are also application-dependent, and are therefore optional.

Evaluating controller performance

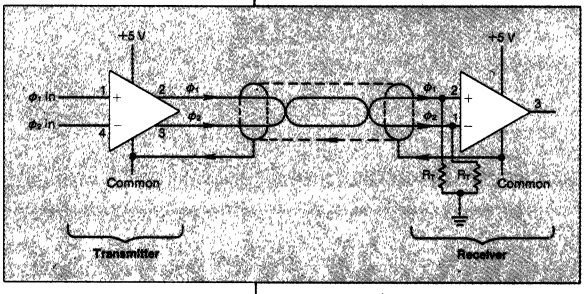
To check the controller's design, breadboards can be connected using Belden Corp. 9855 Twinaxial cable. This inexpensive high-performance cable contains two twisted pairs inside a common shield. The shield has both braided and foil conductors to ensure 100% coverage.

Tying the ends of two twisted pairs together at the end of a 500-ft length of cable produces an effective cable length of 1000 ft. This configuration is useful for observing the effects of possible crosstalk between adjacent pairs inside a common

Why current-mode transmission?

The two most common methods for transmitting digital information over wire are the RS-232 voltage mode and differential-voltage switching. A long-time industry standard, RS-232 can take the abuse that results when many different types of equipment are connected on its lines. But RS-232 is limited to systems working at low speed over short lines. Differential-voltage techniques overcome many of the limitations of RS-232, providing high-speed, long-line data links that have a high degree of immunity to externally generated noise sources.

Both RS-232 and differential-voltage switching have three drawbacks: they are high power consumers, generate crosstalk between adjacent lines, and produce noise in the form of conducted and radiated RFI. The relatively unknown technique called current-mode transmission can eliminate these drawbacks and works well over long lines.



A current-mode transmitter (left half) alternately applies current to each of two conductors (ϕ_1, ϕ_2) in a twisted pair. The total current is constant and always flows in the same direction.

A logic 1 is produced by line ϕ_1 conducting a certain current. This current travels down the transmission line, through a 50-Ω terminating resistor R_T (right half), and returns through the shield to the common point of the transmitter's power supply. A logic 0 results when the current is prevented from flowing in ϕ_1, and flows in ϕ_2. The shield carries the same dc current constantly, since lines ϕ_1 and ϕ_2 always conduct alternately.

Small variations in transmission-line current can occur if there is overlap between the turn-on and turn-off times of ϕ_1 and ϕ_2. However, the complementary outputs of the HD-6408 are designed for near-zero overlap.

With signal swings typically 20 times smaller than in differential-voltage systems, and with its nonsaturating current-switching transmitter producing smooth ramps without overshoot or ringing, current-mode transmission is far superior to differential voltage systems in limiting conducted and radiated RFI. The three types of externally generated noise that affect digital signal-line transmission are: magnetic and capacitive pickup from nearby electrical conductors, magnetic and capacitive crosstalk between transmission lines sharing a common shield, and ground-line noise between transmitter and receiver. Current-mode transmission combats the first two types of noise as well as or better than the other systems. The ground-noise problem is usually eliminated by avoiding ground loops as dictated by standard design practices.

shield. Current-mode transmission systems exhibit very low levels of crosstalk, thereby permitting multiple twisted-pairs within a single shield. Voltage-mode transmission schemes, on the other hand, may require separately shielded cables for long runs, resulting in much higher cable costs than in current-mode systems.

In an actual system, the additional twisted pair may be used as a secondary bus for higher system throughput or as a redundant bus to increase system reliability. Another option is to provide a full-duplex point-to-point data link.

A standard five-pin DIN shielded audio connector is an ideal low-cost method of connecting the breadboards to the 9855 cable. Its shielded shell provides adequate integrity for all but the most stringent requirements.

A complete 1000-ft cable running at a 1-Mbit/s data rate serves as a reliable data link and when tested produced no detectable transmission errors or crosstalk. The typical power consumption is 150 mW. By inserting a 30-MHz crystal at the 82C84A's input, the data rate can be increased to 2.5 Mbits/s. At this rate, some pulse distortion results because of inadequate gain of the simple low-power receiver used. Figure 3 shows oscilliscope photos taken at the receiver's outputs—note the slightly higher distortion in Fig. 3b compared with Fig. 3a. The problem can be solved by substituting premium transistors in place of the 2N4124s ordinarily used. An alternative solution to that is to replace the discrete line receiver with an industry-standard 75107 line receiver.

In a worst-case design, which accounts for temperature and voltage variations, the CMOS shift registers may be too slow at a 2.5-Mbit/s data rate. However, they can be replaced with fast new devices offered by several manufacturers without compromising the low-power aspects of the design.

Because of the design's low power dissipation, the components can be incorporated into a single module using leadless chip carriers, with a ceramic substrate providing the connections between components. Another option is to house the components in a chip-and-wire hybrid, which results in even greater packaging density. □

Take a total-system approach, with advanced CMOS memories

CMOS memories are undergoing continual refinement, and new devices are increasingly competitive with those in other technologies. For these devices, though, specs such as standby and operating current are system parameters, not merely device descriptors.

Walter J Niewierski and **Russell M Pate,**
Harris Semiconductor

Memory manufacturers have improved CMOS so much that it now competes favorably with NMOS in speed while retaining its edge in power consumption. New CMOS devices, though, present design considerations somewhat different from those of older CMOS memories; you must take a systems approach to designing with them.

CMOS-memory choices have definitely expanded. CMOS RAMs, for example, now store as much as 64k bits and achieve access time as short as 55 nsec, operating current of 7 mA/MHz and standby current of 10 μA.

Additionally, CMOS fuse-link PROMs hold 16k bits and spec access time of 200 nsec, 10-mA/MHz operating-current consumption and 100-μA standby-current consumption. The short access time, along with an I_{CC} requirement lower than for NMOS or bipolar devices, gives CMOS the best PROM speed-power product.

CMOS EPROMs also compete well with their NMOS counterparts; devices store as much as 64k, and access time reaches 300 nsec with I_{CC} of 25 mA/MHz vs 100 mA for NMOS. At a 350-nsec access time, CMOS improves NMOS operating current by 4:1 and standby current by 250:1. Finally, in EEPROMs, you'll find 1k×8 block-erasable CMOS devices. However, NMOS, because of higher densities and byte-erase capability, still holds a slight edge here, although future CMOS units will also offer these features.

These performance levels exemplify a trend in MOS memories: the narrowing time span between the appearance of an NMOS device and its CMOS counterpart. For instance, CMOS EEPROMs followed their NMOS equivalents after less than 1 yr. Indeed, 16k CMOS static RAMs even preceded NMOS units by approximately 6 months.

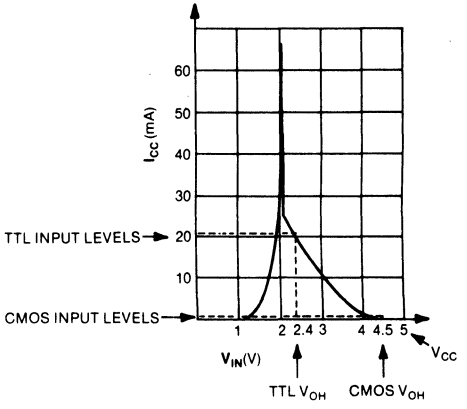


Fig 1—CMOS-memory operating current *varies widely over device operating-voltage range. Standby current is at a minimum when V_{IN} is at either power-supply rail. Note the difference in operating current associated with the V_{OH} (highest output-voltage level) for TTL and CMOS.*

What about price? Lower density (4k) CMOS RAMs are competitive with NMOS devices, but other CMOS memory types still sell at a premium. However, because NMOS is a mature process in all device types and CMOS isn't yet fully mature in all areas, the price gap should decrease.

CMOS memories provide another plus: You have a choice unavailable in most other technologies—synchronous or asynchronous operation. Roughly equal in price, both types have design advantages.

Synchronous memories provide on-chip address latches; thus, the address on the bus must be valid for only a short time, during which it's latched with the Chip Enable signal. This feature allows minimum-

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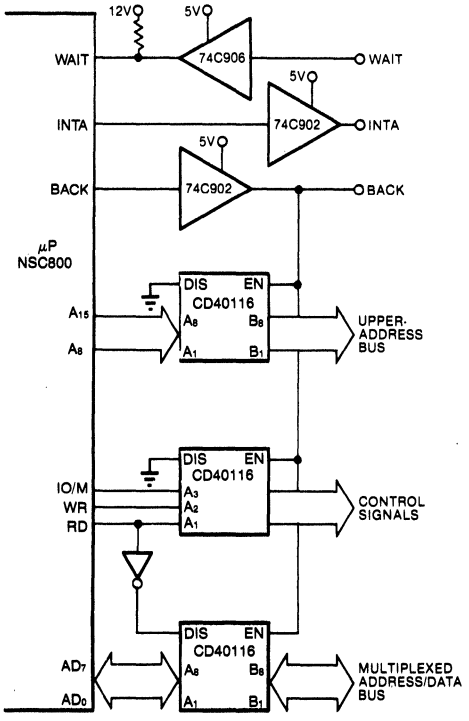
parts-count interfaces for systems with multiplexed address/data buses. Synchronous devices also spec lower average operating power.

Asynchronous memories, on the other hand, achieve shorter cycle times, even at the same access time as a synchronous unit. Why? Synchronous units require a minimum TEHEL (enable-pulse HIGH time) to precharge the matrix-column lines that speed up transitions of the column lines to the proper logic states.

Previously, 4k CMOS RAMs, like most memories, were strictly asynchronous—a feature that gave rise to availability problems. A circuit that accepts both types, however, provides the flexibility of dealing with more device suppliers, especially for 4k and 16k RAMs. The trick to designing such circuits is to devise a Chip Enable signal that undergoes a transition of the proper polarity when a stable bus address is present (**Refs 1, 2 and 3**). This signal causes the selected memories to latch the address, freeing up the system bus.



CD40116 CONTROL-SIGNAL TRUTH TABLE

ENABLE	DISABLE	FUNCTION
X	0	CMOS TO TTL
1	0	TTL TO CMOS
0	1	HIGH IMPEDANCE

Fig 2—Bidirectional level shifters *(CD40116s) interface standard 5V±10% CMOS memory and peripheral chips to the NSC800, which requires 3 to 11V power.*

Despite CMOS memories' increasing speed and other advantages, though, designers generally favor them primarily for their low power consumption in both Operating and Standby mode. The operating current arises mainly when device-enable inputs get switched; additional current arises when input circuits enter their linear operating regions. The low-Z path that occurs when an input voltage crosses through the switching-threshold region increases power-supply current (I_{CC}), which varies directly with the enable and switching frequencies.

Input-switching frequency also affects another major contributor to CMOS operating power—the charging of output loads. Increased load capacitance increases the current needed to charge and discharge such a load. Thus, I_{CC} increases with output-drive requirements.

CMOS memories consume microwatts in Standby mode with input levels stable at V_{CC} or ground; the corresponding current consists of surface, junction and channel-leakage contributions. When using battery-backed CMOS RAMs, you can minimize standby current by idling the devices when not in use and by deselecting all inputs, which you should hold at either power-supply rail.

Given this state of the art in CMOS memories, some designer reorientation might be required to use the newest devices. Users sometimes dispute standby-current specs, for example, because they observe above-spec values in memory devices that are disabled but that remain connected to active address and data buses. This phenomenon arises because of CMOS I_{CC}-vs-V_{IN} transfer characteristics (**Fig 1**), and it reinforces the need to examine device operation within the context of the system.

Note that the current for a CMOS input increases significantly near the threshold or switching voltage. At that point, both enhancement-mode input transistors that implement the input's inverter are ON to some degree (typically 1.3 to 2.2V at room temperature), introducing a dc path between the power-supply rails. When this transient current is time-averaged (accounting for the rise and fall times of bus transitions) and then multiplied by the number of disabled device inputs connected to an active bus, the disabled device's current can increase by a factor of 60 to 100.

You can observe a similar effect when driving CMOS inputs with devices that have valid logic levels within or near threshold regions. To maintain minimum standby current, you might need pull-up resistors to keep V_{OH} from these devices above the thresholds.

You might also need pull-up or -down resistors on some CMOS RAMs in battery-backed applications to

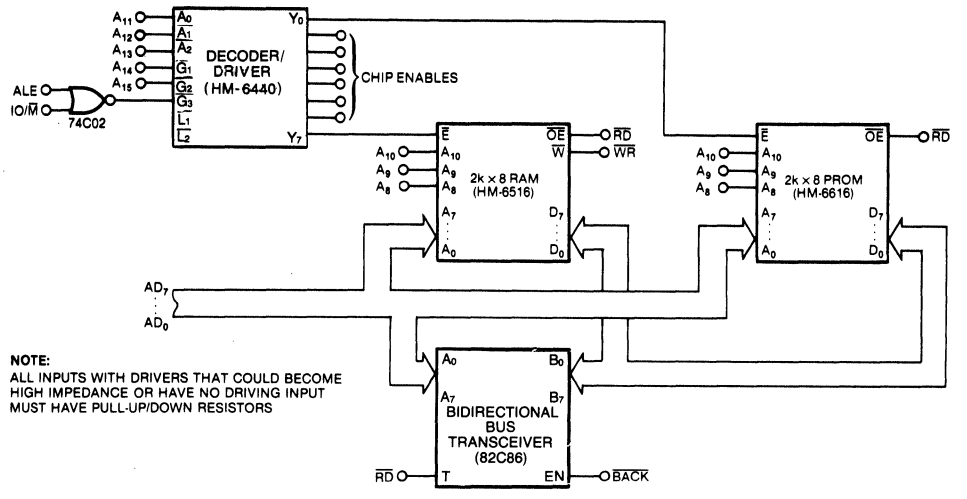


Fig 3—To decode the lower 16k bytes *of memory in Fig 2's multiplexed output into 2k-byte blocks suited for CMOS RAMs, this circuit uses an HM-6440 decoder driver. For data-bus interfacing, it incorporates an 82C86 bus transceiver.*

keep inputs from floating through and around the threshold region when power is lost to other system devices. Input voltages in reduced-power-supply applications should be no more than 0.1V from V_{CC} or ground. Otherwise, the battery-discharge rate increases considerably because of the higher I_{CC} caused by floating inputs. But these resistors can affect the transition times of driver outputs: In Operating mode, pull-down resistors might slow the rise time of TTL drivers by as much as 20%, and pull-up resistors increase their fall times by the same fraction.

CMOS-memory manufacturers have removed some of these design obstacles by adding two MOSFETs to standard 2-transistor input-inverter circuits. Such gated or disabled-input configurations prohibit the circuit's inverter from reacting to input transitions or floating inputs while the device is disabled. This feature simplifies battery-backup designs, reduces standby and operating current and cuts system parts count by eliminating the need for pull-up resistors.

When interfacing to CMOS memories not equipped with this input gating, you might overwhelm the operating power of bus drivers with the memory array's operating current. Avoid this problem by using CMOS bus drivers, which can reduce array power consumption as much as 70% compared with LSTTL buffers, mainly because of the differences in permissible output-voltage ranges between CMOS and LSTTL.

Fig 1 clearly illustrates this advantage. Note the memories' higher power consumption as V_{IN} moves away from V_{CC} and ground toward operating levels, then note the I_{CC} associated with the output-voltage levels of bipolar and CMOS bus drivers. For example, a 16k-byte CMOS static-RAM array running at 5V and 25°C and cycling at 1 MHz dissipates 1.35W with 74LS365 LSTTL bus drivers but only 475 mW with a CMOS bus driver.

Bus-interface considerations also help answer perhaps the most often asked question in memory-system design: Can memory be accessed rapidly enough to be speed compatible with the μP-system operating frequency? Many designers often overlook the effect of bus-interface-device speed—bus-buffer delays can restrict memory speed. But a tradeoff arises: Increasing bus-driver propagation delay by just 1 nsec, for example, might call for buying faster, more expensive memory devices.

Other system conditions can affect CMOS-memory operation. For instance, CMOS parameters generally improve as ambient temperature decreases—output-drive capability increases, providing greater current to charge and discharge load capacitances and thus increasing device speed. Standby power dissipation also decreases as the temperature drops.

Voltage levels of supplies and inputs also affect device performance. Raising the supply level increases device speed and power consumption; input levels above spec can greatly increase current and even damage devices.

Device ac characteristics depend greatly on the capacitive loading arising from interconnect and input

I_{CC} increases significantly near input-threshold values

capacitances of devices attached to the memory outputs. Loads greater than spec can increase memory propagation delay.

Other capacitive effects become more important in the newer high-speed CMOS memories. For instance, the large current transients associated with fast rise/fall times call for installing a decoupling capacitor (0.01 μF min) between the power-supply rails of every device in CMOS memory arrays. You should also install a large electrolytic capacitor where power enters the array. This provision proves especially important in large arrays of synchronous devices, where the largest transients occur on the V_{CC} and ground lines during chip-enable transitions.

CMOS RAMs in data-retention systems

When using CMOS RAMs in battery-power or battery-backup applications, be aware of several additional design precautions. For instance, input and output voltages can create problems. Thus, be sure to establish safe power-up and -down sequences because junction-isolated CMOS devices' inputs contain a parasitic SCR that remains inactive during normal operation but becomes active when input or output voltages exceed spec'd values. To avoid problems, raise and lower supplies in an order that prevents inputs and outputs from existing at potentials higher than V_{CC} or lower than ground.

Note also that you don't always need batteries in CMOS data-retention systems: Capacitor manufacturers now supply high-value, low-voltage units that can substitute for batteries. For instance, a 1F, 5V capacitor measuring 44 mm in diameter and 18.5 mm high requires less maintenance than a battery, exhibits a longer useful lifetime and permits an unlimited number of charge cycles. (However, it has a faster discharge rate and doesn't suit applications requiring data retention for extended periods—a 1F capacitor holds a 1k×8 synchronous-RAM array for 2 to 3 hrs.)

If you take the aforementioned CMOS-memory design factors into account and your battery-backed array is still losing data, use a checklist to troubleshoot most cases:

- Is V_{CC} dropping to less than 2V? If so, the problem probably arises during transitions into or out of Backup mode.
- Is the Write (W) line being pulled up with the Chip Enable (E) line as an added precaution?
- Are V_{CC}, E and W transitions glitch free, and do they ramp up and down smoothly?
- Are all other inputs held at V_{CC} or ground during the backup period? Floating inputs increase I_{CC} and shorten battery life.
- If you drive RAM inputs with LS drivers, are their outputs pulled up? They needn't be in most cases, because LS outputs tend to go to a low-Z-to-ground state when V_{CC} fails. (Some 3-state Schottky drivers don't exhibit this characteristic.)
- Are CMOS bus drivers being powered from the CMOS V_{CC} supply and not the system supply? This should be the case, and you should hold driver inputs HIGH or LOW with resistors. The outputs of CMOS drivers, however, should never be pulled up with resistors.
- For synchronous memories, is E held HIGH for at least one TEHEL period after V_{CC} has risen to normal operating level?

The following design examples, besides showing how to account for such system considerations, illustrate

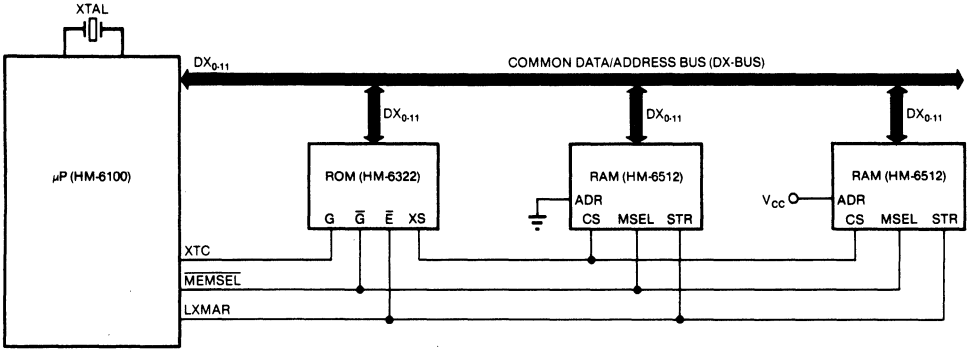


Fig 4—Interfacing CMOS memory to CMOS μPs *such as the 12-bit HM-6100 proves simple. With this all-CMOS design, you can easily create a small data-acquisition system that accommodates 10- or 12-bit A/D or D/A transfers in one byte.*

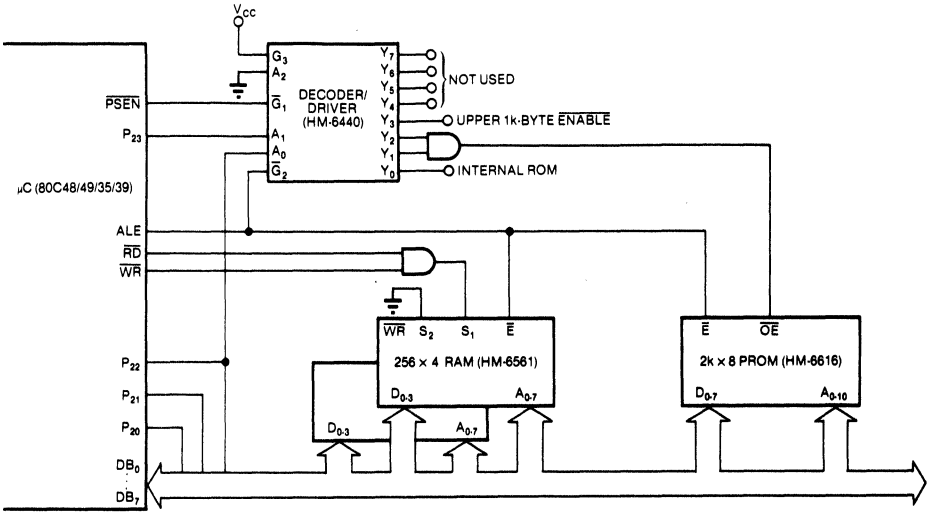


Fig 5—Memory expansion for single-chip μCs *doesn't necessarily introduce a large power penalty. This design applies to systems using the CMOS or NMOS versions of the 8048 as well as other 8048-family members.*

how to implement all-CMOS μC-memory systems and how to adapt CMOS memories to NMOS-processor systems.

The first example uses an NSC800 8-bit CMOS μP. While most CMOS devices require 5V±10%, this μP and a family of support devices accommodate a 3 to 11V operating range. You might, however, need some CMOS devices of the standard 5V±10% type, and using a system supply voltage outside this range for both types can present interfacing problems.

To implement such interfacing, the system must be able to shift voltage levels quickly; for this task, the circuit shown in **Fig 2** uses the CD40116 octal bidirectional level shifter. This device exhibits a 15-nsec propagation delay when shifting from 12 to 5V and 30 nsec when going from 5 to 12V.

Fig 2's 10V/5V translation interface uses two CD40116 control signals to determine the direction of data flow and voltage translation. CMOS inputs $A_{1\text{-}8}$ can withstand levels as high as V_{DD} (10V in this case), while inputs $B_{1\text{-}8}$ are TTL compatible only.

The control signals are generated separately (via three level shifters) for address- and data-bus and control-line buffering. Of these, the control-line interface is the simplest: Its level shifter is constantly enabled for CMOS/TTL conversion. And because these NSC800 control signals and upper addresses are unidirectional outputs, controlling them involves only a shift between CMOS/TTL conversion and the high-impedance state, achieved with the μP's Bus Acknowledge (BACK) line. When the μP gives up control of the bus to another processor or peripheral, these lines have a high impedance. Finally, the multiplexed low-address/data bus is controlled by the μP's RD signal, which gets inverted and applied to that CD40116's Disable input. You can translate remaining control signals (such as WAIT, INTA or BACK) with additional CD40116s or with 74C90X translators as shown.

To decode the lower 16k bytes of memory provided in the multiplexed output into 2k-byte blocks, use the circuit shown in **Fig 3.** Its HD-6440 decoder/driver, with three device enables, allows the circuit to decode addresses directly. You need only a NOR gate to combine ALE (Address Latch Enable) and IO/$\overline{M}$ (Input-Output/Memory). The 6440 also provides eight 2k-block enables for the CMOS memories shown. Moreover, because the circuit uses synchronous memory devices with on-chip address latches, it needs no external latches.

The NSC800 controls memory operation with RD and WR lines, which connect to the all-output enable (OE) controls and the Write line on each RAM. The decoder/driver generates each RAM's enable (E) signal. If you need additional data-bus buffering, or if you choose not to use a CD40116 for voltage translation, consider the 82C86 CMOS bidirectional bus transceiver for the data-bus interface. This device remains enabled unless the μP gives up bus control (BACK

controls the bus transceiver's enable); RD determines data direction.

You can apply this CMOS-based circuit to the NMOS 8085. Using CMOS memories in an NMOS system can improve reliability and system operation by decreasing power requirements and providing higher noise immunity than NMOS devices. Furthermore, by using CMOS bus drivers with CMOS memories, you can further reduce circuit operating-power requirements.

The second all-CMOS microsystem example uses the HM-6100, which suits applications such as remote data acquisition. **Fig 4** shows a minimum memory configuration for this μP. A 1k×12 CMOS ROM (an HM-6322) holds the main program and also provides decoding for the system's 64×12 CMOS RAMs. The ROM's XS (External Select) output places the RAM in the memory map as determined by its decoding logic, which you program. This output enables system RAM whenever the RAM area gets addressed. Both ROM and RAM devices provide on-chip address latches and latch this data on the falling edge of the LXMAR (Latch External Memory Address Register) signal from the μP. To add memory to the system, you can adapt nearly any standard device.

The final design example, which uses the CMOS 80C48 single-chip μC, destroys the myth that single-chip systems should have as few devices as possible for lowest power consumption—the capabilities of new CMOS devices can compensate for this factor in system expansion. This circuit (**Fig 5**) expands both data and program memory via CMOS devices. This expansion concept, though, is applicable to systems with CMOS or NMOS versions of the 8048 or other family members with few modifications. When using an NMOS 8048 with V_{OH} spec'd at 2.4V, you might need to add a few pull-up resistors in the worst case. Timing, though, presents no problems.

Within the CMOS μC, data and program memory reside in separate areas, each with its own control signals. For data-memory expansion, this design uses HM-6561 synchronous RAMs. It needs two such 256×4 devices to fill the 80C48's 256-byte data memory.

The RAMs have two select pins ($S_{1,2}$) and one enable (E); this latter line latches the address bits onto the chip and is active LOW. Address latching occurs on E's HIGH-to-LOW transition. The μC's ALE (Address Latch Enable) connects to the E line, and this signal has the proper polarity and its HIGH-to-LOW transition occurs when addresses are stable on the processor bus. The ALE signal serves for the E function on all devices in the memory array. Chip Select lines ($S_{1,2}$) select the appropriate RAM; S_1 is derived from the 80C48's RD and WR signals while the S_2 pins get tied to ground. The two memory signals occur whenever a data-memory read or write is in progress; you need no further decoding because these signals are active only during data-memory transfers.

For program-memory expansion, this circuit uses an HM-6616 2k×8 CMOS PROM; this high-density device eliminates extensive decoding, reducing parts count for both the decoding scheme and the memory devices. Individual output enables from the HD-6440 decoder are available for each PROM along with an EEPROM enable. If you use no other devices for program memory, you can eliminate the decoder; in that case use the processor's PSEN signal for enabling PROM because it's active only for external program-memory fetches. **EDN**

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LCC implementation procedures enhance a valuable technology

Meeting tight military and commercial packaging requirements, standard leadless chip carriers offer weight, space and density benefits. To take advantage of these fortes, though, you must pay close attention to assembly techniques.

Jeffrey M Wilkinson, Harris Semiconductor

Despite their much-touted benefits—primarily increased packaging density, higher reliability and lower cost compared with other types of IC packages—leadless chip carriers (LCCs) haven't made the expected inroads with system designers. Why? Largely because published information has focused on design concepts and techniques rather than on practical implementation procedures. Consequently, this article describes LCC mounting, soldering, heating and reworking guidelines to help you overcome the constraints posed by the need for compact packaging (see **box,** "LCCs shine in high-density packaging").

MATERIAL THERMAL PROPERTIES

SUBSTRATE MATERIAL	TCE* (IN./IN./°C x 10^{-6})	COMMENTS
ALLOY 42	5.3	42% Ni, 58% Fe
96% ALUMINA	6.3	INDUSTRY STANDARD
94% ALUMINA	6.4	INDUSTRY STANDARD
92% ALUMINA	6.4	INDUSTRY STANDARD
COPPER CLAD INVAR	6.4	INDUSTRY STANDARD
99.5% BeO	6.4	EXPENSIVE
LOW CARBON STEEL	12.0	PORCELAINIZED
POLYIMIDE G30	14.3	INDUSTRY STANDARD
EPOXY/GLASS G10	15.8	INDUSTRY STANDARD
TRIAZINE G40	16.0	INDUSTRY STANDARD
CDA 101 COPPER	17.3	VERY HIGH TCE
6061 ALUMINUM	23.6	VERY HIGH TCE

*TCE = THERMAL COEFFICIENT OF EXPANSION

Match, don't mix, mating materials

After having chosen LCC-packaged ICs for your application (EDN, May 27, 1981, pg 49), you must determine the means of attaching these packages to a pc board or substrate material. To accomplish this chore, evaluate LCC mounting materials (**table**).

Selecting a board or substrate material involves matching its linear thermal coefficient of expansion (TCE) to the LCC's. When the TCEs don't match, thermostatic deflection (twisting or warping) results during the wide temperature changes characteristic of military applications. During twisting, for example, torque effects bear on the solder joints, causing electrical and mechanical connection fatigue.

This thermal problem gets worse with larger LCC pinouts because of increased package size and stress levels. Accordingly, follow a general rule when selecting a substrate material: The larger the TCE difference between LCC and substrate materials, the smaller the substrate's surface area must be. Alumina substrates, for instance, work best when they don't exceed 24 $in.^2$ Ideally, therefore, choose the same material for both the substrate and the LCC: a 92%-alumina ceramic LCC attached to a 92%-alumina substrate (**Fig 1**), for example.

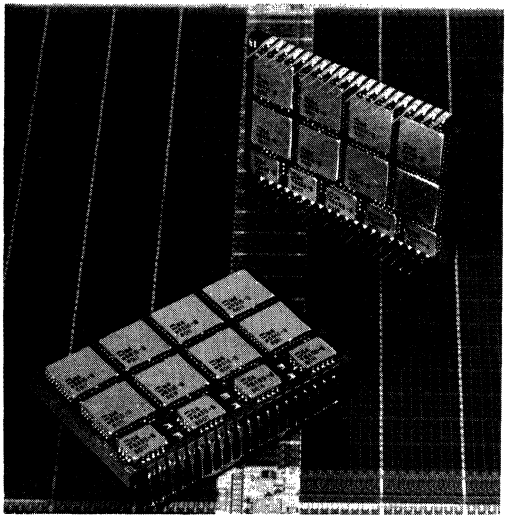

Fig 1—Achieving significant space and weight savings *compared with the equivalent DIP configuration, this multilayer 92%-alumina ceramic substrate holds 92%-alumina LCCs. The materials matching prevents parts from undergoing thermostatic deflections (twisting or warping) during the temperature changes typical of military applications. Note that the LCCs, carrying 256k static-RAM-module prototypes from Harris, mount on both sides of the substrate.*

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Military circuits benefit from LCC size, weight, density assets

In picking pc-board materials, military specifications play a dominant role. One MIL spec, MIL-STD-883B, Method 5004.4, Class B, for instance, outlines pertinent test and qualification methods. It requires Method 1010.2, Condition C thermal cycling (ie, over −64 to +150°C with 10-min durations at each extreme) for at least 10 cycles. This standard covers microelectronic devices, such as those with an LCC as a component, but doesn't apply to printed-wiring-board assemblies.

Another military spec, MIL-P-55110C for printed-wiring boards, calls for 100 thermal-shock cycles, spanning −65 to +125°C for expoxy boards and −65 to +204°C for polyimide boards. Yet another, MIL-P-28809 for printed-wiring assemblies, mandates thermal shocks in accordance with MIL-STD-202, Test Methods for Electronics and Electronic Component Parts, Method 107. This method's applicable worst-case test specifies 100 temperature cycles, ranging over −65 to +150°C with 5-min maximum intermediate hold periods at 25°C, and with soak times at temperature extremes determined by the assembly's weight. (In most cases, soak times run 0.5 or 1 hr.)

Not everyone agrees completely with these temperature-cycle requirements. Martin Marietta (Orlando, FL), for instance, has been mounting LCCs on printed-wiring boards for more than 6 yrs. And based

LCCs shine in high-density packaging

Leadless-chip-carrier (LCC) product designs appear to be becoming the industry-preferred package for high-density, high-pinout ICs. In fact, they should supplant flatpacks and hybrids in the short term and surpass DIPs in the long term. They meet the need for very small, dense and lightweight circuit packaging, especially in military applications, which stress highly reliable electrical and mechanical performance.

In the past, DIPs have proved sufficient for these applications. But as military-circuit specifications continue to demand smaller size and less weight for more complex electrical functions, another packaging method—the flatpack—has evolved.

Flatpacks have proved a worthy alternative to DIPs for reducing board space. However, they also exhibit shortcomings. For one, package cost is high because of extensive gold plating. Moreover, long lead lengths and narrow spacings mandate special handling carriers. Further, during soldering to pc boards, the long lead lengths allow package vibration, jeopardizing lead connection and solder-joint reliability.

Because ICs packaged in DIPs and flatpacks have proved deficient in meeting strict space-vs-function requirements, chip-and-wire hybrids have become popular. Extremely compact, these hybrids provide multiple functions within a small area. Typically, though, they cost more than DIPs and pc boards because of high assembly and test costs, low rework yields and the expensive manufacturing equipment required. In military applications, however, small size and lightweight design generally take priority over cost.

Manufacturers commonly assemble hybrids from dice. This procedure, however, results in limited device performance because of IC-manufacturing constraints on wafer-level testing. Less-than-stringent testing thus passes less-than-perfect devices for hybrid assembly. Nevertheless, subsequent hybrid-level testing assures quality products, although low device yields prove expensive.

An LCC-packaged device attached to a board or substrate material achieves higher performance at a lower price than a hybrid device. Furthermore, LCC packages permit full parametric testing plus burn-in, yielding higher reliability units.

When similarly contrasted with DIPs, LCCs offer much smaller size and weight. For example, an 18-pin DIP occupies 0.276 $in.^2$; an 18-pin LCC, only 0.100 $in.^2$ The space-saving ratio with LCCs therefore approaches 3:1. Likewise, comparing weights, an 18-pin DIP weighs 2.48g; an 18-pin LCC, 0.32g. The LCC thus proves 7.75 times lighter.

LCCs' electrical benefits are outstanding as well. Their small sizes and leads on four edges permit the use of very short conductor lengths from the external leads to the internal chip-cavity bond pads. This layout results in lower parasitic resistances, capacitances and inductances than those demonstrated by corresponding DIPs.

What's more, you can use clock rates as high as 4 GHz with LCCs; DIPs' parasitic deficiencies restrict their speed to about 500 MHz. And besides their small size—often only slightly larger than the installed die—and lack of leads to break or bend, LCCs withstand the rigors of MIL-STD-883B testing at the package level, including Groups A, B, C and D.

To ensure industry-wide acceptance, the Joint Electron Device Engineering Council (JEDEC) and

on its experience and test data, it concludes that 100 temperature cycles are excessive. The packaging industry, on the other hand, favors increased cycling but over a narrower temperature range—300 cycles at −55 to +125°C.

Take care with pc-trace layouts

After board- or substrate-material selection, investigate pc-trace geometries. In accordance with industry-proven practices, make the LCC foot pads' circuit traces the same size as the metallization on the LCC's bottom surface and slightly longer at the package's outer edge (**Fig 2a**). Lengthening the pc board's metallization allows the solder, when heated to reflow temperature, to wet both the base contacts and the grooved region on the LCC package's sides.

The solder deposit's outer surface thus forms a fillet that extends over the metallization pad on the board or substrate surface (**Fig 2b**). This extension aids in strengthening the mechanical bond. Additionally, this type of bond elevates the LCC above the board's mounting surface, facilitating the cleaning of residual flux and debris from under the package.

To take advantage of LCCs' high packaging density, maintain relatively tight geometries in board-metallization layout and manufacturing. Successful

the Dept of Defense (DoD) have sought to develop chip-carrier packaging concepts and standards for military applications. These efforts have resulted in a standard line of LCCs with two packaging styles—one with 50-mil-center terminal spacing and another with 40-mil centers. Within these package styles, a variety of pin counts is available—16 through 156 in 16 common sizes.

The USAF Materials Lab (AFML) has directed and supervised DoD LCC development efforts, funded through the Manufacturing Technology (MANTECH) portion of the DoD's R&D budget. This group has also financed Hughes Aircraft's development and manufacturing of a line of 50-mil LCCs and RCA's development of 40-mil types.

JEDEC's endeavors have centered on coordinating industry projects with the MANTECH program to minimize duplicating tasks. Coordinated investigations have produced eight standard LCC packages, with two more versions expected soon.

Many system designers, however, can't justify the time and expense required to buy manufacturing equipment and develop new assembly procedures for installing LCCs on pc boards. To overcome these problems, consider an alternative packaging method—cofired ceramic substrates with attached LCCs. These substrate mother boards or modules provide interesting design tradeoffs compared with chip-and-wire hybrids and pc-board-mounted LCCs.

As one benefit, you don't need LCC-handling and reflow-soldering equipment. As another, you can mount LCCs on both sides of the module, achieving a parts density twice that of a single-sided pc-board assembly. (Note that you can build 2-sided LCC-based pc-board assemblies, but they are difficult for a first-design effort.) As yet another benefit, you can choose among a variety of LCC packages and quickly configure a system.

On the debit side, though, manufacturers charge more for finished module products than the sum of the parts costs: They typically add the expenses of additional assembly and test time as well as the substrate cost.

To make a worthwhile pc-board-vs-module comparison, therefore, you must make the traditional build-or-buy decision. If your application calls for high density, the module approach usually is more cost effective. Furthermore, major semiconductor manufacturers offer off-the-shelf ceramic mother boards.

For example, Mostek makes a 4332D 32k dynamic-RAM package using two 4116E 18-pin LCC devices. It also plans to combine two 64k 4164E dynamic-RAM LCCs on a mother board to yield a 128k×1 dynamic RAM.

Texas Instruments employs a similar approach in its SMJ-444164 256k dynamic RAM, which contains four TMS4164 64k dynamic RAMs mounted in 28-pin LCCs. And Harris Semiconductor furnishes the HM5-6564 64k CMOS static RAM. Double-side mounted on a ceramic mother board along with four decoupling capacitors, this RAM contains an array of 16 HM-6504 4k RAM chips in LCC packages.

Finally, an analog signal processor from Harris, the HI5-5900, comes assembled with five LCC packages and eight 0.1-μF decoupling capacitors. The LCCs include an input multiplexer, dual buffers, a programmable-gain instrumentation amplifier, a reference buffer and a track/hold.

guidelines dictate chip-carrier package layouts with 0.010-in.-wide trace lines, 0.010-in. spaces between lines and 0.020-in.-diameter (or smaller) feedthrough holes. Pads that connect to the LCCs typically run 0.020 in. wide on 0.050-in. center spacings. This center-spacing dimension permits one 0.010-in.-wide line and 0.010-in. line spacing between LCC mounting pads (**Fig 3**). If you must run trace lines between (or very near) pads, apply a solder mask to the pc board to prevent solder bridging during the reflow process.

Using multilayer boards or substrates calls for added layout awareness. For example, use the surface-layer metallization exclusively to implement LCC mounting pads. This allocation eliminates the need for a solder mask and minimizes solder bridging. Furthermore, to reduce electrical noise, arrange the power-supply buses in a gridded array within a single layer and route signal lines on other substrate layers. Moreover, if you employ the services of a board manufacturer, make sure that the vendor can reproduce the product accurately and reliably with the required line widths, hole diameters, solder masks and multilayer construction before initiating LCC layout.

Mounting LCCs can be difficult

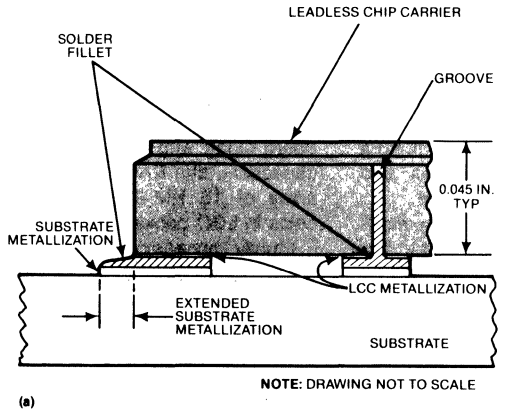
Now that the finished boards are on hand, you must populate them. Attaching LCCs to conventional pc boards entails bonding problems that defy straightforward solutions. Currently, you can choose between two methods—soldering or socketing.

In military applications, socketing falls short: Available sockets are bulky and have unwieldy construction, and although adequate for routine uses, they're deficient for critical ones that demand high packing density and undergo severe environmental stresses. As a result, reflow soldering, although far from ideal for attaching LCCs to boards or substrates, works best.

To aid the reflow-soldering process, pretin both the LCC's package I/O metallization and the interconnecting substrate's metallization. Fluxing and dipping methods serve well for pretinning the LCC's package pads; use wave soldering or screen on a solder paste for the substrate's pads.

For wave soldering, after tinning the substrate, use an adhesive or glue to secure the LCC on top of the substrate's metallization during reflow soldering. Implementing the solder-paste option calls for applying the paste to the substrate's contacts with a screen-printing technique. This process involves depositing an 8- to 9-mil-thick layer of wet paste on the contacts and then air drying the board until the paste becomes tacky. You then mount the LCC, either manually or by machine insertion, onto the corresponding contacts.

Another presoldering process producing favorable results involves bake drying the populated substrate. It allows air- and flux-pocket evacuation within the paste, minimizing volatility effects in a vapor-phase soldering operation. Otherwise, unevacuated flux pockets would float the LCC package during reflow soldering and result in misaligned positioning. Bake drying also



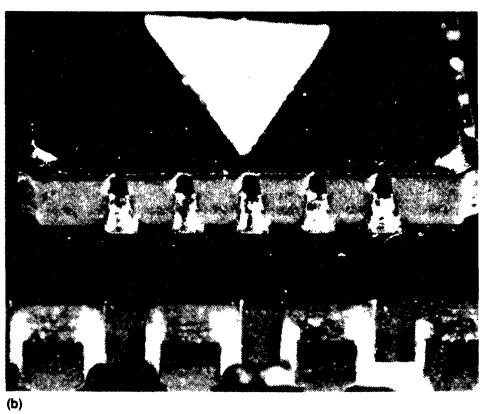


Fig 2—For proper installation on a substrate or board material, *make an LCC's foot-pad metallization the same size as the associated pc traces, but slightly larger at the chip carrier's outer edge* ***(a).*** *Elongating the pc metallization permits the heated solder to wet the base contacts and the grooves located on the chip carrier's sides. Forming a fillet, the solder deposit's outer surface extends over the metallization pad on the substrate's surface* ***(b).*** *This arrangement completes the LCC-to-substrate electrical connection, strengthens the mechanical bond and slightly lifts the LCC from the substrate for cleaning purposes.*

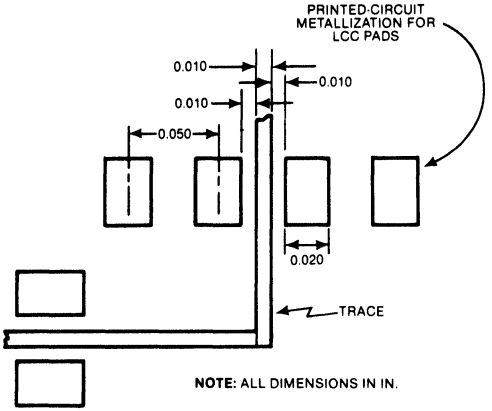


Fig 3—High LCC packaging density *calls for tight geometries in board metallization, layout and manufacturing. Typical chip-carrier layouts mandate 0.010-in.-wide pc traces, 0.050-in. LCC center spacings and 0.010-in. spaces between traces and LCC mounting-pad metallization.*

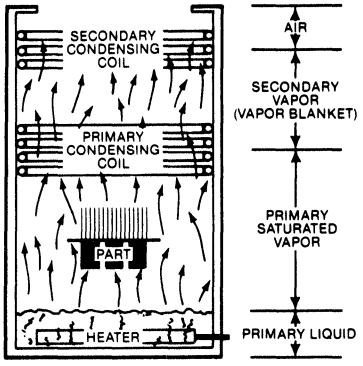


Fig 4—To meet high-volume production needs, *vapor-phase reflow soldering bonds LCCs to a substrate through the use of dried solder paste. Within the soldering chamber, the populated substrate absorbs heat in the primary saturated-vapor region and reflows the solder joints. Lifting the substrate into the secondary-vapor region cools, dries and cleans the soldered assembly.*

reduces the solder paste's liquidity, temporarily holding the LCC to the substrate.

Locating the LCC on the substrate, however, doesn't require critical placement. During reflow soldering, the dried solder paste bonds the LCC in position while heating to reflow temperature. The solder's surface tension pulls the LCC into alignment over the substrate contacts. Placement thus needs only enough accuracy to ensure that the LCC's solder pads don't overlap other pads on the metallization below.

Whatever soldering procedure you choose, though, you must apply sufficient, controlled heat to melt the solder. Widely used methods include belt furnaces, heated air chambers and infrared radiation; however, they haven't received widespread industry acceptance. The vapor-phase reflow-soldering technique, on the other hand, proves efficient for high-volume LCC production (**Fig 4**). It typically involves a chamber containing a primary heating zone, a secondary intermediate cooling and cleansing zone and a pool of high-boiling-point fluorinated hydrocarbons.

During vapor-phase reflow soldering, a populated substrate gets lowered into the primary zone. Here, the saturated vapor causes uniform solder-joint reflow: It condenses over the substrate's surface, dispensing its latent heat through vaporization. This thermal exchange quickly and evenly heats the substrate.

Next, the substrate gets lifted into the secondary zone. In this vaporized region, the condensed fluid accumulated within the primary zone drips off the substrate and drops into the boiling liquid. Then the substrate leaves the chamber soldered, dry and relatively clean. A final cleaning process ensues immediately after substrate removal before any residue congeals.

Yet another reflow-soldering technique—cost effective for experimental and low-volume production needs—employs hot solder oil. In this method, the populated substrate is immersed into a hot oil bath, quickly heating the solder and parts to reflow temperature. After removal from the bath, the substrate undergoes a cooling interval. Finally, a rinsing operation removes residual oil and excess flux.

Reflow soldering simplifies reworking

In addition to the board-assembly techniques just discussed, you must pay an equal amount of attention to removing LCCs for repair or replacement. Because LCCs contain no leads and board substrates possess no holes to deform, rework proves straightforward. Of course, soldering factors such as reflow technique and temperature, solder type and metallization thickness greatly affect the degree of rework difficulty.

One LCC-package-removal method merely reverses the hot-solder-oil immersion technique for installing LCCs. In this approach, after substrate immersion and solder reflow, you remove the LCC from the board using tweezers or a similar tool.

Another removal method involves the use of a soldering iron containing a specially shaped tip for heating LCC contacts. You can also use a forced-hot-air

gun to heat the LCC package and surrounding area. This heat-gun method is widely used because it's convenient, inexpensive and practical. After heating, you lift the package off the board using tweezers.

Before soldering a replacement LCC, though, make sure you tin its contacts and the substrate's exposed contacts. Then manually position the new LCC close to its designated location. Finally, heat the surrounding area or the entire board to the solder-reflow temperature, bonding the LCC to the board and completing the rework cycle. EDN

References

1. Caswell, Greg, and Isaacson, Dale, "Hermetic chip carrier assembly process and materials evaluation," *Electronic Packaging and Production,* January 1982.
2. Dance, Francis J, and Wallace, John L, "Clad metal circuit board substrates for direct mounting of ceramic chip carriers," *Electronic Packaging and Production,* January 1982.
3. Fennimore, John E, "Hermetic ceramic chip carrier implementation," *Electronic Packaging and Production,* May 1981.
4. Hochstedler, Charles M, and Wilkinson, Jeffrey M, "Leadless carriers and CMOS technology yield high-density low-power memory systems," *Wescon Proceedings,* Session 24, 1980.
5. Jonas, A W, and Garner, L E, *Leadless chip carriers: The packaging technique of the 1980s,* Harris Semiconductor publication.
6. Tsantes, John, "Leadless chip carriers revolutionize IC packaging," *EDN,* May 27, 1981, pgs 49-74.

Custom Integrated Circuits Division

9

Introduction	9-2
Custom Capabilities	9-3
Semicustom Capabilities	9-7
Radiation Hardened Products	9-15
Specialized Products	9-27
Product Assurance	9-31
CICD Sales Office Locations	9-33

Custom Integrated Circuits Division

Harris. A reputation in hi-rel custom circuits no one else can match. An emerging force in gate arrays and standard cells. A leader with all the options.

Fifteen years of pace-setting experience from programs like Trident and Peacekeeper to commercial satellites and heart pacemakers make Harris your logical choice for quality, speed and performance in custom/semicustom ICs. From commercial screening all the way to Class S equivalents. And beyond.

If fast turnaround to market introduction or system prove-out in low volumes is your need, look to Harris gate arrays. Minimum initial investment and development time make them the logical choice. And upgrading to standard cell or full custom is easy.

Quick turnaround combined with ease of design and medium-to-large volume cost efficiencies make Harris standard cells your best buy.

However, for highest performance, lowest unit price, maximum reliability and smallest silicon area in high-volume requirements, Harris full custom ICs are the preferred option.

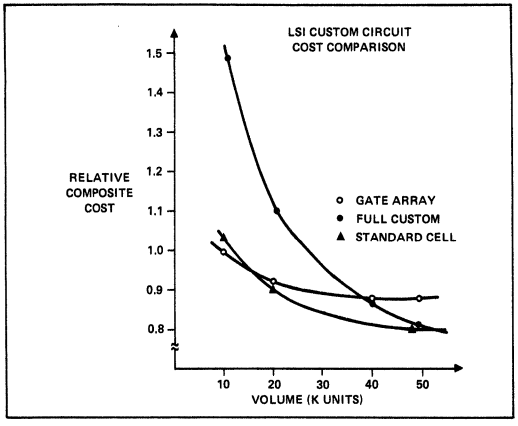
Your choices don't stop there.

Choose the technology. Analog or Digital. Bipolar or CMOS. Separately, or combined onto a single chip. Let us apply our vast experience to provide you with the right product, in the right package, at the right price.

You can even choose your level of design and layout participation to make best use of your in-house capabilities. Use our engineers or use your own. Full capability or silicon foundry, we offer all the support you need.

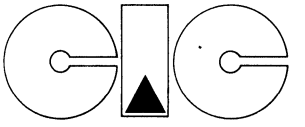
And if you have radiation hardeness requirements look no further. Harris is the leading supplier of radiation hardened circuits in the military marketplace.

No matter which option you take, opt for the experts at Harris. The logical choice.



For more information or data sheets, mail your request to: Harris Custom Integrated Circuits Division, P. O. Box 883, Mail Stop 53/107, Melbourne, Florida 32902.

Or Call: (305) 729-5681



CUSTOM CAPABILITIES

- VLSI Development Alternatives
- Custom VLSI Services
- General Custom Capabilities
- Process Alternatives for MOS Design

VLSI DEVELOPMENT ALTERNATIVES

DEVELOPMENT	ADVANTAGES
Full Custom	Highest speed, highest density (smaller die), lowest recurring cost, lowest power consumption.
Custom/Semicustom (custom blocks & standard cells)	Custom blocks have the advantages of the "full custom" development with high speed, density and power in the standard cell section.
Semicustom (standard cell)	High speed, density and low power, low recurring and nonrecurring cost. Proven cells give high probability of success.
Gate Array	Lowest nonrecurring cost. Proven cells and macros.

CUSTOM VLSI SERVICES

TYPE	SERVICES SUPPLIED	CUSTOMER INPUTS
System/Chip Partitioning	Development of device specification	System specification
Logic Simulation	Verify logic using CAD equipment	Logic diagram
Test Word Generation	Generate the test vectors, add parametrics and produce a test program	Logic diagram and specification
Fault Analysis	Analyze test program for detection of failed states	Logic diagram and test word
Circuit Design	AC simulations, chip plan device design	Specification
Circuit Layout	Generate data base for circuit fabrication	Design package
Mask Fabrication	Generate optical or MEBES masks	PG, Calma or MEBES data base
Wafer fabrication	Produce wafers and if required probe, assemble, test and burn-in	Masks
Device Characterization	Analyze units for compliance with specifications and map working zone	Test program and units
"Built to Print" Production	Run wafers and if required probe, assemble, test and burn-in	Masks, test program and specification

These options are available as stand-alone services or as parts of an integrated development program.

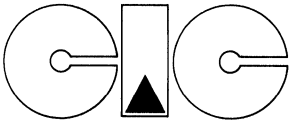
Custom Capabilities

GENERAL CUSTOM CAPABILITIES

High Performance Digital Si-Gate CMOS	Basic process for custom developments, 100+MHz operation of clocks, high density and low power.
Radiation Hardened Option	Available for military and spacecraft use.
Analog Option	Useful in increasing the level of integration. Utilizes mixed high performance Si-Gate CMOS and analog elements.
Class B and Class S Equivalent Screens	Full high reliability screening capabilities (i.e., Burn-in, SEM, Failure Analysis, Wafer lot identity, etc.).
Classified Programs	All CICD design personnel have appropriate clearances to participate in classified developments. Manufacturing and test areas are cleared to process classified material.

PROCESS ALTERNATIVES FOR CUSTOM MOS DESIGN

PROCESS	CHARACTERISTICS	fMAX	GATE t_{pd}	RAD-HARD OPTION	APPLICATIONS
CMOS Self-Aligned Silicon Gate	$V_T \approx 0.6$ to 1.1V $BV_{DSS} > 7V$ $V_{DD} = -1.8$ to 7V			Yes	Custom & semicustom cell library for computers, industrial controls, interface circuits, memories, heart pacemakers, Telecomm, Datacomm, nuclear reactor controls.
SAJI I		$\leq$50MHz @ 4.5V, 125°C	$\sim$5ms Custom $\sim$10ns HL Cell Library		
SAJI IV		$\leq$100MHz @ 4.5V, 125°C	$\sim$2ns Custom $\sim$4ns HD Cell Library		
CMOS Metal Gate	$V_T = 0.5$ to 1.5V $BV_{DSS} > 15V$	5MHz @ 10V	50ns @ 10V	Yes	Digital communications, interface circuits, logic.
PMOS Silicon Gate	$V_T \approx 1.5V$ $BV_{DSS} > 15V$ $V_{DD} = -7V$ $V_{GG} = 15V$	1MHz	125ns Average	No	Digital communications, dynamic shift register
PMOS Metal Gate	$V_T = -3V$ to $-4V$ $BV_{DSS} \geq 30V$ $V_{DD} = -15V$ $V_{GG} = -27V$	$\leq$ 1MHz	$\sim$125ns Average	No	Digital communications, dynamic shift register
Analog CMOS	SAJI IV with added high value resistors & voltage independent capacitors	$\sim$ 2MHz	–	Yes	Mix analog & digital on same chip for op amps, comparators, oscillators, analog switches, switched capacitor filter, voltage mulitpliers.
High Voltage CMOS	SAJI I with 40V Capability	$\leq$ 50MHz @ 4.5V 125°C	$\sim$5ns Custom 10ns Cell Library	Yes	Interface circuits, industrial control, automotive.



SEMICUSTOM CAPABILITIES

- Design Automation Support
- Standard Cell
- Gate Array
- SSI/MSI Library for Semicustom Design

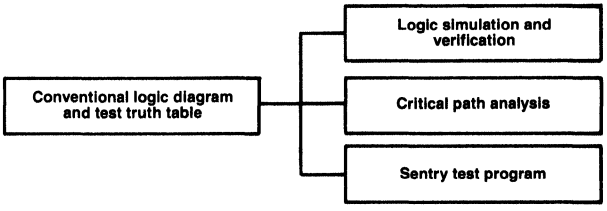
HARRIS

DIAL-A-CHIP[SM] CODING & LOGIC SIMULATION

FEBRUARY, 1983

Features

- DIAL-UP CAPABILITY
- TEGAS SIMULATION
- AUTOMATIC TEST PROGRAM GENERATION
- EASE OF DESIGN



Description

In this phase the designer converts the discrete logic schematic to an equivalent schematic using Harris SSI/MSI library functions from the cell library.

The designer enters the logic description code at the terminal. The code is written in the form of a from-to connection list similar to the component wiring list of a PC board. The overall procedure is to code each software block in a hierarchical manner beginning with the lowest level and progressing to the highest. Software macros may be defined by the designer on repetitive circuitry to make logic coding simpler. After each block is coded, an error-checking program is run to check for coding errors. Errors are corrected using a basic line editor before proceeding to the next block.

Once all software blocks are coded, a logic description file is created which represents the input database for the complete circuit design. It is used as input to several programs which perform logic simulation (TEGAS), initial layout (MERLYN or MP2D) and network checking (NETCHK).

The next step is to generate a test description file which will be used for simulation and test program generation. By having the test vector in this TDF language, a Sentry test program can be made quickly and easily.

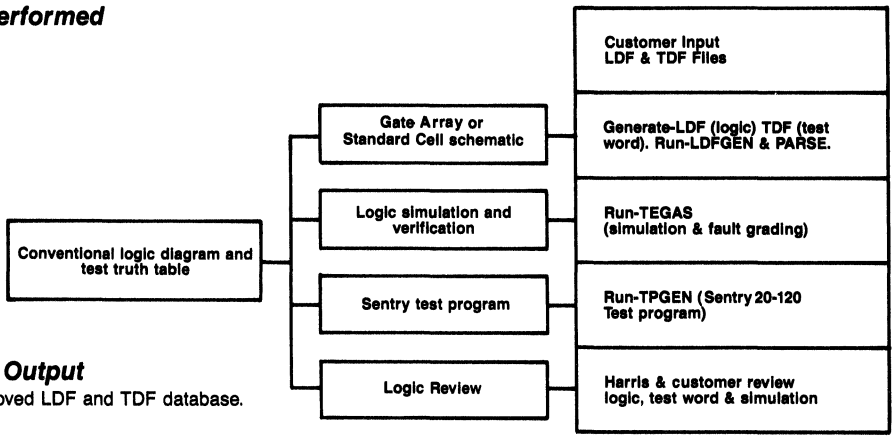
Design verification is next conducted using the TEGAS logic simulation program. During this phase, the system designer simulates the functional operation of the logic design, evaluates circuit speed and determines how effective his input test patterns are in detecting circuit faults.

Customer Input

A design may contain SSI/MSI functions which are required by the design and are not found in the Harris macro library. If it is decided to have Harris design these macros a design cost will be incurred. This additional design charge may be avoided by the customer by breaking down the circuit into primitive logic before defining the logic in the Harris LDF code.

- Customer is to provide a set of test words in TDF truth table format to be used to develop a test program
- Fault simulation of the device must exceed 90% on supplied test word.
- Customer is responsible for identifying critical paths and associated worst case delays.
- The customer is expected to provide logic simulation and fault simulation until TEGAS is approved in the Teledesign™ software package.
- Customer supplies conventional logic diagram in 7400 or 4000 logic.

Task Performed



Harris Output

- Approved LDF and TDF database.

HARRIS

HSC-CXXXXX

Standard Cell

Features

- 3 MICRON CMOS TECHNOLOGY
- VARIABLE DIE SIZE
- 3ns TYPICAL GATE DELAY
- 50MHz TOGGLE FREQUENCY
- 74LS-SSI, MSI LIBRARY IMPLEMENTED
- ADVANCED CAD TELEDESIGN™* SOFTWARE SUPPORT
- VARIABLE DIE SIZE
- INDIVIDUALLY PROGRAMMABLE I/O BUFFERS
- COMPATIBLE WITH DIAL-A—CHIP℠** DESIGN AUTOMATION SYSTEM
- BI-DIRECTIONAL AND THREE STATE I/O
- TTL AND CMOS COMPATIBILITY
- COMMERCIAL TEMPERATURE RANGE
- MILITARY TEMPERATURE RANGE
- MULTIPLE PACKAGE OPTIONS

Description

Harris Custom Integrated Circuits Division offers a complete family of custom and semicustom products. The HARRIS Standard Cell product is a very cost effective alternative to gate arrays or full custom. The standard cell circuit is manufactured using the HARRIS state-of-the-art SAJI IV local oxidation process. The process offers 3 μm channel lengths with typical gate delays of 3ns and toggle frequencies of 50MHz. Each input-output buffer can be individually programmed as input, output, three-state or bi-directional. CMOS and TTL compatibility can be specified. The same SSI MSI 74LS functions used to design the gate array are used for the standard cell circuits.

The logic description and simulator functions are identical for both standard cell circuits and gate arrays. However, the standard cell circuit dimensions can change dynamically for each individual circuit. Where the gate array is a fixed number of gates and fixed chip size, the standard cell uses only enough silicon to fully implement the desired logic function. Typically a standard cell chip is 30% smaller than a fully utilized gate array offering a cost savings benefit to those customers with medium to high volumes.

The standard cell chip does require a complete set of masks rather than the three required by the gate array. The standard cell circuit is fully supported by the HARRIS Teledesign™ software and the HARRIS Dial-A-Chip℠ timeshare service. This allows the customer to perform as much of the design and development as he desires from his own office with a data terminal.

* Trademark of Harris Corporation
** Servicemark of Harris Corporation

HARRIS

HGA-C00600
HGA-C01200
HGA-C02500

CMOS Gate Array

Features

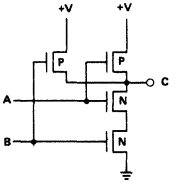
- 3 MICRON CMOS TECHNOLOGY
- 600, 1200, AND 2500 GATE ARRAYS
- 3ns TYPICAL GATE DELAY
- 50 MHz TOGGLE FREQUENCY
- 74LS- SSI, MSI LIBRARY IMPLEMENTED
- ADVANCED CAD TELEDESIGN™ SOFTWARE SUPPORT
- COMPATIBLE WITH DIAL-A-CHIP℠ DESIGN AUTOMATION SYSTEM
- INDIVIDUALLY PROGRAMMABLE I/O BUFFERS
- BI-DIRECTIONAL AND THREE STATE I/O
- TTL AND CMOS COMPATIBILITY
- COMMERCIAL TEMPERATURE RANGE
- MILITARY TEMPERATURE RANGE
- MULTIPLE PACKAGE OPTIONS

CMOS Gate Array Family

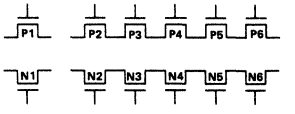
PART NO.	TRANSISTOR	GATE EQUIV.	DIE SIZE (MILS)	I/O PINS	ROWS/ CELLS
HGA-C00600	2592	648	198 X 165	54	6 X 36
HGA-C01200	5184	1296	257 X 198	78	12 X 36
HGA-C02500	10,080	2520	272 X 287	100	14 X 60

* One gate equivalent is equal to one 2-input nand.

TWO-INPUT NAND
1 GATE EQUIVALENT



BASIC CELL



Description

Harris Custom Integrated Circuits Division offers a complete family of custom and semicustom logic. The HGA-C00600, HGA-C01200 and HGA-C02500 are three CMOS gate arrays manufactured using the HARRIS state-of-the-art SAJI IV process. This local oxidation process offers 3 m channel lengths and 2 minimum features. Typical propagation gate delay is 3ns with 50MHz toggle frequencies possible. Personalization is accomplished by patterning two levels of interconnection on three mask layers: polysilicon, contacts and metal.

The entire process is fully supported by advanced CAD Teledesign™* software. With the HARRIS Dial-A-Chip℠** design automation system a customer chooses the amount of his participation in the design and development of his circuit. Using the HARRIS Teledesign™ timeshare system, logic description, simulation, and artwork editing can all be performed by the customer in his own office via a digital data communications link or if he so chooses, he may use the Customer Design Center in Melbourne.

The HARRIS system minimizes the amount of design and logic coding by offering a library of 74LS equivalent SSI and MSI function designs. There is no need to implement large MSI functions with primative gates. Each function has a complete data sheet specifying propagation delays and A. C. parameters. A final software program verifies that the original logic description matches the finished artwork.

Each input-output buffer can be individually specified to be input, output, three-state, or bi-directional. CMOS or TTL compatiblity can also be specified. The large number of I/O buffers keeps the input/output to gate ratio high insuring that the design is not pin limited.

Transition from gate arrays to standard cell circuits is very simple. The same logic description files are used as input to the Dial-A-Chip℠ software. Both utilize the same SSI, MSI 74LS library.

*Trademark of Harris Corporation
**Servicemark of Harris Corporation

HCA SSI/MSI LIBRARY

For use with HARRIS CMOS Gate Array
and Standard Cell Family

HCA000XB	DUAL 2 INPUT NAND
HCA000IB	DUAL 2 INPUT NAND WITH INVERTER
HCA002XB	DUAL 2 INPUT NOR
HCA002IB	DUAL 2 INPUT NOR WITH INVERTER
HCA004XB	TRIPLE INVERTER
HCA007XB	HIGH FANOUT BUFFER (5 pF DRIVE)
HCA008XB	2 INPUT AND
HCA010XB	3 INPUT NAND
HCA011XB	3 INPUT AND
HCA020XB	4 INPUT NAND
HCA021XB	4 INPUT AND
HCA027XB	3 INPUT NOR
HCA029XB	6 INPUT NAND
HCA030XB	8 INPUT NAND
HCA032XB	2 INPUT OR
HCA051XB	4 INPUT AND-OR-INVERT GATE
HCA073XB	JK FLIP FLOP WITH RESET
HCA074RB	D FLIP FLOP WITH RESET
HCA074SB	D FLIP FLOP WITH SET
HCA074XB	D FLIP FLOP WITH SET AND RESET
HCAN74RB	D FLIP FLOP WITH RESET—NEGATIVE EDGE TRIGGERED
HCAN74SB	D FLIP FLOP WITH SET—NEGATIVE EDGE TRIGGERED
HCAN74XB	D FLIP FLOP WITH SET AND RESET—NEGATIVE EDGE TRIGGERED
HCA075XB	QUAD D TYPE LATCH WITH INDIVIDUAL RESETS
HCA083SB	BCD FULL ADDER
HCA085XB	4-BIT MAGNITUDE COMPARATOR
HCA086XB	2 INPUT EXCLUSIVE OR
HCA138XB	3 TO 8 LINE DECODER
HCA139XB	2 TO 4 LINE DECODER
HCA152XB	8 TO 1 DATA SELECTOR
HCA157XB	QUAD 2 TO 1 DATA SELECTOR
HCA161XB	4-BIT SYNCHRONOUS BINARY COUNTER WITH ASYNCHRONOUS RESET
HCA163XB	4-BIT SYNCHRONOUS BINARY COUNTER WITH SYNCHRONOUS RESET
HCA164XB	8-BIT PARALLEL OUTPUT SHIFT REGISTER
HCA165XB	8-BIT PARALLEL LOAD SHIFT REGISTER
HCA173XB	4-BIT D REGISTER WITH THREE STATE OUTPUTS
HCA175XB	QUAD D FLIP FLOP WITH RESET
HCA180XB	9-BIT PARITY GENERATOR
HCA192XB	4-BIT SYNCHRONOUS UP DOWN DECADE COUNTER
HCA193XB	4-BIT SYNCHRONOUS UP DOWN BINARY COUNTER
HCA194XB	4-BIT SYNCHRONOUS LOAD BI-DIRECTIONAL SHIFT REGISTER
HCA225XB	EXPANDABLE 4 WORD BY 1 BIT FIFO
HCA240XB	OCTAL INVERTING THREE STATE BUFFER
HCA244XB	OCTAL NON-INVERTING THREE STATE BUFFER
HCA257XB	QUAD 2 TO 1 LINE DATA SELECTOR
HCA273XB	OCTAL D FLIP FLOP WITH COMMON CLOCK
HCA283XB	4-BIT BINARY FULL ADDER WITH FAST CARRY
HCA352XB	DUAL 4 TO 1 LINE DATA SELECTOR
HCA377XB	OCTAL D FLIP FLOP WITH ENABLE
HCA393XB	4-BIT BINARY RIPPLE COUNTER
HCA645XB	OCTAL BUS TRANSCEIVER
HCA1000B	15:1 RATIO PULL UP RESISTOR WITH ENABLE

HCA SSI/MSI LIBRARY

For use with HARRIS CMOS Gate Array
and Standard Cell Family

GATE ARRAY I/O BUFFERS

HCA900XB	CMOS INPUT BUFFER
HCA901XB	CMOS INPUT BUFFER WITH 18K PULL UP RESISTOR
HCA910XB	TTL INPUT BUFFER
HCA911XB	TTL INPUT BUFFER WITH 18K PULL UP RESISTOR
HCA950XB	3.2 MA OUTPUT BUFFER
HCA951XB	3.2 MA OUTPUT BUFFER—OPEN DRAIN P-CHANNEL
HCA952XB	3.2 MA OUTPUT BUFFER—OPEN DRAIN N-CHANNEL
HCA960XB	3.2 MA OUTPUT BUFFER—THREE STATE
HCA970XB	3.2 MA BI-DIRECTIONAL BUFFER—CMOS INPUT
HCA971XB	3.2 MA BI-DIRECTIONAL BUFFER—CMOS INPUT WITH 18K PULL UP
HCA980XB	3.2 MA BI-DIRECTIONAL BUFFER—TTL INPUT
HCA981XB	3.2 MA BI-DIRECTIONAL BUFFER—TTL INPUT WITH 18K PULL UP RESISTOR
HCAVSSXB	PLACEABLE VSS I/O PAD
HCAVIA	VIA CELL

STANDARD CELL I/O BUFFERS

HCC900XB	CMOS INPUT BUFFER
HCC901XB	CMOS INPUT BUFFER WITH 18K PULL UP
HCC905XB	CMOS INPUT BUFFER—INVERTING
HCC906XB	CMOS INPUT BUFFER—INVERTING WITH PULL UP
HCC908XB	SCHMITT TRIGGER INPUT BUFFER
HCC910XB	TTL INPUT BUFFER
HCC911XB	TTL INPUT BUFFER WITH 18K PULL UP
HCC915XB	TTL INPUT BUFFER WITH 18K PULL UP INVERTING
HCC950XB	3.2 MA OUTPUT BUFFER
HCC951XB	3.2 MA OUTPUT BUFFER WITH OPEN DRAIN P-CHANNEL
HCC952XB	3.2 MA OUTPUT BUFFER WITH OPEN DRAIN N-CHANNEL
HCC955XB	8.0 MA OUTPUT BUFFER
HCC960XB	3.2 MA OUTPUT BUFFER THREE STATE
HCC965XB	8.0 MA OUTPUT BUFFER THREE STATE
HCC970XB	3.2 MA BI-DIRECTIONAL WITH CMOS INPUT
HCC971XB	3.2 MA BI-DIRECTIONAL CMOS INPUT AND 18K PULL UP
HCC975XB	8.0 MA BI-DIRECTIONAL WITH CMOS INPUT
HCC976XB	8.0 MA BI-DIRECTIONAL CMOS INPUT AND 18K PULL UP
HCC980XB	3.2 MA BI-DIRECTIONAL TTL INPUT
HCC981XB	3.2 MA BI-DIRECTIONAL TLL INPUT AND 18K PULL UP
HCC985XB	8.0 MA BI-DIRECTIONAL TTL INPUT
HCC986XB	8.0 MA BI-DIRECTIONAL TTL INPUT AND 18K PULL UP
HCC990XB	UNBUFFERED INPUT WITH STATIC PROTECTION
HCCVDDYB	VDD SUPPLY PAD
HCCVSSYB	VSS SUPPLY PAD

HIGH DENSITY HD CELL LIBRARY (PRIMITIVE FUNCTIONS)

CELL	FUNCTIONAL DESCRIPTION	SIZE	DELAY	TRANS
HD1100	LOGIC I/O CONNECTION	132 x 20 μm	N/A	N/A
HD1110	INVERTER	132 x 30 μm	3.0 ns	4.7 ns
HD1130	3X INVERTER	132 x 40 μm	2.7 ns	4.5 ns
HD1150	5X INVERTER	132 x 50 μm	3.1 ns	5.0 ns
HD1160	CMOS BUFFER	132 x 50 μm	2.7 ns	1.5 ns
HD1180	TTL TO CMOS BUFFER	132 x 50 μm	4.0 ns	2.5 ns
HD1210A	2 INPUT NAND	132 x 40 μm	3.0 ns	5.0 ns
HD1220	2 INPUT AND	132 x 50 μm	3.5 ns	2.7 ns
HD1230	2 INPUT NOR	132 x 40 μm	3.0 ns	5.3 ns
HD1240	2 INPUT OR	132 x 50 μm	3.5 ns	3.0 ns
HD1310	3 INPUT NAND	132 x 50 μm	3.1 ns	4.9 ns
HD1320A	3 INPUT AND	132 x 60 μm	3.3 ns	2.8 ns
HD1330A	3 INPUT NOR	132 x 50 μm	3.3 ns	5.6 ns
HD1340	3 INPUT OR	132 x 70 μm	3.8 ns	2.8 ns
HD1410	4 INPUT NAND	132 x 60 μm	3.3 ns	5.0 ns
HD1420	4 INPUT AND	132 x 70 μm	3.5 ns	2.5 ns
HD1430	4 INPUT NOR	132 x 90 μm	4.8 ns	3.0 ns
HD1440	4 INPUT OR	132 x 80 μm	3.5 ns	2.6 ns
HD2120	EXCLUSIVE—OR	132 x 80 μm	4.7 ns	3.5 ns
HD2130	EXCLUSIVE—NOR	132 x 70 μm	5.4 ns	3.4 ns
HD2140	TRANSMISSION GATE	132 x 40 μm	1.2 ns	7.3 ns
HD2150	TRI-STATE INV	132 x 50 μm	2.0 ns	4.4 ns
HD2210	4 TO 1 MUX	132 x 240 μm	5.0 ns	5.0 ns
HD2220	2 TO 1 MUX	132 x 100 μm	3.9 ns	2.5 ns
HD2230	2, 2—AND, 2—NOR	132 x 60 μm	4.1 ns	6.6 ns
HD2240	2, 3—AND, 2—NOR	132 x 80 μm	4.4 ns	6.9 ns
HD2250	3, 2—AND, 3—NOR	132 x 80 μm	4.8 ns	7.8 ns
HD3100	D FF	132 x 120 μm	2.5 ns	3.2 ns
HD3110	D FF W/RESET	132 x 150 μm	3.4 ns	3.2 ns
HD3120	D FF W/RESET, QBR	132 x 170 μm	4.3 ns	4.0 ns
HD3130	D FF W/SET, RESET	132 x 180 μm	5.0 ns	3.8 ns
HD3140	D FF W/SET, QBAR	132 x 170 μm	4.2 ns	4.2 ns
HD3150	D FF W/QBAR	132 x 140 μm	4.5 ns	3.5 ns
HD3200A	JK FF	132 x 160 μm	4.5 ns	5.0 ns
HD3210	JK FF W/RESET	132 x 180 μm	4.8 ns	4.8 ns
HD3220A	JK FF W/RESET, QBR	132 x 210 μm	5.4 ns	3.5 ns
HD3230	JK FF W/SET, RESET	132 x 250 μm	5.4 ns	4.3 ns
HD3240	JK FF W/SET	132 x 210 μm	5.0 ns	5.4 ns
HD3250	JK FF W/QBAR	132 x 210 μm	6.7 ns	7.0 ns
HD3260A	JK FF W/R, QBAR (POS)	132 x 210 μm	5.5 ns	3.6 ns
HD5040A	4-BIT SHIFT REGISTER	132 x 340 μm	4.6 ns	4.6 ns
HD5060A	6-BIT SHIFT REGISTER	132 x 500 μm	4.6 ns	4.6 ns

NOTE: DESIGN AND DEVELOPMENT SUPPORT FOR THIS LIBRARY IS PROVIDED BY CUSTOM INTEGRATED CIRCUITS DIVISION ENGINEERING.

CELL	FUNCTIONAL DESCRIPTION		SIZE	DELAY	TRANS
HD5080A	8-BIT SHIFT REGISTER		132 x 660 μm	4.6 ns	4.6 ns
HD6210	2 INPUT NAND (INV)		132 x 50 μm	3.4 ns	4.9 ns
HD6220	2 INPUT AND (INV)		132 x 70 μm	4.0 ns	3.0 ns
HD6230	2 INPUT NOR (INV)		132 x 60 μm	4.0 ns	5.3 ns
HD6240	2 INPUT OR (INV)		132 x 50 μm	3.4 ns	5.0 ns
HD6310	3 INPUT NAND (INV)		132 x 70 μm	3.7 ns	4.9 ns
HD6320	3 INPUT AND (INV)		132 x 80 μm	4.5 ns	3.0 ns
HD6330	3 INPUT NOR (INV)		132 x 70 μm	4.2 ns	5.6 ns
HD6340	3 INPUT OR (INV)		132 x 80 μm	4.5 ns	3.1 ns
HD6410	4 INPUT NAND (INV)		132 x 80 μm	4.0 ns	5.1 ns
HD6420A	4 INPUT AND (INV)		132 x 80 μm	5.3 ns	2.6 ns
HD6430	4 INPUT NOR (INV)		132 x 110 μm	5.0 ns	2.6 ns
HD6440	4 INPUT OR (INV)		132 x 100 μm	4.7 ns	3.1 ns
HD8120A	P CHAN TEST DEVICES		239 x 269 μm	N/A	N/A
HD8220A	N CHAN TEST DEVICES		239 x 269 μm	N/A	N/A
HD8310AQ	N- TEST CAPACITOR		174 x 397 μm	N/A	N/A
HD8320	P- TEST CAPACITOR		186 x 358 μm	N/A	N/A
HD8420A	TEST RESISTORS		185 x 251 μm	N/A	N/A
HD8510	ALIGNMENT MARKS		66 x 302 μm	N/A	N/A
HD8520	MASK REVISION ID		64 x 272 μm	N/A	N/A
HD8530	CRITICAL DIMENSION		86 x 174 μm	N/A	N/A
HD8610	CORNER ROT. MARK 1		28 x 78 μm	N/A	N/A
HD8620	CORNER ROT. MARK 2		28 x 78 μm	N/A	N/A
HD8710	COPYRIGHT SYMBOL		82 x 87 μm	N/A	N/A
HD8720	"HARRIS"		34 x 239 μm	N/A	N/A
HD8730	HARRIS LOGO		146 x 146 μm	N/A	N/A
HD8750	CICD		40 x 154 μm	N/A	N/A
HD8810	#1 PAD ID (1 SIDE)		21 x 105 μm	N/A	N/A
HD8820	#2 PAD ID (2 SIDES)		126 x 126 μm	N/A	N/A
HD8910	VIA		6 x 6 μm	N/A	N/A
HD8920	FEED THROUGH CELL		132 x 10 μm	N/A	N/A
HD9100	VDD TYPE A		314 x 170 μm	N/A	N/A
HD9130	VSS TYPE B		314 x 170 μm	N/A	N/A
HD9210	INPUT W/PROTECT	A	314 x 240 μm	N/A	N/A
HD9220	INPUT W/PULLUP	A	314 x 250 μm	N/A	N/A
HD9230	INPUT W/PULLDOWN	A	314 x 280 μm	N/A	N/A
HD9240	BUFFERED OUTPUT	A	314 x 320 μm	6.1 ns	4.1 ns
HD9250	BI-DIRECTIONAL	A	314 x 390 μm	6.8 ns	5.0 ns
HD9310	INPUT W/PROTECT	B	314 x 240 μm	N/A	N/A
HD9320	INPUT W/PULLUP	B	314 x 260 μm	N/A	N/A
HD9330	INPUT W/PULLDOWN	B	314 x 280 μm	N/A	N/A
HD9340	BUFFERED OUTPUT	B	314 x 320 μm	6.1 ns	4.1 ns
HD9350	BI-DIRECTIONAL	B	314 x 390 μm	6.8 ns	5.0 ns

NOTE: DESIGN AND DEVELOPMENT SUPPORT FOR THIS LIBRARY IS PROVIDED BY CUSTOM INTEGRATED CIRCUITS DIVISION ENGINEERING.

RADIATION HARDENED CMOS PRODUCTS

- Current Products
- Future Products

CURRENT RADIATION HARDENED CMOS PRODUCTS

BUS INTERFACE CIRCUITS

HS-15530RH	Rad Hard Mil. Std. 1553 Encoder/Decoder (24 Pins)

RAD HARD MEMORIES

HS-6504RH	Rad Hard 4K x 1 CMOS RAM
HS-6508RH	Rad Hard 1K x 1 CMOS RAM
HS-6514RM	Rad Hard 1K x 4 CMOS RAM
HS-6551RH	Rad Hard 256 x 4 CMOS RAM
HS-6564RH	Rad Hard 64K Memory Module (8K x 8 or 16K x 4)
HS-6532RH	Rad Hard 32K Memory Module (8K x 4 or 16K x 2)

ANALOG SWITCHES/MULTIPLEXERS

HS-508ARM	Rad Hard 8 Channel Multiplexer
HS-1840RH	Rad Hard 16 Channel Multiplexer

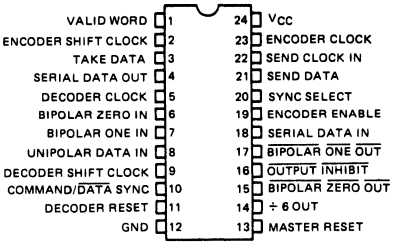
HS-1553ORH

Radiation Resistant CMOS Manchester Encoder-Decoder

Features

- SUPPORT OF MIL-STD-1553
- 1.0 MEGABIT/SEC DATA RATE
- SYNC IDENTIFICATION AND LOCK-IN
- CLOCK RECOVERY
- MANCHESTER II ENCODE, DECODE
- SEPARATE ENCODE AND DECODE
- LOW OPERATING POWER: 50mW AT 5 VOLTS
- FULL MILITARY TEMPERATURE RANGE
- FUNCTIONAL TOTAL DOSE . . . 1 x 10^4 RAD(Si)
- LATCH-UP FREE TO ..... 5 x 10^{11} RAD (Si)/sec

Pinout



Description

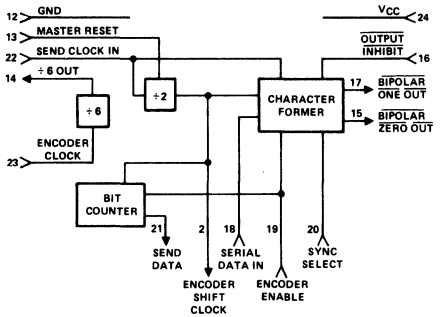
The Harris HS-15530RH is a high performance, radiation resistant, CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocals. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate completely independent of each other, except for the Master Reset function.

This circuit provides many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

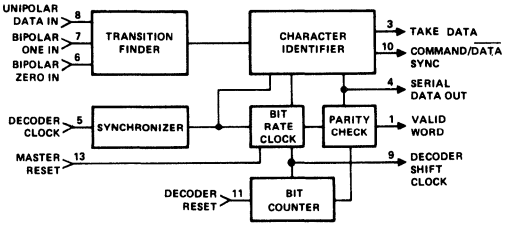
This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL- STD-1553 over both temperature and voltage while residing in a radiation environment . It interfaces with CMOS, TTL or N channel support circuitry, and uses a standard 5 volt supply.

Block Diagrams

ENCODER



DECODER



9 CICD

HARRIS

HS-6504RH

4096 x 1 CMOS RAM

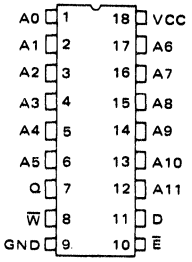
Preliminary

Features

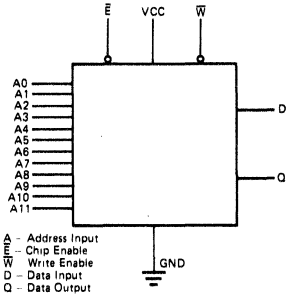
- LOW POWER STANDBY — 25μW TYP.
- LOW POWER OPERATION — 25mW/MHz TYP.
- EXTREMELY LOW SPEED POWER PRODUCT
- FUNCTIONAL TOTAL DOSE — 1×10^5 RAD Si
- DATA UPSET — $> 10^8$ RAD Si/s
- LATCH - UP FREE TO — $> 5 \times 10^{11}$ RAD Si/s
- TTL COMPATIBLE INPUT/OUTPUT
- THREE - STATE OUTPUT
- STANDARD JEDEC PINOUT
- FAST ACCESS TIME — 200nsec TYP.
- MILITARY TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER

Pinout

TOP VIEW



Logic Symbol



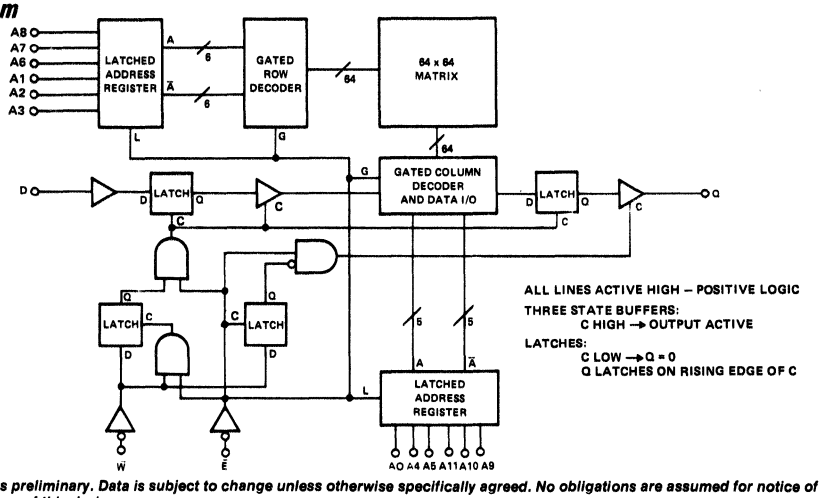
Description

The HS–6504RH is a 4096 x 1 static CMOS RAM fabricated using the Harris Custom Integrated Circuits Division radiation hardened self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On-chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance for use in expanded memory arrays.

The HS–6504RH is a fully static RAM and may be maintained in any state for an indefinite period of time.

Functional Diagram



Information on this device is preliminary. Data is subject to change unless otherwise specifically agreed. No obligations are assumed for notice of change or future manufacture of this device.

CAUTION: These devices are sensitive to electrostatic discharge.

HS-6508RH

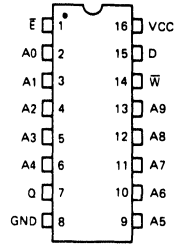
1024 x 1 CMOS RAM

Features

- FUNCTIONAL TOTAL DOSE . . . . . 2×10^4 RAD Si
- LATCH-UP FREE TO . . . . . 5.0×10^{11} RAD Si/sec
- LOW STANDBY POWER . . . . . 550 μW MAX
- LOW OPERATING POWER . . . . . 25mW/MHz MAX
- FAST ACCESS TIME . . . . . 300nsec MAX
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE – 2 TTL LOADS
- HIGH NOISE IMMUNITY
- ON-CHIP ADDRESS REGISTER
- MILITARY TEMPERATURE RANGE
- THREE-STATE OUTPUTS
- 16 PIN PACKAGE FOR HIGH DENSITY

Pinout

TOP VIEW



A – Address Input
Ē – Chip Enable
W̄ – Write Enable
D – Data Input
Q – Data Output

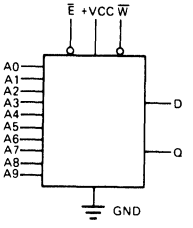
Description

The HS-6508RH is a 1024 by 1 static CMOS RAM fabricated using the HARRIS Programs Division radiation hardened self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

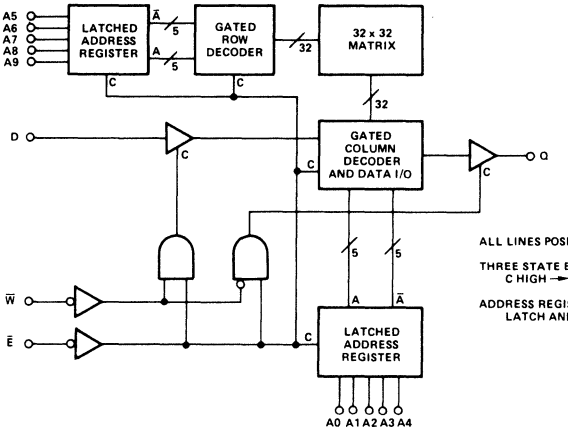
On-chip latches are provided for addresses allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HS-6508RH is a fully static RAM and may be maintained in any state for an indefinite period of time.

Logic Symbol



Functional Diagram



ALL LINES POSITIVE LOGIC – ACTIVE HIGH

THREE STATE BUFFERS:
C HIGH → OUTPUT ACTIVE

ADDRESS REGISTER AND DECODERS.
LATCH AND GATE ON RISING EDGE OF C

9 CICD

HARRIS

HS-6514RH

1024 x 4 CMOS RAM

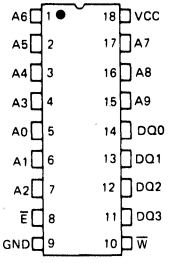
Preliminary

Features

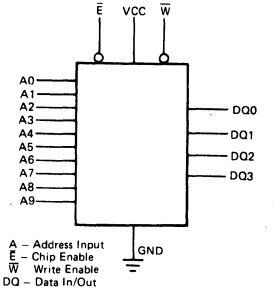
- LOW POWER STANDBY — 25μW TYP.
- LOW POWER OPERATION — 25mW/MHz TYP.
- FUNCTIONAL TOTAL DOSE — 1 x 10^5 RAD Si
- DATA UPSET — > 10^8 RADS Si/s
- LATCH - UP FREE TO — > 5 x 10^{11} RAD Si/s
- TTL COMPATIBLE INPUT/OUTPUT
- COMMON DATA IN/OUT
- THREE - STATE OUTPUTS
- STANDARD JEDEC PINOUT
- FAST ACCESS TIME — 200ns TYP.
- MILITARY TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON - CHIP ADDRESS REGISTER

Pinout

TOP VIEW



Logic Symbol



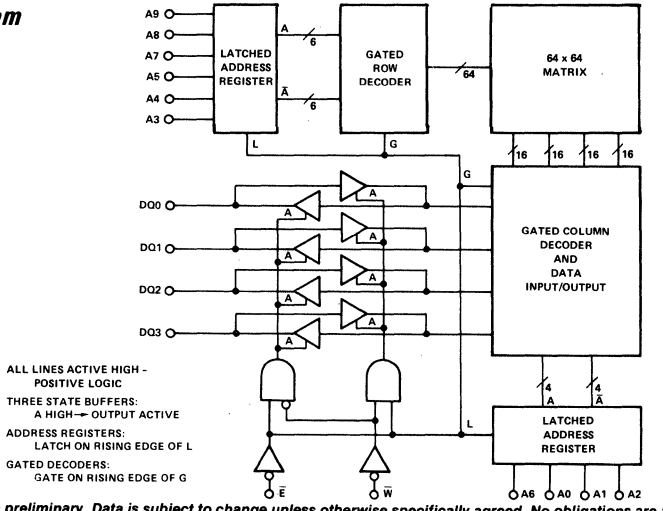
Description

The HS–6514RH is a 1024 x 4 static CMOS RAM fabricated using the Harris Custom Integrated Circuits Division radiation hardened self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On-chip latches are provided for the addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory systems.

The HS–6514RH is a fully static RAM and may be maintained in any state for an indefinite period of time.

Functional Diagram



Information on this device is preliminary. Data is subject to change unless otherwise specifically agreed. No obligations are assumed for notice of change or future manufacture of this device.

CAUTION: These devices are sensitive to electrostatic discharge.

HARRIS

HS-6551RH

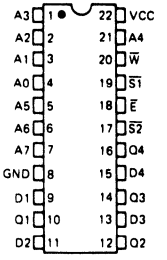
256 x 4 CMOS RAM

Features

- FUNCTIONAL TOTAL DOSE — 2×10^4 RAD Si
- LATCH-UP FREE TO — 5.0×10^{11} RAD Si/sec
- LOW STANDBY POWER — 550μW MAX
- LOW OPERATING POWER — 25mW/MHz MAX
- FAST ACCESS TIME — 300ns MAX
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE - 1TTL LOAD
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTER
- MILITARY TEMPERATURE RANGE
- THREE-STATE OUTPUTS
- 22 PIN PACKAGE FOR HIGH DENSITY

Pinout

TOP VIEW



A – Address Input
$\overline{E}$ – Chip Enable
$\overline{S}$ – Chip Select
$\overline{W}$ – Write Enable
D – Data Input
Q – Data Output

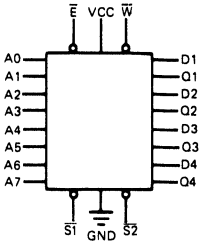
Description

The HS-6551RH is a 256 by 4 static CMOS RAM fabricated using the Harris Programs Division radiation hardened self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

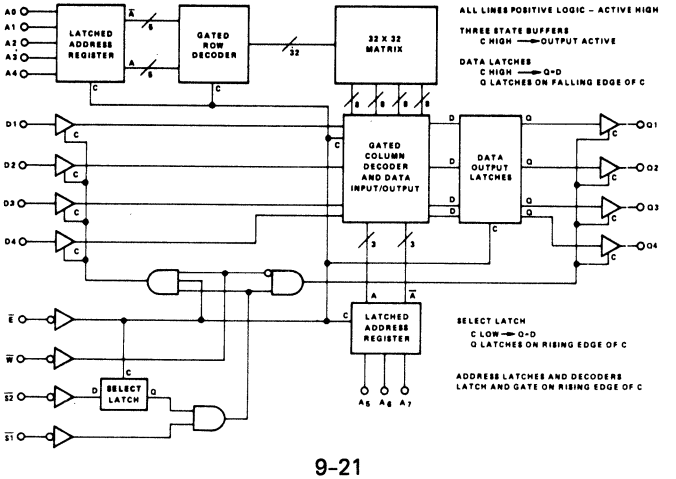
On-chip latches are provided for addresses, allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HS-6551RH is a fully static RAM and may be maintained in any state for an indefinite period of time.

Logic Symbol



Functional Diagram



HARRIS

Preliminary

HS-6564RH

Radiation Resistant 8K x 8, 16K x 4 CMOS RAM

Features

• LOW POWER STANDBY	500μW MAX
• LOW POWER OPERATION	180mW/MHz MAX
• DATA RETENTION	3.0 V MIN
• TTL COMPATIBLE IN/OUT	
• THREE STATE OUTPUTS	
• FAST ACCESS TIME	250 nsec TYP.
• MILITARY TEMPERATURE RANGE	-55°C TO +125°C
• ON CHIP ADDRESS REGISTERS	
• ORGANIZABLE 8K×8 OR 16K×4	
• 40 PIN DIP PINOUT 2.000″ × 0.900″	
• FUNCTIONAL TOTAL DOSE	1×10^5 RAD Si
• DATA UPSET	$>10^{9}$ RAD Si/SEC
• LATCH-UP FREE TO	$> 5 \times 10^{11}$ RAD Si/SEC

Description

The HS-6564RH is a radiation resistant 64K bit, synchronous CMOS RAM. It consists of 16 HS-6504RH 4K×1 radiation resistant CMOS RAMs, in leadless carriers, mounted on a ceramic substrate. The HS-6564RH is configured as an extra wide, standard length 40 pin DIP. The memory appears to the system as an array of 16 4K×1 static RAMs. The array is organized as two 8K by 4 blocks of RAM sharing only the address bus. The data inputs, data outputs, chip enables and write enables are separate for each block of RAM. This allows the user to organize the HS-6564RH RAM as either an 8K by 8 or a 16K by 4 array.

This 64K memory provides a unique blend of low power CMOS semiconductor technology and advanced packaging techniques. The HS-6564RH is intended for use in radiation environments where a large amount of RAM is needed, and where power consumption and board space are prime concerns. On-chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance for use in expanded memory arrays. The guaranteed low voltage data retention characteristics allow easy implementation of non-volatile read/write memory by using very small batteries mounted directly on the memory circuit board.

Pinout

TOP VIEW

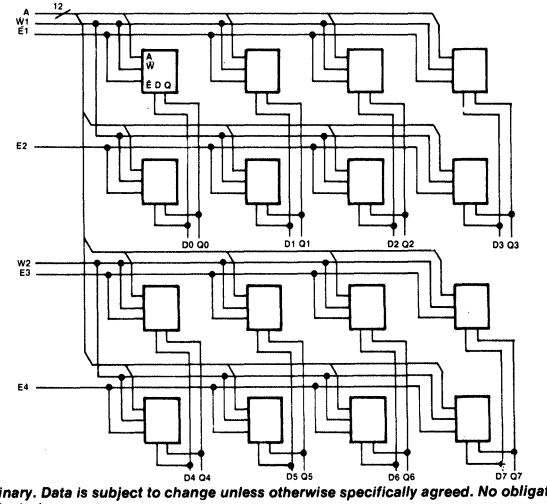
*GND	1	40	VCC*
Q4	2	39	Q0
D4	3	38	D0
Q5	4	37	Q1
D5	5	36	D1
A0	6	35	A6
A1	7	34	A7
A4	8	33	A8
$\overline{E}3$	9	32	$\overline{E}1$
*$\overline{W}2$	10	31	$\overline{W}1$
$\overline{W}2$	11	30	$\overline{W}1$*
$\overline{E}4$	12	29	$\overline{E}2$
A11	13	28	A3
A10	14	27	A2
A9	15	26	A5
D6	16	25	D2
Q6	17	24	Q2
D7	18	23	D3
Q7	19	22	Q3
*VCC	20	21	GND*

***NOTES:**

Pins 20 and 40 (VCC) are internally connected. Similarly pins 1 and 21 (Ground) are connected. The user is advised to connect all four VCC pins and Ground pins to his board busses. This will improve power distribution across the array and will enhance decoupling.

Pin 10 is internally connected to pin 11, and pin 30 is connected to pin 31. For those users wishing to preserve board compatibility with possible future RAM arrays, we recommend connections to the write lines be made at pins 11 and 31, leaving pins 10 and 30 free for future expansion.

Functional Diagram



Information on this device is preliminary. Data is subject to change unless otherwise specifically agreed. No obligations are assumed for notice of change or future manufacture of this device.

CAUTION: These devices are sensitive to electronic discharge.

HARRIS

Preliminary

HS-508ARH

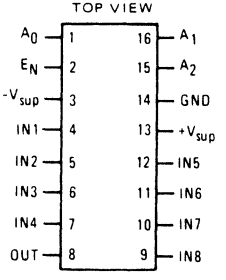
Radiation Resistant 8 Channel CMOS Analog Multiplexer With Overvoltage Protection

Features

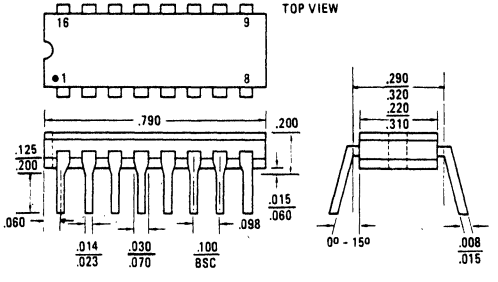
- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK-BEFORE-MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME (TYP.) 500ns
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE (TYP.) 4mA
- STANDBY POWER (TYP.) 7.5mW
- RADIATION ENVIRONMENT

NEUTRON FLUENCE (ϕ) 1×10^9 n/cm^2 (E $\geqslant$ 10KeV)
GAMMA RATE ($\dot{\gamma}$) . . . . . 1×10^8 RADs(Si)/s
GAMMA DOSE (γ) . . . . . 1×10^5 RADs(Si)

Pinout



Package



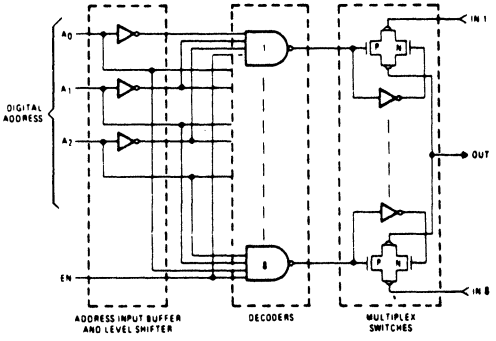
CAUTION: These devices are sensitive to electrostatic discharge.

Description

The HS-508ARH is a dielectrically isolated, radiation resistant, CMOS analog multiplexer incorporating an important feature; it withstands analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important, it can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage current combine to produce low errors. Reference Application Notes 520 and 521, available from the Analog Products Division of Harris, for further information on the 508A multiplexer in general.

The HS-508ARH has been specifically designed to meet exposure to radiation environments. Operation from −55°C to +125°C is guaranteed.

Functional Diagram



9 CICD

HARRIS

Preliminary

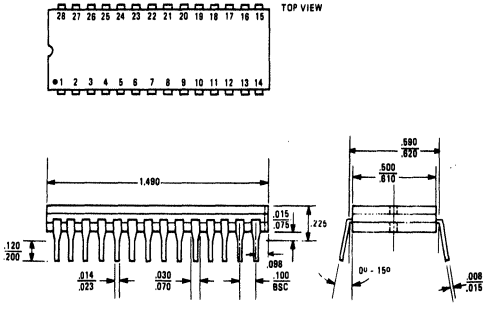
HS-1840RH

Radiation Resistant 16 Channel CMOS Analog Multiplexer with High-Z Analog Input Protection

Features

- HIGH ANALOG INPUT IMPEDANCE DURING POWER LOSS (OPEN) — 500MΩ
- LOW POWER CONSUMPTION (STANDBY) — 600μW
- ACCESS TIME — 500ns
- EXCELLENT IN HI-REL REDUNDANT SYSTEMS
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP
- RADIATION ENVIRONMENT
  - NEUTRON FLUENCE (ϕ) . 1×10^9 n/cm^2(E ≥ 10KeV)
  - GAMMA RATE ($\dot{\gamma}$) . . . . . 1×10^8 RADs (Si)/s
  - GAMMA DOSE (γ) . . . . . 2×10^5 RADs(Si)

Package



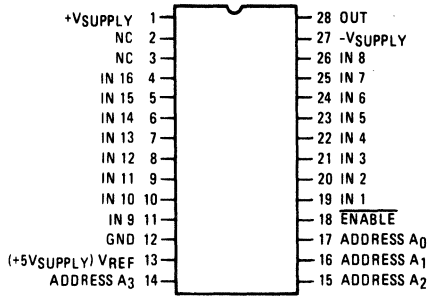
Description

The HS-1840RH is a radiation resistant, monolithic 16 channel multiplexer constructed with the Harris Linear Dielectric Isolation CMOS process. It is designed to provide a high input impedance to the analog source if device power fails (open) or the analog signal voltage inadvertently exceeds the supply rails during powered operation. Excellent for use in redundant applications, since the secondary device can be operated in a standby unpowered mode affording no additional power drain. But more significantly, a very high impedance exists between the active and inactive devices preventing any interaction. One of sixteen channel selection is controlled by a 4-bit binary address plus an Enable-Inhibit input which conveniently controls the ON/OFF operation of several multiplexers in a system. All digital inputs have electrostatic discharge protection.

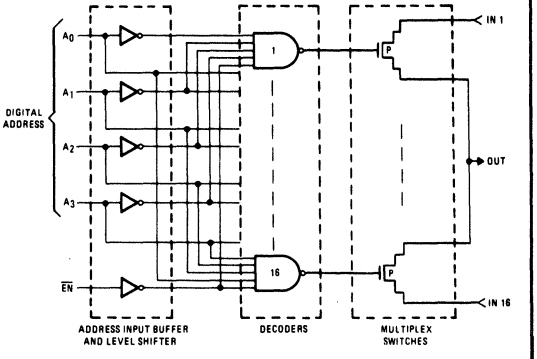
The HS-1840RH has been specifically designed to meet exposure to radiation environments. It is available in a 28 pin dual-in-line package and is guaranteed operational from −55°C to +125°C.

Pinout

TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge.

FUTURE RADIATION HARDENED PRODUCTS

FUTURE RADIATION HARDENED 80C85 FAMILY				
DEVICE	SANDIA P/N	INDUSTRY EQUIVALENT	HCICD P/N	AVAIL-ABILITY
8 Bit CPU 256 x 8 CMOS RAM with I/O Ports and Timer	SA3000 SA3001	8085 8155/56	HS-80C85RH HS-8155/56RH	2Q '84 2Q '84
2K x 8 CMOS RAM	SA3002	8355	HS-8355RH	2Q '84
3 to 8 Line Decoder	SA2995	74138	–	2Q '84
Bi-directional CMOS/TTL Level Converter	SA2996	40116	–	2Q '84
Bus Transceiver	SA2997	8208	–	2Q '84
Input/Output Port	SA3026	8212	–	2Q '84

FUTURE RADIATION HARDENED PROMs				
DEVICE	ORGANI-ZATION	INDUSTRY EQUIVALENT	COMMENTS	AVAIL-ABILITY
4K CMOS PROM	512 x 8	HM-6641	• Latch-up Free • Total Dose Goal $\geq 1 \times 10^5$ RADS (Si)	2Q '84

FUTURE RADIATION HARDENED STATIC RAMs			
DEVICE	ORGANI-ZATION	COMMENTS	AVAIL-ABILITY
16K CMOS STATIC Asynchronous RAM	16K x 1	• Immune to single event upset • Total Dose Tolerant to $\geq 5 \times 10^5$ RADs (Si) • Latch-up Free	2Q '84

SPECIALIZED PRODUCTS

Bus Interface Circuits

- HS-3182 ARINC 429 Line Driver
- HS-3282 ARINC 429 Line Receiver/Transmitter

Other

- HS-3819 Video Character Generator

HS-3182

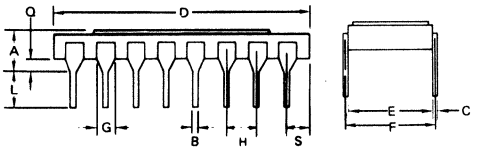
ARINC 429 Bus Interface Line Driver Circuit

Features

- INPUTS T^2L AND CMOS COMPATIBLE
- ADJUSTABLE RISE AND FALL TIMES VIA 2 EXTERNAL CAPACITORS
- PROGRAMMABLE OUTPUT DIFFERENTIAL RANGE VIA VOLTAGE REFERENCE INPUT (V_{REF})
- POWER STROBE INPUT PERMITS LOW QUIESCENT POWER OF < 20mW
- OUTPUTS ARE INHIBITED (0 VOLTS) IF DATA (A) AND DATA (B) INPUTS ARE BOTH IN THE "LOGIC ONE" STATE
- CAN OPERATE UP TO A 100 KILOBITS DATA RATE
- OUTPUT SHORT CIRCUIT PROOF AND CONTAINS OVERVOLTAGE PROTECTION
- DATA "A" AND DATA "B" SIGNALS ARE "AND'D" WITH CLOCK AND SYNC SIGNALS
- FULL MILITARY TEMPERATURE RANGE

Package

16 LEAD BRAZED DIP



LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S
16	— .200	.014 .023	.008 .015	— .840	.220 .310	.290 .320	.030 .070	.100 BSC	.125 .200	.015 .060	— .060

MIN. / MAX.

NOTE: DIMENSIONS IN INCHES

Description

The HS-3182 ARINC 429 bus interface driver circuit is a monolithic dielectrically isolated bipolar differential line driver designed to meet the specifications of ARINC 429. This device is intended to be used with a companion chip, HS-3282 CMOS ARINC bus interface circuit, which provides the data formatting and processor interface function.

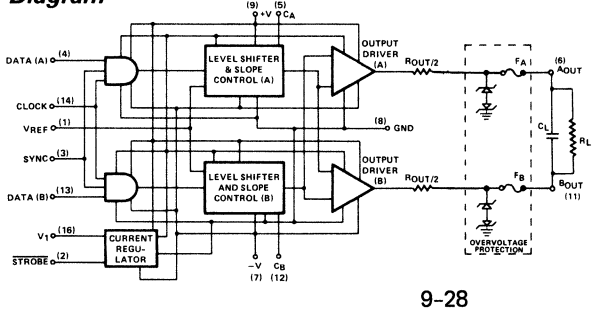
All logic inputs are T^2L and CMOS compatible. In addition to the DATA(A) and DATA(B) inputs there are also inputs for a CLOCK and SYNC signal which are AND'D with the DATA inputs. This feature was added to enhance system performance and to allow the HS-3182 to be used with devices other than the HS-3282. Also adding to system performance is the $\overline{\text{STROBE}}$ input. To minimize power consumption the $\overline{\text{STROBE}}$ input can be asserted to place the chip in the power-down mode where it draws substantially less current. Four power supplies are required; $+V = +15V \pm 10\%$, $-V = -15V \pm 10\%$, $V_1 = 5V \pm 5\%$ and V_{REF}. V_{REF} is used to program the output voltage swing, such that V_{OUT} (DIFF) $= \pm 2V_{REF}$. Typically, $V_{REF} = V_1 = 5V \pm 5\%$.

The driver output impedance is $75\Omega \pm 20\%$ at 25°C. Output rise and fall times are programmed through the use of two external capacitors, C_A and C_B. To meet the requirements for rise and fall times as specified in ARINC 429, $C_A = C_B = 75pF$ for the high speed operation (100 KBPS) and 500 pF for the low speed operation (12-14.5 KBPS). The outputs are protected against overvoltage and short circuit as shown in the Block Diagram. This device is designed to operate with a case temperature range of −55°C to +125°C.

Truth Table

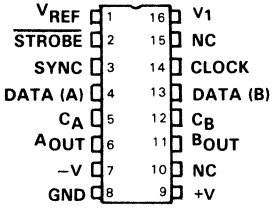
$\overline{\text{STROBE}}$	SYNC	CLOCK	DATA (A)	DATA (B)	A_{OUT}	B_{OUT}	COMMENTS
H	X	X	X	X	HI-Z	HI-Z	Power-Down State
L	X	L	X	X	OV	OV	NULL
L	L	X	X	X	OV	OV	NULL
L	H	H	L	L	OV	OV	NULL
L	H	H	L	H	$-V_{REF}$	$+V_{REF}$	LOW
L	H	H	H	L	$+V_{REF}$	$-V_{REF}$	HIGH
L	H	H	H	H	OV	OV	NULL

Block Diagram



Pinout

TOP VIEW



HARRIS

HS-3282

CMOS ARINC Bus Interface Circuit

Description

The Harris HS-3282 is a high performance CMOS bus interface circuit that is intended to meet the requirements of ARINC Specification 429, and similar encoded, time multiplexed serial data protocols. The ARINC 429 bus interface circuit consists of two (2) receivers and a transmitter operating independently as shown in Figure 1. The two receivers operate at a frequency that is ten (10) times the receiver data rate, which can be the same or different from the transmitter data rate. Although the two receivers operate at the same frequency, they are functionally independent and each receives serial data asynchronously. The transmitter section of the ARINC bus interface circuit consists mainly of a First-In First-Out (FIFO) memory and timing circuit. The FIFO memory is used to hold eight (8) ARINC data words for transmission serially. The timing circuit is used to correctly separate each ARINC word as required by ARINC Specification 429.

Even though ARINC Specification 429 specifies a 32-bit word, including parity, the HS-3282 can be programmed to also operate with a word length of 25 bits. The incoming receiver data word parity is checked, and a parity status is stored in the receiver latch and is outputted on Pin BD08 during the 1st word. [A logic "0" indicates that an odd number of logic "1"s were received and stored; a logic "1" indicates that an even number of logic "1"s were received and stored]. In the transmitter the parity generator will generate either odd or even parity depending upon the status of PARCK control signal. A logic "0" on BD12 will cause odd parity to be generated and inputted to the output data stream. Conversely, a logic "1" on BD12 will result in the generation of even parity that will be inputted to the output data stream.

More versatility is provided in both the transmitter and receiver by the addition of an external TTL clock input allowing the bus interface circuit to operate at data rates from 0 to 1 megabits. The TTL external clock must be ten (10) times the data rate to insure no data ambiguity.

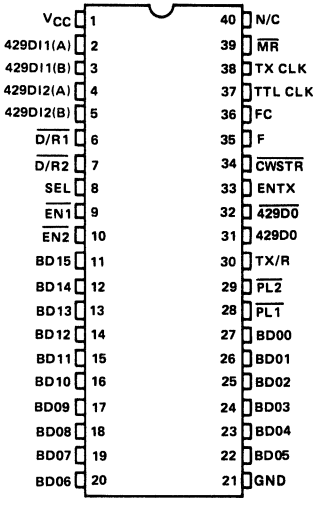
The ARINC bus interface circuit is fully guaranteed to support the data rates of ARINC specification 429 over both the voltage (± 10%) and full military temperature range. It interfaces with TTL, CMOS or NMOS support circuitry, and uses the standard 5-volt V_{CC} supply.

Features

- ARINC SPECIFICATION 429 COMPATIBLE
- DATA RATES OF 100 KILOBITS OR 12.5 KILOBITS
- SEPARATE RECEIVER AND TRANSMITTER SECTION
- DUAL AND INDEPENDENT RECEIVERS, CONNECTING DIRECTLY TO ARINC BUS
- SERIAL TO PARALLEL RECEIVER DATA CONVERSION
- PARALLEL TO SERIAL TRANSMITTER DATA CONVERSION
- WORD LENGTHS OF 25 OR 32 BITS
- PARITY STATUS OF RECEIVED DATA
- GENERATE PARITY OF TRANSMITTER DATA
- AUTOMATIC WORD GAP TIMER
- SINGLE 5-VOLT SUPPLY
- LOW POWER DISSIPATION
- FULL MILITARY TEMPERATURE RANGE

Pinout

TOP VIEW



9

CICD

HARRIS

Preliminary

HS-3819

Video Character Generator

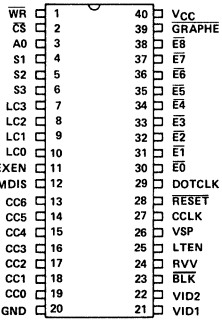
Features

- OPERATION (DOT CLOCK) FROM 1.0 TO 27 MHz
- DESIGNED TO INTERFACE WITH INTEL 8275 PROGRAMMABLE CRT CONTROLLER
- DIRECTLY DECODES (FROM ON-CHIP ROM);
  - ASCII 96 CHARACTER SET
  - 32 PSEUDO-GRAPHIC CHARACTERS
  - 10 OVERLAY PATTERNS
- EXPANDABLE CHARACTER TABLE
- 9 X 12 DOT MATRIX WITH DESCENDER CAPABILITY
- HANDLES VIDEO MODIFIERS;
  - BLANK
  - VIDEO SUPPRESS
  - REVERSE VIDEO
  - LIGHT ENABLE

Description

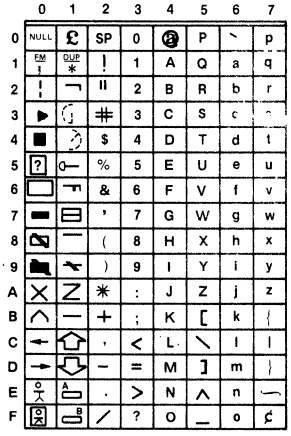
The HS-3819 is a CMOS/LSI Video Character Generator designed to help interface an Intel 8275 Programmable CRT Controller to a video monitor. The character generator must be supplied with a clock frequency of between 1 and 27 MHz which will be used as the dot clock. This signal is then divided by nine to form the character clock output needed by the CRT Controller. The HS-3819 then converts character data into a video output signal, through use of an internal (ROM) character table. Stored in this ROM are the standard 96 ASCII characters, 32 pseudo-graphic characters and 10 overlay patterns used to modify characters. Additional characters, if needed, can easily be decoded from an external memory field.

Pinout

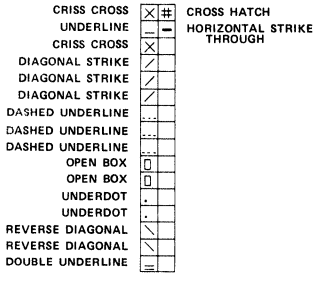


LC0-3 – LINE COUNT
CC0-6 – CHARACTER CODE
ROMDIS – ROM DISABLE
LTEN – LIGHT ENABLE
RVV – REVERSE VIDEO
VSP – VIDEO SUPPRESS
BLK – BLANK
S1-3 – SPECIAL FUNCTION
EXEN – EXPANSION ENABLE
E0-8 – EXPANSION INPUTS
GRAPHE – GRAPHICS ENABLE
WR – WRITE
CS – CHIP SELECT
A0 – ADDRESS 0
VID1-2 – VIDEO OUTPUTS
RESET – RESET
DOTCLK – DOT CLOCK
CCLK – CHARACTER CLOCK

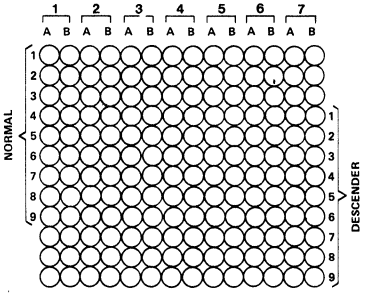
Standard Character Set



Overlay Patterns



Dot Matrix



NOTES:
1. EACH ROW MAY HAVE DOTS IN SET A OR SET B ONLY.
2. EACH CHARACTER MAY HAVE DOTS IN NORMAL SET OR DESCENDER SET ONLY.

PRODUCT ASSURANCE

For the custom, semicustom and rad hard products offered by CICD, any necessary screening or special product assurance testing is available. Class S and Class B military screening is routinely performed. Fabrication lot integrity is maintained, and product traceability to individual wafers is available.

CICD is a supplier to the most demanding high-reliability applications - specifically, for strategic missiles, satellites and heart pacers. If needed, customers may obtain a fully custom designed quality/reliability program to fit their unique requirements.

Custom Integrated Circuits Division

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Suite 800
Washington, DC 20037
202-342-3900
Telecopier: 202-338-3878

5 Old Concord Road
Burlington, MA 01803
617-273-1020
TWX: 710-332-1074
Quip: 617-272-7956

106 Seventh Street
Garden City, NY 11530
516-747-6776
TWX: 510-220-1527

Southeast Region

Suite 113
7040 Lake Ellenor Drive
Orlando, FL 32809
305-851-9450
Telex: 808819
Telecopier: 305-851-5141

Central Region

Suite 704
2850 Metro Drive
Minneapolis, MN 55420
612-854-3224
TWX: 920-576-3418
Telecopier: 612-854-7359

Suite 110
17120 Dallas Parkway
Dallas, TX 75248
214-248-3239
TWX: 910-860-5446

Western Region

Suite 320
1503 South Coast Drive
Costa Mesa, CA 92626
714-957-6557
TWX: 910-595-1533
Telecopier: 714-957-6557

European Sales Office

Harris Semiconductor
P. O. Box 27
145 Farnham Road
Slough SL1 4XD, England
011-447-5334666
Telex: 848174 Harris G

Note: Custom Integrated Circuits Division maintains its own sales force.

CMOS

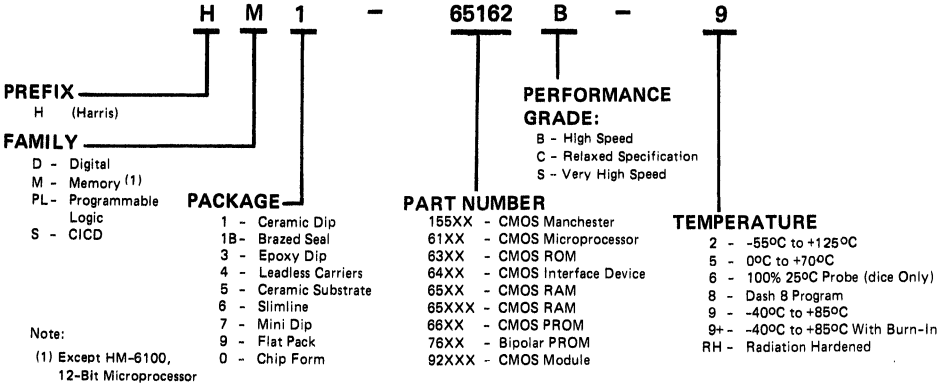
Ordering and Packaging 10

Ordering Information	10-3
Package Availability	10-4
Package Dimensions	10-6

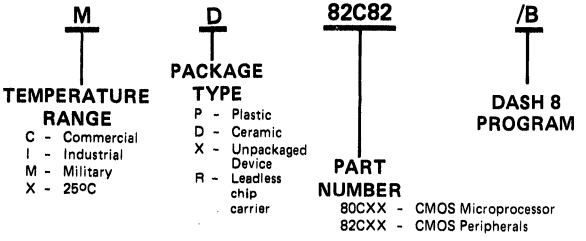
Ordering Information

Harris products are designed by "Product Code". When ordering, please refer to products by the full code.

PRODUCT CODE



80CXX FAMILY PRODUCT CODE



HARRIS DASH 8 PROGRAM

As a service to users of High Rel products, Harris makes readily available via the high reliability DASH 8 program many products from our product lines.

SPECIAL ORDERS

For best availability and price, it is urged that standard "Product Code" devices be specified which are available worldwide from authorized distributors. Where enhanced reliability is needed, note standard "Dash 8" screening described in this Data Book. Harris application engineers may be consulted for advice about suitability of a part for a given application.

If additional electrical parameter guarantees or reliability screening are absolutely required, a Request for Quotation and Source Control Drawing should be submitted through the local Harris Sales Office or Sales Representative. Many electrical parameters cannot be economically tested, but can be assured through design analysis, characterization, or correlation with other parameters which have been tested to specification limits. These parameters are labeled "Sampled and guaranteed, but not 100% tested".

Harris reserves the right to decline to quote, or to request modification to special screening requirements.

Package Availability

PART NUMBER	CERDIP	EPOXY* (Ag)	LEADLESS CARRIER	MODULE SUBSTRATE
CMOS 80C86 Family				
80C86	DE	FF	EA	–
82C82	5Z	7M	LS	–
82C55A	4H	FD	EG	–
82C84A	4N	7W	LS	–
82C88	5Z	7M	LS	–
82C59A	1M	FJ	LX	–
82C54	5F	FG	EH	–
82C52 **	1M	–	–	–
HD-6406	4H	FD	EA	–
80C88	DE	FF	EA	–
82C84B	4N	7W	LS	–
1K RAM				
HM-6508	5C	7I	–	–
HM-6518	5E	7D	LA	–
HM-6551	4M	3E	–	–
HM-6561	4N	7D	LA	–
4K RAM				
HM-6504	5E	7D	LB	–
HM-6514	5E	7D	LB	–
CMOS Memory 16 RAM				
HM-6516	5F	7Z	EC	–
HM-65162	5F	7Z	EC	–
HM-65172	5F	7Z	EC	–
RAM Modules				
HM-6564	–	–	–	MA
HM-92560	–	–	–	MD
HM-92570	–	–	–	MF

* Epoxy (Ag) is the type of leadframe that is recommended. The Epoxy (Au) is an emergency back-up when the silver type (Ag) is not available.

** This part can only be built in Cerdip at this time. Other packages will be built after the 82C52R is redesigned.

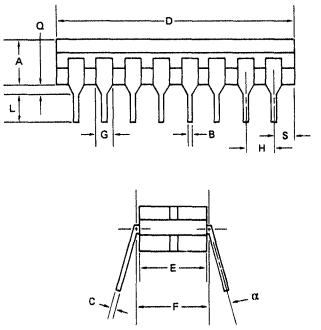
Package Availability (continued)

PART NUMBER	CERDIP	EPOXY* (Ag)	LEADLESS CARRIER	MODULE SUBSTRATE
Future Products				
HM-65262	5M	7F	–	–
HM-65642	DD	–	ED	–
HM-92562	–	–	–	MH
Programmable Memories				
HM-6641	DC, 5F	–	LZ	–
HM-6616	DC, 5F	–	EC	–
HM-6664	DD	–	ED	–
μProcessors & Peripherals Microprocessors				
HD-6120	5H	FE	–	–
HD-6121	5H	FD	–	–
HM-6100	5H	FE	–	–
HM-6101	5H	FE	–	–
Peripherals				
HD-6431	4Z	7H	LA	–
HD-6432	4N	7D	LA	–
HD-6433	4Z	7H	LA	–
HD-6434	4K	GB	–	–
HD-6436	5Z	7J	–	–
HD-6440	4N	7W	LA	–
HD-6495	4Z	7H	LA	–
Data Communications				
HD-15530	4K	7C	LX	–
HD-15531/15531B	5H	FE	–	–
HD-6408	4K	7C	LX	–
HD-6409	5Z	7M	LS	–
HD-6406	4H	FE	EA	–
HD-6402	5H	FD	–	–
HD-4702	4Z	7H	LA	–

* Epoxy (Ag) is the type of leadframe that is recommended. The Epoxy (Au) is an emergency back-up when the silver type (Ag) is not available.

Package Dimensions

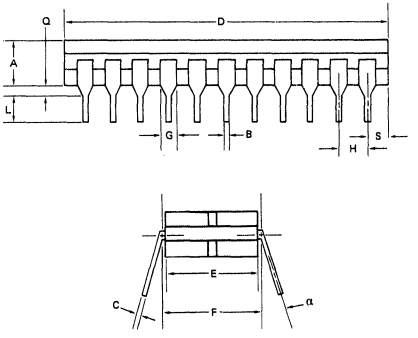
4Z, 4N, 5E, 5Z, 5M, 4L, DC, 5C
CERDIP .300



PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S	DIM. α
4Z	16 MSI	.140/.170	.016/.018	.008/.012	.760/.790	.265/.285	.290/.310	.050/.070	.090/.110	.125/.150	.020/.040	.025/.045	0°/15°
5C	16 LSI	.140/.170	.016/.018	.008/.012	.790/.760	.285/.305	.300/.320	.050/.070	.090/.110	.125/.150	.020/.040	.025/.045	0°/15°
4N 5E	18 LSI	.140/.170	.016/.018	.008/.012	.885/.915	.285/.305	.300/.320	.050/.070	.090/.110	.125/.150	.020/.040	.040/.060	0°/15°
5Z, 5M, 4L	20 LSI	.140/.170	.016/.018	.008/.012	.940/.970	.285/.305	.300/.320	.050/.070	.090/.110	.125/.150	.020/.040	.020/.040	0°/15°
DC	24 SLIM	.150/.180	.016/.018	.008/.012	1.240/1.270	.285/.305	.300/.320	.050/.070	.090/.110	.125/.150	.020/.040	.060/.090	0°/15°

NOTE: 1) Dimensions are: MIN./MAX.
2) All Dimensions in inches

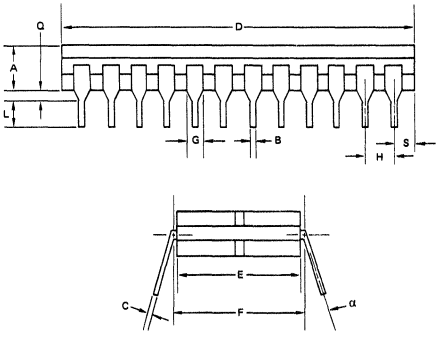
4M
CERDIP .400



PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S	DIM. α
4M	22	.150/.180	.016/.018	.008/.012	1.055/1.085	.375/.395	.395/.415	.050/.070	.090/.110	.125/.150	.020/.040	.030/.050	0°/15°

NOTE: 1) Dimensions are: MIN./MAX.
2) All Dimensions in inches

5F, 4K, 1M, DD, 4H, 5H, DE
CERDIP .600



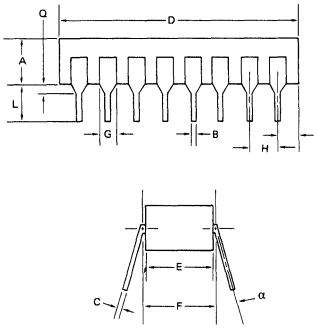
PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S	DIM. α
5F 4K	24 MSI	.150/.180	.016/.018	.008/.012	1.24/1.27	.515/.535	.595/.615	.050/.070	.090/.110	.125/.150	.020/.045	.060/.090	0°/15°
1M DD	28 MSI	.160/.190	.016/.018	.008/.012	1.44/1.47	.515/.535	.595/.615	.050/.070	.090/.110	.125/.150	.020/.060	.060/.090	0°/15°
4H, 5H, DE	40 MSI	.160/.200	.016/.018	.008/.012	2.035/2.075	.515/.535	.595/.615	.050/.070	.090/.110	.125/.150	.020/.060	.065/.095	0°/15°

NOTE: 1) Dimensions are: MIN./MAX.
2) All Dimensions in inches

Package Dimensions

7I, 3L, 7W, 7V, 7D, 7M, 7F, 7H, 7J

EPOXY .300

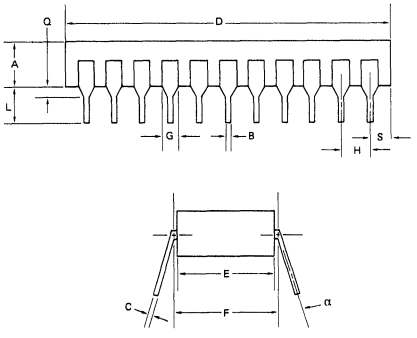


PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S	DIM. α
7I 7H	16	.125/.140	.016/.020	.008/.012	.750/.770	.245/.265	.290/.310	.050/.070	.090/.110	.150/.170	.020/.040	.025/.035	0°/15°
7W, 7V, 7D	18	.125/.140	.016/.020	.008/.012	.900/.920	.245/.265	.290/.310	.050/.070	.090/.110	.150/.170	.020/.040	.040/.060	0°/15°
7M, 7F, 7J	20	.130/.145	.016/.020	.008/.012	1.030/1.050	.250/.270	.290/.310	.050/.070	.090/.110	.150/.170	.020/.040	.060/.080	0°/15°

NOTE: 1) Dimensions are: MIN./MAX.
2) All Dimensions in inches

3E

EPOXY .400

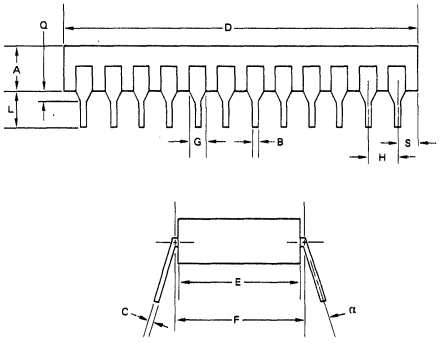


PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S	DIM. α
3E	22	.140/.170	.016/.018	.008/.012	1.10/1.12	.335/.355	.390/.410	.050/.070	.090/.110	.150/.170	.020/.040	.025/.045	0°/15°

NOTE: 1) Dimensions are: MIN./MAX.
2) All Dimensions in inches

FG, 7Z, FJ, FD, FF, 7C, FE

EPOXY .600

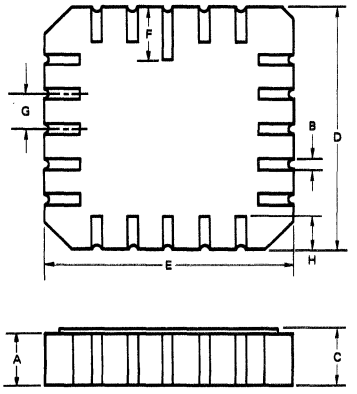


PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S	DIM. α
7C, FG, 7Z, GB	24	.145/.155	.016/.020	.008/.012	1.24/1.26	.540/.560	.590/.610	.050/.070	.090/.110	.150/.170	.020/.040	.065/.085	0°/15°
FJ	28	.145/.155	.016/.020	.008/.012	1.54/1.57	.540/.560	.590/.610	.050/.070	.090/.110	.150/.170	.020/.040	.110/.130	0°/15°
FE, FD, FF	40	.145/.155	.016/.020	.008/.012	2.05/2.07	.540/.560	.590/.610	.050/.070	.090/.110	.150/.170	.020/.040	.070/.090	0°/15°

NOTE: 1) Dimensions are: MIN./MAX.
2) All Dimensions in inches

Package Dimensions

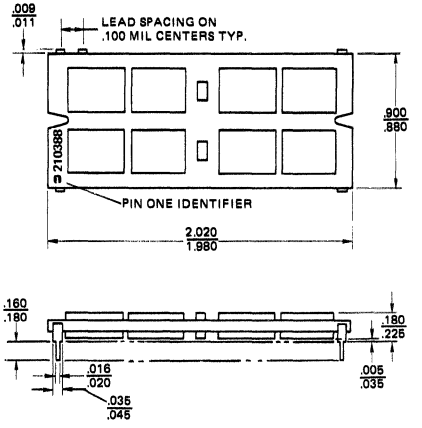
LB, LA, LS, LX, LZ, EC, ED, EA, EG, EH
LEADLESS CHIP CARRIER



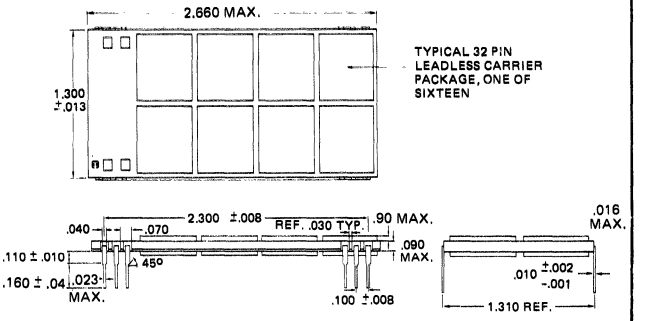
PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H
LB LA	18	.050 / .078	.020 / 0.30	.060 / .090	.342 / .358	.277 / .293	.060 / .095	.050 / BSC	.040 / .055
LS	20	.050 / .078	.020 / 0.30	.060 / .090	.342 / .358	.342 / .358	.060 / .095	.050 / BSC	.040 / .055
LX	28 ,400 sq.	.050 / .078	.020 / 0.30	.060 / .090	.390 / .415	.390 / .415	.060 / .095	.050 / BSC	.040 / .055
LZ	28 ,450 sq.	.050 / .078	.020 / 0.30	.060 / .090	.442 / .458	.442 / .458	.060 / .095	.050 / BSC	.040 / .055
EC, ED, EH	32	.050 / .078	.020 / 0.30	.060 / .090	.545 / .560	.442 / .458	.060 / .095	.050 / BSC	.040 / .055
EA EG	44	.050 / .078	.020 / 0.30	.060 / .090	.643 / .662	.643 / .662	.060 / .095	.050 / BSC	.040 / .055

NOTE: 1) Dimensions are: MIN. / MAX.
2) All Dimensions in inches

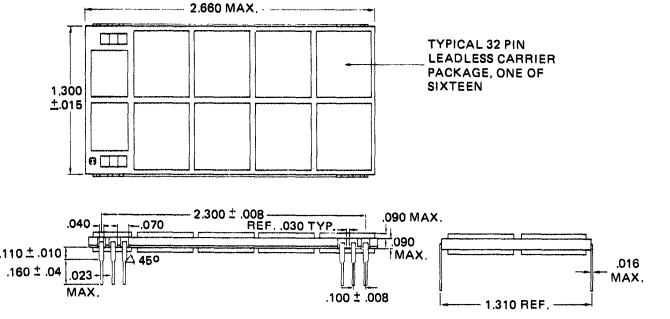
MA MODULE SUBSTRATE
64K CMOS RAM MODULE HM-6564



MD MODULE SUBSTRATE
HM-92560, HM-92562



MF MODULE SUBSTRATE
HM-92570



CMOS Dice Information 11

GENERAL INFORMATION

Harris CMOS Products are available in chip form to the hybrid micro circuit designer. The standard chips are DC electrically tested at +125°C to the data sheet limits for the commercial device and are 100% visually inspected. Packaging for shipment consists of waffle pack carriers plus an anti-static cushioning strip for extra protection.

The hybrid industry has rapidly become more diversified and stringent in its requirements for integrated circuits. To meet these demands Harris has several options additional to standard chip processing available upon request at extra cost. For more information consult the nearest Harris Sales Office.

CHIP ORDERING INFORMATION

Standard and special chip sales are direct factory order only. The minimum order on all sales is $250.00 per line item. Contact the local Harris Sales Office for pricing and delivery on special chip requirements.

MECHANICAL INFORMATION

Dimensions: All chip dimensions nominal with a tolerance of ±.003". Maximum chip thickness is .023".

Bonding Pads: Minimum bonding pad size is .004" x .004" unless otherwise specified.

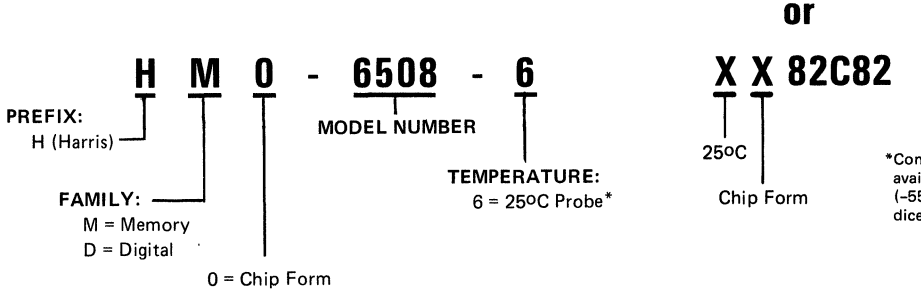
ELECTRICAL INFORMATION

CMOS: Die substrate must be electrically connected to VCC through conductive die attach, to assure proper electrical operating characteristics.

DICE GEOMETRIES AND DIMENSIONS

May be obtained by contacting the factory of your local Harris Sales Office.

PRODUCT CODE EXAMPLE



CMOS Appendices 12

Sector Alpha-Numeric Product Index	**12-3**
Harris Sales Locations	**12-8**
Action Request Cards	**—**

Alpha-Numeric Product Index

Analog

PRODUCT	DESCRIPTION
HA-1608	+10V Adjustable Voltage Reference
HA-2400/04/05	PRAM, Four Channel Operational Amplifiers
HA-2420/25	Fast Sample and Hold Operational Amplifiers
HA-2420/02/05	Precision High Slew Rate Operational Amplifiers
HA-2500/02/05	Precision High Slew Rate Operational Amplifiers
HA-2510/12/15	High Slew Rate Operational Amplifiers
HA-2520/22/25	Uncompensated High Slew Rate Operational Amplifiers
HA-2539	Super High Slew Rate Wideband Operational Amplifiers
HA-2540	Ultra High Slew Rate Operational Amplifiers
HA-2600/02/05	Wideband, High Impedance Operational Amplifiers
HA-2620/22/25	Very Wideband, Uncompensated Operational Amplifiers
HA-2630/35	High Performance Current Booster
HA-2640/45	High Voltage Operational Amplifiers
HA-2650/55	Dual High Performance Operational Amplifiers
HA-2720/25	Wide Range Programmable Operational Amplifiers
HA-2730/35	Wide Range Dual Programmable Operational Amplifiers
HA-2740	Quad Programmable Operational Amplifiers
HA-4156	High Performance Quad Operational Amplifiers
HA-4600/02/05	High Performance Quad Operational Amplifiers
HA-4620/22/25	Wideband, High Performance Quad Operational Amplifiers
HA-4741	Quad Operational Amplifier
HA-4900/0205	Precision Quad Comparators
HA-5033	High-Speed Current Buffer
HA-5062	Dual Low Power, JFET Input Operational Amplifier
HA-5064	Low Power, JFET Input Quad Operational Amplifier
HA-5082	Dul JFET Input Operational Amplifer
HA-5084	JFET Input Quad Operational Amplifier
HA-5100/05	Wideband, JFET Input Operational Amplifiers
HA-5110/15	Wideband, JFET Input, Uncompensated Operational Amplifiers
HA-5130/35	Precision Operational Amplifiers
HA-5141/42/44	Power Operational Amplifier, Single, Dual & Quad
HA-5160/62	Wideband, JFET Input, High Slew Rate, Uncompensated Operational Amplifiers
HA-5170	Precision JFET Input Operational Amplifiers
HA-5180/5180A	Ultra Low I_{BIAS} JFET Input Precision Operational Amplifier
HA-5190/95	Wideband, Fast Settling Operational Amplifiers
HA-5320	High Speed Precision Monolithic Sample and Hold Amplifier
HC-5116A/5156A	Monolithic CODECS (Preliminary)
HC-5502	SLIC-LC Subscriber Line Interface Circuit (PBX)
HC-5504	SLIC-LC Subscriber Line Interface Circuit (PBX)
HC-5510/5511	Monolithic CODECs (Preliminary)
HC-5512/5512A	PCM Monolithic Filter
HC-5531	Automatic Line Balance Network
HC-55536	Decode Digital Continuously Variable Slope Delta Modulator (CVSD)
HC-55564	Encode and Decode all Digtal Continuously Variable Slope Delta Modulator (CVSD)

Analog (Continued)

PRODUCT	DESCRIPTION
HD-0165	Keyboard Encoder
HI-200	Dual SPST CMOS Analog Switch
HI-201	Quad SPST CMOS Analog Switch
HI-201HS	High Speed Quad SPST CMOS Analog Switch
HI-300	Dual SPST CMOS Analog Switch
HI-301	SPDT CMOS Analog Switch
HI-302	Dual DPST CMOS Analog Switch
HI-303	Dual SPDT CMOS Analog Switch
HI-304	Dual SPST CMOS Analog Switch
HI-305	SPDT CMOS Analog Switch
HI-306	Dual DPST CMOS Analog Switch
HI-307	Dual SPDT CMOS Analog Switch
HI-381	Dual SPST CMOS Analog Switch
HI-384	Dual DPST CMOS Analog Switch
HI-387	SPDT CMOS Analog Switch
HI-390	Dual SPDT CMOS Analog Switch
HI-506/507	Single 16/Differential 8 Channel CMOS Analog Multiplexers
HI-506A/507A	16 Channel CMOS Analog Multiplexers with Overvoltage Protection
HI-506L/507L	Latched, 16/8 Channel Analog Multiplexer
HI-508/509	Single 8/Differential 4 Channel CMOS Analog Multiplexers
HI-508A/509A	8 Channel CMOS Analog Multiplexers with Overvoltage Protection
HI-508L/509L	Latched, 8/4 Channel Analog Multiplexer
HI-516	16 Channel/Differential 8 Channel CMOS High Speed Analog Multiplexer
HI-518	8 Channel/Differential 4 Channel CMOS High Speed Analog Multiplexer
HI-524	4 Channel Video Multiplexer
HI-539	Monolithic, Four Channel, Low Level, Differential Multiplexer
HI-562A	12 Bit High Speed Monolithic Digital-to-Analog Converter
HI-565A	High Speed Monolithic Digital-to-Analog Converter with Reference
HI-574A	Fast, Complete 12 Bit A-to-D Converter with P Interface
HI-674A	High Speed, Complete 12-Bit A-to-D Converter with P Interface
HI-1818A/1828A	Low Resistance 8 Channel CMOS Analog Multiplexer
HI-5040	Low Resistance SPST Switch
HI-5041	Low Resistance Dual SPST Switch
HI-5042	Low Resistance SPDT Switch
HI-5043	Low Resistance Dual SPDT Switch
HI-5044	Low Resistance DPST Switch
HI-5045	Low Resistance Dual DPST Switch
HI-5046	Low Resistance DPDT Switch
HI-5046A	Low Resistance DPDT Switch
HI-5047	Low Resistance 4PST Switch
HI-5047A	Low Resistance 4PST Switch
HI-5048	Low Resistance Dual SPST Switch
HI-5049	Low Resistance Dual DPST Switch
HI-5050	Low Resistance SPDT Switch
HI-5051	Low Resistance Dual SPDT Switch
HI-5610	10 Bit High Speed Monolithic Digital-to-Analog Converter

Analog (Continued)

PRODUCT	DESCRIPTION
HI-5618A/18B	8 Bit High Speed Digital-to-Analog Converters
HI-5660	High Speed Monolithic D-to-A Converter
HI-5680	12 Bit Low Cost Monolithic D-to-A Converter
HI-5685	High Performance Monolithic 12 Bit D-to-A Converter
HI-5687	Wide Temperature Range Monolithic 12 Bit D-to-A Converter
HI-5712/12A	High Performance 12 Bit Analog-to-Digital Converters
HI-5900	Analog Data Acquisition Signal Processor
HI-5901	Analog Data Acquisition Signal Processor
HI-7541	12 Bit Multiplying Monolithic Digital-to-Analog Converter
HI-DAC801	12 Bit High Speed Monolithic Digital-to-Analog Converter
HI-DAC16B/C	16 Bit D-to-A Converter
HV-1000/1000A	Single-Phase Induction Motor Energy Saver
LF347	Wideband Quad JFET Input Operational Amplifiers
LF353	Wideband Dual JFET Input Operational Amplifier
LF355 Series	Monolithic JFET Input Operational Amplifiers
LF356 Series	Wideband Monolithic JFET Input OPerational Amplifiers
LF357 Series	Decompensated Wideband Monolithic JFET Input Operational Amplifiers
LM108/308	Operational Amplifiers
LM108A/308A	Operational Amplifiers
LM118/318	Operational Amplifiers
LM143/343	High Voltage Operational Amplifiers
LM143A/343A	High Voltage Operational Amplifiers
LM146/346	Programmable Quad Operational Amplifiers
LM148/348	Quad 741 Operational Amplifiers
LM148A/348A	Quad 741 Operational Amplifiers
LM1558A/1458A	Dual Operational Amplfiers
LM2908	Quad Operational Amplifiers
LM4250/4250C	Programmable Operational Amplifiers

Bipolar

PRODUCT	DESCRIPTION
HD-6600	Quad Power Strobe
HM-0104	10 X 4 Diode Matrix
HM-0168	6 X 8 Diode Matrix
HM-0186	8 X 6 Diode Matrix
HM-0198	9 X 8 Diode Matrix
HM-0410	4 X 10 Diode Matix
HM-7602/03	32 X 8 Bit Generic PROM
HPROM-0512	64 X 8 HPROM
HM-7610/11	256 X 4 Bit Generic PROM
HM-7610A/11A	256 X 4 Bit High Speed Generic PROM
HM-7610B/11B	256 X 4 Bit Ultra High Speed Generic PROM
HM-7620/21	512 X 4 Bit Generic PROM
HM-7620A/21A	512 X 4 Bit High Speed Generic PROM
HM-7620B/21B	512 X 4 Bit Ultra High Speed Generic PROM
HM-7640/41	512 X 8 Bit Generic PROM (24-Pin)
HM-7640A/41A	512 X 8 Bit High Speed Generic PROM (24-Pin)
HM-7649	512 X 8 Bit Generic PROM (20-Pin)
HM-7649A	512 X 8 Bit High Speed Generic PROM (20-Pin)
HM-7642/43	1024 X 4 Bit Generic PROM
HM-7642A/43A	1024 X 4 Bit High Speed Generic PROM
HM-7642B/43B	1024 X 4 Bit Ultra High Speed Generic PROM
HM-7681	1024 X 8 Bit Generic PROM
HM-7681A	1024 X 8 Bit High Speed Generic PROM
HM-7685	2048 X 4 Bit Generic PROM
HM-7685A	2048 X 4 Bit High Speed Generic PROM
HM-76161	2048 X 8 Bit Generic PROM
HM-76161A	2048 X 8 Bit High Speed Generic PROM
HM-76165	4096 X 4 Bit Generic PROM
HM-76321	4096 X 8 Bit Generic PROM
HM-76641	8192 X 8 Bit Generic PROM
HPL-77153	20-Pin Field Programmable Logic Array
HPL-77209	20-Pin Field Programmable Array Logic (Active Low Outputs)
HPL-77215	20-Pin Field Programmable Array Logic (Active Low Outputs)
HPL-77216	20-Pin Field Programmable Array Logic (Programmable Output Polarity)
HPL-77317	20-Pin Field Programmable Array Logic (Active Low Dedicated Outputs)
HPL-77318	20-Pin Field Programmable Array Logic (Active High Dedicated Outputs)
HPL-77319	20-Pin Field Programmable Array Logic (Enhanced HPL-77317)
HPL-77320	20-Pin Field Programmable Array Logic (Enhanced HPL-77318)
M38510/20701BEB	32 X 8 Open Collector QPL1 PROM
M38510/20702BEB	32 X 8 Three State QPL1 PROM
M38510/20101BJB	64 X 8 Open Collector QPL1 PROM
M38510/20301BEB	256 X 4 Open Collector QPL1 PROM
M38510/20302BEB	256 X 4 Three State QPL1 PROM
M38510/20401BEB	512 X 4 Open Collector QPL1 PROM
M38510/20402BEB	512 X 4 Three State QPL1 PROM
M38510/20801BJB	512 X8 Open Collector QPL1 PROM
M38510/20802BJB	512 X 8 Three State QPL1 PROM
M38510/20602BVB	512 X 8 Three State QPL1 PROM
M38510/20904BJB	1024 X 8 Three State QPL1 PROM
M38510/20902BVB	2048 X 4 Three State QPL1 PROM
M38510/21002BJB	2048 X 8 Three State QPL1 PROM

CMOS

PRODUCT	DESCRIPTION
HD-15530	Manchester Encoder-Decoder
HD-15531	Manchester Encoder-Decoder
HD-4702	Programmable Bit Rate Generator
HD-6101	Parallel Interface Element
HD-6120	12 Bit High Performance Microprocessor
HD-6121	I/O Controller
HD-6402	LSI Universal Asynchronous Receiver Transmitter
HD-6406	Programmable Asynchronous Communication Interface
HD-6408	Asynchronous Manchester Adapter
HD-6409	Manchester Encoder-Decoder
HD-6431	Hex Latching Bus Driver
HD-6432	Hex Bi-directional Bus Driver
HD-6433	Quad Bus Separator/Driver
HD-6434	Octal Resettable Latch
HD-6436	Octal Bus Buffer/Driver
HD-6440	Latch Decoder/Driver
HD-6495	Hex Bus Driver
HM-6100	12 Bit Static Microprocessor
HM-6504	4K X 1 Synchronous RAM
HM-6508	1K X 1 Synchronous RAM
HM-6514	1K X 4 Synchronous RAM
HM-6516	2K X 8 Synchronous RAM
HM-65162	2K X 8 Asynchronous RAM
HM-65172	2K X 8 Asynchronous RAM
HM-6518	1K X 1 Synchronous RAM
HM-65262	16K X 1 Asynchronous RAM
HM-6551	256 X 4 Synchronous RAM
HM-6561	256 X 4 Synchronous RAM
HM-6564	64K Synchronous RAM Module
HM-6616	2K X 8 Fuse Link PROM
HM-6641	512 X 8 PROM
HM-6664	8K X 8 Fuse Link PROM
HM-92560	256K Synchronous RAM Module
HM-92570	256K Synchronous RAM Module
HPL- 16LC8	Programmable Logic
HPL-16RC4	Programmable Logic
HPL-16RC6	Programmable Logic
HPL-16RC8	Programmable Logic
80C86	16 Bit Microprocessor
80C88	8 Bit Microprocessor
82C37A	High Performance Programmable DMA Controller
82C52	Full Duplex UART
82C54	Programmable Interval Timer
82C55A	Programmable Peripheral Interface
82C59A	Priority Interrupt Controller
82C82	Octal Latch
82C83	Octal Latching Inverting Bus Driver
82C84A	Clock Generator/Driver
82C84B	Clock Generator Driver
82C86	Octal Bus Transceiver
82C87	Octal Bus Transceiver
82C88	Bus Controller
82C89	Bus Arbiter

Harris Sales Locations

OEM Sales

EASTERN REGION

Suite 215
3890 West Commercial Blvd.
Ft. Lauderdale, FL 33309
(305) 739-0016

Suite 400
875 Johnson Ferry Road
Atlanta, GA 30342
(404) 256-4000

Suite 308
1 Burlington Woods Drive
Burlington, MA 01803
(617) 273-5942

P. O. Box 31747
Raleigh, NC 27622

Suite 1101
996 Old Eagle School Road
Wayne, PA 19087
(215) 687-6680

Suite 273
555 Broadhollow Road
Melville, L. I., NY 11747
(516) 249-4500

CENTRAL REGION

Suite 300
6400 Shafer Court
Rosemont, IL 60018
(312) 692-4960

Suite 101
1717 East 116th Street
Carmel, IN 46032
(317) 844-8011

Suite 703
2850 Metro Drive
Minneapolis, MN 55420
(612) 854-3558

Suite 110
17120 Dallas Parkway
Dallas, TX 75248
(214) 248-3237

WESTERN REGION

Suite 250
1717 E Morten Avenue
Phoenix, AZ 85020
(602) 870-0080

Suite 320
1503 South Coast Drive
Costa Mesa, CA 92626
(714) 540-2176

Suite B120
883 Stierlin Road
Mt. View, CA 94043
(415) 964-6443

Suite 205
6400 Canoga Avenue
Woodland Hills, CA 91367
(213) 992-0686

33919 9th Avenue South
Federal Way, WA 98003
(206) 838-4878

Suite 8
2005 Broadway
Vancouver, WA 98663
(206) 696-0043

International Sales

Europe

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Headquarters
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8057 Eching
West Germany
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TWX: 5-213-866

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Harris Semiconductor Div.
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Via Fratelli Cracchi 48
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8057 Eching
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Ditz Schweitzer A. S.
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DK-2600 Glostrup
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Yleiselektronikka OY
Atomitie 5 B (P.O. Box 33)
SF-00370 Helsinki 37
Tel.: 358-0-90-562-1122

FRANCE

Matra-Harris Semiconductor
Harris S. A
Harris Semi. Division
6 Av Charles de Gaulle
F-78150 Le Chesnay
Tel: 33-3-9548000
TWX: 696514

Matra Harris Semiconductor
B. P. 942
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Max-Planck-Str. 1-3
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54 Jabotinsky street
Ramat-Gan 52117
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722-367
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EMESA SpA
Via L-de Viadana 9
20122, Milano
Tel: 02-8690616860307
TWX 335066

Lasi Elettronica
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I-20092 Cinisello Balsamo
Tel.: 39-2-9273578
TWX: 337612

NETHERLANDS

Techmation Electronics BV
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N-Oslo 5
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TELEX 71265 nen

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Boksburg East Trasvaal
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TWX: 4-25559

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Torre de Madrid
Planta 12 Officina 9
Madrid
Tel: 34-242-5204
TWX 22596

SWEDEN

A. B. Betoma
Box 3005
S17103 Solna 3
Tel: 46-8-820280
TWX 19389

SWITZERLAND

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Ashford, Middlesex
TW15 1AV
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St. Martins Way Industrial Est.
Cambridge Road
Bedford MK 42 OLF
Tel: 44-8442/-3146
TWX: 837508

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Hartlepool, Cleveland
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TWX: 587650 Sempro

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Thame Park Ind. Estate
Thame, Oxon OX9 3RS
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TWX 837508

Phoenix Electronics Ltd.
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Vere Road
Kirkmuirhill, Lankersham
ML11 9 RP, Scotland
Tel.: 44-55589-2393
TWX: 777404

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Trim
County Meath
Eire, Ireland
Tel.: 353-46-36263
TWX: 90342

Far East

SALES OFFICES

Harris Semiconductor, Inc.
Far East Branch
Ace Shoto Bldg. 3F
1-4-7, Shoto
Shibuya-ku, Tokyo 150
Tel.: 81-3-485-1031
TWX: 326525

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Los Angeles, CA 90063
Tel.: 213-267-1145
TWX 69-1159

INDIA

Fegu Electronics
Attn: Raj Saraf
106 Mittal Chambers
Nariman Point
Bombay 400021

Fegu Incorporated
Electronics Division
2584 Wyandotte St.
Mountain View, CA 94043
Tel: 415-961-2380
TWX: 176-572

Zenith Electronics
Attn: Raj Saraf, Mgr. Director
106 Mittal Chambers
Nariman Point
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South America

Elko S. R. L.
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Argentina
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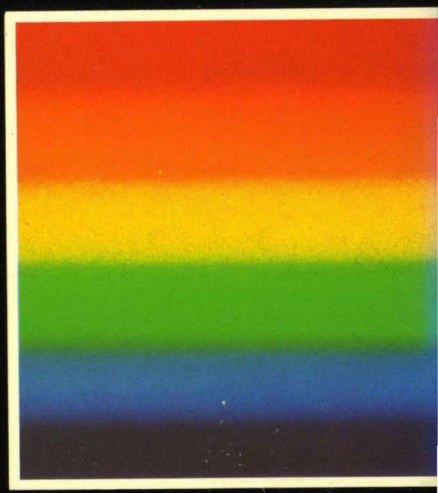

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