Electrically Alterable Non-Volatile Memory Handbook

GENERAL INSTRUMENT

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ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY HANDBOOK

DATA SHEETS

APPLICATION NOTES

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MARCH 1983

Revision A

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APPLICATION NOTES

DATA SHEETS

Electrically Alterable Non-Volatile Memory

Non-Volatile Static RAM

Note

EEPROMs and EAROMs are equivalent terms used to describe Electrically Alterable Non-Volatile Memories.

GENERAL INSTRUMENT

ER0082

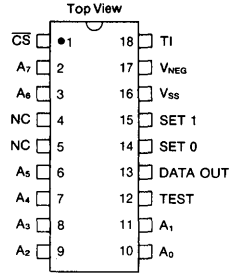
82 Bit Electrically Alterable Read Only Memory

FEATURES

- 82 x 1 Bit Organization
- Addressing by Two 4-bit BCD Digits
- +5V, −30V Power Supplies
- Set Inputs Have Debounce Circuits
- Bit Erasable
- 100 μsec Read Access Time
- Minimum Data Retention, 7 Years Unpowered, 2 Years Powered
- P-Channel Output Transistor, Open Drain, Pull-Down Resistor
- Control, Address and Data Inputs TTL or CMOS Compatible
- Ideally Suited for T.V. Receiver Channel Selection

PIN CONFIGURATION

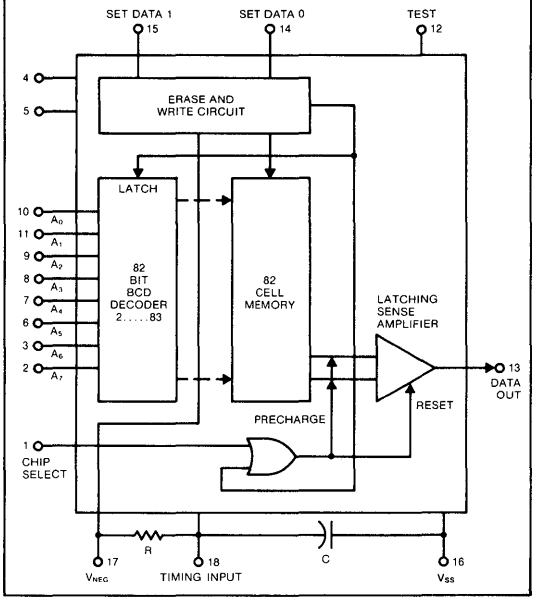
18 LEAD DUAL IN-LINE



DESCRIPTION

The ER0082 is a 82 x 1 bit electrically alterable read only memory. This device can be used as part of a television receiver tuner control system. The memory is programed by the user to maintain a record of channels the user wishes to be tuned, and is non-volatile in that the information stored within is not affected by the condition of or the sequencing of power supplied to the chip.

BLOCK DIAGRAM



OPERATION

Memory Address

The address is provided by two positive logic binary coded decimal (BCD) digits, LSD (A_0-A_3) and MSD (A_4-A_7) (least and most significant digits); i.e. 8 bits which supply the address of a bit in the memory. There is an address in memory associated with each of the BCD numbers 2 through 83. Addresses outside the range of 2 to 83 at the LSD and MSD inputs do not cause any modification of the stored bits or change in the output data.

Example: Address 83 = 10000011 (A_7...A_0)
Address 2 = 00000010 (A_7...A_0)

Address changes must occur only during $\overline{CS}$ high and must be stable at least 20μs before $\overline{CS}$ goes low.

Memory Read

The negative transition of $\overline{CS}$ (from a "1" level to a "0" level) initiates a memory read cycle, except when the transition occurs during a memory alteration cycle, in which case the transition is ignored. A read cycle will cause the DATA OUT pin to indicate the state of the memory bit read. The DATA OUT pin will retain the state until either $\overline{CS}$ goes to "1" or a memory alteration cycle is initiated. DATA OUT will show the contents of the address 100μs after $\overline{CS}$ starts falling. When $\overline{CS}$ is high the DATA OUT pin is low. The DATA OUT pin is internally pulled up to the positive supply, V_{SS} and for a "0" output the DATA OUT pin floats with an external pull-down (10KΩ) to ground.

Memory Alteration

A memory alteration cycle is initiated only when the SET DATA "0" or the SET DATA "1" input, but not both, has been continuously at "0" for the specified debounce time. This allows an input to be entered via a contact closure to ground using switches. These inputs are connected to V_{SS} via internal pull-ups. During the alteration cycle the address is held latched within the LSI. Changes in the address and SET DATA inputs are ignored, and the DATA OUT pin is held at "0". Only one memory bit may be erased or written during any single memory alteration cycle. The alteration cycle, once initiated, must go to completion. Upon completion of an alteration cycle or the fall of $\overline{CS}$ whichever occurs last, the memory bit corresponding to the current input address will be read and output on the DATA OUT terminal. A memory read of a bit altered due to SET DATA "0" input will cause the DATA OUT pin to be "0". Similarly, a read of a bit altered due to a SET DATA "1" input will cause the DATA OUT pin to be "1". The SET DATA inputs have internal circuits to provide delays for interfacing to mechanical switches or relays. Each successful debounce of a SET DATA input will initiate only one memory alteration cycle. Another alteration cycle will not occur until both

SET DATA inputs have remained continuously at a "1" level for the specified release time and only one of the SET DATA inputs has again been successfully debounced. After an alteration cycle is complete, a read cycle may not be initiated by CS until 3 cycles of the clock on the "Timing" input pin have occurred (about 12.5ms for a nominal 200Hz frequency).

Timing

This is an input provided for external components used for a timing reference. A resistor (680K) and a capacitor (.01μF) may be connected to this input to provide a 200Hz nominal clock frequency. A lower capacitor or resistor value will provide a higher frequency. The timer will run only during a read cycle, alteration cycles, or while timing a debounce or release. Increasing the clock frequency will shorten these times. The frequency can vary from 50Hz min to 500Hz max. and may be measured on the timing pin.

PIN FUNCTIONS

NAME	FUNCTIONS
A_0-A_7	Address bus used to select 1 of 82 addresses.
$\overline{CS}$	Chip select. An active low signal which enables or disables the data out pin.
Data Out	DATA OUT is a single bit indicating the state of the addressed memory cell.
Set Data 0 Set Data 1	These are inputs by which the user can modify the memory contents.
TI	Provides a timing reference for internal timing cycles.
TEST	A TEST pin which provides a connection to V_m, an internal voltage used for evaluating chip memory performance. In normal operation this pin should be left unconnected.
V_{SS}	Substrate Supply. Nominally +5V.
V_{NEG}	Power supply input. Nominally −30V.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All input and outputs (except V_{NEG}) with respect to V_{SS} . . −20V to +0.3V
V_{NEG} with respect to V_{SS} . . . . . −40V
Storage temperature (No Data Retention) . . . . . −65° C to +150° C
Storage temperature (with Data Retention)
Operating . . . . . 0° C to +70° C
Unpowered . . . . . −40° C to +85° C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

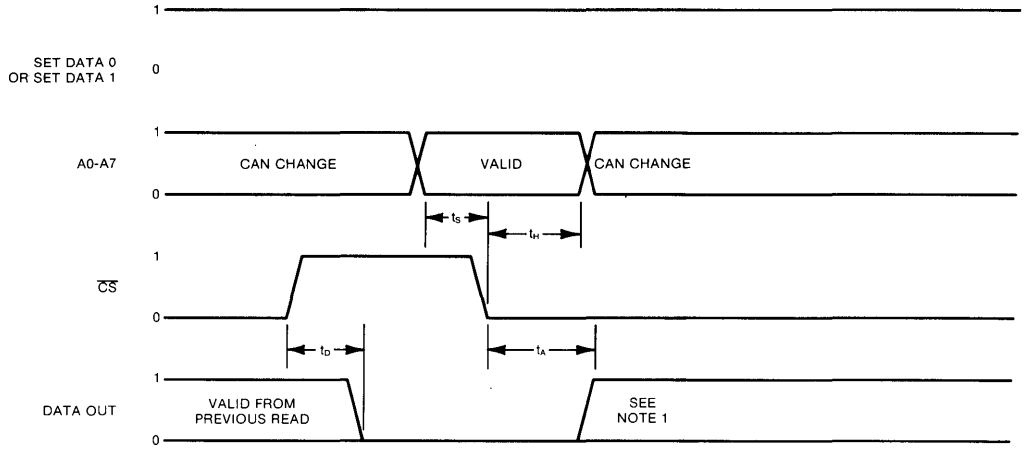
Standard Conditions (unless otherwise noted)

V_{SS} = +4.5V to +8.0V
$V_{SS} - V_{NEG}$ = −32V to −38V
Operating Temperature T_A = 0° C to 70° C

Characteristic	Sym	Min	Max	Units	Conditions
DC CHARACTERISTICS					
Input Logic "1"	V_{IH}	V_{SS} −2	V_{SS} +.3	V	
Input Logic "0"	V_{IL}	V_{SS} −10	V_{SS} −4.1	V	
Input Leakage	I_L	—	10	μA	
Output Logic "1"	V_{OH}	—	V_{SS} −.5	V	@ 0.5mA
Power Supply	I_{SS}	4	20	mA	
Power Dissipation	P_{SS}	130	700	mW	
AC CHARACTERISTICS					
Read Cycle Time	—	130	—	μs	
Read Access Time	t_A	—	100	μs	from fall of $\overline{CS}$
Memory Alteration Time	—	200	—	ms	
Time between Memory Alteration Cycles	t_C	12.5	—	ms	
Debounce Time for Changing Memory	t_B	12.5	37.5	ms	
Address Setup Time	t_S	20	—	μs	
Address Hold Time	t_H	100	—	μs	
Reset Time	t_D	2	30	μs	from rise of $\overline{CS}$
Input Rise & Fall Times	—	0.03	30	ms	on all inputs
EAROM CHARACTERISTICS					
Data Retention, Power Off (Storage)	—	7	—	Years	−40° C to +85° C
Data Retention, Power On	—	2	—	Years	0° C to +70° C
Read Cycles Per Cell	—	10^7	—	—	no loss of data
Erase/Write Cycles per Cell	—	10^3	—	Cycles	10 year retention
Erase/Write Cycles per Cell	—	10^4	—	Cycles	1 year retention

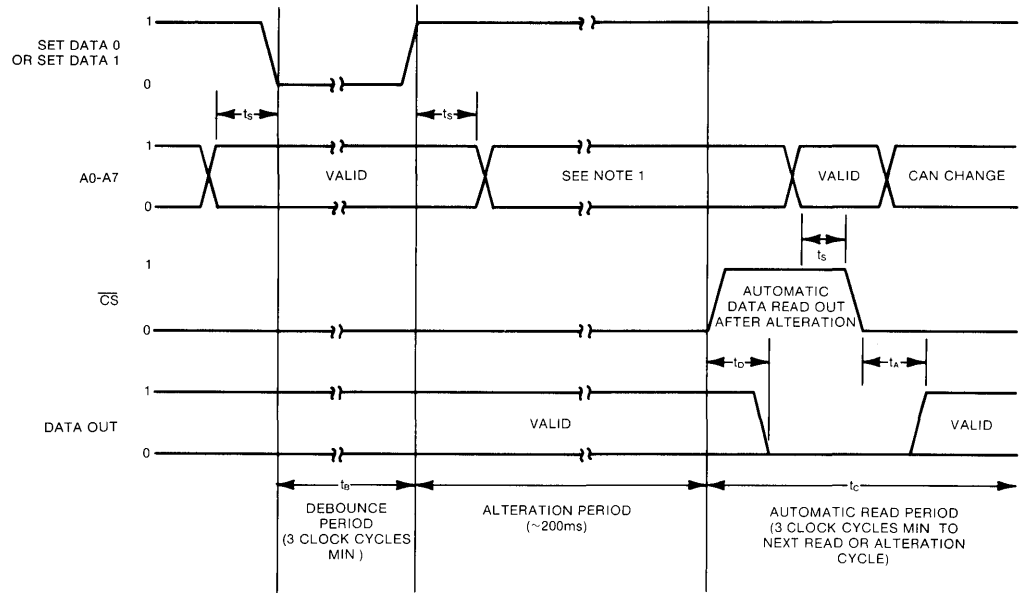
TIMING DIAGRAMS

READ OPERATION



NOTE 1: Data will be valid until the next positive $\overline{CS}$ transition or until initiation of an alteration cycle.

DATA ALTERATION



NOTE 1: Address may change here, but should not change if verification of correct alteration is required.

GENERAL INSTRUMENT

ER1451

700 Bit Serial Electrically Alterable Read Only Memory

FEATURES

- 50 Word x 14 Bit Organization
- Addressing by Two Consecutive One-of-Ten Codes
- Word Alterable
- 10 Year Data Storage
- TTL Compatible Signal Levels
- Write/Erase Time: 10ms

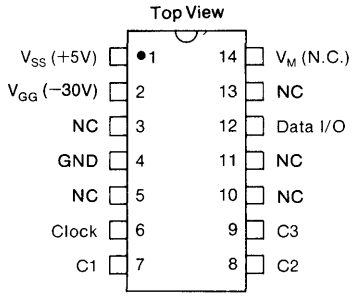
DESCRIPTION

The ER1451 is a serial input/output 700 bit electrically erasable and reprogramable ROM, organized as 50 words of 14 bits each. Data and address are communicated in serial form via a one-pin bidirectional bus. Its operation is similar to the ER1400 in all respects, except that it has only half the memory capacity. The address, in the form of two consecutive one-of-ten codes, is shifted in with the first ten bits indicating the MSD. Address 49 is the highest valid address. For this reason during the first five clock cycles of an ACCEPT ADDRESS function the data input is ignored.

Mode selection is by a 3 bit code applied to C1, C2 and C3.

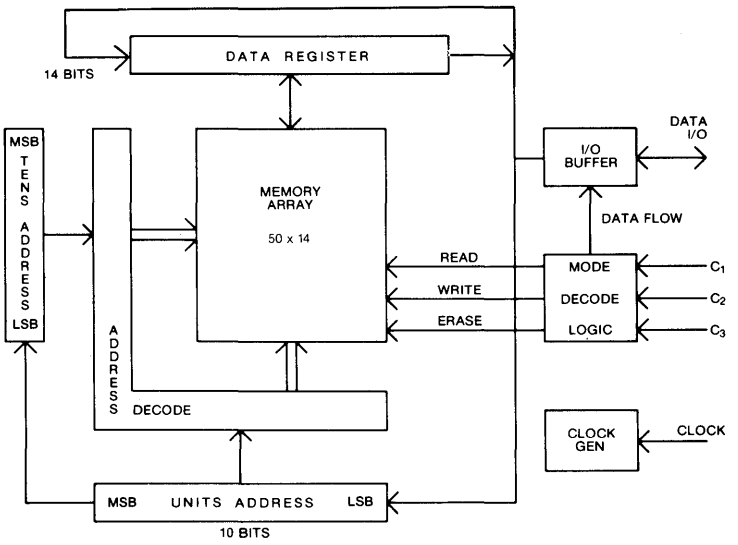
Before writing, a selected location must be preconditioned by an Erase operation. Data is then stored by internal negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 700 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

PIN CONFIGURATION
14 LEAD DUAL IN LINE



NC = No external connection for normal usage

BLOCK DIAGRAM



PIN FUNCTIONS

Name	Function
Data	In the Accept Address and Accept Data modes, this pin is an input pin for address and data respectively. When outputting data it has TTL drive capability, while in all other modes it is left floating.
V_M	Used for testing purposes only. Must be left unconnected for normal operation.
V_{SS}	Chip substrate. Normally connected to +5V
V_{GG}	DC supply. Normally connected to −30 Volt supply.
Clock	Timing reference. Required for all operations. May be left at logic one when device is in standby.
C1, C2, C3	Mode control pins. Their operation is as follows:

C1	C2	C3	Function
1	1	1	Standby—The output buffer is left floating. If the clock is maintained, the contents of the Address and Data Registers will remain unchanged.
1	0	0	Accept Address—Data presented at the I/O pin is shifted into the Address Register with each clock pulse. Addressing is by two consecutive one-of-ten codes.
0	1	1	Read—The address word is read from memory into the data register.
0	1	0	Shift Data Out—The output driver is enabled and the contents of the Data Register are shifted out one bit with each clock pulse.
1	0	1	Erase—The word stored at the addressed location is erased to all zeroes.
0	0	0	Accept Data—The data register accepts serial data presented at the I/O pin. The Address Register remains unchanged.
0	0	1	Write—The word contained in the Data Register is written into the location designated by the Address Register.
1	1	0	Not Used.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs (except V_{GG}) with respect to V_{SS} . . −20V to +0.3V
V_{GG} with respect to V_{SS} . . . . . −40V
Storage temperature (No Data Retention) . . . . . −65° C to +150° C
Storage temperature (with Data Retention)
Operating . . . . . −25° C to +75° C
Unpowered . . . . . −65° C to +80° C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted)

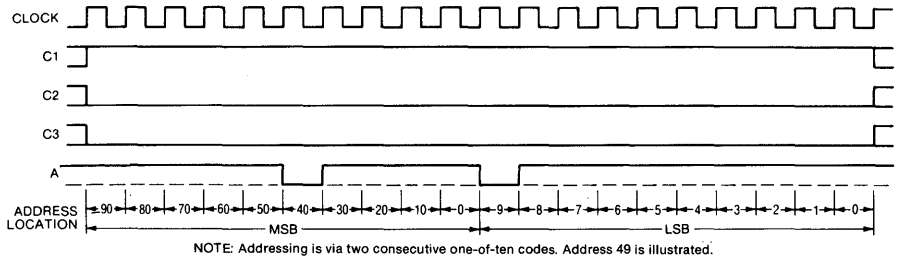
V_{SS} = +5 Volts ± 5% GND = 0 Volts
V_{GG} = −30 Volts ± 5%
Operating Temperature T_A = 0° C to +70° C

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Input Logic "0"	V_{IL}	V_{SS}−15	—	+0.8	Volts	
Input Logic "1"	V_{IH}	V_{SS}−1.5	—	V_{SS}+0.3	Volts	
Input Leakage	I_L	—	—	10	μA	V_{IN} = −10V
Output Logic "0"	V_{OL}	—	—	+0.4	Volts	I_{OL} = 3.2mA
Output Logic "1"	V_{OH}	V_{SS}−1.5	—	V_{SS}	Volts	I_{OH} = 3.2mA
Power Consumption	P_{GG}	—	—	300	mW	
Power Supply Current	I_{GG}	—	—	8	mA	
	I_{SS}	—	—	8	mA	
AC CHARACTERISTICS						
Clock Frequency	fϕ	10	14	17	KHz	
Clock Duty Cycle	Dϕ	35	50	65	%	
Write Time	tw	10	15	24	ms	
Erase Time	te	10	15	24	ms	
Rise, Fall Time	tr, tf	—	—	1	μs	
Control, Data Set Up Time	t_{CS}	1	—	—	μs	
Control, Data Hold Time	t_{CH}	0	—	—	μs	
Propagation Delay	t_{PW}	—	—	20	μs	Load: 2 TTL gates + 100pf
Non-Volatile Data Storage	T_S	10	—	—	Years	See Note 1.
Number of Erase/Write Cycles	N_W	—	—	10^4	—	Per word. See Note 2.
Number of Read Accesses Between Writes	N_{RA}	10^9	—	—	—	Per word

**Typical values are at +25° C and nominal voltages.

NOTES: 1. T_S is for powered or unpowered storage.
2. N_W (=10^4) is a maximum for data retention times greater than 10 years. Beyond 10^4 reprograming cycles, there is a gradual, logarithmic reduction in retention time with 1 year being a typical value after 10^5 cycles.

TIMING DIAGRAMS



NOTE: Addressing is via two consecutive one-of-ten codes. Address 49 is illustrated.

Fig.1 ACCEPT ADDRESS

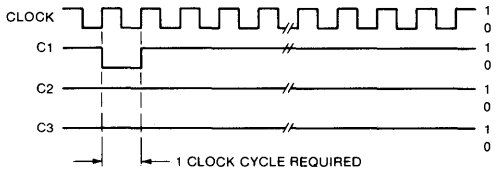
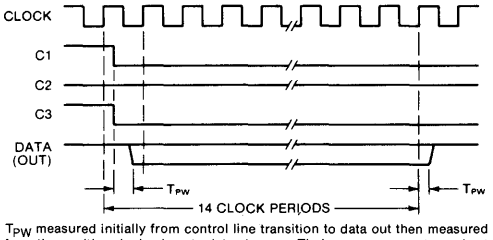


Fig.2 READ



T_{PW} measured initially from control line transition to data out then measured from the positive clock edges to data changes. Timing measurements made at V_{SS} −2 and 0.8 Volt points.

Fig.3 SHIFT DATA OUT

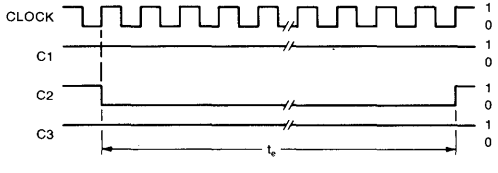


Fig.4 ERASE

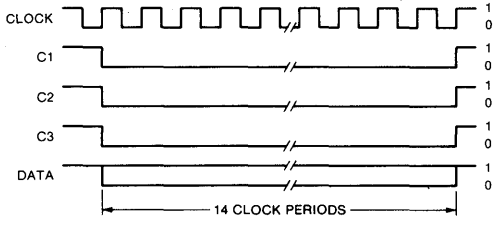


Fig.5 ACCEPT DATA

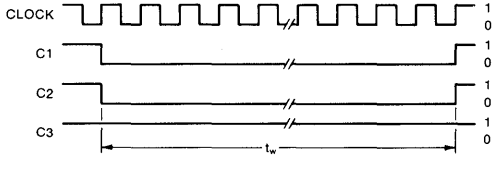


Fig.6 WRITE

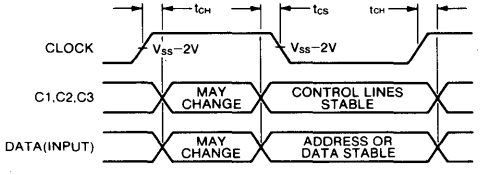


Fig.7 INPUT TIMING

GENERAL INSTRUMENT

ER1400

1400 Bit Serial Electrically Alterable Read Only Memory

FEATURES

- 100 Word x 14 Bit Organization
- Addressing by Two Consecutive One-of-Ten Codes
- Single −35 Volt Supply
- Word Alterable
- 10 Year Data Storage
- MOS Compatible Signal Levels
- Write/Erase Time: 10ms

DESCRIPTION

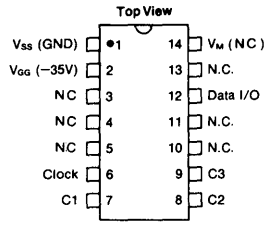
The ER1400 is a serial input/output 1400 bit electrically erasable and reprogramable ROM, organized as 100 words of 14 bits each. Data and address are communicated in serial form via a one-pin bidirectional bus.

Mode selection is by a 3 bit code applied to C1, C2 and C3.

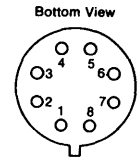
Before writing, a selected location must be preconditioned by an Erase operation. Data is then stored by internal negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 1400 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

PIN CONFIGURATIONS

Standard package
14 LEAD DUAL IN LINE



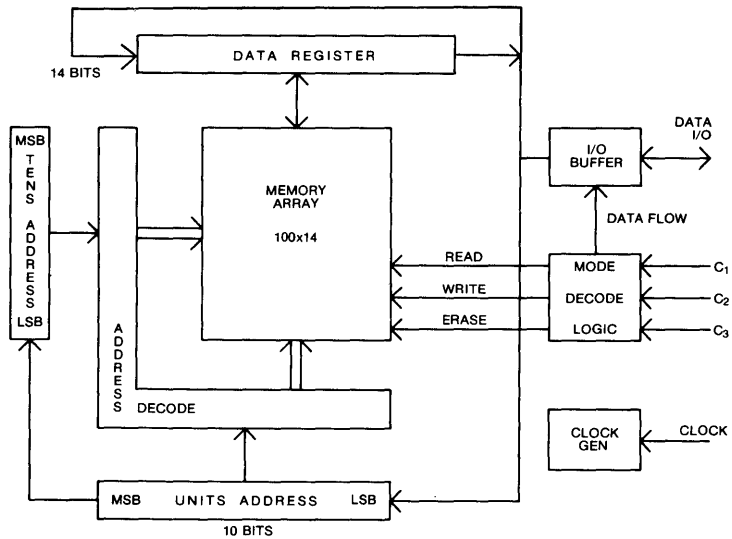
Special Order Package
8 LEAD TO-8 (ER1400T)



1. Data I/O
2. V_M (NC)
3. V_{SS} (GND)
4. V_{GG} (−35V)
5. Clock
6. C1
7. C2
8. C3

NC = No external connection for normal usage

BLOCK DIAGRAM



PIN FUNCTIONS

Name	Function
Data	In the Accept Address and Accept Data modes, this pin is an input pin for address and data respectively. When outputting data it has MOS drive capability, while in all other modes it is left floating.
V_M	Used for testing purposes only. Must be left unconnected for normal operation.
V_{SS}	Chip substrate. Normally connected to ground.
V_{GG}	DC supply. Normally connected to V_{SS} −35 Volt supply.
Clock	Timing reference. Required for all operations. May be left at logic zero when device is in standby.
C1,C2,C3	Mode control pins. Their operation is as follows:

C1	C2	C3	Function
0	0	0	Standby—the output buffer is left floating. If the clock is maintained, the contents of the Address and Data Registers will remain unchanged.
0	1	1	Accept Address—Data presented at the I/O pin is shifted into the Address Register with each clock pulse. Addressing is by two consecutive one-of-ten codes.
1	0	0	Read—The address word is read from memory into the data register.
1	0	1	Shift Data Out—The output driver is enabled and the contents of the Data Register are shifted out one bit with each clock pulse.
0	1	0	Erase—The word stored at the addressed location is erased to all ones.
1	1	1	Accept Data—The data register accepts serial data presented at the I/O pin. The Address Register remains unchanged.
1	1	0	Write—The word contained in the Data Register is written into the location designated by the Address Register.
0	0	1	Not Used

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs (except V_{GG}) with respect to V_{SS} . . −20V to +0.3V
V_{GG} with respect to V_{SS} . . . . . −40V
Storage temperature (No Data Retention) . . . . . −65° C to +150° C
Storage temperature (with Data Retention)
Operating . . . . . −25° C to +75° C
Unpowered . . . . . −65° C to +80° C

Standard Conditions (unless otherwise noted):

V_{SS} = GND
V_{GG} = −35V ±8%
Operating Temperature T_A = 0° C to +70° C

* Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

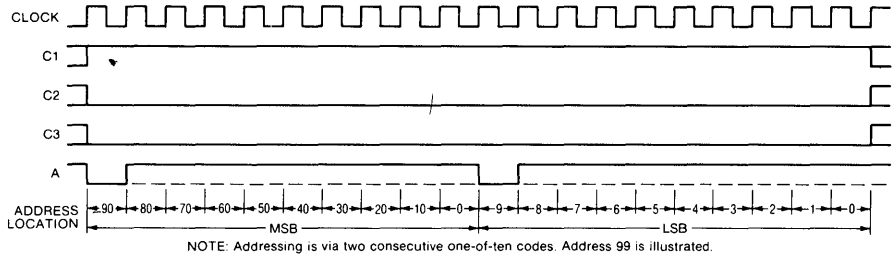
Characteristics	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Input Logic "1"	V_{IL}	V_{SS}−15	—	V_{SS}−8	Volts	
Input Logic "0"	V_{IH}	V_{SS}−1	—	V_{SS}+0.3	Volts	
Input Leakage	I_L	—	—	10	μA	V_{IN} = −15V
Output Logic "1"	V_{OL}	—	—	V_{SS}−10	Volts	Load = 1.5 Meg, 100pf
Output Logic "0"	V_{OH}	V_{SS}−1	—	V_{SS}+0.3	Volts	I_{SOURCE} = 200μA
Power Consumption	P_{GG}	—	—	300	mW	
Power Supply Current	I_{GG}	—	—	12	mA	
AC CHARACTERISTICS						
Clock Frequency	fϕ	10	14	17	KHz	
Clock Duty Cycle	Dϕ	35	50	65	%	
Write Time	tw	10	15	24	ms	
Erase Time	te	10	15	24	ms	
Rise, Fall Time	tr, tf	—	—	1	μs	
Control, Data Set Up Time	t_{CS}	1	—	—	μs	
Control, Data Hold Time	t_{CH}	0	—	—	μs	
Propagation Delay	tpw	—	—	20	μs	Load − 1 Meg. 100pf
Non-Volatile Data Storage	T_S	10	—	—	Years	See Note 1.
Number of Erase/Write Cycles	N_W	—	—	10^4	—	Per word. See Note 2.
Number of Read Accesses Between Writes	N_{RA}	10^9	—	—	—	Per word

** Typical values are at +25° C and nominal voltages.

NOTE 1: T_S is for powered or unpowered storage.

NOTE 2: N_W ($=10^4$) is a maximum for data retention times greater than 10 years. Beyond 10^4 reprograming cycles, there is a gradual, logarithmic reduction in retention time with 1 year being a typical value after 10^5 cycles.

TIMING DIAGRAMS



NOTE: Addressing is via two consecutive one-of-ten codes. Address 99 is illustrated.

Fig.1 ACCEPT ADDRESS

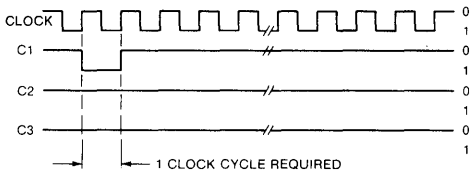
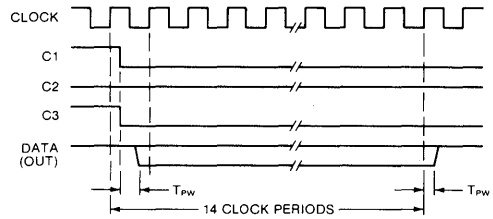


Fig.2 READ



T_{PW} measured initially from control line transition to data out, then measured from the positive clock edges to data changes. Timing measurements are made at $V_{SS}-2$ and -10 volt points.

Fig.3 SHIFT DATA OUT

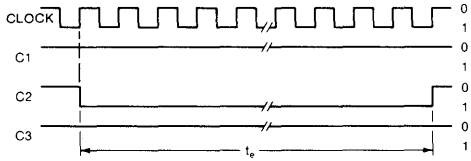


Fig.4 ERASE

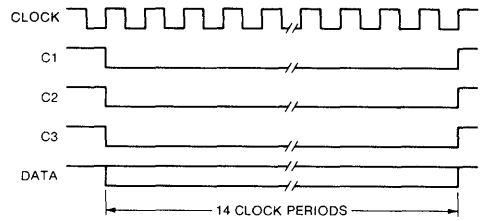


Fig.5 ACCEPT DATA

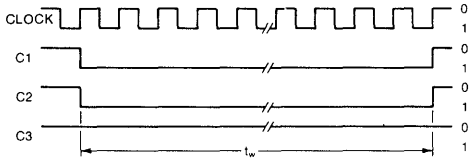


Fig.6 WRITE

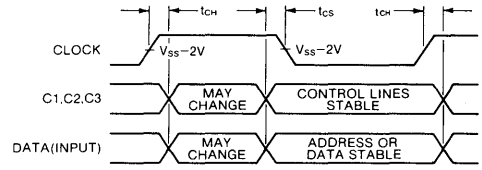


Fig.7 INPUT TIMING

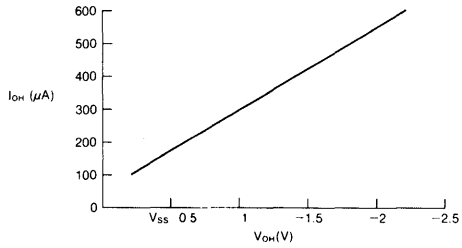


Fig.8 TYPICAL OUTPUT SOURCE CURRENT vs OUTPUT VOLTAGE

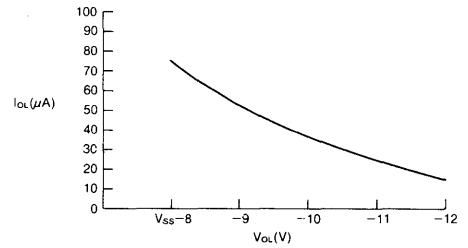


Fig.9 TYPICAL OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

GENERAL INSTRUMENT

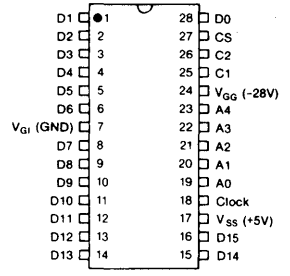
ER2051
ER2051IR
ER2051HR

512 Bit Electrically Alterable Read Only Memory

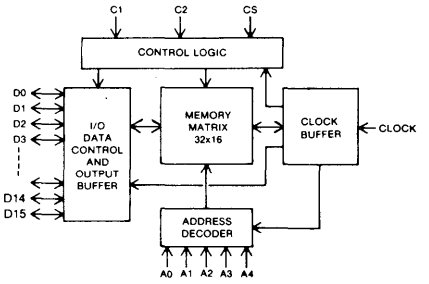
- 32 Word x 16 Bit Organization
- 5 Bit Binary Addressing
- +5, −28V Power Supplies
- Word Alterable
- 10 Year Data Storage for ER2051 (at +70° C)
- 1 Year Data Storage for ER2051 IR (at +85° C) and ER2051 HR (at +125° C)
- TTL Compatibility with Pull-Up Resistors on Inputs
- Tri-State Outputs
- Read Time: 1μs (ER2051), 2μs (ER2051 IR and ER2051 HR)
- Write/Erase Time: 50ms (ER2051), 100ms (ER2051 HR)
- No Voltage Switching Required
- Chip Select
- Two Extended Temperature Ranges:
  −40° C to +85° C (Industrial) ER2051 IR
  −55° C to +125° C (Hi-Rel) ER2051 HR

PIN CONFIGURATION

28 LEAD DUAL IN LINE Top View



BLOCK DIAGRAM



DESCRIPTION

The ER2051, ER2051 IR and ER2051 HR are fully decoded 32 x 16 electrically erasable and reprogramable ROMs. Write, erase, and read voltages are switched internally via a 2-bit code applied to C1 and C2.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 512 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

The EAROM may be operated with the V_{SS} power supply between +5V and +10Volts, as long as the V_{SS}—V_{GG} always equals 33 Volts. Thus, V_{SS} can be +5Volts for TTL compatibility or up to +10Volts for CMOS compatibility, if V_{GG} is appropriately adjusted.

The ER2051 IR and ER2051 HR are screened to Mil Std. 883B/ method 5004.1/level B, pre-cap visual inspection, environmental testing, burn-in and external visual. They are available in 28 lead ceramic dual in line packages.

OPERATION

Data is stored in a two transistor memory cell. After the cell is preconditioned by an erase signal (which causes a positive shift in the threshold of both transistors), data is written into one of the transistors making its threshold more negative. A sensing flip flop is used to read the memory cell and presents a logic high or low to the output depending on which transistor is "written."

It is important to note two things: first, that an erase is required before a wire to precondition the cell, and second, that after an erase, both transistors will have the same threshold voltage and valid data will not be present at the output.

The ER2051, ER2051 IR and ER2051 HR EAROMs use dynamic, edge triggered circuits internally. This requires either a mode change, a clock or a transition of the chip select between successive operations. Thus successive operations in the same mode must be separated by transitions of one of these four lines. Clock pulses are not normally required during erase or write operations, but are needed for successive operations if the chip select is held high, i.e., applications where one EAROM is used.

PIN FUNCTIONS

Name	Function
A_0-A_4	5-Bit Word Address
D_0-D_{15}	Data input and output pins
CS	Chip Select. Chip selected at logic "1". When chip select is at logic "0", outputs are open circuit, read, write and erase are disabled. Power is reduced.
C1, C2	Mode Control Inputs C1 C2 0 1 Erase Mode: stored data is erased at addressed location. 1 Don't Care Read Mode: addressed data read after clock pulse. Output data retained at output pins until chip deselected or control lines switched. 0 0 Write Mode: input data written at addressed location. Clock not required.
CLK	Clock input. Pulse to logic "1" for read operation.
V_{SS}	Substrate supply. Normally at +5 volts.
V_{GI}	Ground Input.
V_{GG}	Power Supply Input. Normally at −28 volts.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All input and outputs (with respect to V_{SS}) ..... −35V to +0.3V
Storage temperature ..... −65°C to +150°C
Soldering temperature of leads (10 seconds)..... +300°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

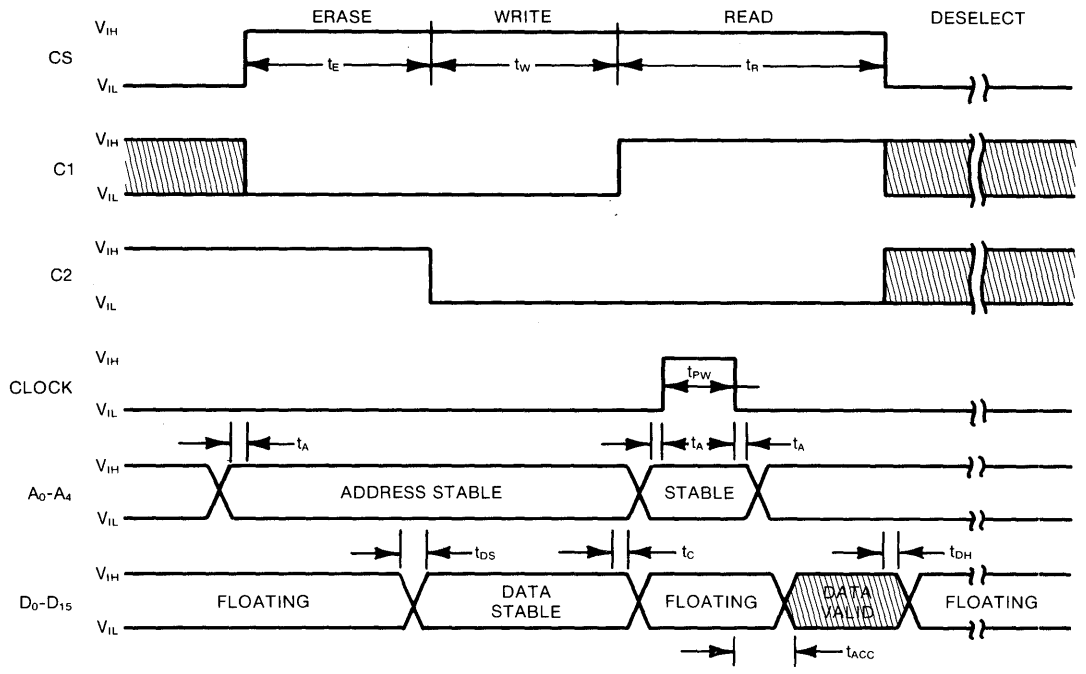
Standard Conditions (for TTL compatibility)

V_{SS} = +5V ±5%
V_{GG} = −28V ±5%
v_{GI} = GND
Operating Temperature T_A = 0°C to +70°C for ER2051
T_A = −40°C to +85°C for ER2051 IR
T_A = −55°C to +125°C for ER2051 HR
Output Load = 100pf, 1 TTL load

		ER2051			ER2051 IR/ER2051 HR				
Characteristics	**Sym**	**Min.**	**Typ.****	**Max.**	**Min.**	**Typ.****	**Max.**	**Units**	**Conditions**
DC CHARACTERISTICS									
Input Logic "1"	V_{IH}	V_{SS} −1.5	—	V_{SS} +0.3	V_{SS} −1.5	—	V_{SS} +0.3	V	
Input Logic "0"	V_{IL}	V_{SS} −15	—	0.8	V_{SS} −10	—	0.6	V	
Output Logic "1"	V_{OH}	V_{SS} −1.5	—	—	V_{SS} −1.5	—	—	V	I_{OH} = 100μA
Output Logic "0"	V_{OL}	—	—	0.6	—	—	0.6	V	I_{OL} = 1.6mA for V_{SS} = 5V
Input Leakage	I_L	—	2	10	—	2	10	μA	V_{IN} = V_{SS} −15
Output Leakage	I_O	—	2	10	—	2	10	μA	Chip deselected
Power Supply Current									
Read	I_{GG}	—	—	14	—	—	18	mA	I_{GG} returned through V_{SS}
Write	I_{GG}	—	—	11	—	—	15	mA	
Erase	I_{GG}	—	—	11	—	—	15	mA	
Deselected	I_{GG}	—	—	9	—	—	12	mA	
AC CHARACTERISTICS									
Access Time	t_{ACC}	—	—	1	—	—	2	μs	
Clock Pulse width	t_{PW}	2	—	20	2	—	20	μs	
Erase Cycle Time	t_E	50	—	200	100	—	200	ms	
Write Cycle Time	t_W	50	—	200	100	—	200	ms	
Read Cycle Time	t_R	3.5	—	24	4.5	—	25	μs	
Address to Clock Time	t_A	50	—	—	50	—	—	ns	
Data Set Up Time	t_{DS}	50	—	—	50	—	—	ns	
Data Hold Time	t_{DH}	50	—	—	50	—	—	ns	
Control to Address & Data Change	t_C	0	—	—	0	—	—	ns	
Number of Reads/Word Refresh	N_{RA}	10''	—	—	10''	—	—		
Number of Erase/Write Cycles	N_W	10^6	—	—	10^5	—	—	—	
Input Capacitance (All Pins)	C_{10}	—	8	15	—	8	15	pf	
Unpowered Data Storage Time	t_S	10	—	—	1	—	—	Years	at max temperature
Power Dissipation Read Cycle	P_D	—	450	500	—	450	500	mW	at 25°C V_{SS} = +5, V_{GG} = −29
	P_D	not applicable			—	—	500	mW	at 125°C V_{SS} = +5, V_{GG} = −29
	P_D	not applicable			—	—	600	mW	at −55°C V_{SS} = +5, V_{GG} = −29
Pulse Rise, Fall Time	t_{rl}, t_r	10	—	100	10	—	100	ns	

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAM



512 Bit Electrically Alterable Read Only Memory

FEATURES

- 64 Word x 8 Bit Organization
- 6 Bit Binary Addressing
- +5, −28V Power Supplies
- Word Alterable
- 10 Year Data Storage for ER2055 (at +70° C)
- 1 Year Data Storage for ER2055 IR (at +85° C) and ER2055 HR (at +125° C)
- TTL Compatible with Pull-Up Resistors on Inputs
- Tri-State Outputs
- Read Time: 2μs (ER2055), 4μs (ER2055 IR and ER2055 HR)
- Write/Erase Time: 50ms (ER2055), 100ms (ER2055 HR)
- No Voltage Switching Required
- 2 Chip Selects
- Two Extended Temperature Ranges:
  −40° C to +85° C (Industrial) ER2055 IR
  −55° C to +125° C (Hi-Rel) ER2055 HR

DESCRIPTION

The ER2055 is a fully decoded 64 x 8 electrically erasable and reprogramable ROM. Write, erase, and read voltages are switched internally via a 2-bit code applied to C1 and C2.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 512 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

OPERATION

Data is stored in a two transistor memory cell. After the cell is preconditioned by an erase signal (which causes a positive shift in the threshold of both transistors), data is written into one of the transistors making its threshold more negative. A sensing flip flop is used to read the memory cell and presents a logic high or low to the output depending on which transistor is "written".

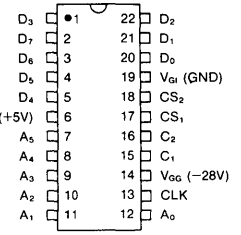
The ER2055 EAROM may be operated with V_{SS} between +5 and +10 volts for either TTL or CMOS compatibility. The negative power supply, V_{GG}, should be adjusted so that the difference between V_{SS} and V_{GG} is always 33 volts.

It is important to note two things: first, that an erase is required before a write to precondition the cell, and second, that after an erase, both transistors will have the same threshold voltage and valid data will not be present at the output.

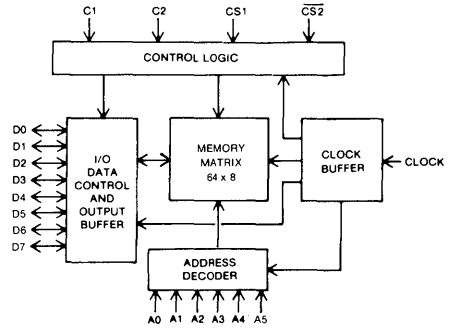
PIN CONFIGURATION

22 LEAD DUAL IN LINE

Top View



BLOCK DIAGRAM



The ER2055 EAROM uses dynamic edge triggered circuits internally. This requires either a mode change, a clock or a transition of the chip selects between successive operations. Thus successive operations in the same mode must be separated by transition of one of these four lines. Clock pulses are not normally required during erase or write operations, but are needed for successive operations if the chip is continuously selected, i.e., applications where one EAROM is used.

The ER2055IR and ER2055HR are screened to Mil Std. 883B/ method 5004. 1/level B, pre-cap visual inspection, environmental testing, burn-in and external visual. They are available in 28 lead ceramic dual in-line packages.

PIN FUNCTIONS

Name	Function
A_0-A_5	6-Bit Word Address
D_0-D_7	Data input and output pins
CS1, $\overline{CS2}$	Chip Selects Chip selected at logic "1" on CS1 and logic "0" on $\overline{CS2}$. When chip is not selected, outputs are open circuit, read, write and erase are disabled. Power is reduced.
C1, C2	Mode Control Inputs C1 / C2 0 / 1 — Erase Mode: stored data is erased at addressed location. 1 / Don't Care — Read Mode: addressed data read after clock pulse. Output data retained at output pins until chip deselected or control lines switched. 0 / 0 — Write Mode: input data written at addressed location. Clock not required.
CLK	Clock Input. Pulse to logic "1" for read operation.
V_{SS}	Substrate supply. Normally at +5 volts.
V_{GI}	Ground Input.
V_{GG}	Power Supply Input. Normally at −28 volts.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs (with respect to V_{SS}) ..... −35V to +0.3V
Storage temperature ..... −65°C to +150°C
Soldering temperature of leads (10 seconds) ..... +300°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

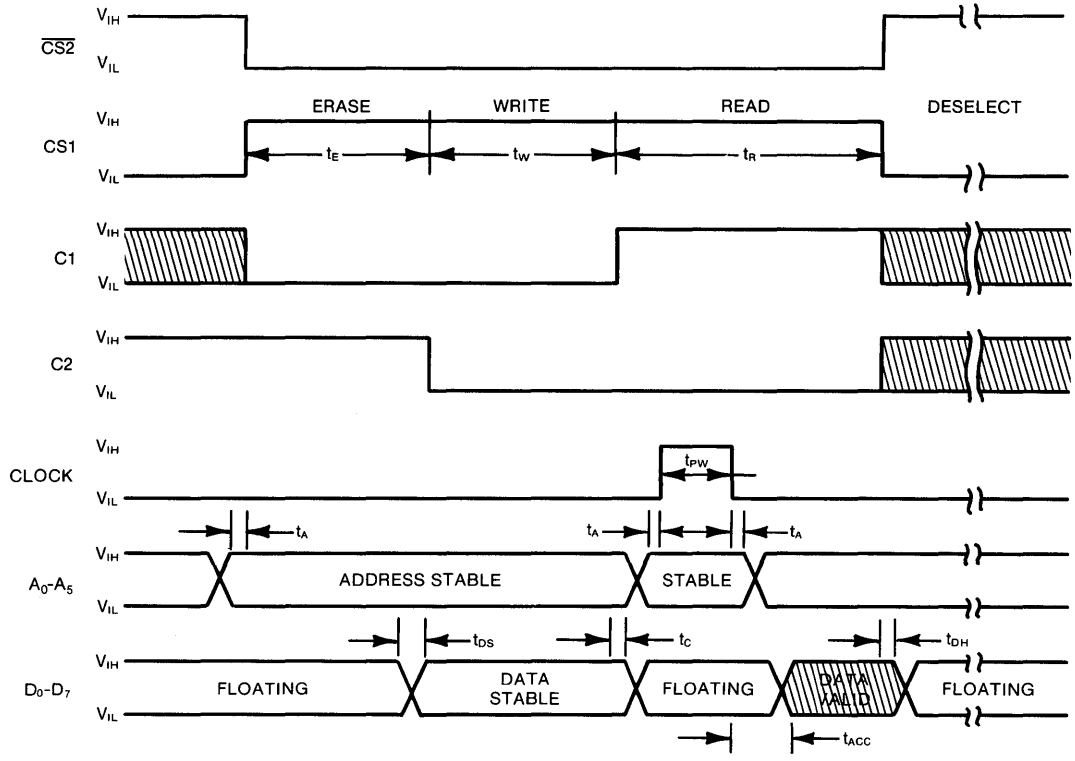
Standard Conditions (for TTL Compatibility)

$V_{SS} = +5V \pm 5\%$
$V_{GG} = -28V \pm 5\%$
$V_{GI} = GND$
Operating Temperature $T_A = 0°C$ to $+70°C$ for ER2055
$T_A = -40°C$ to $+85°C$ for ER2055IR
$T_A = -55°C$ to $+125°C$ for ER2055HR
Output Load = 100pf, 1 TTL load

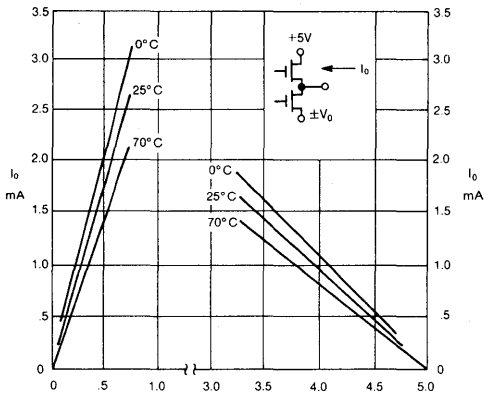
		ER2055			ER2055 IR/ER2055 HR				
Characteristics	**Sym**	**Min.**	**Typ.****	**Max.**	**Min.**	**Typ.****	**Max.**	**Units**	**Conditions**
DC CHARACTERISTICS									
Input Logic "1"	V_{IH}	$V_{SS}-1.5$	—	$V_{SS}+0.3$	$V_{SS}-1.5$	—	$V_{SS}+0.3$	V	
Input Logic "0"	V_{IL}	$V_{SS}-15$	—	0.8	$V_{SS}-10$	—	0.6	V	
Output Logic "1"	V_{OH}	$V_{SS}-1.5$	—	—	$V_{SS}-1.5$	—	—	V	$I_{OH} = 100\mu A$
Output Logic "0"	V_{OL}	—	—	0.6	—	—	0.6	V	$I_{OL} = 1.6mA$ for $V_{SS} = 5V$
Input Leakage	I_L	—	2	10	—	2	10	μA	$V_{IN} = V_{SS}-15$
Output Leakage	I_O	—	2	10	—	2	10	μA	Chip deselected
Power Supply Current									
Read	I_{GG}	—	8	10	—	8	18	mA	I_{SS} approx I_{GG}
Write	I_{GG}	—	6	7	—	6	9	mA	I_{SS} approx I_{GG}
Erase	I_{GG}	—	4	7	—	6	8	mA	I_{SS} approx I_{GG}
Deselected	I_{GG}	—	4	7	—	4	6	mA	I_{SS} approx I_{GG}
AC CHARACTERISTICS									
Access Time	t_{ACC}	—	—	2	—	—	4	μs	
Clock Pulse Width	t_{PW}	2	—	20	2	—	20	μs	
Erase Cycle Time	t_E	50	—	200	100	—	200	ms	
Write Cycle Time	t_W	50	—	200	100	—	200	ms	
Read Cycle Time	t_R	5	—	24	6	—	25	μs	
Address to Clock Time	t_A	50	—	—	50	—	—	ns	
Data Set Up Time	t_{DS}	50	—	—	50	—	—	ns	
Data Hold Time	t_{DH}	50	—	—	50	—	—	ns	
Control to Address & Data Change	t_C	0	—	—	0	—	—	ns	
Number of Reads/Word Refresh	N_{RA}	10^{11}	—	—	10^{11}	—	—		
Number of Erase/Write Cycles	N_W	10^6	—	—	10^5	—	—	—	
Input Capacitance (All Pins)	C_{IO}	—	6	10	—	6	10	pf	
Unpowered Data Storage Time	t_S	10	—	—	1	—	—	Years	at max temperature
Power Dissipation Read Cycle	P_D	—	450	500	—	450	500	mW	at 25°C $V_{SS} = +5$, $V_{GG} = -29$
	P_D	not applicable			—	—	500	mW	at 125°C $V_{SS} = +5$, $V_{GG} = -29$
	P_D	not applicable			—	—	600	mW	at −55°C $V_{SS} = +5$, $V_{GG} = -29$
Pulse Rise, Fall Time	t_{R1} t_F	10	—	100	10	—	100	ns	

**Typical values are at +25°C and nominal voltages.

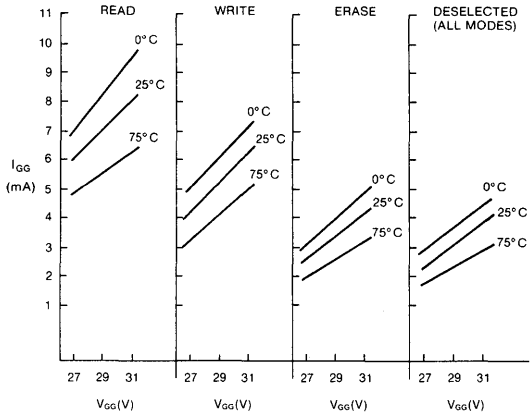
TIMING DIAGRAM



TYPICAL OUTPUT CHARACTERISTICS



TYPICAL SUPPLY CURRENT VS POWER SUPPLY VOLTAGE



GENERAL INSTRUMENT

ER5901
ER5901IR
ER5901HR

PRELIMINARY INFORMATION

Word Alterable 1K Bit Electrically Erasable Programable ROM

FEATURES

- 1024 Bits, Organized 128 x 8
- N-Channel Si-Gate SNOS Technology
- +5V Operation in All Modes; No High Voltages
- Fully TTL Compatible Inputs and Outputs
- On-Chip Latching of Addresses and Data
- Self-Timing, Processor Transparent Programing Mode with RDY/$\overline{\text{BUSY}}$ Signal
- Address and Data Buses may be used Separately or Multiplexed
- $\overline{\text{CE}}$ and $\overline{\text{OE}}$ Inputs to Avoid Bus Contention
- Word Alterable
- Read Access time of Less Than 200ns
- 10 Years' Data Retention over Temperature Range of −40° to +85°C
- Unlimited Read Accesses

DESCRIPTION

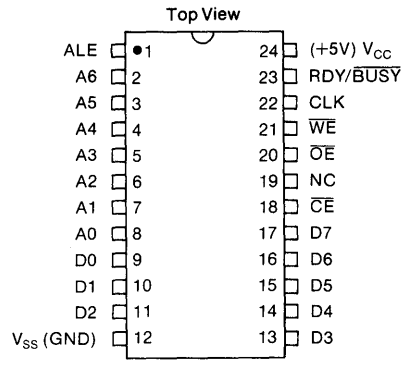
The ER5901 is a high speed electrically word erasable memory manufactured in the General Instrument proven SNOS technology. The key features of this device are its +5V only operation and microprocessor compatible architecture which allows the ER5901 to be accessed from the system bus in the same way as a static RAM.

Internal memory management has been incorporated in this device. On-board latching of address and data lines in the reprograming mode, and busy signal (RDY/$\overline{\text{BUSY}}$) output make this mode transparent to the host processor.

PIN CONFIGURATION

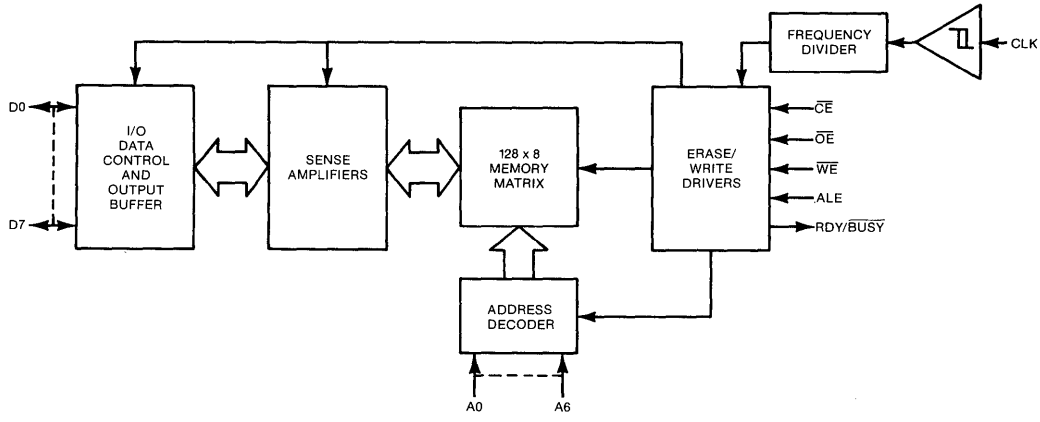
24 LEAD DUAL IN LINE

Top View



NC = No Internal Connection

BLOCK DIAGRAM



An ADDRESS LATCH ENABLE (ALE) input is provided so that memory may be used with a multiplexed address and data bus. When this feature is not required, ALE may be tied to $\overline{WE}$.

Bus contention problems are minimized by twin line control provided by CHIP ENABLE ($\overline{CE}$) and OUTPUT ENABLE ($\overline{OE}$).

By virtue of the on-chip reprograming control and timing of the ER5901, a minimum amount of servicing is required from a host microprocessor or microcomputer.

The user may select one of five operating modes:

1. READ with separate address and data lines.
2. READ with multiplexed address and data lines.
3. PROGRAM with separate address and data lines.
4. PROGRAM with multiplexed address and data lines.
5. STANDBY — power consumption is reduced by 66%.

PIN FUNCTIONS

Symbol	Function	Comments
ALE	Address Latch Enable	Address inputs latched on negative edge. May be tied to $\overline{WE}$ when separate address and data lines are used.
A0-A6	7 bit address	
D0-D7	8 bit data I/O	
V_{SS}	Chip Ground connection	
$\overline{CE}$	Chip Enable input	Used for chip selection.
$\overline{OE}$	Output Enable input	Gates data to output pins during read cycle.
$\overline{WE}$	Write Enable input	Enables reprograming cycle; input data latched on positive edge.
CLK	Timing inputs	Defines clock frequency for reprograming. May be RC or external clock.
RDY/$\overline{BUSY}$	Status output	Low when chip is in reprograming mode and cannot be accessed. High when in read mode.
V_{CC}	+5 Volt power connection	

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs with respect to Ground ..... +6V to −0.3V
Storage temperature (unpowered and without data retention) ..... −65°C to +150°C
Soldering temperature of leads (10 secs.) ..... +300°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted)

V_{SS} = GND
V_{CC} = +5V ±10% Volts
Operating Temperature Ranges T_A: 0°C to + 70°C (Commercial)
−40°C to +85°C (Industrial)
−55°C to +125°C (Military)

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Input Logic "1"	V_{IH}	2	—	V_{CC}+0.3	V	
Input Logic "0"	V_{IL}	−0.1	—	+0.8	V	
Output Logic "1"	V_{OH}	2.4	—	V_{CC}	V	I_{OH} = 400μA
Output Logic "0"	V_{OL}	—	—	0.4	V	I_{OL} = 1.6mA
Input Leakage Current	I_{IL}	—	—	10	μA	V_{IN} = 5.25V
Output Leakage Current	I_{OL}	—	—	10	μA	V_{OUT} = 5.25V
Power Supply Requirements						
V_{CC} Supply:						
Chip Selected	I_{CC}	—	35	80	mA	V_{CC} = +5.5V
Chip Deselected (Standby Mode)	I_{CC}	—	12	35	mA	V_{CC}= +5.5V
Power Dissipation:						
Chip Selected	P_D	—	195	300	mW	V_{CC} = +5.5V
Chip Deselected (Standby Mode)	P_D	—	66	100	mW	V_{CC} = +5.5V

AC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Input Capacitance	C_I	—	—	6	pf	V_{IN} = 0V
Output Capacitance	C_O	—	—	10	pf	V_{OUT} = 0V

MEMORY CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Erased State	V_E	—	V_{IH}, V_{OH}	—	V	
Written State	V_W	—	V_{IL}, V_{OL}	—	V	
Data Retention Time (Powered or Unpowered)	t_S	10	—	—	Years	
Number of Reprograming Cycles per Byte	N_P	10^4	—	—	—	See Note
Number of Read Accesses Between Refresh	N_{RA}	Unlimited				

NOTE:
There is a tradeoff to be made between the data retention time (t_S) and the number of reprograming cycles (N_P) performed per address. A gradual logarithmic reduction in retention time is experienced as the number of reprograming cycles increases. The specified limit is merely one point on this curve and does not imply a sudden cutoff or end of life. After 10^4 cycles a typical retention time is 10 years.

MODE SELECTION: Multiplexed Address and Data Lines

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$(1)	ALE(2)	RDY/$\overline{BUSY}$
Standby	V_{IH}	Don't Care	Don't Care	Don't Care	V_{OH}
Read	V_{IL}	V_{IL}(3)	V_{IH}	⎍	V_{OH}
Program	V_{IL}	V_{IH}	⎎	⎍	V_{OL}

MODE SELECTION: Separate Address and Data Lines

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$/ALE(1, 2, 4)	RDY/$\overline{BUSY}$
Standby	V_{IH}	Don't Care	Don't Care	V_{OH}
Read	V_{IL}	V_{IL}	V_{IH}	V_{OH}
Program	V_{IL}	V_{IH}	⎎	V_{OL}

NOTES:
1. Data inputs latched on rising edge of $\overline{WE}$.
2. Address inputs latched on falling edge of ALE.
3. To avoid bus contention $\overline{OE}$ must be strobed when the device is used in the multiplexed mode.
4. $\overline{WE}$ and ALE inputs may be tied together when the device is used in the non-multiplexed mode.

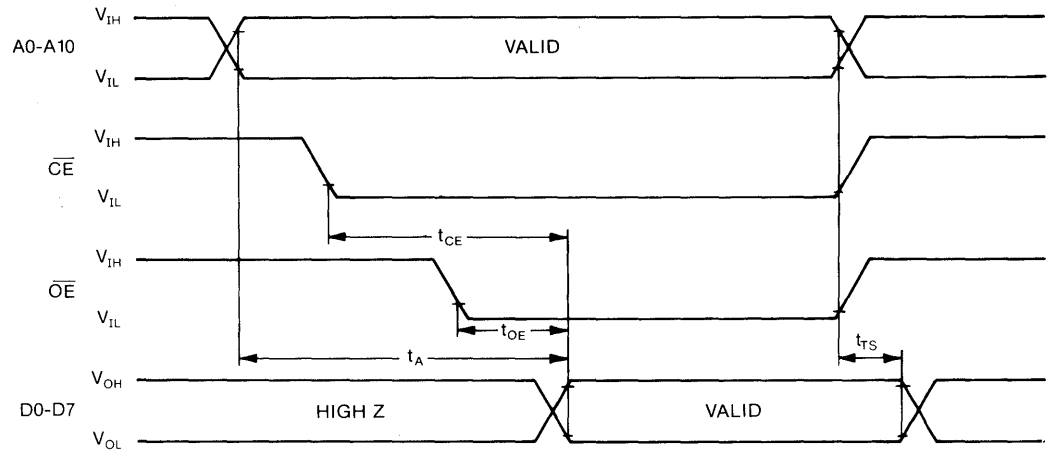


Fig. 1 READ MODE WITH SEPARATE ADDRESS AND DATA LINES

READ OPERATION (With Separate Address and Data Lines)

To initiate a read cycle a valid address must appear on the A_0 to A_6 inputs and remain there for the duration of the cycle because the address is not latched in this mode. $\overline{CE}$ may then be brought low to select the device. The desired memory byte will be in internal registers a short time later and will appear on data lines D_0 to D_7 after a time delay (t_{OE}) measured from the falling edge of $\overline{OE}$. Alternatively, if bus contention is not a problem, $\overline{OE}$ may be tied low. The maximum read access time (t_A) is 200ns, and data will remain valid until a logic level change occurs on $\overline{CE}$, $\overline{OE}$, or an address line. In this mode of operation ALE and $\overline{WE}$ are held high and may be tied together. (See Figure 1.)

READ MODE (Separate Address and Data Lines)

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Access Time — Address to Output Delay	t_A	—	—	200	ns	Load = 1 TTL gate + C_L = 100pf $\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	—	200	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	10	—	150	ns	$\overline{CE}$ = V_{IL}
Address — $\overline{CE}$ or $\overline{OE}$ to Output Tri-State	t_{TS}	10	—	75	ns	

RELATED APPLICATION NOTES

1223 New EEPROM Removes Separate Write/Erase Necessity

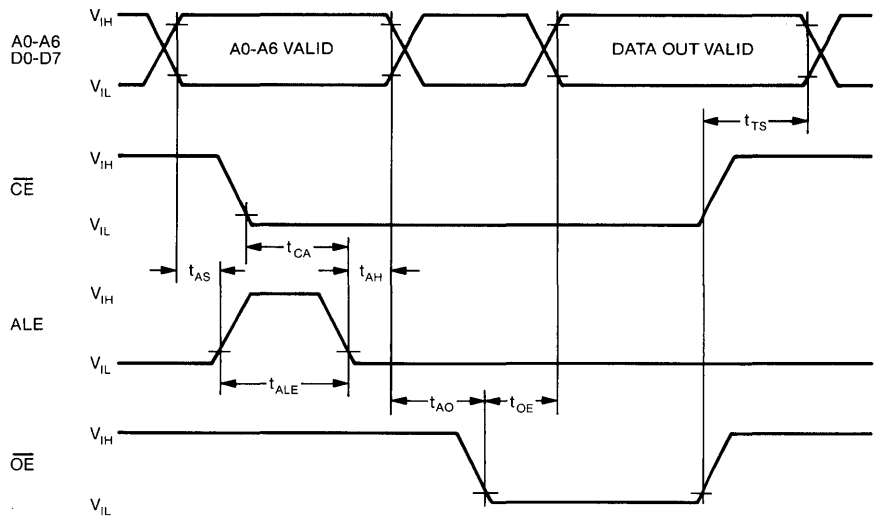


Fig. 2 READ MODE WITH MULTIPLEXED ADDRESS AND DATA LINES

READ OPERATION (With Multiplexed Address and Data Lines)

The ALE line is pulsed high, while a valid address is presented to the A_0 to A_6 inputs of a selected device. The address is latched into the ER5901 on the falling edge of ALE and, in order to avoid bus contention, these lines should be tri-stated prior to pulsing $\overline{OE}$ low. After a delay (t_{OE}), the selected byte will appear on lines D_0 to D_7 until either $\overline{OE}$ or $\overline{CE}$ goes high. (See Figure 2.)

READ MODE (Multiplexed Address and Data Lines)

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address Setup Time	t_{AS}	10	—	—	ns	
Chip Enable to Address Latch Enable	t_{CA}	100	—	—	ns	
ALE Pulse Width	t_{ALE}	100	—	—	ns	
Address Hold Time	t_{AH}	40	—	—	ns	
Address Float to Output Enable	t_{AO}	20	—	—	ns	
$\overline{OE}$ to Output Delay	t_{OE}	10	—	150	ns	$\overline{CE} = V_{IL}$
Address — $\overline{CE}$ or $\overline{OE}$ to Output Tri-State	t_{TS}	10	—	75	ns	

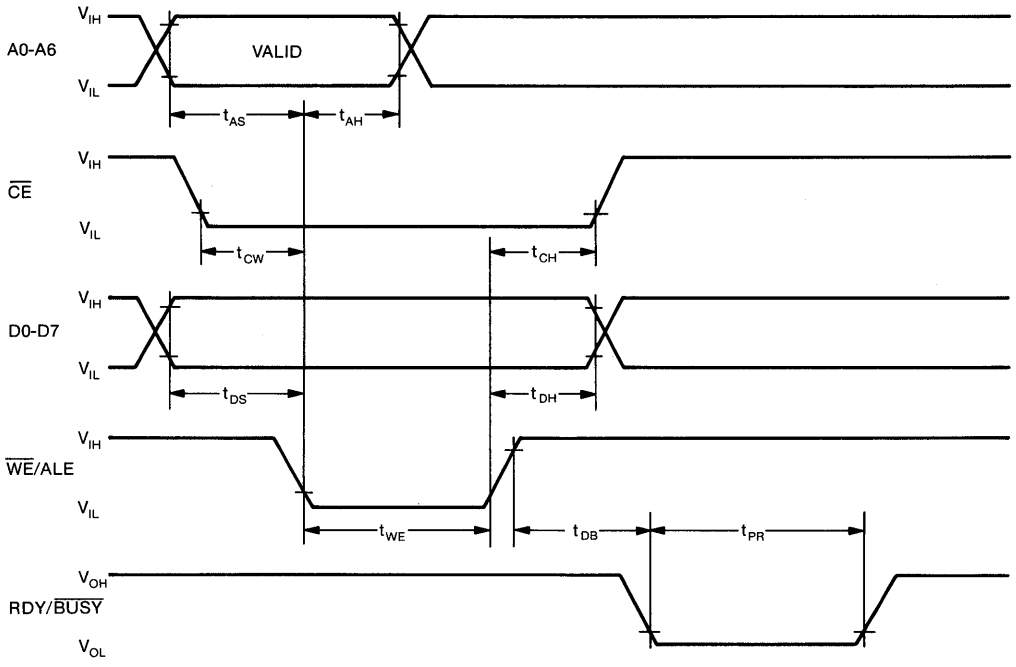


Fig. 3 PROGRAM MODE WITH SEPARATE ADDRESS AND DATA LINES

PROGRAM MODE (With Separate Address and Data Lines)

In this mode the ALE and $\overline{WE}$ inputs may be tied together. With a stable address and data word presented to the respective inputs of a selected device, the $\overline{WE}$/ALE line is pulsed low to initiate a program cycle. The falling edge of $\overline{WE}$/ALE latches the address inputs and the rising edge latches the data inputs. After a delay (t_{DB}), the RDY/$\overline{BUSY}$ output will go low and remain low for the duration of the programing cycle. All inputs to the ER5901 are disabled during a programing cycle. (See Figure 3.)

PROGRAM MODE (Separate Address and Data Lines)

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address Setup Time	t_{AS}	50	—	—	ns	
Chip Enable to Write Enable Delay	t_{CW}	100	—	—	ns	
Data Setup Time	t_{DS}	0	—	—	ns	
Address Hold Time	t_{AH}	40	—	—	ns	
Write Enable Pulse Width	t_{WE}	0.1	—	10	μs	
Data Hold Time	t_{DH}	40	—	—	ns	
$\overline{WE}$ to $\overline{CE}$ Delay	t_{CH}	0	—	—	ns	
Status Delay	t_{DB}	10	—	150	ns	
Status Low Time (Programing Time)	t_{PR}	20	—	100	ms	With min clock freq as defined by TI input
Program Clock Frequency	f_{PR}	10	—	50	KHz	

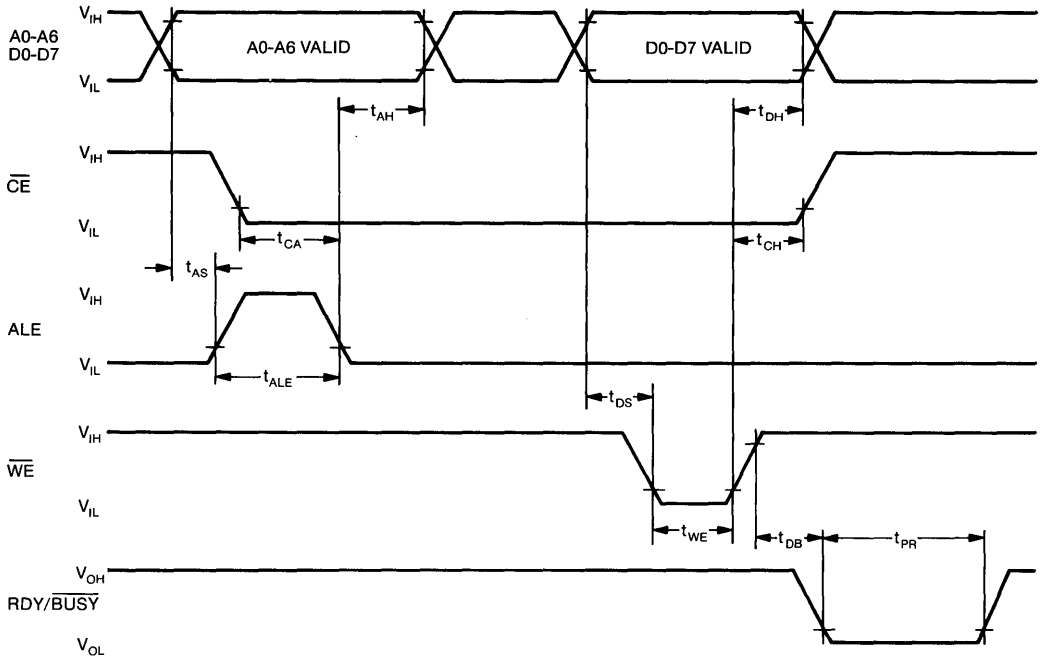


Fig. 4 PROGRAM MODE WITH MULTIPLEXED ADDRESS AND DATA LINE

PROGRAM MODE (With Multiplexed Address and Data Lines)

The ALE line is pulsed high while the address to be altered is presented to lines A_0 to A_6 of the selected device. The fall of ALE latches the address into the ER5901, and the information on the bus line is then changed to the data to be written into the EEPROM. $\overline{WE}$ is pulsed low and the data is latched on its rising edge. After a delay (t_{DB}), the RDY/$\overline{BUSY}$ output will go low for the duration of the programing cycle. (See Figure 4.)

PROGRAM MODE (Multiplexed Address and Data Lines)

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address Setup Time	t_{AS}	10	—	—	ns	
Chip Enable to Address Latch Enable	t_{CA}	100	—	—	ns	
ALE Pulse Width	t_{ALE}	100	—	—	ns	
Address Hold Time	t_{AH}	40	—	—	ns	
Data Setup Time	t_{DS}	10	—	—	ns	
$\overline{WE}$ Pulse Width	t_{WE}	0.1	—	10	μs	
Data Hold Time	t_{DH}	40	—	—	ns	
$\overline{WE}$ to $\overline{CE}$ Delay	t_{CH}	0	—	—	ns	
Status Delay	t_{STA}	10	—	150	ns	
Status Low Time (Programing Time)	t_{PR}	20	—	100	ms	With min clock freq as defined by TI input
Program Clock Frequency	f_{PR}	10	—	50	KHz	

GENERAL INSTRUMENT

ER3400
ER3400I/IR
ER3400HR

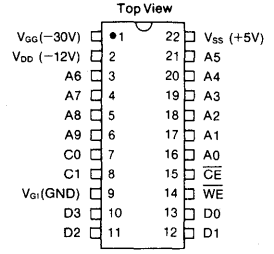
4096 Bit Electrically Alterable Read Only Memory

FEATURES

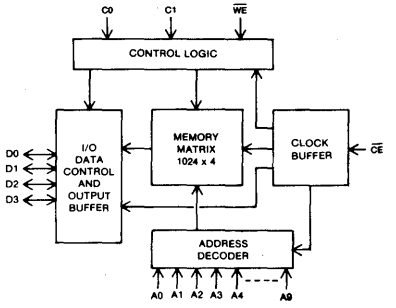
- 1024 Word x 4 Bit Organization
- Latched Address and Data Inputs
- Word or Block Alterable
- 10 Year Data Storage for ER3400
- 1 Year Data Storage for ER3400IR at +85° C and ER3400HR at +95° C
- TTL Compatible with Pull-Up Resistors on Inputs
- Tri-State Outputs
- Read Access Time: 900ns max
- Write Time: 1ms Erase Time: 10ms
- 10^9 Read Cycles/Word Between Refreshes
- 10^7 Read Cycles/Word for ER3400IR and ER3400HR
- Two Extended Temperature Ranges

PIN CONFIGURATION

22 LEAD DUAL IN LINE



BLOCK DIAGRAM



DESCRIPTION

The ER3400 is a 1024 x 4 bit fully decoded Electrically Alterable Read Only Memory fabricated in the General Instrument proven MNOS technology. Address, control and data inputs are latched on board the device thus releasing these lines during Erase and Write operations. Selection of one of the four modes of operation is made by setting the appropriate binary code on control lines C0 and C1. $\overline{CE}$ is used for chip selection and latching of address and control lines. $\overline{WE}$ is used to sample and latch input data on D0-D3 during a Write operation.

Power sequencing protection circuitry is provided on the ER3400 to protect against the accidental alteration of data during power Up/Down. However, due to the unpredictable nature of power up and power down sequences in some systems, it is important to apply and remove the programing voltage V_{GG} only when V_{SS} and V_{DD} are within their specified limits.

For applications requiring extended temperature ranges the ER3400I, ER3400IR and ER3400HR are available.

RELATED APPLICATION NOTES

1217 The ER3400: an easy to use 4K EAROM
1218 Interfacing the ER3400 to an eight bit microcomputer
1220 Generating EAROM programming voltages from a 5 volt supply
1210 Data retention testing of the ER3400

PIN FUNCTIONS

Name	Function
A0-A9	10-Bit Word Address
D0-D3	Data input and output pins
$\overline{CE}$	Chip Enable. Chip selected when $\overline{CE}$ is pulsed to logic "0".
C0, C1	Mode Control Inputs C0 C1 0 1 Block Erase Mode: erase operation performed on all words. 1 1 Word Erase Mode: stored data is erased at addressed location. 0 0 Read Mode: addressed data read after leading edge of $\overline{CE}$ pulse. 1 0 Write Mode: input data written at addressed location.
$\overline{WE}$	Write Enable. Input data read when $\overline{WE}$ is pulsed to logic "0".
V_{SS}	Substrate supply. Normally at +5 volts.
V_{GI}	Ground Input
V_{DD}	Power Supply Input. Normally at -12 volts.
V_{GG}	Power Supply Input. Normally at -30 volts.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs except V_{GG} (with respect to V_{SS}) .... −20V to +0.3V
Storage temperature (without data retention) ..... −65° C to +150° C
Soldering temperature of leads (10 seconds) ..... +300° C

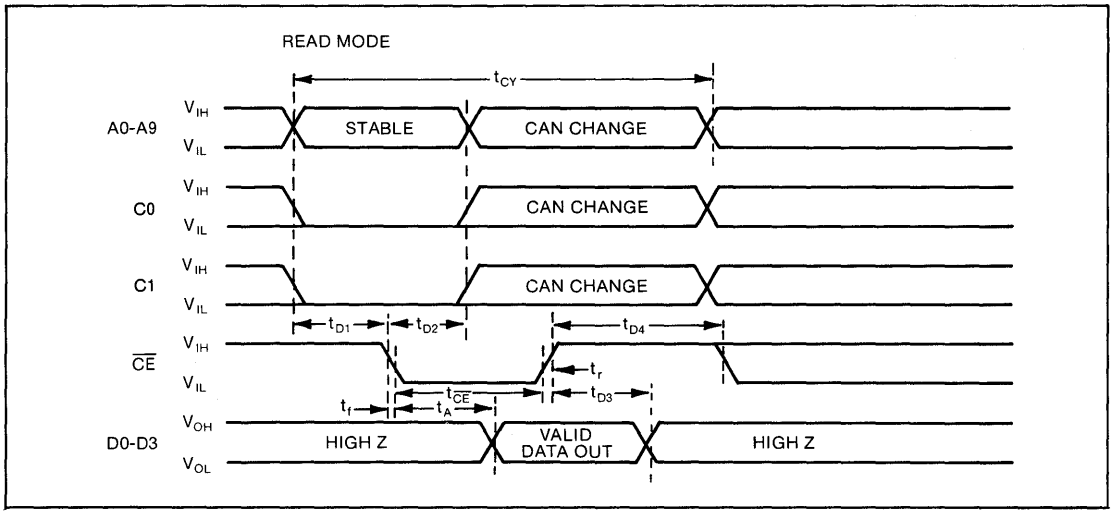
*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Condition (unless otherwise noted)

V_{SS} = +5V to ±5%
V_{DD} = −12V ±5%
V_{GG} = −30V ±5%
V_{GI} = GND
Operating Temperature (T_A) = 0° C to +70° C (ER3400)
−40° C to +85° C (ER3400I/IR)
−55° C to +95° C (ER3400HR)

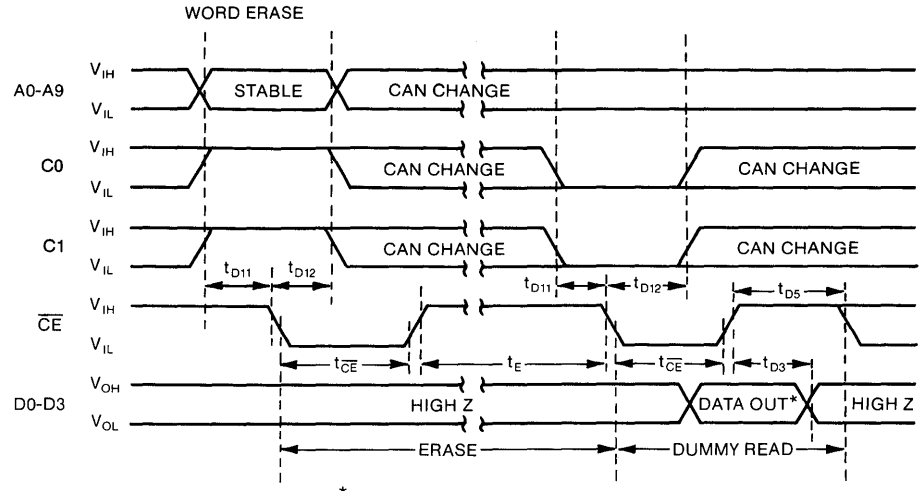
		ER3400			ER3400IR/ER3400HR				
Characteristic	**Sym**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
DC CHARACTERISTICS									
Input Logic "1"	V_{IH}	V_{SS} −1.5	—	V_{SS} +0.15	V_{SS} −1	—	V_{SS} +0.15	V	
Input Logic "0"	V_{IL}	−10	—	0.8	−10	—	0.6	V	
Output Logic "1"	V_{OH}	V_{SS} −1.5	—	—	V_{SS} −1.5	—	—	V	I_{OH} = 2mA
Output Logic "0"	V_{OL}	—	—	0.4	—	—	0.5	V	I_{OL} = 2mA
Control Input Leakage	I_{LC}	—	—	−2	—	—	−2	μA	V_{ON} = V_{SS} −15 Volts
Data Input Leakage	I_{LD}	—	—	−10	—	—	−10	μA	V_{IN} = V_{SS} −15 Volts
Power Supply Current									
V_{DD} Supply Current: Chip Selected	I_{DD}	—	—	−25	—	—	−30	mA	V_{DD} = V_{SS} −17 Volts
Chip De-Selected	I_{DD}	—	—	−12	—	—	−15	mA	V_{DD} = V_{SS} −17 Volts
V_{GG} Supply Current: Write Mode	I_{GG}	—	—	−4	—	—	−5	mA	V_{GG} = V_{SS} −35 Volts
V_{SS} Supply Current: Chip Selected	I_{SS}	—	—	−31	—	—	−37	mA	V_{GG} = V_{SS} −17V, V_{GG} = V_{SS} −35V
Chip De-Selected	I_{SS}	—	—	−14.5	—	—	−18	mA	V_{GG} = V_{SS} −17V, V_{GG} = V_{SS} −35V
AC CHARACTERISTICS									
Input Capacitance—Control Inputs	C_I	—	6	8	—	6	8	pf	
Input Capacitance—Data Inputs	C_D	—	8	10	—	8	10	pf	



Characteristics	Sym	ER3400 Min	ER3400 Max	ER3400IR/HR Min	ER3400IR/HR Max	Unit	Conditions
Read Cycle Time	t_{CY}	1700	—	1750	—	ns	
Address and Control to $\overline{CE}$	t_{D1}	100	—	100	—	ns	
Address and Control Hold Time	t_{D2}	250	—	350	—	ns	
$\overline{CE}$ Rise to Data Tri-State	t_{D3}	50	300	50	350	ns	
$\overline{CE}$ High	t_{D4}	700	—	750	—	ns	
Access Time	t_A	—	900	—	1000	ns	Load = 2K + 100pf to V_{SS}
$\overline{CE}$ Pulse Width	$t_{\overline{CE}}$	1	50	1	50	μs	
$\overline{CE}$ Rise, Fall Time	t_r, t_f	10	100	10	100	ns	
Number of Read Accesses per Location Between Refresh	N_{RA}	10^9	—	10^7	—	—	

READ OPERATION

Address and control line inputs are latched on the falling edge of $\overline{CE}$. With control lines C0 and C1 both low a read cycle will be initiated. After the access time (t_A) the data read will be output on data lines D0-D3. $\overline{CE}$ must be held high for a minimum of 700ns between memory read cycles. To reduce power consumption the ER3400 may be operated with V_{GG} held at V_{SS} in the read mode.



*Data output during a Dummy Read is not valid.

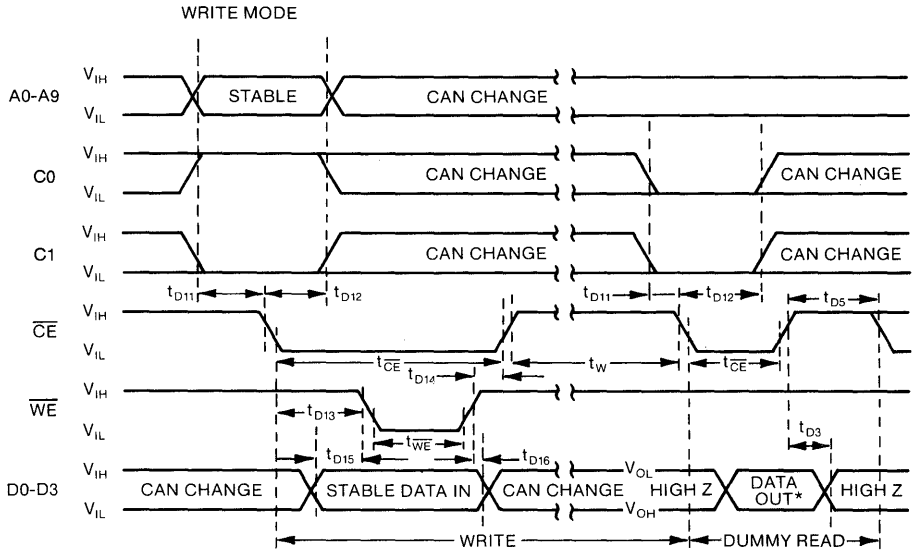
Characteristics	Sym	ER3400 Min	ER3400 Max	ER3400IR/HR Min	ER3400IR/HR Max	Unit	Conditions
Address and Control to $\overline{CE}$	t_{D11}	100	—	100	—	ns	
Address and Control Hold Time	t_{D12}	250	—	250	—	ns	
$\overline{CE}$ Rise to Data Tri-state	t_{D3}	50	300	50	350	ns	
$\overline{CE}$ High (Dummy Read)	t_{D5}	1500	—	1500	—	ns	
$\overline{CE}$ Pulse Width	$t_{\overline{CE}}$	1	50	1	50	μs	
Erase Time	t_E	10	20	10	20	ms	

WORD ERASE OPERATION

An erase cycle is required prior to a write in order to precondition the memory cells to be written. A word erase operation erases only the four bits of the addressed memory location. The falling edge of $\overline{CE}$ latches the control inputs and the address of the word to be erased. The rising edge of $\overline{CE}$ in the erase mode signals the start of the erase cycle which produces a positive shift in the threshold of the selected MNOS memory transistors. An erase operation must be terminated by a dummy read operation. The dummy read need not occur on the same location as the preceding erase, therefore, the state of the address lines A0-A9 are immaterial during the dummy read cycle. Data output during a dummy read cycle is not valid data.

BLOCK ERASE OPERATION

A block erase operation erases all 4096 bits of memory to the "1" state, in all other respects the operation is identical to the word erase operation described above.



*Data output during a Dummy Read is not valid.

Characteristics	Sym	ER3400 Min	ER3400 Max	ER3400IR/HR Min	ER3400IR/HR Max	Unit	Conditions
Address and Control to $\overline{CE}$	t_{D11}	100	—	100	—	ns	
Address and Control Hold Time	t_{D12}	250	—	350	—	ns	
$\overline{CE}$ Fall to $\overline{WE}$ Fall Delay	t_{D13}	0	—	0	—	ns	$\overline{WE}$ rise may overlap $\overline{CE}$
$\overline{WE}$ Rise to $\overline{CE}$ Rise Delay	t_{D14}	−50	—	−100	—	ns	rise by 50ns max
Data Stable to $\overline{WE}$	t_{D15}	0	—	0	—	ns	
$\overline{WE}$ Rise to End of Data Stable	t_{D16}	100	—	100	—	ns	
$\overline{CE}$ Pulse Width	$t_{\overline{CE}}$	1	50	1	50	μs	
$\overline{WE}$ Pulse Width	$t_{\overline{WE}}$	500	—	650	—	ns	
Write Time	t_W	1	2	1	2	ms	
$\overline{CE}$ Rise to Data Tri-State	t_{D3}	50	300	50	350	ns	
$\overline{CE}$ High (Dummy Read)	t_{D5}	1500	—	1500	—	ns	
Unpowered Data Storage Time	t_S	10	—	1	—	Years	See Note 1
Number of Reprogramming Cycles	N_W	10^3	—	10^3	—	—	See Note 1
Number of Read Accesses/Location between Refresh	N_{RA}	10^9	—	10^9	—	—	

NOTE 1: Does not imply end of useful life. See Write Operation for further information.

WRITE OPERATION

Control lines C0 and C1 along with address lines A0-A9 are latched on the falling edge of $\overline{CE}$. Input data on D0-D3 is latched on the rising edge of $\overline{WE}$. $\overline{WE}$ may be tied to $\overline{CE}$ for all operations, however, this separate latching allows the ER3400 to be used in certain systems where address and data busses are multiplexed. The writing of the selected memory transistors is initiated by the rising edge of $\overline{CE}$. $\overline{CE}$ must remain high for the duration of the write time. A write operation can only be terminated by a dummy read. To avoid bus contention, the data lines must be tri-stated prior to initiating the dummy read cycle. The data output by a dummy read cycle is not valid data. The dummy read need not occur on the same location as the previous write, therefore, address line A0-A9 may be allowed to change during the dummy read cycle.

The specification of 10 years non-volatile data retention after a minimum of 10^3 reprograming cycles is merely one point on the curve of retention versus reprograming cycles and does not imply a sudden cut-off or end of life. As the number of Erase/Write cycles per address increases, a gradual, logarithmic reduction in data retention capability occurs with 1 year of retention being a typical figure after 10^4 cycles.

GENERAL INSTRUMENT

ER2055
ER2055IR
ER2055HR

512 Bit Electrically Alterable Read Only Memory

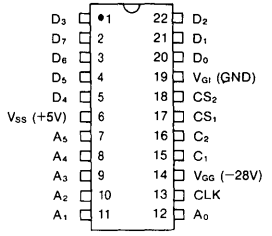
FEATURES

- 64 Word x 8 Bit Organization
- 6 Bit Binary Addressing
- +5, −28V Power Supplies
- Word Alterable
- 10 Year Data Storage for ER2055 (at +70° C)
- 1 Year Data Storage for ER2055 IR (at +85° C) and ER2055 HR (at +125° C)
- TTL Compatible with Pull-Up Resistors on Inputs
- Tri-State Outputs
- Read Time: 2μs (ER2055), 4μs (ER2055 IR and ER2055 HR)
- Write/Erase Time: 50ms (ER2055), 100ms (ER2055 HR)
- No Voltage Switching Required
- 2 Chip Selects
- Two Extended Temperature Ranges:
  −40° C to +85° C (Industrial) ER2055 IR
  −55° C to +125° C (Hi-Rel) ER2055 HR

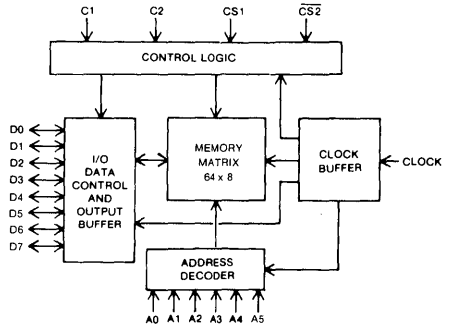
PIN CONFIGURATION

22 LEAD DUAL IN LINE

Top View



BLOCK DIAGRAM



DESCRIPTION

The ER2055 is a fully decoded 64 x 8 electrically erasable and reprogramable ROM. Write, erase, and read voltages are switched internally via a 2-bit code applied to C1 and C2.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 512 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

OPERATION

Data is stored in a two transistor memory cell. After the cell is preconditioned by an erase signal (which causes a positive shift in the threshold of both transistors), data is written into one of the transistors making its threshold more negative. A sensing flip flop is used to read the memory cell and presents a logic high or low to the output depending on which transistor is "written".

The ER2055 EAROM may be operated with V_{SS} between +5 and +10 volts for either TTL or CMOS compatibility. The negative power supply, V_{GG}, should be adjusted so that the difference between V_{SS} and V_{GG} is always 33 volts.

It is important to note two things: first, that an erase is required before a write to precondition the cell, and second, that after an erase, both transistors will have the same threshold voltage and valid data will not be present at the output.

The ER2055 EAROM uses dynamic edge triggered circuits internally. This requires either a mode change, a clock or a transition of the chip selects between successive operations. Thus successive operations in the same mode must be separated by transition of one of these four lines. Clock pulses are not normally required during erase or write operations, but are needed for successive operations if the chip is continuously selected, i.e., applications where one EAROM is used.

The ER2055IR and ER2055HR are screened to Mil Std. 883B/ method 5004. 1/level B, pre-cap visual inspection, environmental testing, burn-in and external visual. They are available in 28 lead ceramic dual in-line packages.

PIN FUNCTIONS

Name	Function
A_0-A_5	6-Bit Word Address
D_0-D_7	Data input and output pins
CS1, $\overline{CS2}$	Chip Selects Chip selected at logic "1" on CS1 and logic "0" on $\overline{CS2}$. When chip is not selected, outputs are open circuit, read, write and erase are disabled. Power is reduced.
C1, C2	Mode Control Inputs C1 / C2 0 / 1 — Erase Mode: stored data is erased at addressed location. 1 / Don't Care — Read Mode: addressed data read after clock pulse. Output data retained at output pins until chip deselected or control lines switched. 0 / 0 — Write Mode: input data written at addressed location. Clock not required.
CLK	Clock Input. Pulse to logic "1" for read operation.
V_{SS}	Substrate supply. Normally at +5 volts.
V_{GI}	Ground Input
V_{GG}	Power Supply Input. Normally at −28 volts.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs (with respect to V_{SS}) ..... −35V to +0.3V
Storage temperature ..... −65°C to +150°C
Soldering temperature of leads (10 seconds) ..... +300°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

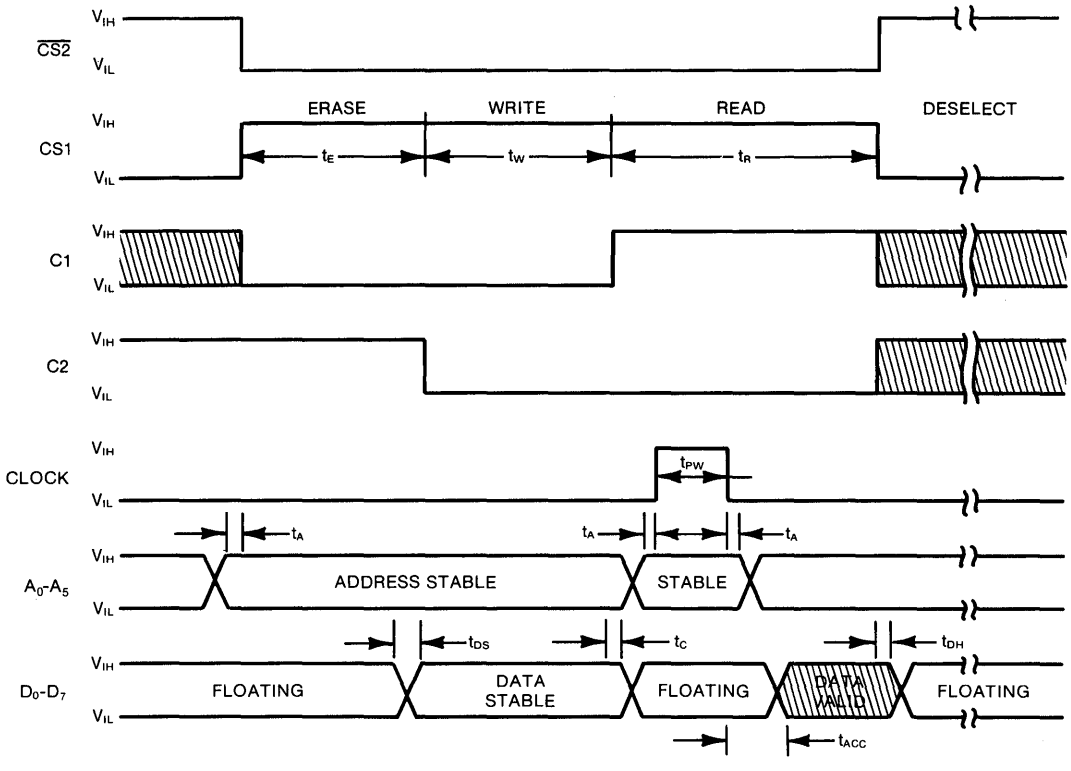
Standard Conditions (for TTL Compatibility)

$V_{SS} = +5V \pm 5\%$
$V_{GG} = -28V \pm 5\%$
$V_{GI} = GND$
Operating Temperature $T_A = 0°C$ to $+70°C$ for ER2055
$T_A = -40°C$ to $+85°C$ for ER2055IR
$T_A = -55°C$ to $+125°C$ for ER2055HR
Output Load = 100pf, 1 TTL load

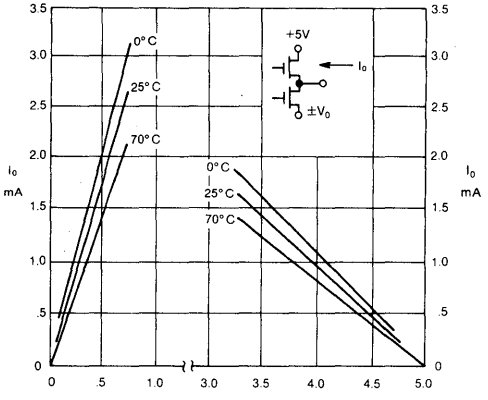
		ER2055			ER2055 IR/ER2055 HR				
Characteristics	**Sym**	**Min.**	**Typ.****	**Max.**	**Min.**	**Typ.****	**Max.**	**Units**	**Conditions**
DC CHARACTERISTICS									
Input Logic "1"	V_{IH}	$V_{SS}-1.5$	—	$V_{SS}+0.3$	$V_{SS}-1.5$	—	$V_{SS}+0.3$	V	
Input Logic "0"	V_{IL}	$V_{SS}-15$	—	0.8	$V_{SS}-10$	—	0.6	V	
Output Logic "1"	V_{OH}	$V_{SS}-1.5$	—	—	$V_{SS}-1.5$	—	—	V	$I_{OH} = 100\mu A$
Output Logic "0"	V_{OL}	—	—	0.6	—	—	0.6	V	$I_{OL} = 1.6mA$ for $V_{SS} = 5V$
Input Leakage	I_L	—	2	10	—	2	10	μA	$V_{IN} = V_{SS}-15$
Output Leakage	I_O	—	2	10	—	2	10	μA	Chip deselected
Power Supply Current									
Read	I_{GG}	—	8	10	—	8	18	mA	I_{SS} approx I_{GG}
Write	I_{GG}	—	6	7	—	6	9	mA	I_{SS} approx I_{GG}
Erase	I_{GG}	—	4	7	—	6	8	mA	I_{SS} approx I_{GG}
Deselected	I_{GG}	—	4	7	—	4	6	mA	I_{SS} approx I_{GG}
AC CHARACTERISTICS									
Access Time	t_{ACC}	—	—	2	—	—	4	μs	
Clock Pulse Width	t_{PW}	2	—	20	2	—	20	μs	
Erase Cycle Time	t_E	50	—	200	100	—	200	ms	
Write Cycle Time	t_W	50	—	200	100	—	200	ms	
Read Cycle Time	t_R	5	—	24	6	—	25	μs	
Address to Clock Time	t_A	50	—	—	50	—	—	ns	
Data Set Up Time	t_{DS}	50	—	—	50	—	—	ns	
Data Hold Time	t_{DH}	50	—	—	50	—	—	ns	
Control to Address & Data Change	t_C	0	—	—	0	—	—	ns	
Number of Reads/Word Refresh	N_{RA}	10^{11}	—	—	10^{11}	—	—		
Number of Erase/Write Cycles	N_W	10^6	—	—	10^5	—	—	—	
Input Capacitance (All Pins)	C_{IO}	—	6	10	—	6	10	pf	
Unpowered Data Storage Time	t_S	10	—	—	1	—	—	Years	at max temperature
Power Dissipation Read Cycle	P_D	—	450	500	—	450	500	mW	at 25°C $V_{SS} = +5$, $V_{GG} = -29$
	P_D	not applicable			—	—	500	mW	at 125°C $V_{SS} = +5$, $V_{GG} = -29$
	P_D	not applicable			—	—	600	mW	at −55°C $V_{SS} = +5$, $V_{GG} = -29$
Pulse Rise, Fall Time	t_{R1} t_F	10	—	100	10	—	100	ns	

**Typical values are at +25°C and nominal voltages.

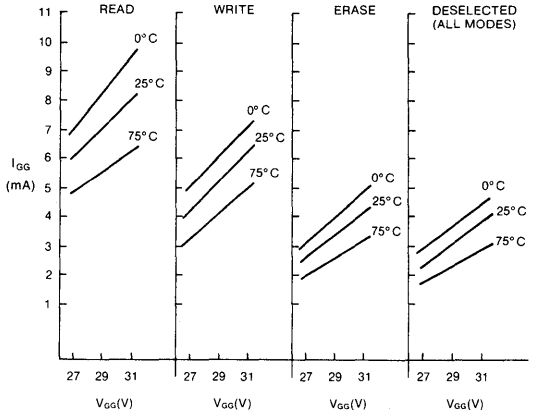
TIMING DIAGRAM



TYPICAL OUTPUT CHARACTERISTICS



TYPICAL SUPPLY CURRENT VS POWER SUPPLY VOLTAGE



GENERAL INSTRUMENT

ER5901
ER5901IR
ER5901HR

PRELIMINARY INFORMATION

Word Alterable 1K Bit Electrically Erasable Programable ROM

FEATURES

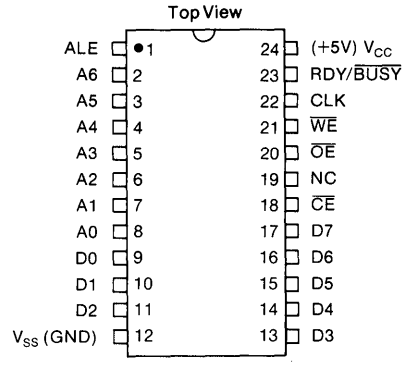
- 1024 Bits, Organized 128 x 8
- N-Channel Si-Gate SNOS Technology
- +5V Operation in All Modes; No High Voltages
- Fully TTL Compatible Inputs and Outputs
- On-Chip Latching of Addresses and Data
- Self-Timing, Processor Transparent Programing Mode with RDY/$\overline{\text{BUSY}}$ Signal
- Address and Data Buses may be used Separately or Multiplexed
- $\overline{\text{CE}}$ and $\overline{\text{OE}}$ Inputs to Avoid Bus Contention
- Word Alterable
- Read Access time of Less Than 200ns
- 10 Years' Data Retention over Temperature Range of −40° to +85°C
- Unlimited Read Accesses

DESCRIPTION

The ER5901 is a high speed electrically word erasable memory manufactured in the General Instrument proven SNOS technology. The key features of this device are its +5V only operation and microprocessor compatible architecture which allows the ER5901 to be accessed from the system bus in the same way as a static RAM.

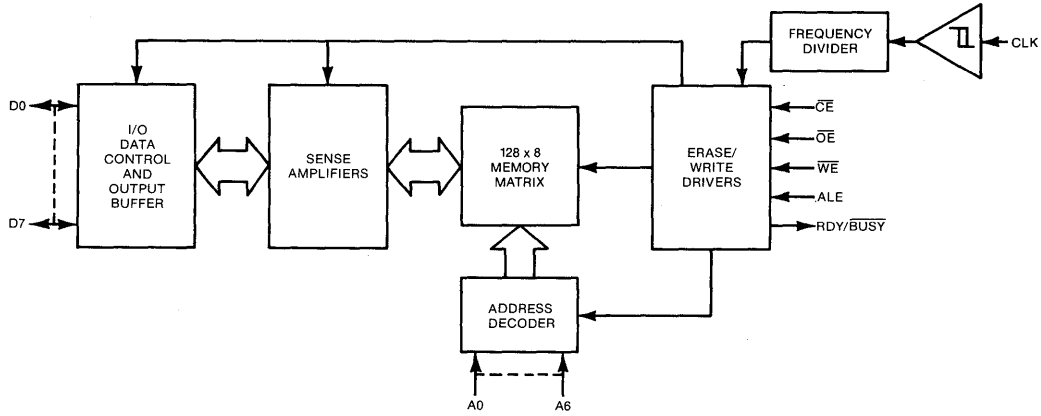
Internal memory management has been incorporated in this device. On-board latching of address and data lines in the reprograming mode, and busy signal (RDY/$\overline{\text{BUSY}}$) output make this mode transparent to the host processor.

PIN CONFIGURATION
24 LEAD DUAL IN LINE



NC = No Internal Connection

BLOCK DIAGRAM



An ADDRESS LATCH ENABLE (ALE) input is provided so that memory may be used with a multiplexed address and data bus. When this feature is not required, ALE may be tied to $\overline{WE}$.

Bus contention problems are minimized by twin line control provided by CHIP ENABLE ($\overline{CE}$) and OUTPUT ENABLE ($\overline{OE}$).

By virtue of the on-chip reprograming control and timing of the ER5901, a minimum amount of servicing is required from a host microprocessor or microcomputer.

The user may select one of five operating modes:

1. READ with separate address and data lines.
2. READ with multiplexed address and data lines.
3. PROGRAM with separate address and data lines.
4. PROGRAM with multiplexed address and data lines.
5. STANDBY — power consumption is reduced by 66%.

PIN FUNCTIONS

Symbol	Function	Comments
ALE	Address Latch Enable	Address inputs latched on negative edge. May be tied to $\overline{WE}$ when separate address and data lines are used.
A0-A6	7 bit address	
D0-D7	8 bit data I/O	
V_{SS}	Chip Ground connection	
$\overline{CE}$	Chip Enable input	Used for chip selection.
$\overline{OE}$	Output Enable input	Gates data to output pins during read cycle.
$\overline{WE}$	Write Enable input	Enables reprograming cycle; input data latched on positive edge.
CLK	Timing inputs	Defines clock frequency for reprograming. May be RC or external clock.
RDY/$\overline{BUSY}$	Status output	Low when chip is in reprograming mode and cannot be accessed. High when in read mode.
V_{CC}	+5 Volt power connection	

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs with respect to Ground ..... +6V to −0.3V
Storage temperature (unpowered and without data retention) ..... −65° C to +150° C
Soldering temperature of leads (10 secs.) ..... +300° C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted)

V_{SS} = GND
V_{CC} = +5V ±10% Volts
Operating Temperature Ranges T_A: 0° C to + 70° C (Commercial)
−40° C to +85° C (Industrial)
−55° C to +125° C (Military)

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Input Logic "1"	V_{IH}	2	—	V_{CC}+0.3	V	
Input Logic "0"	V_{IL}	−0.1	—	+0.8	V	
Output Logic "1"	V_{OH}	2.4	—	V_{CC}	V	I_{OH} = 400μA
Output Logic "0"	V_{OL}	—	—	0.4	V	I_{OL} = 1.6mA
Input Leakage Current	I_{IL}	—	—	10	μA	V_{IN} = 5.25V
Output Leakage Current	I_{OL}	—	—	10	μA	V_{OUT} = 5.25V
Power Supply Requirements						
V_{CC} Supply:						
Chip Selected	I_{CC}	—	35	80	mA	V_{CC} = +5.5V
Chip Deselected (Standby Mode)	I_{CC}	—	12	35	mA	V_{CC}= +5.5V
Power Dissipation:						
Chip Selected	P_D	—	195	300	mW	V_{CC} = +5.5V
Chip Deselected (Standby Mode)	P_D	—	66	100	mW	V_{CC} = +5.5V

AC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Input Capacitance	C_I	—	—	6	pf	V_{IN} = 0V
Output Capacitance	C_O	—	—	10	pf	V_{OUT} = 0V

MEMORY CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Erased State	V_E	—	V_{IH}, V_{OH}	—	V	
Written State	V_W	—	V_{IL}, V_{OL}	—	V	
Data Retention Time (Powered or Unpowered)	t_S	10	—	—	Years	
Number of Reprograming Cycles per Byte	N_P	10^4	—	—	—	See Note
Number of Read Accesses Between Refresh	N_{RA}	Unlimited				

NOTE:
There is a tradeoff to be made between the data retention time (t_S) and the number of reprograming cycles (N_P) performed per address. A gradual logarithmic reduction in retention time is experienced as the number of reprograming cycles increases. The specified limit is merely one point on this curve and does not imply a sudden cutoff or end of life. After 10^4 cycles a typical retention time is 10 years.

MODE SELECTION: Multiplexed Address and Data Lines

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$[1]	ALE[2]	RDY/$\overline{BUSY}$
Standby	V_{IH}	Don't Care	Don't Care	Don't Care	V_{OH}
Read	V_{IL}	V_{IL}[3]	V_{IH}	⎍	V_{OH}
Program	V_{IL}	V_{IH}	⎍	⎍	V_{OL}

MODE SELECTION: Separate Address and Data Lines

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$/ALE[1, 2, 4]	RDY/$\overline{BUSY}$
Standby	V_{IH}	Don't Care	Don't Care	V_{OH}
Read	V_{IL}	V_{IL}	V_{IH}	V_{OH}
Program	V_{IL}	V_{IH}	⎍	V_{OL}

NOTES:
1. Data inputs latched on rising edge of $\overline{WE}$.
2. Address inputs latched on falling edge of ALE.
3. To avoid bus contention $\overline{OE}$ must be strobed when the device is used in the multiplexed mode.
4. $\overline{WE}$ and ALE inputs may be tied together when the device is used in the non-multiplexed mode.

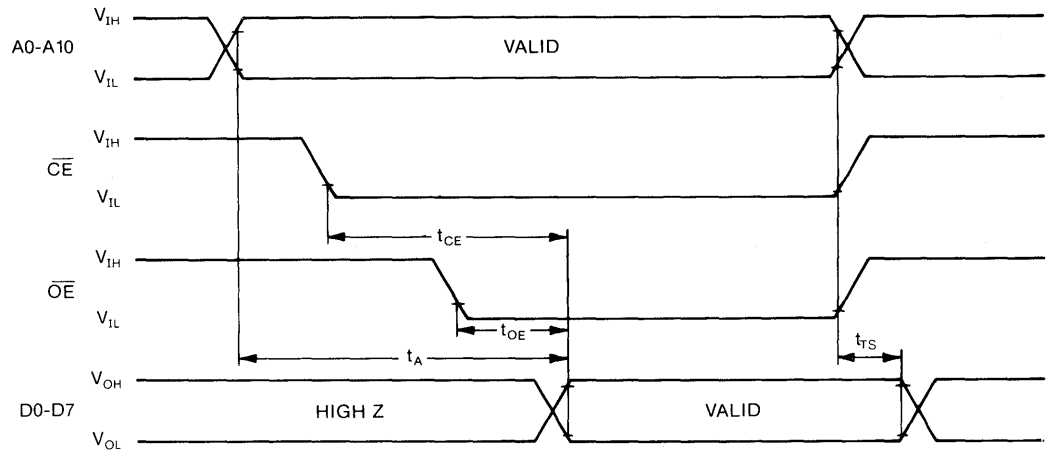


Fig. 1 READ MODE WITH SEPARATE ADDRESS AND DATA LINES

READ OPERATION (With Separate Address and Data Lines)

To initiate a read cycle a valid address must appear on the A_0 to A_6 inputs and remain there for the duration of the cycle because the address is not latched in this mode. $\overline{CE}$ may then be brought low to select the device. The desired memory byte will be in internal registers a short time later and will appear on data lines D_0 to D_7 after a time delay (t_{OE}) measured from the falling edge of $\overline{OE}$. Alternatively, if bus contention is not a problem, $\overline{OE}$ may be tied low. The maximum read access time (t_A) is 200ns, and data will remain valid until a logic level change occurs on $\overline{CE}$, $\overline{OE}$, or an address line. In this mode of operation ALE and $\overline{WE}$ are held high and may be tied together. (See Figure 1.)

READ MODE (Separate Address and Data Lines)

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Access Time — Address to Output Delay	t_A	—	—	200	ns	Load = 1 TTL gate + C_L = 100pf $\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	—	200	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	10	—	150	ns	$\overline{CE}$ = V_{IL}
Address — $\overline{CE}$ or $\overline{OE}$ to Output Tri-State	t_{TS}	10	—	75	ns	

RELATED APPLICATION NOTES

1223 New EEPROM Removes Separate Write/Erase Necessity

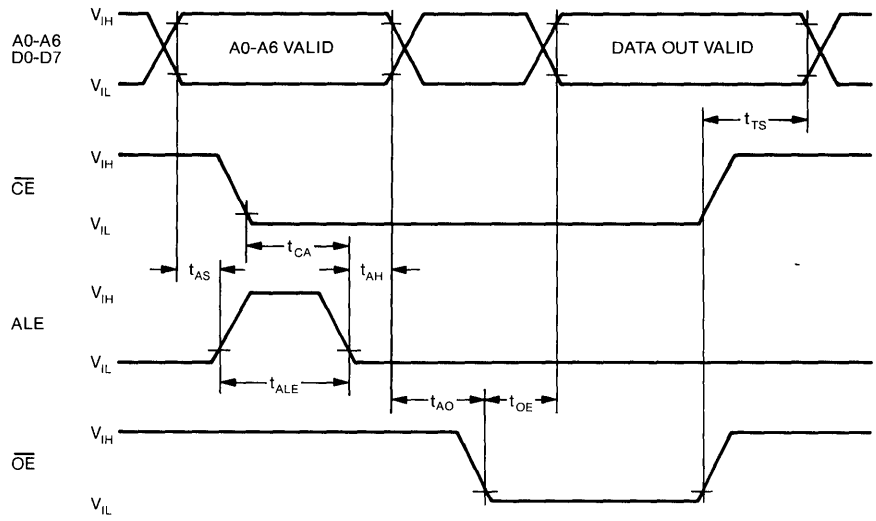


Fig. 2 READ MODE WITH MULTIPLEXED ADDRESS AND DATA LINES

READ OPERATION (With Multiplexed Address and Data Lines)

The ALE line is pulsed high, while a valid address is presented to the A_0 to A_6 inputs of a selected device. The address is latched into the ER5901 on the falling edge of ALE and, in order to avoid bus contention, these lines should be tri-stated prior to pulsing $\overline{OE}$ low. After a delay (t_{OE}), the selected byte will appear on lines D_0 to D_7 until either $\overline{OE}$ or $\overline{CE}$ goes high. (See Figure 2.)

READ MODE (Multiplexed Address and Data Lines)

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address Setup Time	t_{AS}	10	—	—	ns	
Chip Enable to Address Latch Enable	t_{CA}	100	—	—	ns	
ALE Pulse Width	t_{ALE}	100	—	—	ns	
Address Hold Time	t_{AH}	40	—	—	ns	
Address Float to Output Enable	t_{AO}	20	—	—	ns	
$\overline{OE}$ to Output Delay	t_{OE}	10	—	150	ns	$\overline{CE} = V_{IL}$
Address — $\overline{CE}$ or $\overline{OE}$ to Output Tri-State	t_{TS}	10	—	75	ns	

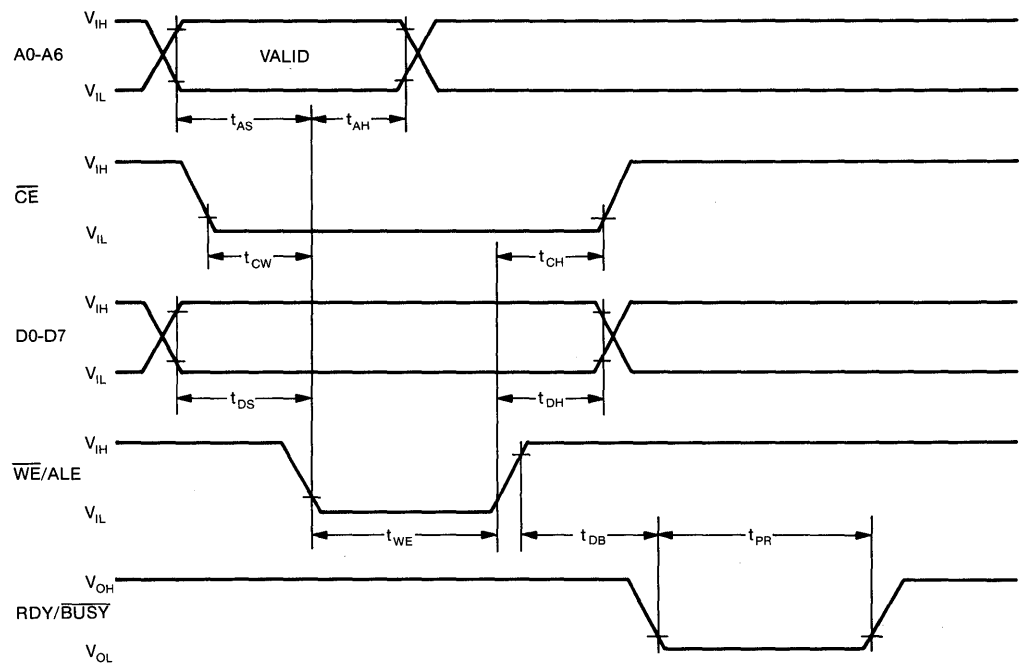


Fig. 3 PROGRAM MODE WITH SEPARATE ADDRESS AND DATA LINES

PROGRAM MODE (With Separate Address and Data Lines)

In this mode the ALE and $\overline{WE}$ inputs may be tied together. With a stable address and data word presented to the respective inputs of a selected device, the $\overline{WE}$/ALE line is pulsed low to initiate a program cycle. The falling edge of $\overline{WE}$/ALE latches the address inputs and the rising edge latches the data inputs. After a delay (t_{DB}), the RDY/$\overline{BUSY}$ output will go low and remain low for the duration of the programing cycle. All inputs to the ER5901 are disabled during a programing cycle. (See Figure 3.)

PROGRAM MODE (Separate Address and Data Lines)

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address Setup Time	t_{AS}	50	—	—	ns	
Chip Enable to Write Enable Delay	t_{CW}	100	—	—	ns	
Data Setup Time	t_{DS}	0	—	—	ns	
Address Hold Time	t_{AH}	40	—	—	ns	
Write Enable Pulse Width	t_{WE}	0.1	—	10	μs	
Data Hold Time	t_{DH}	40	—	—	ns	
$\overline{WE}$ to $\overline{CE}$ Delay	t_{CH}	0	—	—	ns	
Status Delay	t_{DB}	10	—	150	ns	
Status Low Time (Programing Time)	t_{PR}	20	—	100	ms	With min clock freq as defined by TI input
Program Clock Frequency	f_{PR}	10	—	50	KHz	

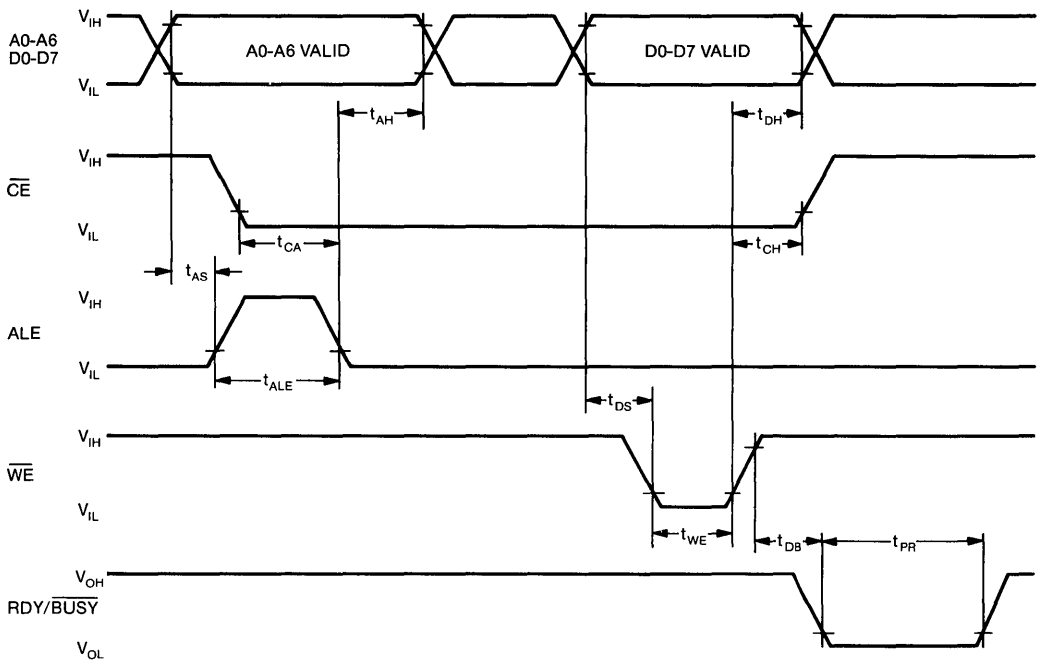


Fig. 4 PROGRAM MODE WITH MULTIPLEXED ADDRESS AND DATA LINE

PROGRAM MODE (With Multiplexed Address and Data Lines)

The ALE line is pulsed high while the address to be altered is presented to lines A_0 to A_6 of the selected device. The fall of ALE latches the address into the ER5901, and the information on the bus line is then changed to the data to be written into the EEPROM. $\overline{WE}$ is pulsed low and the data is latched on its rising edge. After a delay (t_{DB}), the RDY/$\overline{BUSY}$ output will go low for the duration of the programing cycle. (See Figure 4.)

PROGRAM MODE (Multiplexed Address and Data Lines)

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address Setup Time	t_{AS}	10	—	—	ns	
Chip Enable to Address Latch Enable	t_{CA}	100	—	—	ns	
ALE Pulse Width	t_{ALE}	100	—	—	ns	
Address Hold Time	t_{AH}	40	—	—	ns	
Data Setup Time	t_{DS}	10	—	—	ns	
$\overline{WE}$ Pulse Width	t_{WE}	0.1	—	10	μs	
Data Hold Time	t_{DH}	40	—	—	ns	
$\overline{WE}$ to $\overline{CE}$ Delay	t_{CH}	0	—	—	ns	
Status Delay	t_{STA}	10	—	150	ns	
Status Low Time (Programing Time)	t_{PR}	20	—	100	ms	With min clock freq as defined by TI input
Program Clock Frequency	f_{PR}	10	—	50	KHz	

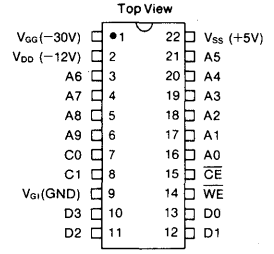
4096 Bit Electrically Alterable Read Only Memory

FEATURES

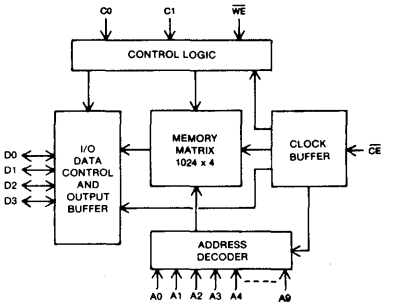
- 1024 Word x 4 Bit Organization
- Latched Address and Data Inputs
- Word or Block Alterable
- 10 Year Data Storage for ER3400
- 1 Year Data Storage for ER3400IR at +85° C and ER3400HR at +95° C
- TTL Compatible with Pull-Up Resistors on Inputs
- Tri-State Outputs
- Read Access Time: 900ns max
- Write Time: 1ms Erase Time: 10ms
- 10^9 Read Cycles/Word Between Refreshes
- 10^7 Read Cycles/Word for ER3400IR and ER3400HR
- Two Extended Temperature Ranges

PIN CONFIGURATION

22 LEAD DUAL IN LINE



BLOCK DIAGRAM



DESCRIPTION

The ER3400 is a 1024 x 4 bit fully decoded Electrically Alterable Read Only Memory fabricated in the General Instrument proven MNOS technology. Address, control and data inputs are latched on board the device thus releasing these lines during Erase and Write operations. Selection of one of the four modes of operation is made by setting the appropriate binary code on control lines C0 and C1. $\overline{CE}$ is used for chip selection and latching of address and control lines. $\overline{WE}$ is used to sample and latch input data on D0-D3 during a Write operation.

Power sequencing protection circuitry is provided on the ER3400 to protect against the accidental alteration of data during power Up/Down. However, due to the unpredictable nature of power up and power down sequences in some systems, it is important to apply and remove the programing voltage V_{GG} only when V_{SS} and V_{DD} are within their specified limits.

For applications requiring extended temperature ranges the ER3400I, ER3400IR and ER3400HR are available.

RELATED APPLICATION NOTES

1217	The ER3400: an easy to use 4K EAROM
1218	Interfacing the ER3400 to an eight bit microcomputer
1220	Generating EAROM programming voltages from a 5 volt supply
1210	Data retention testing of the ER3400

PIN FUNCTIONS

Name	Function
A0-A9	10-Bit Word Address
D0-D3	Data input and output pins
$\overline{CE}$	Chip Enable. Chip selected when $\overline{CE}$ is pulsed to logic "0".
C0, C1	Mode Control Inputs C0 C1 0 1 Block Erase Mode: erase operation performed on all words. 1 1 Word Erase Mode: stored data is erased at addressed location. 0 0 Read Mode: addressed data read after leading edge of $\overline{CE}$ pulse. 1 0 Write Mode: input data written at addressed location.
$\overline{WE}$	Write Enable. Input data read when $\overline{WE}$ is pulsed to logic "0".
V_{SS}	Substrate supply. Normally at +5 volts.
V_{GI}	Ground Input
V_{DD}	Power Supply Input. Normally at -12 volts.
V_{GG}	Power Supply Input. Normally at -30 volts.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs except V_{GG} (with respect to V_{SS}) .... −20V to +0.3V
Storage temperature (without data retention) ..... −65° C to +150° C
Soldering temperature of leads (10 seconds) ..... +300° C

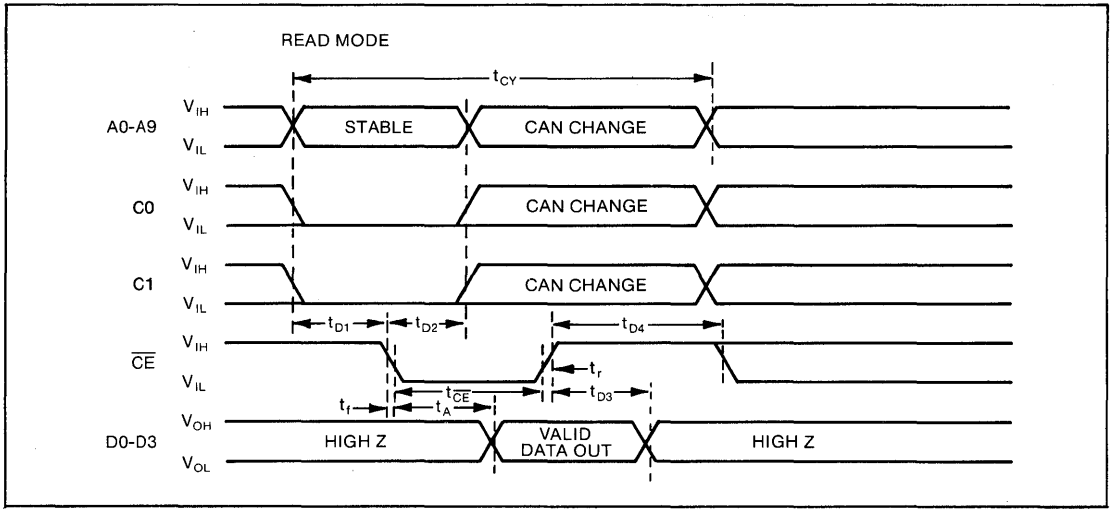
Standard Condition (unless otherwise noted)

V_{SS} = +5V to ±5%
V_{DD} = −12V ±5%
V_{GG} = −30V ±5%
V_{GI} = GND
Operating Temperature (T_A) = 0° C to +70° C (ER3400)
−40° C to +85° C (ER3400I/IR)
−55° C to +95° C (ER3400HR)

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

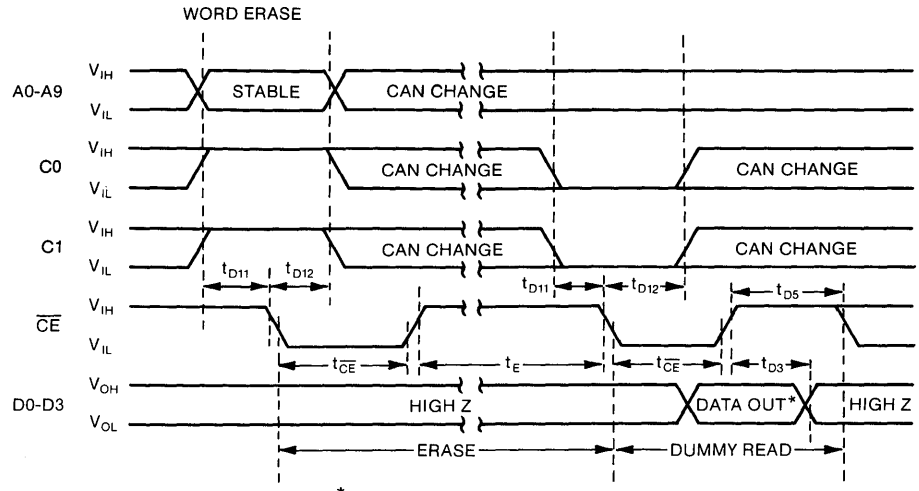
		ER3400			ER3400IR/ER3400HR				
Characteristic	**Sym**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
DC CHARACTERISTICS									
Input Logic "1"	V_{IH}	V_{SS} −1.5	—	V_{SS} +0.15	V_{SS} −1	—	V_{SS} +0.15	V	
Input Logic "0"	V_{IL}	−10	—	0.8	−10	—	0.6	V	
Output Logic "1"	V_{OH}	V_{SS} −1.5	—	—	V_{SS} −1.5	—	—	V	I_{OH} = 2mA
Output Logic "0"	V_{OL}	—	—	0.4	—	—	0.5	V	I_{OL} = 2mA
Control Input Leakage	I_{LC}	—	—	−2	—	—	−2	μA	V_{ON} = V_{SS} −15 Volts
Data Input Leakage	I_{LD}	—	—	−10	—	—	−10	μA	V_{IN} = V_{SS} −15 Volts
Power Supply Current									
V_{DD} Supply Current: Chip Selected	I_{DD}	—	—	−25	—	—	−30	mA	V_{DD} = V_{SS} −17 Volts
Chip De-Selected	I_{DD}	—	—	−12	—	—	−15	mA	V_{DD} = V_{SS} −17 Volts
V_{GG} Supply Current: Write Mode	I_{GG}	—	—	−4	—	—	−5	mA	V_{GG} = V_{SS} −35 Volts
V_{SS} Supply Current: Chip Selected	I_{SS}	—	—	−31	—	—	−37	mA	V_{GG} = V_{SS} −17V, V_{GG} = V_{SS} −35V
Chip De-Selected	I_{SS}	—	—	−14.5	—	—	−18	mA	V_{GG} = V_{SS} −17V, V_{GG} = V_{SS} −35V
AC CHARACTERISTICS									
Input Capacitance—Control Inputs	C_I	—	6	8	—	6	8	pf	
Input Capacitance—Data Inputs	C_D	—	8	10	—	8	10	pf	



Characteristics	Sym	ER3400 Min	ER3400 Max	ER3400IR/HR Min	ER3400IR/HR Max	Unit	Conditions
Read Cycle Time	t_{CY}	1700	—	1750	—	ns	
Address and Control to $\overline{CE}$	t_{D1}	100	—	100	—	ns	
Address and Control Hold Time	t_{D2}	250	—	350	—	ns	
$\overline{CE}$ Rise to Data Tri-State	t_{D3}	50	300	50	350	ns	
$\overline{CE}$ High	t_{D4}	700	—	750	—	ns	
Access Time	t_A	—	900	—	1000	ns	Load = 2K + 100pf to V_{SS}
$\overline{CE}$ Pulse Width	$t_{\overline{CE}}$	1	50	1	50	μs	
$\overline{CE}$ Rise, Fall Time	t_r, t_f	10	100	10	100	ns	
Number of Read Accesses per Location Between Refresh	N_{RA}	10^9	—	10^7	—	—	

READ OPERATION

Address and control line inputs are latched on the falling edge of $\overline{CE}$. With control lines C0 and C1 both low a read cycle will be initiated. After the access time (t_A) the data read will be output on data lines D0-D3. $\overline{CE}$ must be held high for a minimum of 700ns between memory read cycles. To reduce power consumption the ER3400 may be operated with V_{GG} held at V_{SS} in the read mode.



*Data output during a Dummy Read is not valid.

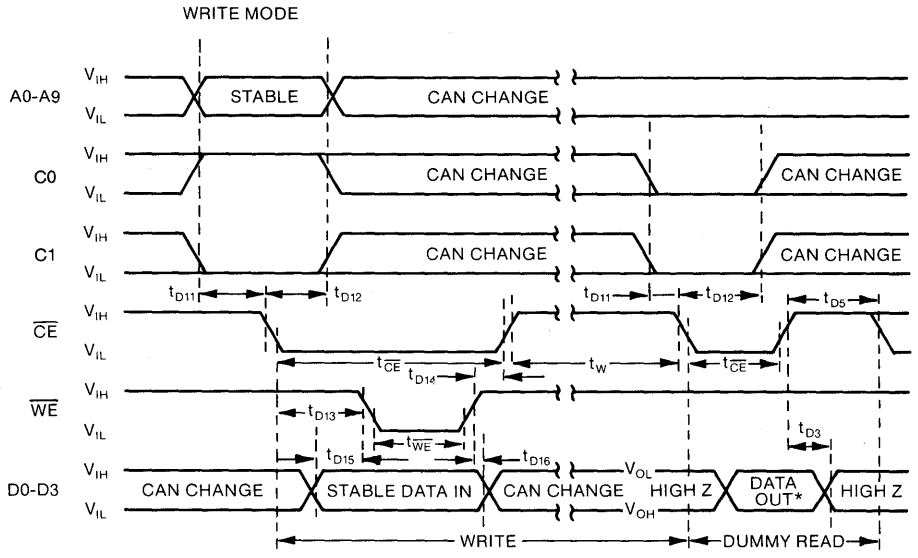
Characteristics	Sym	ER3400 Min	ER3400 Max	ER3400IR/HR Min	ER3400IR/HR Max	Unit	Conditions
Address and Control to $\overline{CE}$	t_{D11}	100	—	100	—	ns	
Address and Control Hold Time	t_{D12}	250	—	250	—	ns	
$\overline{CE}$ Rise to Data Tri-state	t_{D3}	50	300	50	350	ns	
$\overline{CE}$ High (Dummy Read)	t_{D5}	1500	—	1500	—	ns	
$\overline{CE}$ Pulse Width	$t_{\overline{CE}}$	1	50	1	50	μs	
Erase Time	t_E	10	20	10	20	ms	

WORD ERASE OPERATION

An erase cycle is required prior to a write in order to precondition the memory cells to be written. A word erase operation erases only the four bits of the addressed memory location. The falling edge of $\overline{CE}$ latches the control inputs and the address of the word to be erased. The rising edge of $\overline{CE}$ in the erase mode signals the start of the erase cycle which produces a positive shift in the threshold of the selected MNOS memory transistors. An erase operation must be terminated by a dummy read operation. The dummy read need not occur on the same location as the preceding erase, therefore, the state of the address lines A0-A9 are immaterial during the dummy read cycle. Data output during a dummy read cycle is not valid data.

BLOCK ERASE OPERATION

A block erase operation erases all 4096 bits of memory to the "1" state, in all other respects the operation is identical to the word erase operation described above.



*Data output during a Dummy Read is not valid.

Characteristics	Sym	ER3400 Min	ER3400 Max	ER3400IR/HR Min	ER3400IR/HR Max	Unit	Conditions
Address and Control to $\overline{CE}$	t_{D11}	100	—	100	—	ns	
Address and Control Hold Time	t_{D12}	250	—	350	—	ns	
$\overline{CE}$ Fall to $\overline{WE}$ Fall Delay	t_{D13}	0	—	0	—	ns	$\overline{WE}$ rise may overlap $\overline{CE}$
$\overline{WE}$ Rise to $\overline{CE}$ Rise Delay	t_{D14}	−50	—	−100	—	ns	rise by 50ns max
Data Stable to $\overline{WE}$	t_{D15}	0	—	0	—	ns	
$\overline{WE}$ Rise to End of Data Stable	t_{D16}	100	—	100	—	ns	
$\overline{CE}$ Pulse Width	$t_{\overline{CE}}$	1	50	1	50	μs	
$\overline{WE}$ Pulse Width	$t_{\overline{WE}}$	500	—	650	—	ns	
Write Time	t_W	1	2	1	2	ms	
$\overline{CE}$ Rise to Data Tri-State	t_{D3}	50	300	50	350	ns	
$\overline{CE}$ High (Dummy Read)	t_{D5}	1500	—	1500	—	ns	
Unpowered Data Storage Time	t_S	10	—	1	—	Years	See Note 1
Number of Reprogramming Cycles	N_W	10^3	—	10^3	—	—	See Note 1
Number of Read Accesses/Location between Refresh	N_{RA}	10^9	—	10^9	—	—	

NOTE 1: Does not imply end of useful life. See Write Operation for further information.

WRITE OPERATION

Control lines C0 and C1 along with address lines A0-A9 are latched on the falling edge of $\overline{CE}$. Input data on D0-D3 is latched on the rising edge of $\overline{WE}$. $\overline{WE}$ may be tied to $\overline{CE}$ for all operations, however, this separate latching allows the ER3400 to be used in certain systems where address and data busses are multiplexed. The writing of the selected memory transistors is initiated by the rising edge of $\overline{CE}$. $\overline{CE}$ must remain high for the duration of the write time. A write operation can only be terminated by a dummy read. To avoid bus contention, the data lines must be tri-stated prior to initiating the dummy read cycle. The data output by a dummy read cycle is not valid data. The dummy read need not occur on the same location as the previous write, therefore, address line A0-A9 may be allowed to change during the dummy read cycle.

The specification of 10 years non-volatile data retention after a minimum of 10^3reprograming cycles is merely one point on the curve of retention versus reprograming cycles and does not imply a sudden cut-off or end of life. As the number of Erase/Write cycles per address increases, a gradual, logarithmic reduction in data retention capability occurs with 1 year of retention being a typical figure after 10^4 cycles.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs with respect to Ground ..... +6V to −0.3V
Storage temperature (unpowered and without data retention) ..... −65°C to +150°C
Soldering temperature of leads (10 secs.) ..... +300°C

Standard Conditions (unless otherwise noted)

V_{SS} = GND
V_{CC} = +5V ±10% Volts
Operating Temperature Ranges T_A: 0°C to + 70°C (Commercial)
−40°C to +85°C (Industrial)
−55°C to +125°C (Military)

* Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Input Logic "1"	V_{IH}	2	—	V_{CC}+0.3	V	
Input Logic "0"	V_{IL}	−0.1	—	+0.8	V	
Output Logic "1"	V_{OH}	2.4	—	V_{CC}	V	I_{OH} = 400μA
Output Logic "0"	V_{OL}	—	—	0.4	V	I_{OL} = 1.6mA
Input Leakage Current	I_{IL}	—	—	10	μA	V_{IN} = 5.25V
Output Leakage Current	I_{OL}	—	—	10	μA	V_{OUT} = 5.25V
Power Supply Requirements						
V_{CC} Supply:						
Chip Selected	I_{CC}	—	40	90	mA	V_{CC} = +5.5V
Chip Deselected (Standby Mode)	I_{CC}	—	15	25	mA	V_{CC}= +5.5V
Power Dissipation:						
Chip Selected	P_D	—	200	450	mW	V_{CC} = +5.5V
Chip Deselected (Standby Mode	P_D	—	75	125	mW	V_{CC} = +5.5V

AC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Input Capacitance	C_I	—	4	6	pf	V_{IN} = 0V
Output Capacitance	C_O	—	—	10	pf	V_{OUT} = 0V

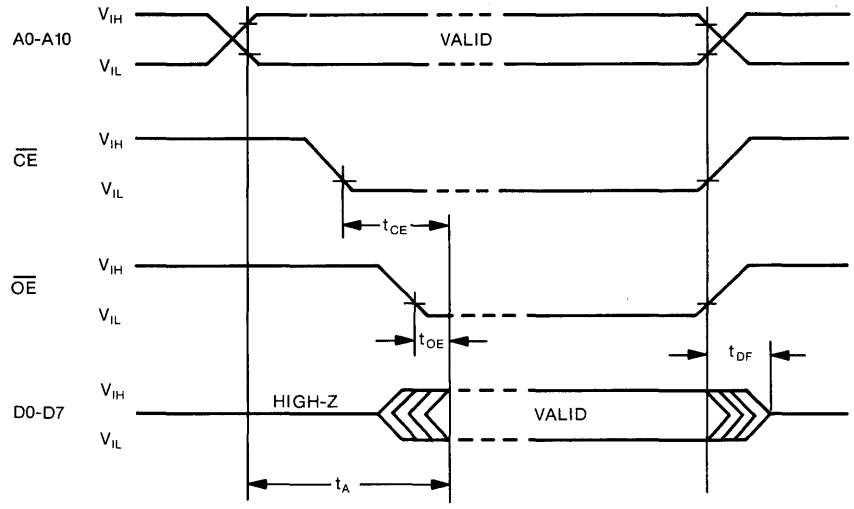


Fig. 1 READ MODE

READ OPERATION

The ER5916A and ER5916B have a two line control architecture to eliminate bus contention. They can be read within the device selection time, using the processor $\overline{RD}$ signal connected to $\overline{OE}$. To initiate a read cycle, a valid address must appear on the A_0 to A_{10} inputs. The address is latched on the falling edge of $\overline{CE}$ and the desired memory byte will be in internal register a short time (t_{CE}) later. $\overline{OE}$ must be brought low to transfer the data bits from the internal register to the data output lines D_0 to D_7. Alternatively, if bus contention is not a problem, $\overline{OE}$ may be tied low.

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address to Output Delay	t_A	—	200	250	ns	Output Load: 1 TTL gate + C_L = 100pf
CE to Output Delay	t_{CE}	—	200	250	ns	
Output Enable to Output Delay	t_{OE}	10	50	75	ns	
Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	t_{DF}	20	—	100	ns	

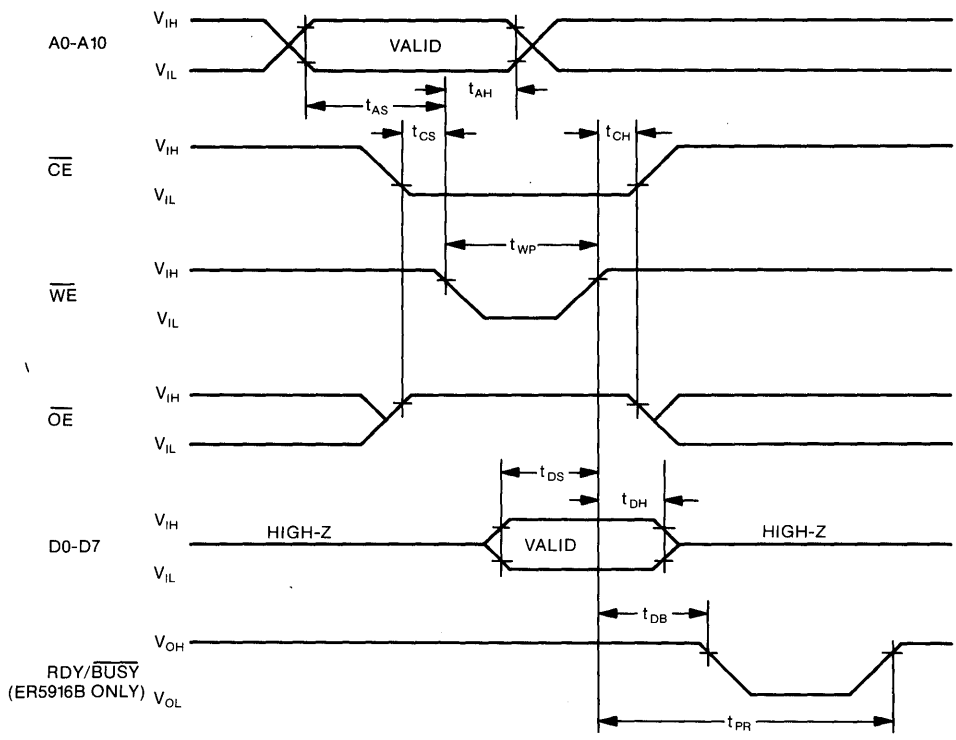


Fig. 2 PROGRAM MODE

PROGRAM MODE

No external latching, pre-erasing, or clock timing is needed. With a stable address and data word presented to the respective inputs of a selected device, the $\overline{WE}$ line is pulsed low to initiate a programing cycle, which consists of an automatic 5ms (typ) erase followed by a 5ms (typ) write. $\overline{OE}$ must be held high concurrent with the falling and rising edges of $\overline{WE}$. The falling edge of $\overline{WE}$ latches the address inputs and the rising edge latches the data inputs. After a delay (t_{DB}), the RDY/$\overline{BUSY}$ output will go low and remain low for the duration of the programing cycle (t_{PR}), indicating to the external processor that the ER5916B has entered the BUSY mode; all inputs are disabled when the RDY/$\overline{BUSY}$ line is low. The ER5916A operates in an identical manner, and a time (t_{PR}) must elapse before the beginning of another program, read, or block erase cycle. The ER5916A and ER5916B have on-chip data verification to ensure successful byte programing. This is achieved by comparing the data written to the cell with the data latched on chip during the write request.

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address to Write Setup Time	t_{AS}	20	—	—	ns	
Address Hold Time	t_{AH}	50	—	—	ns	
$\overline{CE}$ to $\overline{WE}$ Setup Time	t_{CS}	20	—	—	ns	
$\overline{CE}$ Hold Time	t_{CH}	50	—	—	ns	
$\overline{WE}$ Pulse Width	t_{WP}	100	—	—	ns	
Data Setup Time	t_{DS}	50	—	—	ns	
Data Hold Time	t_{DH}	20	—	—	ns	
Time to Device Busy	t_{DB}	—	—	75	ns	
Internal Erase Time	—	—	5	37.5	ms	
Internal Write Time	—	—	5	37.5	ms	
Programing Time	t_{PR}	—	10	75	ms	

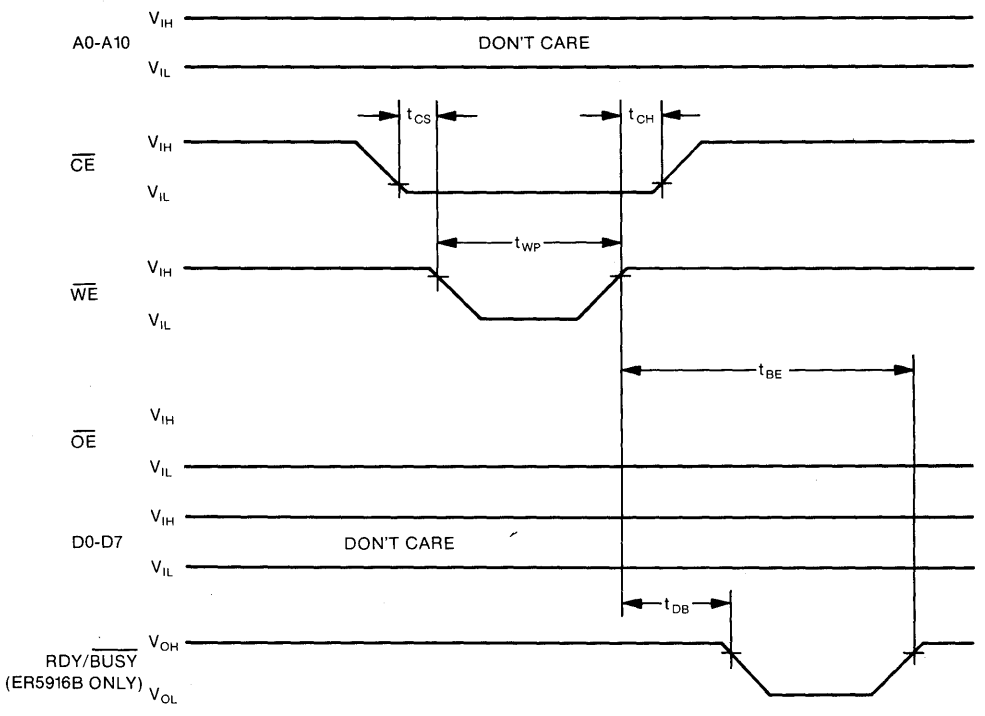


Fig. 3 BLOCK ERASE MODE

BLOCK ERASE OPERATION

No external latching or clock timing is needed. The $\overline{CE}$ and $\overline{WE}$ timing input requirements are identical to those required in the PROGRAM mode; $\overline{OE}$ must be held low. The RDY/$\overline{BUSY}$ line goes low for the duration of the internal 5ms (typ) block erase cycle, indicating to the host processor that the ER5916B has entered the BUSY mode. The ER5916A operates in an identical manner, and a time (t_{BE}) must elapse before the beginning of another program or read cycle.

Characteristics	Sym	Min	Typ	Max	Units	Conditions
$\overline{CE}$ to $\overline{WE}$ Setup Time	t_{CS}	20	—	—	ns	
$\overline{CE}$ Hold Time	t_{CH}	50	—	—	ns	
$\overline{WE}$ Pulse Width	t_{WP}	100	—	—	ns	
Time to Device Busy	t_{DB}	—	—	75	ns	
Block Erase Time	t_{BE}	—	5	37.5	ms	

4K N-Channel Non-Volatile Static RAM

FEATURES

- 512 x 8 Bit Organization, Fully Decoded RAM Overlaid Bit for Bit with Non-Volatile EEPROM
- Single +5V Power Supply
- 300ns RAM Cycle Time
- TTL Compatible
- Unlimited Data Recall
- 10^4 Store Cycles with 10 Year Data Retention
- Power Failure Protection

DESCRIPTION

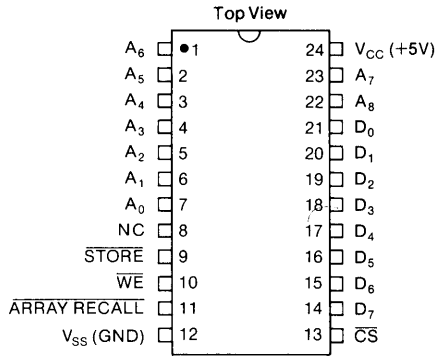
The ER5304 is a high speed non-volatile Si-Gate RAM. The device contains 4K bits of memory organized as a conventional 4K static RAM overlaid bit-for-bit with a non-volatile 4K Electrically Erasable ROM (EEPROM). The device can be used as a conventional static RAM while the non-volatile data stored in the EEPROM remains unaffected. Non-volatile data can be transferred back and forth between the RAM and the EEPROM by simple STORE and ARRAY RECALL signals. During the lifetime of the device, data can be recalled from the EEPROM an unlimited number of times.

A single 5V supply is the only power source ever required for any function. High voltage pulses or supplies are never required. All inputs and outputs are TTL compatible with Tri-state outputs. The device cycle time for both read and write is 300ns.

The device is capable of protecting against data loss due to a power failure. One simple TTL signal saves the entire RAM contents. A non-volatile copy of all RAM data is internally stored in the EEPROM and can be recalled to the RAM when power returns. No battery backup is required.

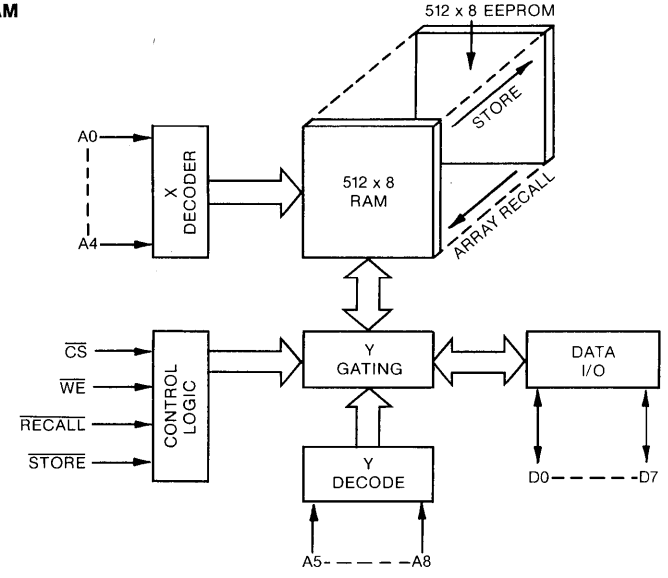
PIN CONFIGURATION

24 PIN DUAL IN LINE



NC = No connection for normal usage

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All Inputs and Outputs with Respect to Ground ..... −0.3 to +7V
Storage Temperature (without Data Retention) ..... −65°C to +150°C
Storage Temperature (with Data Retention) ..... −40°C to +85°C
Soldering Temperature of Leads (10 seconds) ..... +300°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated):

V_{SS} = GND
V_{CC} = 5 ± 5% Volts
Operating Temperature T_A = −40°C to +85°C

DC CHARACTERISTICS

Characteristics	Sym	Min	Max	Units	Conditions
Power Supply Current	I_{CC}	—	60	mA	All Inputs = 5.25V D_{OUT} Open T_A = 0°C
Output Leakage Current	I_{LO}	−1	+1	μA	V_{OUT} = GND to V_{CC}
Input Low Voltage	V_{IL}	−0.3	0.8	V	
Input High Voltage	V_{IH}	2	V_{CC}	V	
Output Low Voltage	V_{OL}	—	0.4	V	I_{OL} = 2.0mA
Output High Voltage	V_{OH}	2.4	—	V	I_{OH} = 1mA

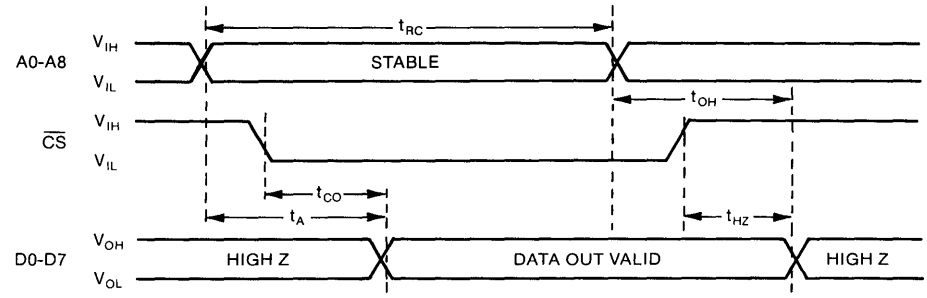
PIN FUNCTIONS

NAME	FUNCTION
A0-A8	Address Lines
D0-D7	Data I/O
CS	Chip Select
$\overline{WE}$	Write Enable
ARRAY RECALL	Transfers Data Stored in EEPROM Back to RAM
$\overline{STORE}$	Transfers Data from RAM into Non-Volatile EEPROM
V_{CC}	+5 Volts
GND	Ground

MODE \ PINS	$\overline{CS}$ (13)	$\overline{WE}$ (10)	$\overline{STORE}$ (9)	ARRAY $\overline{RECALL}$ (11)	DATA I/O (14-21)
Deselected (See Notes 1 & 2)	1	Don't Care			High Z
RAM Write	0	0	1	1	Data In
RAM Read	0	1	1	1	Data Out
EEPROM Store (See Note 2)	0	1	0	1	High Z
EEPROM Recall	0	1	1	0	High Z

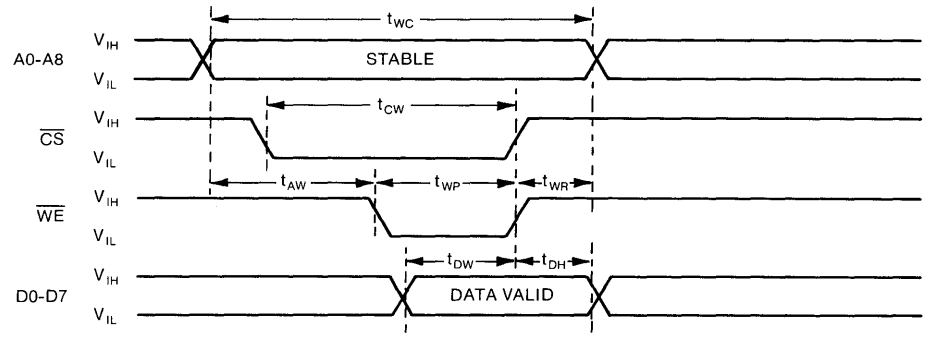
NOTES:
1. Chip is deselected but may be automatically completing a store cycle.
2. $\overline{CS}$ and $\overline{STORE}$ must be low only to initiate a store cycle, after which the cycle will continue to completion automatically ($\overline{CS}$, $\overline{STORE}$ = X).

READ CYCLE



Characteristics	Sym	Min	Typ	Max	Units	Conditions
Read Cycle Time	t_{RC}	300	—	—	ns	
Access Time	t_A	—	—	300	ns	
Chip Select to Output Valid	t_{CO}	—	—	200	ns	
Output Hold from Address Change	t_{OH}	50	—	—	ns	
Chip Deselect to Output in High Z	t_{HZ}	10	—	100	ns	

WRITE CYCLE



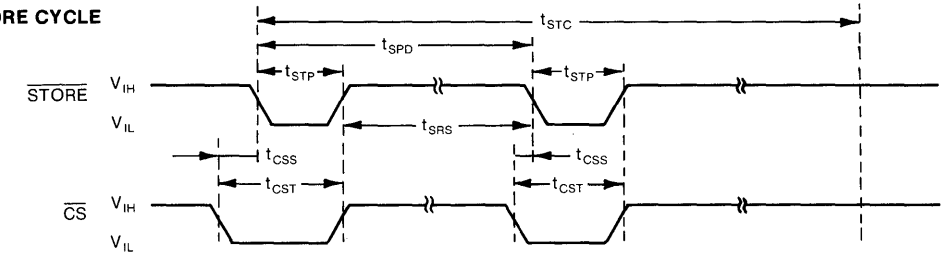
Parameter	Sym	Min	Typ	Max	Units	Conditions
Write Cycle Time	t_{WC}	300	—	—	ns	
Chip Select to End of Write	t_{CW}	150	—	—	ns	
Address to Write Set-up Time	t_{AW}	50	—	—	ns	
Write Pulse Width	t_{WP}	100	—	—	ns	
Write Recovery Time	t_{WR}	25	—	—	ns	
Data Valid to End of Write	t_{OW}	100	—	—	ns	
Data Hold Time	T_{OH}	20	—	—	ns	

In read and Write modes the device operates as a conventional static RAM. The device is selected with a logic "0" level applied to the $\overline{CS}$ pin. A logic "1" input on $\overline{WE}$ selects the Read mode, a logic "0" selects the Write mode. Address lines must remain stable for the duration of the Read or Write cycle. Data outputs are in the high impedance state whenever the Device is deselected or during a store or Array Recall Cycle.

A Store Cycle is initiated by applying two logic "0" level pulses to the $\overline{\text{STORE}}$ pin of a selected device. This causes all 4096 bits of data in the EEPROM to be modified to an exact copy of the current RAM data. The original data in the RAM remains valid. The $\overline{\text{WE}}$ and $\overline{\text{ARRAY RECALL}}$ inputs are inhibited during the store operation and the data outputs are Tri-stated. The inhibited inputs will be enabled upon completion of the Store Operation if the $\overline{\text{STORE}}$ input is high. Data stored in the EEPROM remains valid with or without power supplied to the ER5304.

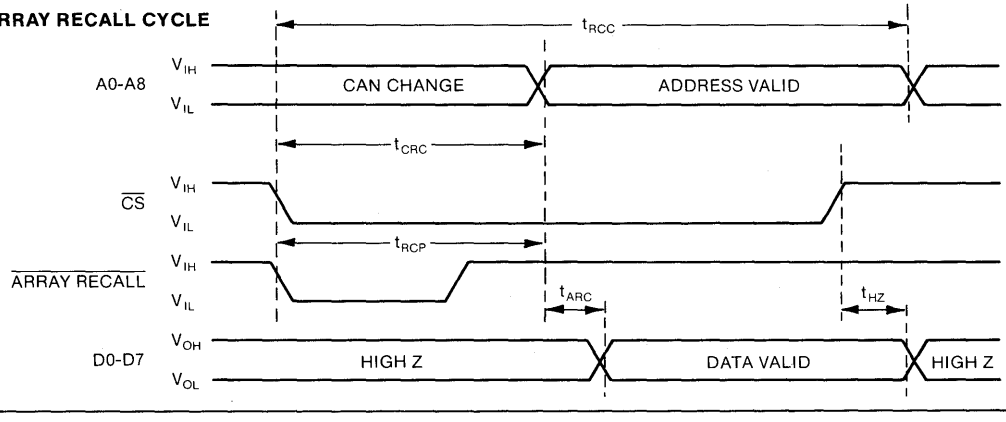
To prevent an unintentional Store Cycle during power-up or power-down either the $\overline{\text{STORE}}$ or $\overline{\text{CS}}$ input should be kept high by tying the input to V_{CC} through a pull up resistor.

STORE CYCLE



Characteristics	Sym	Min	Typ	Max	Units	Conditions
Store Cycle Time (t_{SPD} = 5ms)	t_{STC}	—	—	10	ms	
Store Pulse Width	t_{STP}	100	—	—	ns	
Chip Select to End of Store	t_{CST}	125	—	—	ns	
Chip Select to Store Set-up Time	t_{CSS}	25	—	—	ns	
Store Second Pulse Delay Time	t_{SPD}	5	—	—	ms	
Store Reset Time	t_{SRS}	300	—	—	ns	

ARRAY RECALL CYCLE



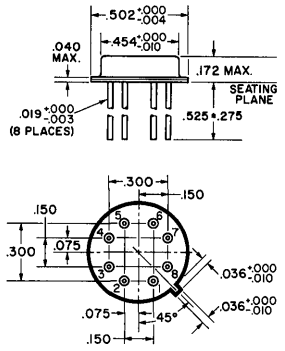
Characteristics	Sym	Min	Typ	Max	Units	Conditions
Array Recall Cycle Time	t_{RCC}	1500	1000	—	ns	
Chip Select to End of Recall	t_{CRC}	750	—	—	ns	
Recall Pulse Width	t_{RCP}	750	—	—	ns	
Chip Deselect to Output in High Z	t_{HZ}	10	—	100	ns	
Recalled Data Access Time from End of Recall	t_{ARC}	—	—	600	ns	

The Array Recall Cycle reads the non-volatile data stored in the EEPROM and copies it back into the RAM. A logic "0" on the $\overline{\text{ARRAY RECALL}}$ input of a selected device will initiate a cycle that in a single operation will overwrite all 4096 bits of data in the RAM with the data from the EEPROM. The data in the EEPROM remains unaltered. Once the EEPROM data is back in the RAM it can be accessed by normal RAM Read or Write cycles.

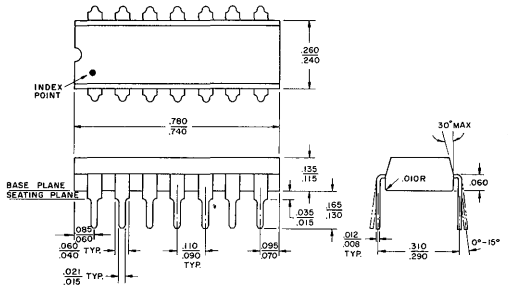
Data that has been stored properly in the non-volatile EEPROM of the ER5304 may be recalled an unlimited number of times during the lifetime of the device.

PACKAGE OUTLINES

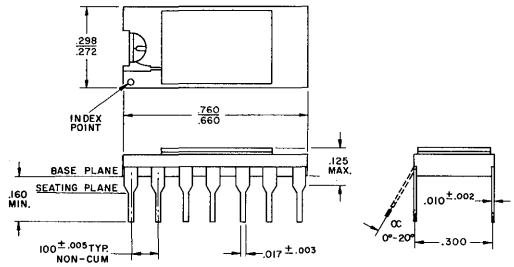
8 LEAD TO 8



14 LEAD DUAL IN LINE

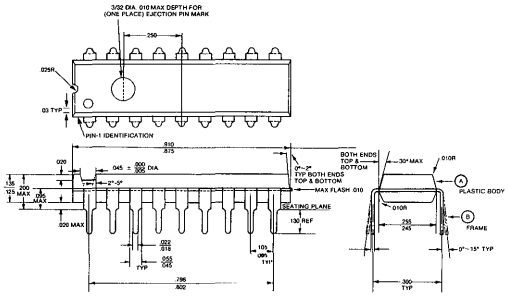


PLASTIC



CERAMIC

18 LEAD DUAL IN LINE



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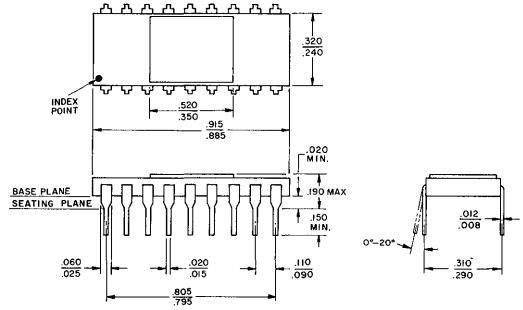

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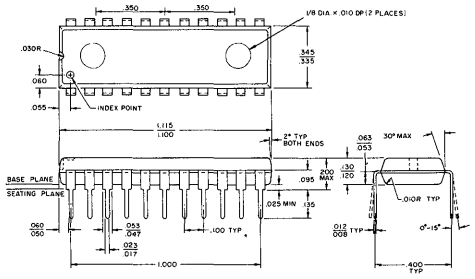
PACKAGE OUTLINES

22 LEAD DUAL IN LINE



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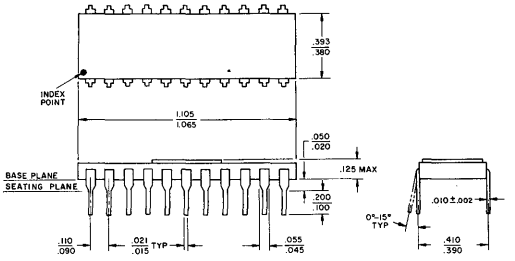

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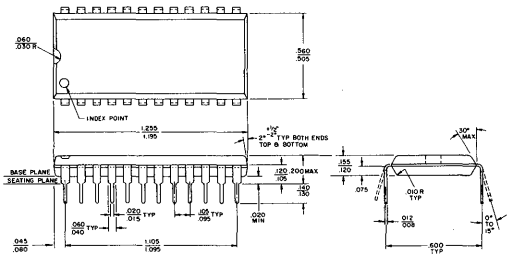

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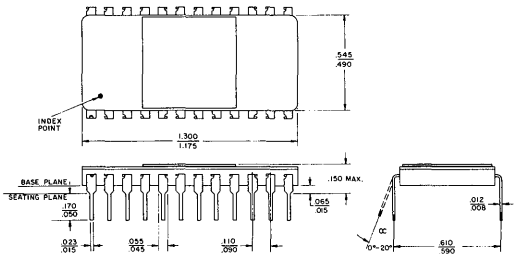

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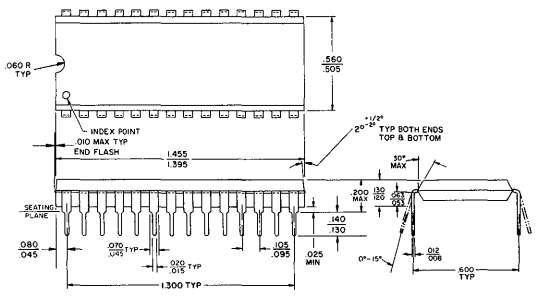
28 LEAD DUAL IN LINE



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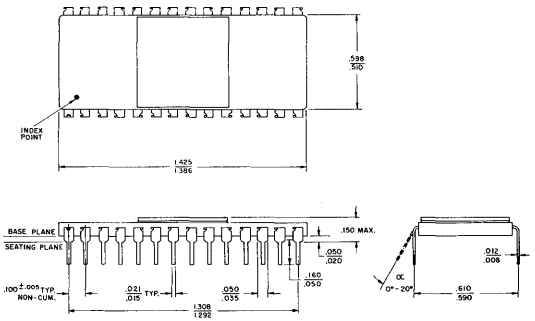

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APPLICATION NOTES

Note

EEPROMs and EAROMs are equivalent terms used to describe Electrically Alterable Non-Volatile Memories.

Bulletin 1215

EAROM — The Electrically Word Alterable Memory for Permanent Storage

Morton Kalet
Emyr Edwards

This application note is a reprint of the paper presented as part of the professional program of WESCON '80 in Anaheim, California — September, 1980. It presents a concise description of the MNOS technology, EAROM characteristics and some applications.

INTRODUCTION

In the area of non-volatile memory, currently available devices lend themselves well to different applications, but no one is ideally suited to all possible modes of use: Read Only Memories (ROM) require programming at the mask level during the manufacturing process and thereafter cannot be reprogrammed. Ultra Violet Erasable ROMs (EPROM) are difficult, costly and slow to reprogram while the new electrically reprogrammable ROMs (EEPROM), fabricated using floating gate technology, suffer from the drawback of having bulk erasing capabilities only.

A technology which has emerged as both mature and reliable is the Metal Nitride Oxide Semiconductor (MNOS) technology used in electrically alterable ROMs (EAROMs). EAROMs are non-volatile, electrically reprogrammable in-circuit and word alterable allowing random accessing and reprogramming of any memory location without affecting the data stored at adjacent locations. These properties have allowed EAROMs to be used in many applications where no other single device could have performed the same task.

MNOS TECHNOLOGY

The normal MOSFET gate dielectric consists of a layer of dielectric material (usually silicon dioxide), 750-1000Å in thickness isolating the metal gate from the silicon substrate. To allow conduction between the source and drain terminals of the MOSFET, a sufficiently large negative potential must be applied to the gate, relative to the source, to induce inversion of the surface of the N-type substrate under the gate. The P-Channel thus formed allows conduction between source and drain, the potential at which conduction begins being defined as the threshold voltage, V_t, of the transistor. Thus,

$|V_{GS}| < |V_t|$, $I_{DS} = 0$

$|V_{GS}| \geq |V_t|$, $I_{DS} = f(V_{GS}, V_{DS})$

The exact relationships between parameters have been detailed in the literature (see references 1, 2), but are not of immediate relevance here. P-Channel devices have negative V_ts and N-Channel positive.

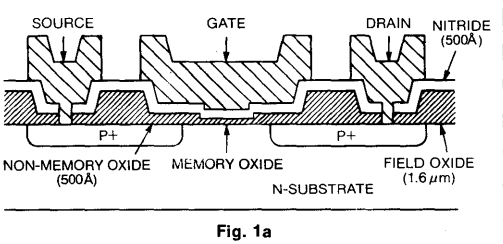

Fig. 1a

The gate structure of the device of Figure 1(a) has been modified to form a MNOS memory transistor in two ways:

1. the silicon dioxide layer has been replaced by a silicon nitride/silicon dioxide sandwich
2. the oxide of the center portion of the gate region has been thinned down to less than 100Å in thickness.

A useful schematic representation of this modified structure is the tri-gate model of Figure 1(b). The center transistor, numbered 2, exerts the controlling influence on the overall characteristics of the device. When used as a storage element, the threshold voltage of transistor 2 may be modified by tunneling a charge through its thin oxide layer to become stored in trap sites in the nitride.

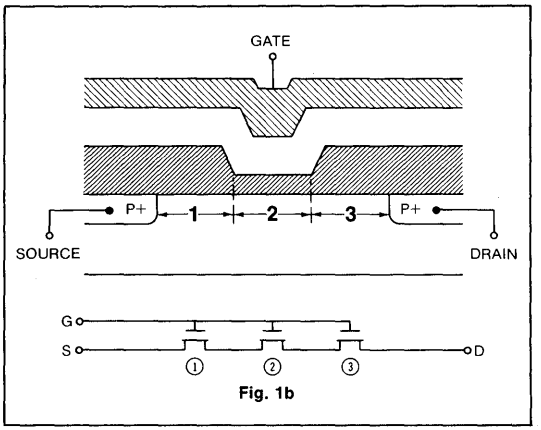

Fig. 1b

Erase Operation

On application of a large positive potential (+25V) to the gate of an MNOS transistor relative to its substrate, the tunneling phenomenon results in a net negative charge stored in the nitride trap centers which manifests itself as a shift in V_t of transistor 2 in the positive direction. Note that no change occurs in the thresholds of side transistors 1 and 3 since the oxide layers in these regions are too thick for charge tunneling to occur with the potential applied.

The erase operation described results in a V_t for transistor 2 of approximately +1V, which places it into the depletion or "normally-on" mode. In order that conduction occur between source and drain, the gate voltage applied must be sufficiently negative to turn on all three portions of the device. However, since the center portion is normally conducting, the effective V_t of an erased transistor, V_E, is that of devices 1 and 3; approximately −3V as indicated in Figure 1(c). Saturation of the nitride charge traps occurs after erase times in the range of 10-100ms depending on circuit implementation.

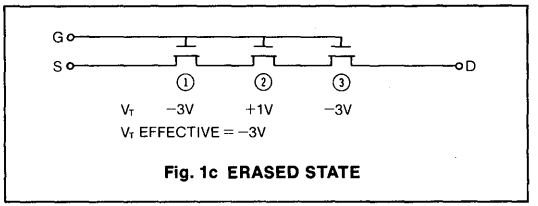

Fig. 1c ERASED STATE

Write Operation

Writing is the inverse of erasing. By reversing the polarity of the potential across the gate dielectric, a net positive charge is stored in the nitride with a correspondingly negative shift in V_t of transistor 2. The effective threshold will be that voltage (−12 to −14V) which will allow conduction through all three transistors (Figure 1(d)).

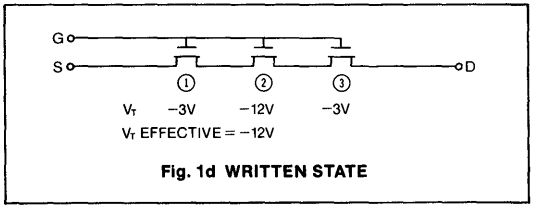

Fig. 1d WRITTEN STATE

Data storage in an MNOS memory is accomplished by designating the written transistor voltage (V_W) a binary 1 or 0, and the erased transistor voltage (V_E) the opposite state. For purposes of explanation, V_W is arbitrarily defined as a 1 and V_E as a 0. Write times for available devices are 1-100ms.

Read Operation

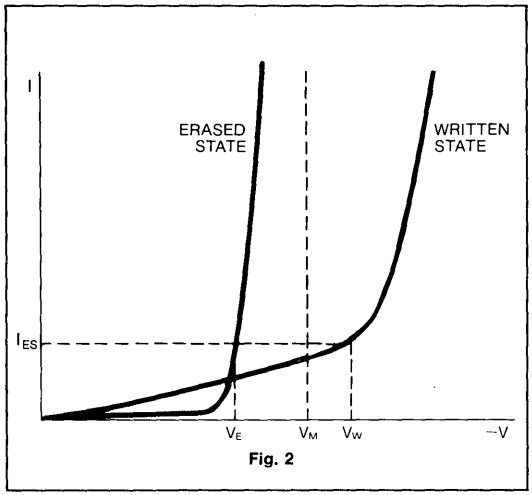

Fig. 2

Figure 2 represents graphically the I-V characteristics of the two states of a memory device, V_E and V_W. By applying, to the gate of a device, a reference voltage, V_M, set between V_E and V_W, its state may be determined by virtue of the fact that V_M will be sufficiently negative to overcome V_E, causing conduction in an erased transistor, but not negative enough to overcome V_W, leaving a written transistor in the off state. Therefore a stored '1' will present a high impedance to the sense amplifier and a stored '0' a low impedance.

MEMORY CHARACTERISTICS

Three parameters are peculiar to non-volatile memories and should be considered when characterizing their behavior. They are:

1. Retention—the length of time data may be stored.
2. Endurance—the effect on retention of erase/write cycling.
3. Read Disturb—the effect on retention of a large number of read cycles.

Of the three, retention and read disturb are non-destructive, whereas endurance has a cumulative, destructive effect, actually gradually destroying the ability of the nitride layer to hold charge.

1) Retention

Analogously to a very good capacitor, charge de-trapping in the non-conductive nitride occurs in an exponential manner with the result that the initial thresholds, V_E and V_W decay linearly against the log of time as shown in Figure 3.

The end of life point for the stored data is the point at which a '1', or written threshold, can no longer be distinguished from a '0' by the sense amplifier. It should be understood that once this point is reached, rewriting the data will restore the thresholds to the initial, t_O value and the decay curve will be repeated.

Different devices have different end of life points depending on the internal cell structure employed. In a single transistor cell structure, each bit location in memory is represented by one MNOS transistor, while two transistors per bit are used in the two transistor cell structures. Each has advantages and disadvantages. High packing density is possible with the former, but retention time is a little less than in the latter case due to the need to be

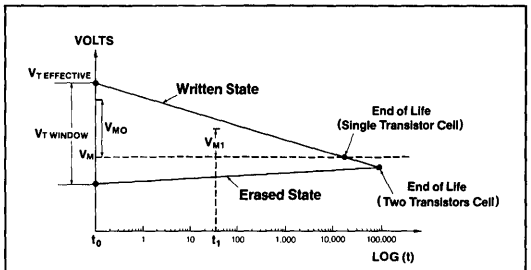

Fig. 3

able to detect an absolute level of threshold voltage (see Figure 3). The two transistor cell improves retention time since relative differences between V_W and V_E, not absolute values, must be detected, but this is achieved at the expense of packing density.

A compromise solution is a structure which uses one reference device per word of memory. Differences are measured as for the two transistor cell, but packing density is not as good as in the single transistor arrangement.

2) Endurance

Continual high voltage stressing of the nitride/oxide dielectric has a destructive effect on the charge holding properties of the nitride. Stressing occurs during erasing and writing when the 25V potential difference appears across the memory device. Its detrimental effect appears as a reduction in data retention time in the manner shown in Figure 4. As for retention, rewriting will restore the threshold voltages to the original, t_o levels. Retention time is reduced slightly with every reprogramming cycle, but in most cases, greater than 10 years' retention at 70° C is attained after several thousand cycles.

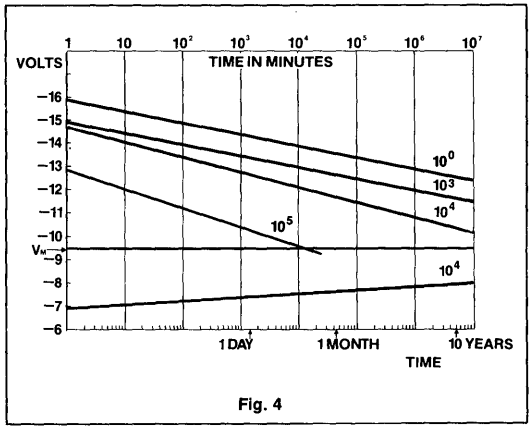

Fig. 4

3) Read Disturb

Reading is performed by applying V_M (approx. −9V) to the memory gates, which act as a low energy write on erased transistors. The voltage is −9V as opposed to −25V during writing and is applied for microseconds rather than milliseconds, but the effect is the same with each read causing an immeasurable negative shift in V_E. However, the cumulative effect of a large number of reads becomes significant enough, at some point to degrade V_E to below its detectable level ($> 10^9$ reads). Again, the mechanism is non-destructive and rewriting restores V_E to the original level.

4) Temperature Effects

Since retention is a charge leakage phenomenon, increasing temperature has an increasingly detrimental effect on data storage time. The typical response is similar to that of endurance.

APPLICATIONS

The important characteristics of EAROMs are:

- Non-volatility
- In circuit, electrical reprogrammability
- Word alterability
- Ease of use and cost effectiveness in terms of cost per bit and reprogramming cost.

Some of these, or a combination of several have been responsible for the adoption of MNOS technology in a large number of different areas of application

Traditional uses have been in TV and Radio tuners where non-volatility and electrical, word alterability are essential. A significant proportion of the EAROMs shipped by General Instrument in the last four years have been used successfully in this tough environment to hold tuning information, usually the digital equivalent of varactor tuning voltages or frequency divisors in phase locked loop systems.

EAROMs were also developed for security reasons for use in point of sales terminals and, more recently, have been used for the same reason in postage meters where thousands of dollars are at stake.

In many cases, the use of MNOS memory has eliminated the need for expensive service calls by field engineers as previously required for customizing terminal format features determined by arrays of DIP switches. EAROM replacement of the switches now allows formatting information to be modified by the user from the keyboard. A similar application is in PABX systems where, again non-volatility, in-circuit reprogrammability and word alterability are necessary.

Increasingly, EAROMs are being used in microprocessor and microcomputer applications to store program and data, very often as non-volatile backup during power outage. Advancing technology, specifically the move from P-Channel to N-Channel will make these memory devices more readily microprocessor compatible by reducing access time, increasing the number of read accesses and minimizing cost through improved packing density.

New applications are being continually developed, particularly in the industrial control and automotive fields. An application where non-volatility is essential is in automobile odometers in which EAROMs have been used for long term storage of mileage.

In the industrial field, infrequently changed process parameters and process sequence steps are stored in EAROM, again making use of the easy, electrical and word reprogramming capabilities of the devices. The information may be altered from a keyboard by the operator at the site without the need for a service engineer visit.

In the military field, EAROMs have found application in critical areas such as missile control circuitry, flight recorders and crash recorders — in this case as a replacement for unreliable, mechanical tape units.

CONCLUSION

In conclusion, the MNOS technology is a mature one, which by its extensive implementation in many varied applications in the field has proven to be highly reliable as a non-volatile information storage medium. EAROM is the only non-volatile memory device type currently available, in quantity, which in addition to electrical, in-system reprogramming ability also offers word alterability — a feature which has made it feasible for use in many areas which no other device could serve as effectively.

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Bulletin 1223

New EEPROM Removes Separate Write/Erase Necessity

Morton L. Kalet
Joseph J. Spadaro

Throughout the evolution of semiconductor memories, the primary goals have been higher density and higher speeds. The higher densities implied a greater number of bits per device at a lower price per bit, while the higher speeds were required to permit interfacing with the faster microprocessors appearing on the market. This paper will describe a memory device which takes advantage of improvements in density, not to obtain a larger memory, but to create an inexpensive small memory having an access time of less than 200ns and on-chip features permitting additional system cost savings. It also attains the speeds necessary to operate with today's microprocessors.

MEMORY CLASSIFICATION

In general, memories have fallen into two categories: Non-reprogramable memories, which are non-volatile, and reprogramable memories, which are volatile. The non-reprogramable memories are used in applications where permanent data, such as the series of instructions for the operation of a calculator or the rules of a TV game, is stored in a Read Only Memory (ROM). Reprogramable memories, on the other hand, are used in applications where data will be altered (such as the storage of the results of a number crunching operation in a calculator) and are defined as Random Access (read/write) Memories. This type of memory has suffered from a major disadvantage: the loss of data when power is removed. The introduction of the EAROM (Electrically Alterable Read Only Memory) in the 1970's combined the advantages of both of the above mentioned memory types, that is, a ROM which could have its data altered, electrically, within the operating system.

This now permitted the system architect to include a memory in his design which could store variable data and retain it during a power outage. The disadvantages of these devices, for some applications, were the slower access times (inherent in the original P-MOS technology), and the external high voltage power supply required. Additionally, since the erase/write times are several milliseconds, during which time the address and data must be present, the system basically remained in a wait state. An exception to this situation is the General Instrument ER3400, which has address, data and control mode latches.

The above disadvantages, however, have all been eliminated in the new SNOS (Silicon Gate Nitride Oxide Semiconductor) ER5901, which is organized as a 128 x 8 memory (see Figure 1) and has a typical read access time of less than 200 nanoseconds, on-board latches for address and data and operates from a single +5V power supply in all modes. In order to make the device more versatile, the chip has been designed to operate in either a multiplexed or non-multiplexed system environment.

Before describing the actual device operations, a short review of the technology will be presented.

SNOS THEORY

Basically, the data stored in any digital memory is represented by either a device or circuit which may be placed into either one of two states.

The original MNOS (Metal Nitride Oxide Semiconductor) transistor used in all EAROM products is a tri-gate structure shown in cross section in Figure 2a and the equivalent schematic representation shown in Figure 2b. The insulator between the metal gate and semiconductor is a dual dielectric made up of an oxide-nitride sandwich. Transistors 1 and 3, with oxide and nitride thicknesses of approximately 500 Å each, have non-variant threshold voltages of −3V. On the other hand, transistor 2, which has an oxide thickness of less than 50 Å, has a variable threshold which determines the effective threshold of the tri-gate transistor. This is due to the fact that all three transistors are of the enhancement type and must be turned on to obtain conduction between source and drain. The variable threshold is dependent on whether there is a net negative or positive charge stored in the nitride. A stored negative charge moves the threshold voltage of transistor 2 in a positive direction and a stored positive charge moves it in a negative direction. The result of this charge storage on the effective threshold is shown in Figures 2c and 2d. The movement of charge takes place through the thin oxide region of transistor 2 by the Fowler-Nordheim mechanism and is dependent on the polarity of the high voltage (approximately ±25V) applied to the gate. It should be pointed out that both thresholds (erased and written) vary only in magnitude. The I-V characteristic plots are shown in Figure 3, and it may be observed that by applying a voltage V_m, which has been optimally selected, one may interrogate the device to determine which logic state is being stored in the memory.

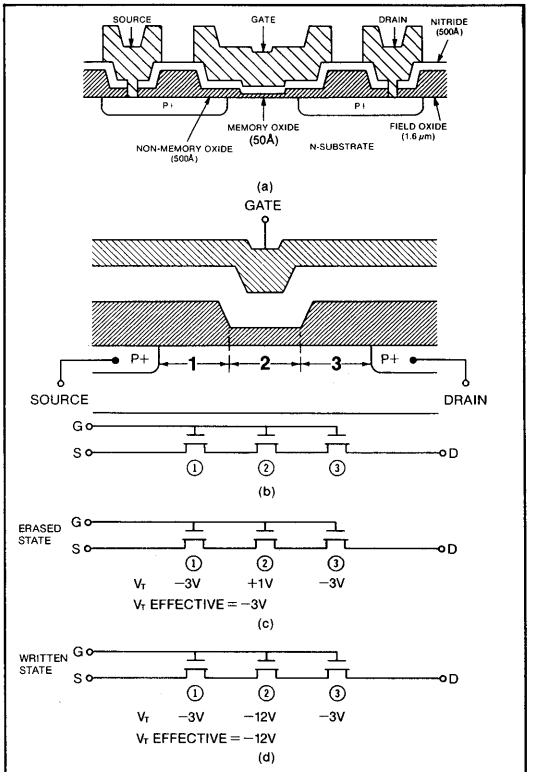

Fig. 2 TRI-GATE MNOS TRANSISTOR

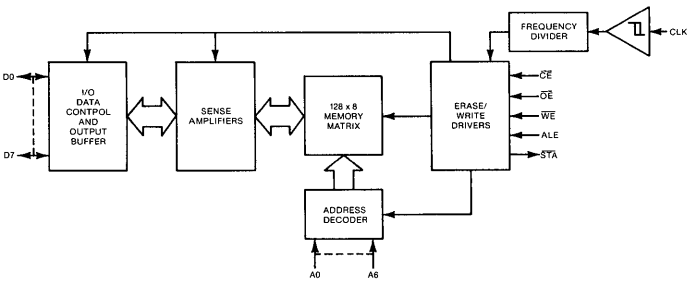

Fig. 1 ER5901 ARCHITECTURE

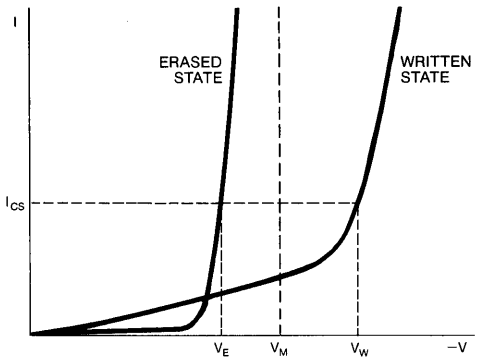

Fig. 3 I-V CHARACTERISTICS

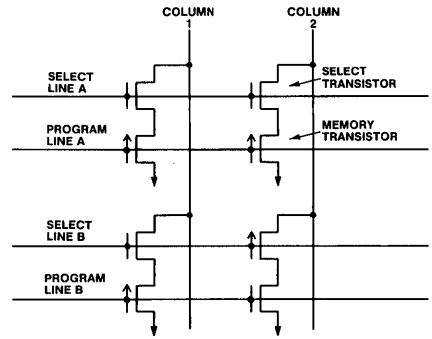

Fig. 4 MEMORY ORGANIZATION

TECHNOLOGY ADVANCEMENT

As in the standard MOS processes, a speed and scaling advantage is obtained by using N-Channel Silicon Gate technology. The tighter design rules used in the layout of integrated circuits in this technology permit modifications to the cell structure with corresponding performance benefits. Figure 4 shows schematically the memory cell used in the ER5901. Transistor A is the actual memory transistor whose threshold varies with the charge stored in the nitride over its channel region. The cross section of this device is identical to region 2 in the tri-gate structure shown in Figure 2a, although the gate is polysilicon rather than metal. Applying a large negative or positive voltage to the gate will cause Fowler-Nordheim tunnelling to occur. A net positive or negative charge causes the device to remain in either the depletion or enhancement state, respectively. In order to isolate the memory transistors from each other select transistor B is placed in series allowing the addressing of the chosen memory device. Interrogation of the memory is accomplished by applying a positive voltage to all columns and the gates of the select transistors of the addressed row, while grounding the gates of the memory transistors. If the memory device is in the depletion mode, then the corresponding columns will be grounded through the two transistors in series, both of which are turned on. Should the memory device addressed be in the enhancement mode, then it will be turned off preventing a path to ground and thereby resulting in the column remaining at a positive voltage. The sense amplifiers, which are monitoring the columns, will react to the voltage conditions and output the proper logic levels.

A significant portion of the chip silicon is given to the DC to DC voltage generator, on-board address and data latches, counters and random logic in order to present this device as a stand-alone, non-volatile memory, easily interfaceable with existing microprocessor systems.

ER5901 FEATURES

This EEPROM has been developed with the user in mind, and the reader will quickly grasp the fact that the ER5901 may be accessed from the system bus with the simplicity of accessing a static RAM (see Figure 5).

The advanced ER5901 has the following features:

- 1024 Bits, Organized 128 x 8
- N-Channel Silicon Gate SNOS Technology
- +5 Volts Operation in All Modes
- Fully TTL Compatible Inputs and Outputs
- On-Chip Latching of Addresses and Data
- Self-Timed, Processor Transparent Programing Mode with $\overline{STA}$ Busy Signal
- Address and Data Buses May be Used Separately or Multiplexed
- $\overline{CE}$ and $\overline{OE}$ Inputs to Avoid Bus Contention
- Word Alterable
- Read Access Time of Less than 200ns
- 10 Years Data Retention Over the Temperature Range of −40° to +85° C
- 10,000 Programing Cycles Per Word

INTERNAL MEMORY MANAGEMENT

By virtue of the on-chip reprograming control and timing of the ER5901, a minimum amount of servicing is required from a host microprocessor.

The user may select one of four operating modes:

1. READ with separate address and data lines.
2. READ with multiplexed address and data lines.
3. PROGRAM with separate address and data lines.
4. PROGRAM with multiplexed address and data lines.

The correct sequence of events necessary for operation in each mode is as follows:

1) READ Mode with Separate Address and Data Lines (See Fig. 6)

To initiate a read cycle a valid address must appear on the A0 to A6 inputs and remain there for the duration of the cycle because the address is not latched in this mode. $\overline{CE}$ may then be brought low to select the device. The desired memory byte will be in internal registers a short time later and will appear on data lines D0-D7 after a time delay t_{OE} measured from the falling edge of $\overline{OE}$. Alternatively, if bus contention is not a problem, $\overline{OE}$ may be tied low. The maximum read access time (T_A) is 200ns and data will remain valid until a logic level change occurs on $\overline{CE}$, $\overline{OE}$, or an address line. In this mode of operation ALE and $\overline{WE}$ are held high and may be tied together.

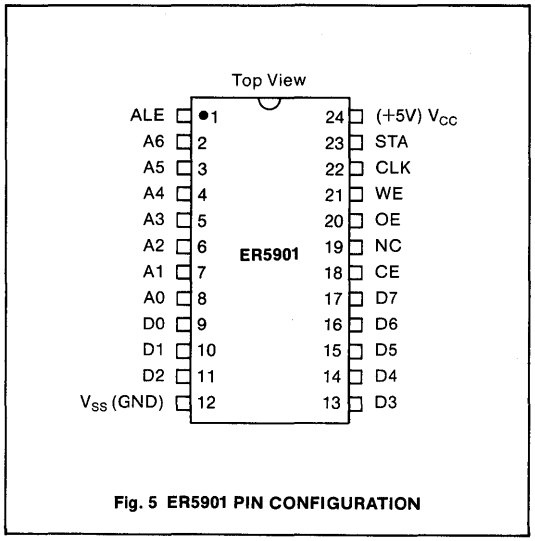

Fig. 5 ER5901 PIN CONFIGURATION

of a selected device, the $\overline{WE}$/ALE is pulsed low to initiate a program cycle. The falling edge of $\overline{WE}$/ALE latches the address inputs and the rising edge latches the data inputs. After a delay t_{STA} the $\overline{STA}$ output will go low and remain low for the duration of the programing cycle. All inputs to the ER5901 are disabled during the programing cycle.

4) PROGRAM Mode with Multiplexed Address and Data Lines (See Fig. 9)

The ALE line is pulsed high while the address to be altered is presented to lines A0-A6 of the selected device. The fall of ALE latches the address into the ER5901, and the information on the bus lines is then changed to the data to be written into the EEPROM. $\overline{WE}$ is pulsed low and the data is latched on its rising edge. After a delay t_{STA}, the $\overline{STA}$ output will go low and remain low for the duration of the programing cycle.

A GROWING FAMILY

The ER5901 was developed to satisfy a growing family of applications that require small (1K or less) user-programable nonvolatile memories which interface to a host microprocessor with a minimum of support hardware (see Figure 10). Such applications include DIP switch replacement in CRT terminals, look up table storage in frequently updated point-of-sale terminals (such as gasoline pumps), home appliances with programable duty cycles (washing machines), instruments which store their own calibration constants, electronic security systems, automobile odometers, etc.

The advanced features of this device will no doubt lead to painless designs with enhanced system price/performance ratios. And, of course, both the host microprocessor and the memory designer will derive the same benefit from using the ER5901 — both will have more time to perform other tasks!

Pin	Symbol	Function	Comments
1	ALE	Address Latch Enable	Address inputs latched on negative edge. May be tied to $\overline{WE}$ when separate address and data lines are used.
2-8	A0-A6	7 Bit Address	
9-11, 13-17	D0-D7	8 Bit Data I/O	
12	V_{SS}	Chip Ground Connection	
18	$\overline{CE}$	Chip Enable Input	Used for chip selection
20	$\overline{OE}$	Output Enable Input	Gates data to output pins during a read cycle.
21	$\overline{WE}$	Write Enable Input	Enables a reprograming cycle; input data latched on a positive edge.
22	CLK	Timing Inputs	Defines clock frequency for reprograming. May be RC or external clock.
23	$\overline{STA}$	Status Output	Low when chip is in reprograming mode and cannot be accessed. High when in read mode.
24	V_{CC}	+5 Volt Power Connection	

2) READ Mode with Multiplexed Address and Data Lines (See Fig. 7)

The ALE line is pulsed high, while a valid address is presented to the A0-A6 inputs of a selected device. The address is latched into the ER5901 on the falling edge of ALE and in order to avoid bus contention these lines should be tri-stated prior to pulsing $\overline{OE}$ low. After a delay t_{OE} the selected byte will appear on lines D0-D7 until either $\overline{OE}$ or $\overline{CE}$ goes high.

3) PROGRAM Mode with Separate Address and Data Lines (See Fig. 8)

In this mode the ALE and $\overline{WE}$ inputs may be tied together. With a stable address and data word presented to the respective inputs

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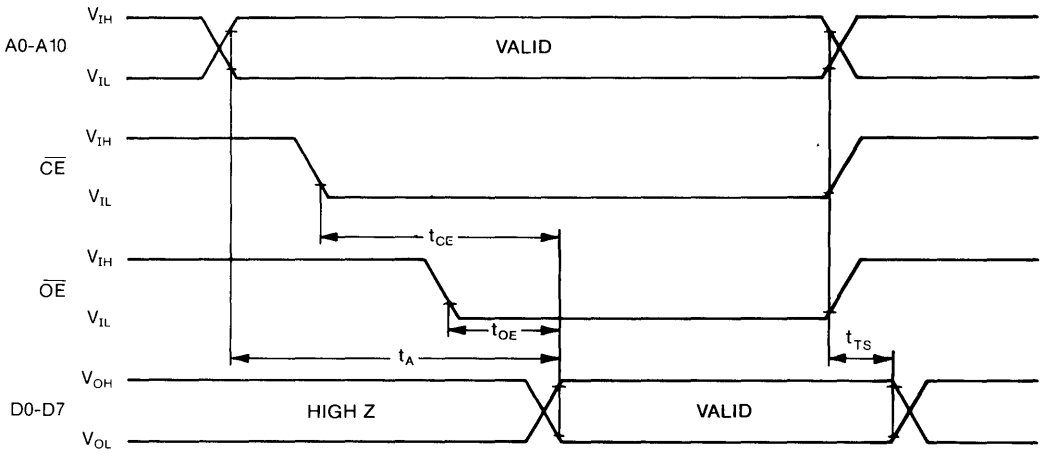


Fig. 6 READ MODE WITH SEPARATE ADDRESS AND DATA LINES

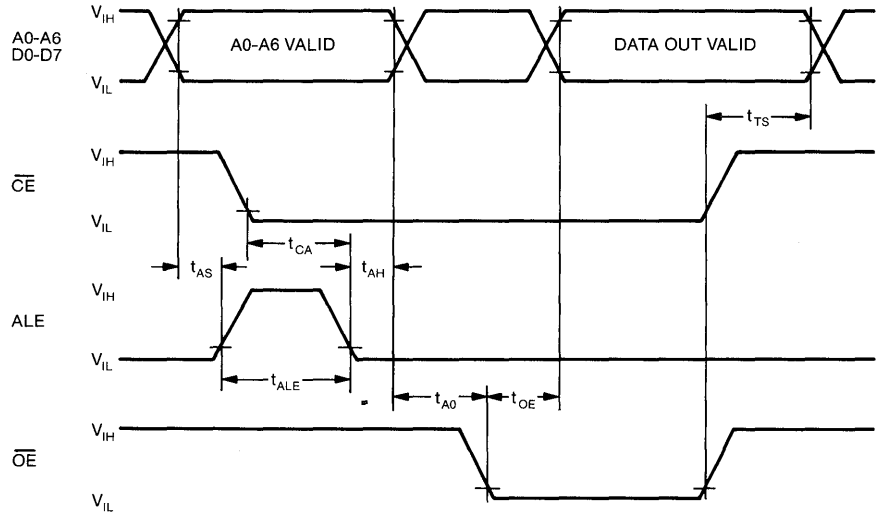


Fig. 7 ER5901 READ MODE WITH MULTIPLEXED ADDRESS AND DATA LINES

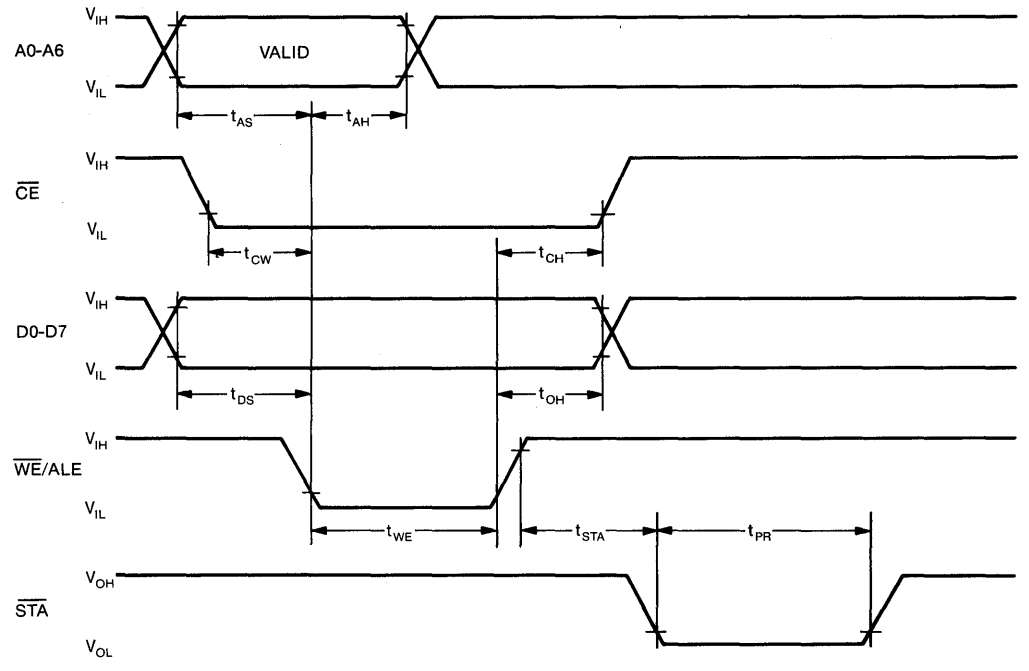


Fig. 8 ER5901 PROGRAM MODE WITH SEPARATE ADDRESS AND DATA LINES

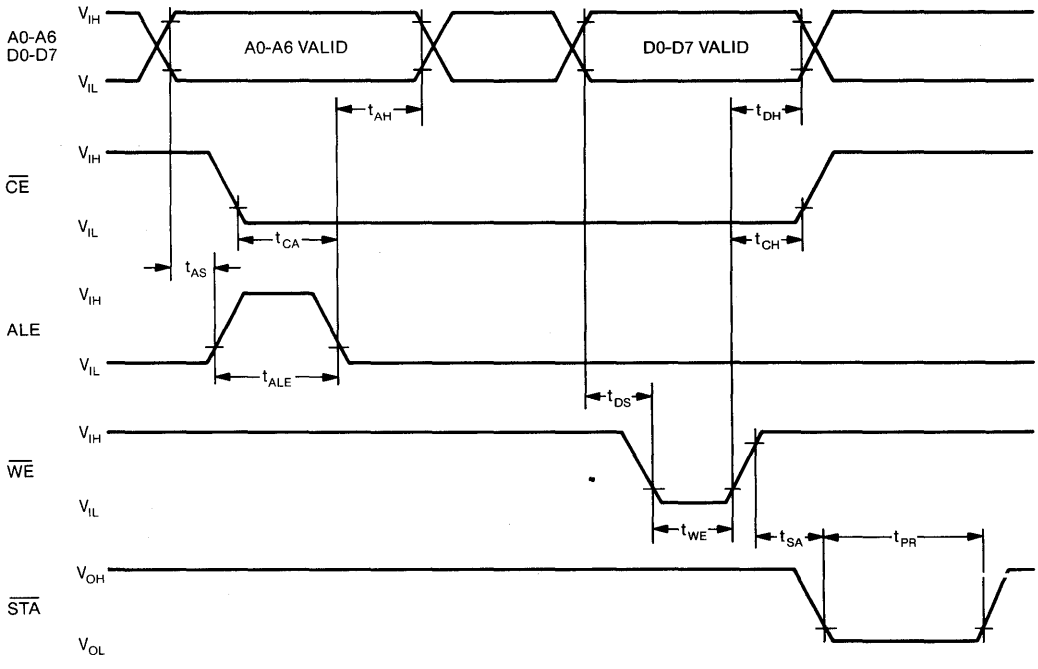


Fig. 9 ER5901 PROGRAM MODE WITH MULTIPLEXED ADDRESS AND DATA LINES

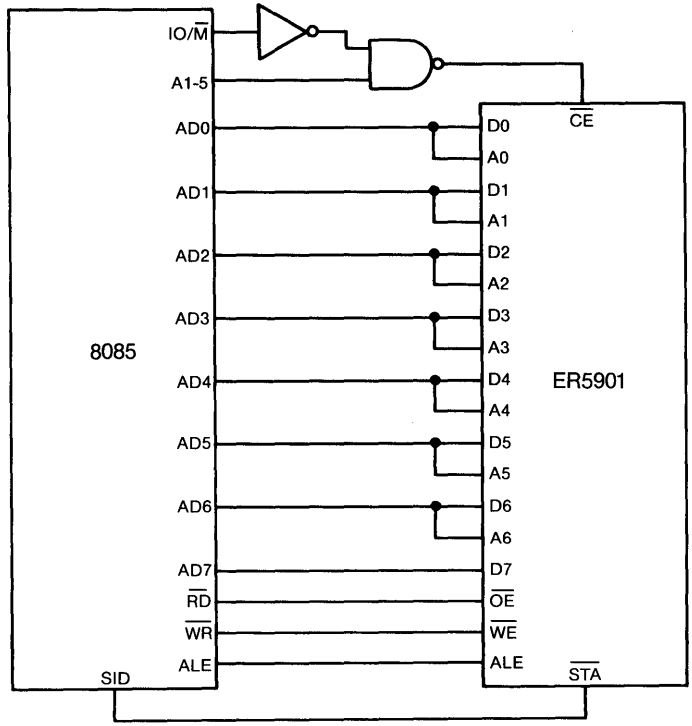


Fig. 10 ER5901 TO 8085 INTERFACE

Bulletin 1202A

The Role of Non-Volatile Memories in Consumer Electronics

Les Penner

The digital memory is, of course, a fundamental building block in modern electronic technology. Large scale integration has further increased its cost-effectiveness. A new type of memory, having fundamental properties differing from traditional memories, has the potential to make significant improvement in electronic devices used in the consumer field. The memory is called the EAROM, (Electronically-Alterable-Read-Only-Memory) and the property which is of significance is its non-volatility, its ability to retain information even when power is removed.

This application report was originally presented as a paper at the Chicago Spring Conference, 1977.

TRADITIONAL DIGITAL MEMORIES

To explain with clear perspective the function of the **non-volatile** memory, it is necessary to first review the properties of traditional digital memories. There are basically two types, the ROM (Read Only Memory), and the RAM (Random Access Memory). The ROM is a memory which has a fixed data pattern. The pattern cannot be altered once built in, but the data is not lost when power is removed.

The RAM has no pattern built into it and is loaded (written) by the host system. In this device data is volatile. These traditional semiconductor memories presented the designer with the choice of non-volatility coupled with unalterable data or alterable data that is volatile. Actually some improvements have been made in recent years with PROM and EPROM devices whose properties are compared in Figure 1 with ROM and RAM devices. Both PROM and EPROM devices have been developed to partially fill the gap between the ROM and RAM, that is, to provide non-volatile storage with the ability to write in them at the user's discretion. There are limitations however. In the case of the fusable PROM, writing can only be done once after which the pattern is permanently set in the memory. While in the case of EPROM, the erasure is done en masse by ultraviolet light and writing is done by a special apparatus. This device can be erased and rewritten numerous times but the entire contents of the memory must be changed simultaneously and the unit must be removed from the equipment. You will notice that the EAROM can be erased and rewritten many times. This can be done on any limited portion (word) of the memory at a time without disturbing the rest of the data and it can be done by electronic signals within the system. In a sense the EAROM has all the versatility of reading and writing that the RAM has but has the non-volatile properties of the ROM.

TYPE	NON-VOLATILE?	PROGRAMMABLE?	COMMENTS
ROM	Yes	No	Data Built in once Fast Read Cost Effective in Large Quantities
RAM	No	Yes	Fast Read
PROM (Fusable Links)	Yes	Once - In the Field	Fast Read Cost Effective for Small Quantities
EPROM	Yes	Numerous times in the Field but outside the System	Not Word-Alterable Bulk erased by UV Light
EAROM	Yes	Numerous Times in the System	Word Alterable Fast Read Slow Write

Fig.1 COMPARISON OF MEMORY FEATURES

MNOS STRUCTURE

The EAROM is fabricated by an MOS process called MNOS which stands for metal-nitride-oxide-silicon. The process is a refinement of the standard P-Channel nitride gate process, and in fact, the logic transistors surrounding and supporting the memory matrix itself, have conventional P-Channel nitride characteristics. The memory device, however, has a gate structure whose center has an extremely thin portion of oxide. This thin portion (on the order of 25 to 50 angstroms) is the key to the memory structure. This is illustrated in Figure 2.

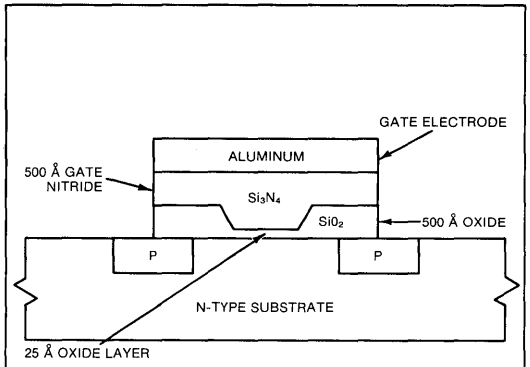


Fig.2 P-CHANNEL MNOS MEMORY TRANSISTOR GATE STRUCTURE

When gate voltage is applied, extremely high field gradients appear across this thin oxide area. This field causes tunneling to take place which is a semipermanent transfer of charges. These charges move from the substrate to the interface between the nitride and oxide layers of the gate. The charge transfer only takes place when the field intensity is present. When the field is removed the charge does not leak off. When the gate electrode is made highly negative with respect to the substrate we call this polarity "writing". When the gate electrode is made highly positive with respect to the substrate we call this polarity "erasing". To achieve the strong fields necessary, a voltage on the order of 25V is required. This supply voltage is a necessary part of the system but it need be present only during alteration of data, not during reading or standby. There are also limitations to the number of times that writing and erasing can take place. Figure 3 shows the typical electrical characteristics of an EAROM memory.

Supply Voltage for Writing and Erasing	−25 to −35V
Supply Voltage for Logic	−12 to −17V
Logic Levels	CMOS+TTL Compatible
Write Time (Per Word)	1 to 50ms
Erase Time (Per Word)	10 to 50ms
Read Access Time	1μs
Data Retention Between Writes	10 Yrs.
Number Write Erase Cycles	10^5
Number Read Cycles Between Writes	10^{11}

Fig. 3 TYPICAL ELECTRICAL CHARACTERISTICS—MNOS LSI

HOW TO USE IN CONSUMER PRODUCTS

In a general sense, there are three ways in which the EAROM device can be used to advantage in consumer products:

1. **Stored data or information.**
   In this mode the EAROM can contain tables which may be varied from time to time, identification numbers, or subtotals.
2. **Current status.**
   In this mode the EAROM can be used to protect the system against power loss either intentional or accidental. Vital data can be stored in the EAROM; current status or mode can be stored; progress through a sequence can be remembered so that all this information can be restored to the system when power is eventually returned permitting the system to continue its sequence where it left off when power was interrupted.
3. **Store program for microcontroller.**
   The microcontroller is achieving widespread use. Characteristics of these devices are varied by their programs. When the program is stored in an EAROM the characteristics of the system can be altered by changing part or all of the program ROM.

HOW TO MODIFY EAROM

The EAROM depending upon the nature of the data stored, would be loaded or modified at various points:

1. In some applications, the user of the end product updates the EAROM. For example, when the EAROM is used to store favorite stations in a tuning system, storage of that information is done by the listener when he updates his tuning buttons.
2. The equipment manufacturer can update the EAROM. In systems where a unique identification code or serial number is to be loaded into each piece of equipment the manufacturer can load the EAROM.
3. The system itself can update the EAROM. When used, for example, to protect against power outage, the equipment is constantly updating the EAROM with vital data.

SOME EXAMPLES

Some specific examples of how to use the EAROM in this system are as follows:

1. **Protection against power outage either accidental or intentional.**
   This is becoming more important as electronic devices come to replace their electro-mechanical counterparts. In appliance timers and other similar applications, the electro-mechanical motor and cam-driven timer inherently has the ability to remember its current status when power is removed. Until now, the electronic analogy was achieved by keeping power on the electronic timer even when the main appliance was shut off, or by providing a battery backup. Both of these approaches have their obvious drawbacks.
2. **User programming of functions and buttons.**
   In this application, the user of the consumer product programs certain buttons to perform specific functions by teaching the machine in a set-up mode. The buttons then perform the desired function when called upon. The most well-known case is the five button selector of the automobile radio in which the listener sets up the five buttons to tune to his favorite stations when selected. The EAROM permits the electronic counterpart of this popular device to be produced.
3. **To "Curve-Fit" to varactor tuners.**
   With the advent of electronic tuning open-loop voltage synthesizer systems are becoming more popular because of their cost advantages. A varactor tuner, however, must be accompanied by a memory device with flexible programming capability since each varactor tuner differs from unit to unit, this must be set up either manually or automatically and stored in the non-volatile memory. Again this is the ideal component.
4. **To store semipermanent tables and data.**
   Various applications exist in which it is desirable, to store for long periods of time, particular information but to also be able to alter that information from time to time. For example, in point-of-sale equipment, one would like to load in a tax rate or an identification code which might remain valid for long periods of time but one would like to modify that data with relative ease.

The EAROM has already found its way into numerous consumer applications; radio and TV tuning, point-of-sale equipment and calculators. In the near future, we can expect to see EAROMS entering into such systems as repertory dialers, message reminders, video games, utility meters and automobile odometers.

Bulletin 1217

The ER3400: An Easy to Use 4K EAROM

Gary Ritter
Emyr Edwards

The ER3400 is the most sophisticated P-Channel EAROM available from General Instrument. Its easy usage makes it ideal for both microprocessor-based and random logic-based systems requiring either in-system or out of system programming.

DESCRIPTION

The ER3400 is organized as 1024 — 4-bit words. Each word can be individually erased and reprogrammed or alternatively, the entire device can be erased. Selection of the four modes of operation, Read, Write, Word Erase and Bulk Erase, is by a 2-bit TTL level code entered on control lines C0 and C1. A Chip Enable is provided to allow bussing several chips together; it also acts as a strobe to load in address and control data. Finally, "Write Enable" input is used to strobe data in the ER3400 for writing.

OPERATION

Erase

To erase one word, C0 and C1 are set in the logic high state, and the desired address location is set. A negative excursion of Chip Enable ($\overline{CE}$) loads in the address and control and initiates the Erase. To avoid tying up a microprocessor buss, this mode is latched on the falling edge of $\overline{CE}$. The Erase will continue while $\overline{CE}$ is high.

When it is desired to erase the entire device, the operation is the same except that C0 is low while C1 is high.

A "Dummy" Read is required to end the Erase cycle.

Write

The control code for write is C0 high, C1 low. The control word and address are strobed in via the $\overline{CE}$. Data is strobed in via the Write Enable ($\overline{WE}$). The timing requirements for $\overline{WE}$ are designed so that $\overline{WE}$ may be generated by gating the Chip Enable and a Write signal.

As is the case with Erase, the control code and address are latched on the falling edge of $\overline{CE}$. Data is latched by the rising edge of $\overline{WE}$. As in Erase, a "Read" is required to end the Write.

Read

To read out data, C0 and C1 are both held low and the desired address selected. Chip Enable strobes in the mode and address data and clocks out the data.

In all modes, when $\overline{CE}$ is high the data input/outputs are in a high impedance state.

C0	C1	Mode
0	1	Block Erase
1	1	Word Erase
0	0	Read
1	0	Write

In the WRITE and ERASE (both word and bulk) modes, data, addresses and the state of the control lines are loaded into internal registers within the ER3400 on the falling edge of the $\overline{CE}$ pulse and later cleared by a "Dummy READ" pulse on $\overline{CE}$. Reliable operation of the EAROM requires that the maximum delay times given in the ER3400 data sheet for the WRITE and ERASE operations not be exceeded. Specifically, these are the times between the $\overline{CE}$ pulse initiating the ERASE or WRITE operation and the $\overline{CE}$ pulse for the "Dummy READ" terminating the cycle. Permanent damage may be done to the EAROM memory transistors if the "Dummy READ" is omitted or excessively delayed. In microprocessor based systems where the $\overline{CE}$ pulse is software generated, care should be taken to avoid long delays before the $\overline{CE}$ "Dummy READ", and to avoid leaving the $\overline{CE}$ pulse low too long. Unreliable operation may also result if the maximum rise and fall times specified for the $\overline{CE}$ and $\overline{WE}$ pulses are exceeded.

Power Supplies

The ER3400 contains internal power supply sensing circuits to insure that stored data cannot be lost due to power supplies being out of range thereby causing faulty WRITE or ERASE cycles. If a $\overline{CE}$ pulse occurs while a power supply is not within specifications, the operation will become a READ independent of the external states of C1 and C0. Thus care should be taken that V_{SS}, V_{DD} and V_{GG} are within specification before each ERASE or WRITE, otherwise these operations may be replaced by READS.

The ER3400 may be operated in a read only power saving mode. If the V_{GG} (−30 Volt) power supply is turned off and brought to V_{SS}, data can be read from the EAROM. When V_{GG} equals V_{SS}, internal circuits create the memory reference voltage from V_{DD}, the −12 Volt power supply. This saves approximately 100 milliwatts, and prevents any ERASE or WRITE.

In systems with CMOS and PMOS microprocessors, the ER3400 may be operated from +15 and −20 volt power supplies, instead of the usual +5, −12 and −30 volt power supplies. Operation in this mode is possible because of the very high MOS input impedances. Tie V_{SS} to +15 ±5% Volts and both V_{DD} and V_{G1} to ground. With V_{GG} at −20 Volts, ERASE, WRITE and READ modes are functioning. With V_{GG} at +15 Volts, the ER3400 is in the power saving READ mode. The READ data access time will be increased by 10% whenever V_{SS}-V_{DD} equals 15 Volts.

SUGGESTED CIRCUIT

A programmer using CMOS is illustrated in Figure 2. A CMOS 14 stage divider is the main timing source, eliminating the need of one shots for generating the Read, Write and Erase times. The dual D-type, U2, generates the Dummy Read required to terminate a Write or Erase operation. If a visual display is desired a CD4042 Quad latch may be added. If this is done, the latch input of the chip should be tied to the Chip Enable line. This will hold the read data for display.

Figure 1 shows the timing of the signals produced by the circuit of Figure 2. With a 1MHz input clock, a Read occurs every 1.1ms. The Write time is also 1.1ms and the erase is 17 ms. Flip-flop 4013D changes state with every cycle causing alternate cycles to be "dummy READS," by forcing C_0 and C_1 to be low.

The high input impedance of the ER3400 and associated CMOS circuitry eliminates the need for a bi-directional bus driver on the data lines.

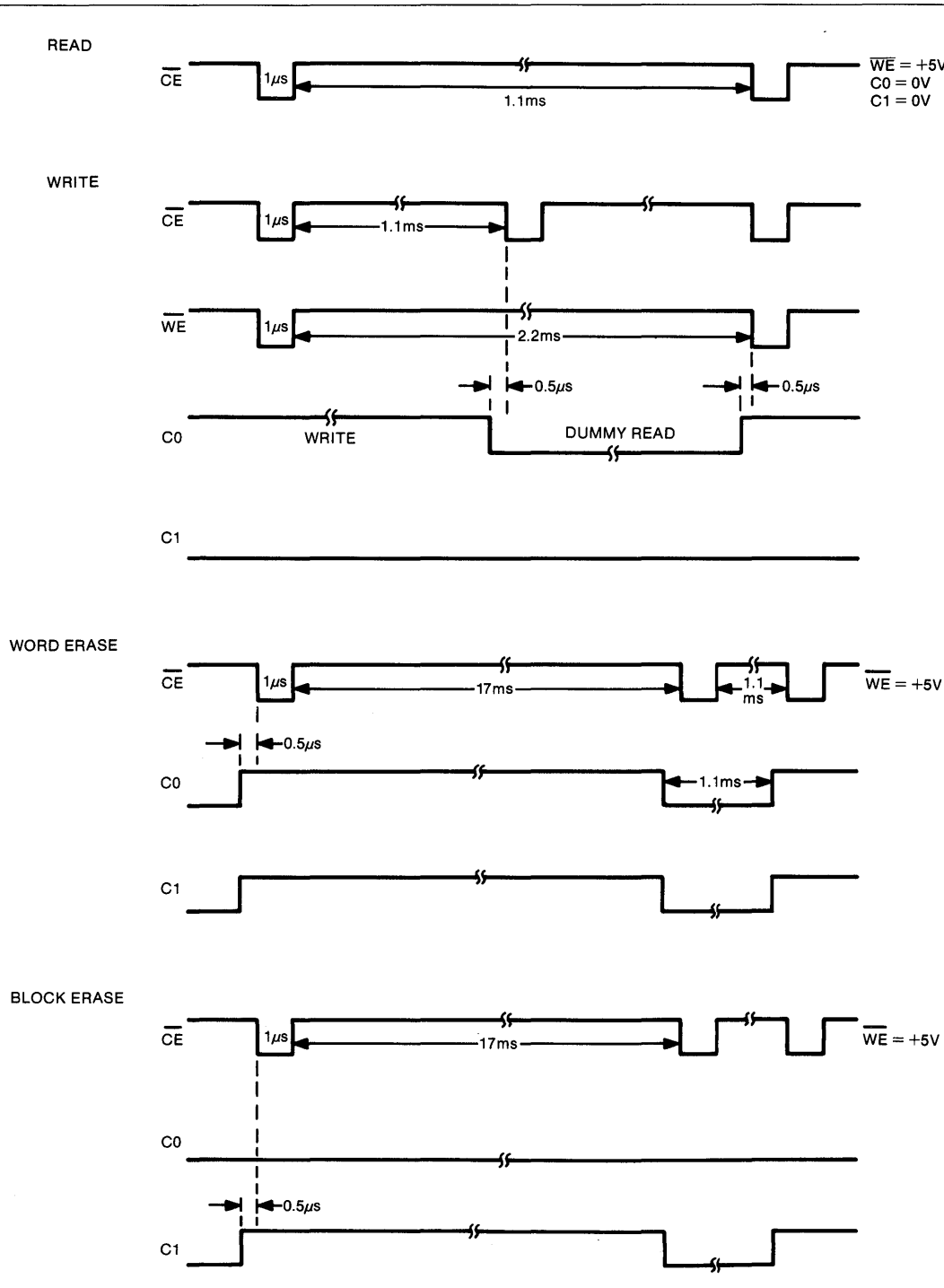
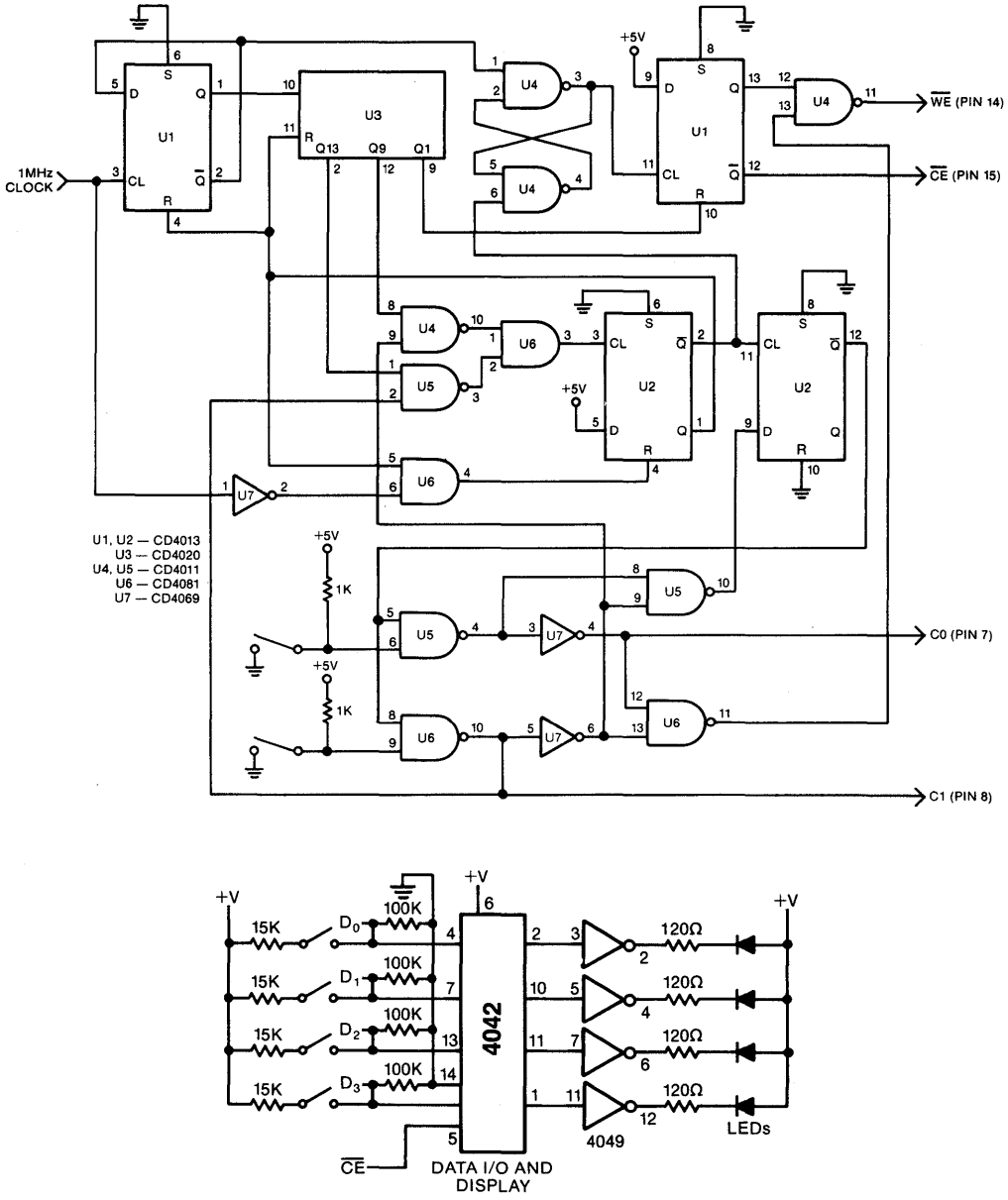

READ
CE
1μs
1.1ms
WE = +5V
C0 = 0V
C1 = 0V
WRITE
CE
1μs
1.1ms
WE
1μs
2.2ms
0.5μs
0.5μs
C0
WRITE
DUMMY READ
C1
WORD ERASE
CE
1μs
17ms
1.1 ms
WE = +5V
0.5μs
C0
1.1ms
C1
BLOCK ERASE
CE
1μs
17ms
WE = +5V
C0
0.5μs
C1

Fig. 1


1MHz CLOCK
U1
U3
U4
U5
U6
U7
U2
+5V
1K
WE (PIN 14)
CE (PIN 15)
C0 (PIN 7)
C1 (PIN 8)
U1, U2 — CD4013
U3 — CD4020
U4, U5 — CD4011
U6 — CD4081
U7 — CD4069

+V
15K
100K
D0
D1
D2
D3
4042
120Ω
LEDs
4049
CE
DATA I/O AND DISPLAY

Fig. 2

Bulletin 1210

Data Retention Testing of ER3400

Michael French
Emyr Edwards

GI non-volatile Electrically Alterable Read Only Memories, EAROMs, have their data retention guaranteed for ten years. Data retention can be measured by a simple non-destructive analog test. This testing can be performed by customer incoming inspection to verify good parts or by engineers to measure the effects of varying parameters on data retention. Volatility testing is already being used by several large EAROM customers for routine incoming inspection.

Data is stored in EAROMs by trapping charge within the silicon and nitride gate insulators of the MNOS transistors. For a detailed explanation, see the "Technology" article in EAROM application note Bulletin #1215.

Data Retention (volatility) measurements consist of measuring the amount of charge stored on a transistor's gate and its rate of decay. The decay of trapped charge is analogous to charge leakage from a high quality capacitor. The amount of charge stored depends on how well it was written, while the rate of decay depends on temperature, the number of Erase/Write cycles (this is termed "Endurance"), and process variations. As in a capacitor, the rate of charge decay is constant with respect to the log of time. This means that the charge loss, measured by a change in voltage threshold, is constant for each decade of time. By measuring this rate of change over the first ten hours, the user knows what it will be between 1000 and 10,000 hours, or between 10,000 and 100,000 hours, since the rate of change is constant for all decades of time.

Data is stored in the EAROM by writing high and low threshold states into the individual MNOS memory transistors. Data retention fails when the EAROM can no longer accurately read back the written data. This occurs when the charge has decayed to a point where the high and low threshold states are no longer distinguishable. Data retention times are measured by first writing the memory, reading the MNOS transistor's threshold, waiting a short time and reading the threshold again. How long to wait depends on the required accuracy and the sophistication of test equipment. General Instrument does a 100% 24 hour READ-only test on all ER3400's.

The data thresholds can be measured by varying the memory reference voltage (the voltage applied to the MNOS transistor gate) while continuously reading the part. As long as the part continues to read data correctly, the threshold has not been reached. The value of the reference voltage which causes the part to read inaccurately is the threshold. As shown in figure 1, there are two thresholds. The low, or "erased" threshold, remains approximately constant with time, as shown. The high, or "written" threshold, decays exponentially with time (thus the rate of decay is constant per decade of time) and is a function of the following variables:

a. Number of ERASE and WRITE cycles. There is a gradual, logarithmic increase in charge decay rate with number of erase/write cycles. At some number of cycles, the change will have become significant enough to reduce data retention time to less than 10 years. This number is always greater than 10^3. Degradation of the retention time continues beyond 10^3 cycles but is typically still greater than 1 year after 10^4 cycles.

b. Duration of ERASE and WRITE cycles. Long erase/write operations degrade a part's life due to the increased voltage stressing of the nitride/oxide gate dielectric of the MNOS transistors.

c. Temperatures above 70° C reduce the time a part will retain data. Higher temperatures increase charge leakage and cause MOS transistor voltage thresholds to shift.

d. Process variations also effect the high threshold. The ER3400 specification calls for ten year data retention. The 24 hour data volatility test guarantees that every EAROM will store data for at least that long. In fact, most EAROMs, due to processing variations, are far better and will retain data much longer. When measuring the written thresholds on ER3400 EAROM's, most parts show no detectable written threshold for the first 24 hours. The 24 hour volatility test, which is done on 100% of ER3400s, tests that the written threshold is above a certain level by reading all addresses with the voltage reference externally offset to simulate a ten year life.

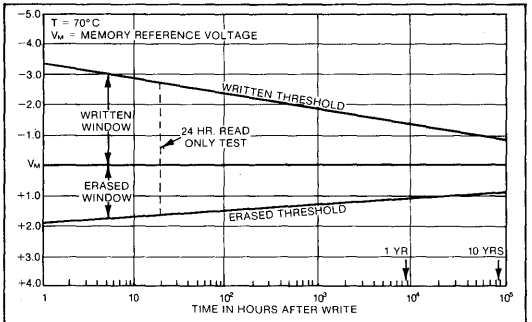


Fig. 1 TYPICAL DATA RETENTION CURVES

Measuring Memory Cell Thresholds on the ER3400

To actually measure the threshold of all or selected memory locations do the following:

1. First measure the voltage reference on C1 (pin 8) by making C0 (pin 7) equal to −28 volts, V_{GG}.
2. Set V_{GG} (pin 1) equal to the nominal reference voltage and read the ER3400. A minimum of 50 read cycles is required before data will be valid. Note that this is necessary only in test mode, not for normal operation of the EAROM.
3. While reading continuously, vary V_{GG} (the reference voltage for test purposes) more positive. The difference between the nominal reference voltage and the (low) threshold of first failure should be at least 0.5 Volts.
4. Now vary V_{GG} more negative. The part should read correctly until the externally supplied reference voltage equals the written (high) threshold. At this value the Read data will be inaccurate.
5. Repeated testing, without rewriting the EAROM, will show a constant value of low threshold and a time varying high threshold.
6. It is suggested that readings not be taken earlier than 1 hour after writing the part. The reason for this is that accurate measurements of threshold are time consuming, and for times less than 1 hour, there may be significant errors in time duration measurements.
7. The General Instrument 24 hour "Read-only"test uses voltage windows for written and erased thresholds calculated, in conjunction with empirically determined threshold decay slopes, to extrapolate out to a retention time greater than 10 years.

Bulletin 1218

Interfacing the ER3400 to an Eight Bit Microcomputer

Gary Ritter

This application note describes how to interface and control two ER3400 EAROMs with a PIC1650 microcomputer. The ER3400 is a reliable 4K EAROM available from General Instrument which is organized as 1K x 4 bits. To obtain an eight bit data word with a minimum of I/O lines and no additional hardware, the two 1K x 4 bit EAROMs are connected in parallel and accessed simultaneously. In addition to creating an 8 bit data word, this effectively cuts Erase and Write times in half.

This subroutine generates all the control signals and timing necessary to exercise the ER3400 EAROMs in any of their four modes of operation (i.e., Read, Block Erase, Word Erase, Word Write). In addition, an automatic Erase Write cycle can be executed by the subroutine.

The schematic for interfacing the two ER3400 EAROMs to the PIC1650 microcomputer is shown in Figure 1. The ten address lines and three control lines are shared by the two ER3400s and are directly connected to the PIC I/O ports without any additional hardware interface. The eight EAROM data lines are also connected directly to a PIC I/O port. The Write Enable signal $\overline{WE}$, although useful in certain applications, is not needed in this design and is therefore tied to $\overline{CE}$.

Prior to the execution of this subroutine, the users program sets the EAROM address to be accessed into file registers ADDR1 and ADDR2. If a Write operation is to be performed, the data to be written must be stored in the file register DATA. After a read operation, this register will contain the data read from the EAROMs.

Read Operation

With the EAROM address in the file registers, the user program need only execute one command, "CALL READ". This will cause the subroutine to be entered at Line 60. The control lines will be set to the read mode and the address lines will be output on I/O registers RA and RD. The $\overline{CE}$ line is next pulsed and the 8 bits of EAROM data are read in on RB and then stored in file register DATA. The subroutine then returns to the next command in the users program.

Reprogram Operation

Execution of a "CALL REPGM" command will enter the subroutine at Line 50. The subroutine uses bit 3 in file register ADDR2 as a flag bit to keep track of the Erase/Write cycle. The address contained in ADDR1 and ADDR2 will be output and the control lines set to the Word Erase mode. After the $\overline{CE}$ line is pulsed to start the operation, the Erase time loop will be executed. After 12ms the subroutine will generate a dummy read cycle to terminate the Erase operation. The data to be written is then output on the RB port and the control lines are set to Word Write mode. $\overline{CE}$ is pulsed and the Write time loop is executed for 1ms. A final dummy read cycle is then generated to end the Write operation and the subroutine returns control to the users program. The contents of file register DATA are undisturbed as is the address in ADDR1 and ADDR2. Bit 3 of ADDR2, however, has been set to Zero.

Block Erase

The subroutine is entered at Line 23 via a CALL BE command. This will cause the entire contents of the EAROMs to be erased to the "1" state. Address and data register contents are not considered in this operation. A dummy read cycle is automatically generated after 1ms to end the Erase operation and return control to the users program.

Word Erase

The subroutine is entered at Line 46 by means of a CALL WE command. The operation is similar to the Block Erase except that only one word, the one indicated by the contents of ADDR1 and ADDR2, will be erased.

Word Write

A word which has been previously erased via a Block or Word Erase may be written with the contents of register DATA. A CALL WRITE command will cause the subroutine to be entered at Line 35. Address and data will be output on the I/O lines and the control lines will be set to the Word Write mode. After execution of the Write Time loop, a dummy read is generated to end the Write cycle and control will be returned to the users program. Bit 3 of ADDR2 will be set to Zero upon exiting this subroutine.

Expanding to 16K

With an additional address line, an inverter and two OR gates this subroutine is capable of controlling 4 ER3400 EAROMs for a total of 16K bits. The two additional EAROMs are wired in parallel with the first two devices except for the $\overline{CE}$ line which is now gated with address line A_{10} as shown in Figure 2.

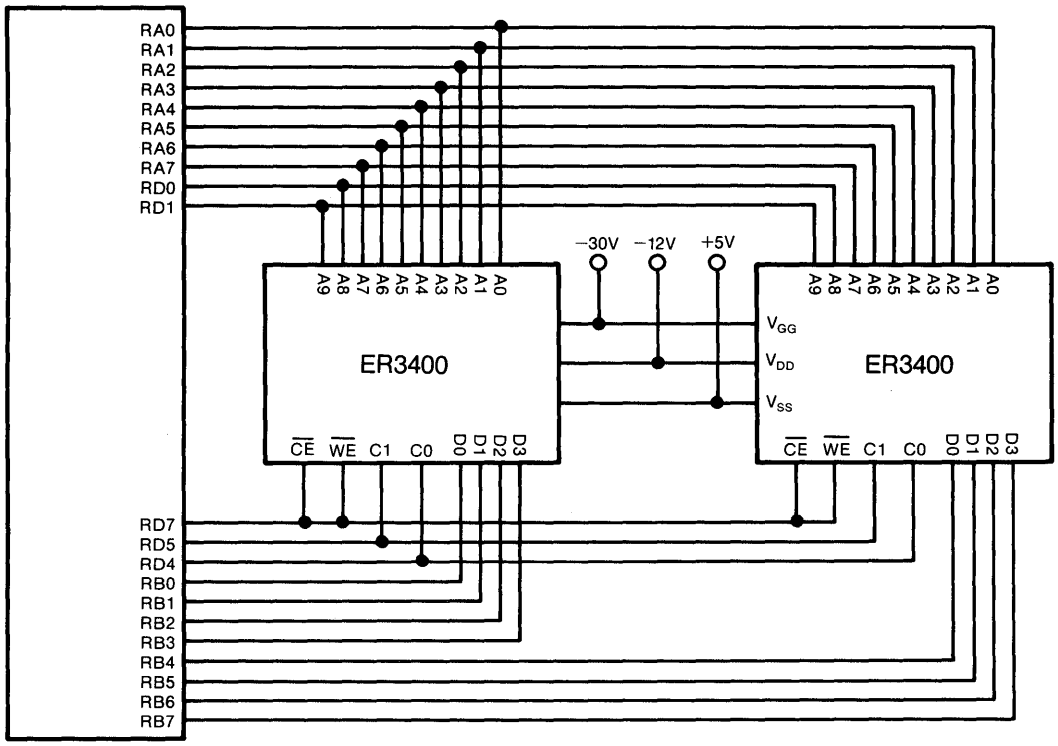


Fig. 1 PIC1650 TO ER3400 INTERFACE

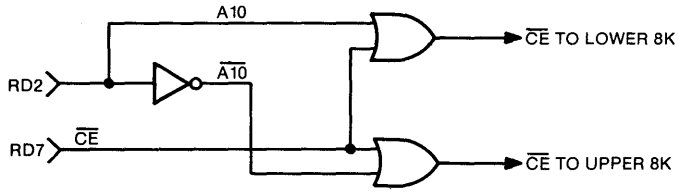


Fig. 2 INTERFACE FOR AN ADDITIONAL 8K OF EAROM MEMORY

```
                    ;************************
                    ;*  ER3400 TO PIC 1650  *
                    ;* INTERFACE SUBROUTINE *
                    ;*                      *
                    ;*                      *
                    ;************************
                    ;
000005              RA      EQU     5               ;A0 -A7 ADDRESS OUTPUT LINES
000006              RB      EQU     6               ;BITS 0 - 7 DATA IO LINES
000010              RD      EQU     10              ;BITS 0-1 = ADDRESS LINES A8,A9
                    ;                               BITS 4-5 = CONTROL LINES C0,C1
                    ;                               BIT 7 = CE'
                    ;DATA REGISTERS
000011              ADDR1   EQU     11              BITS 0-7 = ADDRESS BITS A0-A7
000012              ADDR2   EQU     12              BITS 0-1 = ADDRESS BITS A8,A9
                    ;                               BIT 3 = REPROGRAM FLAG (CONTROLLED BY SUBROUTINE)
                    ;                                   WILL BE = 0 UPON EXITING SUBROUTINE
000013              DATA    EQU     13              BITS 0-7 = EAROM DATA
000014              TEMP1   EQU     14              USED TO GENERATE TIMING FOR
000015              TEMP2   EQU     15              ERASE AND WRITE OPERATIONS
                    ;
                    ;         TIMER  SUBROUTINE
                    ;WRITE TIME IS CONTROLLED BY LITERAL AT LOCATION 0 AND 2
                    ;ERASE TIME IS CONTROLLED BY LITERAL AT LOCATION 5
                    ;
000000 06001        WTIME   MOVLW   1               WRITE TIME (1 MS)
000001 00055                MOVWF   TEMP2
000002 06114                MOVLW   114
000003 00054                MOVWF   TEMP1
000004 05007                GOTO    WAIT
000005 06004        ETIME   MOVLW   4               ;ERASE  TIME (12MS)
000006 00055                MOVWF   TEMP2
000007 01354        WAIT    DECFSZ  TEMP1
000010 05007                GOTO    WAIT
000011 01355                DECFSZ  TEMP2
000012 05007                GOTO    WAIT
000013 04001                RETLW   1               ;TIME IS UP
                    ;
                    ;   ADDRESS OUTPUT SUBROUTINE
000014 01012        ADDOUT  MOVF    ADDR2,W
000015 07017                ANDLW   X"0F"           ;SET CONTROL LINES TO READ MODE
000016 06600                IORLW   X"80"           HOLD CE' HIGH
000017 00050                MOVWF   RD              ;OUTPUT A8,A9 ON RD0,1
000020 01011                MOVF    ADDR1,W
000021 00045                MOVWF   RA              OUTPUT A0-A7 ON RA
000022 04001                RETLW   1
                    ;
                    ;****** ENTRY POINT FOR BLOCK ERASE ******
000023 06240        BE      MOVLW   X"A0"
000024 00050                MOVWF   RD              SET CONTROL LINES TO BLOCK ERASE MODE
000025 02350                BCF     RD,7            ;PULSE CE' TO START OPERATION
000026 02750                BSF     RD,7
000027 04405                CALL    ETIME
                    ;AUTOMATIC DUMMY READ
000030 04414        DREAD   CALL    ADDOUT
000031 02350                BCF     RD,7            ;PULSE CE
000032 02750                BSF     RD,7
000033 03552                BTFSS   ADDR2,3         ;1ST HALF OF E/W CYCLE ?
000034 04001                RETLW   1               ;RETURN TO USERS PROGRAM
                    ;
                    ;******* ENTRY POINT FOR WORD WRITE *******
                    ;
000035 04414        WRITE   CALL    ADDOUT
000036 02152                BCF     ADDR2,3         ;CLEAR REPROGRAM FLAG
000037 01013                MOVF    DATA,W
000040 00046                MOVWF   RB              ;OUTPUT DATA
000041 02610                BSF     RD,4            ;SET C0
000042 02350                BCF     RD,7            ;PULSE CE'
000043 02750                BSF     RD,7
000044 04400                CALL    WTIME
000045 05030                GOTO    DREAD
                    ;
                    ;***** ENTRY POINT FOR WORD ERASE *****
                    ;
000046 02152        WE      BCF     ADDR2,3         SET REPROGRAM FLAG LOW
000047 05051                GOTO    ERASE
                    ;***** ENTRY POINT FOR REPROGRAM CYCLE *****
                    ;
000050 02552        REPGM   BSF     ADDR2,3         ;SET FLAG FOR ERASE/WRITE CYCLE
000051 04414        ERASE   CALL    ADDOUT
000052 06260                MOVLW   X"B0"
000053 00450                IORWF   RD              ;SET C0 AND C1 HIGH
000054 02350                BCF     RD,7            ;PULSE CE'
000055 02750                BSF     RD,7
000056 04405                CALL    ETIME
000057 05030                GOTO    DREAD
                    ;
                    ;***** ENTRY POINT FOR READ *****
                    ;
000060 04414        READ    CALL    ADDOUT
000061 06377                MOVLW   X"FF"
000062 00046                MOVWF   RB
000063 02350                BCF     RD,7            ;PULSE CE'
000064 01006                MOVF    RB,W            ;READ EAROM DATA
000065 00053                MOVWF   DATA
000066 02750                BSF     RD,7            SET CE'
000067 04001                RETLW   1               ;RETURN TO USERS PROGRAM
```

Bulletin 1219

A Voltage Switching Circuit for the ER2810

Gary Ritter
Emyr Edwards

Popular due to its high bit density and low cost, the ER2810 electrically erasable read only memory requires switching of voltages on various pins to control the mode of operation. The circuit described is a simple, low-cost means of providing this control.

Only two control signals are required — $\overline{\text{Erase}}$ and $\overline{\text{Write}}$. These provide the three modes of operation, Erase, Write and Read, as shown in Table 1. These two inputs are TTL compatible.

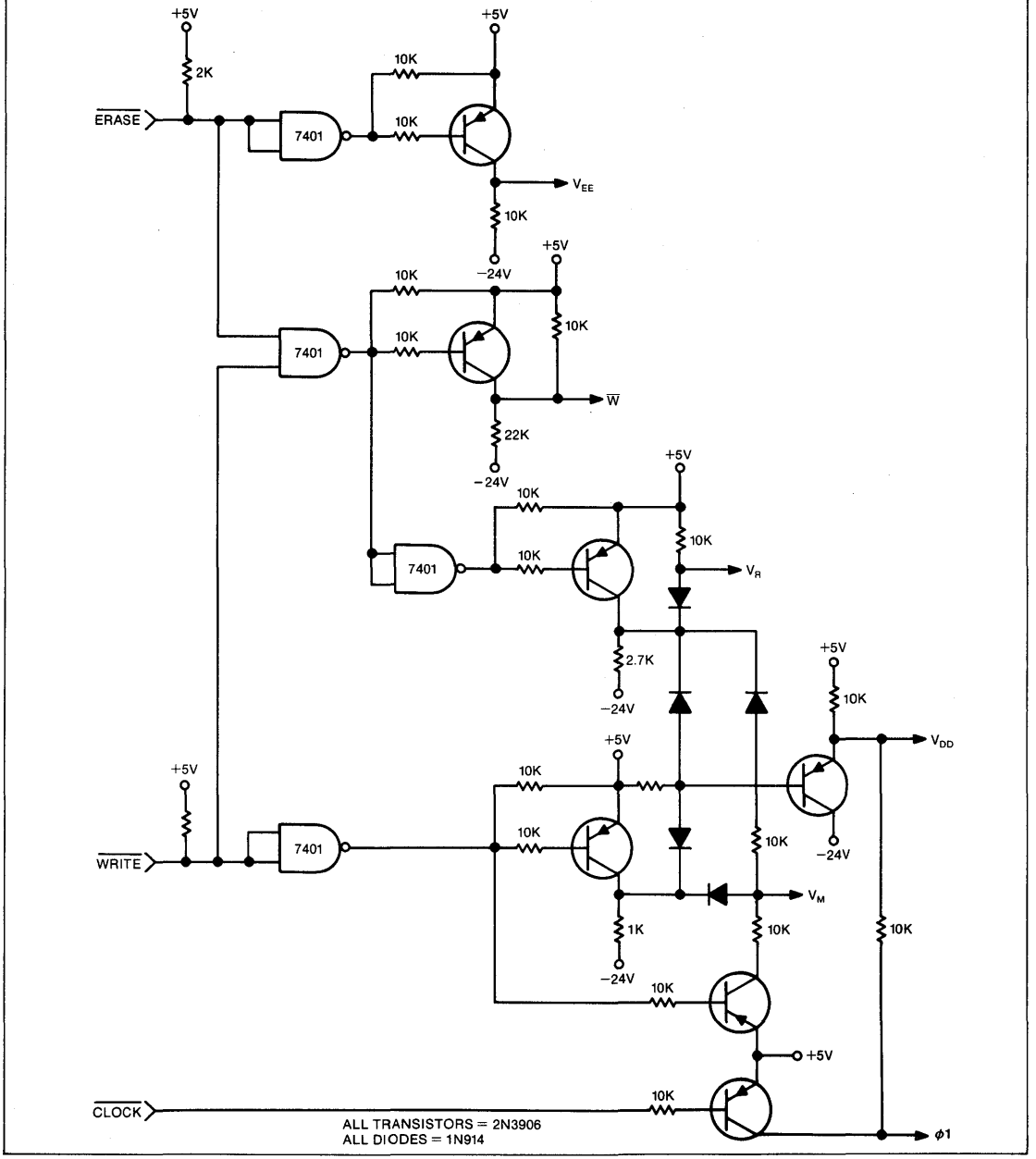
The circuit shown also buffers and level shifts a TTL level clock to provide the proper operating voltage levels.

The 2K pull-up resistors shown on the $\overline{E}$ and $\overline{W}$ inputs are also necessary when mechanically switching the inputs. When driving with TTL, these resistors may be omitted.

TABLE 1

INPUT		MODE	OUTPUTS TO ER2810					
$\overline{W}$	$\overline{E}$		$\phi 1$ (PIN 1)	$\overline{W}$ (PIN 9)	V_R (PIN 10)	V_M (PIN 23)	V_{DD} (PIN 24)	V_{EE} (PIN 4)
+5	+5	READ	+5 to −14	+5	−14	−5	−14	+5
+5	0	ERASE	+5	−5	+5	+5	+5	−23
0	+5	WRITE	+5 to −23	−5	+5	−23	−23	+5
0	0	NOT USED						

ER2810 VOLTAGE SWITCHING CIRCUIT



Bulletin 1220

Generating EAROM Programming Voltages from a 5 Volt Supply

Gary Ritter

Most EAROMs and EEPROMs require relatively high voltages for erase and write operations. This application note describes a low cost DC to DC converter circuit capable of generating this voltage from a +5 volt power supply.

A problem frequently encountered by EAROM users is the need for a power supply capable of delivering the relatively high voltage necessary when erasing and writing the device.

This simple, low cost DC to DC converter fills that need. Operating from a standard +5V power supply, the circuit as shown in Fig. 1 will deliver −30V at 8mA.

The circuit itself consists of two switching transistors which form a 50kHz oscillator. This signal is then applied to the output driver, which must be a high gain transistor to ensure sufficient output current. The 820μh choke coil in the collector circuit of the output driver produces high voltage pulses which are then regulated by the zener diode. Other negative voltages can be produced simply by substituting the corresponding zener diode. To obtain a positive output voltage reverse the polarity of the zener and the two switching diodes.

As one ER3400 EAROM needs only 4mA, this circuit is able to drive two devices in parallel, thus making the ER3400 a viable solution to many applications which require an eight bit data word. The circuit is also capable of driving one ER1451 or one ER1400. Should higher output currents be required, moderately priced DC to DC converters are available commercially.

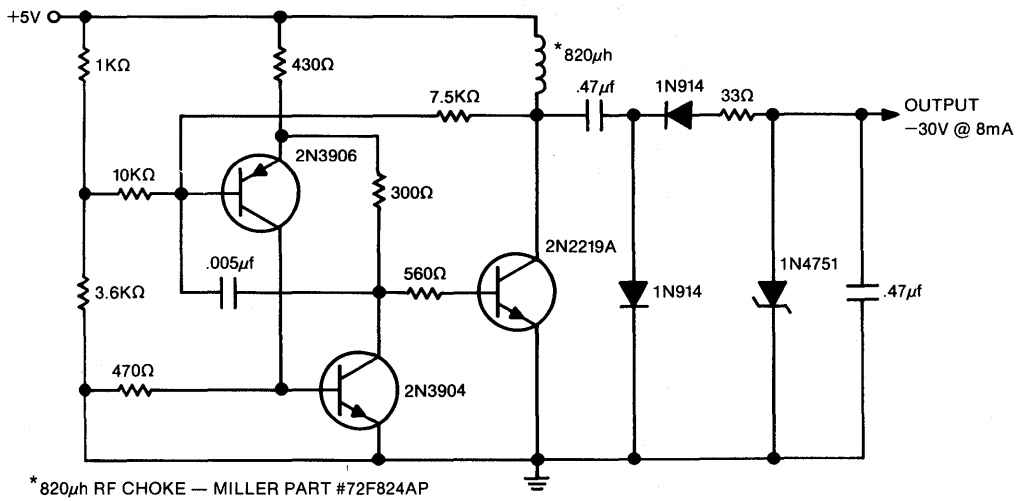


Fig. 1 +5V TO −30V DC CONVERTER

Bulletin 1206B

Electronic Digital Lock

Peter Rush and Brian Cayton

Illustrating a typical EAROM application, the digital lock described in this application note uses the ER2051 to store 4 different lock "combinations." This application provides data storage without power as well as easy reprogramming.

INTRODUCTION

The EAROM is a memory device which can retain information without any power being required. To that extent it is like a Read Only Memory. Unlike a ROM or PROM, however, the stored information can be erased and replaced with new information by the supply of electrical signals to the device. To this extent it is like a Random Access Memory.

The unique feature of electrical Read/Write capability, along with zero-power retention of data has major implications in the security industry as well as elsewhere. The diagram shows a demonstration of a new kind of electronic lock that

1) "Opens" when the correct 8 digit code is entered on a keyboard
2) Locks out if incorrect code is entered
3) Runs off a standard 9 V dry battery
4) Uses zero power when not keying-in
5) Contains no internal rechargeable battery
6) Has 4 different codes that will "open" the lock
7) Has one of these codes which additionally gives master access to a "programming" mode
8) Has a "programming" mode which allows any one or all of the 4 different codes to be changed, *including the master code.*

Some existing locks have some of these features, none can have all, since if the lock is PROM based, then there can be no "programming" mode (a PROM needs 5 mins of ultraviolet light to erase it, not an electrical impulse). If the lock is RAM based, then some standby power will always be needed, eg: from an internal rechargeable battery and mains supply.

Of course the features indicated are largely dependent on the logic surrounding the EAROM and can be designed to meet individual requirements.

In particular, a lock without the 4 number access (i.e. one only) and with a switch to achieve programmability instead of a "master" code, would use much less peripheral logic. A coded keyboard would also achieve reductions. The diagram shows a breadboarded circuit which could be changed and improved in many ways to meet a particular need.

CIRCUIT DESCRIPTION

The programming control circuit is similar to that shown in Figure 1, with the key difference that this circuit does not simultaneously generate timing signals for erase, write and read. Rather, the basic timing source, IC1, is slowed down during write and erase to provide the required timing.

All power is drawn from a single nine volt battery. To conserve power, no current is drawn unless a key is depressed, turning on Q3. All logic is supplied from the nine volt battery through Q3, the ER2051 is powered from a DC inverter also switched by Q3.

IC1, the master oscillator, in conjunction with IC2, provides the basic timing. IC3 scans through a set of eight addresses (for an eight digit combination). The most significant address Bits, A3 and A4, are encoded from the key switches, allowing a choice of four "combinations" that will open the lock. The "Master" combination in addition places the lock in the program mode, to allow changing any of the combinations.

An incorrect entry locks out the output relay until a power on reset occurs. Since Q1, Q2 together with the 4.7 capacitor provide a 15-20 second power store, an incorrect combination must be followed by a twenty second wait before a new combination may be entered.

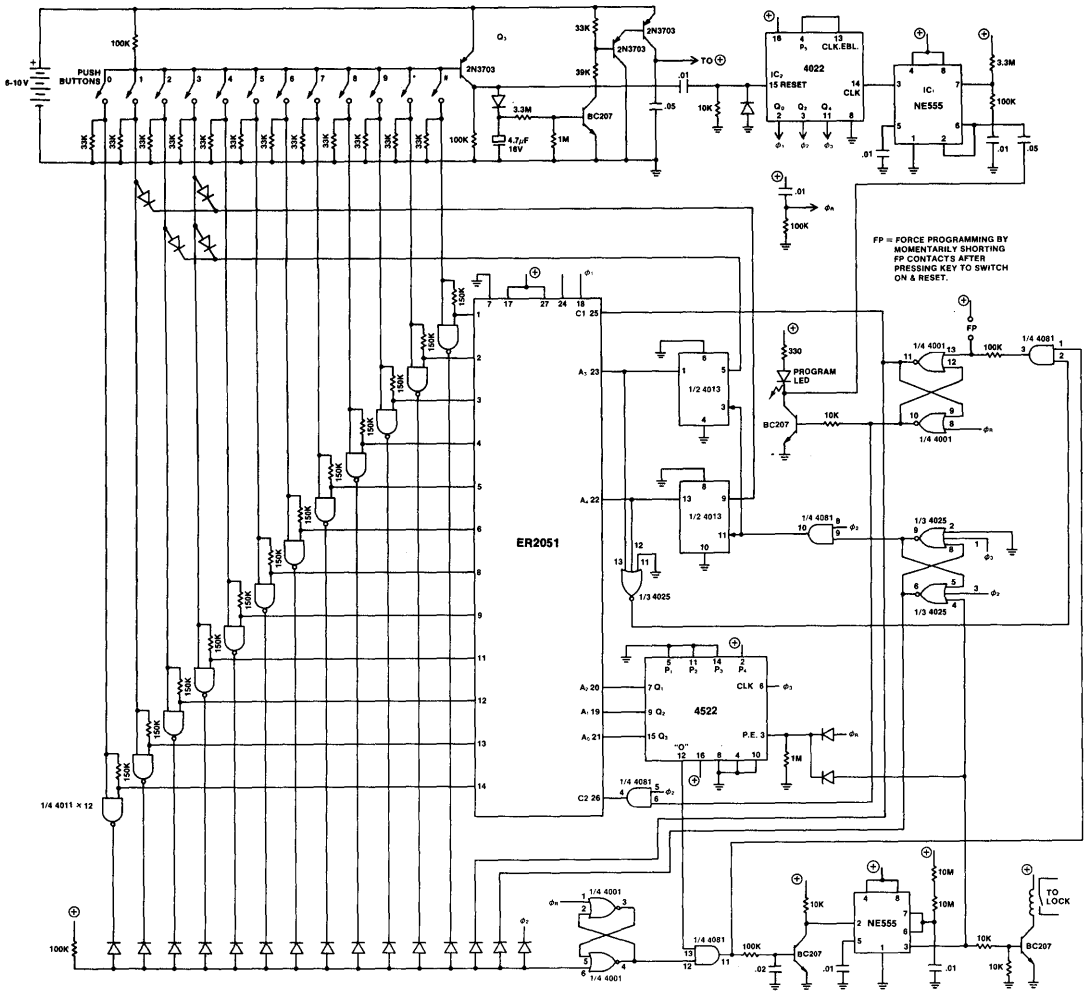
OPERATION

To program initially: Press the "FP" switch (normally hidden in the door). This places the lock in the program mode. Load in the master program, consisting of a "0" followed by an eight digit combination. All subsequent entries of the master code will open the lock and place the lock into the program mode.

To program non-master codes: Enter the master code to place the lock in the program mode. Enter either a 1, 2 or 3 followed by the combination. Three non-master codes may be stored.

To open lock. Key in one of the four combinations. In the event that an incorrect combination is entered, wait 20 seconds, before re-entering the combination. A combination must be preceded by the appropriate key number, either 0, 1, 2 or 3.

Fig.1 EAROM DOORLOCK DEMONSTRATOR



Bulletin 1214

ER1400 — Measuring Data Retention Times

Emyr Edwards

A major advantage of some General Instrument MNOS memories over other non-volatile memory types is the capability they offer to the user of measuring memory threshold voltages and, hence predicting retention times. This application note is intended to describe, in detail, how to take advantage of this built in capability for General Instrument's ER1400 serial Electrically Alterable Read Only Memory.

INTRODUCTION

General Instrument Electrically Alterable Read Only Memories (EAROMs) are based on the P-Channel Metal Nitride Oxide Semiconductor (MNOS) transistor. Charge injected from the silicon substrate by the application of a tunnelling voltage of approximately 30V to the gate is trapped and stored in the Nitride/Oxide interface. A detailed description and explanation of MNOS transistor action appears in another Application Note, Bulletin No. 1201A. Stored positive charge has the effect of making the transistor threshold more negative giving rise to the state known as the WRITTEN state. Conversely, stored negative charge causes a positive shift in threshold, placing the device in the ERASED state.

In much the same way as leakage of charge from a capacitor, the stored charge in a MNOS device decays linearly as a function of log (Time) as shown in the typical Data Retention (Volatility) curves of Fig. 1. V_M is an internally generated reference voltage set at a point between the two thresholds. This V_M, when applied to a MNOS gate, is sufficiently negative to overcome an erased threshold causing flow of current between Drain and Source of an erased transistor, but is more positive than the written threshold so that no conduction occurs in a written transistor. In the ER1400, a written location corresponds to a data logic '0' at the Input/Output port.

At some point in time the written and/or erased windows (defined as the difference between the written or erased threshold and V_M-see Fig. 1) will collapse to a level which is no longer detectable by the on-chip sensing circuitry and erroneous data will appear at the Data Output.

A number of factors affect the initial thresholds and the decay rates of memory transistors:

(a) Number of Erase and Write cycles per address location.

(b) Duration of Erase and Write cycles. The longer the Erase and Write periods used, the greater the stressing of the Silicon Nitride dielectric which results in a reduction in the useful life of the part. Erase and Write times which are too short (less than the minimum specified) may cause incomplete or inadequate erasing or writing with a resultant reduction in memory retention.

(c) High temperature operation has the effect of reducing retention. This is readily understood since retention depends on rate of charge leakage from the Nitride which increases with temperature.

(d) Device fabrication variables also produce differences in memory thresholds and decay rates. ER1400s are 100% tested at zero time (i.e. within seconds of writing the part), stored for 24 hours and again 100% tested for memory retention before shipping. At the 24 hour point, minimum windows are tested for which will ensure extrapolation to greater than 10 years' retention given an empirically determined maximum decay rate.

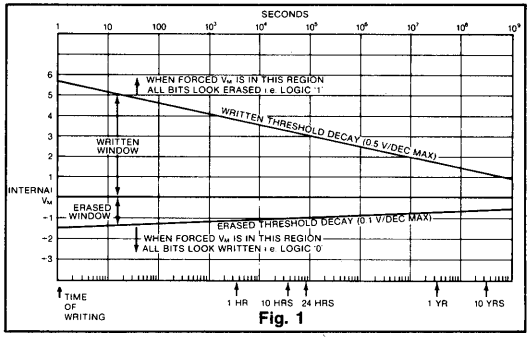


Fig. 1

MEASUREMENT OF MEMORY THRESHOLDS

The principle of the measurement is to start with the internally measured V_M and vary it positively (for erased threshold) or negatively (for written threshold) while constantly reading one location of the memory. At some point, when the forced V_M is slightly more positive than the erased threshold or more negative than the written threshold, both an erased and a written bit will look alike (both will be detected as either a '1' or a '0') and erroneous data will be read.

It is suggested that the erased threshold be measured at a different location to that used for the written threshold. The reason for this is that reading the location repeatedly with a voltage more negative than the internally generated V_M is, in essence, a low energy Write which degrades the thresholds of erased bits in the same memory word. Alternatively, the same address may be used as long as the erased threshold is measured prior to the written.

The measurement procedure then is as follows:

1. With the device powered up, first measure the internal reference voltage, V_M with a voltmeter. This is pin 14 on a 14 pin DIP and pin 2 on a TO-8 package. It's typical value is −9V relative to V_{SS} at $V_{GG} = -35V$.

2. Supply, via the I/O pin, the address of the location to be read as specified by Fig. 1 in the ER1400 data sheet.

3. The selected location is actually read by pulsing the C1 control input to logic '1', keeping C2 and C3 at logic '0' (Fig. 2 of data sheet). This applies the V_M to the selected memory gates, thus detecting the data stored, and then latches the data into the output register.

4. Data is shifted out serially by pulsing C1 and C3 to a '1' (Fig. 3 of data sheet). Thus, a continuous Read + Shift Data Out cycle may be set up and the data train displayed on an oscilloscope. Alternatively, the Data Out may be stored externally and compared with expected data. If it is required to interrogate the complete memory, an extended cycle of "Shift Address In" - "Read" - Shift Data Out" may be set up, the address being incremented at the start of each cycle.

5. The next step is to vary the V_M voltage by applying an external voltage to the V_M pin. Starting at V_M, the voltage at the V_M pin is increased positively or negatively, depending on which threshold is to be measured, while continuously reading the memory. This will overcome the internally generated V_M and force the external voltage onto the gates of the memory transistors.

6. At some voltage, one or more of the data bits will flip into the opposite state (i.e. a '1' becomes a '0' or vice versa).

7. The voltage which causes first failure is the threshold of the memory device at that location and may be plotted as in Fig. 1.

8. Steps 2 through 7 are then repeated after storing the part for a convenient period. The thresholds may be measured at any number of points in time in order to accurately plot the threshold decay. Measurements taken less than 1 hour after writing may be subject to gross errors due to the fact that small errors in measurement time will extrapolate out to give large errors in retention time. Thus, convenient measurement times may be 1 and 10 hours after writing.

All measurements should be made at the same temperature.

Bulletin 1207C

Microprocessor Interfaces To The ER1400 EAROM

Michael French

This application note describes microprocessor interfaces for the ER1400 word alterable non-volatile ROM. Increasingly, one-chip microprocessors or microcontrollers are being used in high volume people oriented systems. The ER1400 is a serial I/O memory which can reliably store occasionally updated data that must be retained when the power is turned off. The ER1400 I/O directly drives MOS/CMOS circuits and can be easily used with most of the popular microprocessors. This application note illustrates ER1400 interfaces to four widely used microprocessors, and shows a variety of interfacing techniques.

The new one-chip microprocessors fill a growing need for low cost microcontrolled systems. In many of these systems the need exists for storing data even when the power is turned off. Such applications include appliance timers, metering pumps, controllers, portable instruments, and data terminals. The data stored may represent cumulative totals, as in a metering system; hardware configuration information, as in a data terminal; or a users program in a hand-held calculator.

The ER1400 with its serial I/O is a natural way to provide this capability. Organized as 100 14-bit words, the ER1400 is an electrically erasable and reprogrammable non-volatile memory. Individual words may be erased and reprogrammed. Once programmed, or written, a word will retain its data for a minimum of ten years.

The ER1400 consists of a memory array, control circuitry, twenty-bit serial to parallel shift register for addressing, and a 14-bit serial to parallel, parallel to serial shift register for data I/O.

In the accept address mode, the address is shifted serially into the ER1400. The address consists of two consecutive one-of-ten codes controlling the "tens" digit and the "units" digit respectively. The Accept Address command may be followed by either Erase, Accept Data, Write (for reprogramming), or Read, and Shift Data Out (for reading).

What makes the ER1400 so ideal for use with the microcomputer is its serial address/data flow. This allows full access to its 1400 data bits with only 5 I/O ports of the microcomputer: one for clocking, three for control, and one for addressing and data flow. A 256×4 1K memory as an alternative would require 8 ports for addressing, four for data and two for control — 14 in all. In effect, the ER1400 can be used as a low-cost peripheral, rather than a buss-oriented memory.

Data is transferred to or from the ER1400 by first serially inputting two ten-bit address words and then serially shifting in or out the fourteen-bit data word. Control of these operations is done by three chip control lines and a 14kHz clock. It is essential that the clock is not interrupted between ACCEPT ADDRESS and SHIFT DATA OUT and between ACCEPT ADDRESS and ACCEPT DATA. Write and erase cycles require a 10 msec delay to guarantee data retention. The four ER1400 to microprocessor interfaces described below show the variety of ways the non-volatile memory may be used.

The first example is the Rockwell single-chip microcomputer, the PPS 4/1. The PPS 4/1 uses a single +15 Volt power supply and is electrically compatible with the ER1400. Figure 1 shows the three ER1400 control lines connected directly to the channel B I/O lines. The fourth channel B output line triggers a 20 millisecond monostable which controls the ERASE/WRITE cycle delays. At the end of these cycles the microprocessor receives an interrupt and turns off the ER1400 cycle.

By using an external timer with an interrupt, the microprocessor is freed to perform other functions during the 20 millisecond delay time.

Timing for the PPS 4/1 is provided by internal clock circuitry operating at 112kHz. Dividing this frequency by 8 provides the 14kHz clock for the ER1400. The ER1400 is only clocked when the microprocessor outputs a control code on channel B. Stopping the 14kHz clock is not necessary, but may be done, after putting the device in standby. In this application, restarting the clock for each operation insures synchronization between the hardware generated clock and the transitions of the software created data and control lines. The bi-directional serial data line on the ER1400 is connected to one of the microprocessor's individual I/O control lines. In this example, external hardware, the CD4098B and CD4520B CMOS I.C.'s, provide the 14kHz clock and 20 msec delay timing. In other examples, these functions are handled by microprocessor software.

The next example shows the Intel 8048 Microcomputer with the ER1400 attached to the 8-bit I/O Port #1. As shown in Figure 2, the 14kHz clock comes from one bit of Port #1 and clock timing is controlled by interrupts from external monostables with a 35.7μs period. Generating the clock signal by microprocessor software does reduce external hardware. Care must be taken to insure no loss of clock pulses if the microprocessor services higher priority interrupts. Level shifting between the five Volt microcomputer and the 15 Volt ER1400 is done by a seven transistor array (RCA CA3081 or equivalent). The 20 millisecond erase/write cycle time period is controlled by the internal timer in the 8048 microcomputer. Output data from the microcomputer comes from bit P/4, while input data goes to pin T_0. P/4 is high when the processor is receiving data.

In the examples above, timing for the 14kHz clock and the 20 millisecond Erase/Write cycle was controlled by hardware. In the next example, (using the General Instrument PIC1650 microcontroller) all timing is controlled by software. The internal oscillator on the chip runs at 1MHz providing an instruction cycle time of 4 microseconds. Thus a programming loop of 18 instruction cycle times can be used to generate the 14kHz clock for the ER1400. The 20 millisecond delay can similarly be generated in software by loading a counter with a large number and decrementing it in a loop until the number becomes zero. An example of this software delay using the PIC1650 is included later in this application note.

Another feature of the PIC1650, and some N-channel microprocessors, is that the 5 Volt logic from the PIC1650 can directly drive the 10 Volt I/O for the ER1400 as shown in Figure 3. The outputs of the PIC1650 can be pulled more positive than the chip's power supply. High level outputs are pulled up, almost to the 10 Volt supply by the 15K resistors, while low levels are pulled to ground by the output transistors on the PIC1650. In Figure 3, bit A4 is high for data or address transfers to the ER1400, and low for data transfers to the PIC1650. Thus the 100K resistor provides a pull-up for data read cycles and adds very little current when the data out from the ER1400 is in a low state. The high impedance data output port from the ER1400 can source 200 microamps in a high state, but can only sink around 10 microamps in the output low state. Thus in Figures 2 and 4, it is necessary to disable pull-up resistors for data read cycles. Complete software subroutines for address formatting and for READ/WRITE are available. The combined routines use 86 instructions.

The final interface is between the ER1400 and the Motorola MC6800 Figure 4. This interface differs from the previous examples in two respects. First, a peripheral interface adaptor PIA is used. Second, the high voltage required for the ER1400 is strobed to conserve power. Both of these features are useful in many applications and could be employed with different microprocessors. The use of the PIA expands the microprocessor's I/O capability by providing additional data lines, and increases its effectiveness by providing I/O buffer latches. Thus the MC6800 can service the ER1400 and several other peripherals simultaneously. The use of power strobing greatly reduces the power requirements especially in battery powered equipment. In normal operation, the ER1400 dissipates 300 milliwatts. If the ER1400 stores data that is only accessed occasionally, significant amounts of power may be saved by strobing its power supply. In Figure 4, an unregulated switching power supply is driven by the same 14kHz clock used for the ER1400. The clock should be initiated 20 milliseconds before the first command is sent to the ER1400. The negative 23 Volts is created by using an audio frequency transformer with turns ratio of 1:2 with 12 Volts on the primary.

The four interface examples should illustrate the ease and variety of ways that the ER1400 electrically alterable ROM can be interfaced to microprocessors. In each application, the designer must make his own decisions about hardware or software for certain functions, like the 14kHz clock. Depending on the trade-off, between hardware costs and software timing, each interface should be tailored to the application requirements.

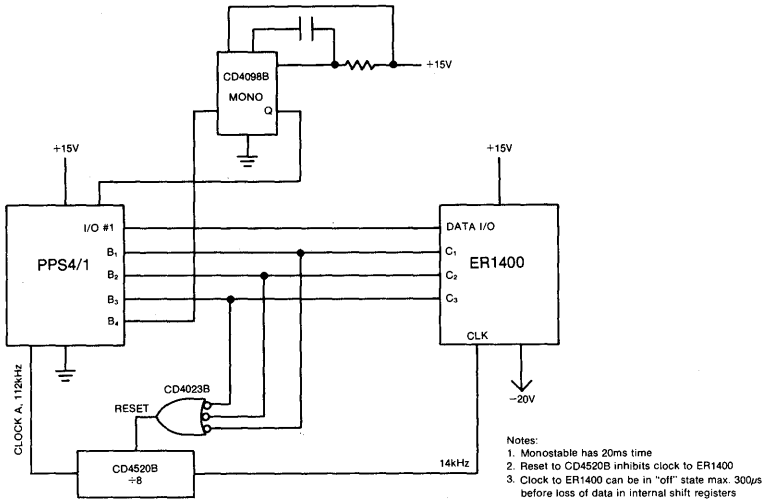


Fig. 1 PPS4/1 TO ER1400 INTERFACE

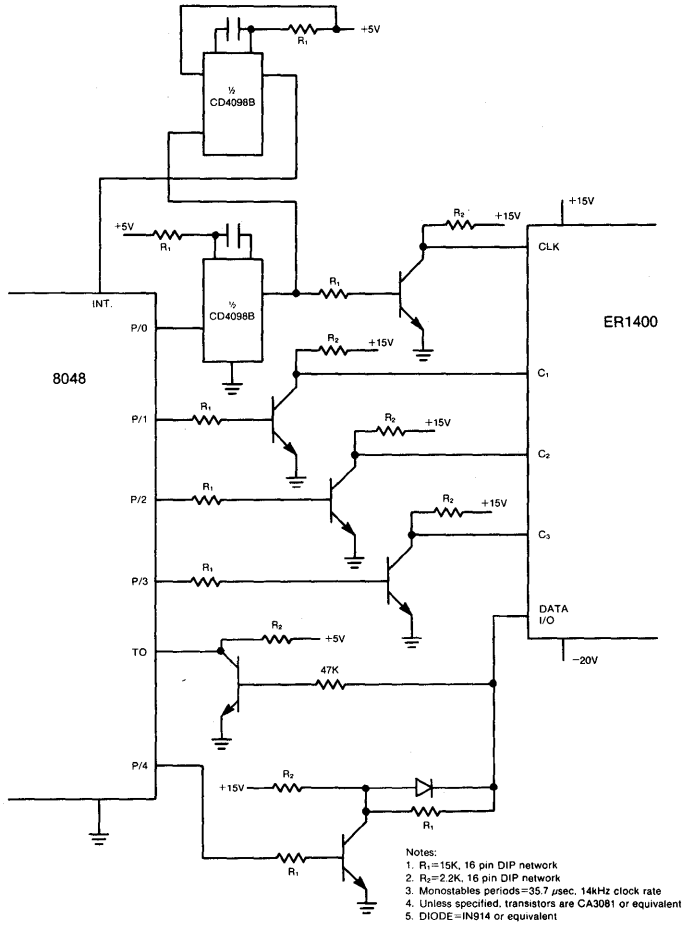
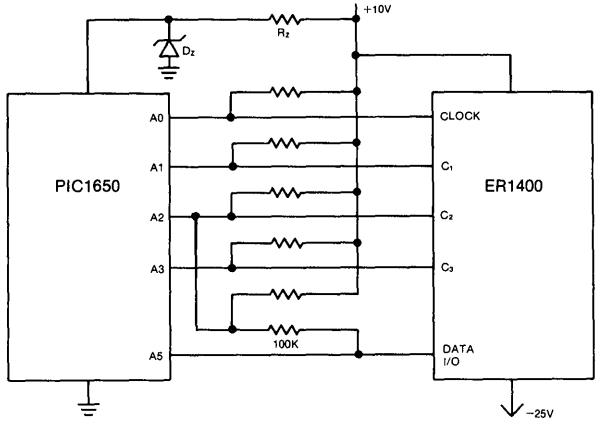
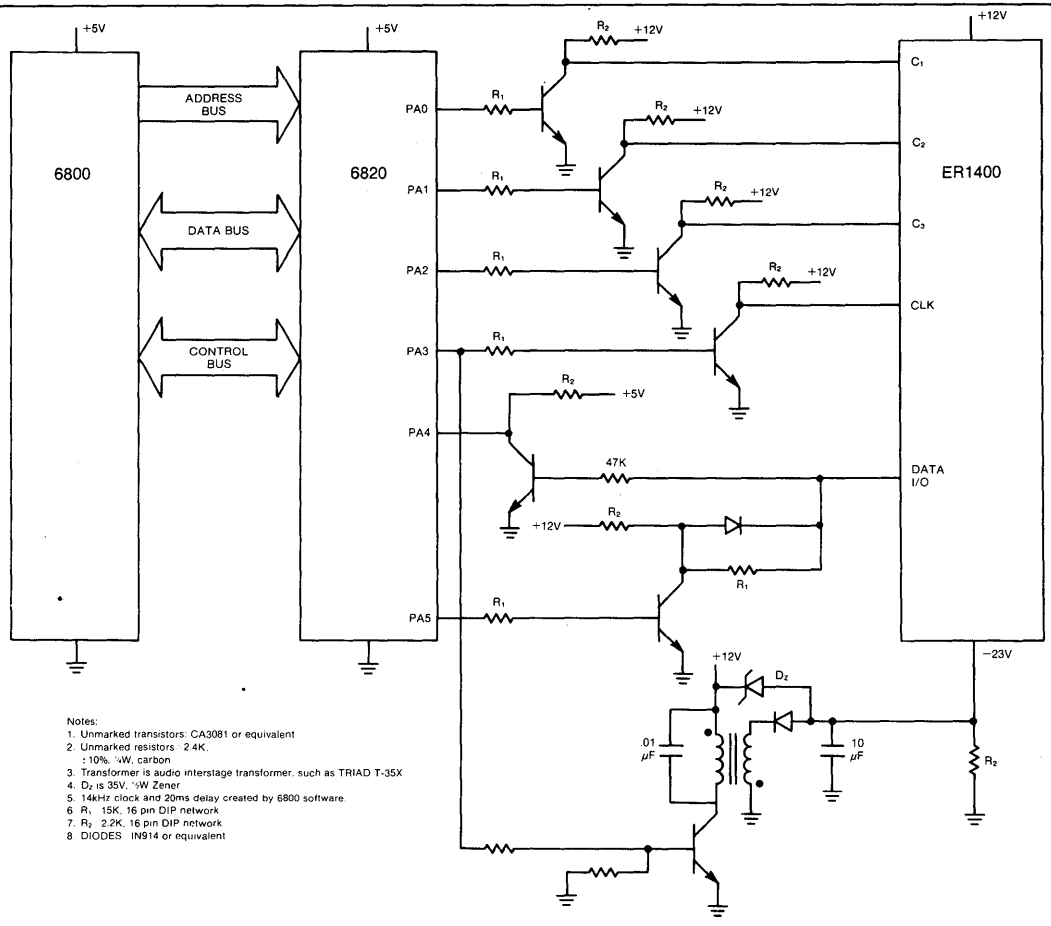


Fig. 2 8048 TO ER1400 INTERFACE



Notes:
1. Internal timing for 14kHz clock and 20ms delay generated by PIC1650 software
2. 300μs max. clock off time between control commands or data transfer clocks
3. Unmarked resistors = 15K.
4. R_z value selected to match 5V Zener diode characteristics
5. PIC1650 uses open collector outputs

Fig. 3 PIC1650 TO ER1400 INTERFACE



Notes:
1. Unmarked transistors: CA3081 or equivalent
2. Unmarked resistors: 2.4K, ±10%, ¼W, carbon
3. Transformer is audio interstage transformer, such as TRIAD T-35X
4. D_Z is 35V, ½W Zener
5. 14kHz clock and 20ms delay created by 6800 software.
6. R_1 15K, 16 pin DIP network
7. R_2 2.2K, 16 pin DIP network
8. DIODES IN914 or equivalent

Fig. 4 6800 TO ER1400 BUFFERED INTERFACE

PIC 1650 SOFTWARE

To show the ease with which the interface lines for the ER1400 may be controlled by microprocessor software, part of the PIC 1650 program is shown below. The PIC 1650 is an 8-bit microcomputer with 512 words of program memory. The software routine in the following uses only 86 words for a complete PIC-ER1400 software interface.

```
                ;PIC - ER1400 INTERFACE SUBROUTINE
                ;
                ;
                ;HARDWARE AS IN APPLICATION NOTE 1207
                ;
                ;PIC & ER1400 WITHIN SPEC FOR PIC FREQ 807-1000KHZ
                ;SUBROUTINE READ OR WRITE IS CALLED BY USERS PROG.
                ;READ 3.4MS          WRITE 40MS (@ 1MHZ NOMINAL)
                ;
                ;ON ENTRY TO READ OR WRITE:
                ;  FILE LOCATN - BITS 0-3 LOW  ADDRESS OF ER1400 (BCD)
                ;                BITS 4-7 HIGH ADDRESS OF ER1400 (BCD)
                ;  FILE DATA1  - DATA REGS:      8 BITS TO/FROM EAROM
                ;  FILE DATA2  -                 6 BITS TO/FROM EAROM
                ;                               (BITS 6-7 DON'T CARE ON
                ;                               WRITE & LOGIC 0 ON READ)
                ;  FILE IOREG  - I/O REGISTER: AT 377
                ;
                ;ON EXIT FROM READ OR WRITE:
                ;  FILE LOCATN - UNCHANGED
                ;  FILE 4      - CHANGED
                ;  FILE DATA1  - CHANGED (BITS 0-7 HAVE DATA IF READ)
                ;  FILE DATA2  - CHANGED (BITS 0-5 HAVE DATA IF READ
                ;                         BITS 6-7 ARE AT LOGIC 0)
                ;
                ;  5 UTILITY FILES ARE REQUIRED AND ARE CORRUPTED
                ;
                ;DEFINE PIC-ER1400 INTERFACE
                ;
                IOREG  EQU     5        ;BIT 0: CLOCK & 15K TO +10V
                                        ;BIT 1: C1 & 15K TO +10V
                                        ;BIT 2: C2 & 15K TO +10V
                                        ;BIT 3: C3 & 15K TO +10V
                ;
                ;
                                        ;BIT 5: DATA I/O
                                        ;BITS 6 & 7: UNUSED. CAN BE I/P
                                        ; ELSEWHERE SINCE SET TO LOGIC 1
                                        ; AT END OF PIC-ER1400 ROUTINE.
                                        ; IF USED AS O/P NOTE THAT THIS
                                        ; ROUTINE SETS THEM TO LOGIC 1.
                                        ;THE ER1400 USES +10V/-25V
                                        ; & THE PIC USES +5V/0V
                LOCATN EQU     .9       ;ER1400 ADDRESS TO BE USED
                DATA1  EQU     .10      ;8 BITS DATA TO/FROM EAROM
                DATA2  EQU     .11      ;OTHER 6 BITS OF DATA
                                        ;DATA1 & DATA2 MUST BE CONSECUTIVE
                ;
                ;DEFINE UTILITY REGISTERS
                ;
                TEMP   EQU     .31      ;UTILITY
                COUNT  EQU     .30      ;UTILITY
                CONAD3 EQU     .29      ;UTILITY:CONVERTED 10 BIT
                CONAD2 EQU     .28      ;UTILITY:ADDRESSES FUNCTIONING
                CONAD1 EQU     .27      ;UTILITY:AS 24 BIT SHIFT REGISTER
                                        ;CONAD1/CONAD3 MUST BE CONSECUTIVE
                ;
                ;READ EAROM ENTRY POINT
                ;
000 4446 READ   CALL    ADEAR    ;ADDRESS ER1400. COUNT LEFT AT 0
001 2436        BSF     COUNT,0  ;SET COUNT TO 1
002 6375        MOVLW   B'11111101';CONTROL CODE FOR READ
                                 ;DATA & CLOCK HIGH.
003 4474        CALL    ERTRAN   ;READ TO DATA REG, COUNT LEFT AT 0
004 2636        BSF     COUNT,4  ;SHIFT OUT 16 BITS (14 PLUS 2 TO
                                 ;NORMALISE DATA TO LOWER
                                 ;6 BITS OF DATA2)
005 6012        MOVLW   DATA1
006 0044        MOVWF   4        ;POINT TO DATA REGS
007 6345        MOVLW   B'11100101';CON CODE FOR SHIFT DATA OUT
010 4474        CALL    ERTRAN   ;SHIFT DATA OUT. LEAVE 77 IN W
011 0553        ANDWF   DATA2    ;ENSURE BITS 6-7 CLEAR
012 6377 EXEAR  MOVLW   B'11111111';CONTROL CODE FOR STANDBY
                                 ;WITH CLOCK BIT SET.
013 0045        MOVWF   IOREG    ;OUTPUT CONTROL CODE
014 4000        RET
                ;
                ;REWRITE EAROM ENTRY POINT
                ;
015 4446 WRITE  CALL    ADEAR    ;ADDRESS THE ER1400
016 6373        MOVLW   B'11111011';CON CODE FOR ERASE
                                 ;DATA & CLOCK HIGH
017 0045        MOVWF   IOREG
020 4436        CALL    W18MS    ;18MS FOR ERASE THEN PUT .14 TO W
021 0076        MOVWF   COUNT    ;SHIFT IN 14 BITS
022 6012        MOVLW   DATA1
023 0044        MOVWF   4        ;POINT TO DATA REGS
024 6361        MOVLW   B'11110001';CON CODE FOR ACCEPT DATA
                                 ;DATA & CLOCK HIGH
025 4474        CALL    ERTRAN
026 6371        MOVLW   B'11111001';CON CODE FOR WRITE
027 0045'       MOVWF   IOREG    ;DATA & CLOCK HIGH
030 4436        CALL    W18MS    ;18MS FOR WRITE
031 5012        GOTO    EXEAR    ;GO TO STANDBY & RETURN
                ;
                ;
                ;SUBROUTINE TO WAIT 18.4MS WHILE CLOCKING EAROM
                ;ON ENTRY FILE COUNT ALWAYS AT ZERO SO IS USED AS FLAG
                ;ENTRY POINT IS AT W18MS
                ;ON EXIT .14 IS LEFT IN W
                ;
032 0645 WMID   XORWF   IOREG    ;INVERT CLOCK O/P
033 3036        BTFSC   COUNT,0
034 4016        RETLW   .14      ;EXIT WITH .14 IN W
035 2436        BSF     COUNT,0
036 0177 W18MS  CLRF    TEMP
037 1377 W36US  DECFSZ  TEMP
040 5042        GOTO    WNZYET
041 5032        GOTO    WMID
042 6001 WNZYET MOVLW   1
043 0645        XORWF   IOREG    ;INVERT CLOCK O/P
044 5045        GOTO    WPAD
045 5037 WPAD   GOTO    W36US
                ;
                ;SUBROUTINE TO CREATE TEN BIT ADDRESSES FOR ER1400
                ; AND AT END TO PREPARE TO GO STRAIGHT INTO ROUTINE
                ; TO TRANSFER TEN BIT ADDRESS TO ER1400
                ;
046 1011 ADEAR  MOVFW   LOCATN   ;GET LOW NIBBLE OF ADDRESS
047 7017 LOADDC ANDLW   17       ;TO LOW NIBBLE OF TEMP
050 0077        MOVWF   TEMP
051 6012        MOVLW   .10      ;NO OF LOOPS BEFORE
052 0076        MOVWF   COUNT    ;THIS ADDRESS PART COMPLETE
053 6001        MOVLW   1        ;DECREMENT FOR ADDRESS
054 0277 ROT3SR SUBWF   TEMP     ;CLRS CARRY IF THIS PART OF ADDRESS
                                 ;HAS NOW REACHED ZERO
055 1573        RLF     CONAD1   ;SHIFT THE 'SHIFT REGISTER'
056 1574        RLF     CONAD2
057 1575        RLF     CONAD3
060 1376        DECFSZ  COUNT    ;,10 SHIFTS DONE YET?
061 5054        GOTO    ROT3SR   ;NOT YET
062 3605        BTFSS   IOREG,4  ;YES. WAS THIS SECOND ADDRESS?
063 5067        GOTO    OPADD    ;YES. NOW OUTPUT CONVERTED ADDRESS
064 2205        BCF     IOREG,4  ;NO. NOW CONVERT HIGH ADDRESS
065 1611        SWAPF   LOCATN,0 ;READY FOR HIGH NIBBLE OF ADDRESS
066 5047        GOTO    LOADDC   ;GO DO HIGH ADDRESS
067 6033 OPADD  MOVLW   CONAD1   ;O/P CONVERTED ADDRESSES
070 0044        MOVWF   4        ;PT TO START OF CONVERTED ADDRESSES
                                 ;3-REGISTER 'SHIFT REGISTER'
071 6024        MOVLW   .20
072 0076        MOVWF   COUNT    ;SET FOR 10 BIT TRANSFER TO ER1400
073 6363        MOVLW   B'11110011';ACCEPT ADDRESS CONTROL CODE
                                 ;DATA HIGH, CLOCK HIGH
                                 ;GO INTO I/O ROUTINE 'ERTRAN'
                ;
                ;
                ;SUBROUTINE TO TRANSFER DATA OR ADDRESS
                ;TO OR FROM ER1400. AT ENTRY REGISTERS HAVE
                ;THE DATA, NUMBER OF ER1400 CLOCK CYCLES OR BITS,
                ;AND ER1400 CONTROL CODE NEEDED.
                ;
                ;ON CALLING SUBROUTINE ERTRAN:
                ;  FILE 4      - POINTS TO START OF INFORMATION FILES
                ;                (CONAD1 IF ADDRESS, DATA1 IF DATA)
                ;  FILE COUNT - NUMBER OF ER1400 CLOCK CYCLES OR BITS
                ;  W          - ER1400 CONTROL CODE
                ;
074 0045 ERTRAN MOVWF   IOREG    ;OUTPUT STANDBY CONTROL WORD
075 6010        MOVLW   .8       ;OUTPUT 8 BITS BEFORE
076 0077        MOVWF   TEMP     ;MOVING TO NEXT INFO FILE
077 2405 STLOOP BSF     IOREG,0  ;SET CLOCK BIT (13.888KHZ 1:1 M/S)
100 3605        BTFSC   IOREG,2  ;DIRECTION CONTROL
101 5107        GOTO    RECEIV   ;INPUT TO PIC FROM ER1400
102 2645 GIVE   BSF     IOREG,5  ;OUTPUT FROM PIC TO ER1400
103 1440        RRF     0        ;ROTATE INFO FILE TO CARRY
104 3403        SKPC             ;TEST DATA TO BE OUTPUT
105 2245        BCF     IOREG,5  ;CLR OUTPUT DATA BIT
106 5114        GOTO    NEXTI
107 2645 RECEIV BSF     IOREG,5  ;ENSURE I/P NOT LATCHED AT 0
110 2003        CLRC             ;INPUT TO PIC. RECEIVE DATA
111 3245        BTFSC   IOREG,5  ;TEST I/P 24US AFTER CLOCK HIGH
112 2403        SETC
113 1440        RRF     0        ;ROTATE CARRY INTO INFO FILE
114 2005 NEXTI  BCF     IOREG,0  ;CLR CLOCK BIT
115 1377        DECFSZ  TEMP     ;DONE 8 BITS YET?
116 5125        GOTO    STPAD    ;NO
117 2577        BSF     TEMP,3   ;SETS TO ,8 SINCE TEMP ZERO
120 1244        INCF    4        ;INCREMENT FSR TO NEXT INFO FILE
121 1376 FINL?  DECFSZ  COUNT    ;DONE ALL EAROM CYCLES?
122 5077        GOTO    STLOOP   ;NO
123 2405        BSF     IOREG,0  ;SET CLOCK AT END
124 4077        RETLW   77       ;END OF SUBROUTINE. 77 LEFT IN W
125 5121 STPAD  GOTO    FINL?    ;PAD
                ;
                ;
```

Bulletin 1209B

EAROMs Replace Mechanical Switches

Michael French

The ER1400 EAROM is being used by CRT terminal makers to replace DIP switches and provide new features. It offers the OEM manufacturer lower cost, reduced parts count and improved reliability, plus the feature of field programming of hardware options.

Now an operator can reconfigure the terminal or test system from the front panel, instead of needing a serviceman to open the unit.

The ER2055 and ER1400 are respectively 8-bit parallel or 1-bit serial access EAROMs that offer the user a choice of system configurations. CRT Terminals, especially "intelligent" terminals, need to store programming or configuration information. Seldom changed, non-volatile information is stored in DIP Switches, UV Proms, RAMs with battery backup and now in EAROMs. To compare EAROMs with other devices, first ask:

- How much data needs to be stored? How many bits? How many DIP switch positions?
- How much does the complete storage function cost? How much does the interface between the DIP switch or RAM and the System cost?
- Would letting the CRT terminal user alter the system configuration or options from the keyboard be an attractive sales feature? Would money be saved by elminating field service calls to reconfigure equipment?
- How would one EAROM replace six DIP switches? Figure 1 shows a typical example comparing the interfaces for the ER2055 and DIP switches to a microprocessor. The four DIP switches hold 32 bits and can be expanded to hold more data by adding more switches and buffers. The ER2055 EAROM ties directly onto an 8 bit bus and provides 512 bits.

Here is an explanation and block diagram showing how the ER1400 or ER2055 can be effectively used in intelligent CRT terminals, and other EDP peripherals or test systems. The recently introduced ER2055 is a 64 word 8-bit parallel I/O EAROM. The ER1400 has the simplicity of 1-bit serial access for both data I/O and addresses. (See Application Note #1207 for microprocessor examples.) The ER2055 has an 8-bit tri-state data bus and 64 words. The ER1400 EAROM holds 100 serial 14-bit words of non-volatile memory. The ER1400 in the 14 pin DIP package, is economical enough for use in systems that only read 8 or 12-bit words. Both EAROMs hold variables that are very seldom changed, such as:

1. Configuration data, which options chosen;
2. System data such as polling or interrupt addresses for addressing a terminal within a large EDP system;
3. Application data such as field control for data input applications. In these applications the EAROMs hold data, controlling the data type and size of data input fields.

In all of these applications the EAROM is competing against DIP switches, UV Proms, or RAM with battery backup. The specific advantages of EAROM against these parts are explained below:

1. EAROM vs. DIP switches.

The advantages are both purchase price and total system cost. DIP switches cost about $2.25 each in volume for eight single pole switches. An "intelligent" CRT terminal requires 6-12 of these packages. One EAROM costs under $4.00 in volume (either ER1400 or ER2055), and the EAROM holds 1400 or 512 bits of data. In addition, the individual DIP switches require much more PC board space and interface circuits, compared to an EAROM which directly interfaces to a microprocessor.

2. EAROM vs. EPROM.

EPROMs are reasonably priced, high density and high speed. Their disadvantage for this application is that they must be removed from the circuit for reprogramming, whereas the EAROM can be reprogrammed, either entirely or a few words, in the circuit.

3. EAROM vs. RAM + battery.

Here the key point is reliability. Batteries do fail, prolonged shelf life lowers their charge. All batteries, except expensive lithium units, only work over limited temperature ranges. The EAROM can operate over the full military temperature range. In addition, the real system cost of RAM plus battery, plus charging circuit is more than the cost of the EAROM.

In summary, the EAROM provides high density, reliability and low cost. The ER1400 serial EAROM is being successfully used in CRT Terminals for exactly these reasons. The 100 14-bit words are economical and easy to serially access. For newer designs, the customer now has a choice of the 8-bit parallel device, the ER2055. This 8-bit by 64 word non-volatile memory directly interfaces to popular microprocessors with 8-bit words. A quick comparison of the two memories is listed below:

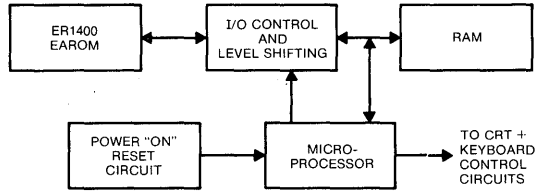
Part	Package	Capacity	I/O	Word Read Time	I/O Voltages
ER1400	14 pin DIP	100 x 14	1-bit Serial	2.5 msec	8-15 Volt Logic
ER2055	22 pin DIP	64 x 8	8-bit parallel	2 μsec	TTL Compatible Logic

Both EAROMs can be reprogrammed up to 10^5 times per word. Their data retention times are greater than 10 years for up to 10^3 Erase/Write operations per word. They can be read up to 10^{11} times per word before needing rewriting of that word.

Because of the great differences in total time to read a word, the ER1400 is generally read into a buffer RAM for high speed access, while the ER2055 is tied directly to a microprocessor.

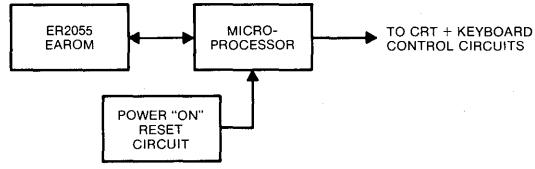
BLOCK DIAGRAM OF EAROM APPLICATION IN CRT TERMINALS

A. ER1400 SERIAL DATA I/O USING RAM



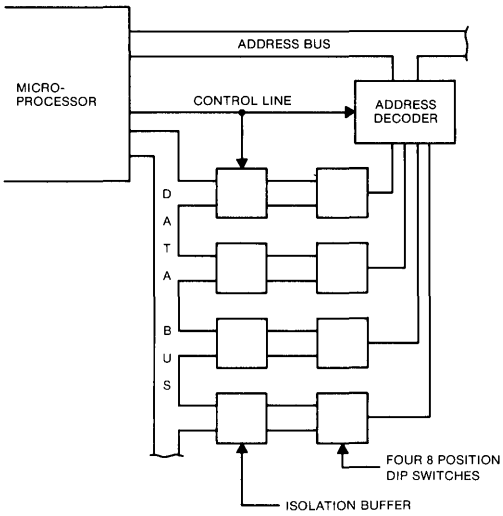
1. ER1400 Read during power on sequence. Data stored in RAM for fast READ access
2. Control I/O + level shifting circuits handle clock generation and data transfer.

B. ER2055 8-BIT PARALLEL DATA I/O



1. ER2055 can be READ at power start up or during system operation (2 microsecond Read access time).
2. 8-bit parallel tristate data I/O bus to EAROM may be data bus for other devices.
3. Control and strobe lines from microprocessor, 5 Volt logic.

A. MICROPROCESSOR TO DIP SWITCH INTERFACE: 32 BIT CAPACITY



B. MICROPROCESSOR TO ER2055 EAROM INTERFACE: 512 BIT CAPACITY

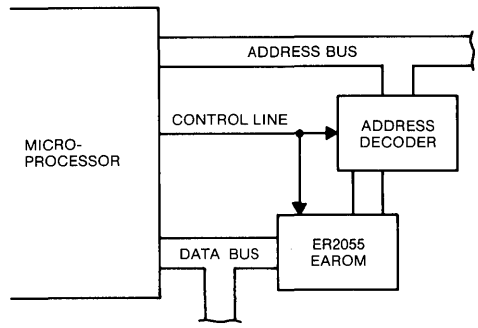


Fig. 1

Bulletin 1221

ER2055 Benchtop Programmer

Joseph J. Spadaro
Steven J. Glica

This circuit fills the need for a manual benchtop programmer. It will enable the user to become familiar with the operation of the ER2055 prior to designing it into a prototype circuit. The TTL control circuit is low cost and allows the user to erase, write, and read any desired data pattern.

The ER2055 is a fully decoded, word alterable, non-volatile memory device. It is organized in a 64 x 8 configuration.

THEORY OF OPERATION

The circuit described in this note is designed to erase or write one or all 64 bytes of memory by depressing the START button. See Figure 1. The data word D_0 to D_7 is presented to the ER2055 via the eight switches SD_0 to SD_7. Memory address and EAROM operating mode are then selected and the START button is depressed. The binary counters IC-11, 12 address each memory location and allow either sequential addressing through all 64 memory locations or individual memory word addressing. The circuit's master timing is selected via the logic configuration of IC-1 and the switch setting of C-1. The 2MHz external clock signal is applied when C-1="1", otherwise, the on-board 100Hz clock is used. These signals represent the MASTER CLOCK pulses which are applied to the 74193 binary counter, IC-9 through the gating of IC-2. The counter drives a 4 to 16 decoder, IC-10 which decodes four binary inputs into one of sixteen mutually exclusive outputs, t_0 to t_{15}. These inputs provide the timing basis for an easy and trouble-free method of generating the necessary timing signals for the ER2055.

The pulse from t_0 of IC-10 is used to load the address selected from switches SA_0 to SA_5. When the "ADDRESS MODE" switch is in the "LOAD 64" position, the load pulse is blocked by IC-5 and the pulse from t_2 is allowed to increment the address counters.

Chip select signals CS_1 and CS_2 are generated next. IC-17B is preset by the pulse from t_4 and cleared by the pulse from t_{15}. When CS_1 is held low, all inputs to the device are tri-stated, and thus enabling and disabling the CS_1 input during each tester cycle ensures that the ER2055 is in a particular mode only for a specified length of time.

The CLK pulse is required only during the read mode and is generated by IC-17A which is preset by t_5 and cleared by t_9. Following a clock pulse, the data on output lines D_0-D_7 becomes valid for 1 msec and therefore must be latched. This is accomplished by flip flops IC-13-16 which are clocked by the pulse from t_{14}.

With the "ADDRESS MODE" switch in the "1" position, the pulse generated by t_{15} is used to reset the circuit; if in the "64" position, the reset pulse is generated by gating the address counter outputs A_0 and A_6.

OPERATING PROCEDURE

To exercise the EAROM in each of its three modes of operation, proceed as follows:

Erase Mode

See Figure 2. Before writing new data into an 8 bit memory location, an ERASE cycle is required, which preconditions each memory cell within the selected location. When an ERASE cycle is desired, set the mode switches C1=0 and C2=1. The address mode switch must also be set to either '1' or '64'. When set to the '1' position, the particular memory location to be addressed is represented by switches SA_0 thru SA_5. The settings of the DATA SELECT and DATA WORD switches (SD_0-SD_7) are not critical due to the fact that data is neither being written into, nor read out of the ER2055.

Write Mode

See Figure 3. When a WRITE cycle is desired, set the mode switches C1=0 and C2=1. Again, the address mode switch must also be set to either '1' or '64'. The DATA SELECT switch should be set at 'IN' in order that the DATA WORD, which is set through switches SD_0-SD_7, can be written into the ER2055.

Read Mode

See Figure 4. When a READ cycle is desired, set the mode switches C1=1 and C2=0. The address mode switch must be set to '1' in order that a particular memory location can be read. The DATA SELECT switch should be set to the 'OUT' position so that the data appearing on I/O pins (D_0-D_7) can be latched. Since a READ cycle is being performed, the position of the DATA WORD switches (SD_0-SD_7) is not critical.

PARTS LIST

Part Number	Description
IC 1-5	7400
IC 6, 7	7414
IC 8	74LS240
IC 9, 11, 12	74LS193
IC 10	74154
IC 13-17	7474
IC 18	555

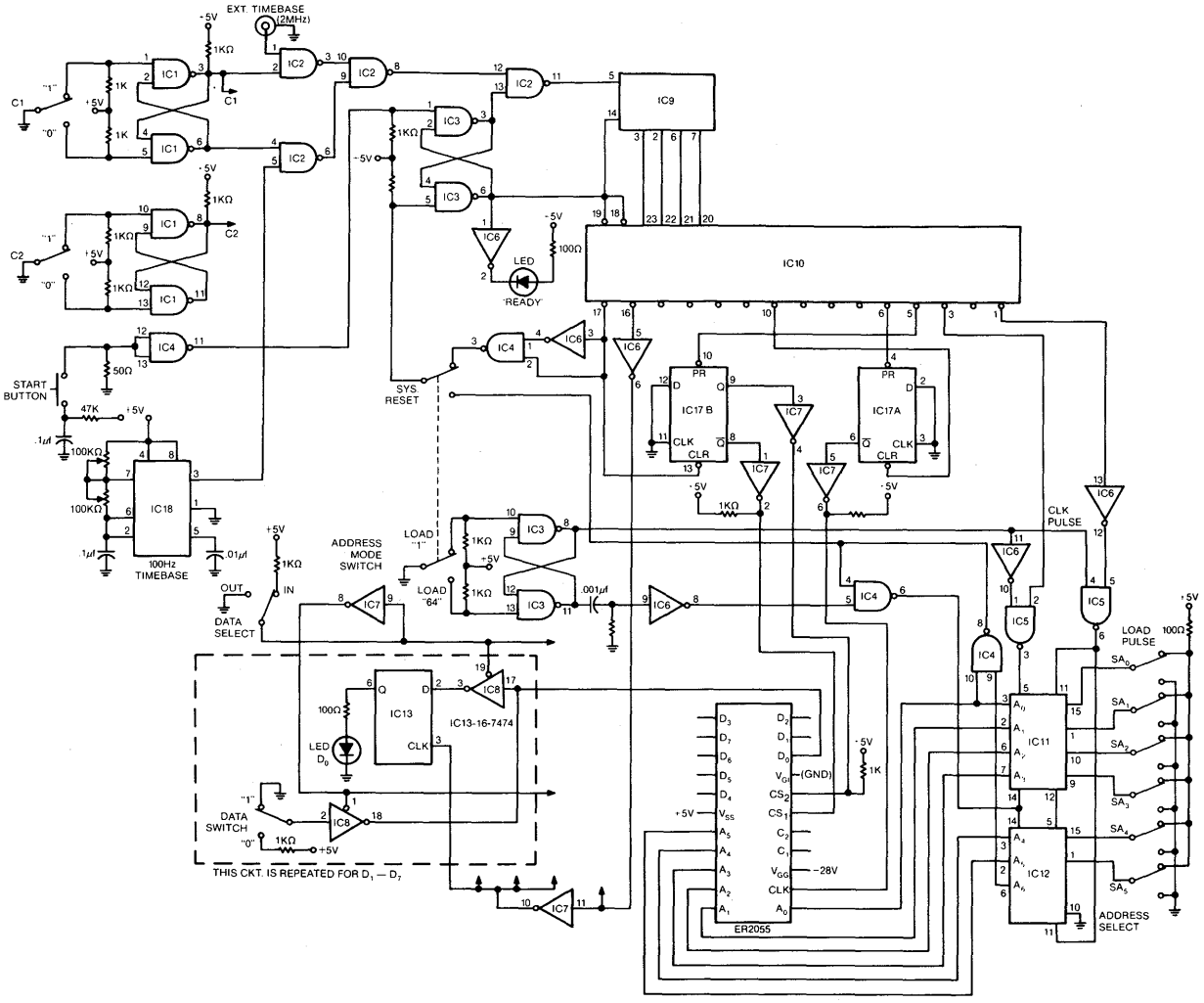

EXT. TIMEBASE (2MHz)
+5V
1KΩ
IC1
IC2
IC3
IC4
IC5
IC6
IC7
IC8
IC9
IC10
IC11
IC12
IC13
IC17 B
IC17A
IC18
C1
"1"
"0"
1K
C2
1KΩ
50Ω
START BUTTON
47K
.1μf
100KΩ
1μf
100Hz TIMEBASE
.01μf
OUT
IN
DATA SELECT
SYS. RESET
LED
"READY"
100Ω
ADDRESS MODE SWITCH
LOAD "1"
LOAD "64"
.001μf
CLK PULSE
LOAD PULSE
IC13-16-7474
DATA SWITCH
THIS CKT. IS REPEATED FOR $D_1 - D_7$
ER2055
(GND)
-28V
ADDRESS SELECT

Fig. 1

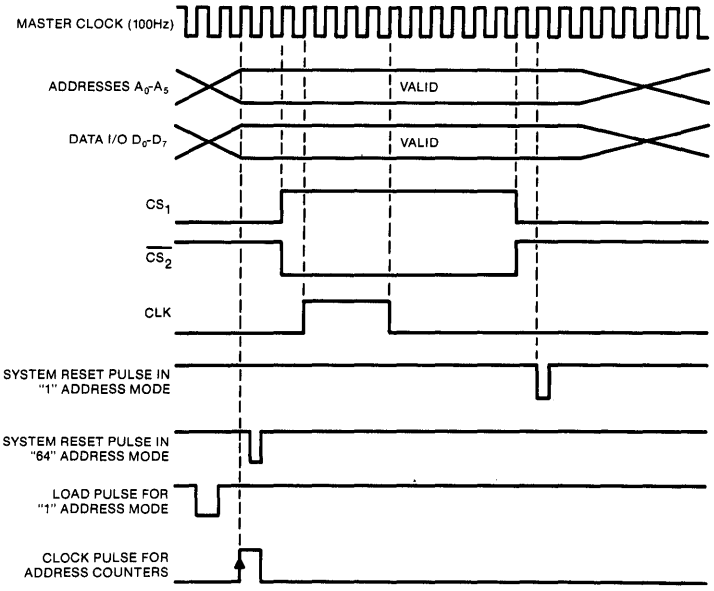


Fig. 2 ERASE MODE

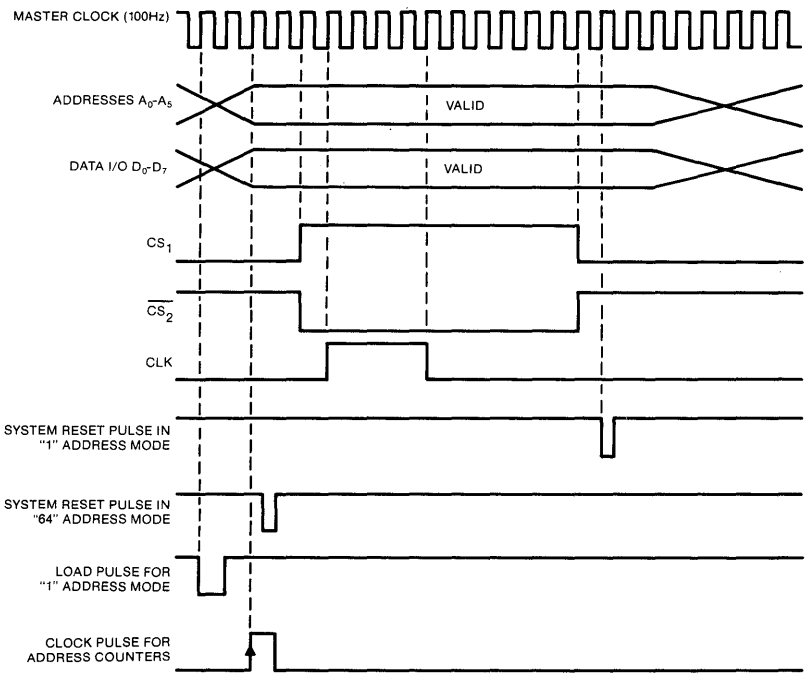


Fig. 3 WRITE MODE

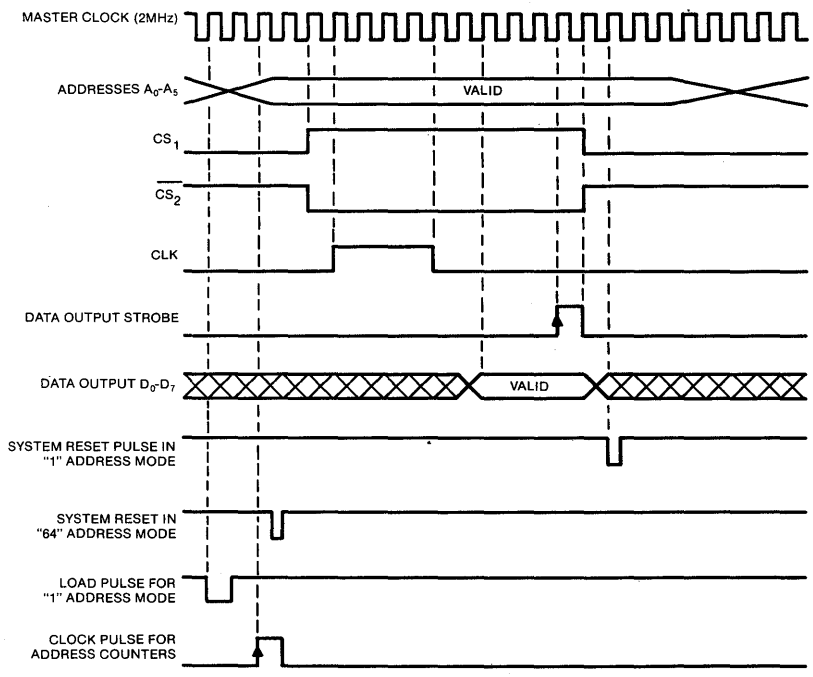


Fig. 4 READ MODE

Bulletin 1222

Measuring Data Retention of the ER0082

Emyr Edwards

The length of time that data may be retained in a non-volatile memory is a crucial parameter to the system designer. Many of General Instrument's EAROM devices incorporate circuitry which enables this parameter to be measured. The method for doing this for the ER0082 is described in this application note.

INTRODUCTION

General Instrument Electrically Alterable Read Only Memories (EAROMs) are based on the P-Channel Metal Nitride Oxide Semiconductor (MNOS) transistor. Charge injected from the silicon substrate by the application of a tunnelling voltage of approximately 30V to the gate is trapped and stored in the Nitride/Oxide interface. A detailed description and explanation of MNOS transistor action appears in another Application Note, Bulletin No. 1201A. Stored positive charge has the effect of making the transistor threshold more negative giving rise to the state known as the WRITTEN state. Conversely, stored negative charge causes a positive shift in threshold, placing the device in the ERASED state.

In much the same way as leakage of charge from a capacitor, the stored charge in a MNOS device decays linearly as a function of log (Time) as shown in the typical Data Retention (Volatility) curves of Fig. 1. V_M is an internally generated reference voltage set at a point between the two thresholds. This V_M, when applied to a MNOS gate, is sufficiently negative to overcome an erased threshold causing flow of current between Drain and Source of an erased transistor, but is more positive than the written threshold so that no conduction occurs in a written transistor. In the ER0082, a written location corresponds to a data logic '0' at the Input/Output port.

At some point in time the written and/or erased windows (defined as the difference between the written or erased threshold and V_M-see Fig. 1) will collapse to a level which is no longer detectable by the on-chip sensing circuitry and erroneous data will appear at the Data Output.

A number of factors affect the initial thresholds and the decay rates of memory transistors:

(a) Number of Erase and Write cycles per address location.

(b) Duration of Erase and Write cycles. The longer the Erase and Write periods used, the greater the stressing of the Silicon Nitride dielectric which results in a reduction in the useful life of the part. Erase and Write times which are too short (less than the minimum specified) may cause incomplete or inadequate erasing or writing with a resultant reduction in memory retention.

(c) High temperature operation has the effect of reducing retention. This is readily understood since retention depends on rate of charge leakage from the Nitride which increases with temperature.

(d) Device fabrication variables also produce differences in memory thresholds and decay rates. ER0082s are 100% tested at zero time (i.e. within seconds of writing the part), stored for 24 hours and again 100% tested for memory retention before shipping. At the 24 hour point, minimum windows are tested for which will ensure extrapolation to greater than 10 years' retention given an empirically determined maximum decay rate.

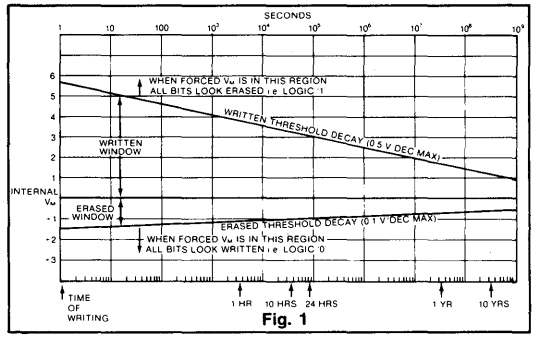


Fig. 1

MEASUREMENT OF MEMORY THRESHOLDS

The principle of the measurement is to start with the internally measured V_M and vary it positively (for erased threshold) or negatively (for written threshold) while constantly reading one location of the memory. At some point, when the forced V_M is slightly more positive than the erased threshold or more negative than the written threshold, both an erased and a written bit will look alike (both will be detected as either a '1' or a '0') and erroneous data will be read.

The measurement procedure then is as follows:

1. With the device powered up, first measure the internal reference voltage, V_M. This is pin 12, marked TEST and its value will be typically −8.5V relative to V_{SS} under nominal voltage conditions.

2. Set up the memory address to be measured.

3. Make the Set 1 and Set 0 lines high, as described in the timing diagrams for a Read operation, and continuously pulse the $\overline{CS}$ line, i.e., put the chip into a continuous Read mode. Note that the minimum Read cycle time is 130μs, so that the $\overline{CS}$ input frequency should be adjusted accordingly. Monitor the Data Out pin (pin 13) constantly.

4. The next step is to vary the V_M voltage by applying an external voltage to the V_M pin. Starting at V_M, the voltage at the V_M pin is increased positively or negatively, depending on which threshold is to be measured, while continuously reading the memory. This will overcome the internally generated V_M and force the external voltage onto the gates of the memory transistors.

5. At some voltage, one or more of the data bits will flip into the opposite state (i.e. a '1' becomes a '0' or vice versa).

6. The voltage which causes first failure is the threshold of the memory device at that location and may be plotted as in Fig. 1.

7. Steps 2 through 6 are then repeated after storing the part for a convenient period. The thresholds may be measured at any number of points in time in order to accurately plot the threshold decay. Measurements taken less than 1 hour after writing may be subject to gross errors due to the fact that small errors in measurement time will extrapolate out to give large errors in retention time. Thus, convenient measurement times may be 1 and 10 hours after writing.

All measurements should be made at the same temperature.

Bulletin 1224

The ER5901: Designer's Choice for Low Cost Small Memory Applications

Joseph J. Spadaro

Would a few bytes of non-volatile memory enhance your product? The self-programing ER5901 will store up to 128 bytes, requires no special interfacing circuitry or power supplies and, best of all, is cheaper to use than the devices it replaces.

In recent years, a number of new uses have arisen for EEPROMs with bit densities of less than 1024 bits. Some of these new applications are:

1. Channel selection in cable TV tuners.
2. Settings for microwave ovens.
3. Storage of instrument calibration constants.
4. Intelligent controllers.
5. Look-up table storage in frequently updated point-of-sale terminals (such as gasoline pumps).
6. Home appliances with programable cycles (such as washing machines).
7. Electronic security systems.
8. Automobile odometers.
9. DIP switch replacement in terminals.

System designers have placed ease of use and low cost at the forefront of their non-volatile memory requirements. Consequently, "smart" memories will occupy the greatest number of sockets in new designs. To be classified as a "smart" memory a EEPROM must:

1. Operate from a single +5V power supply in all modes.
2. Have on-chip latches to capture the addresses and data.
3. Have a self-timed automatic erase/write cycle on-chip.

The General Instrument ER5901 contains all three features, and operates from either separate or multiplexed address and data lines.

ER5901 VS DIP SWITCHES

Let's look at one particular application—DIP switch replacement in CRT terminals—to highlight the advantages of using the ER5901.

To the delight of terminal manufacturers, the number of CRT terminals in homes, businesses, offices, airports, etc. is increasing around the world. Worldwide usage, however, places special demands on the CRT controllers which are called upon to accommodate a wide variety of languages, processing speeds and transmission protocols. Therefore, configuration of the terminal attributes must be made flexible, that is, programable, to satisfy the needs of each individual user. The most prevalent solution to this problem has been to incorporate one or more DIP switches within each CRT terminal. Typically, the switches are located just below a small, removable access panel on the terminal console. Field service personnel can then remove the panel and reconfigure the terminal attributes by changing the settings of the DIP switches. The major disadvantage of this scheme is the high cost of OEM field service calls—at least $100 an hour. Now let's compare the cost of using DIP switches with the cost of using one ER5901.

TYPICAL DIP SWITCH INTERFACE

Figure 1 shows the requirements for interfacing one or more 8 pole, double throw DIP switch packages with the popular 8085 microprocessor. An octal buffer (74LS240) and 8 resistors are required for any quantity of switches tied together in the same system. Each DIP switch pack is selected by a logic 0 on the decoder output. Closed switches are read as a logic 0 and open switches are read as a logic 1 due to the pull-up resistors. When more than one DIP switch pack is used, the unselected switch packs are isolated by diodes.

In the following analyses, N will be used to represent the number of DIP switch packs per system.

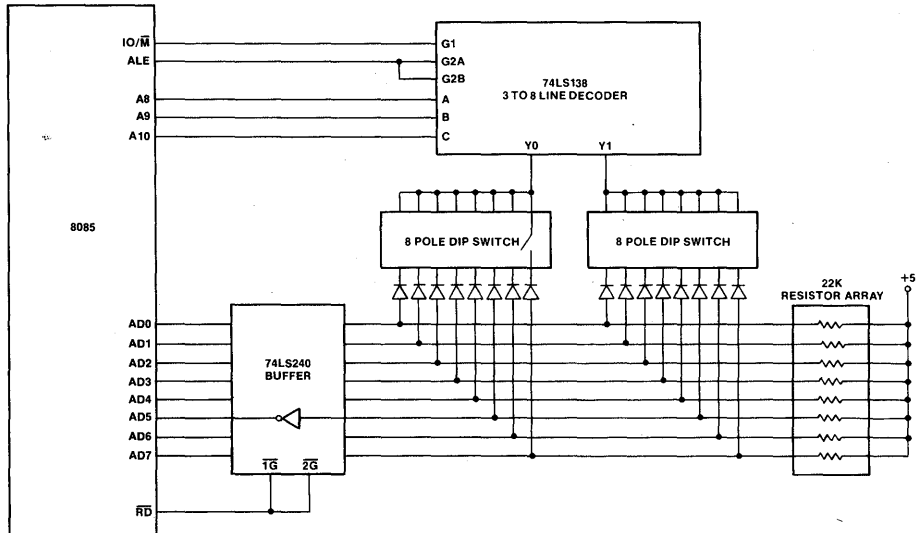


Fig. 1 DIP SWITCH TO 8085 INTERFACE

HOW MUCH DOES IT COST?

The cost of using any component in a system includes the purchase price of the component itself as well as the cost of assembling each component into the system. The assembly costs listed include incoming inspection, handling, inventory, board real estate and insertion. Component costs quoted are based on 10,000 piece prices.

The system costs are calculated as follows:

Device	Qty.	Component Cost ($)	Assembly Cost ($)
Dip Switch	1	1.00	1.00
Resistor Array	1	.32	1.00
Buffer (74LS240)	1	.50	1.00
Decoder (74LS138)	1	.60	1.00
Subtotal		$2.42	$4.00

Total Cost = Equipment Cost + Assembly Cost = $6.42

Conclusion: The cost of interfacing one DIP switch to an 8085 microprocessor is $6.42. The cost per switch is $6.42 divided by 8 = $0.80.

HOW MUCH DOES IT REALLY COST?

When more than one DIP switch pack is used, only one 8-resistor array and one 74LS240 buffer are needed; that is to say their cost is non-recurring. Recurring costs are associated with the additional DIP switch packs and diode arrays.

The cost of a system using more than one DIP switch pack is calculated as follows:
Recurring Costs + Non-Recurring Costs = TOTAL COST
($3.65) N + $4.42 = TOTAL COST

Device	Qty.	Component Cost ($)		Assembly Cost ($)		Recurring Costs ($)	Non-Recurring Costs ($)
8 Pole DIP Switch Pack (Recurring)	1	1.00	+	1.00	=	2.00	—
Diode Array (Recurring)	1	.65		1.00		1.65	—
Decoder (Non-Recurring)	1	.60		1.00		—	1.60
Resistor Array (Non-Recurring)	1	.32		1.00		—	1.32
Buffer (Non-Recurring)	1	.50		1.00		—	1.50
Subtotals:						$3.65	$4.42

Device	Qty.	Component Cost ($)	Assembly Cost ($)	Equipment & Assembly ($)
ER5901	1	4.94	1.00	5.94
7400	1	.15	1.00	1.15
				7.09

N	Total Cost ($)	Cost Per Bit ($)
1	7.09	.007
2	7.09	.007
3	7.09	.007
4	7.09	.007
5	7.09	.007
6	7.09	.007
7	7.09	.007
8	7.09	.007

Conclusion: The cost of replacing up to eight DIP switch packs with one ER5901 is $7.09; the cost per bit is $7.09 divided by 1024 = $0.007.

THE BOTTOM LINE

The following table highlights the system cost savings that result from using the ER5901:

N	DIP Switch		ER5901	
	Total ($)	Cost Per Switch ($)	Total ($)	Cost Per Bit ($)
1	6.42	.80	7.09	.007
2	11.72	.73	7.09	.007
3	15.37	.64	7.09	.007
4	19.02	.59	7.09	.007
5	22.67	.57	7.09	.007
6	26.32	.55	7.09	.007
7	29.97	.54	7.09	.007
8	33.62	.53	7.09	.007

As shown above, the ER5901 is almost five times more effective than eight DIP switch packages. Even at one DIP switch pack the increased flexibility of the ER5901 and its low cost makes it a cost effective alternative. Additionally, customers using the ER5901 will benefit from:

1. A simplified microprocessor interface
2. Increased system flexibility and memory capacity
3. Keyboard and remote programing
4. Downline loading of CRT configuration data
5. Elimination of DIP switch access panels and field service reprograming costs
6. Denser board designs
7. Improved reliability

The General Instrument ER5901 is indeed a "smart" memory.

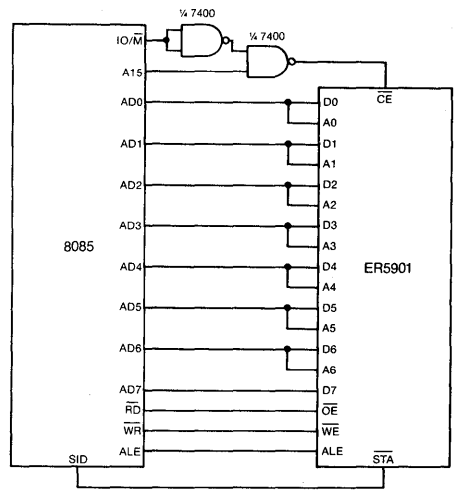


Fig. 2. ER5901 TO 8085 INTERFACE

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