GENERAL INSTRUMENT

MOS DATA 1976

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GENERAL INSTRUMENT CORPORATION

MOS DATA 1976

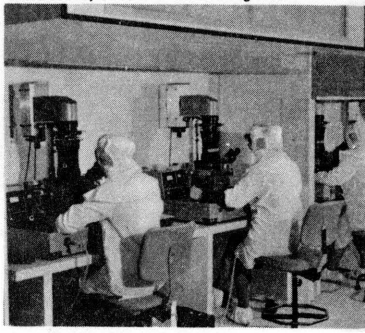
MOS DATA 1976 ■ SECTIONS

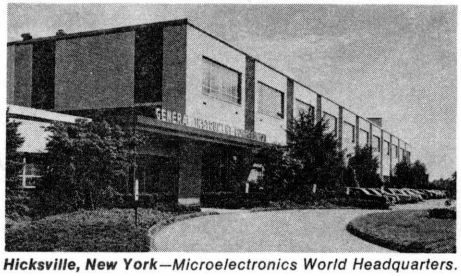
GENERAL INSTRUMENT MICROELECTRONICS

A TOTAL TECHNOLOGICAL SERVICE

***Hicksville, New York**—Test area.*

***Glenrothes, Scotland**—Mask Aligners.*





***Hicksville, New York**—Microelectronics World Headquarters.*

General Instrument Microelectronics is one of the world's leading manufacturers of MOS (metal oxide semiconductor) LSI (large scale integration) products. A pioneer in MOS/LSI in 1966, General Instrument is now a worldwide supplier of volume microelectronic products.

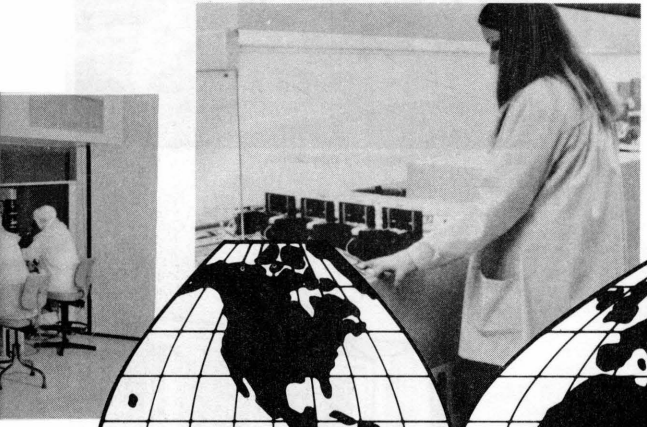
GI has facilities in every major market, providing customers with the full spectrum of services: new product development... applications engineering support... circuit manufacturing.

Strategically Located Plants

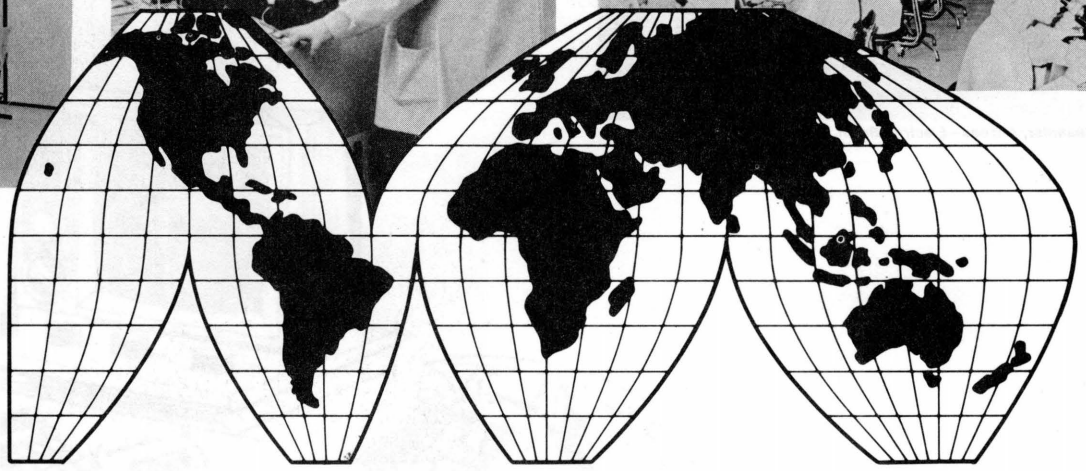
General Instrument operates four production facilities in the United States, Europe and the Far East. The plants at Glenrothes, Scotland; Chandler, Arizona and Hicksville, New York have full capability for design, mask making, diffusion, assembly, test and quality assurance. The factory in Kaohsiung, Taiwan is specifically set up for high volume assembly, test, quality assurance and Far East applications assistance.

In addition to providing nearby sources of supply on three continents, each plant has a backup facility designated as an in-house second source to insure uninterrupted delivery. Common processes and equipment are employed and major product styles are always produced in at least two separate locations. To maintain uniform standards from plant to plant, the quality assurance group at each facility reports to a worldwide quality assurance director.

Chandler, Arizona—*Wafer Coating.*



Kaohsiung, Taiwan—*Assembly operation.*



Because General Instrument has a comprehensive exposure to the world MOS market, it has been able to structure its facilities to conform to evolving customer needs. Production capabilities are concentrated in product areas of greatest volume. Furthermore, cost effectiveness is enhanced because import duties are saved on locally manufactured products.

Broad Product Lines

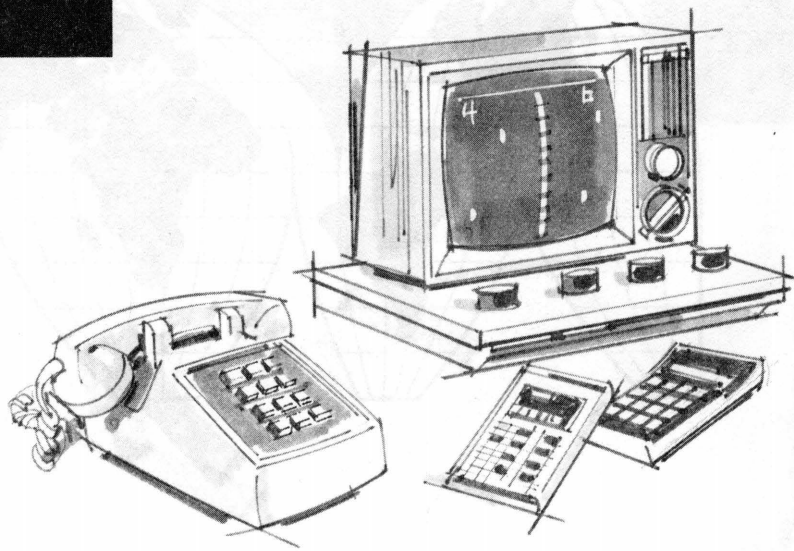
General Instrument Microelectronics offers the widest range of standard LSI circuits in the industry. The company's off-the-shelf microcircuit portfolio consists of over 200 different MOS/LSI devices for a diversity of markets: consumer, calculator, tele-communications, and data management.

Chandler, Arizona—*Electron Beam Evaporation.*

As a leading supplier of consumer microelectronics, General Instrument manufactures MOS/LSI circuits for clocks, clock radios, TV tuners, remote control, appliance timers, radio and high fidelity systems. GI is a leading supplier of LSI for video games; the AY-3-8500 was the first single chip LSI product to provide six different games with on-screen scoring and realistic sound.

General Instrument is the largest independent manufacturer of microcircuits for hand held and printing calculators. The product selection ranges from the basic functions to advanced scientific and printing calculator LSI.

Glenrothes, Scotland—*Assembly operation.*



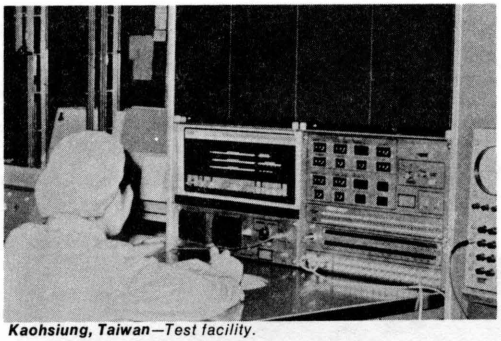
As an outgrowth of General Instrument Corporation's long experience in telecommunications, GI Microelectronics has introduced a series of standard telephone circuits for use in the conversion of telephone apparatus from electromechanical to all-electronic operation. These circuits are being sold to the independent producers of telephone equipment around the world.

This catalog not only contains an extensive range of products but offers the widest choice of circuits within each specific family. Note, for example, the microprocessor and memory product line. In addition to supplying ROMs and RAMs, General Instrument Microelectronics has introduced a major new product style. It's the EAROM, or electrically alterable ROM, which combines the reprogrammability of the RAM with the non-volatility of the ROM. Further, GI's 4K Static RAM is particularly suited for use with microprocessors for data terminals and telecommunications.

The CP1600 Microprocessor, which General Instrument developed jointly with Honeywell, is the world's most powerful 16 bit microprocessor. For the first time, the logic byte size, or computing power, of mini-computer hardware is made available in a single chip of silicon.

Continuing Cost Effectiveness

General Instrument helps you to compete. Our high volume orientation, coupled with aggressive cost reduction, has made



***Kaohsiung, Taiwan**—Test facility.*

possible products previously beyond the reach of the everyday consumer. The GI Mini-Pak, introduced for calculator and consumer products, provides a further saving in labor and material for the GI Microelectronics customer.

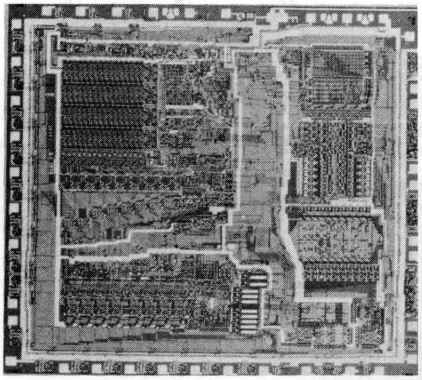
Advanced Design Centers
MOS design and development centers are maintained at Glenrothes, Scotland; Hicksville, New York and Chandler, Arizona. Research and development for new processes and products are conducted at each of these locations.

Custom Design Services
In addition to its extensive catalog of standard products, General Instrument Microelectronics provides custom design services to satisfy specific customer requirements. In some cases, the custom application is best served by software or firmware programming of a standard microprocessor. In other cases, a custom chip layout is more cost effective. These services may be arranged through any of the Microelectronics sales offices.

Applications Assistance Around the Globe
To provide the special applications assistance that customers may require, General Instrument Microelectronics maintains fully staffed Applications Centers at strategic locations around the world...

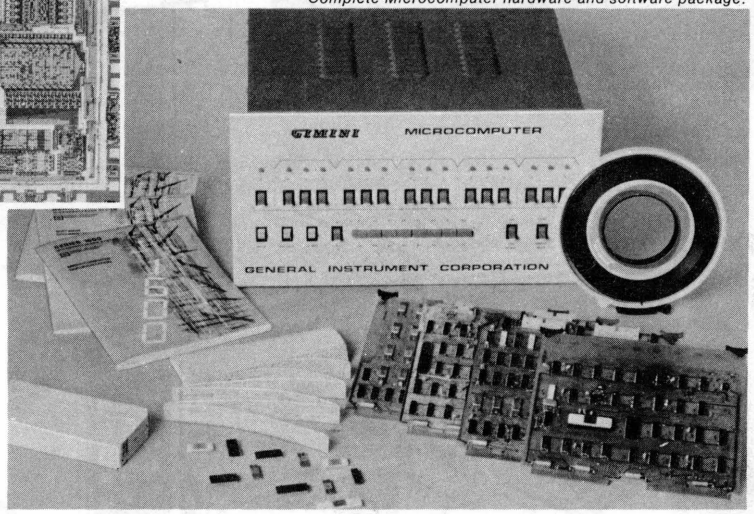
U.S.A.—Hicksville, New York / Chandler, Arizona

EUROPE—Glenrothes, Scotland / London, England / Munich, Germany



Microphoto of CP1600 Microprocessor chip.

Complete Microcomputer hardware and software package.



ASIA—Kaohsiung, Taiwan / Tokyo, Japan / Hong Kong

SOUTH AMERICA— Sao Paulo, Brazil

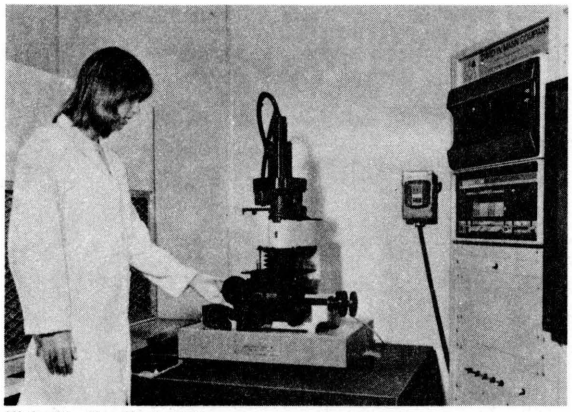
Arrangements can be made for immediate assistance from these centers by contacting any of the sales offices listed in this catalog.

Corporate Support

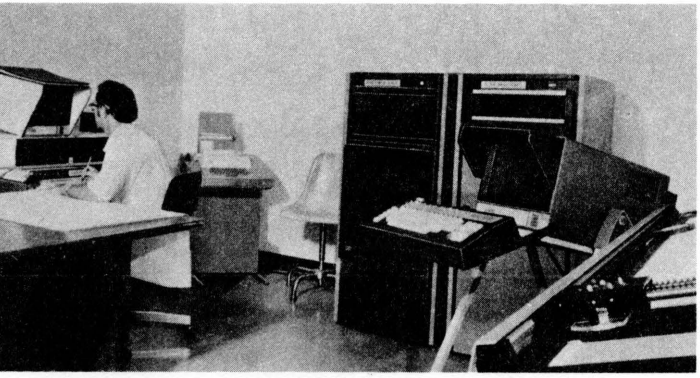
General Instrument Microelectronics is backed by the full resources of the General Instrument Corporation, which has for over 50 years been among the leaders in the application of modern electronics to entertainment, industrial, military, data and communications systems. The skills, production techniques and technological know-how of the entire General Instrument organization are utilized by GI Microelectronics to further improve its products and customer services.

Among the other electronic components manufactured by General Instrument are discrete semiconductors, relays, display devices and TV components. GI also produces CATV equipment, off-track and on-track wagering systems and equipment for defense applications.

***Glenrothes, Scotland**—Test area.*



***Hicksville, New York**—Pattern generator.*



***Hicksville, New York**—*
Computer-aided design system.

FUNCTIONAL INDEX

CALCULATORS — Section 2

Description	Function	9V Fluorescent	9V LED	9V LED (Direct)	15V Fluorescent	15V LED	PAGE NO.
8 DIGIT BASIC	4 functions and percent key.	CF-683	C-683	C-683D	CF-583	C-583	21
	4 functions, percent key, one-key or multi-key memory.	CF-685	C-685	C-685D	CF-585	C-585	22
8 DIGIT ALGEBRA	4 functions, percent key, x^2, $\sqrt{x}$, 1/x, +/-, one-key or multi-key memory, choice of 20 to 29 keys.			C-689D	CF-589	C-589	23
9 DIGIT BASIC	4 functions and percent key.				CF-593	C-593	24
	4 functions, percent key, one-key memory.				CF-594	C-594	25
	4 functions, percent key, multi-key memory.				CF-595	C-595	26
9 DIGIT SCIENTIFIC	Basic 4 functions, scientific notation, sin, cos, tan, arc sin, arc cos, arc tan, memory, square root, pi, natural logs, 1/x, e^x, memory exchange, degrees and radians, exponent* range ±99, choice of 19 to 35 keys.				CF-596	C-596	27
	All the above plus: 0 to 10^{99} degree trig range, $\log_{10}$, 10^x, y^x, extended digit accuracy of transcendentals, choice of 21 to 38 keys.				CF-598	C-598	28
	All the above plus: two levels of parenthesis, x^2, %, +/-, choice of 24 to 41 keys.				CF-599	C-599	29

The C-500/C-600 series are pin-for-pin compatible chips designed to fit in the same basic PC board. All have automatic constant in 4 functions, floating decimal, on-board oscillator, single power supply, and drive LED segments or fluorescent displays directly. All are in a 28 lead DIP.

DESCRIPTION	FUNCTION	MEMORY FUNCTION	PART NUMBER	PACKAGE	FEATURES	PAGE NO.
12 DIGIT PRINTING	Basic 4 functions and percent, automatic constant in multiply and divide, repeat add/subtract, decimal select mode, memory-in-use indicator, rounding options, non-add(#)/date key, and other features.	Accumulator and Grand Total Memories	C-717 C-717X	40 DIP	Interfaces with the Shinshu Seiki Model 310 impact printer.	31
		Accumulator, item counter, and four-key independent memory.	*C-718			32
PRINTER-DISPLAY INTERFACE	Adds display capability to the C-717X and C-718 printing calculator circuits.	—	*C-719	28 DIP	For both LED and fluorescent displays.	33

*For future release.

CLOCKS & CLOCK RADIOS — Section 3

DESCRIPTION	FUNCTION	PART NUMBER	DISPLAY TYPE	FLASHING SECONDS	ZERO BLANKING	50/60 Hz OPERATION	PACKAGE	FEATURES	PAGE NO.
4 DIGIT	12/24 hour clock	AY-5-1200A	7-SEGMENT FLUORESCENT		✓	✓	24 DIP	Direct fluorescent display drive.	36
		AY-5-1202A	7-SEGMENT FLUORESCENT	✓	✓	✓	24 DIP	Direct fluorescent display drive.	36
		AY-5-1203A	BCD OUTPUTS	✓		✓	24 DIP	See AY-5-8320 TV circuit.	36
		AY-5-1204A	7-SEGMENT FLUORESCENT	✓		✓	24 DIP	Direct fluorescent display drive.	36
		AY-5-1224A	BCD OR 7-SEGMENT LED		✓	✓	16 DIP	Zero blanking in 12 hour mode only.	38
4 DIGIT WITH ALARM AND DIRECT DISPLAY DRIVE	12 hour clock, 24 hour alarm	CK3000	7-SEGMENT PLASMA	✓	✓	✓	40 DIP	Snooze alarm, individual digit drive.	41
		CK3100	7-SEGMENT LED	✓	✓	✓	40 DIP	Snooze alarm, individual digit drive.	41
	12/24 hour clock, 24 hour alarm	CK3200	7-SEGMENT PLASMA	✓	✓	✓	28 DIP	Snooze alarm, duplexed digits.	46
		CK3400	7-SEGMENT LED	✓	✓	✓	28 DIP	Snooze alarm, duplexed digits.	46
	12/24 hour clock radio	CK3300	7-SEGMENT LED	✓	✓	✓	28 DIP	Snooze alarm, duplexed digits, sleeptimer, time-switch, battery standby capability.	52

FUNCTIONAL INDEX

RADIO / TELEVISION / TV GAMES — Section 4

DESCRIPTION	FUNCTION	PART NUMBER	POWER SUPPLIES	PACKAGE	FEATURES	PAGE NO.
RADIO RECEIVER FREQUENCY COUNTER/DISPLAY	Counts & displays MW, SW, and VHF frequencies	AY-5-8100	GND, −17	28 DIP	4½ digit display; MW 2999 kHz, SW 29.995 MHz, VHF 299.95 MHz; 0 to 99 FM channel indication (European standard), 7-segment outputs.	72
		AY-5-8101	GND, −12			
TV CHANNEL DISPLAY	Displays channels 0—15 on TV screen.	AY-5-8300	+18, GND	14 DIP	Display is positioned at top-right corner. Capable of color numerals/black background. Automatic display recall.	76
	Displays channels 1-16 on TV screen	AY-5-8302				
TV CHANNEL/TIME DISPLAY	Displays channels 0—15 or 00—99 or time on TV screen.	AY-5-8310	+18, GND	24 DIP	Display is positioned at top-right corner. Capable of color numerals/black background and either separate (AY-5-8310) or simultaneous (AY-5-8320) time and channel display (see AY-5-1203A clock circuit), with flashing seconds and colon. Automatic display recall.	76
	Displays channels 1-16 and/or time on TV screen	AY-5-8320				
TV REMOTE CONTROL	Transmitter	SAA 1024	9V BATTERY	16 DIP	30 ultrasonic control channels, 34-44 kHz. Utilizes a 4.4 MHz TV crystal for accuracy.	66
	Receiver	SAA 1025	SEE DATA SHEET	16 DIP	Power on/off output, 16 TV channel selection (& 5 spares), brightness, saturation and volume analog outputs.	68
	Transmitter	*AY-5-8410	GND, -15	-	23 channels, either local control at receiver or remote control.	82
		*AY-5-8411	9V BATTERY	-		
	Receiver	*AY-5-8420	GND, -15	-	63 channels with error-detection.	83
TV GAMES	Add-on for TV sets. 6 games: tennis, squash, hockey (soccer), pelota, rifle shooting 1 & 2	AY-3-8500 AY-3-8500-1	9V BATTERY	24 DIP	3 two-person and 3 one-person games. Automatic scoring (displayed on TV screen), realistic sounds, visually defined playing area, 525 and 625 line standards.	84

ELECTRONIC ORGANS / FREQUENCY DIVIDERS — Section 5

DESCRIPTION	FUNCTION	PART NUMBER	MAXIMUM FREQUENCY	POWER SUPPLIES	PACKAGE	FEATURES	PAGE NO.
MASTER FREQUENCY GENERATOR	Generates a complete octave of musical frequencies	AY-1-0212	1.5 MHz	+12, GND	16 DIP	250 kHz minimum frequency	91
		AY-1-0212A	2.5 MHz				
TOP OCTAVE GENERATOR	Generates top octave scale	AY-3-0214	4.5 MHz	+10 to +16, GND	16 DIP	12 outputs, 50% duty cycle	94
		AY-3-0215				13 outputs, 50% duty cycle	
		AY-3-0216				13 outputs, 30% duty cycle	
PRIORITY LATCHING NETWORK	Establishes priority level of 13 latch inputs/outputs	AY-1-1313	20 kHz	GND, −12, −27	40 DIP	Stackable for expanded latching/priority function.	100
RHYTHM GENERATOR	Generates 6 rhythms. drives 8 instruments	AY-5-1315	10 kHz	GND, −15	18 DIP	Resets for coupling chords to rhythm. 32 beat pattern. Mask programmable.	102
CHORD GENERATOR	Produces major, minor, 7th chords, walking bass	AY-5-1317A	50 kHz	GND, −15	40 DIP	Mixed outputs, sustain, top key priority	104
FREQUENCY DIVIDERS	4 stage	AY-1-5051	1 MHz	GND, −13, −27	10 TO	Arranged 2+1+1	108
	5 stage	AY-1-6721/5	1 MHz	GND, −13, −27	10 TO	Arranged 3+2	108
	6 stage	AY-1-6721/6	1 MHz	GND, −13, −27	12 TO	Arranged 3+2+1	108
		AY-1-1006	50 kHz	GND, −12, −27	14 DIP	Arranged 3+2+1	96
		AY-1-2006	50 kHz	GND, −12, −27	14 DIP	Arranged 2+2+1+1	96
	7 stage	AY-1-5050	1 MHz	GND, −13, −27	14 DIP	Arranged 3+2+1+1	108
		AY-1-1007B	50kHz	GND, −12, −27	14 DIP	Arranged 3+2+1+1, power-on reset	98

APPLIANCE TIMERS — Section 6

DESCRIPTION	FUNCTION	PART NUMBER	POWER SUPPLIES	PACKAGE	FEATURES	PAGE NO.
CLOCK TIMER	24 hour programmable, repeatable on/off time switch with 24 hour clock.	AY-5-1230	GND, −17	28 DIP	50 Hz input (60 Hz option on request), BCD or 7-segment direct fluorescent display drive outputs, zero blanking, 24 hour display (12 hour option on request).	112
COUNT-DOWN TIMER	Keyboard programmable count-down timer with 99 min/99 sec capability.	*CT 7000	GND, −15	40 DIP	60 Hz input, drives 4 digit display, end-of-count audio output.	116

*For future release

FUNCTIONAL INDEX

TELECOMMUNICATIONS — Section 7

DESCRIPTION	FUNCTION	PART NUMBER	POWER SUPPLIES	PACKAGE	FEATURES	PAGE NO.
PUSH BUTTON TELEPHONE DIALLER CIRCUIT	Converts push button input to rotary dial pulses	**AY-5-9100**	SEE DATA SHEET	18 DIP	Programmable timing, one-call memory, optional re-dial and access pause capability.	**120**
REPERTORY DIALLER	Stores ten telephone numbers	**AY-5-9200**	SEE DATA SHEET	16 DIP	Complements AY-5-9100 to enable storage of up to ten 22-digit telephone numbers. Stackable.	**124**
COINBOX CIRCUIT	Controls the operation of a standard pay telephone	**AY-5-9300**	SEE DATA SHEET	24 DIP	Up to 3 coin denominations recognized. 16 selectable coin value ratios.	**130**
DUAL TONE MULTI-FREQUENCY GENERATOR	Generates MF/tone telephone frequencies	**AY-3-9400**	+5, GND	14 DIP	With a low cost ceramic resonator, generates 12 tone pairs.	**131**
		AY-3-9410	+5, GND	16 DIP	Same as AY-3-9400 but generates 16 tone pairs for data transmission.	**131**
C-MOS CLOCK GENERATOR	Generates 2-phase clocks from a single power supply	**AY-5-9500**	SEE DATA SHEET	14 DIP	Generates 2-phase clocks for AY-5-9100 & AY-5-9200.	**134**
MULTI-FREQUENCY RECEIVER	Detects and converts MF/Tone telephone frequencies.	***AY-5-9800**	SEE DATA SHEET	28 DIP or 40 DIP	Many programmable features provide wide applications.	**137**

DATA COMMUNICATIONS — Section 8

DESCRIPTION	FUNCTION	PART NUMBER	REPLACES (PIN-FOR-PIN)	BAUD RANGE	MAX. FREQ.	TEMP. RANGE	POWER SUPPLIES	PACKAGE	FEATURES	PAGE NO.
UAR/T®	Complete 5-8 bit serial/ parallel, parallel/serial interface	***AY-3-1015**	AMI S1757 SIG 2536 SMC COM2505 TI TMS6011 WD TR1402A WD TR1602A	0 to 30 kb	480 kHz	0 to 70	+5, GND	40 DIP	1, 1.5, or 2 stop bits	**149**
		†**AY-6-1013**		0 to 20 kb	320 kHz	−55 to +125	+5, GND, −12	40 DIP	1 or 2 stop bits	**145**
		AY-5-1013		0 to 30 kb	480 kHz	0 to 70				
		AY-5-1013A		0 to 40 kb	640 kHz	0 to 70				
		***AY-3-1014A**		0 to 30 kb	480 kHz	0 to 70	+5, GND	40 DIP	1, 1.5, or 2 stop bits	**149**
RANDOM/ SEQUENTIAL ACCESS MULTIPLEXER	Multiplexes 16 analog channels, current, voltage, or differential mode	**AY-5-1016**	—	—	2 MHz	0 to 70	+5, GND, −12	40 DIP		**154**
		†**AY-6-4016**				−55 to +125				

†Also available with MIL STD 883 screening (add suffix TX to part number).
®UAR/T is a registered trademark of General Instrument Corporation.

COUNTERS / DIGITAL METERS — Section 9

DESCRIPTION	FUNCTION	PART NUMBER	MAX. COUNT FREQUENCY	DISPLAY CURRENT	POWER SUPPLIES	PACKAGE	FEATURES	PAGE NO.
1 DIGIT COUNTER	Counts & decodes one decade to BCD outputs.	**MEM1056BCD**	1.0 MHz	—	GND, −13, −27	24 DIP	BCD outputs.	**162**
1 DIGIT COUNTER/ DISPLAY DRIVER	Counts & decodes one decade to 7-segment outputs.	**MEM1056**	1.0 MHz	1.0 mA	GND, −13, −27	24 DIP	7-segment outputs	**162**
4 DIGIT COUNTER	Counts, stores & decodes four decades to BCD outputs.	**AY-5-4057**	500 kHz	—	+5, GND, −12	16 DIP	BCD outputs	**178**
4 DIGIT COUNTER/ DISPLAY DRIVER	Counts (up or down), stores & decodes four decades to 7-segment outputs.	**AY-5-4007**	600 kHz	25 mA/V	+5, GND, −12	24 DIP	BCD outputs, true/ complement control	**172**
		AY-5-4007A				40 DIP	Includes features of AY-5-4007 & 4007D.	**172**
		AY-5-4007D				24 DIP	Serial count output, three carry outputs	**172**
3½ DIGIT DVM CIRCUIT	DVM logic incorporating dual ramp integration	**AY-5-3507**	40 kHz	6 mA	GND, −15	18 DIP	Range to 1999, 7-segment outputs	**168**
		AY-5-3510		—		16 DIP	Range to 1999, BCD outputs	**168**
3¾ DIGIT DVM CIRCUIT	DVM logic incorporating single ramp integration	**AY-5-3500**	200 kHz	6 mA	GND, −7.5, −15	28 DIP	3 ranges: 999, 1999, 2999. Dual polarity, BCD & 7-seg. outputs	**163**
10 BIT D/A CONVERTOR	Ladderless D/A converter	**AY-5-5053**	SEE DATA SHEET	—	+5, GND, −12	24 DIP	Employs stochastic techniques.	**181**
A/DCONVERTOR CONTROL	With AY-5-5053, performs A/D with transmitter facility.	**AY-5-5054**	SEE DATA SHEET	—	+5, GND, −12	24 DIP	For use in remote sensing applications.	**186**

*For future release.

MICROPROCESSORS — Section 10

DESCRIPTION	PART NUMBER	INTERNAL REGISTER ADD	CLOCKS/ FREQUENCY/ MICROCYCLE	INTER-FACE	POWER SUPPLIES	PACKAGE	PAGE NO.
16 BIT—High performance, N-Channel, single-chip with 3rd generation minicomputer architecture, 87 basic instructions, 8 general purpose 16 bit registers, last-in/first-out stack of unlimited depth, 65K memory address capability, dual level priority interrupt system, and Direct Memory Access capability.	CP1600	3.6 μs	2/3.3 MHz/ 600 ns.	TTL	+12, +5, GND, −3	40 DIP	192
	*CP1600A	2.4 μs	2/5 MHz/ 400 ns.				
8 BIT—PIC: A single-chip byte oriented micro-programmable interface controller for low cost microprocessor/peripheral device interfacing. An internal ROM microprogram defines the overall functional characteristics and operational waveforms on each of the general purpose I/O lines. Both products emphasize control and interface functions. PIC 1650 design/instruction set also supports computing functions. Full software support and a Hardware Emulator are available.	*PIC 1640	1μs	1/4 MHz/1μs	TTL	+5, GND	40 DIP	210
	*PIC 1650					28 DIP	213
8 BIT—ALPS: Advanced Logic Processing System. A kit of 5 P-Channel arrays consisting of microprocessor, ROM, I/O, memory interface (to standard, RAM, ROM, PROM), and a clock/reset generator circuit. The microprocessor contains an 8 bit accumulator, 48 internal registers, binary and decimal capability, and an input/output port allowing simple systems to be configured with as few as two chips.	LP 8000	5.5μs	1/720 kHz/694 ns.	TTL or high level (open drain)	+5, GND, −12	40 DIP	216
	LP 6000					40 DIP	216
	LP 1010					40 DIP	216
	LP 1000					40 DIP	216
	LP 1030					8 DIP	216

General Instrument offers a "total product family" approach to microprocessor circuits including the circuits described here plus a full complement of semiconductor circuits, PC card modules, prototype development hardware, extensive software support and comprehensive documentation. For further information call the sales office nearest you.

*For future release

RANDOM ACCESS MEMORIES — Section 11

BITS/ MODE	MEMORY ORGANIZATION	PART NUMBER	REPLACES (PIN-FOR-PIN)	ACCESS TIME/ CYCLE TIME	POWER SUPPLIES	PACKAGE	FEATURES	PAGE NO.
1024/ STATIC	256 x 4	RA-3-4256	—	500ns/500 ns	+5, GND	24 DIP	Power down mode	224
		RA-3-4256A	—	650ns/650ns	+5, GND	24 DIP	Power down mode	224
		RA-3-4256B	—	650ns/650ns	+5, GND	22 DIP		224
4096/ STATIC	4096 x 1	RA-3-4200	SEMI 4200	215ns/400ns	+12, +5, GND, −5	22 DIP	TTL output	228
		RA-3-4402	SEMI 4402	200ns/350ns	+12, GND, −5	22 DIP	Differential outputs	232

ELECTRICALLY ALTERABLE READ ONLY MEMORIES — Section 12

BITS	MEMORY ORGANIZATION	PART NUMBER	READ ACCESS TIME	ERASE TIME	ERASE MODE	WRITE TIME	POWER SUPPLIES	PACKAGE	FEATURES	PAGE NO.
512	32 x 16	ER 2050	4μs	100 ms	WORD (16 BIT)	100ms/ 16 BIT WORD	+5, −29	28 DIP	10 year data storage @ 70°C	246
1024	256 x 4	ER 1105	2μs	100 ms	BLOCK (32 x 1)	10 ms/ 4 BIT WORD	+12, −12	24 DIP		238
1400	100 x 14	ER1400	3.4 ms	100 ms	WORD (14 BIT)	100ms/ 14 BIT WORD	-35	8 TO		243
4096	1024 x 4	ER 2401	2μs	100 ms	BLOCK (1024 x 4)	10 ms/ 4 BIT WORD	+5, -5 -14, -24	24 DIP		248
		*ER3400	600ns	1ms	WORD (4 BIT)	100μs/ 4 BIT WORD	+5,-12, -30	22 DIP		255
8192	2048 x 4	*ER2800	2μs	100 ms	BLOCK (2048 x 4)	20ms/ 4 BIT WORD	+5, -5 -14, -24	24 DIP		254

*For future release.

FUNCTIONAL INDEX

READ ONLY MEMORIES — Section 13

DESCRIPTION	BITS	MEMORY ORGANIZATION	PART NUMBER	REPLACES (PIN-FOR-PIN)	ACCESS TIME	CLOCKS/ VOLTAGE	POWER SUPPLIES	PACKAGE	FEATURES	PAGE NO.
GENERAL PURPOSE	1024	256 x 4	**RO-7-1024/4**	—	1μs (typ.)	STATIC	+5, GND, −12	16 DIP	RO-6-1024/4 avail. for −55° to +125°	**258**
		128 x 8	**RO-7-1024/8**	—	1μs (typ.)	STATIC	+5, GND, −12	24 DIP	RO-6-1024/8 avail. for −55° to +125°	**258**
	2048	512 x 4	**RO-7-2048/4**	—	1.5μs (typ.)	STATIC	+5, GND, −12	24 DIP	RO-6-2048/4 avail. for −55° to +125°	**262**
		256 x 8	**RO-7-2048/8**	—	1.5μs (typ.)	STATIC	+5, GND, −12	24 DIP	RO-6-2048/8 avail. for −55° to +125°	**262**
			RO-5-1302	INTEL 1302	1.5μs (typ.)	STATIC	+5, GND, −12	24 DIP	Mask programmable version of 1702	**260**
	2560	512 x 5	**RO-3-2560**	—	450 ns.	STATIC	+5, GND	18 DIP		**264**
	4096	512 x 8	**RO-3-4096**	—	500 ns.	STATIC	+5, GND	22 DIP		**266**
	5120	512 x 10	**RO-3-5120**	EA 4000	500 ns.	STATIC	+5, GND	24 DIP		**268**
	8192	2048 x 4	**RO-5-8192**	AMI S8865 TI TMS4000	1.2μs (typ.)	2/TTL	+5, −12	24 DIP		**270**
	16384	4096 x 4	**RO-3-16384**	AMI S8996	1μs	STATIC	+5, GND	24 DIP	Address/CS latch	**278**
		2048 x 8	**RO-3-8316A** **RO-3-9316A**	INTEL 2316,A INTEL 4316,A INTEL 8316,A	850 ns.	STATIC	+5, GND	24 DIP		**273**
			RO-3-8316B **RO-3-9316B**		450 ns.					
	20480	2048 x 10	***RO-3-20480**	—	500 ns.	STATIC	+5, GND	24 DIP		**281**

Note: All Read Only Memories are mask-programmable.

*For future release.

KEYBOARD ENCODERS / CHARACTER GENERATORS — Section 14

DESCRIPTION	BITS	MEMORY ORGANIZATION	PART NUMBER	REPLACES (PIN-FOR-PIN)	ACCESS TIME	CLOCKS/ VOLTAGE	POWER SUPPLIES	PACKAGE	FEATURES	PAGE NO.
KEYBOARD ENCODER	2376	88 x 3 x 9	**AY-5-2376**	SMC KR2376	10-100 KHz SCAN RATE	1/TTL OR INT. OSC.	+5, GND, −12	40 DIP	2 key rollover, 88 keys, 3 modes	**284**
	3600	90 x 4 x 10	**AY-5-3600**	SMC KR3600	10-100 kHz SCAN RATE	1/TTL OR INT. OSC.	+5, GND, −12	40 DIP	2/N key rollover, 90 keys, 4 modes	**289**
CHARACTER GENERATOR	2240	64 x 5 x 7	**RO-5-2240S**	MK 2302 FSC 3257	1μs (typ.)	1/TTL FOR SCANNING	+5, GND, −12	24 DIP	5 x 7 characters, column output, on-chip scanning	**295**
	2560	64 x 8 x 5	**RO-3-2513**	SIG 2513	450 ns.	STATIC	+5, GND	24 DIP	5 x 7 characters, row output	**299**
	5184	64 x 9 x 9	**RO-5-5184**	—	5μs (typ.)	1/TTL FOR SCANNING	+5, GND, −12	24 DIP	9 x 9 characters, on-chip left/right scanning	**303**

Note: All Keyboard Encoders and Character Generators are mask-programmable.

STATIC SHIFT REGISTERS (Contact any GI Sales Office for details.)

BITS	ORGANIZATION	0° to 70° PART NO.	−55° to +125° PART NO.	OPERATING FREQ. RANGE	INPUT/ OUTPUT	CLOCKS/ VOLTAGE	POWER SUPPLIES	PACKAGES	FEATURES
32	VARIABLE	**SS-5-1032**	**SS-6-1032**	DC-1 MHz	TTL	1/TTL	+5, GND, −12	16 DIP	6 S/R's arranged 1-1-2-4-8-16
	DUAL 16	‡**SS-5-8211**	**SS-6-8211**	DC-2 MHz	TTL	1/TTL	+5, GND, −12	16 DIP	Set control dual input selector
		†**SS-5-8212**	**SS-6-8212**	DC-2 MHz				8/14 DIP, 8 TO	
64	QUAD 16	†**SL-5-4016**	—	DC-2 MHz	TTL	1/TTL	+5, GND, −12	14 DIP	
100	DUAL 50	†**SL-5-2050**	**SL-6-2050**	DC-1 MHz	TTL	1/TTL	+5, GND, −12	8/14 DIP, 8 TO	
	QUAD 25	†**SL-5-4025**	**SL-6-4025**	DC-1 MHz				14 DIP	
128	DUAL 64	†**SL-5-2064**	**SL-6-2064**	DC-1 MHz	TTL	1/TTL	+5, GND, −12	8/14 DIP, 8 TO	
	QUAD 32	†**SL-5-4032**	**SL-6-4032**	DC-1 MHz				14 DIP	
200	DUAL 100	†**SL-5-C2100**	—	DC-2 MHz	TTL	1/TTL	+5, GND, −12	14 DIP, 8 TO	
256	DUAL 128	†**SL-5-2128**	—	DC-1 MHz	TTL	1/TTL	+5, GND, −12	8/14 DIP, 8 TO	
		SL-5-C2128	—	DC-2 MHz					

‡Available in Europe as part number SS-7-2016 (16 lead plastic DIP only)

†Available in Europe as part number SS-7/SL-7 (14 lead plastic DIP only).

AMI	GI
DEVICE NO.	REPLACEMENT
S1757	AY-5-1013/1013A
S1757	AY-3-1014A/1015
S2470	AY-1-1006
S8865	RO-5-8192
S8996	RO-3-16384

ELECTRONIC ARRAYS	GI
DEVICE NO.	REPLACEMENT
EA4000	RO-3-5120

EMM/SEMI	GI
DEVICE NO.	REPLACEMENT
4200	RA-3-4200
4402	RA-3-4402

FAIRCHILD	GI
DEVICE NO.	REPLACEMENT
3257	RO-5-2240S

INTEL	GI
DEVICE NO.	REPLACEMENT
1302	RO-5-1302
2316A	RO-3-8316A/8316B
8316A	RO-3-8316A/8316B

MOSTEK	GI
DEVICE NO.	REPLACEMENT
MK2302	RO-5-2240S
MK50240	AY-3-0215
MK50241	AY-3-0216
MK50242	AY-3-0214
MK50242	AY-1-0212

NATIONAL	GI
DEVICE NO.	REPLACEMENT
MM5303	AY-5-1013/1013A
MM5303	AY-3-1014A/1015
MM5823	AY-1-2006
MM5824	AY-1-1006

SIGNETICS	GI
DEVICE NO.	REPLACEMENT
2513	RO-3-2513
2536	AY-5-1013/1013A
2536	AY-3-1014A/1015

SMC	GI
DEVICE NO.	REPLACEMENT
COM2505	AY-5-1013/1013A
COM2505	AY-3-1014A/1015
KR2376	AY-5-2376
KR3600	AY-5-3600

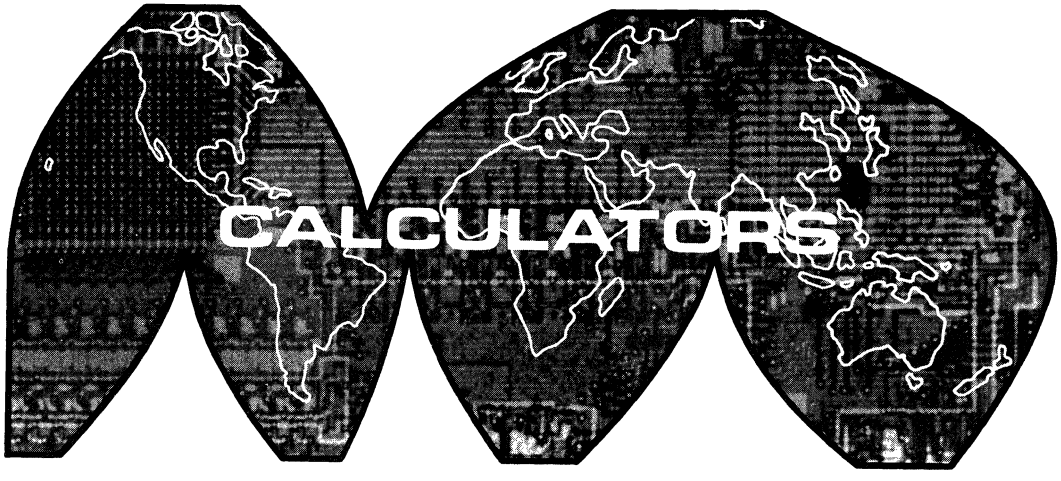
WESTERN DIGITAL	GI
DEVICE NO.	REPLACEMENT
TR1602	AY-5-1013/1013A
TR1602	AY-3-1014A/1015

TEXAS INSTRUMENTS	GI
DEVICE NO.	REPLACEMENT
TMS0803	C-593
TMS0851	CF-593
TMS4000	RO-5-8192
TMS5001	AY-5-3600
TMS6011	AY-5-1013/1013A
TMS6011	AY-3-1014A/1015

GENERAL INSTRUMENT

C/CF-583
C/CF-683
C-683D
C/CF-589
C/CF-585
C/CF-685
C-685D
C-689D
C/CF-593
C/CF-594
C/CF-595
C/CF-596
C/CF-598
C/CF-599
C-717
C-717X
C-718
C-719

2



Display Calculator Circuits

FEATURES

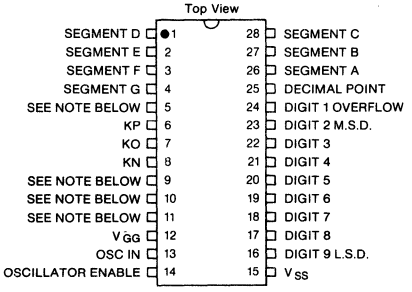
- Printed circuit board compatibility of circuits.
- Direct segment drive for LED displays (C-XXX)
- Direct segment and digit drive for LED displays (C-XXXD)
- Direct fluorescent display drive (CF-XXX)
- Algebraic operation
- Automatic constant
- Floating point operation
- Constant or chain operation (no switch required)
- Leading zero suppression
- Automatic power-on clear
- Internal clock (on-chip oscillator)
- Internal keyboard debounce logic

DESCRIPTION

General Instrument's broad line of display calculator circuits, the C/CF-500 Series and the C/CF-600 Series, consists of pin-for-pin compatible circuits designed to fit in the same basic PC board. This provides a high degree of flexibility in calculator models manufactured while minimizing the tooling required.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



NOTE:
All Display Calculator circuits offered by General Instrument have identical pin functions on all pins except pins 5, 9, 10 and 11. These pins are utilized for the distinctive functions of each calculator circuit model as described on the following pages of this section.

Description	Function	9V Fluorescent	9V LED	9V LED (Direct)	15V Fluorescent	15V LED
8 DIGIT BASIC	4 functions and percent key.	CF-683	C-683	C-683D	CF-583	C-583
	4 functions, percent key, one-key or multi-key memory.	CF-685	C-685	C-685D	CF-585	C-585
8 DIGIT ALGEBRA	4 functions, percent key, x^2, $\sqrt{x}$, 1/x, +/-, one-key or multi-key memory, choice of 20 to 29 keys.			C-689D	CF-589	C-589
9 DIGIT BASIC	4 functions and percent key.				CF-593	C-593
	4 functions, percent key, one-key memory.				CF-594	C-594
	4 functions, percent key, multi-key memory.				CF-595	C-595
9 DIGIT SCIENTIFIC	Basic 4 functions; scientific notation, sin, cos, tan, arc sin, arc cos, arc tan, memory, square root, pi, natural logs, 1/x, e^x, memory exchange, degrees and radians, exponent range ±99, choice of 19 to 35 keys.				CF-596	C-596
	All the above plus: 0 to 10^{99} degree trig range, $\log_{10}$, 10^x, y^x, extended digit accuracy of transcendentals, choice of 21 to 38 keys.				CF-598	C-598
	All the above plus: two levels of parenthesis, x^2, %, +/-, choice of 24 to 41 keys.				CF-599	C-599

I THE FOLLOWING APPLY AS NOTED:

A. AUTOMATIC CONSTANT (All circuits)

The answer from any operation is entered automatically as a Constant by the = key without a constant switch. The Constant may then be used with all five functions and the answer from any Constant calculation can be used for further calculations without re-entry. This provides an extremely powerful facility for solving many complex equations without the need for writing down or remembering intermediate results. It is particularly useful for raising to a power, compound interest calculations, nth roots, depreciation calculations, etc. In constant multiplication, the constant is the first entered number (constant multiplicand). In division, addition and subtraction, the constant is the second entered number. The completion of the first operation with the depression of the = key initiates the storage of the constant number. For subsequent operations it is only necessary to enter a number and depress the = key.

B. DECIMAL ALIGNMENT (C/CF-593, C/CF-594, C/CF-595)

The results of addition or subtraction will remain aligned to the preceding number having the most decimal places. This feature allows computation in the dollar and cents mode without suppression of the zeros to the right of the decimal point. If a right shift is needed to keep the eight most significant digits, the least significant digits are lost. The results of multiplication and division will be completely right adjusted such that only the most significant digits are displayed except during overflow.

C. CAPACITY (All except Scientific Circuits)

For the C/CF-580 Series and the C/CF-680 Series, in the case of overflow, the eight most significant digits are displayed (seven digits and minus sign for negative answers) all decimal points are lit and the keyboard is locked out. Only the operation of the clear key will allow continued operation. On depression of the clear key, the decimal point is shifted eight places to the left of its actual position.

For the C/CF-593, 594 and 595, in the case of overflow, the overflow symbol is displayed, and the decimal point shifted eight places to the left of its actual position. Under these conditions, the keyboard is locked out such that only the operation of the clear key will allow continued operation.

In all cases, for an attempted entry requiring more than eight display digits, the most significant digits are protected upon the attempted entry of another digit. The keyboard is not locked out and operations are still able to be performed.

When division by zero is attempted, an overflow condition results and a zero is displayed.

D. PERCENT KEY (all except C/CF-596 and 598)

Multiplies the two preceding entries and divides by 100, and when followed by = gives add-on and discount: A+B% yields (AB/100); A+B%=yields A+(AB/100). A−B% yields (AB/100); A−B%=yields A−(AB/100).

E. CHANGE NOTATION KEY (Scientific Circuits)

Depression of the CHG NOT key will convert the displayed number to scientific notation, if it is in the "normal" mode, or it will display the 8 most significant digits of a scientific mantissa with the decimal point correctly located (even if it falls beyond the display area) and trailing zeroes shall be blanked. In addition, for numbers less than one, the digits are left shifted until all leading zeroes have been eliminated.

F. EXPONENT KEY (Scientific Circuits)

EEX: This key operates as follows: The EEX key sets the two right most digits to zero, the third digit from the right is blanked and the calculator is conditioned to accept sign and numeral keys to define the exponent value of the number entry. If the mantissa had numbers in any of the last three digit positions, these are retained but not displayed.

G. FUNCTION KEY OPERATIONS (Used only with dual-function keys)

Depression of the F key sets the calculator in the "Function" mode and the F indicator is lit. The dual function keys will then function as indicated by their upper case designation. Single function keys directly perform the indicated function.

Depression of the second key of the sequence resets the "Function" mode and the F indicator is turned off when the answer is displayed. The "Function" mode can also be reset by a second depression of the F key.

II THE FOLLOWING APPLY AS NOTED TO CIRCUITS WITH MEMORY:

A. MEMORY DESCRIPTION: One-Key memory as provided in C/CF-585, 589, 594, 685, C-685D & C-689D.

M: The Memory key is used in conjunction with other function keys to define a two key sequence which sets a mode of operation associated with the memory register and terminates any immediately preceding entry.

Operation of the M key followed by + adds the contents of the display register to the memory register without altering the contents of the display register.

Operation of the M key followed by − subtracts the contents of the display register without altering the contents of the display register.

Operation of the M key followed by = transfers the contents of the memory register into the display register without altering the contents of the memory register.

Operation of the M key followed by C/CE clears the contents of the memory register.

Operation of the M key followed by the X key performs a memory-display exchange function. The contents of the memory register are brought out to the display register and the contents of the display register are written into the memory register, replacing the previous contents of the memory register.

Operation of the M key followed by any key other than +, −, X, =, or C/CE shall reset the M condition and act upon the subsequent entry as if the M had not been entered.

In addition, two optional keys are provided with the C/CF-594 for operation as follows:

MR, MEMORY READ: Functions identically to the M = sequence above.

MC, MEMORY CLEAR: Functions identically to the M C/CE sequence above.

B. MEMORY DESCRIPTION: Multi-key memory as provided in all algebra and scientific circuits

MR, MEMORY READ: Functions identically to the M = sequence above.

MC, MEMORY CLEAR: Functions identically to the M C/E sequence above.

M+, MEMORY PLUS: Functions identically to the M+ sequence above.

M−, MEMORY MINUS: Functions identically to the M− sequence above.

MEX, MEMORY EXCHANGE: Functions identically to the MX sequence above.

In addition, the C/CF-589 and C-689D are provided with a STORE key which transfers the contents of the display to memory without changing the display.

C. MEMORY DESCRIPTION: Multi-key memory as provided in C/CF-585, 595, 685 and C-685D.

MC, MEMORY CLEAR: clears the memory while leaving the display intact.

MR, MEMORY READ: transfers the data in memory to the display without changing the memory.

M$\bar{+}$, MEMORY EQUALS/PLUS: completes the preceding operation, displays the result, and adds the result to the memory.

M$\bar{-}$, MEMORY EQUALS/MINUS: completes the preceding operation, displays the result and subtracts the result from the memory.

In addition, the C/CF-585, C/CF-685 and C-685D are provided with a MEX (Memory Exchange) Key which functions as previously described.

The C/CF-595 is provided with the following additional memory keys:

MR/MC, MEMORY READ/MEMORY CLEAR: this single key operation transfers the memory data to the display on the first depression. When depressed two successive times, the memory data is transferred to the display and the memory cleared.

Σ, SUM KEY: when connected to V_{SS}, this accumulate switch, independent of the keyboard, adds the contents of the display to memory with each depression of the equals key.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*	**Fluorescent Display CF-6XX Series**	**Fluorescent Display CF-5XX Series**	**LED Display C-5XX Series**	**LED Display C-6XX Series**	**LED Display C-6XXD Series**
V_{GG} supply voltage range[1]	-15V to +0.3V	−20V to +0.3V	−20V to +0.3V	−15V to +0.3V	-15V to +0.3V
Clock input voltage range[1]	-15V to +0.3V	−20V to +0.3V	−20V to +0.3V	−15V to +0.3V	-15V to +0.3V
Data input voltage range[1]	-30V to +0.3V	−32V to +0.3V	−20V to +0.3V	−15V to +0.3V	-15V to +0.3V
Applied output voltage range[1]	-30V to +0.3V	−32V to +0.3V	−20V to +0.3V	−15V to +0.3V	-15V to +0.3V
Maximum power dissipation at +25° C[2]	500 mW				
Storage temperature range	-20° C to +70° C				
Operating free-air temperature range	0° C to +40° C				
Relative humidity range (no condensation)	0 to 95%				

All inputs and outputs are internally protected against static charge damage during handling consistent with standard industry practices.

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

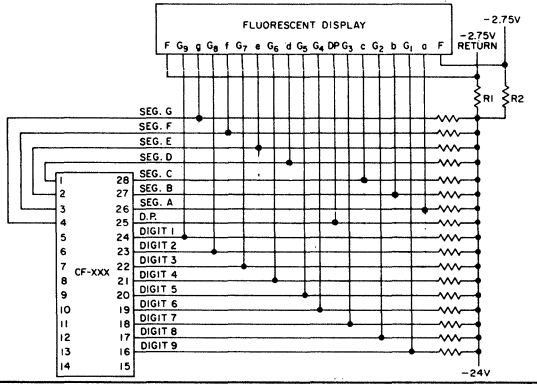
[1] Measured with respect to V_{SS}.
[2] Derate at 10mW/° C.

Operating Conditions	**CF-5XX Series Range**	**C-5XX Series Range**	**C/CF-6XX Series** Min.	Typ.	Max.	**C-6XXD Series** Min.	Typ.+	Max.
V_{SS}, substrate supply	OV	OV		OV			OV	
V_{GG}, gate supply: C/CF-5XXA	−15.0V±5%	−15.0V±5%		—			—	
C/CF-5XXB	−16.0V±5%	−16.0V±5%		—			—	
C/CF-5XXC	-17.0V±5%	-17.0V±5%		—			—	
C-6XXA	—	—	−10.3V	−7.5V	−6.5V		—	
C-6XXB	—	—	-9.5V	-7.5V	-6.5V		—	
C-6XXD	—	—		—		+6.5V	—	+9.5V

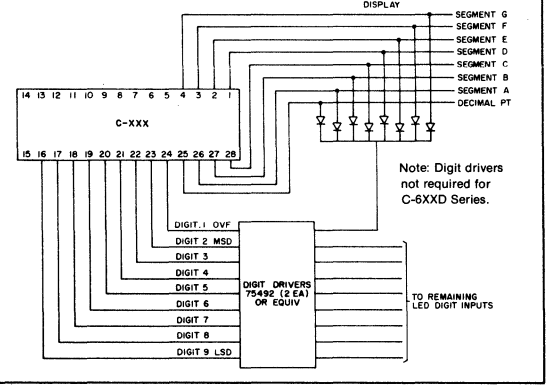
Characteristics- at typical operating conditions over a 0° C to +40° C range.	**CF-5XX/6XX Series** Min.	Typ.+	Max.	**C-5XX Series** Min.	Typ.+	Max.	**C-6XX Series** Min.	Typ.	Max.	**C-6XXD Series** Min.	Typ.	Max.
Keyboard input characteristics-												
Input signal levels: Logic 0	−1.5V	—	0V	−1.5V	—	0V	−0.5V	—	0V	OV	—	+1.0V
Logic 1	V_{GG}	—	−6.0V	V_{GG}	—	-6.0V	V_{GG}	—	−4.0V	+4.5V	—	V_{GG}
Keyboard resistance	—	—	1K	—	—	1K	—	—	1K	—	—	1K
Output buffer characteristics-[3]												
Segment output on-resistance: at -0.5V V_{OUT}	—	—	—	—	—	—	—	200Ω	300Ω	—	1K	1.3K[4]
at −1.5V V_{OUT}	—	200Ω	600Ω	—	200Ω	300Ω	—	—	—	—	—	—
Digit output on-resistance at −1.5V V_{OUT}	—	200Ω	300Ω	—	200Ω	300Ω	—	200Ω	300Ω	—	30Ω	50Ω[5]
Digit and segment off-leakage: at V_{OUT}=−9V	—	—	—	—	—	18μA	—	—	18μA	—	—	100μA[6]
at V_{OUT}=-27V (CF-590, CF-680 Series) or V_{OUT}=-30V (CF-580 Series).	—	—	18μA	—	—	—	—	—	—	—	—	—
Anode and grid supply voltage through 200K resistor: CF-580 Series	−30V	−24V	—	—	—	—	—	—	—	—	—	—
CF-590, CF-680 Series	−27V	−24V	—	—	—	—	—	—	—	—	—	—
Power (all outputs off)-												
at V_{GG}=−16.0V, C/CF-580 Series	—	75mW	100mW	—	75mW	100mW	—	—	—	—	—	—
at V_{GG}=−16.0V, C/CF-590 Series	—	100mW	125mW	—	100mW	125mW	—	—	—	—	—	—
at V_{GG}=−7.5V, C-680 Series	—	—	—	—	—	—	—	15mW	30mW	—	20mW	50mW

[3] All output buffers are open-drain to V_{SS}.
+ Typical values are at +25° C and nominal voltages.
[4] At 4mA.
[5] At 36mA.
[6] At +9V.

FLUORESCENT DISPLAY INTERCONNECT



LED DISPLAY INTERCONNECT



8 Digit / 5 Function Basic Calculator Circuit

FEATURES

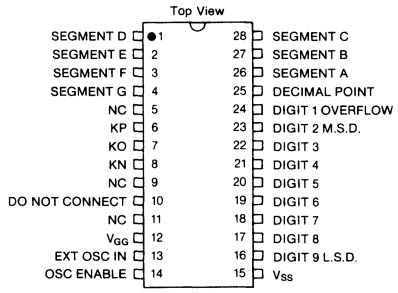
- 8 digit, 7 segment display outputs.
- Basic four arithemetic functions (+, −, x, ÷).
- Percent (add-on and discount).
- Floating negative sign.
- Right-justified entry and result.
- C-583 and C-683: direct LED segment drive.
  CF-583 and CF-683: direct fluorescent display drive.
  C-683D: direct LED segment and digit drive.
- All other features listed on the first page of this section.

DESCRIPTION

The C/CF-583, C/CF-683 and C-683D circuits are basic five-function circuits which may be used with either eight or nine digit LED or fluorescent displays. They compute and display the results of calculations with numbers up to eight digits (seven for negative). On overflow, the keyboard is locked and all decimal points are lighted. In addition, an overflow symbol will appear in the ninth digit position for those calculators having nine digit displays.

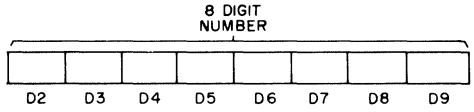
PIN CONFIGURATION

28 LEAD DUAL IN LINE

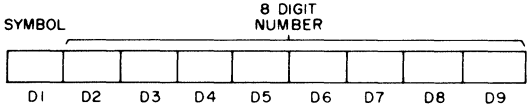


DISPLAY

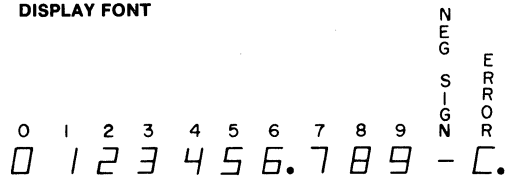
8 DIGIT DISPLAY



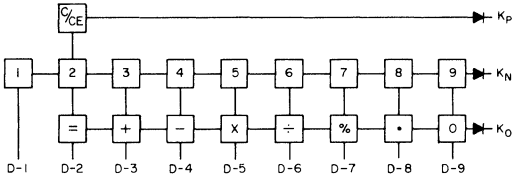
OPTIONAL 9 DIGIT DISPLAY



DISPLAY FONT



KEY MATRIX



Note: Diodes used only for CF-583 and CF-683.

8 Digit / 5 Function Basic Calculator Circuit With One-Key or Multi-Key Memory

FEATURES

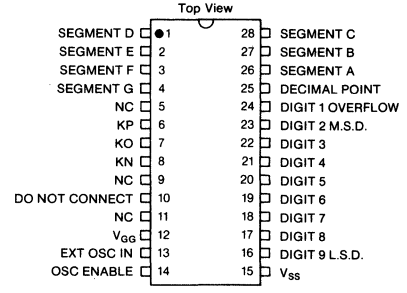
- 8 digit, 7 segment display outputs.
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount).
- Floating negative sign.
- Right-justified entry and result.
- One-key or multi-key memory function (refer to the description at the beginning of this section.)
- C-585 and C-685: direct LED segment drive.
  CF-585 and CF-685: direct fluorescent display drive.
  C-685D: direct LED segment and digit drive.
- All other features listed on the first page of this section.

DESCRIPTION

The C/CF-585, C/CF-685 and C-685D circuits are basic five-function memory circuits which offer the user the highest degree of functional flexibility in implementing a memory calculator. The circuits include all the features of the C/CF-583, C/CF-683 and C-683D circuits with the addition of the memory function.

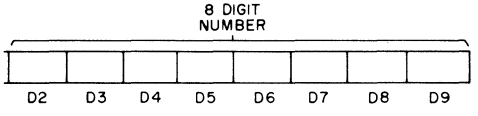
PIN CONFIGURATION

28 LEAD DUAL IN LINE

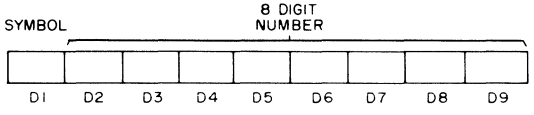


DISPLAY

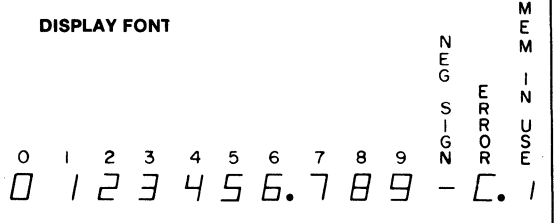
8 DIGIT DISPLAY



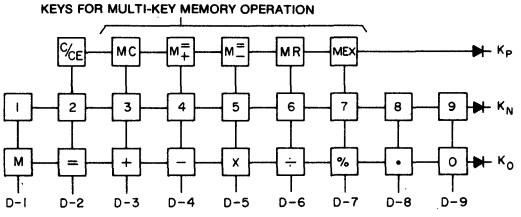
OPTIONAL 9 DIGIT DISPLAY



DISPLAY FONT



KEY MATRIX



Note: Diodes used only for CF-585 and CF-685.

8 Digit / 9 Function Algebra Calculator Circuit With One-Key or Multi-Key Memory

FEATURES

- 8 digit, 7 segment display outputs.
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount).
- Convenience functions (x^2, $\sqrt{x}$, 1/x, +/-)
- Floating negative sign.
- Right-justified entry and result.
- One-key or multi-key memory function (refer to the description at the beginning of this section.)
- C-589: direct LED segment drive.
  CF-589: direct fluorescent display drive.
  C-689D: direct LED segment and digit drive.
- All other features listed on the first page of this section.

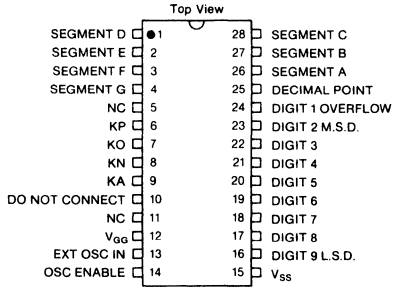
DESCRIPTION

The C/CF-589 and C-689D circuits are basic eight-function memory circuits which offer the user the highest degree of functional flexibility in implementing a memory calculator. The circuits include all the features of the C/CF-585 and C-685 circuits with the addition of the functions x^2, $\sqrt{x}$, 1/x and +/-.

The C/CF-589 and C-689D circuits may be operated with either single or dual function keys with a keyboard configuration of from 20 to 29 keys.

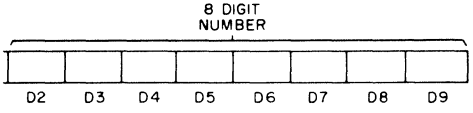
PIN CONFIGURATION

28 LEAD DUAL IN LINE

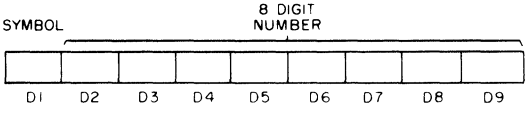


DISPLAY

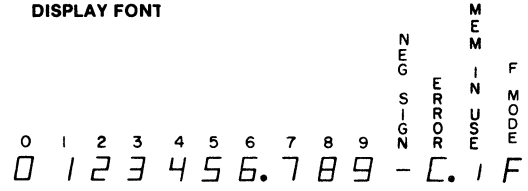
8 DIGIT DISPLAY



OPTIONAL 9 DIGIT DISPLAY

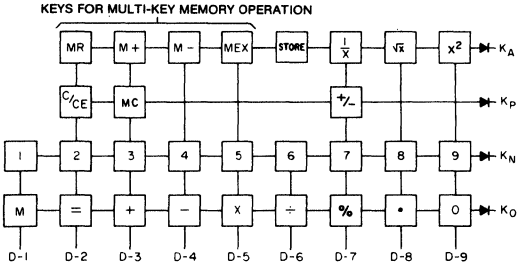


DISPLAY FONT

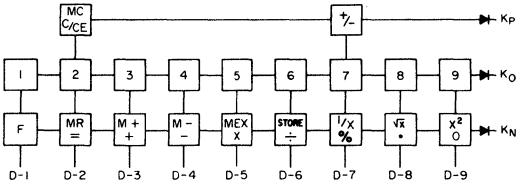


KEY MATRIX

SINGLE FUNCTION KEYS



DUAL FUNCTION KEYS



Note: Diodes used only for CF-589.

9 Digit / 5 Function Basic Calculator Circuit

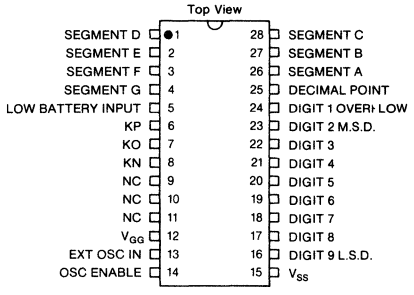
FEATURES

- 8 digit, 7 segment display outputs with ninth digit for sign or symbol.
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount).
- Floating negative sign.
- Right-justified entry and result.
- Results of addition or subtraction remain aligned to preceding number having most decimal places.
- C-593: direct LED segment drive.
  CF-593: direct fluorescent display drive.
- All other features listed on the first page of this section.

DESCRIPTION

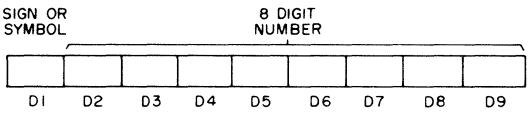
The C/CF-593 circuits are basic five-function circuits for use with nine digit LED or fluorescent displays. These circuits enter and compute both positive and negative numbers to an eight digit resolution. On overflow, the overflow symbol is displayed in the ninth digit position, the decimal point is automatically shifted eight positions to the left of its computed position and the keyboard is locked.

PIN CONFIGURATION
28 LEAD DUAL IN LINE

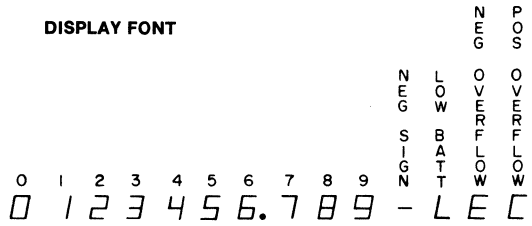


DISPLAY

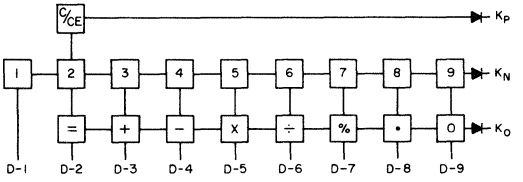
9 DIGIT DISPLAY



DISPLAY FONT



KEY MATRIX



Note: Diodes used only for CF-593.

9 Digit / 5 Function Basic Calculator Circuit With One-Key Memory

FEATURES

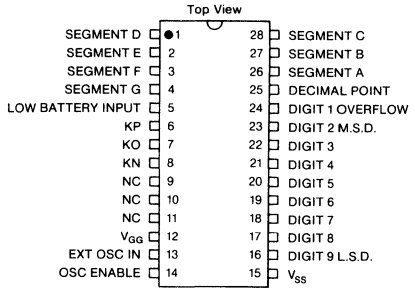
- 8 digit, 7 segment display outputs with ninth digit for sign or symbol.
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount).
- Floating negative sign.
- Right-justified entry and result.
- Results of addition or subtraction remain aligned to preceding number having most decimal places.
- One-key memory operation, with option for two additional memory function keys (refer to the description at the beginning of this section).
- C-594: direct LED segment drive.
  CF-594: direct fluorescent display drive.
- All other features listed on the first page of this section.

DESCRIPTION

The C/CF-594 circuits enable a manufacturer to add a memory calculator to his line with the simple inclusion of one additional memory key in the matrix of the C/CF-593 keyboard. All other operations are identical to the C/CF-593.

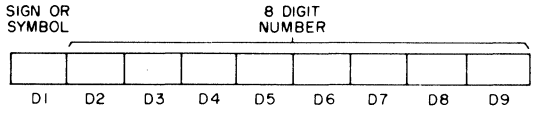
PIN CONFIGURATION

28 LEAD DUAL IN LINE

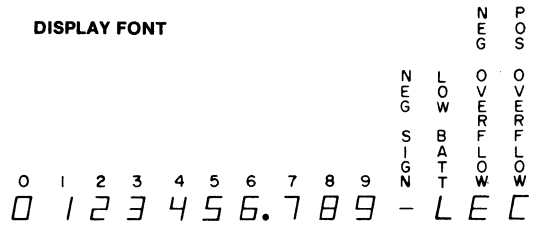


DISPLAY

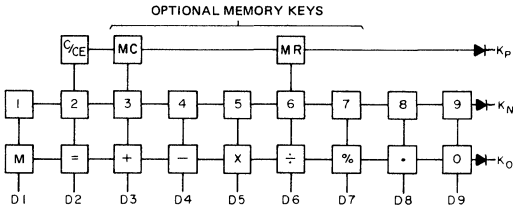
9 DIGIT DISPLAY



DISPLAY FONT



KEY MATRIX



Note: Diodes used only for CF-594.

9 Digit / 5 Function Basic Calculator Circuit With Multi-Key Memory

FEATURES

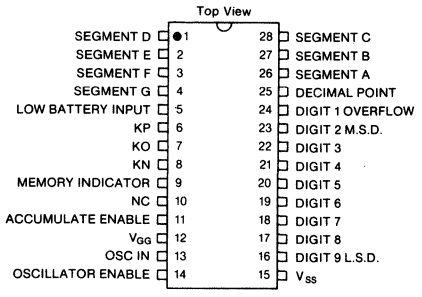
- 8 digit, 7 segment display outputs with ninth digit for sign or symbol.
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount).
- Floating negative sign.
- Right-justified entry and result.
- Results of addition or subtraction remain aligned to preceding number having most decimal places.
- Multi-key memory operation and automatic accumulating memory (refer to the description at the beginning of this section.)
- C-595: direct LED segment drive.
  CF-595: direct fluorescent display drive.
- All other features listed on the first page of this section.

DESCRIPTION

The C/CF-595 circuits add a variety of memory options to the basic C/CF-593 functions. While the basic pin configuration is identical to the C/CF-593, two additional connections are provided for a selectable "memory accumulate" switch and a "memory in use" indicator output.

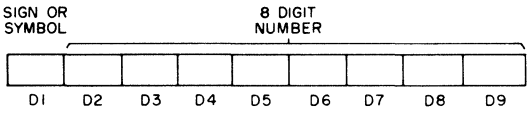
PIN CONFIGURATION

28 LEAD DUAL IN LINE

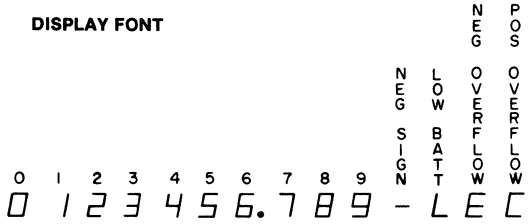


DISPLAY

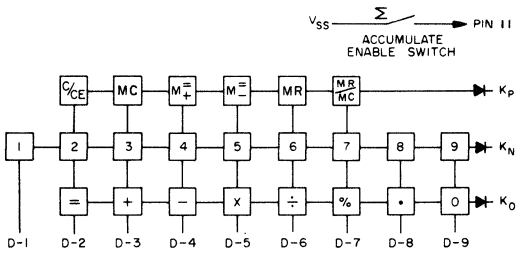
9 DIGIT DISPLAY



DISPLAY FONT



KEY MATRIX



Note: Diodes used only for CF-595.

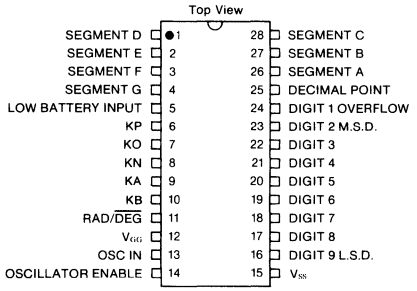
9 Digit / 15 Function Scientific Calculator Circuit

FEATURES

- Number entry in floating point or scientific notation.
- 9 digit output with 5 digits of the mantissa displayed, 2 digits for the exponent, and 2 digits for the sign of the mantissa and exponent.
  8 digit display and sign for numbers not requiring scientific notation or for the display of the 8 significant digits of a number that is in scientific notation.
- Basic four arithmetic functions (+, −, x, ÷).
- Transcendental functions (sin, cos, tan, $\sin^{-1}$, $\cos^{-1}$, $\tan^{-1}$, ln x and e^x).
- Convenience functions ($\sqrt{x}$, 1/x).
- A separate memory register (refer to the description at the beginning of this section).
- Trigonometric functions are performed in degrees or radians (switch selectable).
- π key to display the value of π.
- Left-justified entry and result.
- User option for single or dual function key operation.
- C-596: direct LED segment drive.
  CF-596: direct fluorescent display drive.
- All other features described on the first page of this section.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



DESCRIPTION

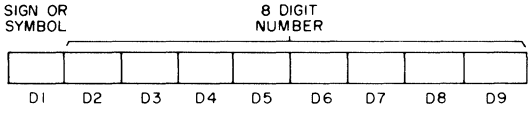
The C/CF-596 circuits are fifteen function circuits which offer trigonometric and inverse trigonometric functions, natural logs, e^x, $\sqrt{x}$, 1/x and π as well as the basic four functions and memory.

The circuit operates in the normal 8 digit mode until the display capacity is exceeded at which time it converts to the scientific mode of operation.

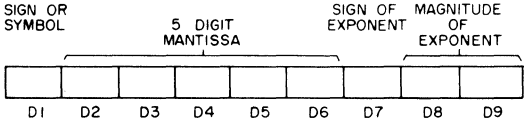
The C/CF-596 features single or dual function key operation for a keyboard configuration of from 19 to 35 keys.

DISPLAY

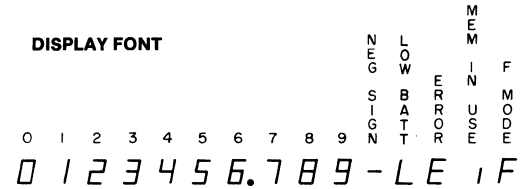
NORMAL MODE



SCIENTIFIC NOTATION

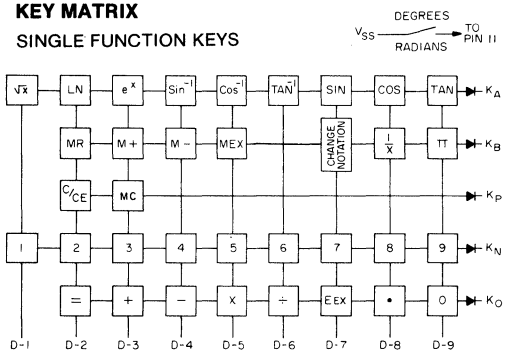


DISPLAY FONT

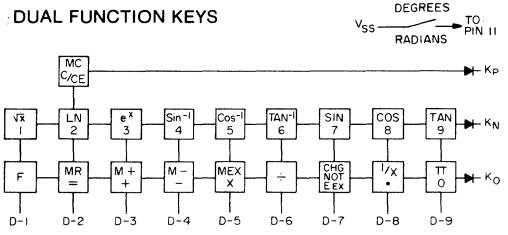


KEY MATRIX

SINGLE FUNCTION KEYS



DUAL FUNCTION KEYS



Note: Diodes used only for CF-596.

9 Digit / 18 Function Scientific Calculator Circuit

FEATURES

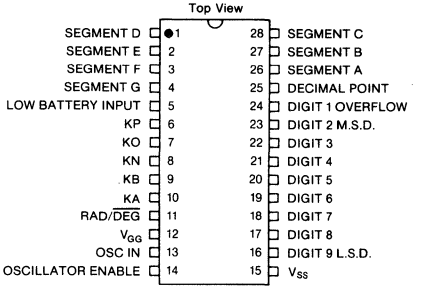
- Number entry in floating point or scientific notation.
- 9 digit output with 5 digits of the mantissa displayed, 2 digits for the exponent, and 2 digits for the sign of the mantissa and exponent.
- 8 digit display and sign for numbers not requiring scientific notation or for the display of the 8 significant digits of a number that is in scientific notation.
- Basic four arithmetic functions (+, −, x, ÷).
- Transcendental functions (sin, cos, tan, $\sin^{-1}$, $\cos^{-1}$, $\tan^{-1}$, ln x, e^x, $\log_{10}$ and 10^x).
- Convenience functions ($\sqrt{x}$, 1/x, y^x).
- A separate memory register (refer to the description at the beginning of this section).
- Trigonometric functions are performed in degrees or radians (switch selectable).
- π key to display the value of π.
- Left-justified entry and result.
- User option for single or dual function key operation.
- C-598: direct LED segment drive.
  CF-598: direct fluorescent display drive.
- All other features described on the first page of this section.

DESCRIPTION

The C/CF-598 circuits are eighteen function circuits whose operations are identical to the C/CF-596 with the addition of three functions: $\log_{10}$, 10^x and Y^x. Single or dual function key operation is optional with keyboard configurations of from 21 to 38 keys.

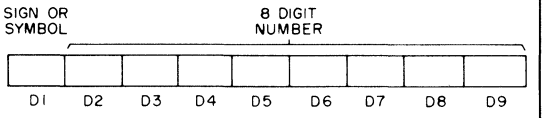
PIN CONFIGURATION

28 LEAD DUAL IN LINE

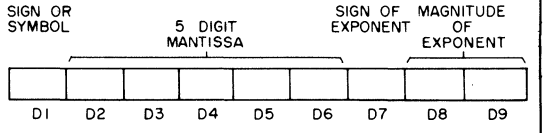


DISPLAY

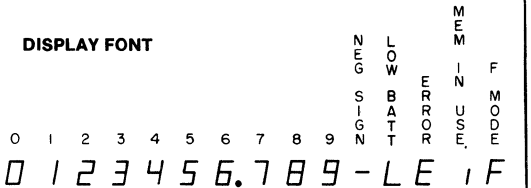
NORMAL MODE



SCIENTIFIC NOTATION

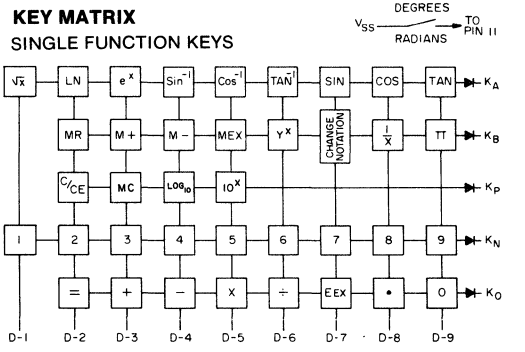


DISPLAY FONT

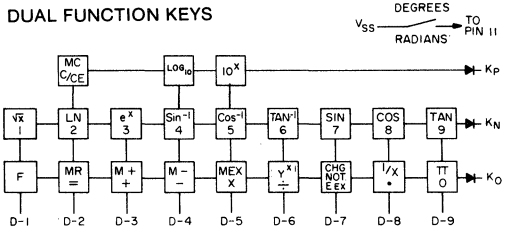


KEY MATRIX

SINGLE FUNCTION KEYS



DUAL FUNCTION KEYS



Note: Diodes used only for CF-598.

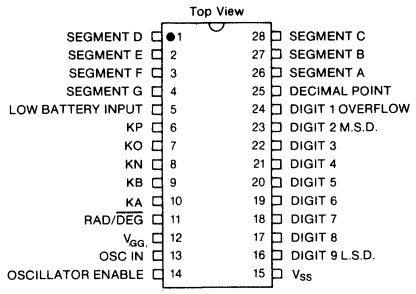
9 Digit / 21 Function Scientific Calculator Circuit

FEATURES

- Number entry in floating point or scientific notation.
- 9 digit output with 5 digits of the mantissa displayed, 2 digits for the exponent, and 2 digits for the sign of the mantissa and exponent.
- 8 digit display and sign for numbers not requiring scientific notation, or for the display of the 8 significant digits of a number that is in scientific notation.
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount)
- Transcendental functions (sin, cos, tan, $\sin^{-1}$, $\cos^{-1}$, $\tan^{-1}$, ln x, e^x, $\log_{10}$ and 10^x).
- Convenience functions ($\sqrt{x}$, $^1/x$, y^x, x^2, +/-).
- A separate memory function (refer to the description at the beginning of this section).
- Two levels of parentheses.
- Trigonometric functions are performed in degrees or radians (switch selectable).
- π key to display the value of π.
- Left-justified entry and result.
- User option for single or dual function key operation.
- C-599: direct LED segment drive.
  CF-599: direct fluorescent display drive.
- All other features described on the first page of this section.

PIN CONFIGURATION

28 LEAD DUAL IN LINE

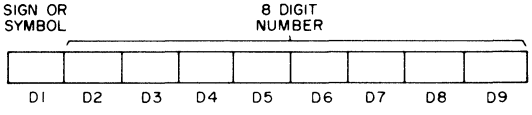


DESCRIPTION

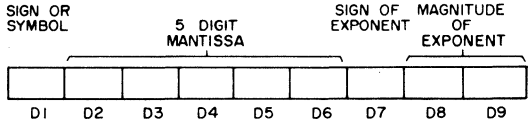
The C/CF-599 circuits are twenty-one function circuits whose operations are identical to the C/CF-598 with the addition of two levels of parentheses and three functions: x^2, % and +/-. Single or dual function key operation is optional with keyboard configurations of from 24 to 41 keys.

DISPLAY

NORMAL MODE



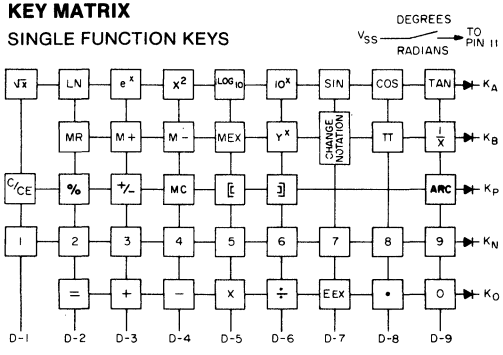
SCIENTIFIC NOTATION



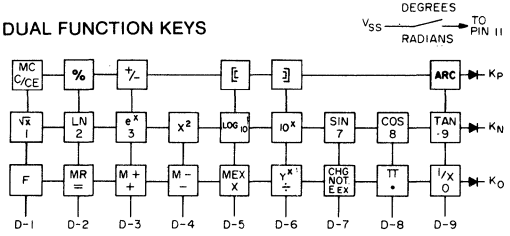
DISPLAY FONT

KEY MATRIX

SINGLE FUNCTION KEYS



DUAL FUNCTION KEYS



Note: Diodes used only for CF-599.

Printer Calculator Circuits

FEATURES

- 12 digit printout plus 2 full right-hand justified audit trail columns.
- 5 functions (+,−,×,÷,%).
- Chain calculations.
- Rounding options (truncate, 5/4 round off, 1/0 round up).
- Repeat add/subtract.
- Automatic underflow and reverse underflow.
- Non-add (#)/date key.
- Memory non-zero indicators.
- Overflow indication.
- Automatic constant in multiply or divide.
- Right-justified entries and results.
- Leading zero suppression.
- 2 key rollover operation.
- Internal oscillator and power-on clear.

DESCRIPTION

The C-700 Series is a growing family of circuits for the printing calculator manufacturer which provide the capability for a broad-based, multi-feature business calculator product offering. The C-700 Series currently includes three different calculator circuits (the C-717, C-717X and C-718) and a printer-display interface circuit (C-719), each described on the following pages of this section.

STANDARD CHARACTER LAYOUT

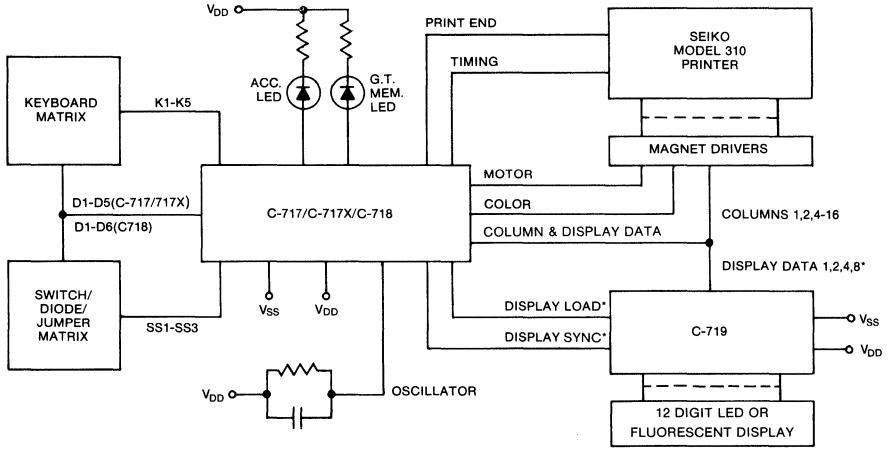
SEIKO MODEL 310 PRINTER

PRINT COLUMNS

16	15	11	13	12	11	10	9	8	7	6	5	4	3	2	1	
0	0	0	0	0	0	0	0	0	0	0	0	0		=	C	1
1	1	1	1	1	1	1	1	1	1	1	1	1		+	I	2
2	2	2	2	2	2	2	2	2	2	2	2	2		−	II	3
3	3	3	3	3	3	3	3	3	3	3	3	3		×	R	4
4	4	4	4	4	4	4	4	4	4	4	4	4		÷	5/4	5
5	5	5	5	5	5	5	5	5	5	5	5	5		↕	√	6
6	6	6	6	6	6	6	6	6	6	6	6	6		%	A	7
7	7	7	7	7	7	7	7	7	7	7	7	7		S	M	8
8	8	8	8	8	8	8	8	8	8	8	8	8		≠	K	9
9	9	9	9	9	9	9	9	9	9	9	9	9		◊	E	10
•	•	•	•	•	•	•	•	•	•	•	•	•		*	M+	11
—	—	—	—	—	—	—	—	—	—	—	—	—		T	M−	12

CHARACTER POSITIONS

SYSTEM INTERCONNECT DIAGRAM



*DISPLAY SIGNALS ONLY ON C-717X AND C-718.

12 Digit / 5 Function Printing Calculator Circuits with Accumulating and Grand Total Memories

FEATURES

- Automatic accumulating memory (stores group totals).
- Grand total memory.
- Selectable memory modes: normal (last entry printed); (running subtotal printed); GT (grand total memory access).
- Fully arithmetic operation.
- Decimal select modes: full floating; fixed point (0-6); add mode (with hardwired secondary add mode option for quantity × dollars).
- Multistage keyboard buffer stores up to 12 keyed entries to allow uninterrupted operation during print.
- C-717: printer only.
  C-717X: printer and display (with the C-719 interface chip).
- All other features listed on the General Information page.

DESCRIPTION

The C-717 and C-717X are each single MOS/LSI circuits containing all the logic functions required to implement a five-function, two memory general purpose business calculator using a Seiko Model 310 impact printer. While both the C-717 and C-717X are pin-compatible with each other, the C-717X additionally provides signals for use with the C-719 printer-display interface chip. This allows the addition of a 12-digit fluorescent or LED display to the basic printer.

PIN CONFIGURATION

40 LEAD DUAL IN LINE

Top View

V_{SS}(GND)	1	40	K2
K3	2	39	K1
K4	3	38	Column 6
K5	4	37	Column 7/Display Data 1*
V_{DD}(-15V)	5	36	Column 8/Display Data 4*
Column 5	6	35	Column 9/Display Data 8*
Column 4	7	34	Column 10/Display Data 2*
Column 2	8	33	Column 11
Column 1	9	32	Oscillator/Clock Input
Timing	10	31	GT LED
Print End	11	30	Acc. LED
Motor	12	29	Column 12
Color	13	28	Column 13
Column 16	14	27	Column 14
D1	15	26	Column 15
D2	16	25	Display Load (N.C. on C-717)
N.C.	17	24	Display Sync (N.C. on C-717)
D3	18	23	SS2
D4	19	22	SS3
D5	20	21	SS1

*NOTE: On the C-717X, pins 34-37 are multifunction pins with both display data and column 7—10 data. On the C-717, these pins are single-function containing only column 7—10 data.

KEYBOARD SWITCH MATRIX

	D1	D2	D3	D4	D5
K1	0	5	00	.	=
K2	1	6	000	+	%
K3	2	7	=+	−	*
K4	3	8	=−	×	◊
K5	4	9	# DATE	÷	C/CE

STATIC SWITCH MATRIX

	D1	D2	D3	D4	D5
SS1	DECIMAL SELECT- SEE CHART				
SS2			ADD MODE OPTION		PRINTER ON/OFF
SS3	◊ MODE	GT MODE	PAPER ADVANCE	TRUNCATE	ROUND OFF

DECIMAL SELECT CHART

The decimal select switch is a four-pole switch with encoded outputs during D1 thru D4 strobe periods. In the chart below, a '1' denotes a switch closure.

DECIMAL POSITION	D1	D2	D3	D4
+	1	1	0	1
F	1	0	0	1
0	1	0	0	0
1	0	1	0	0
2	1	1	0	0
3	0	0	1	0
4	1	0	1	0
5	0	1	1	0
6	1	1	1	0

12 Digit / 5 Function Printing Calculator Circuit with Accumulator, Item Counter and Independent Memory

FEATURES

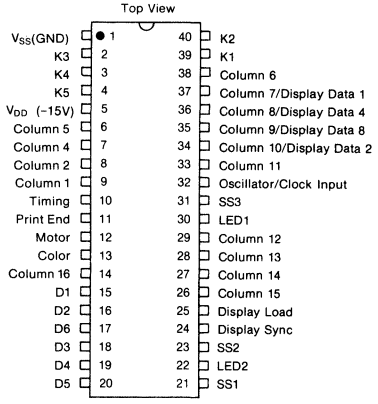
- Switch-selectable automatic accumulation.
- Three digit item counter.
- Four-key independent memory.
- Arithmetic operation in add/subtract sequences, algebraic in multiply/divide (business logic).
- Decimal select modes: full floating; fixed point (0-6, excluding 5); add mode (automatic decimal 2 in + and −, unit/price mode in ×, price/unit mode in ÷.).
- Non-coded decimal select switch input.
- Separate clear-all key.
- Full floating accuracy on intermediate results in chain operation.
- Multistage keyboard buffer stores up to 6 keyed entries to allow uninterrupted operation during print.
- Display capability (with the C-719 interface chip).
- All other features listed on the General Information page.

DESCRIPTION

The C-718 is a single MOS/LSI circuit containing all the logic functions required to implement a five-function general purpose business calculator with an accumulator, item counter and four-key independent memory. The C-718 has been designed to operate with a Seiko Model 310 16 column impact printer. When used with the C-719 printer-display interface, the C-718 also provides a 12-digit display capability, using either fluorescent or LED displays.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



KEYBOARD SWITCH MATRIX

	D1	D2	D3	D4	D5	D6
K1	0	5	00	.	=	M+
K2	1	6	CA	+	%	M−
K3	2	7	=+	−	*	M◊
K4	3	8	=−	×	◊	M*
K5	4	9	# DATE	÷	C/CE	N

STATIC SWITCH MATRIX

	D1	D2	D3	D4	D5	D6
SS1	ACC	Paper Advance	5/4	ROUND OFF	PRINTER ON/OFF	
SS2	4	5	6		M/A	TEST
SS3	+	F	O	1	2	3

NOTE:
Positions SS2-D1,D2,D3 and SS3-D1 thru D6 are the decimal select positions.

Printer-Display Interface Circuit

FEATURES

- Adds display capablity to C-717X and C-718 printer chips.
- Full 12 digit display capability.
- Drives LED or fluorescent displays.

DESCRIPTION

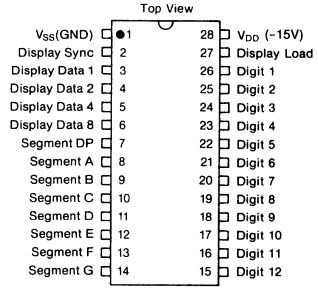
The C-719 is a single MOS/LSI circuit designed to add a 12 digit display capability to General Instrument's C-717X and C-718 printer calculator circuits. Data from the printer calculator chips is transferred to the C-719 interface chip serially and re-formulated to drive seven segment multiplexed common cathode displays.

The segment and digit outputs of the C-719 are open-drain and have a breakdown voltage of −30 Volts to enable the driving of fluorescent displays with a minimum of interface components. LED displays may also be driven by the C-719 with direct drive of the segments and the addition of digit-drive buffers.

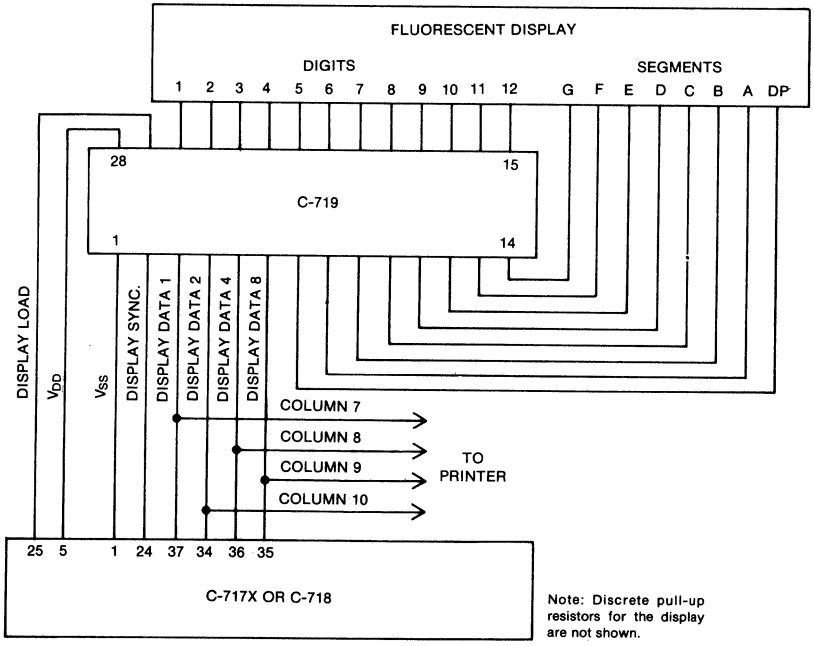
In the display, leading zeroes are suppressed and entries and results are right-justified.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



SYSTEM DIAGRAM



Note: Discrete pull-up resistors for the display are not shown.

GENERAL INSTRUMENT

AY-5-1200A
AY-5-1202A
AY-5-1203A
AY-5-1204A
AY-5-1224A
CK3000
CK3100
CK3200
CK3300
CK3400

3

4 Digit Clock Circuits

FEATURES

- Hours and minutes display.
- 12/24 hour operation.
- 50/60Hz operation.
- High voltage direct Fluorescent drive Outputs.
- Flashing seconds output (option).
- BCD output (option).
- Leading Zero Blanking (option).
- Power-On Reset to zero.
  (Counting does not start until time is set.)
- Options:

	7 Seg	BCD	Zero Blank	Flashing Sec
AY-5-1200A	Yes	No	Yes	No
AY-5-1202A	Yes	No	Yes	Yes
AY-5-1203A	No	Yes	No	No
AY-5-1204A	Yes	No	No	Yes

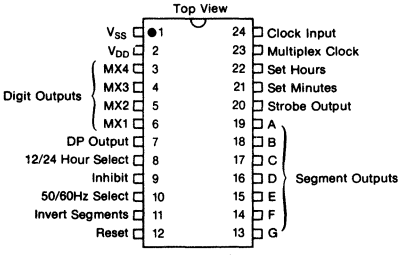
DESCRIPTION

The AY-5-1200A Series are P-Channel MOS integrated circuits, containing all the logic necessary to make a 4 digit, 12 or 24 hour clock, operating from 50 or 60Hz. High voltage output stages capable of driving fluorescent displays are provided.

PIN CONFIGURATION

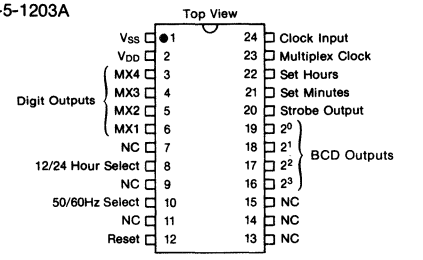
24 LEAD DUAL IN LINE

AY-5-1200A/AY-5-1202A/AY-5-1204A

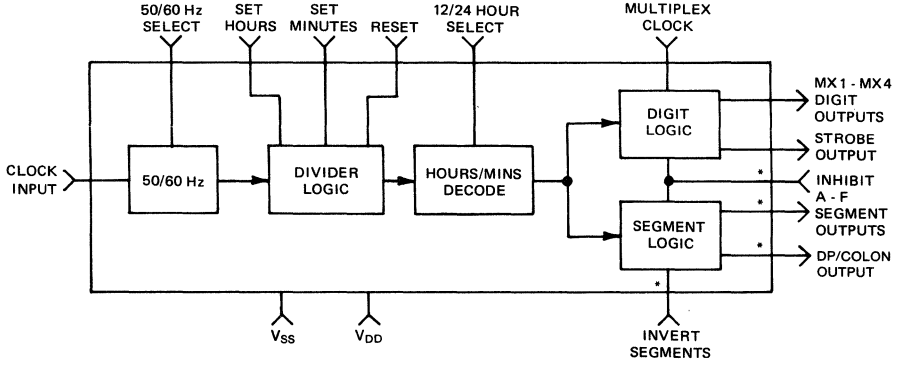


24 LEAD DUAL IN LINE

AY-5-1203A



BLOCK DIAGRAM



* Not included in the AY-5-1203A.
Four BCD outputs are provided in place of the seven segment outputs.

PIN FUNCTIONS

Name	Function
Segment Outputs A—F	In 7 segment mode the digits are multiplexed on to these pins. These outputs are at logic '0' to display (positive) and will drive Fluorescent displays directly. In BCD mode outputs A to D are used, the code for 0 being 0000.
Decimal Point Output	This is a high voltage output intended to drive a decimal point or colon. It is enabled during the MX3 time slot and can flash once per second if required.
Multiplex Outputs MX1—MX4	These outputs select the display digits sequentially, they will drive Fluorescent displays directly. Five multiplex time slots are generated the fifth one being blank. Minutes are output in MX1 time, 10's of hours in MX4 time.
Reset Input	When taken to logic '0' the clock is reset to zero.
Set Minutes Input	When taken to logic '0' the minutes counter is advanced at the rate of 2 min. per sec. and the hours counter at the rate of 2 hours per minute.
Set Hours Input	When taken to logic '0' the hours counter is advanced at the rate of 2 hours per second.
50/60Hz Select Input	When taken to logic '0', 60Hz operation will result.
12/24 Hours Select Input	When taken to logic '0', 12 hour operation will result.
Invert Segments Input	When taken to logic '0' the segment outputs will be inverted.
Multiplex Oscillator	An external capacitor is used to select the multiplex frequency. If required the pin can be driven by an external oscillator.
50/60Hz Input	The master clock is input to the pin. Hysteresis is provided so that the input waveform is not critical.
V_{SS}	Positive Supply.
V_{DD}	Negative Supply.
Inhibit Input	When taken to logic '0' all outputs are switched OFF.
Strobe Output	This is a short pulse occurring during the middle of each multiplex period.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin
(except Segment and Multiplex outputs) . . . . . +0.3 to -35V
Operating Temperature Range. . . . . 0°C to +70°C
Storage Temperature Range . . . . . -65°C to +150°C
Power Dissipation at +70°C Ambient—Total 500mW
Per Output. 50mW

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
V_{DD} = -17V ±10%
Operating Temperature (T_A) = 0°C to +70°C

Characteristic	Min.	Typ**	Max	Units	Conditions
Clock input frequency	DC	50/60	—	Hz	
Clock input logic '0'	+0.5	—	−2	Volts	Note 1
Clock input logic '1'	−8	—	V_{DD}	Volts	
Multiplex clock frequency	DC	—	50	KHz	Note 2
Control inputs logic '0'	+0.3	—	−1.5	Volts	
Control inputs, current logic '0'	—	100	—	μA	Note 3
Control inputs logic '1'	−6	—	$-V_{DD}$	Volts	
Segment Outputs					
ON current	2	—	—	mA	V_{OUT} = −2V
OFF leakage	—	—	5	μA	V_{OUT} = −25V
	—	—	10	μA	V_{OUT} = −35V
Multiplex Outputs					
ON current	5	—	—	mA	V_{OUT} = −2V
OFF leakage	—	—	5	μA	V_{OUT} = −25V
	—	—	10	μA	V_{OUT} = −35V
Supply Current	—	8.5	14	mA	

**Typical values are at +25°C and nominal voltages.

NOTES:
1. The clock input pin may be taken positive with respect to V_{SS} provided that the current is limited to 100μA. The input will behave like a forward biased silicon diode in this condition.
2. The frequency is determined by an external capacitor.
3. These inputs have a 170Kohm pull up resistor to V_{DD}.

4 Digit Clock Circuit

FEATURES

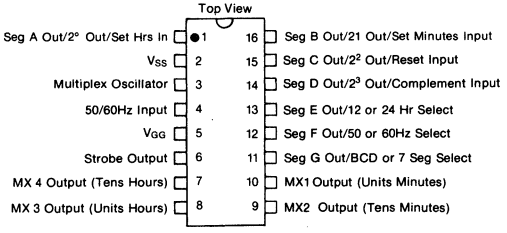
- 12/24 hour operation.
- Leading zero blanking in 12 hour mode.
- 50 or 60 Hz clock input.
- Hours and minutes display (4 digits).
- 7 segment outputs direct LED drive or TTL compatible BCD outputs.
- Complement control for segment outputs.
- Interdigit blanking for gas discharge displays.
- On chip multiplex oscillator.
- Single 15V supply.
- Power-On Reset to zero. (Counting does not start until time is set.)

DESCRIPTION

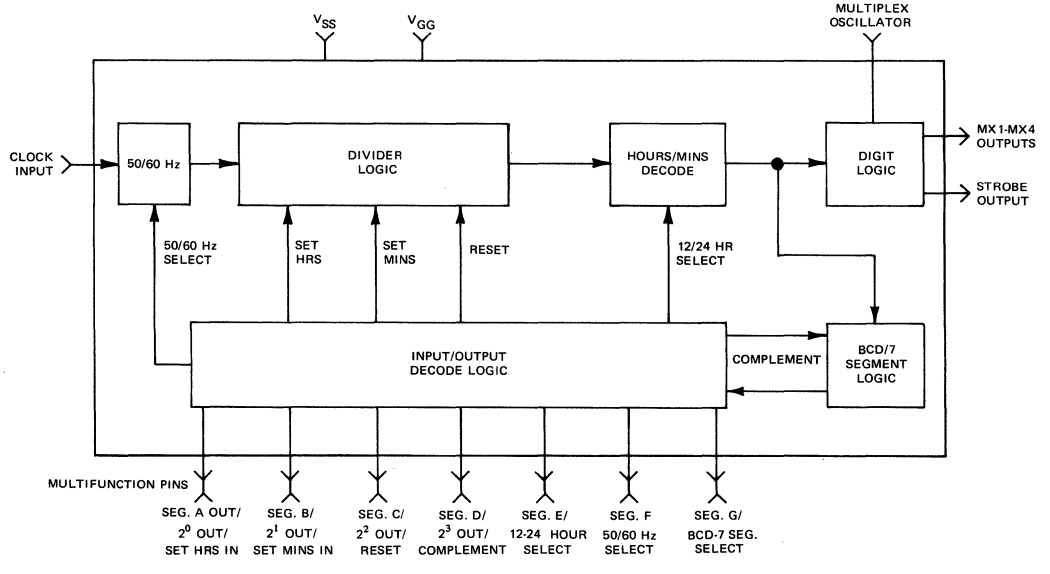
The AY-5-1224A is a P channel MOS integrated circuit containing all the logic necessary to make a 4 digit, 12 or 24 hour clock operating from a 50 or 60Hz input. It has multiplexed BCD or 7-segment outputs and will drive LED, Fluorescent and Gas discharge displays with the minimum of interfacing.

PIN CONFIGURATION

16 LEAD DUAL IN LINE



BLOCK DIAGRAM



PIN FUNCTIONS

Pins 1 and 11 to 16 are multifunction. During multiplex times 1 to 4 they function as data outputs, either 7 segment code or BCD according to the display mode selected. During multiplex time 5 (Strobe) they function as inputs.

Segment Outputs A-G (Pins 1 and 11 to 16)
In 7 segment mode the digits are multiplexed out on to these pins. Normally the outputs are at logic '0' (positive to display). Inter-digit blanking for ¼ the digit time is incorporated for gas discharge displays.

BCD Outputs 2^0—2^3 (Pins 1, 16, 15, 14)
In BCD mode the digits are multiplexed on to these pins in BCD code. Normally the outputs are at logic '0' (positive), i.e. code 0=0000.

Multiplex Outputs 1-4 (Pins 10, 9, 8, 7)
These pins are successively switched to logic '0' to select appropriate digit display. A fifth multiplex time (Strobe) is used to enable the control inputs. These outputs have interdigit blanking. The multiplex rate is 1/20th the multiplex clock frequency.

Strobe Output (Pin 6)
This pin is used to enable the control input keyboard, it goes to logic '0' to enable.

Set Hours Input (Pin 1)
When taken to logic '0' during strobe time this input causes the hours counter to advance at the rate of 1 hour per second.

Set Min Input (Pin 16)
When taken to logic '0' during strobe time this input causes the minutes counter to advance at the rate of 1 minute per second and the hours counter to advance at the rate of 1 hour per minute.

Reset Input (Pin 15)
When taken to logic '0' during strobe time this input causes the clock to reset to zero.

Complement Input (Pin 14)
When left open the segments and BCD outputs will have normal polarity. When connected to Strobe output via a diode the 7 segment and BCD output will be inverted.

12/24 Hour Select (Pin 13)
When left open the clock will run in the 12 hour mode, when connected to strobe via a diode 24 hour operation will result.

50/60Hz Select (Pin 12)
When left open a 50Hz clock will be accepted. When connected to strobe via a diode 60 Hz operation will result.

BCD/7 Segment Select (Pin 11)
When left open 7 segment outputs will be provided, when connected to strobe via a diode BCD outputs will be provided.

50/60Hz Input (Pin 4)
The master clock (50 or 60Hz) is input to this pin. Hysteresis is provided on the input so that the input wave form is not critical.

Multiplex Oscillator (Pin 3)
An external capacitor is used to set the multiplex frequency. If required this input can be driven by an external oscillator.

V_{SS} (Pin 2)
Positive supply line nominally OV.

V_{GG} (Pin 5)
Negative supply line nominally -15V.

Power-On Reset
At power-on the chip is reset to zero. Counters will not start until Set Hours or Set Minutes has been activated.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} . . . . . +0.3 to −20V
Operating Temperature Range . . . . . 0° to +70°C
Storage Temperature Range . . . . . −65°C to +150°C
Power Dissipation at 70°C Ambient—Total 500mW
Per Output. 50mW

*Exceeding these ratings could cause permanet damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

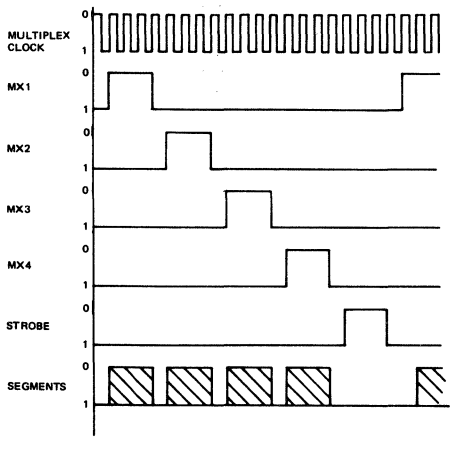
V_{SS} = 0V
V_{GG} = −12 to −18V
Operating Temperature (T_A) = 0°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
Clock input frequency	DC	50/60	—	Hz	—
Clock input logic '0'	+0.5	—	−2	Volts	Note 1
Clock input logic '1'	−8	—	V_{DD}	Volts	—
Multiplex Clock Frequency	DC	—	50	KHz	Note 2
Interdigit Blanking	—	150	—	μs	at 6.67 KHz Note 3
Control inputs logic '0'	+0.3	—	−1.5	Volts	—
Control inputs logic '1'	−6	—	V_{DD}	Volts	—
Outputs Logic '0'	—	—	500	Ohms	V_{OUT} = -2V, I_{OUT} = 4mA
Outputs Logic '1' (Leakage)	—	—	10	μA	V_{OUT} = −18V
Supply Current	—	—	10	mA	V_{GG} = -15V

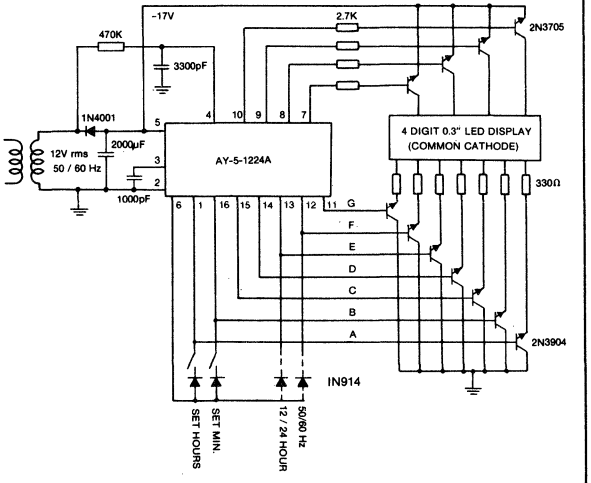
**Typical values are at +25°C and nominal voltages.

NOTES:
1. The clock input pin may be taken position with respect to V_{SS} provided that the current is limited to 100μA. The input will behave like a forward biased silicon diode in this condition.
2. The frequency is determined by an external capacitor.
3. At 6.67KHz multiplex frequency the digit ON time is 450μS and the OFF time is 150μS.

TIMING DIAGRAMS



AY-5-1224A WITH 0.3" LED DISPLAY



4 Digit Alarm Clock Circuit

FEATURES

- 12 Hour clock, 24 Hour alarm setting
- AM/PM indication
- 50 or 60 Hz operation
- Snooze (Sleep-over) alarm
- Direct display driving
  - CK3000- Plasma
  - CK3100 - LED
- No display interface components
- Seconds flashing colons
- Alarm, set, and snooze indication
- Power interrupt indication
- Low current consumption
- Alarm output tone - direct drive with magnetic speakers
- Wake output for appliance switching (CK3100)

DESCRIPTION

The CK3000 and CK3100 are N-Channel MOS integrated circuits, containing all the logic necessary to produce low cost 4 digit alarm clocks operating from 50 or 60 Hz line frequencies. The output stages of these circuits have been designed specifically to directly drive the cathodes of Plasma displays (CK3000) or the cathodes of large digit common anode L.E.D.'s (CK3100) with no interface electronic components whatsoever.

These integrated circuits also contain all the logic needed for contact noise elimination and line frequency noise rejection reducing further support components.

PIN CONFIGURATION

40 LEAD DUAL IN LINE
CK3000

Top View

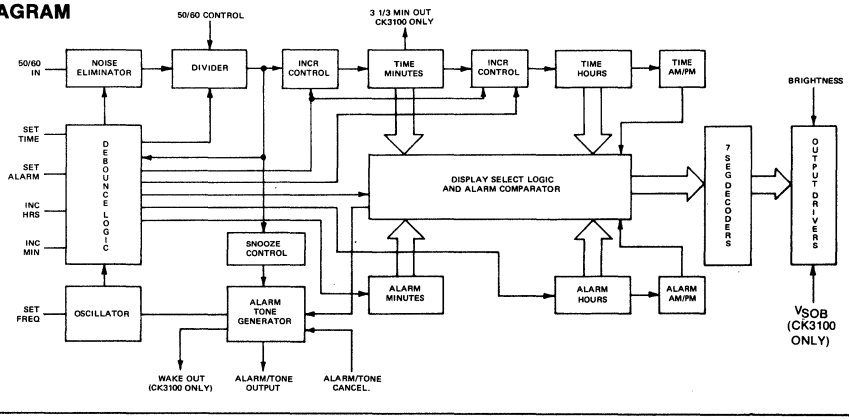
V_N	1	40	N/C (do not connect)
50/60 Hz Control	2	39	Seg. Out. a, Digit 1
Alarm/Tone Cancel	3	38	Seg. Out. b, Digit 1
Alarm Tone Output	4	37	Seg. Out. g, Digit 1
Set Internal Frequency	5	36	Seg. Out. c, Digit 1
Set Time Enable	6	35	Seg. Out. d, Digit 1
Set Alarm Enable	7	34	Seg. Out. e, Digit 1
Increment Min. Enable	8	33	Seg. Out. f, Digit 1
Increment Hr. Enable	9	32	Seg. Out. a, Digit 2
50/61 Hz Input	10	31	Seg. Out. b, Digit 2
V_P	11	30	Seg. Out. g, Digit 2
Seg. Current Control	12	29	Seg. Out. c, Digit 2
V.S.O Control	13	28	Seg. Out. d, Digit 2
AM/PM Ind Seg. Out.	14	27	Seg. Out. e, Digit 2
Seg. Out. b, Digit 4	15	26	Seg. Out. f, Digit 2
Seg. Out. c, Digit 4	16	25	Colon/Clock
Seg. Out. a, Digit 3	17	24	Colon/Alarm
Seg. Out. f, Digit 3	18	23	Seg. Out. b, Digit 3
Seg. Out. g, Digit 3	19	22	Seg. Out. c, Digit 3
Seg. Out. e, Digit 3	20	21	Seg. Out. d, Digit 3

40 LEAD DUAL IN LINE
CK3100

Top View

V_N	1	40	Wake Output
3.33. Min. Out.	2	39	Seg. Out. a, Digit 1
50/60 Hz Control	3	38	Seg. Out. b, Digit 1
Alarm/Tone Cancel	4	37	Seg. Out. g, Digit 1
Alarm Tone Output	5	36	Seg. Out. c, Digit 1
Set Internal Frequency	6	35	Seg. Out. d, Digit 1
Set Time Enable	7	34	Seg. Out. e, Digit 1
Set Alarm Enable	8	33	Seg. Out. f, Digit 1
Increment Min. Enable	9	32	Seg. Out. a, Digit 2
Increment Hr. Enable	10	31	Seg. Out. b, Digit 2
50/60 Hz Input	11	30	Seg. Out. g, Digit 2
V_P	12	29	Seg. Out. c, Digit 2
Seg. Out. Blanking	13	28	Seg. Out. d, Digit 2
AM/PM Ind Seg. Out.	14	27	Seg. Out. e, Digit 2
Seg. Out. b, Digit 4	15	26	Seg. Out. f, Digit 2
Seg. Out. c, Digit 4	16	25	Colon/Clock
Seg. Out. a, Digit 3	17	24	Colon/Alarm
Seg. Out. f, Digit 3	18	23	Seg. Out. b, Digit 3
Seg. Out. g, Digit 3	19	22	Seg. Out. c, Digit 3
Seg. Out. e, Digit 3	20	21	Seg. Out. d, Digit 3

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The block diagram shows diagramatically the various logical function blocks that make up the CK3000 and CK3100 integrated circuits. The various units have the following functions.

Oscillator

The oscillator provides two basic functions in the integrated circuit.

1. Provides a suitable frequency in the audio range for modulating an external transducer at and during the alarm time (nominally 1 KHz).
2. Provides a strobe frequency for strobing the 50 or 60 Hz line frequency into a 'D' type flip flop to statistically eliminate line noise (nominally 250 Hz).

Debounce Logic

The logic here is used to eliminate contact noise closure on any input line and this is achieved using one second digital one shots in combination with 250 Hz strobe pulses. e.g. with the set-time or alarm enable inputs at logic zero the increment inputs are looking for one contact closure in each one second period. Any further closures are ignored. However if any increment pin is at logic zero and the set alarm set time switch is open and closed multiple counting will result. This logic also directs increment signals to the appropriate counters.

Divider

The divider counts down the line frequency counts to one per second depending on the 50/60 Hz control.

Snooze Control

This logic stores the information that an alarm compare has been reached, and initiates a 5 minute counter, which then runs continuously until such time that on an exact multiple of five minutes if the alarm/tone control switch is at zero, it will then stop and reset the alarm compare store. During the 5 minutes the alarm tone is made active for 1 minute in each five, producing a 1 Hz modulated 1 KHz tone. If when the alarm tone is active the alarm tone cancel is taken to logical zero the tone will cease until the next five minute period.

50/60Hz Control

For 50 Hz operation - Connect to V_P or leave open circuit
For 60 Hz operation - Connect to V_N

Alarm/Tone Cancel - Tone Output

For normal operation the alarm cancel input is left open circuit. Under this condition any coincidence between the time and alarm store will cause the alarm tone to output on alarm tone pin. This tone will remain present for one minute unless cancelled by momentarily connecting alarm cancel to a logical '0'. This tone will re-occur five minutes (and subsequent multiples of 5 minutes) after the original alarm time for a duration of one minute unless cancelled by momentary connection of tone cancel to a logic '0', thus providing a snooze facility.

To completely cancel the alarm sequence, the coincidence of the alarm cancel pin being at a logical 0 and the start of the next alarm tone period is required. Immediately after this occurrence the alarm cancel input may be open circuited and the alarm will be re-enabled for the following day.

Alternatively if either the set time or set alarm inputs are connected momentarily to a logical '0' after the first minute of alarm, the alarm logic will be re-triggered for the next day.

The alarm tone is a nominal 1 KHz square wave chopped by a 1 Hz square wave.

Frequency Set

An external resistor to V_P and external capacitor to V_N are used to control the frequency of the oscillator. These values should be selected to ensure appropriate 4 KHz oscillation.

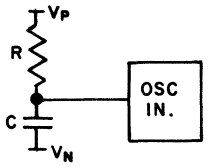


Fig.1

Typical Values for 4KHz:
R = 680K
C = 2200pF
} for V_P = 15V

Figure 3 shows frequency vs. capacitance and resistance for nominal supply voltage.

Figure 4 gives a guide to component values for different V_P values.

With the oscillator set to 4KHz, the alarm tone output will be 1KHz, and the internal antibounce logic is strobed at 250 Hz.

Setting Up Procedure (Pins 6 thru 9)

In the normal clock running condition pins 6 thru 9 should be open circuit or at a logical '1'.

To enter set mode either set time or set alarm should be pulled to logical '0'. Under this condition the increment minutes and increment hours inputs are enabled and when either is pulled to a logical '0' then the corresponding hours and minutes will increment at a 1 Hz rate. All minutes to hours carries are suppressed while time is being set.

When set alarm is at a logical '0' the contents of the alarm store are displayed.

When set time/increment minutes occurs, the clock is stopped and remains stopped with the seconds reset until set time is open circuited or returned to a logical '1'. This enables the clock to be easily synchronized to an independent time source. No other setting conditions interrupt the seconds.

50/60Hz Input

This input accepts a line frequency signal at either 50 or 60 Hz and is subsequently used as the basic count time base.

Segments Output Control (Brightness) - CK3000

All output stages consist of a three device cascade configuration of which one device controls the output voltage current characteristics. (See Fig. 7.) From the characteristics it will be seen that a wide range of operating conditions are possible, allowing operation in either the resistive region (V proportional to I) or the constant current region. (I independent of V). Note that during device operation 24 of the 26 available segments can be on simultaneously, so in setting the device operating point it is important that each output stage does not exceed (on an average basis) one twenty fourth of the peak allowable package dissipation, i.e. approximately 20 mW per output.

It is also important that the display V-I load characteristic does not interrupt the avalanche region of the output device characteristic or off segment glow will be observed or in the limit device malfunction or damage can occur.

The output stages and control brightness were designed to be used with half line cycle anode voltage and a corresponding half cycle control of brightness to ensure the display is: (a) Off during segment data changes, and (b) To allow current to turn off and on in display gradually. Which will result in almost a total absence of R.F.I.

Segments Output Control (Blanking) - CK3100

Due to the high current handling capabilities of the output stages of this I.C., it is not possible to control the output V.I. characteristic by using a second series device. To regulate the display to the required brightness several options are possible externally and the following internally. The segment output control can turn off the display at any time by taking this input to a logical '0'. It is possible therefore to use half or full wave rectified signal on this display anode and prematurely shut the display down in each line cycle to control the conduction angle hence, average light output, using this control pin in phase relationship to the anode wave form.

Stand Off Voltage (VSO) — CK3000
The voltage on this pin influences the voltage current characteristics of the segment drives, its prime purpose is to enable the segment outputs to withstand more than 30 volts. Any voltage from 5 volts to V_P will ensure that 45 volts can be withstood through a plasma tube off-segment. For ease of operation it is suggested that V.S.O. is connected to V_P.

AM/PM Indicator
This output is an additional segment driver which can be used to give AM/PM indicator. (voltage current characteristic as other segments).

Cathode (Segment) Output Drivers (Pins 15 thru 39) — CK3000
All these pins drive the cathodes of the display without any additional interface components. These outputs are designed to withstand higher voltage signals than the other outputs. The output characteristics of the segment drivers can be controlled by pin 12 (See Figs.7 and 8).

Cathode (Segment) Drivers (Pins 15 thru 39) — CK3100
The output drivers of the CK3100 have sufficient current handling capabilities to drive even the most inefficient of today's available L.E.D.'s.

The output characteristics of the segments are shown in (Fig.5). Note: It is recommended that the package power dissipation be kept below 500mW, therefore, with a possible 24 simultaneous outputs being on together then each segment should be operated with an average power level of 21 mW or on average current of 15mA. The peak current for maximum number of segments condition (i.e. 24) should not exceed 40 mA per segment or the device will suffer permanent damage.

Colon Utilization (Pins 24 and 25)
Two colons show alarm/clock condition.

Clock	Alarm	Colon A	Colon B
Stopped/Setting	Don't care	Off	Off
Running	Set	1 Hz flash.	1 Hz flash.
Running	Not set	1 Hz flash.	Off
Running	Snooze period	1 Hz flash*	$\overline{1 \text{ Hz flash}}$*

*colons flash alternately.

3.33 Minute Output — CK3100
This pin produces 3 pulses in each ten-minute period or 18 pulses per hour, and can be used for inputting to an external sleep counter, for clock radio type applications.

Wake Output — CK3100
This output turns "on" at the instance of alarm compare and stays on until the I.C. receives an alarm cancel signal. The wake output has been incorporated for appliance control, or clock radio applications. Output characteristics are shown in Figure 6.

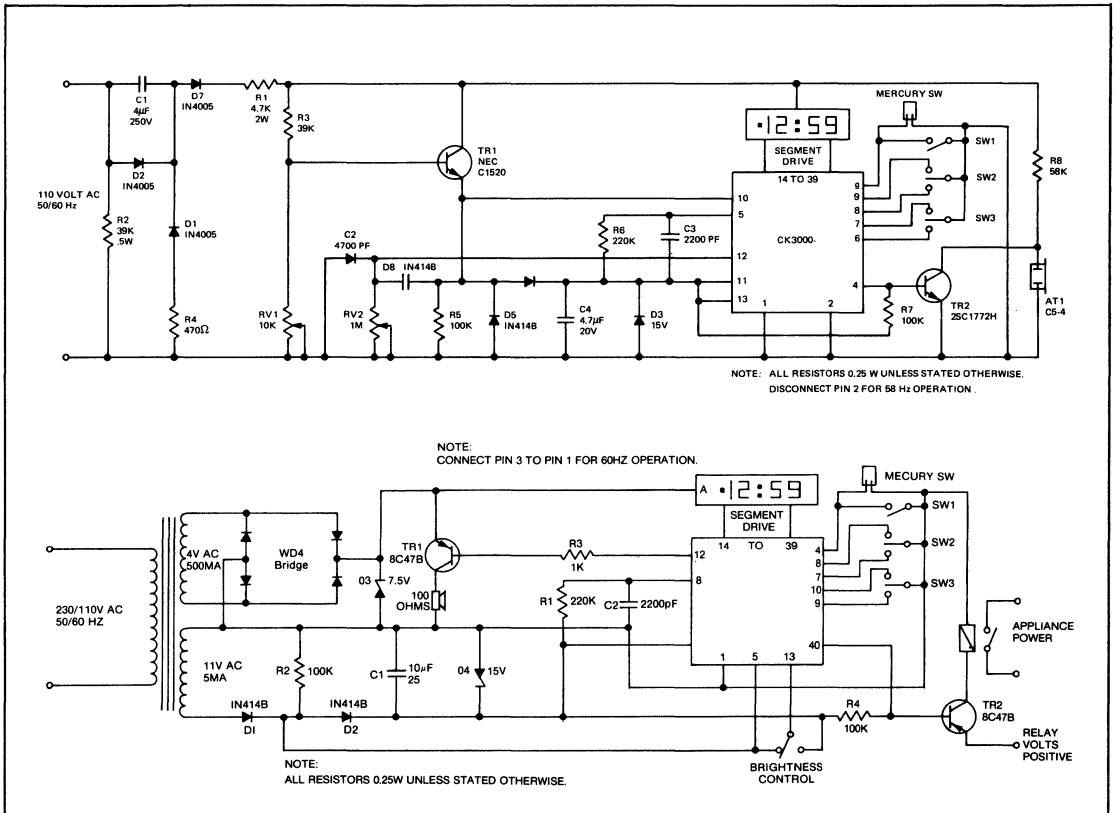


Fig.2 110 OR 230V LINE OPERATED CLOCK USING CK3000 DIRECT DRIVE PLASMA DISPLAY

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to VN . . . . . 0 to +25V
Voltage on Segment Output Pins . . . . . 0 to +45V (CK3000-2)
Storage Temperature Range . . . . . −65°C to +150°C
Power Dissipation at 70°C. 500mW
Operating Temperature. . . . . −25°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

$V_N = 0V$
$V_P = +7$ to $+18V$
$V_{SO} = +5$ to $+18V$ (CK3000)
Operating Temperature (T_A) = +25°C

CK3000

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Input Frequency	DC	50/60	2500	Hz	Max. figure for test only.
Clock Input					
Logic '0'	0	-	+1.0	V	
Logic '1'	0.7 V_P	-	V_P	V	
Oscillator Frequency (Fosc)	3.5	4	8	kHz	Set by external resistor and capacitor - See Fig.3
Control Inputs					
Logic '0'	0	-	+1.0	V	
Logic '1'	0.7 V_P	-	V_P	V	
Outputs					
Alarm Tone					
'0' Level	20	-	-	mA	at $V_{OUT} = 3V$; $V_P = 15V$
'1' Level	-	-	10	µA	at $V_{OUT} = 15V$
Display Drive					
OFF Level	-	-	500	nA	$V_{OUT} = V_P = V_{SO} = 15V$; $V_{OUT} = 30V$
ON Level	2	-	-	mA	See Figs.7 & 8; $V_{OUT} = 5V$
Current	-	-	2.5	mA	Not including outputs

CK3100

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Input Frequency	DC	50/60	2500	Hz	Max figure for test only
Clock Input					
Logic '0'	0	-	+1.0	V	
Logic '1'	0.7 V_P	-	V_P	V	
Oscillator Frequency (Fosc)	2.5	4	6	KHz	Set by external capacitor and resistor - See Fig.3
Control Inputs					
Logic '0'	0	-	+1.0	V	
Logic '1'	0.7 V_P	-	V_P	V	
Outputs					
Alarm Tone					
'0' Level	20	-	-	mA	$V_{OUT} = 3V$; $V_P = 15V$
'1' Level	0.7 V_P	-	-	V	Internal pull-up to V_P (approx. 5KΩ)
Wake Output					
'0' Level	20	-	-	mA	$V_{OUT} = 3V$; $V_P = 15V$
'1' Level	-	-	10	µA	$V_{OUT} = V_P$
Display Drive					
'0' Level	20	-	-	mA	$V_{OUT} = 2.2V$; $V_P = 15V$
'1' Level	-	-	10	µA	$V_{OUT} = V_P$
3-1/3 Min. Output					
'0' Level	5	-	-	mA	$V_{OUT} = 3V$; $V_P = 15V$
'1' Level	0.7Vp	-	-	V	Internal pull-up (approx. 5KΩ)
Current	-	-	5	mA	

**Typical values are at +25°C and nominal voltages.

NOTES:
1. Pins 2,6,7,8 and 9 have an internal pull-up resistor to V_P, value approximately 200KΩ. (CK3000)
2. Pins 3,4,6,7,8,9 and 10 have an internal pull-up resistor to V_P, value approximately 200KΩ. (CK3100)
3. Under no circumstances must any pin be biased temporary or permanently negative with respect to V_N or device operation will be affected.
4. No output pin during operation must exceed V_P transiently or operation will be affected.

TYPICAL CHARACTERISTIC CURVES

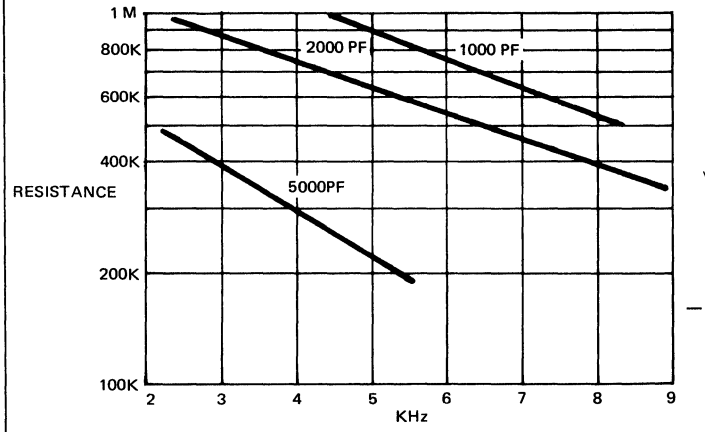


Fig.3 OSCILLATOR FREQUENCY VS. RESISTANCE/CAPACITANCE V_P = 15V

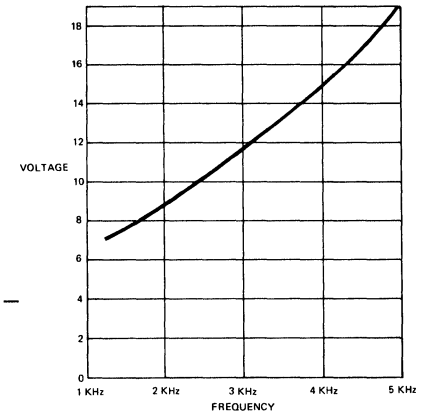


Fig.4 OSCILLATOR FREQUENCY VS. SUPPLY VOLTAGE (V_P) R-680K C = 2000 pf

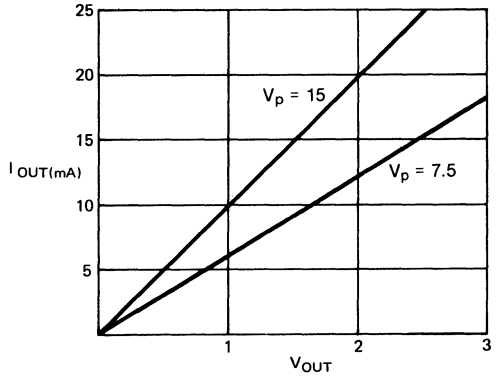


Fig.5 TYPICAL LED OUTPUT DRIVER

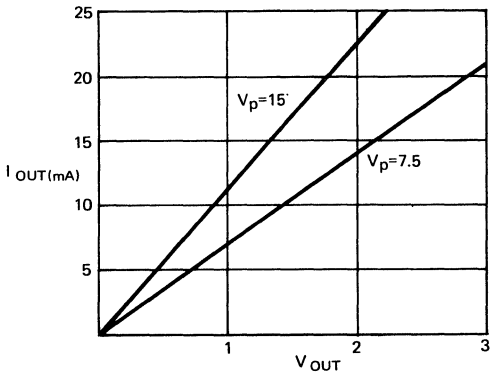


Fig.6 TYPICAL WAKE OUTPUT CURRENT CHARACTERISTIC FOR CK3000, CK3100 ALARM OUTPUT AND WAKE OUT FOR CK3100

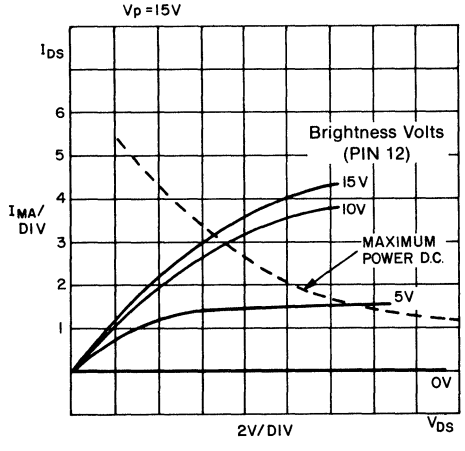


Fig.7

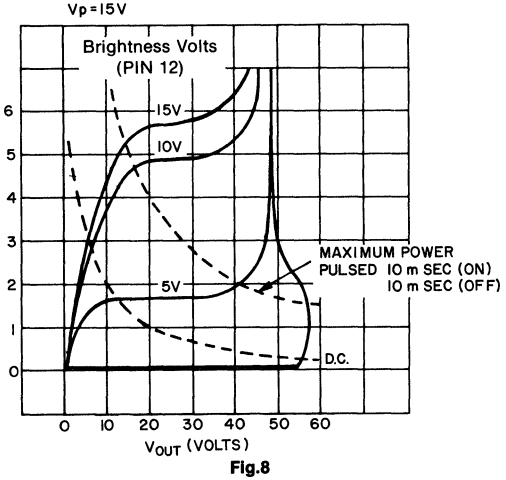


Fig.8

TYPICAL PLASMA OUTPUT DEVICE "ON" CHARACTERISTICS

4 Digit Alarm Clock Circuit

FEATURES

- 12 and/or 24 hour clock, 24 hour alarm setting
- Leading zero suppression in 24 hour mode
- PM indication in 12 hour mode
- 50 or 60 Hz operation
- Snooze (sleep-over) alarm
- Direct display driving (two digit duplexing)
  CK3200 - Plasma
  CK3400 - LED
- No display interface components
- Seconds flashing colons
- Alarm, set, and snooze indication
- Line power interrupt indication
- Low current consumption

DESCRIPTION

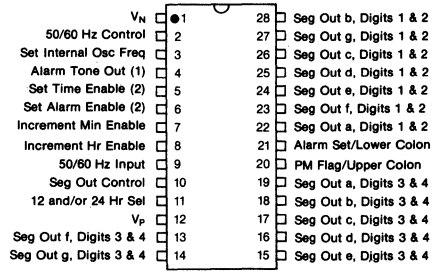
The CK3200 and CK3400 are N-Channel MOS integrated circuits, containing all the logic necessary to produce low cost 4 digit alarm clocks operating from 50 or 60 Hz line frequencies. The output stages of these circuits have been designed specifically to directly drive the cathodes of Plasma displays (CK3200) or the cathodes of large digit common anode L.E.D.'s (CK3400) with no interface electronic components whatsoever (Duplex mode).

These integrated circuits also contain all the logic needed for contact noise elimination and line frequency noise rejection reducing further support components. In order to overcome the extreme difficulties in eliminating radio frequency interference (common problem of multiplexed display clocks) and to keep the device in a low cost package a novel display driving technique is used - that of half line cycle anode duplexing. The duplex technique depends on the use of the two half sine-waves produced by two diodes placed across an a.c. supply where the common connection becomes the system reference.

PIN CONFIGURATION

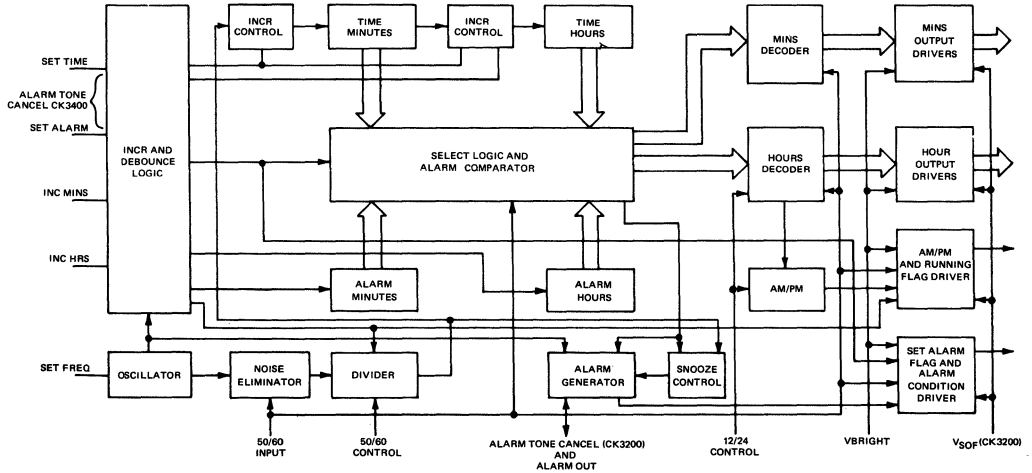
28 LEAD DUAL IN LINE

Top View



NOTES:
1. For CK3200, this pin is also alarm tone cancel.
2. For CK3400, either of these pins can be used as alarm cancel.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The block diagram shows diagramatically the various logical function blocks that make up the CK3200 and CK3400 integrated circuits. The various units have the following functions.

Oscillator

The oscillator provides two basic functions in this integrated circuit.

1. Provides a suitable frequency in the audio range for modulating an external transducer at and during the alarm time. (Nominally 1 KHz)
2. Provides a strobe frequency for strobing the 50 or 60 Hz line frequency into a 'D' type flip flop to statistically eliminate the noise. (Nominally 250 Hz)

Debounce Logic

The logic here is used to eliminate contact noise closure on any input line and this is achieved using one second digital one shots in combination with 250 Hz strobe pulses. e.g. With the set-time or alarm enable inputs at logic zero the increment inputs are looking for one contact closure in each one second period. Any further closures are ignored. However if any increment pin is at logic zero and the set time switch is open and closed multiple counting will result. This logic also directs increment signals to the appropriate counter.

Divider

The divider counts down the line frequency counts to one per second depending on the 50/60 Hz control.

Snooze Control

This logic stores the information that an alarm compare has been reached, and initiates a 5 minute counter, which then runs continuously until such time that on an exact multiple of five minutes if the alarm/tone cancel switch is at zero, it will then stop and reset the alarm compare store. During the 5 minutes the alarm tone is made active for one minute in each five producing a 1 Hz modulated 1 KHz tone. If when the alarm tone is active the alarm tone cancel is taken to logical zero the tone will cease until the next five minute period.

Duplex Display Driving

To use either CK3200 or CK3400 the display is connected in the following manner.

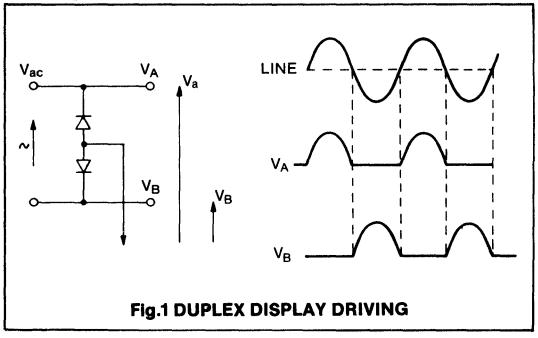


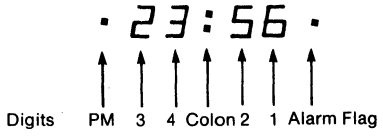
Fig.1 DUPLEX DISPLAY DRIVING

Segment	a	Digit 1 connected to segment	a	Digit 2
	b		b	
	c		c	
	d		d	
	e		e	
	f		f	
	g		g	
Segment	a	Digit 3 connected to segment	a	Digit 4
	b		b	
	c		c	
	d		d	
	e		e	
	f		f	
	g		g	

PM flag (indicator) segment connected to upper colon segment
Alarm setting flag segment connected to lower colon segment
Anode digit 1 connected to Anode digit 3
Anode PM indicator connected to Anode digit 4
Anode digit 2 connected to Anode digit 4
Upper colon anode connected to anode digit 2
Lower colon anode connected to anode digit 3
Alarm setting flag connected to anode digit 1

The anode can then be selected by the application of alternate half-cycle sine waves.

NOTE:
The phase of the incoming 50/60 Hz count to IC will then automatically deliver the correct segment data to display.



Anode phasing 50/60 Hz High = Digits 1 and 3 selected
Low = Digits 2 and 4 selected

DEVICE UTILIZATION

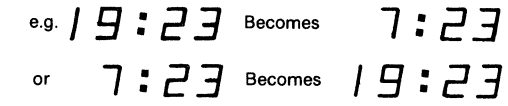
50/60 Hz Control

For 60 Hz operation Connect to V_P or leave open circuit
For 50 Hz operation Connect to V_N

12 And/Or 24 Hour Select

The IC has the ability to display the correct time in 12 or 24 hour mode under the control of the 12/24 select pin. Changing this pin from Logic '0' to '1' or '1' to '0' will immediately display the corrected time.

High i.e. '1' = 24 hour mode
Low '0' = 12 hour mode



No leading zero is shown in 24 hour mode.

For economy a single segment is employed which is illuminated in 12 hour time, during PM period.

Alarm Cancel & Alarm Tone Output - CK3200

In CK3200 (Plasma) the alarm tone output, alarm and tone cancel input uses the same pin for all three functions.

1. Alarm pin held to less than 1 volt (inputting a logic '0') alarm is not requested.
2. Alarm pin returned to positive supply through an appropriate resistance such that output is above 3 volts. (IC pulling approximately 1 mA) Alarm is requested.
3. At the alarm time this pin alternates between an open circuit condition and pulling 1 mA at the alarm tone rate.

[See Fig. 2 for typical external connections]

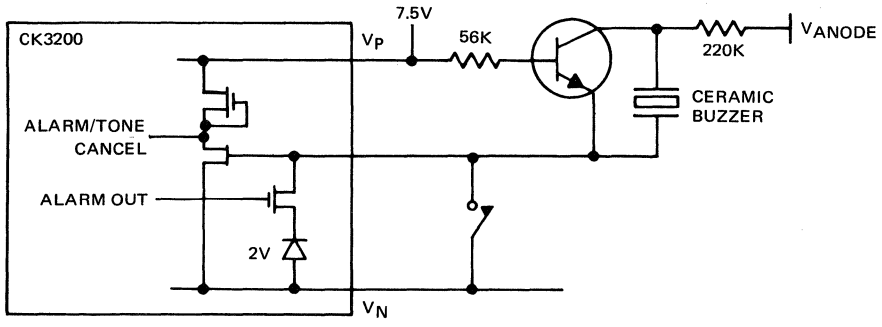


Fig.2 TYPICAL BUZZER CIRCUIT - CK3200

For normal operation the alarm cancel input is allowed to establish its own voltage (see Fig. 2). Under this condition any coincidence between the time and alarm store will cause the alarm tone to be output on this pin. This tone will remain present for one minute unless cancelled by momentarily connecting this pin to a logical '0' (less than one volt). This tone will re-occur five minutes (and subsequent multiples of 5 minutes) after the original alarm time for a duration of one minute unless cancelled by momentary connection of pin to logic '0' thus providing the snooze facility.

To completely cancel the alarm - snooze sequence, the coincidence of this alarm pin being at a logical '0' and the start of the next alarm tone period is required. Immediately after this occurence the alarm cancel input may be returned to the normal position and the alarm will be re-enabled for the following day.

Alternately if either the set time or set alarm inputs are connected momentarily to a logical '0' after the first minute of alarm, the alarm logic will be triggered for the next day.

Alarm Cancel & Alarm Tone Output - CK3400

In CK3400 the alarm output is on a dedicated pin (see Fig.3) Alarm cancel can be achieved by either taking set time or set alarm to a logic '0' during the post alarm time.

Tone cancel is achieved by a momentary connection to a logic '0' of both set time and set alarm simultaneously.

For normal operation the set time and set alarm input are left open circuit. Under this condition any coincidence between the time and alarm store will cause the alarm tone to output on the alarm tone pin. This tone will remain present for one minute unless cancelled by momentarily connecting both set time and set alarm simultaneously to a logical '0'. This tone will re-occur five minutes (and subsequent multiples of 5 minutes) after the original alarm time for a duration of one minute unless cancelled by momentary connection of set time alarm to a logic '0' thus providing a snooze facility.

To completely cancel the alarm sequence, either set time or set alarm pin is taken to a logical '0'. Immediately after this occurence the alarm will be re-enabled for the following day.

The alarm tone is a nominal 1 KHz square wave chopped by a 1 Hz square wave.

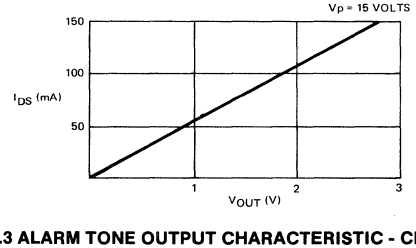


Fig.3 ALARM TONE OUTPUT CHARACTERISTIC - CK3400

Frequency Set

An external resistor to V_p and external capacitor to V_N are used to control the frequency of the oscillator. These values should be selected to ensure approximately 4KHz oscillation.

The following graphs give a guide to component values for different V_p values.

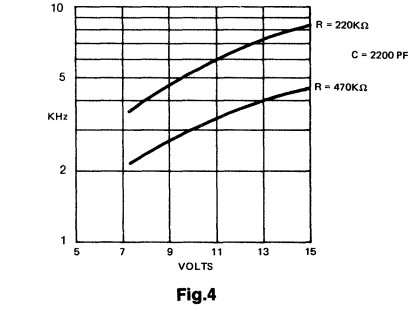


Fig.4

With the oscillator set to 4KHz, the alarm tone output will be 1KHz and the internal antibounce logic is strobed at 250 Hz.

Setting Up Procedure (Pins 6 Thru 9)

In the normal clock running condition, pins (6 thru 9) should be open circuit or at logical '1'.

To enter set mode either set time or set alarm should be pulled to logical '0'. Under this condition increment minutes and increment hours inputs are enabled and when either is pulled to a logical '0' then the corresponding hours or minutes will increment at a 1 Hz rate. All minutes to hours carries are suppressed while time is being set.

When set alarm is at a logical '0' the contents of the alarm store are displayed.

When set time/increment minutes occurs, the clock is stopped and remains stopped with the seconds reset until set time is open circuited or returned to a logical 1. This enables the clock to be easily synchronized to an independent time source. No other setting conditions interrupt the seconds.

50/60 Hz Input

This input accepts a line frequency signal at either 50 or 60 Hz and is subsequently used as the basic count time base.

Segments Output Control (Brightness) - CK3200

All output stages consist of a three device cascode configuration of which one device controls the output voltage current characteristics (see Fig.5). From the characteristics it will be seen that a wide range of operating conditions are possible, allowing operation in either the resistive region (V proportional to I) or the constant current region (I independent of V).

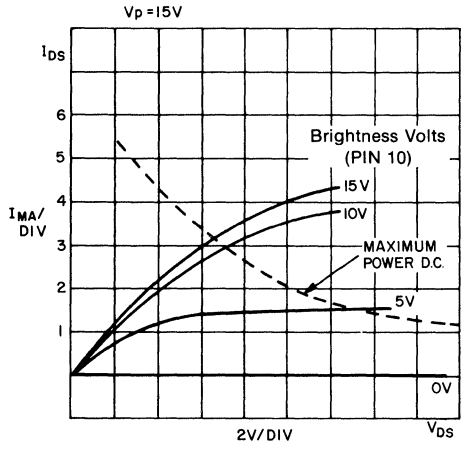


Fig.5 TYPICAL LED OUTPUT DRIVER

The output stages and control brightness were designed to be used with a half line cycle anode voltage and a corresponding half cycle control of brightness to ensure the display is

a. Off during segment data changes
b. To allow current to turn off and on in display gradually.

This will result in almost a total absence of R.F.I.

Segments Output Control (Blanking) - CK3400

Due to the high current handling capabilities of the output stages of this I.C., it is not possible to control the output V.I. characteristic by using a second series device. To regulate the display to the required brightness several options are possible externally and the following internally. The segments output control can turn off the display at any time by taking this input to a logical '0'. It is possible therefore to use half or full wave rectified signal on the display anode and prematurely shut the display down in each line cycle to control the conduction angle hence average light output, using this control pin in phase relationship to the anode wave form.

AM/PM Indicator

This output is an additional segment driver which can be used to give an AM/PM indicator. (Voltage current characteristic as other segments)

Cathode (Segment) Output Drivers - CK3200

All these pins drive the cathodes of the display without any additional interface components. These outputs are designed to withstand higher voltage signals than the other outputs. The output characteristic of the segment drivers can be controlled by pin 10. (See Fig.5)

Cathode Segment Drivers - CK3400

The output drivers of the CK3400 have sufficient current handling capabilities to drive even the most inefficient of todays available L.E.D.'s. The output characteristics of the segments are shown in Fig.5.

NOTE:

It is recommended that the package power dissipation is kept to below 500mW, therefore, with a possible 16 simultaneous outputs being on together, then each segment should be operated with an average power level of 31mW or on average current of 25mA. The peak current for the maximum number of segments condition (i.e. 16) should not exceed 60mA per segment or the device will suffer permanent damage.

It is also important that the display V-I load characteristic does not interrupt the avalanche region of the output device characteristic or off segment glow will be observed or in the limit device malfunction. or damage can occur.

Colon Utilization

Two colons (Pins 24 and 25) show alarm/clock condition.

Clock	Alarm	Colon A	Colon B
Stopped/Setting	Don't care	OFF	OFF
Running	Set	1 Hz Flash.	1 Hz Flash.
Running	Not set	1 Hz Flash.	1 Hz Flash.
Running	Snooze period	1 Hz Flash.	1 Hz Flash.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_N . . . . . −0.3 to +30 volts
Voltage on segment output pins . . . . . −0.3V to +45V
Storage temperature range. . . . . −65°C to +150°C
Power dissipation at 70°C . . . . . 500 milliwatts
Operating temperature . . . . . −25°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_N = OV
V_p = +10 to +18V
Operating Temperature (T_A) = +25°C

CK3200

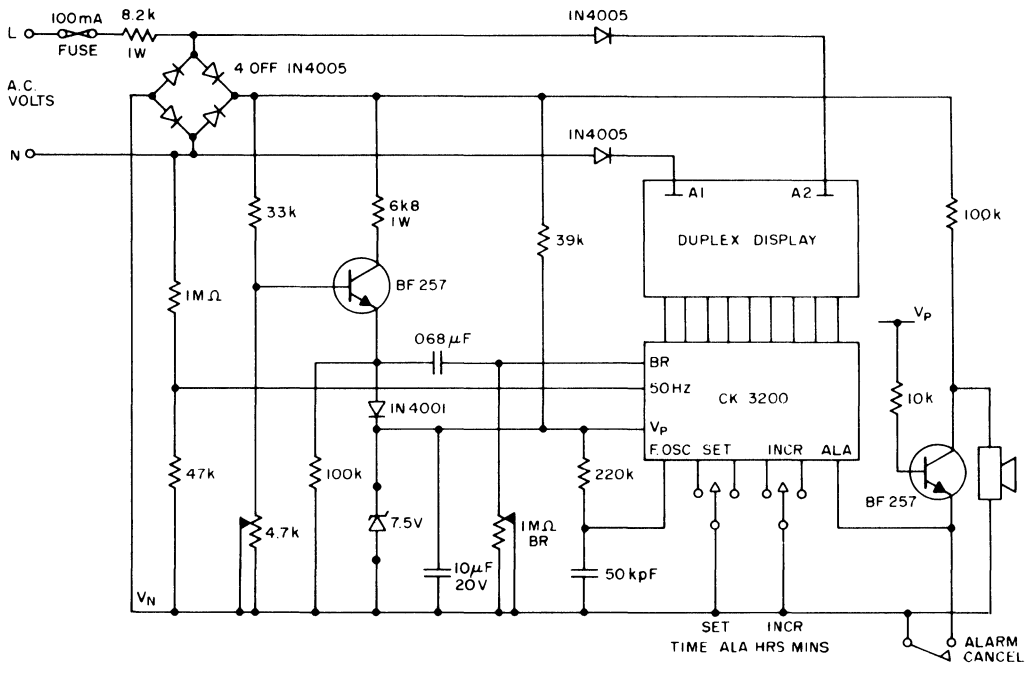
Characteristic	Min	Typ**	Max	Units	Conditions
Clock Input					
Frequency	DC	50/60	50,000	Hz	Max figure for test only
Logic '0'	0	—	0.8	V	
Logic '1'	$0.7V_p$	—	V_p	V	
Oscillator Frequency (Fosc)	3	4	6	kHz	Set by external resistor and capacitor at V_p = 15V
Control Inputs					
Logic '0'	0	—	0.8	V	
Logic '1'	$0.7V_p$	—	V_p	V	
Outputs					
Alarm Tone					
Cancelled	−0.3	—	0.3	V	Typ I sink = 3ma at > 2.5V
Tone	3	—	V_p	V	
Display Drive					
OFF Level	—	—	2	μA	V_p = 15 V, V_{OUT}=45 Volts
ON Level	—	—	—	—	See Figs.4a-b-c
Current	0.4	—	3.0	mA	Not including outputs

CK3400

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Input					
Frequency	DC	50/60	50,000	Hz	Max figure for test only
Logic '0'	0	—	0.8	V	
Logic '1'	$0.7V_p$	—	V_p	V	
Oscillator Frequency (Fosc)	3	4	6	kHz	Set by external resistor and capacitor at V_p15V
Control Inputs					
Logic '0'	0	—	0.8	V	
Logic '1'	$0.7V_p$	—	V_p	V	
Outputs					
Alarm Tone			40	μA	V_{OUT} = 0.3 Volts, Typ I sink = 3ma at > 2.5V
Display Drive					
OFF Level	—	—	10	μA	V_p = 15V, V_{OUT} = V_p
ON Level	—	—	20	mA	See Figs. 4a-b-c, V_{OUT} = 3 Volts
Current	0.4	—	3.0	mA	Not including outputs

**Typical values are at +25°C and nominal voltages.

Fig.6 TYPICAL APPLICATION



Digital Clock Radio Circuit

FEATURES

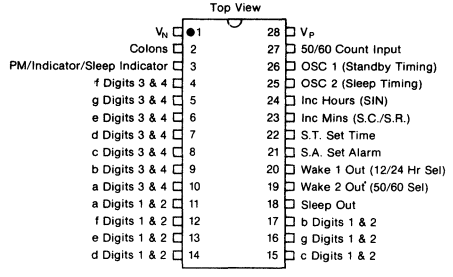
- 4 Digits plus colons
- LED direct duplex drive
- No display-IC interface components
- No radio frequency interference problems
- No external contact noise elimination circuits required
- No external line frequency noise rejection circuits required
- 12 or 24 hour display
- Leading zero suppression in 24 hour mode
- PM indication in 12 hour mode
- Alarm-snooze indicator
- 50Hz or 60Hz operation
- On-chip oscillator for standby operation with battery during line Failure
- Line power interrupt indication
- Sleep operation indicator
- Low power dissipation (under 30 mW)

CLOCK RADIO FEATURES

- Simple support electronics
- Analog sleep setting (user controlled 5 to 120 mins with 1 minute resolution). No necessity for daily adjustment
- Totally independent sleep and wake timing
- Independent volume of music during sleep and wake
- Radio sound muting during normal radio listening
- Wake to music or alarm tone
- Self-cancelling alarm after 80 minutes of wake
- 5 minute repeating snooze with radio and/or alarm
- Sleep override or sleep repeat
- Wake to alarm tone with quiet radio override (every 5 minutes) during snooze time (repeatable)
- Simple setting of time, alarm, and sleep
- Hold and synchronize capability for time setting
- Independent hours, minutes setting (carry propogation suppressed)
- 5 minute pre-alarm applicance switching
- Automatic tape recorder control (record your favorite program automatically 0-120 minutes—starting from the exact second)

PIN CONFIGURATION

28 LEAD DUAL IN LINE



DESCRIPTION

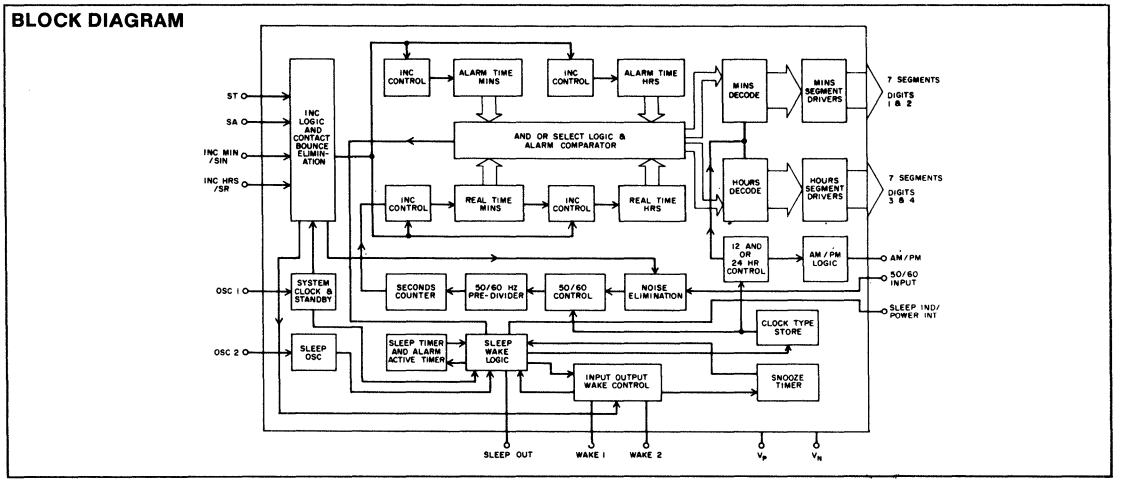
The CK3300 N-Channel MOS I.C. contains all the necessary logic, contact noise elimination circuits, control switching, segment drivers and timing circuits to implement simple-to-use, low cost, multi-featured clock radios.

Due to the extreme difficulties in eliminating R.F.I. in radios when used in conjunction with digital electronics a great deal of care has gone into the design of the L.S.I. to ensure that little or no R.F.I. problems are met by the clock radio designer. The largest R.F.I. problem in Display Driving has been solved using a novel technique—that of half-line cycle anode duplexing using the half-sine waves produced by two diodes, and ensuring that all segment data changes occur at the zero crossings of the line cycle. This technique allows brightness control to be achieved simply by resistively dividing down the line voltage with a potentiometer, or a simple two level scheme using a transformer tap.

Segment driving of the two groups is directly from the I.C. through 50 ohm switches which allow the high current peaks required of LEDs, up to one inch in size, while keeping the I.C. Power dissipation, for reliability, down to the 200 to 250 mW level.

The I.C. also contains many unique features which enable the equipment designer to put into the clock radio his company's own product image.

BLOCK DIAGRAM



PIN FUNCTIONS

V_N - (Pin 1)
Is the most negative power supply to the chip (0 volts).

Segment Drivers (Pins 2-17)
These outputs are 50 Ω switches which drive the segments of common anode LED's directly. Their use and operation is as follows:

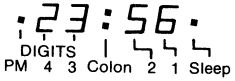
To use the CK3300 with LEDs, the LEDs must be of the COMMON ANODE TYPE, and connected in the following manner.

segment a digit 1 connected to segment a digit 2
segment b digit 1 connected to segment b digit 2
segment c digit 1 connected to segment c digit 2
segment d digit 1 connected to segment d digit 2
segment e digit 1 connected to segment e digit 2
segment f digit 1 connected to segment f digit 2
segment g digit 1 connected to segment g digit 2

segment a digit 3 connected to segment a digit 4
segment b digit 3 connected to segment b digit 4
segment c digit 3 connected to segment c digit 4
segment d digit 3 connected to segment d digit 4
segment e digit 3 connected to segment e digit 4
segment f digit 3 connected to segment f digit 4
segment g digit 3 connected to segment g digit 4

Colon 1 segment connected to colon 2 segment
PM indicator segment connected to sleep/power down indicator segment
Anode digit 1 to anode digit 3
Anode PM indicator to anode digit 4
Anode sleep indicator to anode digit 1
Anode colon upper to anode digit 3
Anode digit 2 to anode digit 4
Anode colon lower to anode digit 2

The anodes can then be selected by the application of alternate half-cycle sine waves derived from a transformer from the line. The phase of the incoming 50/60Hz count to IC will then automatically deliver the correct segment data to the display.



Anode phasing: 50/60 high = digit (1 & 3) selected
low = digit (2 & 4) selected

Sleep Output (Pin 18)
This output turns on while the sleep counter is running and is indicated as active by an indicator in the display (Pin 3). This output turns on immediately following a sleep initiate and is cancelled either by sleep time being complete, a sleep cancel, an alarm comparison taking place, or an end of snooze period. This pin is also used as an input during circuit test to speed up testing.

Wake 2 Output/50-60 Hz Mode Select (Pin 19)
This output turns on at alarm compare time and stays on unless either an alarm cancel or a snooze repeat is activated.

If snooze repeat is activated this pin will go off until the next 5 minute period elapses when it will again turn on.

The snooze can be repeated indefinitely.

If the alarm is not cancelled this output will turn off 80 mins after the last snooze repeat re-triggering alarm for the next 24 hour period.

This pin is also the 50/60 Hz Select input during the time at which Set Time and Set Alarm are at a logic '1' (last data on this input when either Set Time or Set Alarm changes state is stored in an internal latch).

Wake 1 Output/12 Or 24 Hour Select (Pin 20)
This output turns on at alarm compare time and stays on uninterrupted until either:

a. An alarm cancel
b. 80 continuous minutes from alarm time
c. 80 continuous minutes from last snooze repeat

During the time that Set Time and Set Alarm are at a logic '1' together, this pin is the 12/24 hour select input.

The last data on this pin before a data change on Set Time or Set Alarm is stored internally in a latch, and defines 12 or 24 hour operation.

Set Alarm (Pin 21)
This pin, held at zero while Set Time is at a logic '1', enables the Increment Minutes and Increment Hours inputs to the alarm counter, such that each change of state (1—0) of the increment inputs will advance the appropriate counter by one unit.

Set Time (Pin 22)
Is identical in operation to the Set Alarm pin, but in this instance allows the counts to be entered into the time counter.

Taking both Set Time and Set Alarm to a logic '0' allows the Wake outputs to become active when the time reaches the alarm time. Returning either Set Time or Set Alarm to a logic '1' will cancel the alarm.

Increment Mins/Sleep Cancel/Snooze Repeat (Pin 23)
If Set Time or Set Alarm is at zero, this input provides one unit of increment for each logic transition from one to zero. (This input is de-bounced against switch noise). If both Set Time and Set Alarm are at a logic '1' or logic '0' and the sleep timer is running, a logic zero on this input will cancel sleep.

If both Set Time and Set Alarm are at a zero and the Wake outputs are active (i.e., post alarm time), then Wake 2 will be cancelled for a period of up to 5 mins when Pin 23 is taken to logic '0'. If this input is at zero when the alarm comparison takes place, then Wake 2 will stay off until 5 minutes have passed.

Increment Hours/Sleep Initiate (Pin 24)
If either Set Time or Set Alarm is at logic '0', this input provides one unit of increment to the required counter for each logic transition from 1 to 0. (This input is de-bounced against switch noise). If both Set Alarm and Set Time are at logic '1' or logic '0', this input will cause Sleep output to become active for the time resulting from current sleep oscillator frequency.

OSC 2 (Pin 25)
This pin produces a triangular wave oscillation depending on the value of resistance and capacitance. This oscillator is used to produce the sleep period by being gated internally with 160th of Osc 1 frequency (i.e. 50/60Hz).

Additionally connected to this pin is a low level detect circuit used with oscillator 1 for re-setting all internal logic to 12:00 in 12 hour mode and 0:00 in 24 hour mode. This low level detect is also used to detect that standby operation is required.

OSC 1 (Pin 26)
This pin produces a triangular wave oscillation depending on the external value of resistance and capacitance. The signal is used during normal operation to provide internally to the I.C. -
a. the internal timing for a series of one-shot gates
b. After division, the frequency to de-bounce other external pins via D-type latches. This frequency is further divided down to 50/60Hz and is used as the source frequency during standby operation.
Connected internally to this pin is a low level voltage detector which is used in conjunction with a low level voltage detector on Osc. 2 (pin 25) to reset all the internal logic to 12:00 in 12 hour mode and 0:00 in 24 hour mode. This low level detect is also used for test purposes.

50/60 Hz In (Pin 27)
This input is the normal source of timing. This input drives both the internal count and the alternate half line selection of the segment outputs.
For equal brightness in the display this input must have a 1:1 mark space ratio (±20%).
There is no necessity for eliminating line noise externally when providing this input signal as an internal arrangement eliminates undesired counts.

V_P (Pin 28)
Is the most positive power supply to the chip (typically 10 volts)

FUNCTIONAL OPERATION

Pins 19, 20, 23 and 24 are dual function pins which operate as inputs or outputs dependent on the state of the Set Time and Set Alarm inputs:

S.T.	S.A.	INC MIN	INC HR	SC/ SR	SIN	Wake 1	Wake 2	50/ 60	12/ 24
1	1	-	-	*	*	-	-	*	*
1	0	*	*	-	-	-	-	-	-
0	1	*	*	-	-	-	-	-	-
0	0	-	-	*	*	*	*	-	-

*Operable - Not Operable

Set time (S.T.)	Pin 22
Set alarm (S.A.)	Pin 21
Increment minutes (inc min)	Pin 23
Increment hours (inc hrs)	Pin 24
Sleep cancel (S.C.)	Pin 23
Snooze repeat (S.R.)	Pin 23
Sleep initiate (SIN)	Pin 24
Wake 1	Pin 20
Wake 2	Pin 19
50/60Hz Select	Pin 19
12/24Hr. Select	Pin 20

Using Wake 1 Or 2—Input/Output Functions

When the Set Time (S.T.) and Set Alarm (S.A.) inputs are at logic one, the IC outputs Wake 1 and Wake 2 become inputs to two bistable gates which store the logic conditions on those pins: 50/60Hz Select on the Wake 2 pin and 12/24Hr. Select on the Wake 1 pin.

50/60Hz Select

Set Time or Set Alarm must be at zero before data on Wake 2 changes, or clock can change its 50/60 pre-divide mode. To avoid this, the following circuit is recommended:

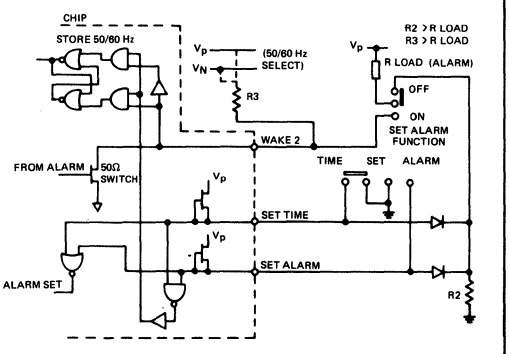


Fig.1 SUGGESTED USE OF WAKE OUTPUTS TO ENSURE PROPER OPERATION OF INPUT/OUTPUT FUNCTION

With the Set switch in the center position the set inputs are pulled up to a logic '1' by the IC, provided the Alarm switch is in the off position. The load (R load) will pull the junction of the two diodes and R2 to a logic '1'.

The output pin Wake 2 will either be pulled up or down depending on the connection of R3.

Changing of Set switch will pull down the appropriate input and not affect other external circuit conditions.

Change of position of alarm ON-OFF switch will allow R2 to pull down both Set inputs to zero before Wake 2 output is connected to load. This ensures that the internal IC latch is disconnected from wake line before data on wake line can influence stored data in latch.

12/24 Hr. Select

For the "Wake 1 output 12-24 hour select", changing the logic polarity will immediately change the displayed time from 12 hour mode to 24 hour mode or vice versa.

e.g. 21 : 56 becomes •9 : 56
or •9 : 56 becomes 21 : 56

No leading zero is shown in 24 hour mode:

12 : 32 in 12 hour time becomes 0 : 32 in 24 hour time

(Note: 12 to 24 hour displayed time change can only be achieved when the alarm is not requested and not in set mode)

For economy of LEDs a single dot is employed which is illuminated during the PM period in 12 hour time.

Time Setting

Four input pins (S.T., S.A., Inc Hr., Inc Mins.) are provided to enable the following four functions to be provided:

a. Setting the time
b. Setting the alarm
c. Stopping the clock
d. Starting the clock

For synchronizing purposes

S.T. = 0

Allows each depression of Inc Hrs to advance hrs by one count. Clock will stop on the first inc mins and will remain stopped until ST = 1, thus allowing synchronization. The device assumes that the hours may need to be changed without affecting mins, but assumes clock is incorrect if minutes are changed, thus stopping clock and re-setting internal seconds counter to zero.

S.A. = 0

Selects alarm time and, for each depression of Inc Hours, hours are advanced one and, for each depression of Inc Mins, minutes are advanced one.

NOTE:
No carries from minutes to hours occur during setting of time or alarm

Radio Control Inputs

The inputs S.T., S.A., Inc Min, Inc Hr, serve as radio control inputs under the following conditions.

S.T. And S.A.

At zero together - alarm is requested. S.T. and S.A. at logic one together - alarm not requested, but if taken to logic one during post alarm, alarm is cancelled.

S.T. and S.A. different will also cancel alarm if alarm is active.

S.T.	S.A.	Pre-Alarm	Post-alarm
1	1	Not required	Cancel
1	0	Not required	Cancel
0	1	Not required	Cancel
0	0	Requested	Alarm maintained for 80 mins

S.T., S.A. = 1

If S.T. and S.A. are at a logic 1 together during pre-alarm time, the following functions can be obtained using Inc Min - Inc Hrs inputs. Inc Hrs input going to logic zero for at least 20m secs will result in sleep output going to zero for the period of time set by sleep potentiometer.

At any time Inc Mins input (SC/SR) going to zero for at least 20m secs will cancel sleep timer if sleep output is active.

To reduce the number of knobs, switches, wiring etc., in the clock radio the following alternative feature is provided. If (S.C./S.R.) is wired to (SIN) a dual action is achieved, 1st depression of switch activates sleep, 2nd cancel sleep, 3rd re-activates etc. This allows features (a) if user decides he wishes radio off after he has been in bed for a few minutes, he pushes button, or (b) radio goes off automatically because sleep period has finished, but user is not asleep and would like radio to continue, so he presses button again.

S.T., S.A. = 0

In pre-alarm period the function performed when S.T., S.A. = 1 is identical. (When the alarm sounds at the requested alarm time the input (S.C./S.R.) (Inc Mins) becomes the 5 min snooze repeat input.)

At alarm, the effect of (S.C./S.R.) becoming zero for at least 20m secs is to turn Wake 2 output off until next 5 min interval, if again depressed, Wake 2 will turn off for a further 5 mins—this sequence will go indefinitely until S.T., or S.A. or both are returned to logic '1', cancelling alarm. If inputs to the device are left unchanged for 80 mins then alarm will re-set for 24 hours.

Again to improve the radio features and simplify radio operation the tied function of (S.C./S.R.) and (SIN) on one button performs the following three functions:

Initiate sleep (SIN)
Cancel sleep (S.C.)
Snooze repeat (S.R.)

Delaying Alarm by 5 Minutes

If, when Wake 1 output is capactively coupled to (S.C./S.R.) input then at alarm time Wake 1 will turn on and stay on but Wake 2 will immediately become cancelled, hence no alarm will be heard from radio until 5 minutes later; this allows an electrical appliance to be turned on 5 minutes prior to alarm sounding.

Use of Sleep Timer for Tape Recorder Control

If sleep input (SIN) in directly coupled to Wake 1 output, then a tape recorder or any electrical equipment can be turned on at alarm time using sleep output for a period of time set on sleep potentiometer.

Radio Control Outputs

There are three radio control outputs:

a. Wake 1
b. Wake 2
c. Sleep output

Function

1. Wake 1—goes at zero; i.e. is on at alarm time for a period of 80 mins or until an alarm cancel.

2. Wake 2 goes to zero at alarm time, and stays at zero until a snooze repeat is activated then it will stay off until next 5 minute point then return to zero, for a period of 80 mins unless snooze repeat is re-activated. Snooze repeat can be used indefinitely, until either a continuous 80 mins occurs or alarm is cancelled.

Note: The 5 minute period is any 5 min interval from alarm time and not 5 min from each snooze repeat.

3. Sleep output goes low after a sleep initiate for the period of time set by sleep potentiometer. (Will be overidden by Wake if sooner.)

Colon Utilization

	COLON CONDITIONS	
FUNCTION	BOTTOM	TOP
Set time	on	off
Set alarm	off	on
Stopped (Sync)	off	off
Run (alarm not requested)	1Hz	off
Run (alarm requested)	1Kz	1Hz
Snooze period	1Hz	1Hz

Sleep dot is on for sleep timer running, flashing for post line interrupt (removed from flashing by movement of S.T. or S.A. to '0')

Stand-By Operation

If a circuit is employed to change the IC power source to battery during line failure, e.g. two diodes, then if the external timing components of oscillator 1 are set to give 8KHz (nominally R = 120K Ω = 2200pF), then the IC will maintain operation to an accuracy of one part in 120, i.e., 30 secs/hr, during the failure. On return to main power the sleep indicator will flash at 1HZ to notify user that indicated time could be in error.

The standby condition is detected by the failure of oscillator 2 to oscillate, therefore oscillator 2 is connected to the line-derived power source, not the battery.

It is assumed OSC 2 input has gone to zero volts.

To remove flash condition take S.T. or S.A. momentarily to zero.

Analog Sleep Control

A second oscillator is provided on IC whose frequency can be controlled by an RC network. This osillator is identical to oscillator one (Standby oscillator) and occupies the same silicon real estate location ensuring that process variations, temperature variations and voltage variations have as nearly as possible identical effects on frequency stability. Oscillator 1, which is set to 8KHz is divided down to 50HZ (20.0 msecs) and is used as a gating time for oscillator 2 (Sleep Timer Source). The number of gated counts is loaded in the sleep timer (capacity 160 counts) and subsequently counted up at one per minute until 160 is reached.

The range of sleep time is controlled by varying OSC 2 resistance. At 4:1 change in resistance will give variation of 160 to 40 gated pulses, this giving a sleep time of 0 to 120 minutes.

NOTE:
Minimum sleep time to ensure correct snooze operation should be a minimum of 5 minutes.

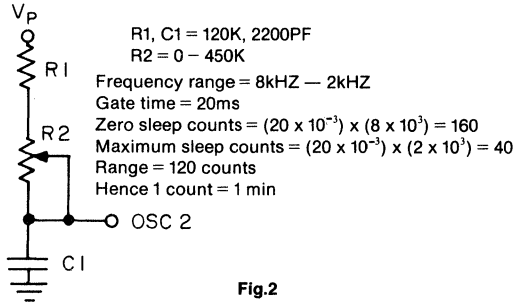


Fig.2

To initiate the sleep timer both S.T. and S.A. must logically be the same, and INC HR/SIN must be momentarily at zero. (See later section).

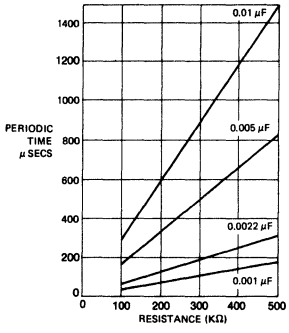


Fig.3 OSCILLATOR CHARACTERISTICS FOR V_P = 10V

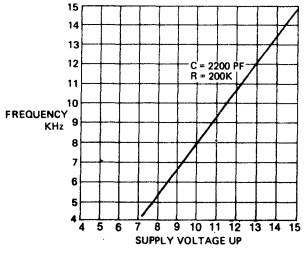


Fig.4 OSCILLATOR CHARACTERISTICS WITH VOLTAGE

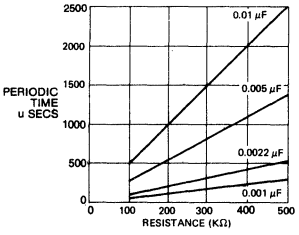


Fig.5 OSCILLATOR CHARACTERISTICS FOR V_P = 7.5V

ELECTRICAL CHARACTERISTICS

Voltage any pin with respect to V_n . . . . . 0 to +20V
Storage temperature. . . . . −65°C to +150°C
Operating temperature . . . . . −20°C to +70°C
Lead temperature (soldering 10 sec) . . . . . +300°C

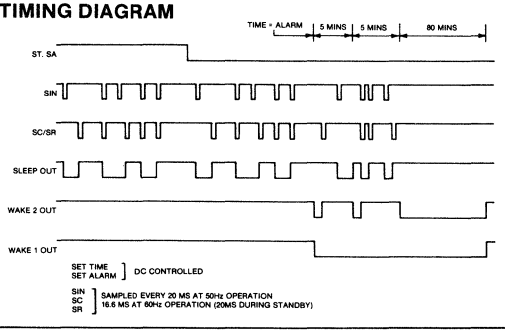
*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Characteristic	Min	Typ**	Max	Units	Conditions
Power Supply Voltage	6	10	18	Volts	$V_n = 0V$
Supply Current	—	2	—	mA	
50/60HZ Input					
Frequency (must be identical to anodes)	0	50/60	50,000	Hz	$V_p = 10V$
Logic '1' level	0.6Vp	—	Vp	Volts	
Logic '0' level	0.0	—	0.7	Volts	
Inputs (Excl Oscillators)					
Logic '1' level	0.6Vp	—	Vp	Volts	
Logic '0' level	0.0	—	0.7	Volts	
Segments Out (on)	—	30	—	mA	$V_{OUT} = 1.5V$
(off)	—	10	—	μA	
Wake 1, 2, Sleep Out (on)	—	30	—	mA	$V_{OUT} = 1.5V$
(off)	—	10	—	μA	
Wake 1, 2 (As Inputs)					
Logic '1' level	0.6Vp	—	Vp	Volts	
Logic '0' level	0.0	—	0.7	Volts	
Oscillators 1 and 2					
Hi level	—	5.5	—	Volts	Free run
Lo level	—	3.5	—	Volts	
Reset Level	—	—	0.7	Volts	

Unless specified otherwise, characteristics are defined with $V_p = 10V$ at $T_A = +25°C$.
**Typical values are at +25°C and nominal voltages.

NOTES:
1. Under no circumstances during IC operation must any pin either input or output be taken to a voltage more negative than V_n or IC malfunction will occur.
2. No input or output must be taken to a positive voltage greater than 20 volts or permanent damage can result.
3. No output must be allowed to dissipate a continuous power in excess of 100mW.
4. Total chip continuous power dissipation must not exceed 500mW.
5. The total current being returned to V_n through all device pins must not exceed 1 amp.

TIMING DIAGRAM



Input and Output Characteristics

INPUTS
S.A.
S.T.
INC HR (SIN)
INC MIN (SC/SR)
Active pull up's to V_p
Operate level logic '0'
250KΩ

50/60HZ count input, active pull down
For correct operation duty cycle of 50/60Hz must be 1:1 ± 20%

OUTPUTS
Normally open circuit
Operate "on" (low impedance typically 50Ω)

INPUTS
Wake 1 - as input '1' = 12hr '0' = 24hr
Wake 2 - as input '1' = 60Hz '0' = 50Hz

CLOCK INPUT NOISE ELIMINATION TIMING
50/60Hz - strobed every 4ms internally for less than 1 μs

Testing I.C. Facilities
1. Master reset: This can be activated by pulling OSC1 (Pin 26) and OSC 2 (Pin 25) to zero volts together.
2. Internal debounce and predivider logic may be bypassed if OSC 1 is taken to zero volts while OSC 2 is left running.
a. Under this condition Inc Hrs and Inc Mins pins are not debounced to allow fast incrementing for test purposes.
b. Also in this mode the 50/60Hz input pin is directed straight to the main counters under control of the sleep pin. If Sleep pin at '0'—50/60Hz input clocks 120 minute sleep counter, and with Sleep at '1' it clocks the main minutes count by passing the debounce and divide by 50/60 counter. Under this condition it also clocks the 5 minute snooze counter.

Operation Clock Radio Example
(showing some features and their use) - ref Figs.21 and 22.

Start-Up
Radio is connected to line for 1st time, then battery is inserted.

Assume following switch position RADIO OFF, SET TIME SWITCH = RUN

Actions
Display will illuminate and read 12:00 sleep indicator will flash at 1Hz. Set clock as indicated previously (Flashing will cease).

In 24hr mode 0:00 will illuminate with flashing sleep indicator.

Snooze Bar Action
IN RADIO OFF POSITION

1st button depression	Low volume radio (set required volume)
2nd button depression	Radio off
3rd button depression	Radio on low volume
4th button depression	Radio off

etc. . . .

IN RADIO ON POSITION
Radio comes on high volume (set wake volume required)

1st button depression	Low volume radio (mute facility)
2nd button depression	High volume
3rd button depression	as 1
4th button depression	as 2

Radio Auto
In auto, alarm is requested at "set alarm" time. If sleep is desired press button. Subsequent button pushes will have same effect as in radio "off" position.

Select Wake to Alarm Tone or Radio
Assume radio selected

At alarm time radio will come on at wake volume setting.

1st button depression	Radio will switch to low volume
2nd button depression	Radio will switch off
3rd button depression	Radio back a low volume

If after first depression radio is left untouched, radio will return to wake volume after five minutes.

If after 2nd depression radio is left untouched, radio will stay off for five minutes then return to wake volume.

This wake volume, if left, will be maintained for 80 mins unless radio is returned to radio ON or radio OFF switch position, changing switch momentarily from auto to ON or OFF and back to auto will reset alarm and re-request for same time next day. The above, repeating snooze, can be maintained idenfinitely if button is pushed before 80 mins elapses.

Note: 80 mins is timed either from alarm time, if untouched, or 80 mins from last button depression

Select Wake to Alarm Tone
The alarm tone or buzzer is obtained by placing positive feedback around the audio amplifier or radio in such a manner that the desired sound can be achieved and the feedback can be stopped by open circuit one point in the network.

At alarm time buzzer will sound:

On 1st button depression	Buzzer will cease and radio will switch to low volume
2nd button depression	Radio and buzzer will be off

If after first depression radio is left untouched, radio will return to buzzer after 5 mins.

If after 2nd depression radio is left untouched, radio and buzzer will be off and at 5 mins BUZZER WILL AGAIN SOUND.

As for radio position - radio will reset after 80 mins for 24 hrs. At any time in buzzer sequencing, buzzer radio select can be changed over to radio, then the radio will alternate high-low volume with button. Cancelling in buzzer mode is identical to radio mode.

Typical Application
To combine the S.A. and S.T. functions to provide simple and rapid clock setting. It is suggested that the following is incorporated in the clock radio.

Two toothed wheels are placed over two seperate sprung contacts and coupled to two concentric rotating knobs, (say 12 teeth each) along side is a three position switch labeled 'set time, run, set alarm'.

To set clock, select time or alarm and rotate Hrs knob, or mins knob, each click will result in one unit change of time, rapid rotation will result in 12 increments per revolution of knob.

The above procedure results in an easy to use system with the advantage over mechanical clocks of independent hrs and mins setting.

NOTE:
No carries from mins to hrs can occur during setting of time or alarm.

Use of Auto Tape
Fig.21 shows - the facility for automatically switching on an appliance (e.g. tape recorder) at a specific time and keeping appliance active for a period of time up to 120 mins. In this mode the wake output is made to start the sleep - timer at the wake time.

Use of 5 Min Delayed Alarm with Appliance Switching
In this mode of operation the wake 1 output is made to cancel the first alarm through the SC (inc hr) input such that radio or alarm time will only occur at the end of the first snooze period.

This result in appliance being activated at set alarm time and after 5 mins the alarm or radio will sound.

Fig.6 — shows a typical clock-radio block diagram
Fig.7 — shows the chip/display circuit.

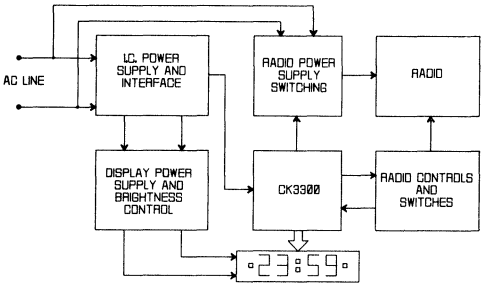


Fig.6

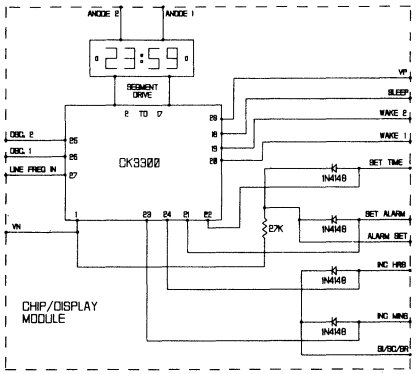


Fig.7

Interface with a Radio

There are many possible configurations of clock radios in use today and a wide range of different radio chassis are employed in these units. It is necessary therefore that the clock radio I.C. be sufficiently flexible to allow simple interfacing to be accomplished.

The following section gives different options, features and interfacing to demonstrate some of the approaches possible with the CK3300.

Power Supply Interface

To enable any existing line operated radio chassis to be used with the minimum of changes it is suggested that the following power supply is used with the adoption of a 2nd line transformer. This will (a) reduce the need for a change at the existing transformer. (It is unlikely that the existing transformer will be capable of provi ling the additional power required of the display).

a. Allow the electronic clock movement to be self contained therefore, keeping the interface wiring to a minimum.

b. Allow the same electronic movement to be used with several radio chassis.

Options

1. Without battery standby facility Fig.8
2. With battery standby facility Fig.9

Display Interface and Power Source

Four options are shown

1. No brightness control Fig.10
2. Day/night brightness (two level) Fig.11
3. Manual brightness control Fig.12
4. Automatic brightness control Fig.13

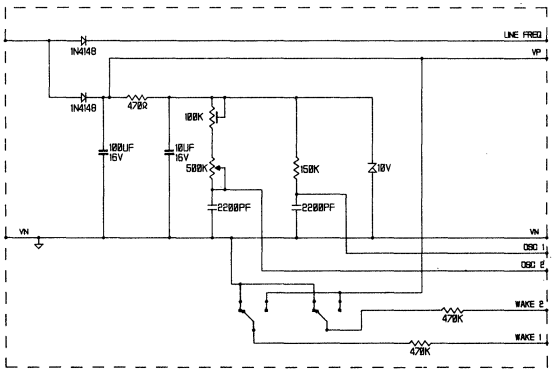


Fig.8 POWER SUPPLY INTERFACE WITHOUT STANDBY

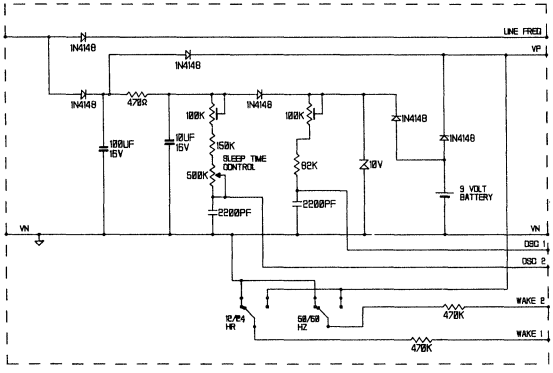


Fig.9 POWER SUPPLY INTERFACE WITH STANDBY OPTION

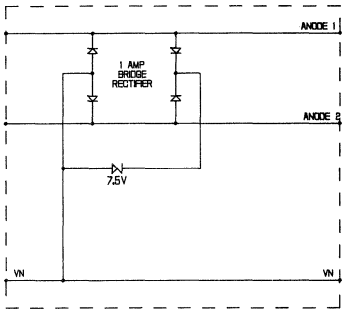


Fig.10 NO BRIGHTNESS CONTROL

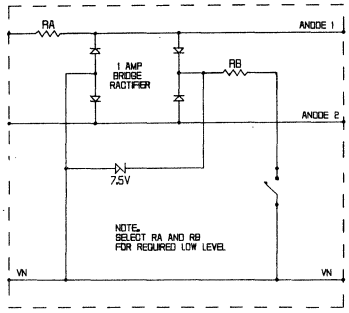


Fig.11 TWO LEVEL BRIGHTNESS CONTROL

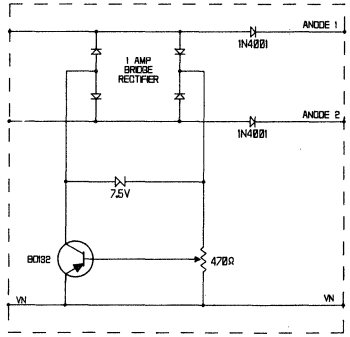


Fig.12 MANUAL BRIGHTNESS CONTROL

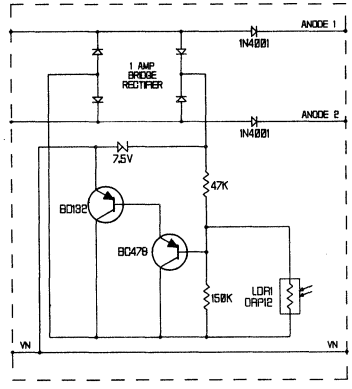


Fig.13 AUTOMATIC BRIGHTNESS CONTROL

Radio Switching
Option 1 Push button operation (Fig.14)
Option 2 Rotary switch operation (Fig.15)

Radio Powering
Option 1(Fig.16A, 16B) Direct audio amplifier control (no active components)
Option 2 (Fig.17) Power supply switching using Transistor
Option 3 (Fig.18) Power supply switching using a relay

Tone Generation
Option 1 (Fig.19) Saw tooth generation independ of radio
Option 2 (Fig.20) Sine wave generation independent of radio
Option 3 (Fig.15,16B) Sine wave using the existing radio audio amplifier

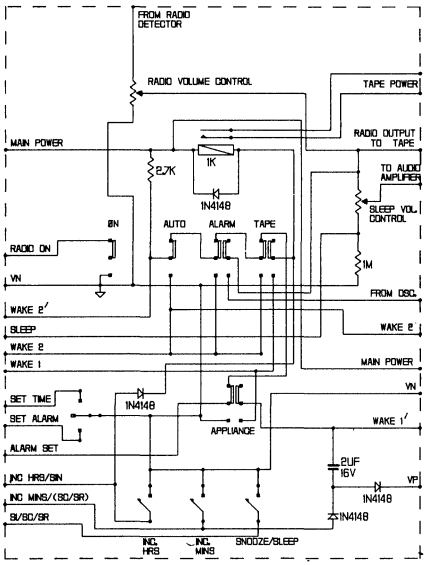


Fig.14 RADIO SWITCHING

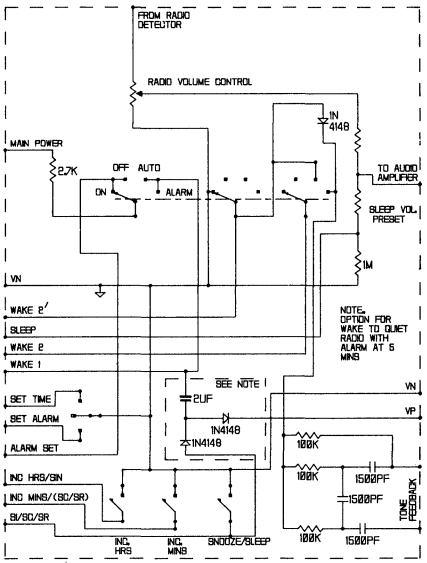


Fig.15 RADIO SWITCHING

Additional Facilities
1. Automatic tape recording (Fig.21)
2. Appliance switching with delayed alarm (Fig.21)
3. Wake to normal radio with 5 minute alarm over-ride (Fig.21)
4. Wake to quiet radio with 5 minute alarm over-ride (Figs. 21 and/or 22)
5. Ratio muting during normal radio listening (Figs.21 and /or 22)

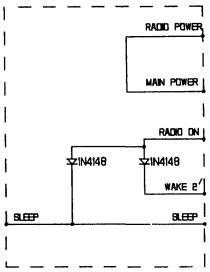


Fig.16a RADIO SWITCHING BY BIAS CHANGE

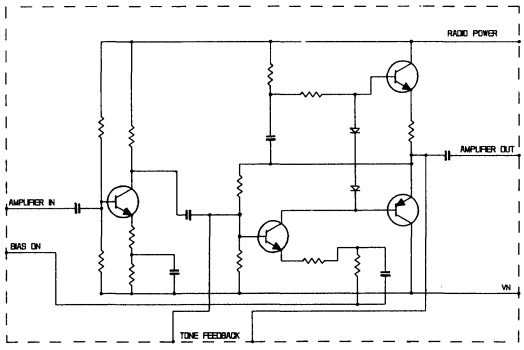


Fig.16b TYPICAL TRANSFORMERLESS AUDIO AMPLIFIER

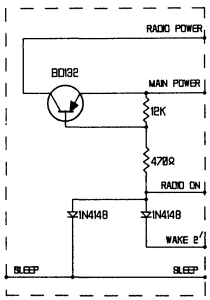


Fig.17 RADIO POWER SWITCHED BY TRANSISTOR

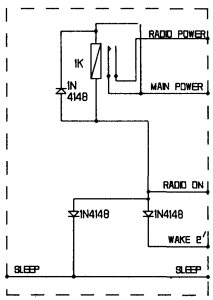


Fig.18 RADIO POWER SWITCHED BY RELAY

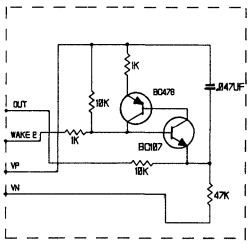


Fig.19 SAW TOOTH OSC

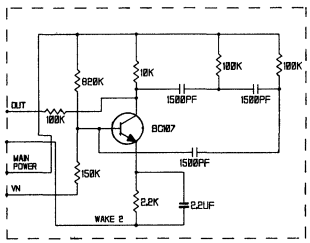


Fig. 20 SINE-WAVE OSC

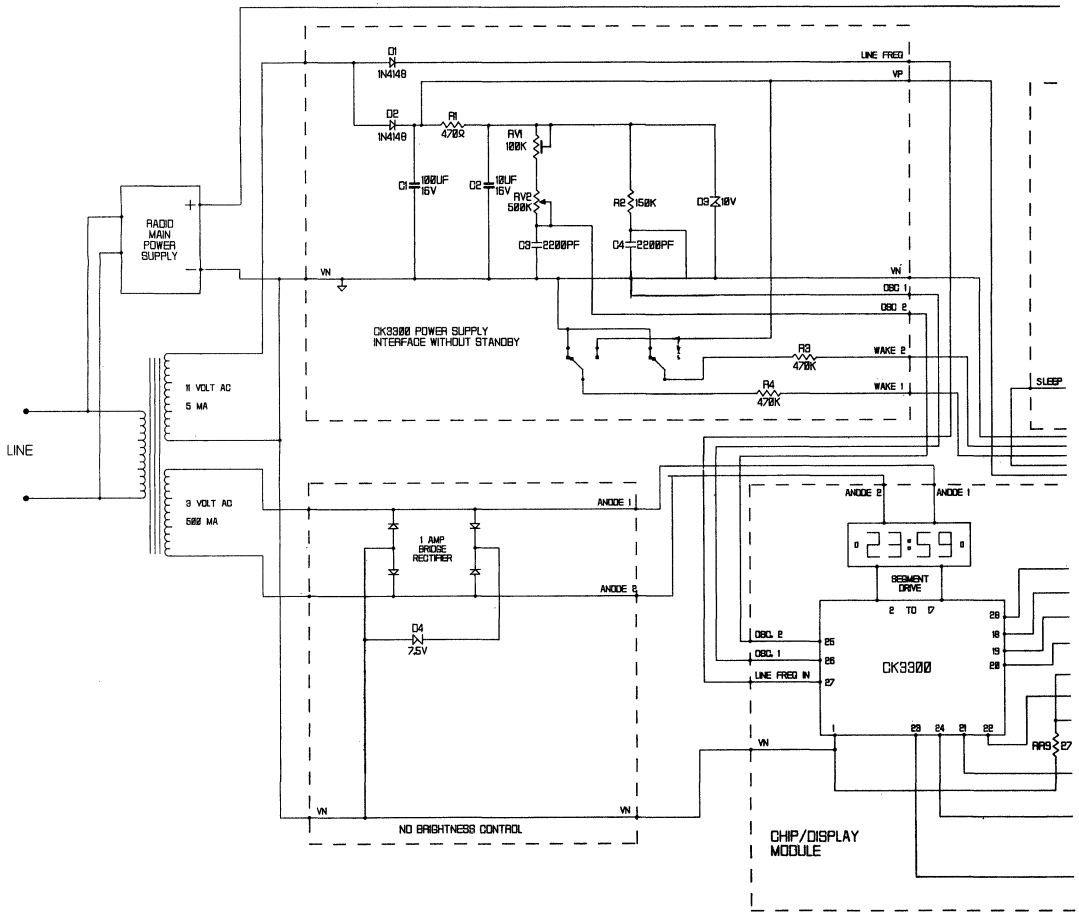


Fig.21(a) TYPICAL "BASIC" CLOCK RADIO CIRCUITRY

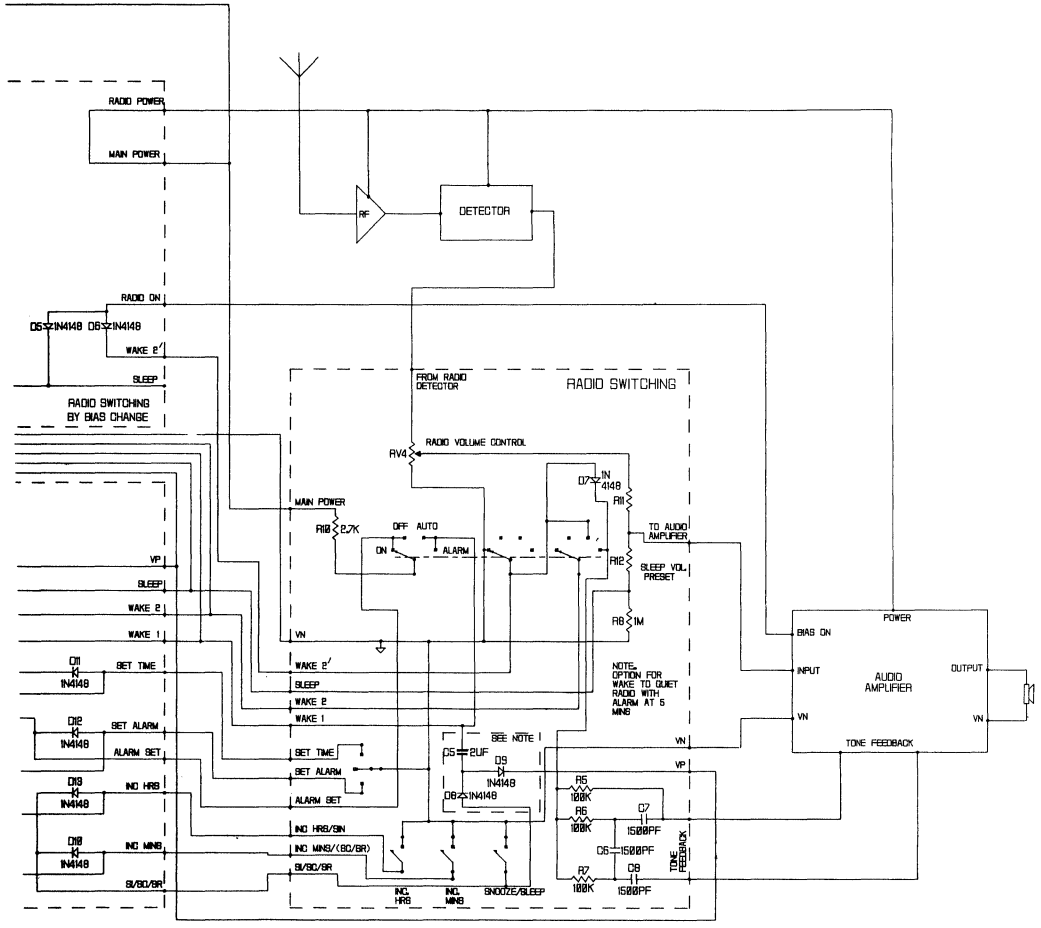


Fig.21(b) TYPICAL "BASIC" CLOCK RADIO CIRCUITRY

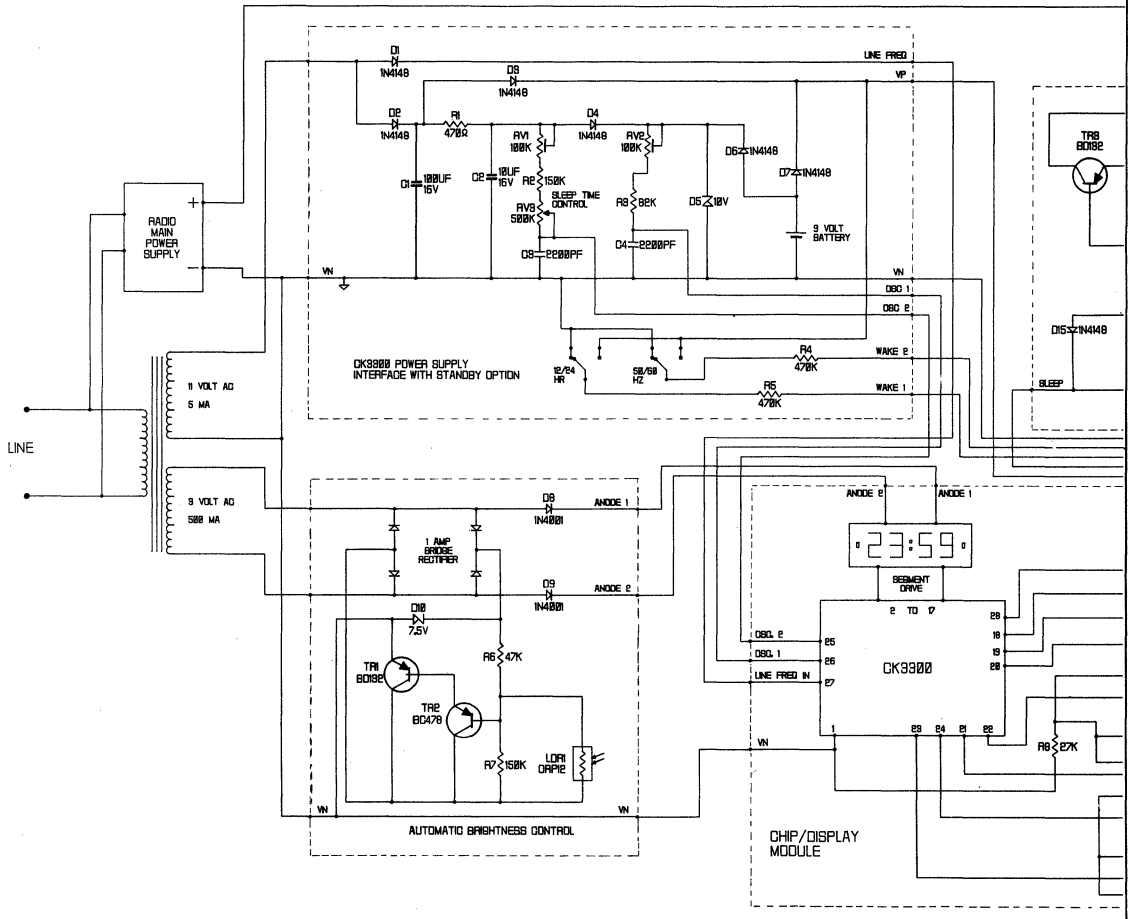


Fig.22(a) TYPICAL "FULL-FEATURE" CLOCK RADIO CIRCUITRY

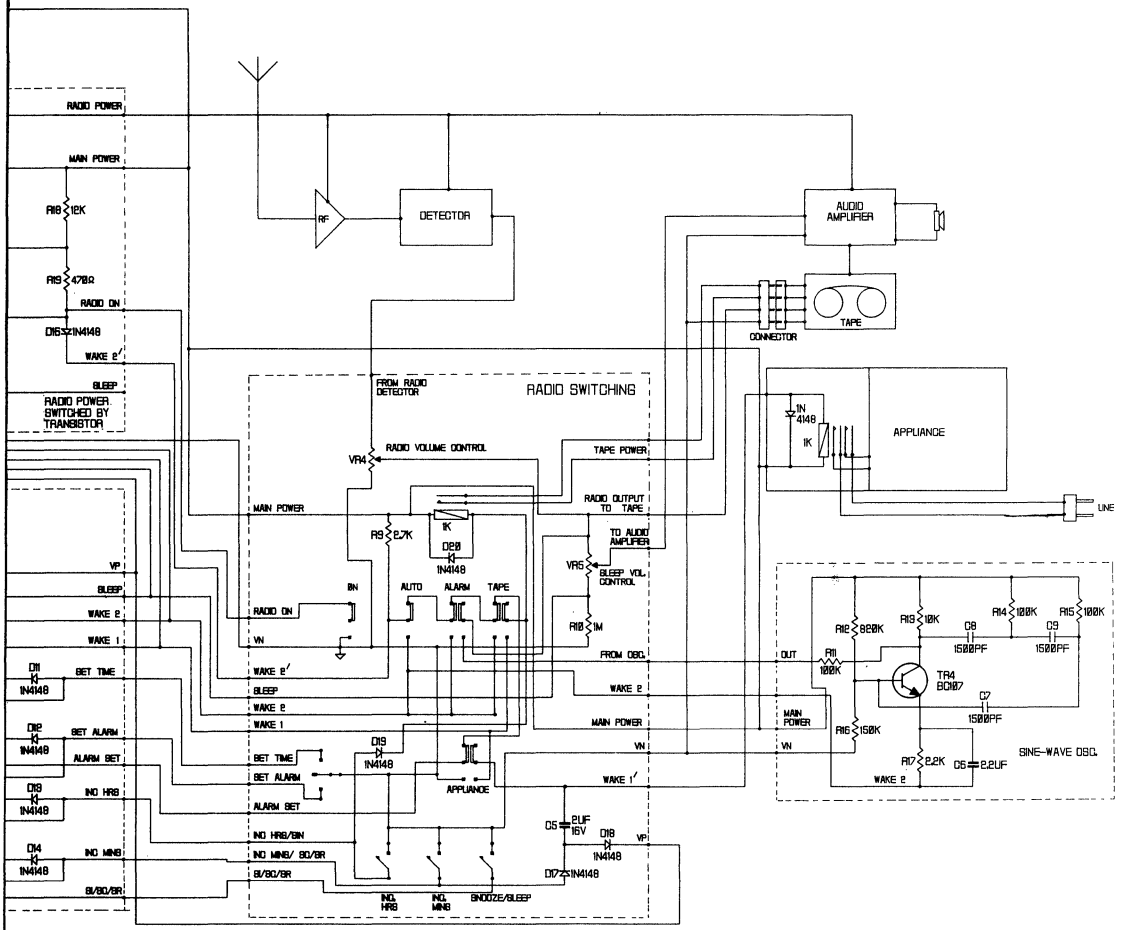


Fig.22(b) TYPICAL "FULL-FEATURE" CLOCK RADIO CIRCUITRY

GENERAL INSTRUMENT

SAA1024
SAA1025
AY-5-8100
AY-5-8101
AY-5-8300
AY-5-8302
AY-5-8310
AY-5-8320
AY-5-8410
AY-5-8411
AY-5-8420
AY-3-8500
AY-3-8500-1

4

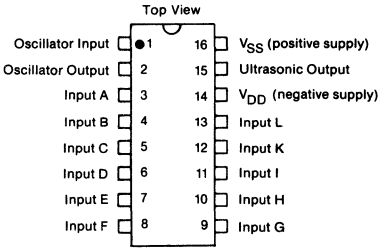
Ultrasonic Remote Control Transmitter

FEATURES

- 30 channels. 346.4Hz spacing in the range 34-44KHz.
- 9V battery operation.
- 4.433 MHz TV crystal master oscillator.
- Touch or mechanical keyboard, 1 of 5 and 1 of 6 coding.
- Low standby current drain (10 μA).
- Equivalent to I.T.T. SAA1024.

PIN CONFIGURATION

16 LEAD DUAL IN LINE

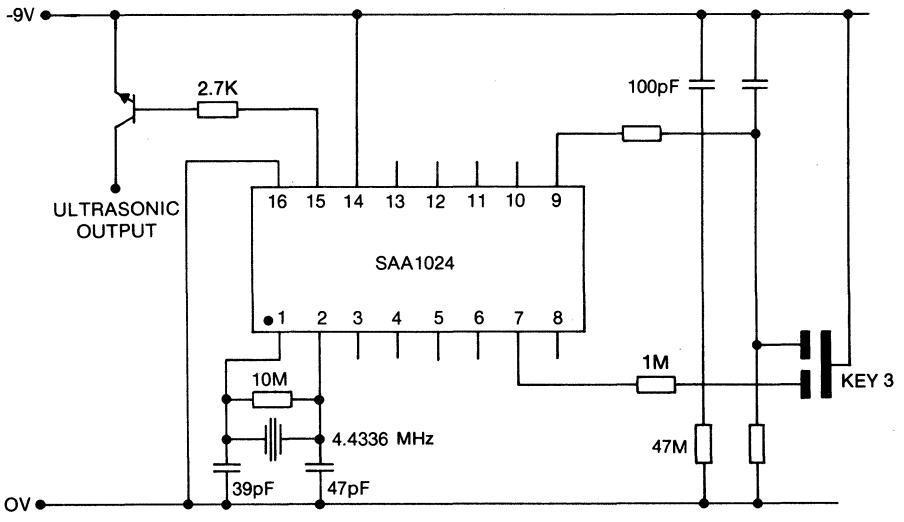


DESCRIPTION

The Transmitter allows the transmission of 30 commands using 30 different ultrasonic frequencies in the range 33.945 to 43.990 KHz. It is designed for battery operation and uses a low cost TV crystal as the master oscillator. When inactive the circuit is in a standby mode having a current drain of less than 10μA. As soon as a valid input code is applied the main circuit is powered up and transmission commences.

The code input can be generated by either a mechanical keyboard or a touch plate.

TRANSMITTER WITH TOUCHPLATE INPUT



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin . . . . . +0.3 to −12 Volts
Output current 10mA
Storage temperature range. . . . . −65°C to +150°C
Ambient operating temperature range . . . . . −10°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
V_{DD} = −7 to −10V
Operating Temperature (T_A) = −10°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Frequency	—	4.4336	—	MHz	See diagram for external components.
Output Frequencies	—	See Table	—		
Input logic '0'	—	—	−0.5	V	
Input logic '1'	−3	—	—	V	
Input leakage	—	—	200	nA	at 70°C, Vin = −3V
Output On Resistance	—	500	—	Ω	to V_{SS}, V_{OUT} = −1V
Output Off Resistance	—	1.5	—	K Ω	to V_{DD}, V_{OUT} = V_{DD}+0.5V
Standby current drain	—	—	10	μA	
Operating current drain	—	8.0	—	mA	

**Typical values are at +25°C and nominal voltages.

ULTRASONIC FREQUENCIES

Crystal = 4.4336MHz (code in negative logic)

Key	Frequency	a	b	c	d	e	f	g	h	i	k	l
1	33,945 Hz	0	0	0	0	1	0	0	1	0	0	0
2	34,291 Hz	0	0	0	0	1	0	0	0	0	0	1
3	34,638 Hz	0	0	0	0	1	0	1	0	0	0	0
4	34,984 Hz	0	0	0	0	1	0	0	0	0	1	0
5	35,330 Hz	0	0	0	0	1	1	0	0	0	0	0
6	35,677 Hz	0	0	0	0	1	0	0	0	1	0	0
7	36,023 Hz	1	0	0	0	0	1	0	0	0	0	0
8	36,370 Hz	1	0	0	0	0	0	0	0	1	0	0
9	36,716 Hz	0	1	0	0	0	1	0	0	0	0	0
10	37,062 Hz	0	1	0	0	0	0	0	0	1	0	0
11	37,409 Hz	0	0	1	0	0	1	0	0	0	0	0
12	37,755 Hz	0	0	1	0	0	0	0	0	1	0	0
13	38,101 Hz	0	0	0	1	0	1	0	0	0	0	0
14	38,448 Hz	0	0	0	1	0	0	0	0	1	0	0
15	38,794 Hz	1	0	0	0	0	0	1	0	0	0	0
16	39,141 Hz	1	0	0	0	0	0	0	0	0	1	0
17	39,487 Hz	0	1	0	0	0	0	1	0	0	0	0
18	39,833 Hz	0	1	0	0	0	0	0	0	0	1	0
19	40,180 Hz	0	0	1	0	0	0	1	0	0	0	0
20	40,526 Hz	0	0	1	0	0	0	0	0	0	1	0
21	40,872 Hz	0	0	0	1	0	0	1	0	0	0	0
22	41,219 Hz	0	0	0	1	0	0	0	0	0	1	0
23	41,565 Hz	1	0	0	0	0	0	0	1	0	0	0
24	41,911 Hz	1	0	0	0	0	0	0	0	0	0	1
25	42,258 Hz	0	1	0	0	0	0	0	1	0	0	0
26	42,604 Hz	0	1	0	0	0	0	0	0	0	0	1
27	42,951 Hz	0	0	1	0	0	0	0	1	0	0	0
28	43,297 Hz	0	0	1	0	0	0	0	0	0	0	1
29	43,643 Hz	0	0	0	1	0	0	0	1	0	0	0
30	43,990 Hz	0	0	0	1	0	0	0	0	0	0	1

Ultrasonic Remote Control Receiver

FEATURES

- 30 Control Channels.
- 16 TV Channels.
- 3 Analog Channels.
- ON/OFF Channel.
- Normalize Control.
- Local Control.
- Uses 4.4MHz TV Crystal.
- Equivalent to I.T.T. SAA1025.

DESCRIPTION

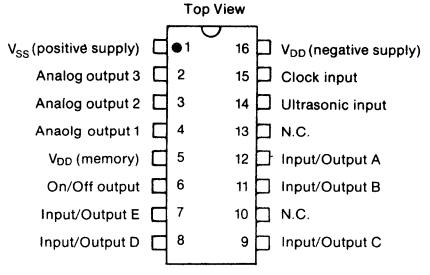
The Receiver has 30 control channels, each channel being allocated a separate ultrasonic frequency. Sixteen of the channels are allocated to selection of TV programs, six are used to control three analog outputs, one for On/Off, one for Normalizing, one for Muting and five are left spare. All channels are output on a 5 line binary bus. The bus is also used as an input for local control.

The analog channels have a pulse width modulated output with 31 possible values, the time taken to go from maximum to minimum being 5.5 seconds. The Normalize button sets the outputs approximately to their mid-point.

The ON/OFF channel toggles every time it is activated, there is a delay of approximately 0.7 seconds to prevent accidental operation.

PIN CONFIGURATION

16 LEAD DUAL IN LINE



To prevent false operation the frequency of the ultrasonic input is measured in the following manner. As soon as the signal appears a 23mSec. timer is started, at the end of this period the room reflections will have died away.

The frequency is then measured for 23mSec. and the appropriate output activated. If at any time a signal is received with a period shorter than 18μSec. or longer than 36μSec. the receiver is reset. Out of band and noisy signals are therefore rejected.

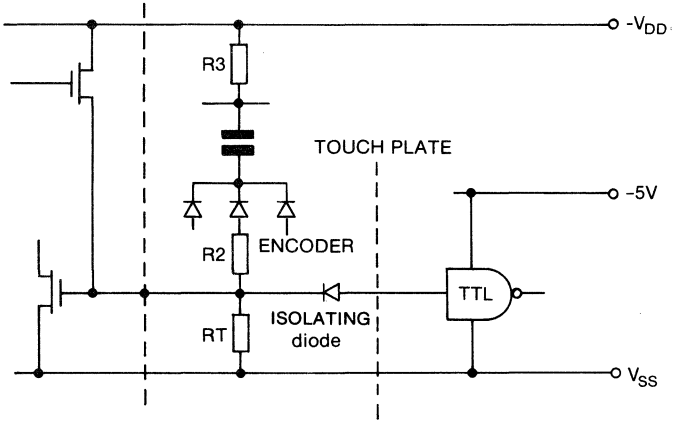


Fig.1 INPUT/OUTPUT CIRCUIT

PIN FUNCTIONS

Pin No.	Name	Function
1	V_{SS}	Positive supply.
16	V_{DD}	Negative supply 18V nominal.
5	V_{DD} (memory)	Negative supply to D/A store, allowing the analog values to be retained with very low power consumption (Typ. 0.2mA at 10V).
15	Clock Input	This pin is driven by a 4.4336MHz crystal oscillator. The input signal should be a minimum of 4V peak to peak.
14	Ultrasonic Input	The ultrasonic signal should be capacitively coupled and be at least 500 mV peak to peak. The first incoming pulse triggers a 23.1mS timer and after a delay of this period, two measurements of the ultrasonic signal are made over the following two 23.1mS periods. If the measurements produce a comparison, an output pulse 23.1mS long is generated after a further pause of 46.2mS. With continuous input signals an output pulse is generated every 184.8mS. During the complete receiving time the period of the ultrasonic signal is measured. If it is less than 18μSec or greater than 36μSec the signal is rejected and the receiver is set back to the start conditions and a new measuring cycle commences. The input signals need not be completely accurate for satisfactory reception. At the lowest frequency an error of $\pm$0.51% can be tolerated and at the highest $\pm$0.39%.
2, 3, 4	Analog Outputs	These outputs are in the form of a pulse, the mark to space ratio of which can be changed in 31 steps from 0:31 to 31:0, the repetition frequency being 8.99KHz. The mark space ratio is incremented by one step about 115mSec after the start of an ultrasonic command, thereafter it is incremented every 184.8mSec. The output stage is an open drain MOS transistor which appears as a 1 KOhm (Max.) resistor connected to V_{SS} when ON and an open circuit when OFF. At power ON the outputs are normalized to the following mark space ratios: Output 1 16:15 Output 2 18:13 Output 3 10:21 When command 4 (Normalize) is received, Outputs 1 and 2 are reset to their normalized values. Output 3 is unchanged. When command 2 (Mute) is received Output 3 is turned OFF, a further command re-enables the output. A delay of approximately 0.7 seconds is built in to this control to prevent false operation.
6	ON/OFF Output	This output is toggled ON and OFF by reception of command 1, the command must be present for 0.7 sec. At power ON the output is set to the OFF condition. When in the OFF condition the Analog outputs are prevented from changing. Also, when OFF, any one of the 16 channels for selecting TV programs, if present for 0.7 seconds, will change this output to the ON condition. However, these channels will not switch the output to OFF. The output can also be switched ON by connecting pin 6 to V_{SS} for 10 μ seconds.
7, 8, 9, 11, 12	Input/Output A, B, C, D, E	These pins have the dual function of receiving input commands from local keyboard or touch plate and for providing output control signals in response to commands from the transmitter or the keyboard. When the receiver is inactive the pins are held to within 1 Volt of V_{SS} by R1 (Fig.1). If a touch contact is activated current flows through R3 and R2 (Safety Isolating resistors) into R1 driving the input negative. When the input voltage exceeds 3 Volts for at least 10μSec the command is accepted and after a processing time of 46.2mSec an output pulse 23.1mSec long is generated. During the output pulse the output pin is driven negative by the output transistor. The output current is sufficient to drive TTL (Fig.2). When commands are received from both the remote transmitter and the local keyboard the local command takes precedence.

NOTE: Pin 6 — An option is available whereby this output can be turned "off" by the reception of a channel 1 command but not "on".

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin . . . . . +0.3 to -20V
Output Current 10mA
Storage Temperature Range . . . . . -65°C to +150°C
Ambient Operating Temperature Range . . . . . -20°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = OV
V_{DD} = -16.5 to -19.5V
Fc = 4.4336MHz
Operating Temperature (T_A) = -20°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Input					
Logic 0	+0.3	—	−1	Volts	
Logic '1'	−4	—	−19.5	Volts	
Capacitance	—	—	10	pF	
Ultrasonic Input	0.5	—	—	Vp-p	capacity coupled
Inputs A-E					
Logic '0'	+0.3	—	−1	Volts	
Logic '1'	−3	—	−19.5	Volts	
Outputs A—E					
Logic '0'	—	—	−0.5	Volts	RL = 4.7M to V_{SS}
Logic '1'	−5.5	—	—	Volts	Iout = 1.6mA (Fig.1)
On/Off Output					
Off leakage	—	—	10	μA	Vout = −19.5 Volts
On resistance	—	—	1	KOhm	Vout = −1V (resistance to V_{SS})
Analog Outputs					
Off leakage	—	—	10	μA	Vout = −19.5 Volts
On resistance	—	—	1	KOhm	Vout = −1V (resistance to V_{SS})
Output frequency	—	8.99	—	KHz	
Increment time per stop	—	184.8	—	mSec	
Memory Supply Current	—	0.2	—	mA	V_{DD}(mem) = −10V
Chip Supply Current	—	20	—	mA	V_{DD} = -19V

**Typical values are at +25°C and nominal voltages.

TYPICAL CHARACTERISTIC CURVE

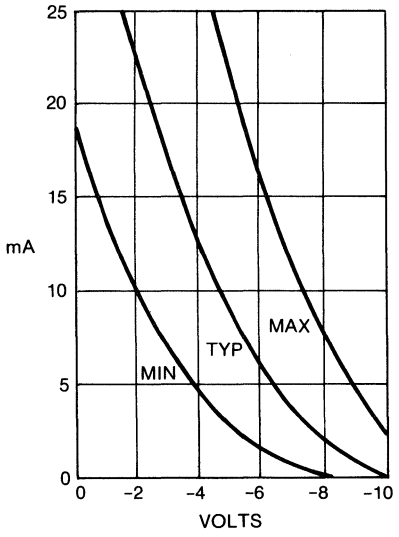


Fig.2 OUTPUT CHARACTERISTICS

FREQUENCY/CHANNEL ALLOCATIONS

F = Channel Select Clock frequency 4.4336 MHz Output in Negative logic

CH	Frequency Hz	Channel Function	Output Code A	B	C	D	E
1	33,944.89	ON/OFF	1	0	0	0	0
2	34,291.21	Mute A3	1	0	0	0	1
3	34,637.65	A1 up	0	1	0	0	0
4	34,984.02	Normalize	0	1	0	0	1
5	35,330.40	A1 down	1	1	0	0	0
6	35,676.78	Z1	1	1	0	0	1
7	36,023.15	A2 up	0	0	1	0	0
8	36,369.53	Z2	0	0	1	0	1
9	36,715.91	A2 down	1	0	1	0	0
10	37,062.28	Z3	1	0	1	0	1
11	37,408.66	A3 up	0	1	1	0	0
12	37,755.03	Z4	0	1	1	0	1
13	38,101.41	A3 down	1	1	1	0	0
14	38,447.79	Z5	1	1	1	0	1
15	38,794.16	F1	0	0	0	1	0
16	39,140.54	F2	0	0	0	1	1
17	39,486.92	F3	1	0	0	1	0
18	39,833.29	F4	1	0	0	1	1
19	40.179.07	F5	0	1	0	1	0
20	40,526.05	F6	0	1	0	1	1
21	40,872.42	F7	1	1	0	1	0
22	41,218.80	F8	1	1	0	1	1
23	41,565.18	F9	0	0	1	1	0
24	41,911.55	F10	0	0	1	1	1
25	42,257.93	F11	1	0	1	1	0
26	42,604.31	F12	1	0	1	1	1
27	42,950.68	F13	0	1	1	1	0
28	43,297.06	F14	0	1	1	1	1
29	43,643.43	F15	1	1	1	1	0
30	43,989.81	F16	1	1	1	1	1

Radio Receiver Frequency Counter/Display Driver

FEATURES

- Three frequency ranges: MW 2999KHz, SW 29.995MHz, VHF 299.95MHz.
- Mask programmable IF offset, Standard part is 460KHz on MW and SW, 10.7MHz on VHF.
- Channel mode 0-99 channel spacing 300KHz, Standard part channel 0 is 87MHz.
- High voltage segment and digit outputs give direct drive of fluorescent displays.
- Inversion control for digit select outputs.
- Direct drive of liquid crystal displays.
- 1.28MHz master clock input frequency.
- 300KHz input with 8mS sample time.
- TTL compatible inputs and outputs.
- 50Hz output to drive the AY-5-1200A digital clock.

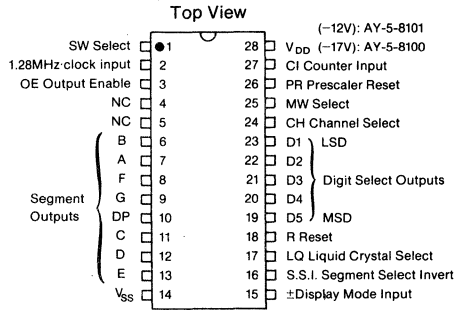
DESCRIPTION

The AY-5-8100/8101 are four and a half digit frequency counters for use in Radio Receivers. Three main frequency ranges are provided, 2999KHz and 29.995MHz with 460KHz IF offset and 299.95MHz with 10.7MHz IF offset. For use in VHF FM receivers a channel mode is available In this mode a channel number from 0 to 99 is displayed together with a "+" or "−" sign for tuning indication. In this mode the IF is 10.7MHz and channel 0 is 87MHz.

The outputs are multiplexed in five time slots onto a seven segment bus. Digit and segment outputs have high voltage capability and will drive fluorescent displays directly. A pin option allows the driving of liquid crystal displays using the two-frequency multiplexing system.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



SYSTEM DIAGRAM

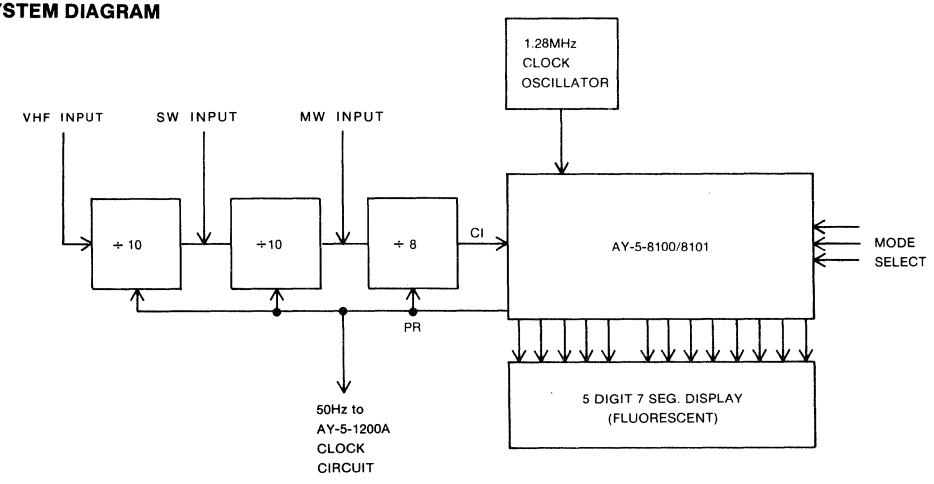


Fig.1 FREQUENCY COUNTER CLOCK CONNECTION DIAGRAM—DIRECT FLUORESCENT DISPLAY DRIVE

PIN FUNCTIONS

Pin No.	Name	Function
1	SW Select	Selects 29.995MHz counter range when at logic '0'. See Mode Select truth table.
2	1.28MHz Clock	Master clock input controls timing of whole system.
3	Output Enable	Disables the outputs when taken to logic '0'.
4	—	
5	—	
6-13	Segment Outputs	The digits to be displayed are output on these pins in 7 segment code. They are at logic '1' to display. These outputs will also drive fluorescent, liquid crystal and low current LED displays.
14	V_{SS}	Positive supply.
15	±Display Mode Input	Selects either combined or separate + or − display when in channel mode. Logic '0' selects combined mode. In the combined mode the horizontal bar is output on segment "g" and the vertical bar on segment "f". In the separate mode the − sign is output on segment "g" and the + sign on segment "f".
16	Segment Select Invert	When taken to logic '1' inverts the Segment Select outputs (Note 1).
17	Liquid Crystal Select	When taken to logic '1' the output timing is arranged to drive liquid crystal displays using two frequency multiplexing.
18	Reset	Master reset to all counters and registers. Resets when at logic '1'.
19-23	Digit Select Outputs D1-D5	These outputs sequentially select the digit to be displayed. They are normally at logic '1' to display. The outputs are high voltage and are capable of driving fluorescent and liquid crystal displays directly. Each digit is on for 4mS. A bonding option gives inverted outputs.
24	Channel Select	Selects channel mode when at logic '0' and SW and MW are at logic '1'. See Mode Select truth table.
25	MW Select	Selects 2999KHz counter range when at logic '0'. See Mode Select truth table.
26	Prescaler Reset	This output resets the external prescaler divider, at logic '0' during count interval.
27	Counter Input	Frequency measuring input. Frequency range 10KHz to 600KHz.
28	V_{DD}	Negative supply.

NOTE:
1. If the digit invert bonding option is used (bonding to logic '1') the SSI input logic sense will be inverted.

FREQUENCY COUNTER OPERATION

The frequency counter section is intended to work with an external prescaler. The three frequency ranges require division ratios of 8, 80 and 800. The appropriate IF offset is loaded into the counter before measuring. The local oscillator must always be at a higher frequency than the receiver frequency.

Measurement period	8mSec
Reading rate	50 per second
Master clock frequency	1.28MHz

Mode	Display Range D5	D4	D3	D2	D1		Discrimination	Prescaler	IF
MW	2	9	9	9		KHz	1KHz	÷ 8	460
SW	2	9	9	9	5	MHz	5KHz	÷ 80	460
FM	2	9	9	9	5	MHz	50KHz	÷800	10.7
CH	±	9	9			MHz	300KHz	÷800	10.7

NOTES:
1. Leading zeros are blanked.
2. In Channel Mode the + or − signs are lit if the receiver is more than 50KHz off tune.
3. The IF offset is mask programmed and can in principle be made to any value.
4. In Channel Mode, Channel 0 = 87MHz.

MODE SELECTION

MW	SW	CH	OE	Mode
0	1	X	1	MW
1	0	X	1	SW
1	1	1	1	VHF
1	1	0	1	VHF/Channel
0	0	0	1	Counter mode
X	X	X	0	Clock

DISPLAY OUTPUT

The output is in 7 segment form multiplexed into five time slots at a rate of 50Hz. All the display outputs have high voltage capability and will drive fluorescent displays directly. LED displays can either be driven directly or with simple interfacing depending on the digit size.

A pin selected option allows the direct driving of liquid crystal displays using two frequency multiplexing (125Hz and 8000Hz).

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin (except Segment and Digit Outputs) . . . . . +0.3V to −20V
Voltage on Segment and Digit Outputs with respect to V_{SS} pin . . . +0.3V to −35V
Ambient operating temperature range . . . . . 0°C to +70°C
Storage temperature range. . . . . −65°C to +150°C
Power dissipation. 600mW

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

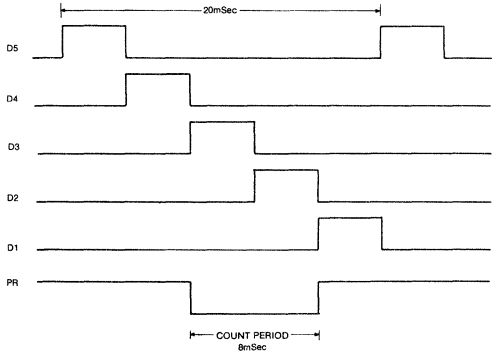
V_{SS} = +5V ±0.5V
V_{DD} = −12V ±1V (AY-5-8100) or -7V ±1V (AY-5-8101)
V_{II} = −28V ±2V
Operating Temperature (T_A) = 0°C to +70°C
Fc = 1.28MHz ±0.01%

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
Input logic '0' level	V_{IL}	—	—	+0.8	Volts	
Input logic '1' level	V_{IH}	V_{SS} −1	—	—	Volts	
Input load current (SW, 1.28MHz, OE, MW, CI, CH)	I_{IL}	—	—	0.2	mA	$V_{IN} = -V_{DD}$ Note 1
Input sink current (DMI, SSI, LQ, R)	I_{IH}	—	—	0.2	mA	$V_{IN} = +V_{SS}$ Note 2
Input capacitance	C_{IN}	—	—	10	pF	V_{IN} = OV f = 1MHz
Digit Select Outputs				—		
Logic '1' On Current		2	—		mA	$V_{OUT} = (V_{SS} - 2)V$ Fig.1
Logic '0' Off Current		—	—	10	μA	$V_{OUT} = (V_{II} + 1)V$ Fig.1
Segment Outputs						
Logic '1' On Current		5	—	—	mA	$V_{OUT} = (V_{SS} - 2)V$ Fig.2
Logic '0' Off Current		—	—	10	μA	$V_{OUT} = (V_{II} + 1)V$ Fig.2
PR Output						
Logic '0'	V_{OL}	—	—	0.4	Volts	} Load = 2TTL gates (3.2mA), 3.3K
Logic '1'	V_{OH}	V_{CC} −2.2		—	Volts	} resistor to V_{DD}, +20pF
Clock input frequency	f_C		1.28	1.4	MHz	Note 3
Clock pulse width		350	—	—	nSec	logic '0' or '1'
Count input frequency		10	—	600	KHz	
Count input pulse width		600	—	—	nSec	logic '0' or '1'
Multiplex rate		—	50	—	Hz	
Power consumption		—	450	—	mW	

**Typical values are at +25°C and nominal voltages.

NOTES:
1. These inputs have resistors of nominally 170Kohm connected to V_{SS}.
2. These inputs have resistors of nominally 170Kohm connected to V_{DD}.
3. For correct frequency readings the clock input frequency must be 1.28 MHz ± 0.01%.

TIMING DIAGRAM



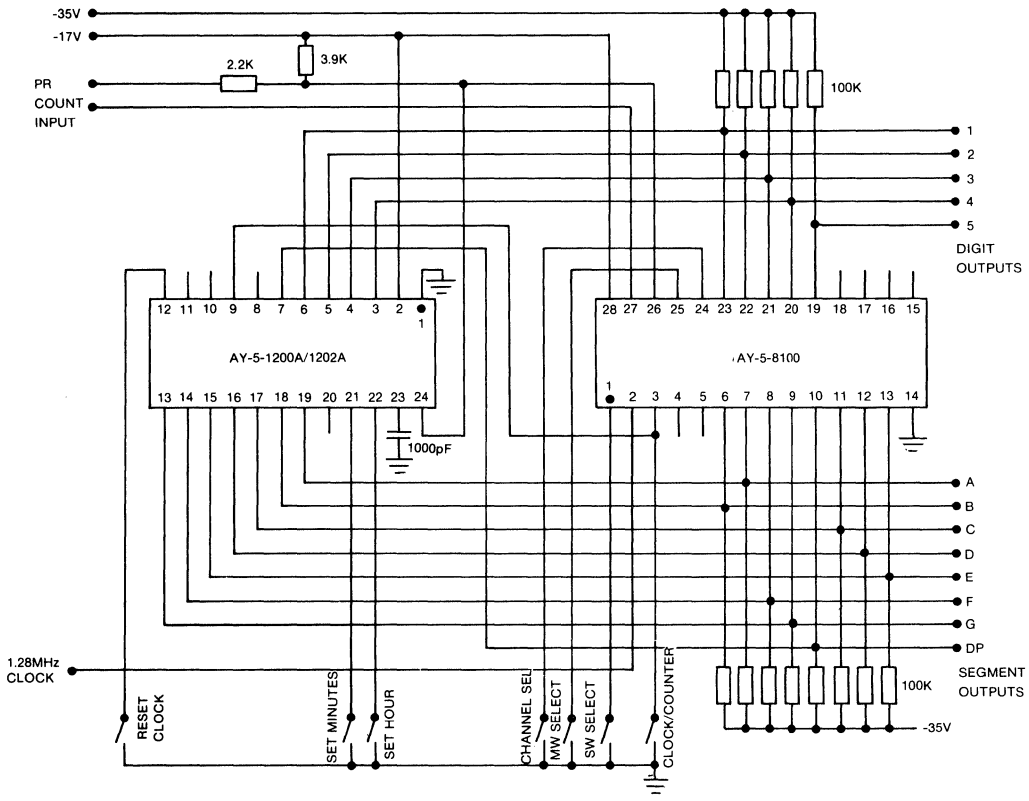


Fig.2 FREQUENCY COUNTER/CLOCK CONNECTION DIAGRAM-DIRECT FLORESCENT DISPLAY DRIVE

TV Display Series

FEATURES

- Channel Display 0 to 15 or 1 to 16 or 00 to 99.
- 4 Digit Clock Display option.
- Color character on black background or color character on color background.
- 14 or 24 DIL package.

OPTIONS

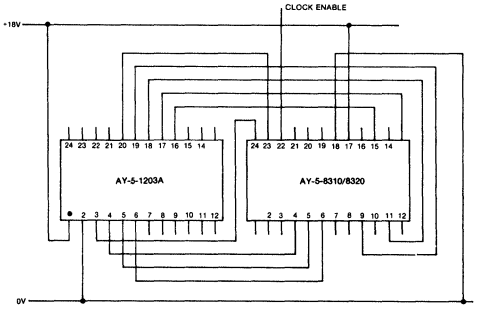
Part Number	Channel	Time	Character/ Background
AY-5-8300	0-15	No	Color/Black
AY-5-8302	1-16	No	Color/Color
AY-5-8310	0-15 or 00-99	Yes	Color/Black
AY-5-8320	1-16	Yes*	Color/Color

*The AY-5-8320 is capable of either simultaneous or separate time and channel display.

DESCRIPTION

The AY-5-8300 series is a family of MOS circuits designed to display channel and time information on the screen of a TV set. The information is displayed as color characters on a black or color background. Channel information is displayed either as a single character 0 to 15 or 1 to 16 or as a dual character 00 to 99. Time is provided as a 4 digit hours and minutes display. The display is positioned at the top right hand corner of the screen, the display may be permanent or momentary.

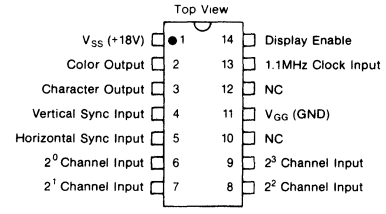
INTERCONNECT DIAGRAM FOR TV TIME DISPLAY



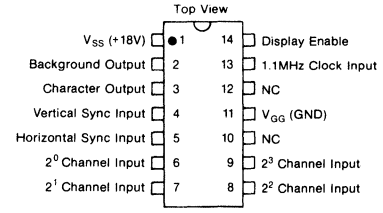
PIN CONFIGURATION

14 LEAD DUAL IN LINE

AY-5-8300

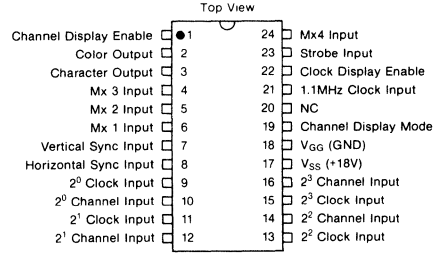


AY-5-8302

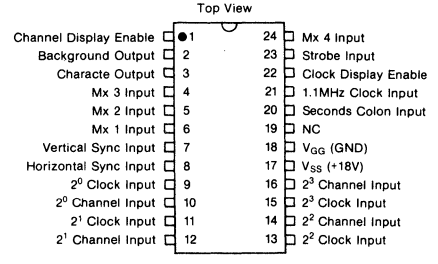


24 LEAD DUAL IN LINE

AY-5-8310



AY-5-8320



PIN FUNCTION

Name	Function
Character Output (All types)	Defines the character outlines. At logic '1' when displaying a character.
Vertical Sync Input (All types)	Resets the circuit at the end of each frame. At logic '0' during vertical flyback.
Horizontal Sync Input (All types)	Activates the line counter. At logic '0' during horizontal flyback.
1.1 MHz Clock Input (All types)	Determines character position and width. Must be synchronized by horizontal sync pulse to prevent ragged edges on character.
Channel Inputs 2^0—2^3 (All types)	See table below.
Color Output (AY-5-8300/8310)	Determines the character color. Goes to logic '1' during a character block.
Background Output (AY-5-8302/8320)	Defines the background block. At logic '1' when outputting background.
Display Enable (AY-5-8300/8302)	When taken to logic '1', the display is enabled. If an RC network is connected to this pin, a momentary display can be obtained.
Channel Display Enable (AY-5-8310/8320)	When taken to logic '1', the channel dsplay is enabled. If an RC network is connected to this pin, a momentary display can be obtained.
Clock Display Enable (AY-5-8310/8320)	When taken to logic '1', the clock display is enabled.
Clock Inputs 2^0—2^3 (AY-5-8310/8320)	Multiplexed 4 digit BCD clock data inputs such as available from the AY-5-1203A clock circuit.
Mx1—Mx4 (AY-5-8310/8320)	Multiplex inputs, at logic '1' during multiplex time slot. For the AY-5-8310, when operating in the 00-99 channel mode, Mx1 and Mx2 time slots are used.
Strobe Input (AY-5-8310/8320)	This input must go to a logic '1' during the middle of each Mx time slot to load the clock data into the chip.
Channel Display Mode (AY-5-8310)	When at logic '1', the 0-15 channel mode is selected; logic '0' for 00-99 channel mode.
Seconds Colon Input (AY-5-8320)	This input controls the colon between the hours and minutes display. When at logic '0', the colon is blanked. If connected to the DP output of the AY-5-1203A clock circuit, the colon will flash once per second.

Code 2^3 2^2 2^1 2^0	Display AY-5-8300	Display AY-5-8302, AY-5-8320	Display AY-3-8310
0 0 0 0	0	1	0 0*
0 0 0 1	1	2	1 1
0 0 1 0	2	3	2 2
0 0 1 1	3	4	3 3
0 1 0 0	4	5	4 4
0 1 0 1	5	6	5 5
0 1 1 0	6	7	6 6
0 1 1 1	7	8	7 7
1 0 0 0	8	9	8 8
1 0 0 1	9	10	9 9
1 0 1 0	10	11	10 —
1 0 1 1	11	12	11 —
1 1 0 0	12	13	12 —
1 1 0 1	13	14	13 —
1 1 1 0	14	15	14 —
1 1 1 1	15	16	15 —

*00-99 MODE.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin . . . . +0.3 to −20V
Ambient Operating temperature range . . . . . 0°C to +85°C
Storage temperature range. . . . . −65°C to +150°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these condtions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{GG} = 0V
V_{SS} = +16V to +19V
Operating Temperature (T_A) = 0°C to +85°C
Clock Frequency = 1.1 MHz ±10%

Characteristic	Min	Typ**	Max	Units	Conditions
Vertical Sync Input (Note 1)					
Logic '0'	0	—	7	Volts	
Logic '1'	V_{SS} −5	—	V_{SS} +0.5	Volts	
Rise & Fall Time	—	—	5	μs	10% to 90% Min slew rate 5V/μsec
Horizontal Sync Input					
Logic '0'	0	—	7	Volts	
Logic '1'	V_{SS} −1.5	—	V_{SS} +0.3	Volts	
Rise & Fall Time	—	—	1	μs	10% to 90%
1.1MHz Clock Input					
Logic '0'	0	—	7	Volts	
Logic '1'	V_{SS} −5	—	V_{SS} +0.3	Volts	
Rise & Fall Time		—	300	ns	10% to 90%
Pulse width	250	—		ns	at logic 0 and logic 1 levels
Channel Inputs (Note 1)					
Logic '0'	0	—	7	Volts	
Logic '1'	V_{SS} −5	—	V_{SS} +0.5	Volts	
Clock Inputs, Multiplex, Strobe Inputs					
Logic '0'	0	—	7	Volts	
Logic '1'	V_{SS} −1.5	—	V_{SS} +0.3	Volts	
Input Resistance	—	20	—	Kohm	To V_{GG}
Display Enable Inputs					
Switch point positive edge	V_{SS} −8	—	V_{SS} −5	Volts	
Outputs					
On resistance	—	—	1	Kohm	V_{OUT} = V_{SS} −2V
Off leakage	—	—	1	μA	V_{OUT} = 0V
Turn ON time	—	—	200	μs	10-90% load 25K & 20pF to ground
Power	—	—	400	mW	V_{SS} = +19V

**Typical values are at +25°C and nominal voltages.

NOTE:
1. These inputs are diode clamped to V_{SS}. Maximum clamp current 50μA.

TIMING DIAGRAMS

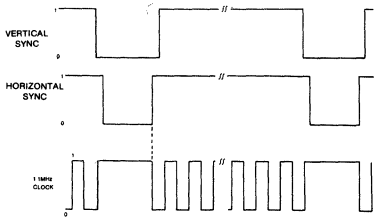


Fig.1 INPUT WAVEFORMS

TIMING DIAGRAMS

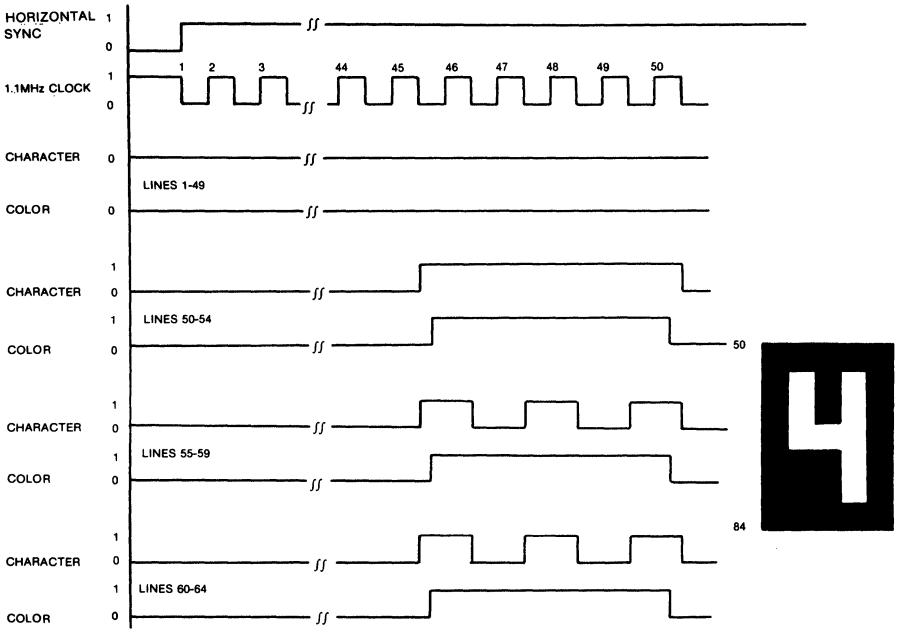


Fig.2a OUTPUT WAVEFORMS (AY-5-8300/8310)
COLOR CHARACTER ON A BLACK BACKGROUND

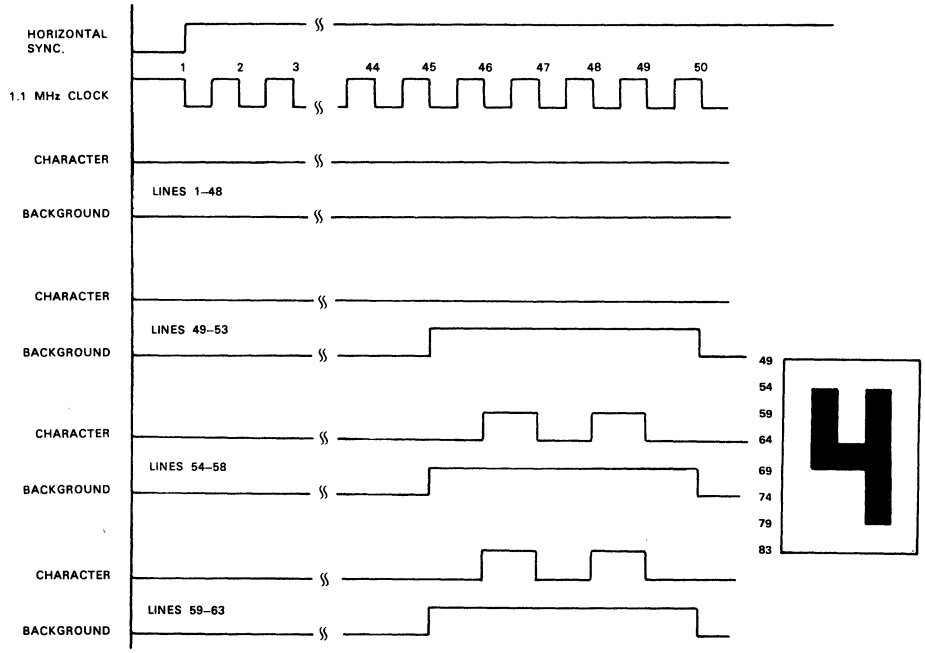


Fig.2b OUTPUT WAVEFORMS (AY-5-8302/8320)
COLOR CHARACTER ON A COLOR BACKGROUND

OPERATION

The display is positioned digitally in both the vertical and horizontal directions. The vertical position is determined by counting horizontal sync pulses (the counting is initiated by the vertical sync pulse). The timing relationships are shown in Figs. 2a and 2b. Additionally, for the AY-5-8320, the time display is positioned 35 lines further down so that it appears immediately below the channel display.

In the horizontal direction the display is positioned by counting pulses from an external 1.1 MHz oscillator which is synchronized with the horizontal sync pulse to prevent ragged edges on each character.

Each character is made up of 15 dots in a 3×5 matrix. With a one dot border around each character a total matrix of 35 dots in a 5×7 format is utilized. Each dot lasts 0.9usec in the horizontal direction and is 5 lines high. This gives a rectangular dot and characters as shown in Figs. 3a and 3b.

The various channel/time display formats are illustrated in Figs. 4, 6 and 7. The display positioning on the TV screen is shown in Figs. 8a and 8b.

In the AY-5-8300 and AY-5-8310, the character display is controlled by two outputs, Character and Color. The video channels are controlled in the following manner:

(a) Black/white display

Character	Color	
0	0	Normal picture
1	0	Black (luminance channel full off)
1	1	Black
0	1	White

(b) Black/Yellow display

Character	Color	Normal picture
1	0	Black (luminance full off)
1	1	Black (luminance full off and blue suppressed)
0	1	Yellow (luminance full on and blue suppressed)

Other color displays are generated by suppressing one or two chrominance channels.

In the AY-5-8302 and AY-5-8320, one video output defines the characters and the other a background block. Using these outputs, a display of any color character on a background of any color may be obtained.

The channel data is input on four lines; in the 0—15 or 1—16 channel mode, this information is applied in binary from a diode encoder attached to the varactor tuning drivers. Binary numbers greater than 9 are detected and displayed as a two digit character.

In the clock mode, data is entered on a 4 line BCD bus multiplexed into 4 time slots. A strobe signal occurring in the middle of each time slot is used to read the data into the chip. When the AY-5-1203A clock is used it can be directly connected to the AY-5-8310 or AY-5-8320 with no external components. The AY-5-8310 displays the time with hours and minutes (Fig.6); the AY-5-8320 displays the time with hours, minutes and a flashing colon for seconds (Fig.7).

In the 00-99 channel mode the data is entered as a two digit BCD number in Multiplex time slots 1 and 2 in the same manner as the clock formation.

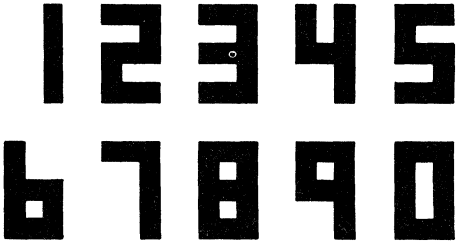


Fig.3a CHARACTER SET (AY-5-8300/8310)

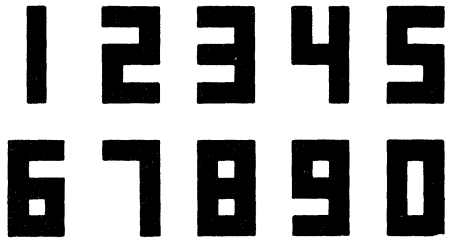


Fig.3b CHARACTER SET (AY-5-8302/8320)

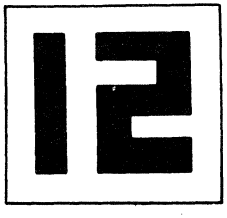


Fig.4 CHANNEL DISPLAY

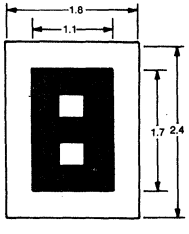


Fig.5 CHARACTER SIZE (25/26 INCH SCREEN)

Fig.6 TIME DISPLAY (AY-5-8310)

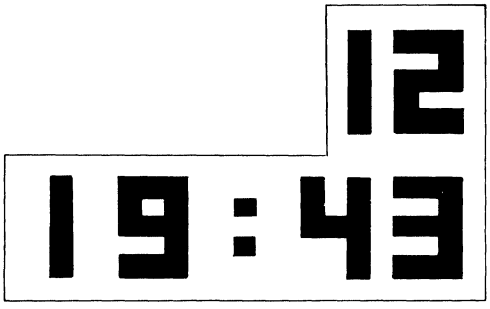


Fig.7 TIME AND CHANNEL DISPLAY (AY-5-8320)

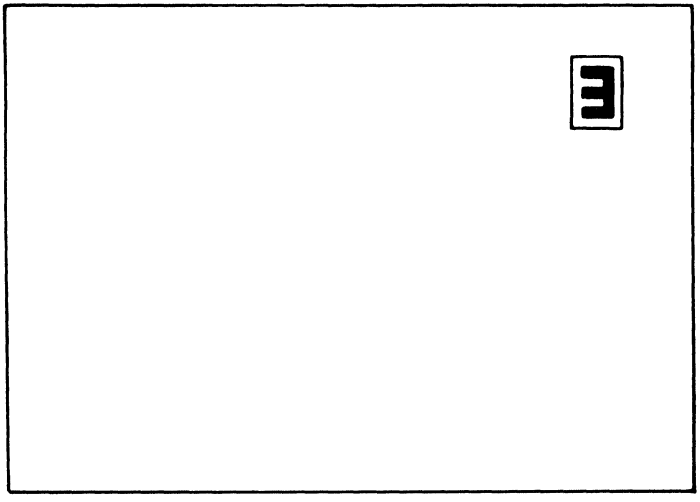


Fig.8a DISPLAY POSITION—CHANNEL (AY-5-8300/8302/8310) OR TIME (AY-5-8310)

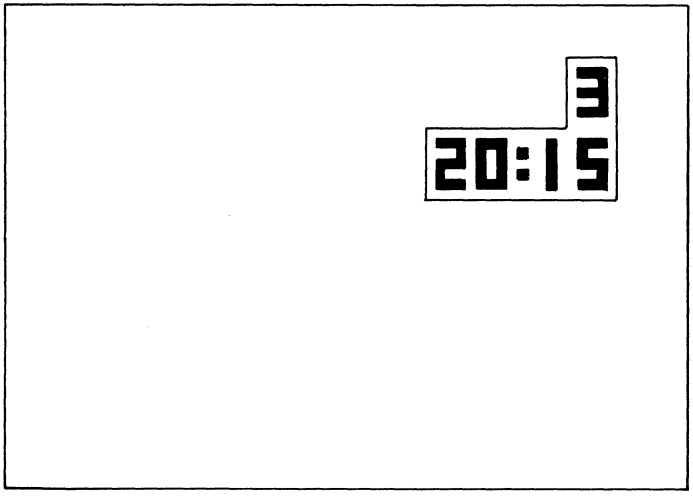


Fig.8b DISPLAY POSITION—SIMULTANEOUS CHANNEL AND TIME (AY-5-8320)

Ultrasonic Remote Control Transmitter

FEATURES

- 23 channels of information
- Direct drive for 40KHz transducer
- Power consumption only during keying of information.
- AY-5-8410 — local control at receiver
  AY-5-8411 — remote control operates on 9V battery
- Keyboard bounce protection built in.
- No external oscillator is required.
- Local transmitter wire-OR'ed to receiver

DESCRIPTION

The AY-5-8410/8411 transmitter provides the electronics to transmit 23 channels of information. The transmission is in pulse code modulated form. The transmitter will drive a 40KHz transducer either directly or via a step-up transformer. When any key is depressed battery power is applied to the chip, power is removed at the end of the code sequence following the release of the key. The requirement for a separate on/off switch is avoided. The keyboard is an 8×3 matrix as shown below. Key bounce protection is incorporated. A stable on-chip oscillator is also provided.

If a local keyboard is required an additional transmitter chip can be used to encode the local keyboard and the chip output can be wire-OR'ed with the output from the receiver transducer amplifier before being fed to the receiver chip.

ELECTRICAL CHARACTERISTICS

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
V_{DD} = -9V Nominal (AY-5-8411)
-15V Nominal (AY-5-8410)
Operating Temperature (T_A)= -20°C to +70°C

Characteristic	Min	Typ*	Max	Units	Conditions
Inputs					
Clock					
Output polarity					
Key lines 1-8					
Logic 0	+0.3	—	-1	Volts	
Logic 1	-3	—	-15	Volts	
Outputs					
Strobes S1,S2,S3	—	2.5	—	Kohms	Output at -7V
Ultrasonic output	—	100	—	ohms	
standby mode	—	6	—	μA	
transmitting mode	—	2	—	mA	Chip alone

*Typical values are at +25°C and nominal voltages.

TRANSMITTER KEY MATRIX

Key Strobe / Input Line	S 2	S 3	S 1
0	Ch 24	16	16
1	9	17	25
2	10	18	26
3	11	19	27
4	12	20	28
5	13	21	29
6	14	22	30
7	15	23	31

PIN FUNCTIONS

Key Lines S1, S2, S3

These key lines form part of the key matrix as shown above and are strobe signals which each go low in sequence.

Key Inputs K1-K8

Those key lines form part of the key matrix as shown above and they are connected to strobe lines S1, S2 or S3 when appropriate keys are depressed.

Ultrasonic Outputs

The ultrasonic output is a tri state push pull output which goes to logic 1 between trains of pulse in a data block.

A transducer or step up transformer can be connected between the ultrasonic output and V_{DD}.

When using the transmitter to encode a local keyboard, the output polarity pin should be connected to V_{DD}. This inverts the polarity of the ultrasonic output and enables the transmitter output to be wire-OR'ed with an output from an ultrasonic receiver transducer amplifier, before being fed to an ultrasonic receiver.

Output Polarity

The polarity of the output is controlled by the output polarity pin. With the pin linked to 0 volts the transmitter can be wire-OR'ed with a receiver transducer amplifier.

With the pin linked to V_{DD} the transmitter output will drive a transducer or step up transformer.

ØR and ØL

These are the oscillator input pins. The chip frequency is not critical except in so far as is necessary to satisfy the requirements of the ultrasonic transducers.

The chip may be driven from an external clock by connecting the clock to both ØR and ØL linked together.

Ov or V_{SS}

Ov or positive supply

V_{DD}

Negative supply nominally 9 volts.

V_{pu}

This pin is concerned with automatic circuit start up and should be connected to V_{DD} by a 1M ohms resistor.

Ultrasonic Remote Control Receiver

FEATURES

- 63 channels of information
- On board oscillator — external oscillator optional
- Automatic power on clear
- Local control from wire-OR of transmitter
- Error detection is contained
- Output provided to show information being received

DESCRIPTION

The AY-5-8420 provides the electronics to produce an ultrasonic remote control receiver which with an appropriate transmitter can accept up to 63 channels of information. An on chip oscillator is provided the frequency of which is non-critical (≈66KHz.) The oscillator frequency is set by one external resistor, an external oscillator can be used if required. Two outputs are provided to indicate that data has been received and is ready for use. Automatic internal power-on-clear is provided.

Error checking bits are transmitted with the code, these are interrogated by the receiver and prevent it from accepting incorrect data caused by attenuation, reflection or multiple path propogation effects. If the first received block of data is not accepted due to introduced errors the receiver logic resets and attempts to accept the next block. Data blocks are repeatedly transmitted whenever the transmitter is keyed.

ELECTRICAL CHARACTERISTICS

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
V_{DD} = -15V nominal
Operating Temperature (T_A) = -20°C to +70°C

Characteristic	Min	Typ*	Max	Units	Conditions
Inputs					
Clock					
Ultrasonic					
5/6					
Logic 0	+0.3	—	-1	Volts	
Logic 1	-3	—	-15	Volts	
Outputs					
A-F					
LED					
STROBE					
Logic 0 sink current	—	2	—	mA	2V drop
Chip supply current	—	—	—	mA	
Oscillator frequency	—	66	—	KHz	

*Typical values are at +25° C and nominal voltages.

PIN FUNCTIONS

Ov
0 volt or positive supply.

V_{DD}
Negative supply 15V nominal.

Clock inputs ØR, ØL
The clock frequency is determined by the value of resistor connected between ØR and ØL.

ØR and ØL may be connected together and overdriven by an external clock input.

Ultrasonic Input
The ultrasonic input should be driven from an amplifier output stage. The receiver is insensitive to input frequency except in so far as is necessary to satisfy the requirements of the ultrasonic transducers.

A local keyboard input can be wire-OR'ed. The frequency is set to approximately 66 KHz with a single resistor.

5/6 Control
This pin alters the function of the receiver to enable it to accept data from either a 5 bit or 6 bit transmitter. With the pin not connected the receiver functions in 5 bit mode. With the pin connected to 0 v the receiver functions in 6 bit mode.

Outputs 1,2,4,8,16,32
The six outputs 1,2,4,8,16,32 are latching outputs which retain the data until it is replaced by new input data. The outputs are open ended and clamp to 0 volts with no output data present.

The output codes change state midway through the end code following correct reception of a data block.

Power-on-clear sets the outputs to an all ones state when power is first applied.

LED
This signal can be used to drive an indicator to show that new data has been received.

The LED output is normally at 0 vol and goes open circuit simultaneous with the outputs changing. The signal remains in this state during the time that the transmitter is keyed and the receiver is receiving input signals. The signal goes to 0 volts 32 m.sec after the input signals cease.

By gating the LED output with a discrete decode of the outputs 1,2,4,8,16,32 a signal is obtained to drive an analog function i.e. volume up. Such a signal would be present only during the time that the transmitter was keyed.

Strobe
The strobe output is open ended and clamps to 0 volts.

The clamp is released 60 μ.sec after the data on outputs 1,2,4,8,16,32 has changed and is re-applied 60 μ.sec later.

TV Games

FEATURES

- 6 Selectable Games - Tennis, hockey/soccer, squash, pelota and two rifle shooting games.
- 625 Line (AY-3-8500) and 525 Line (AY-3-8500-1) versions.
- Automatic Scoring
- Score display on T.V. Screen, 0 to 15.
- Selectable Bat Size
- Selectable Angles
- Selectable Ball Speed
- Automatic or Manual Ball Service
- Realism Sounds
- Shooting Forwards in Hockey Game
- Visually defined area for all Ball Games.

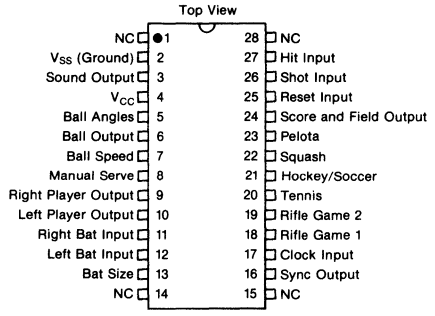
DESCRIPTION

The AY-3-8500 and AY-3-8500-1 circuits have been designed to provide a TV 'games' function which gives active entertainment using a standard domestic television receiver.

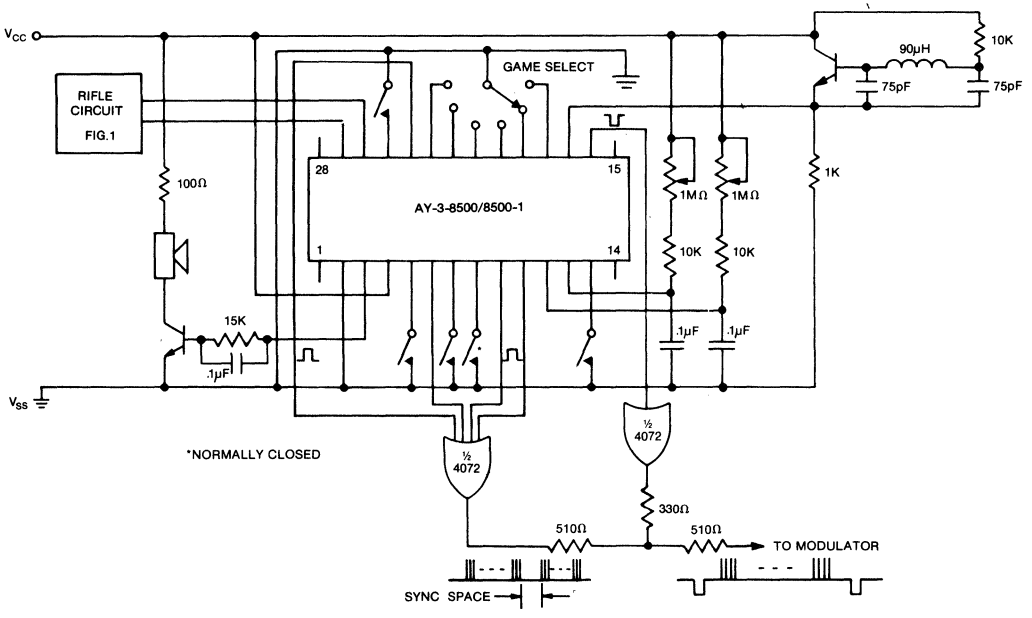
The circuit is intended to be battery powered and a minimum number of external components are required to complete the system. A block diagram is shown below.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



SYSTEM BLOCK DIAGRAM



PIN FUNCTIONS

Left Bat Input
Right Bat Input
An R-C network connected to each of these inputs controls the vertical position of the bats. Use a 10K resistor in series with each pot.

Reset
This input is connected momentarily to V_{SS} (Logic '0') to reset the score counter and start a game.

Bat Size
This input is left open circuit (Logic '1') to select small bats and connected to V_{SS} (Logic '0') to select large bats. For a 19" T.V. Screen large bats are 1.9" and small bats are 0.95" high.

Ball Angles
This input is left open circuit (Logic '1') to select two rebound angles and connected to V_{SS} (Logic '0') to select four rebound angles. When two angles are selected they are ±20°, when four are selected they are ±20° and ±40°.

Ball Speed
When this input is left open-circuit, low speed is selected (1.3 seconds for ball to traverse the screen). When connected to V_{SS} (Logic '0'), the high speed option is selected (0.65 seconds for ball to traverse the screen).

Tennis, Hockey/Soccer, Squash, Pelota, Rifle Game 1 and Rifle Game 2
These inputs are normally left open circuit (Logic '1') and are connected to V_{SS} (Logic '0') to select the desired game.

Manual Serve
This input is connected to V_{SS} (Logic '0') for automatic serving. When left open circuit (Logic '1') the game stops after each score. The serve is indicated by momentarily connecting the input to V_{SS}.

Shot Input
This input is connected to V_{SS} when the Rifle Trigger is pulled.

Hit Input
If this input is at V_{SS} when the Rifle trigger is pulled a hit is recorded.

Sound Output
The hit (32ms pulse/976Hz tone), boundary reflection (32ms pulse/488Hz tone) and score (160ms pulse/1.95KHz tone) tones are output on this pin.

Sync Output
The T.V. vertical and horizontal sync signals are output on this pin.

Ball Output
The ball video signal is output on this pin thus allowing the brightness of the ball to be adjusted relative to the rest of the picture.

Score and Field Output
The video signals are output on this pin.

Left Player Output/Right Player Output
The left and right players are output on separate pins.

Note: The "Shot" and "Hit" inputs have on-chip pull-down resistors to V_{SS}. All other inputs (except the "Bat" inputs) have on-chip pull-up resistors to V_{CC}.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin . . . . . −0.3 to +12V
Storage Temperature Range . . . . . −55°C to +150°C
Ambient Operating Temperature Range . . . . . 0°C to +50°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +7 to +9.5V (AY-3-8500)
V_{CC} = +6 to +9.5V (AY-3-8500-A/AY-3-8500-1A)
V_{CC} = +6 to +8.5V (AY-3-8500-B/AY-3-8500-1B)
V_{CC} = +6 to +7.5V (AY-3-8500-C/AY-3-8500-1C)

V_{SS} = 0V
Operating Temperature (T_A) = 0°C to +50°C
F Clock = 2.01MHz ±1%

Characteristic at 25°C and V_{CC} = 9 Volts	Min	Typ**	Max	Units	Conditions
Clock Input	—		—		Maximum clock source impedance
Frequency	—	2.01	—	MHz	of 1K to V_{CC} or V_{SS}.
Logic '0'	—	0.5	—	Volts	
Logic '1'	—	V_{CC}—1.0	—	Volts	
Pulse Width —Pos.	—	200	—	ns	
Pulse Width — Neg.	—	300	—	ns	
Capacitance	—	10	—	pF	V_{IN} = OV, F = 1MHz
Leakage	—	100	—	μA	V_{IN} = +9.5V
Control Inputs					Maximum contact resistance of 1K
Logic '0'	—	0.5	—	Volts	to V_{SS}.
Logic '1'	—	V_{CC}—1.0	—	Volts	Inputs have 100KΩ pull up to V_{CC}
Input Impedance	—	1.0	—	M Ohms	Pull up to V_{CC}
Rifle Input	—	1.0	—	M Ohms	Pull down to V_{SS}
Outputs					
Sync. Logic '0'	—	1.0	—	Volt	I out = 0.5mA
Logic '1'	—	V_{CC}—2.0	—	Volts	I out = 50μA
Ball. Logic '0'	—	1.0	—	Volt	I out = 0.5mA
Logic '1'	—	V_{CC}—2.0	—	Volts	I out = 50μA
Sound					
Logic '0'	—	1.0	—	Volts	I out = 0.5mA
Logic '1'	—	V_{CC}—2.0	—	Volts	I out = 50 μA
Power Supply Current	—	24	—	mA	

**Typical values are at +25°C and nominal voltages.

OPERATION

1) Tennis

With the tennis game the picture on the television screen would be similar to Figure 2 with one 'bat' per side, a top and bottom boundary and a center net, the individual scores are counted and displayed automatically in the position shown. The detail of the game will depend upon the selection of the options. Considering the situation where small bats are used and all angles, after the reset has been applied, the scores will be 0, 0 and the ball will serve arbitrarily to one side at one of the angles. If the ball hits the top or bottom boundary it will assume the angle of reflection and continue in play. The player being served must control his bat to intersect the path of the ball. When a 'hit' is detected by the logic, the section of the bat which made the hit is used to determine the new angle of the ball.

To expand on this, all 'bats' or 'players' are divided logically into four adjacent sections of equal length. When using the four angle option it is the quarter of bat which actually hits which defines the new direction for the ball.

The direction does not depend upon the previous angle of incidence. With the two angle option the top and bottom pairs of the bats are summed together and only the two shallower angles are used to program the new direction for the ball.

The ball will then traverse towards the other player, reflecting from the top or bottom as necessary until the other player makes their 'hit'. This action is repeated until one player misses the ball. The circuitry then detects a 'score' and automatically increments the correct score counter and updates the score display. The ball will then serve automatically from the center line towards the side which had just missed. This sequence is repeated until a score of 15 is reached by one side, whereupon the game is stopped. The ball will still bounce around but no further 'hits' or 'scores' can be made. While the game is in progress, three audio tones are output by the circuit to indicate top and bottom reflections, bat hits and scores.

2) Hockey/Soccer

The 'hockey' type game is shown in Figure 3, and with this game each participant has a 'goalkeeper' and a 'forward'. The layout is such that the 'goalkeeper' is in his normal position and the 'forward' is positioned in the opponent's half of the playing area.

When the game starts, the ball will appear travelling from one goal line towards the other side. If the opponent's forward can intercept the ball, (Figure 3a), he can 'shoot' it back towards the goal. If the ball is missed it will travel to the other half of the playing area and the first team's forward will have the opportunity of intercepting the ball and redirecting it forward at a new angle according to the 'player' section which is used, (Figure 3b). If the ball is 'saved' by the 'goalkeeper' or it reflects back from the end boundary, the same forward will have the opportunity to intercept the outcoming ball and divert it back towards the 'goal.

A 'score' is made in the 'hockey' game by 'shooting' the ball through the defined goal area. The scoring and game control is done automatically as for the tennis game. The same audio signals are used to add atmosphere to the game.

3) Squash

This game is illustrated in Fig.4. There are two players who alternately hit the ball into the court. The right hand player is the one that hits first, it is then the left hand player's turn. Each player is enabled alternately to insure that the proper sequence of play is followed.

4) Pelota

This game is similar to squash except that there is only one player.

5) Rifle Shooting

This game is illustrated in Fig.5. It has a large target which bounces randomly about the screen, a photocell in the rifle is aimed at the target. When the trigger is pulled the shot counter is incremented, if the rifle is on target the hit counter is incremented, a hit noise is generated and the target is blanked for a while. After 15 shots the score appears but the game can still continue.

6) Rifle Game No. 2

In this game the ball traverses the screen from left to right under control of the manual serve button. Otherwise the game is as above.

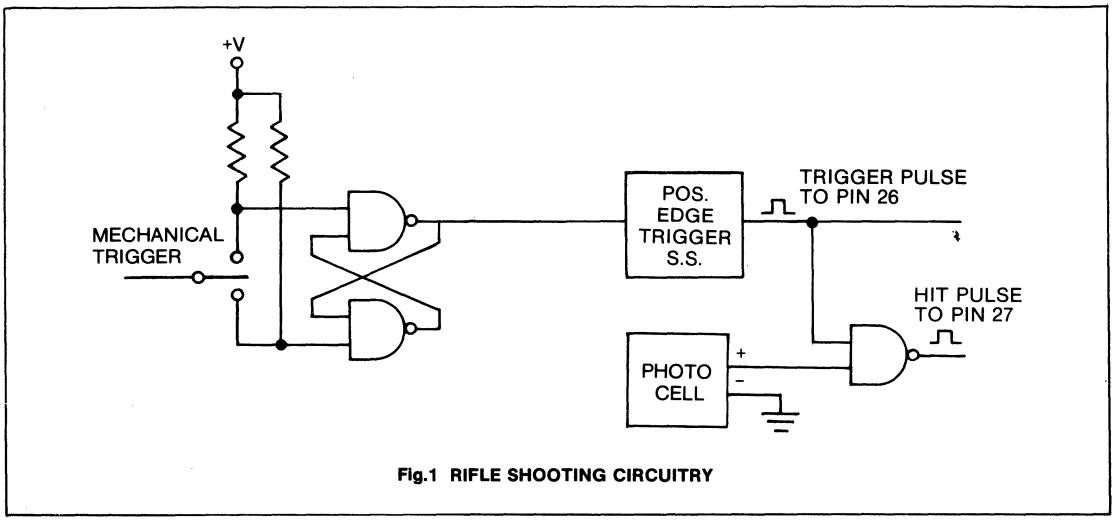


Fig.1 RIFLE SHOOTING CIRCUITRY

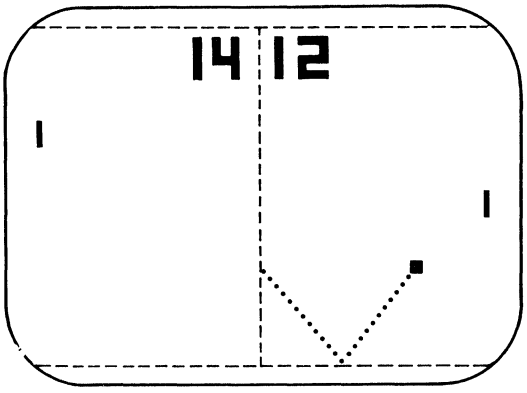


Fig.2 TENNIS GAME

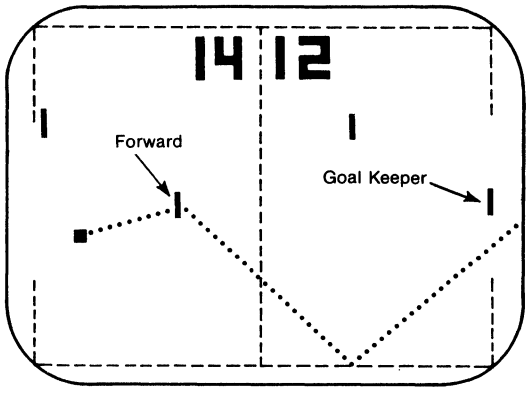


Fig.3 HOCKEY GAME

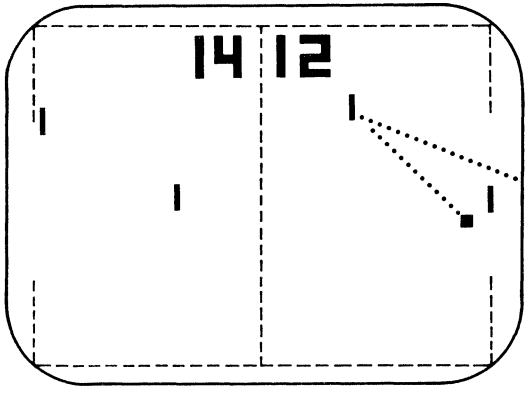


Fig.3a RETURN OF 'GOAL SAVE'

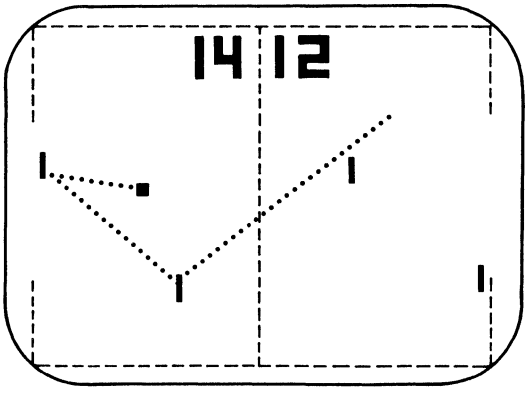


Fig.3b 'SHOOTING' FORWARD

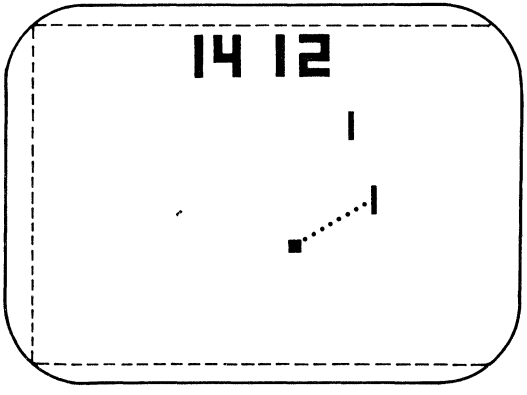


Fig.4 SQUASH

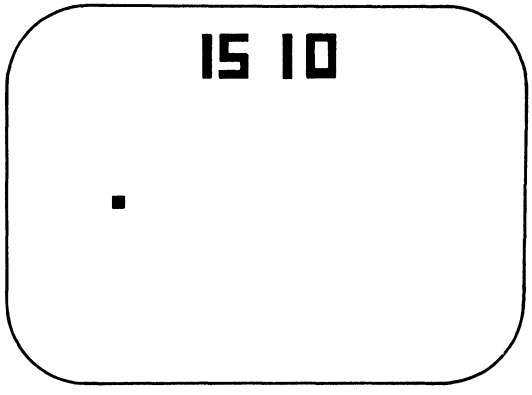


Fig.5 RIFLE SHOOT

GENERAL INSTRUMENT

AY-1-0212
AY-1-0212A
AY-3-0214
AY-3-0215
AY-3-0216
AY-1-1006
AY-1-2006
AY-1-1007B
AY-1-1313
AY-5-1315
AY-5-1317A
AY-1-5050
AY-1-5051
AY-1-6721/5
AY-1-6721/6

5

Master Frequency Generator/Top Octave Generator

FEATURES

- Wide Input Frequency Range:
  1) AY-1-0212—250KHz to 1.5MHz
  2) AY-1-0212A—250KHz to 2.5MHz
- Low Impedance Push-Pull Outputs
- Full Musical Scale in One Chip
- Zener Protected Input

DESCRIPTION

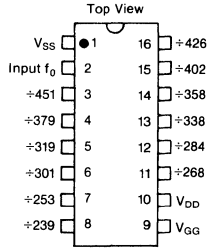
The Master Frequency Generator/Top Octave Generator is a digital tone generator which produces, from a single input frequency, a full octave of twelve frequencies on twelve separate output terminals.

The M.F.G./T.O.G. consists of twelve divider circuits which divide the input by an exact integer to produce a chromatic scale of twelve notes. When used in conjunction with an oscillator and frequency dividers, a system may be configured which generates all the frequencies required by an electronic music synthesizer.

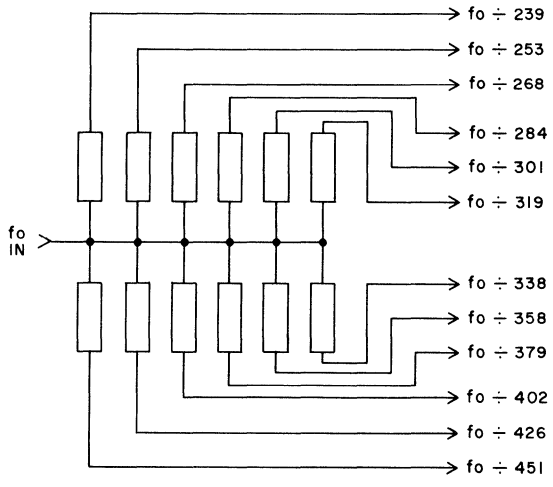
The AY-1-0212 operates with input frequencies of up to 1.5MHz. A premium device designated AY-1-0212A operates up to 2.5MHz.

PIN CONFIGURATION

16 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All Pin Voltages with respect to Vss .....-30V to +0.3V
Storage Temperature .....-55°C to +150°C
Operating Temperature (T_A) .....0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)
V_{SS} = GND
See Fig.1 for V_{DD} and V_{GG} Operating Voltages

Characteristic	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS					
Input Leakage	—	—	10	μA	at 27V
Input Positive Level	+0.3	—	−2.0	Volts	
Input Negative Level	−10.0	—	V_{DD}	Volts	
Output on Impedance to V_{DD}	—	—	3500	Ohms	
Output on Impedance to V_{SS}	—	—	3500	Ohms	See Note 1
I_{GG} Supply Current	—	—	16	mA	
I_{DD} Supply Current	—	—	20	mA	
AC CHARACTERISTICS					
AY-1-0212 Input Frequency f_o	.25	—	1.5	MHz	See Fig.3
AY-1-0212A Input Frequency f_o	.25	—	2.5	MHz	
Input Capacitance	—	5	10	pF	1 MHz
Input Positive Level Width t_p	.33	—	—	μs	AY-1-0212
Input Negative Level Width t_n	.33	—	—	μs	AY-1-0212
Input Positive Level Width t_p	.2	—	—	μs	AY-1-0212A
Input Negative Level Width t_n	.2	—	—	μs	AY-1-0212A
Output Rise Time t_r	—	1	—	μs	no load
Output Fall Time t_f	—	1	—	μs	no load

** Typical values are at +25°C and nominal voltages.

NOTE:
1. Output impedance measurements are made with 1.0V across the device to be measured with 17K Ohm load to −6V.

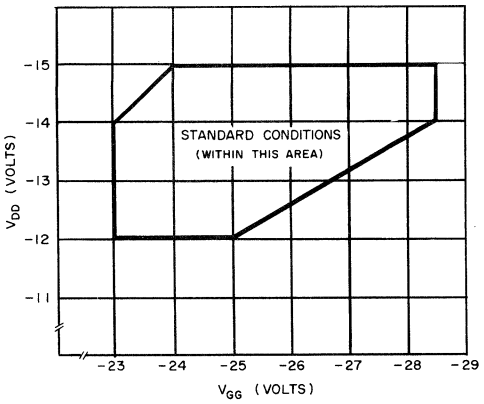


Fig.1 OPERATING VOLTAGES

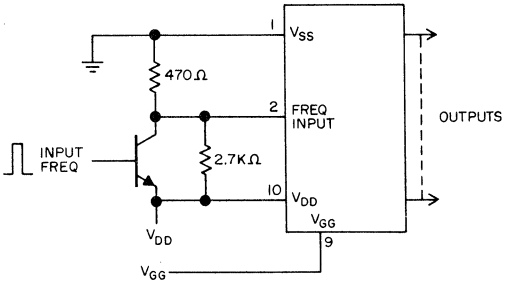


Fig.2 TYPICAL INPUT BUFFER (IF REQUIRED)

TYPICAL CHARACTERISTIC CURVE

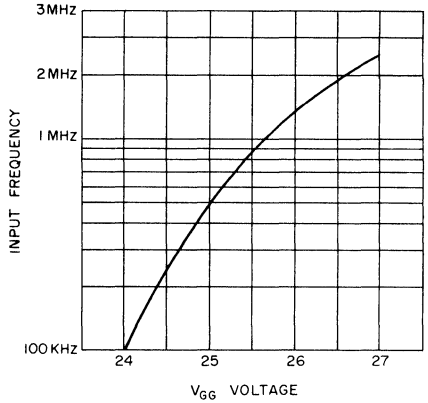
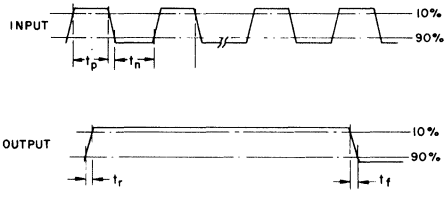
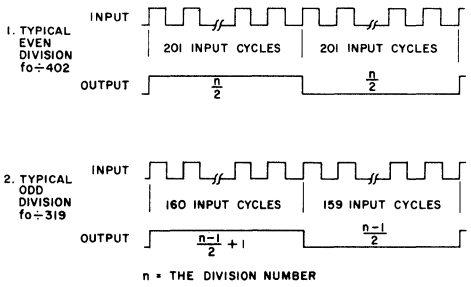


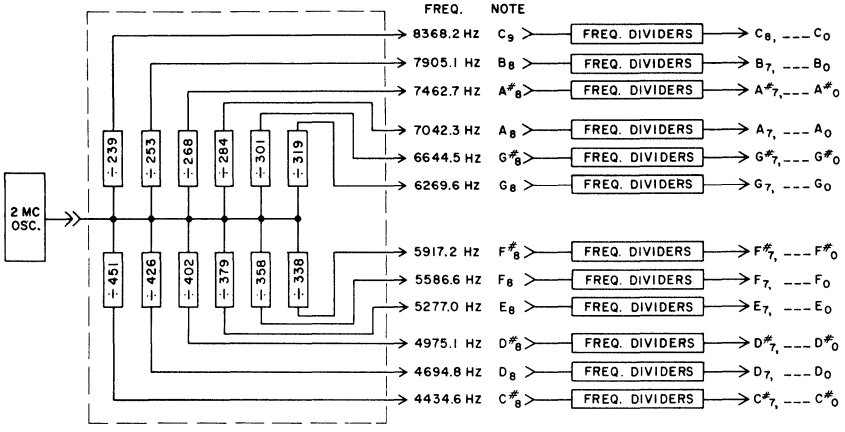
Fig.3 TYPICAL FREQUENCY VS. V_{GG} VOLTAGE OPERATION

TIMING DIAGRAMS





TYPICAL APPLICATION



Master Frequency Generator/Top Octave Generator

FEATURES

- Wide input frequency range: 100 KHz to 4.5 MHz
- Single power supply
- Full musical scale on one chip
- Low impedance push-pull outputs
- Zener protected input.
- AY-3-0214: 12 outputs — 50% Duty Cycle (Highest accuracy)
- AY-3-0215: 13 outputs — 50% Duty Cycle
- AY-3-0216: 13 outputs — 30% Duty Cycle

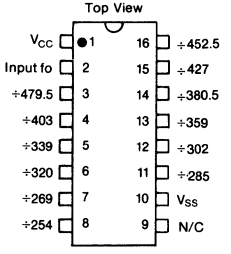
DESCRIPTION

The General Instrument M.F.G./T.O.G. is a digital tone generator which produces, from a single input frequency, 12 or 13 semitone outputs fully spanning the equal tempered scale. When used in conjunction with an oscillator and frequency dividers such as the G.I. AY-1-1007B, a system maybe configured which generates all the frequencies required by an electronic music synthesizer.

PIN CONFIGURATION

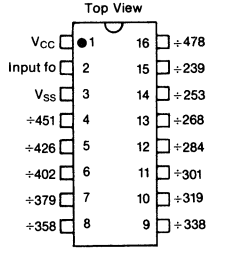
16 LEAD DUAL IN LINE

AY-3-0214

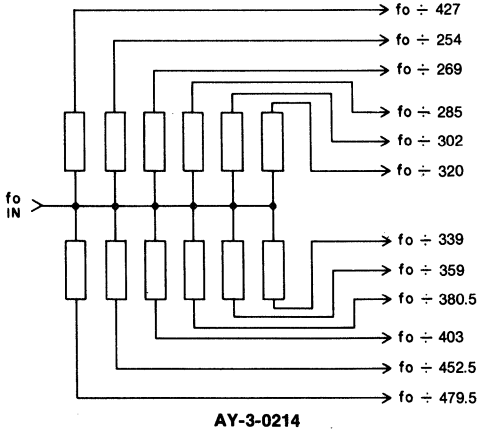


16 LEAD DUAL IN LINE

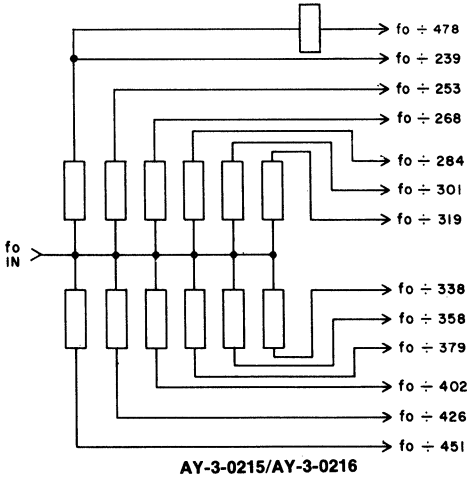
AY-3-0215/AY-3-0216



BLOCK DIAGRAMS



AY-3-0214



AY-3-0215/AY-3-0216

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... +20 to -0.3
Storage Temperature .....-55°C to +150°C
Operating Temperature (T_A) .....0°C to +50°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

0°C ≤ TA ≤ 50°C
V_{SS} = 0.0V
V_{CC} = +10V to +16V

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Input					
Low	0.0	—	0.8	V	
High	V_{CC} −3.0	V_{CC}	V_{CC}	V	
Frequency	100	—	4500	KHz	
Rise Time	—	—	30	ns	4.5 MHz
Fall Time	—	—	30	ns	4.5 MHz
Duty Cycle	40	50	60	%	
Capacitance	—	—	10	pf	
Outputs					
High	V_{CC} −1.5	—	V_{CC}	V	0.25 mA
Low	0.0	—	0.5	V	0.7 mA
Fall Time	—	—	2.5	μs	20K & 500 pf to 16V
Rise Time	—	—	2.5	μs	20K & 500 pf to V_{SS} when V_{CC} = 16V
Duty Cycle	—	50	—	%	AY-3-0214/5
	—	30	—	%	AY-3-0216
Supply current	—	—	120	mA	16V, 4.5 MHz, 25°C

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS

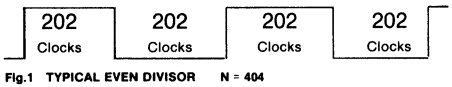


Fig.1 TYPICAL EVEN DIVISOR N = 404

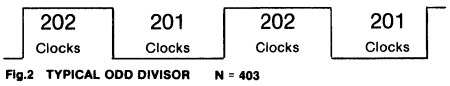


Fig.2 TYPICAL ODD DIVISOR N = 403

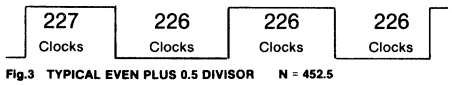


Fig.3 TYPICAL EVEN PLUS 0.5 DIVISOR N = 452.5

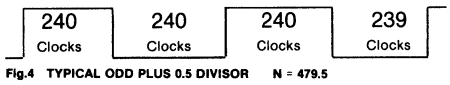
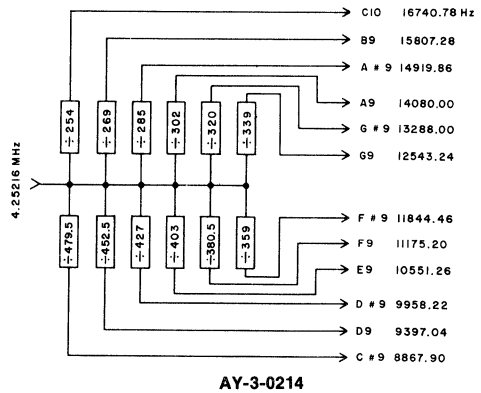
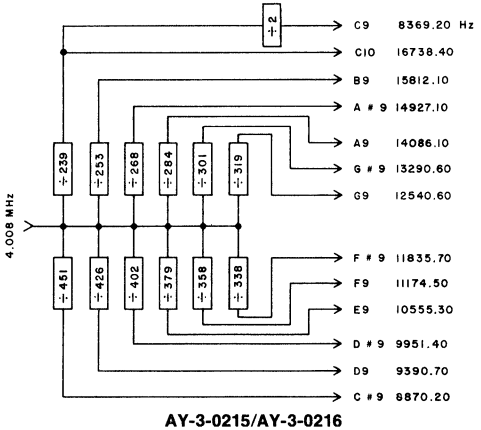


Fig.4 TYPICAL ODD PLUS 0.5 DIVISOR N = 479.5

TYPICAL APPLICATIONS



AY-3-0214



AY-3-0215/AY-3-0216

Six Stage Frequency Dividers

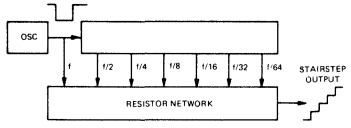
FEATURES

- Sine or Square Wave Input
- Low Impedance Push-Pull Outputs
- Six Divider Stages:
  3-2-1 (AY-1-1006)
  2-2-1-1 (AY-1-2006)

DESCRIPTION

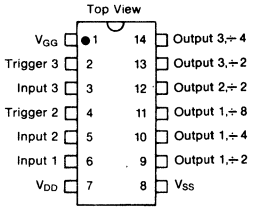
The AY-1-1006 and AY-1-2006 are monolithic frequency divider circuits which utilize MOS technology. Each consists of six flip-flops arranged either 3-2-1 (AY-1-1006) or 2-2-1-1 (AY-1-2006) and diffused into a single silicon substrate. Each circuit can be driven from a sine or square wave input. Each output is a low impedance push-pull output which is capable of driving external circuitry as well as other flip-flops.

APPLICATION

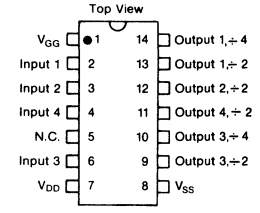


PIN CONFIGURATIONS

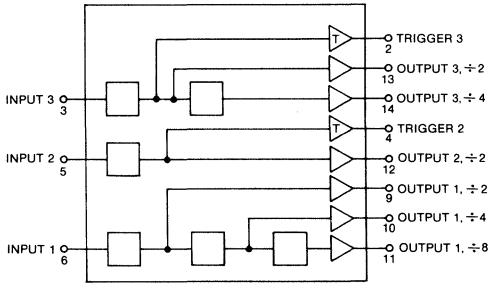
14 LEAD DUAL IN LINE
AY-1-1006



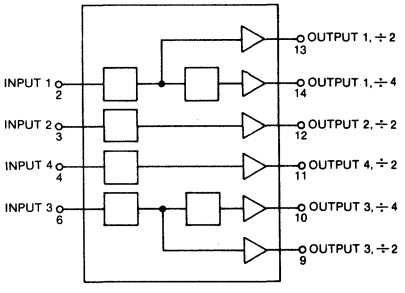
14 LEAD DUAL IN LINE
AY-1-2006



BLOCK DIAGRAMS



AY-1-1006



AY-1-2006

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All Pin Volages with respect to V_{SS} .....-30V to +0.3V
Storage Temperature .....-55°C to +150°C
Operating Temperature (T_A) .....0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

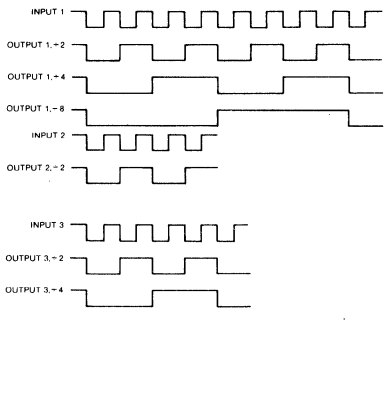
$-14 < V_{DD} < +0.3V$ $V_{GG} = -27 \pm 2V$ $V_{SS} = GND$

Characteristic	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS					
Input Leakage	—	—	1	μA	$V_{IN} = -20V$
Input Positive Level	—	—	−2.0	Volts	
Input Negative Level	−8.0	—	—	Volts	
Output Positive Level	—	—	−1.0	Volts	$V_{GG} = -27V$, $V_{DD} = -12V$
Output Negative Level	−10.0	—	—	Volts	$V_{GG} = -27V$, $V_{DD} = -12V$
I_{GG} Supply Current	—	—	10.0	mA	$V_{GG} = -28V$
D.C. Noise Immunity (Note 2)	+1.0	—	—	Volts	
AC CHARACTERISTICS					
Input Repetition Rate	D.C.	—	50	kHz	
Input Capacitance	—	—	5	pF	$V_{IN} = 0V$

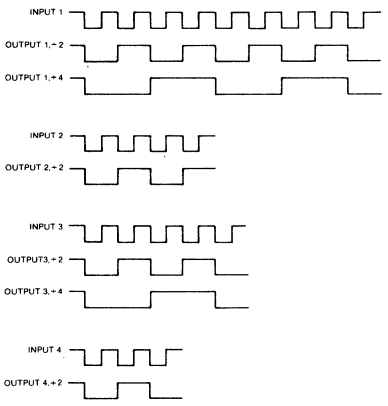
**Typical values are at +25°C and nominal voltages.

NOTES:
1. Outputs may be momentarily grounded (individually) without damage to the device.
2. D.C. noise immunity is definded as follows:
   "1" state N.I. = V_{OUT} "1" — V_{IN} "1" = [−10] −[−8] = 2V
   "0" state N.I. = V_{IN} "0" — V_{OUT} "0" = [−2] −[−1] = 1V
3. V_{DD} not used internally. Used for output negative supply only.
4. Outputs change on the negative transition of the respective inputs.

TIMING DIAGRAMS

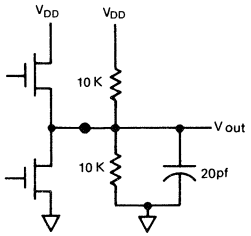


AY-1-1006

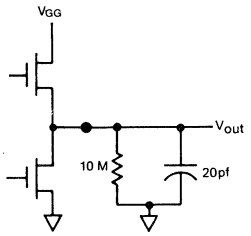


AY-1-2006

CIRCUIT TEST CONFIGURATIONS



BUFFER OUTPUT TEST LOAD



TRIGGER OUTPUT TEST LOAD

7-Stage Frequency Divider

FEATURES

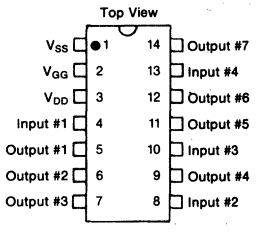
- Sine or Square Wave Input
- Low Inpedance Push-Pull Outputs
- Seven Divider Stages
- Power-On-Reset

DESCRIPTION

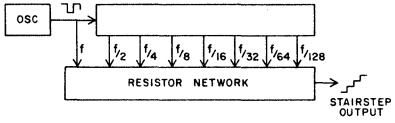
The AY-1-1007B is a monolithic frequency divider circuit which utilizes MOS technology. The divider circuit consists of seven flip-flops arranged in a 3-2-1-1 configuration and diffused into a single silicon substrate. The circuit can be driven from a sine or square wave input. Each flip-flop has a low impedance push-pull output which is capable of driving external circuitry as well as other flip-flops.

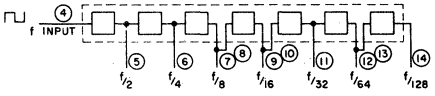
PIN CONFIGURATION

14 LEAD DUAL IN LINE

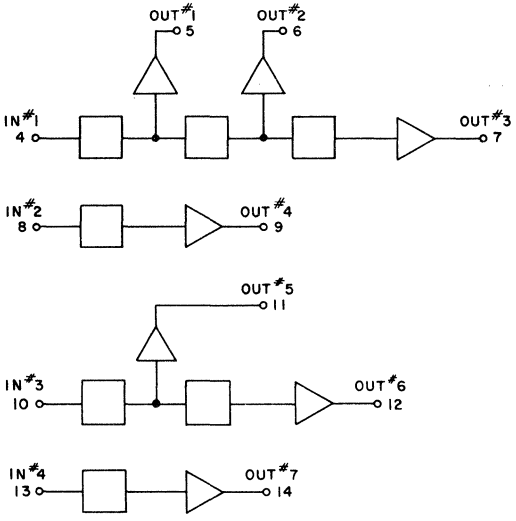


TYPICAL APPLICATIONS

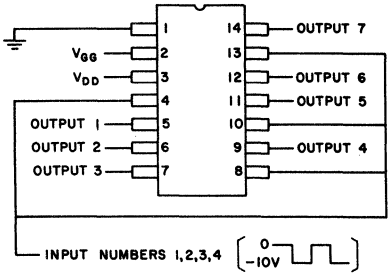




BLOCK DIAGRAM



CIRCUIT TEST CONFIGURATION



REFER TO TIMING DIAGRAM FOR OUTPUT PHASE AND FREQUENCY

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All Pin Voltages with respect to V_{SS} .....-30V to +0.3V
Storage Temperature .....-55°C to +150°C
Operating Temperature (T_A) .....0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

$-14 < V_{DD} < +0.3V$ $V_{GG} = -27V \pm 2V$ V_{SS} = GND

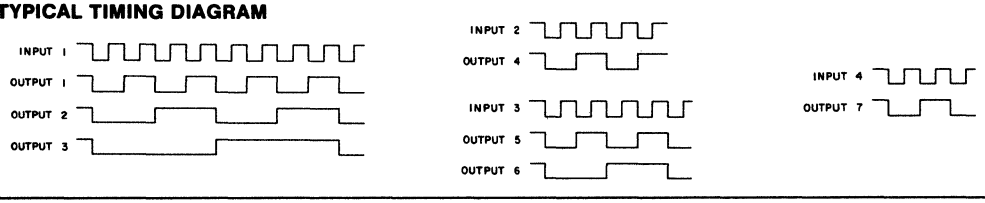
Characteristics	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS					
Input Leakage	—	—	1	μA	$V_{IN} = -20V$
Input Positivie Level	—	—	−2.0	Volts	
Input Negative Level	−9.0	—	—	Volts	
Output Positive Level	—	—	−1.0	Volts	$V_{GG} = -27V$, $V_{DD} = -12V$,
Output Negative Level	−11.0	—	—	Volts	$V_{GG} = -27V$, $V_{DD} = -12V$,
I_{GG} Supply Current	—	—	14.0	mA	$V_{GG} = -25V$,
D.C. Noise Immunity (Note 2)	+1.0	—	—	Volts	
AC CHARACTERISTICS					
Input Repetition Rate	D.C.	—	50	kHz	
Input Capacitance	—	—	5	pF	$V_{IN} = 0V$

**Typical values are at +25°C and nominal voltages.

Notes:

1. Outputs may be momentarily grounded (individually) without damage to the device.
2. D.C. noise immunity is defined as follows:
   "1" state N.I. = V_{OUT} "1" — V_{IN} "1" = [−10] −[−9] = 1V
   "0" state N.I. = V_{IN} "0" —V_{OUT} "0" = [−2] −[−1] = 1V
3. V_{DD} not used internally. Used for output negative supply only.
4. Typical output impedance to V_{SS} or V_{DD} is 1.2K ohms.

TYPICAL TIMING DIAGRAM



Priority Latching Network

FEATURES

- Low Power Consumption
- Two or more units may be connected in tandem

DESCRIPTION

The AY-1-1313 Priority Latching Network is a LSI subsystem designed for use in electronic organ keyboard and pedal latching circuits. When any combination of one or more "switch" inputs is connected to logic "1" the output switch corresponding to the highest priority, or lowest number, input will close, connecting the selected frequency to the output frequency bus. The output switch will remain closed even if the input switch is released, and will remain closed until a new input switch closure occurs.

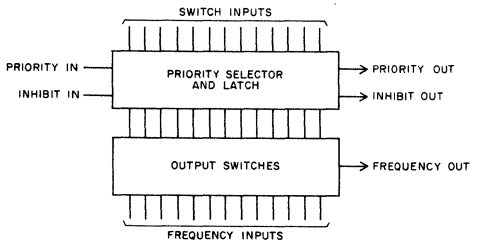
PIN CONFIGURATION

40 LEAD DUAL IN LINE

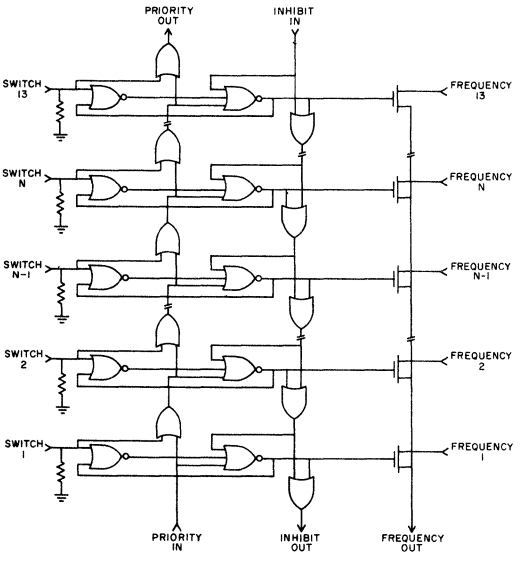
Top View

Switch 6	1	40	Switch 6
Switch 5	2	39	Switch 8
Switch 4	3	38	Switch 9
Switch 3	4	37	Switch 10
Switch 2	5	36	Switch 11
Switch 1	6	35	Switch 12
Ground	7	34	Switch 13
V_{DD}	8	33	N.C
Frequency Out	9	32	N.C
Priority IN	10	31	Priority Out
Inhibit Out	11	30	Inhibit In
N.C.	12	29	V_{GG}
N.C.	13	28	N.C.
N.C.	14	27	Frequency 13
Frequency 1	15	26	Frequency 12
Frequency 2	16	25	Frequency 11
Frequency 3	17	24	Frequency 10
Frequency 4	18	23	Frequency 9
Frequency 5	19	22	Frequency 8
Frequency 6	20	21	Frequency 7

BLOCK DIAGRAM



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All Pin Voltages with respect to V_{SS} .....-30V to +0.3V
Storage Temperature .....-55°C to +150°C
Operating Temperature (T_A) .....-20°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

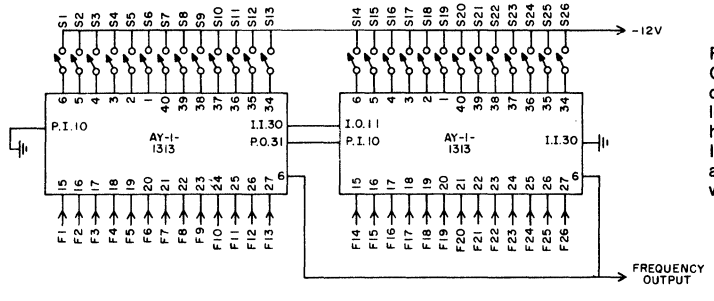
Standard Conditions (unless otherwise noted)

V_{DD} = -12±1V
V_{GG} = -27±1.5V
V_{SS} = GND

Characteristic	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS					
Switch Inputs Impedance	15	—	80	KΩ	Measured to Ground
Priority and Inhibit Inputs Impedance	1	—	—	MΩ	Measured to Ground
Input Logic "0"	—	—	-2	Volts	
Input Logic "1"	-9	—	—	Volts	
Output Logic "0"	—	—	-2	Volts	R_L = 47K to V_{DD}
Output Logic "1"	-9	—	—	Volts	R_L = 47K to V_{DD}
Frequency Output Switch					
Impedance — "ON"	—	—	20	KΩ	
"OFF"	5	—	—	MΩ	
I_{DD} Supply Current	—	—	8	ma	
I_{GG} Supply Current	—	—	1	ma	

**Typical values are at +25°C and nominal voltages.

TYPICAL APPLICATION



For multiple unit operation, the Priority Output of the higher priority unit is connected to the Priority Input of the lower, and the Inhibit Input of the higher priority unit is connected to the Inhibit Output of the lower. The Priority and Inhibit Inputs must be grounded when not in use.

Rhythm Generator

FEATURES

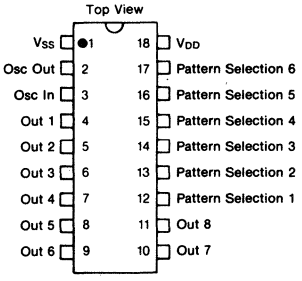
- Drives 8 instruments
- 32 beat long pattern
- 6 rhythm selections
- Internal oscillator
- Mask programmable rhythm pattern and pattern length
- Automatic reset for easy chord coupling

DESCRIPTION

The AY-5-1315 is a P-Channel MOS IC specifically designed for the Rhythm and Percussion section of an Electronic Organ and for Automatic Rhythmers. It contains all the logic circuits necessary to generate six sets of rhythm patterns driving eight instruments. The automatic reset feature allows it, when coupled with the chord section of the organ, to start on the downbeat every time a new chord is played. Selecting multiple patterns will result in a combination of the patterns selected. Tempo is externally adjustable from slower than largo to faster than presto. For added stability of the internal tempo oscillator a ÷ 32 circuit is provided. If an external tempo oscillator is used this circuit could be mask programmed out of the counter decoder chain. For added flexibility the output buffers could be mask programmed for either 100% or 50% duty cycle. The AY-5-1315 may be operated alone or in conjunction with the AY-5-1317A chord generator.

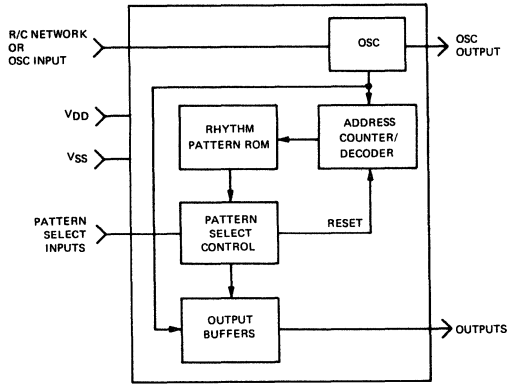
PIN CONFIGURATION

18 LEAD DUAL IN LINE

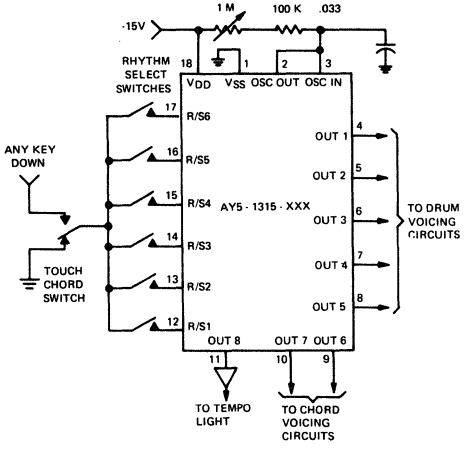


A separate publication, "AY-5-1315 Custom Coding Information", available from GI Sales Offices, describes the punched card and truth table format for custom programming of the AY-5-1315 memory.

BLOCK DIAGRAM



TYPICAL APPLICATION



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} .....-20V to +0.3V
Storage Temperature .....-65°C to +150°C
Operating Temperature (T_A) .....-25°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0 Volts, V_{DD} = -12 to -18 V

Characteristic	Min	Typ**	Max	Units	Conditions
Clock input					
Freq.	DC	100/1000	100K	Hz	with ÷32 circuit in
	DC	3/300	100K	Hz	with no ÷32 circuit
Logic '0'	V_{DD}–4.0	—	V_{DD}	V	
Logic '1'	+0.3	—	–1.0	V	
Internal osc. freq.	—	100/1000	—	Hz	Set by external resistor & capacitor
Rhythm select inputs					
Logic '0'	V_{DD}–4	—	V_{DD}	V	
Rhythm select inputs					
Logic '1'	+0.3	—	–1.0	V	
Rhythm select input					
impedance	10	—	—	KOhm	Pulled to V_{DD}
Instrument & osc. output					
Logic '0' (Note 1)	V_{DD}–6.0	—	V_{DD}–4.0	V	with internal pull ups to V_{DD} (instrument outputs only) supplying 0.1 mA
Instrument & osc. output					
Logic '1'	—	—	–1.0	V	Sinking 1.0 mA
Power	—	—	300	mw	V_{DD} = 15 volts

**Typical values are at +25°C and nominal voltages.

NOTE: 1. Open ended devices have a minimum impedance of 500K ohm to GND when in the off condition.

OPERATION

The AY-5-1315 Rhythm Generator contains an internal oscillator, a clock generator circuit, a 5-bit synchronous resetable counter/decoder, and a ROM that drives 8 instruments and the reset circuit. By selecting one of the 6 available rhythm patterns, the appropriate section of the ROM is enabled.

If no pattern is selected the reset circuit is activated which stops the internal oscillator, inhibits the output drivers and resets the counter to count 1. When a selection is made, the outputs are enabled which brings out the program as stored in count 1- the down beat program.

The oscillator frequency determines the tempo of the rhythm pattern generated. The clock generator generates a 2 phase clock $\phi 1$ and $\phi 2$. If the internal divide by 32 option is selected $\phi 1$ is on for the first 16 count and $\phi 2$ is on between count 17 and 32, thus producing two non overlaping clocks. If the divide by 32 circuit is programmed out, the circuit $\phi 1$ and $\phi 2$ will be directly related to the ON (logic 1) and OFF (logic 0) time at the clock generator input as provided by an external oscillator. The $\phi 2$ clock drives the 5 bit counter/decoder which sequentially turns on one of the 32 lines of the ROM.

On the $\phi 1$ clock, the program out of the ROM is transferred to the output thus eliminating decoding spikes at the output. If the output of the ROM is a '1' the proper instrument will be turned on. The output drivers are programmed either for 100% duty cycle or 50% duty cycle. When programmed for 100% duty cycle the output turned on will remain on for an entire $\phi 1/\phi 2$ cycle. If the next bit in the program is a '1' again, the output will remain on for the next cycle without going to zero between cycles. When programmed for 50% duty cycle the output will be on during $\phi 1$ only and return to zero during $\phi 2$.

AY-5-1317A

Chord Generator

FEATURES

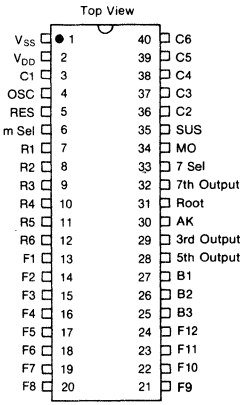
- ROOT, 3rd, 5th, 7th Chord Elements
- Additional output for special effects
- Sustain capability
- Top key priority
- Self-contained oscillator circuit
- Operated with single pole, single throw switch matrix

DESCRIPTION

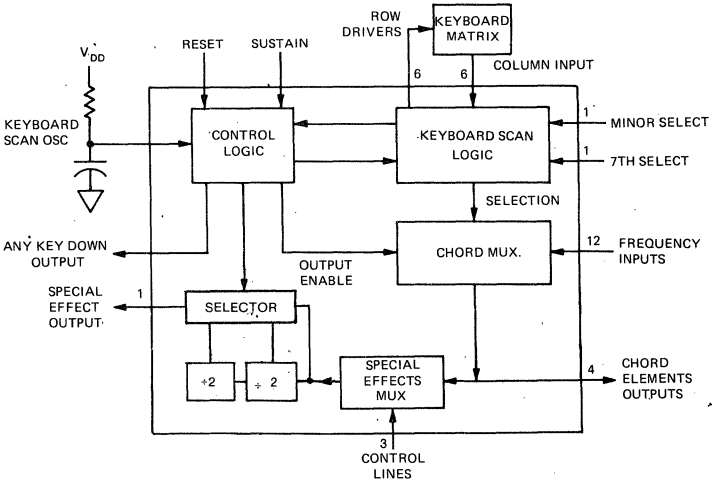
The AY-5-1317A is a P-Channel MOS IC which accepts twelve basic frequencies (one full octave) and outputs the notes necessary to form Major, Minor and Seventh chords. This is the only known standard chord generator IC that performs these functions. The chord elements (ROOT, 3rd, 4th, 5th, 6th, and 7th) can be multiplexed internally to perform special effects such as walking bass, rhythm arpegio, alternating bass, etc. The AY-5-1317A will operate in conjunction with and, through the KEY DOWN output, synchronize a rhythm generator such as the General Instrument AY-5-1315. The AY-5-1317A has a keyboard priority system with the C Major chord having the highest priority.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Name (Symbol)	Function
1	Ground (V_{SS})	Ground
2	Power Supply (V_{DD})	Negative Supply
3, 36-40	Column Inputs (C1-C6)	Column inputs from Keyboard Matrix
4	Oscillator Input (OSC)	R/C network connection for keyboard scan oscillator
5	Reset (RES)	A logic '1' (ground) will reset the keyboard scanner, and the memorized key
6	Minor Select (m Sel)	A Ground on this line changes the 3rd output from Major to Minor
7-12	Row Outputs (R1-R6)	Row outputs to Keyboard Matrix
13-24	Frequency Inputs (F1-F12)	These are the input lines for the 12 frequencies (one full octave B thru C) used to generate the chords.
25-27	Control Inputs (B3-B1)	These 3 lines will be internally latched and decoded to select either the ROOT, 3rd, 4th, 5th, 6th, or 7th frequency as the special effect output.
28	5th Output (5th)	This line will output the 5th frequency element of the selected chord.
29	3rd Output (3rd)	This line will output the 3rd frequency element of the selected chord. Minor 3rd will be provided if a Minor chord is selected. Major 3rd will be provided if a Major or 7th chord are selected.
30	Any Key Down (AK)	This line goes to a logic '1' whenever a chord selection key is depressed.
31	Root Output (Root)	This line will output the ROOT frequency element of the selected chord.
32	7th Output (7th)	This line will output the 7th frequency element of the selected chord if a 7th chord is selected otherwise the output is logic '0' (voltage).
33	7th Select (7 Sel)	A ground on this line turns the 7th output on.
34	Special Effect Output (MO)	This line will output one of the six frequency elements as programmed by the control lines B1-B3. The 7th chord element frequency will be provided independently of the chord selection.
35	Sustain (SUS)	A logic '1' on this line will activate the memory circuit which memorizes the last key played.

B1	B2	B3	Selection
0	0	0	No change from last selection.
0	0	1	ROOT
0	1	0	5th
0	1	1	3rd
1	1	1	7th
1	1	0	4th
1	0	1	6th

TRUTH TABLE FOR SPECIAL EFFECT OUTPUT

FREQUENCY OUTPUTS

Chord Selection	Root	3rd Minor	3rd Major	4th	5th	6th	7th
C	C (÷2)	D (÷2)	E (÷2)	F (÷2)	G (÷2)	A (÷2)	A# (÷2)
C#	C# (÷2)	E (÷2)	F (÷2)	F# (÷2)	G# (÷2)	A# (÷2)	B (÷2)
D	D (÷2)	F (÷2)	F# (÷2)	G (÷2)	A (÷2)	B (÷2)	C# (÷1)
D#	D# (÷2)	F# (÷2)	G (÷2)	G# (÷2)	A# (÷2)	C (÷1)	C (÷1)
E	E (÷2)	G (÷2)	G# (÷2)	A (÷2)	B (÷2)	C# (÷1)	D# (÷1)
F	F (÷2)	G# (÷2)	A (÷2)	A# (÷2)	C (÷1)	D (÷1)	D (÷1)
F#	F# (÷4)	A (÷4)	A# (÷4)	B (÷4)	C# (÷2)	D# (÷2)	E (÷2)
G	G (÷4)	A# (÷4)	B (÷4)	C (÷2)	D (÷2)	E (÷2)	F# (÷2)
G#	G# (÷4)	B (÷4)	C (÷2)	C# (÷2)	D# (÷2)	F (÷2)	F (÷2)
A	A (÷4)	C (÷2)	C# (÷2)	D (÷2)	E (÷2)	F# (÷2)	G (÷2)
A#	A# (÷4)	C# (÷2)	D (÷2)	D# (÷2)	F (÷2)	G (÷2)	G# (÷2)
B	B (÷4)	D (÷2)	D# (÷2)	E (÷2)	F# (÷2)	G# (÷2)	A (÷2)

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} with respect to V_{SS} . . . . . −20V to +0.3V
Logic Input Voltages with respect to V_{SS} . . . . . −20V to +0.3V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied —operating ranges are specified below.

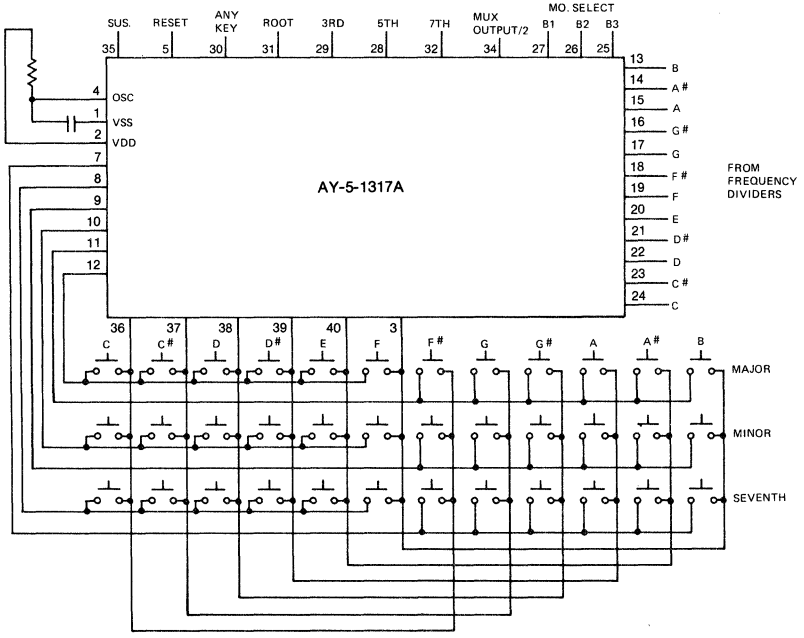
Standard Conditions (unless otherwise noted)

V_{DD} = −15V ±3V
V_{SS} = 0V (substrate voltage)
Operating Temperature (T_A) = +25°C

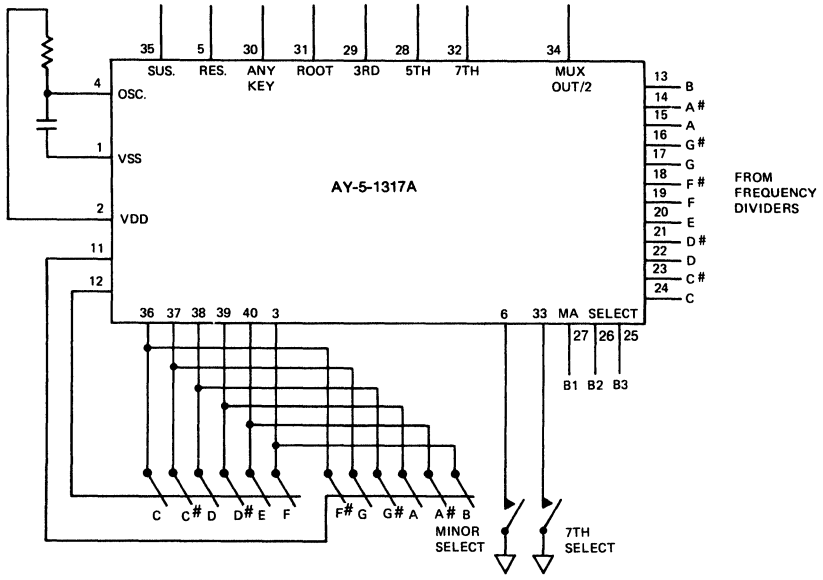
Characteristic	Sym	Min	Typ**	Max	Conditions
Input Logic Levels					
Logic 0	VIL	V_{DD}	—	−8.5	
Logic 1	VIH	−1.0V	—	+0.3V	
Input Capacitance	CIN	—	—	10 pf	
Note Outputs					
Logic 0	R_{OFF}	160KΩ	—	—	
Logic 1	R_{ON}	—	—	500Ω	
Row Drivers Output Impedance		—	750Ω	—	V_{DD} = −15V
Control Input		10KΩ	—	1000KΩ	
Keyboard Row Input Impedance		24KΩ	—	100KΩ	
Keyboard Scan Frequency		—	25KHz	—	500 pf,750K,V_{DD} = −15V

**Typical values are at +25°C and nominal voltages.

STANDARD INTERCONNECTION FOR A 3×12 KEY MATRIX



STANDARD INTERCONNECTION FOR A SINGLE ROW KEYBOARD WITH SEPARATE KEY FOR MINOR AND SEVENTH



5

4-5-6-7 Stage Frequency Dividers

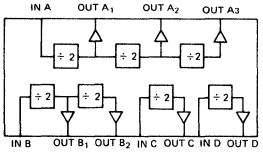
FEATURES

- DC to 1 MHz operating frequency range.
- Diode protection on all inputs.
- Low output impedance in both states.
- Choice of configurations:
  1) AY-1-5050: 7-Stage Frequency Divider, 3+2+1+1
  2) AY-1-5051: 4-Stage Frequecy Divicer, 2+1+1
  3) AY-1-6721/5: 5-Stage Frequency Divider, 3+2
  4) AY-1-6721/6: 6-Stage Frequency Divider, 3+2+1

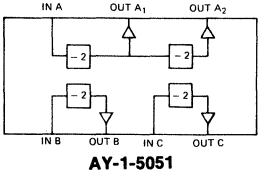
DESCRIPTION

The AY-1-5050, AY-1-5051, AY-1-6721/5 and the AY-1-6721/6 are constructed on monolithic silicon chips using MTOS (Metal-Thick-Oxide-Silicon) P-Channel Enhancement Mode Field Effect Transistors. All circuits can be driven from a sine or square wave input. The different types all have the same specifications and are fully compatible with one another.

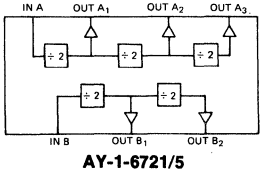
BLOCK DIAGRAMS



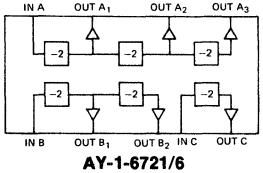
AY-1-5050



AY-1-5051



AY-1-6721/5

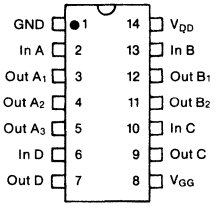


AY-1-6721/6

PIN CONFIGURATIONS

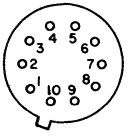
14 LEAD DUAL IN LINE
AY-1-5050

Top View



10 LEAD
AY-1-5051

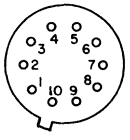
Bottom View



1	Out A_1	6	In C
2	Out A_2	7	Out C
3	In B	8	V_{GG}
4	Out B	9	V_{DD}
5	GND	10	In A

10 LEAD
AY-1-6721/5

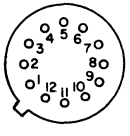
Bottom View



1	GND	6	In A
2	Out B_2	7	Out A_1
3	Out B_1	8	Out A_2
4	In B	9	Out A_3
5	V_{GG}	10	V_{DD}

12 LEAD
AY-1-6721/6

Bottom View



1	GND	7	Out C
2	In A	8	V_{DD}
3	Out A_1	9	Out B_2
4	Out A_2	10	Out B_1
5	Out A_3	11	In B
6	In C	12	V_{GG}

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Drain Voltage	−30V to +0.3V
Gate Voltage	−30V to +0.3V
Data Input Voltage	−30V to +0.3V
Storage Temperature	−55°C to +150°C
Operating Temperature (T_A)	0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

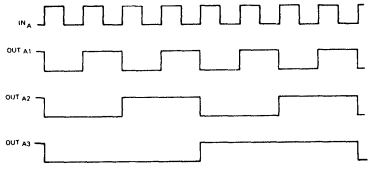
V_{DD} = −13V ±1V
V_{GG} = −27V ±1V
R_L = 1M Ohm
C_L = 10 pF
Operating Temperature (T_A) = +25°C

Characteristics	Min.	Typ**	Max	Units	Conditions
Data Input					
Logic "0" level	—	—	−2	V	
Logic "1" level	−10	—	—	V	
Data Input operating freq.	DC	—	1	MHz	Sine or square wave
Data Input Pulse width					
— "0" level	300	—	—	nS	
— "1" level	300	—	—	nS	
Input Leakage	—	—	5	μA	V_{in} = −20V dc
Output Parameters					
Logic "0" level	—	—	−1	V	
Logic "1" level	−11	—	—	V	
Drive Capability					
— "0" level	—	−1	−1.5	V	Sinking current = 0.5 mA
— "1" level	−11	—	—	V	R_L = 100 KΩ
— "1" level	−8	—	—	V	R_L =10 KΩ
Data output Rise and Fall time	—	0.6	—	μS	
Current Drain					
I_{GG}	—	3	—	mA	V_{GG} = −27 V
I_{DD}	—	***	—		

**Typical values are at +25°C and nominal voltages.

*** V_{DD} is only used for the push-pull outputs therefore I_{DD} is equal to the sum of load currents. This separate V_{DD} enables tremulant to be introduced in the electronic organ application.

TIMING DIAGRAM



NOTE: The AY-1-5051 outputs change state on the negative going edge of the clock. All others operate as shown.

GENERAL INSTRUMENT

AY-5-1230
CT7000

6

Clock / Appliance Timer

FEATURES

- 4 Digit Clock.
- Drives 7 segment Fluorescent Displays.
- Programmable switch on and switch off times.
- Repeating or non-repeating operation.
- Dimming control.
- Power on reset, remains reset until time is set.
- Foolproof switch on/off setting, if switch off time not programmed output stays on for 10 minutes only.
- Non multiplexed set inputs for low radiated noise.
- Indication of set alarm state.

DESCRIPTION

The AY-5-1230 Clock/Appliance Timer is a circuit designed to provide a four digit clock display and automatic on/off switching of a TV or other appliance at any desired time.

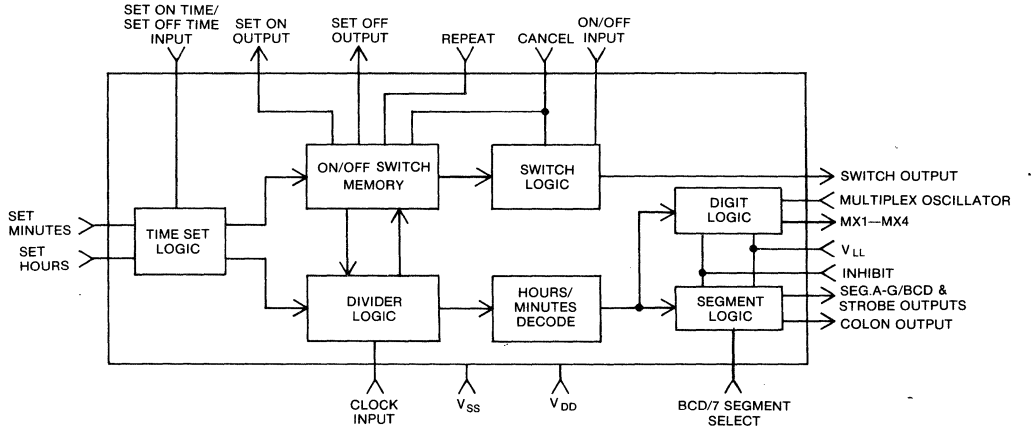
PIN CONFIGURATION

28 LEAD DUAL IN LINE

Top View

V_{SS} (GND)	1	28	Inhibit Input
Set ON Time/Set OFF Time	2	27	BCD/7 Segment
Repeat Input	3	26	V_{DD}
Set ON Output	4	25	Cancel Input
Set OFF Output	5	24	ON/OFF Input
Clock Input	6	23	Multiplex Oscillator
Set Minutes Input	7	22	Switch Output
Set Hours Input	8	21	MX_1 Output
V_{LL} (Display Supply)	9	20	MX_2 Output
Seg. G Output	10	19	MX_3 Output
Seg. F Output	11	18	MX_4 Output
Seg. E Output/Strobe Out	12	17	Colon Output
Seg. D Output/2^0 Out	13	16	Seg. A Output/2^3 Out
Seg. C Output/2^1 Out	14	15	Seg. B Output/2^2 Out

BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Name	Function
1.	V_{SS}	Positive Supply
2.	Set ON time/Set OFF time Input	When taken to logic '0' the ON time is displayed and the Set hours and Set minutes inputs operate the ON time counter. When taken to logic '1' the OFF time is displayed and the Set hours and Set minutes inputs operate the OFF time counter. When left open circuit the time is displayed. When either Set ON or Set OFF is activated the Switch logic is set and the switch output will operate at the set times.
3.	Repeat Input	When connected to logic '0' the Switch output comes on every 24 hours. When left open circuit the Switch output comes on only once after which the Switch logic is reset. The switch logic can be set again by pressing Set ON and Set OFF.
4.	Set ON Output	This output goes to logic '0' when an ON time has been set. It returns to '1' when the switch logic has timed out or has been cancelled.
5.	Set OFF Output	This output goes to logic '0' when an OFF time has been set. It returns to '1' when the switch logic has timed out or has been cancelled.
6.	50Hz Clock Input	The timing clock is input to this pin. Hysterisis is provided so that the input waveform is not critical.
7.	Set Minutes Input	When this input is taken to logic '0' the minutes counter is advanced twice per second. During setting the minutes counter does not overflow into the hours counter.
8.	Set Hours Input	When this input is taken to logic '0' the hours counter is advanced twice per second.
9.	V_{LL} (Display supply)	The on chip pull up resistors provided for each high voltage output are connected to this pin. When driving fluorescent display this pin is connected to −32 Volts.
10-13	7 Segment Outputs	High voltage outputs capable of driving fluorescent displays directly. At logic '0' to display. They have on-chip pull down resistors to V_{LL}.
13-16	BCD Outputs	In the BCD mode the time data is output on these pins.
17.	Colon Output	This high voltage output is enabled on Mx3 time and flashes once per second.
18-21	Mx1-Mx4 Outputs	These outputs are switched to logic '0' successively to select the digits, Mx4 is 10s hours, Mx1 is units mins. There are 5 time slots the fifth being blank. These outputs are high voltage and have on-chip pull down resistors to V_{LL}.
22.	Switch Output	This output goes to logic '0' when the ON time is reached and returns to logic '1' when the OFF time is reached. If an OFF time has not been programmed the output will return to logic '1' ten minutes after the ON time has been reached. The output will sink 30mA.
23.	Multiplex Oscillator	Not used normally. An external capacitor can be connected to reduce the mux frequency, or an external clock can be applied if required.
24.	ON/OFF Input	When this input is taken to logic '0' the switch output is alternately turned ON and OFF. This input has antibounce logic to prevent maloperation.
25.	Cancel Input	When this input is taken to logic '0' the Switch logic is reset and the Switch output turned off.
26.	V_{DD}	Negative supply 15V nom. (11-19V)
27.	BCD/7 Segment Select	When this input is wired to logic '0' BCD operation results.
28.	Inhibit Input	When this input is taken to logic '0' display outputs are switched off. This input can be used for display dimming.

NOTE:
1. All inputs have a pull down resistor to V_{GG}
2. At power-on the chip is reset but the clock does not start to count until either the set hours or set minutes button has been pressed.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin (except display pins) with respect to V_{SS} pin . . . . . +0.3 to −20V
Voltage on display pins with respect to V_{SS} pin . . . . . +0.3 to −35V
Operating temperature range . . . . . 0°C to +70°C
Storage temperature range. . . . . −55°C to +150°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

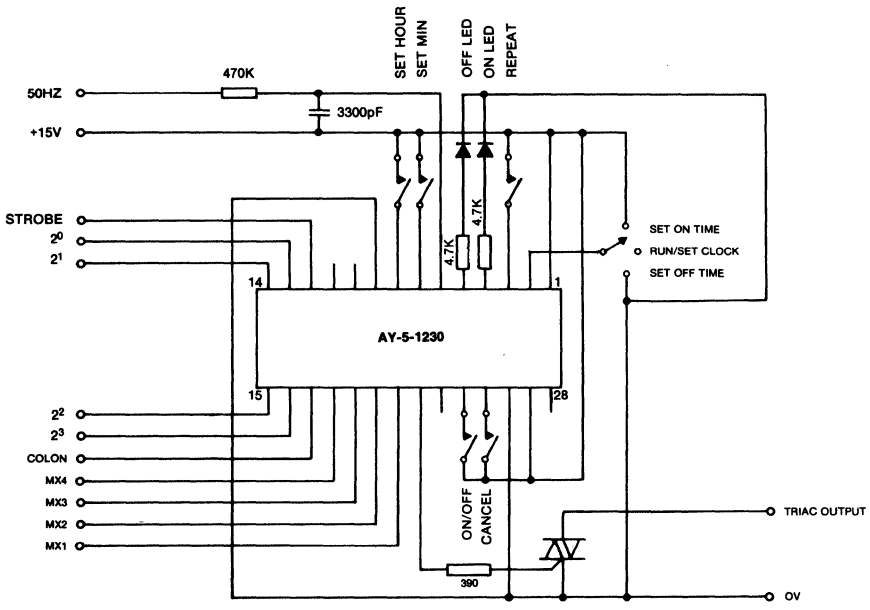
Standard Conditions (unless otherwise noted)

V_{SS} = OV
V_{DD} = −11 to −19V
V_{LL} = −31 to −33V
Operating Temperature (T_A) = 0°C to +70°C

Characteristics	Min	Typ**	Max	Units	Conditions
Clock Input					
Frequency	—	50	—	Hz	
Logic '0'	+0.5	—	−2	Volts	Note 1
Logic '1'	−8	—	−19	Volts	
Multiplex Clock Frequency	—	100	—	KHz	Note 2
Control Inputs					
Logic '0'	+0.3	—	−1.5	Volts	
Logic '1'	−6	—	−19	Volts	
Pull Up Resistance	—	200	—	Kohm	to V_{DD}
Segment Output					
Logic '0'	—	—	−2	Volts	Iout = 2mA
Logic '1'	—	—	10	μA	V_{OUT} = −35V
Mx Outputs					
Logic '0'	—	—	−2	Volts	Iout = 5mA
Logic '1'	—	—	10	μA	V_{OUT} = −35V
Pull Up Resistance	—	200	—	Kohm	to V_{LL}
Switch Output					
Logic '0'	—	—	−2	Volts	I_{OUT} = 30mA
Logic '1'	—	—	10	μA	V_{OUT} = −19V
Set ON, OFF Outputs:					
Logic '0'	—	—	−2	Volts	I_{OUT} =2mA
Logic '1'	—	—	10	μA	V_{OUT} = −19V
Power	—	350	—	mW	

**Typical values are at +25°C and nominal voltages.

NOTE:
1. The clock input may be taken positive provided that the current is limited to 100μA
2. This results in a multiplex rate of 5KHz.


SET HOUR
SET MIN
OFF LED
ON LED
REPEAT
470K
50HZ
3300pF
+15V
4.7K
4.7K
STROBE
2^0
2^1
SET ON TIME
RUN/SET CLOCK
SET OFF TIME
14
1
AY-5-1230
15
28
2^2
2^3
COLON
MX4
MX3
MX2
MX1
ON/OFF
CANCEL
TRIAC OUTPUT
390
OV

Appliance Mini-Timer

FEATURES

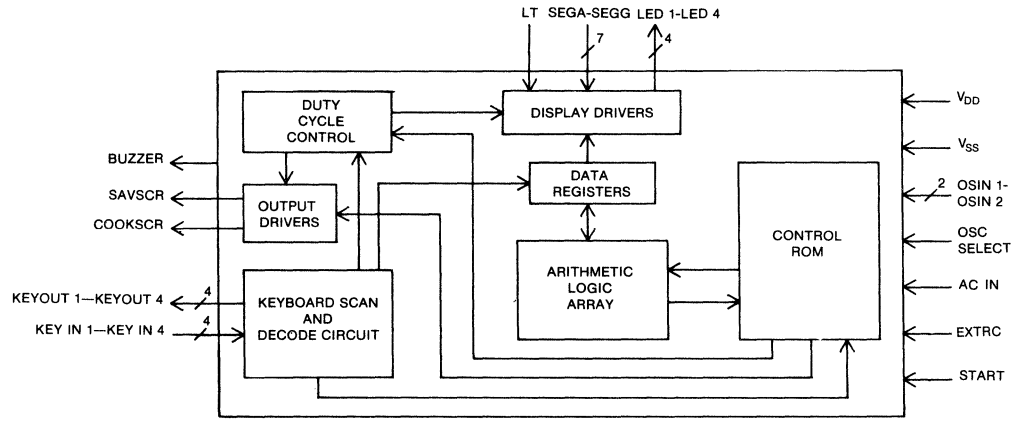
- Three modes of operation:
  1) Microwave oven control with selectable cycles—up to 100 minutes.
  2) Down count timer—up to 100 minutes.
  3) Up count timer—up to 10 hours.
- Four digit 7-segment display with direct drive or segments.
- Four direct sink single LED's as mode indicators:
  1) COOK mode with 100% duty cycle.
  2) SLOW COOK mode with selectable duty cycle at 10% increments.
  3) DOWN COUNT mode.
  4) UP COUNT mode.
- Positive feedback for a higher degree of safety.
- Resonator as an alternative frequency source.
- Low power dissipation.

DESCRIPTION

The Appliance Mini-Timer is a N-Channel integrated circuit containing all the logic necessary for a multifunction timer. Its features are especially adapted for operating as a microwave oven timer. As a general timer, it can receive its frequency source from the 60 Hz AC line or a crystal/resonator source. It is capable of operating in up count or down count modes which are interchangeable by pressing a stop key and then the key of the mode desired. The remaining time is not lost and is constantly being displayed. Count time can also be altered as the keyboard is equipped with a reset key. When the count down sequence is finished, a gentle buzz is generated indicating the end of the cycle. The count down sequence can also be initiated by an AC switch supplying a 60 Hz source to the Timer. Then by positive feedback action, the 60 Hz is sustained even after this switch is released.

This count down mode is especially adapted for the microwave oven and the positive feedback action ensures a higher degree of safety. The cooking duty cycle can be selected through the keyboard. The range is from 10% to 90% in 10% increments. The 100% duty cycle is the default value when no selection is indicated. When the 60 Hz source is discontinued through a stop switch or the opening of the oven door, the count down stops but the remaining time continues being displayed. The duty cycle can now be examined or altered before re-initiation of the cycle through the start switch. Furthermore, through the use of mask programming techniques, the duration of a cycle can also be selected. It is from 10 seconds to 60 seconds at 5 second increments. The Appliance Mini-Timer is offered in a 40 pin plastic DIP.

BLOCK DIAGRAM



PIN FUNCTIONS

Name	Function
V_{DD}	+4.5 to +14 volts supply
V_{SS}	Ground
LED 1 TO LED 4	Digit drivers
SEG A TO SEG G	Segment drivers
LT	Mode indicator LED driver
KEY IN 1 TO KEY IN 4	Keyboard sinking inputs forming the horizontal scan for the keyboard.
START	Input for 60 Hz AC signal or ground to initiate start of a COOK or SLOW COOK cycle
BUZZER	2 KHz signal output for 2 to 3 seconds at the end of a count down cycle.
KEYOUT1 TO KEYOUT4	Keyboard sourcing outputs forming the vertical scan for the keyboard.
OSC SELECT	Select oscillation source '1' : AC source "0" : resonator source
AC IN	AC source input for time base.
OSIN1 AND OSIN2	Resonator/crystal inputs connecting to resonator/crystal directly.
EXTRC	Connection for external resistor and capacitor.
SAVSCR	Positive feedback output for driving SCR used to control switch relay.
COOKSCR	Output for driving SCR used for sinking magnetron tube.

6

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} . . . . . 18V to −0.3V
Storage temperature. . . . . −55°C to +150°C
Operating temperature . . . . . −25°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0 Volts
V_{DD} = +4.5 to +14 Volts

Characteristics	Min	Typ**	Max	Units	Conditions
Input logic '1'	2.4	—	V_{DD}	Volts	
Input logic '0'	0	—	.8	Volts	
Output logic '1'	2.8	—	V_{DD}	Volts	
Output logic '0'	—	—	.4	Volts	
Clock frequency (time base)	—	60	—	Hz	AC operated
	—	559.7	—	KHz	crystal/resonator
High frequency	375	500	625	KHz	Resistance=100K ohms capacitance=30 pfd
Buzzer frequency	—	High freq÷256	—	—	

**Typical values are at +25°C nominal voltages.

GENERAL INSTRUMENT

AY-5-9100
AY-5-9200
AY-5-9300
AY-3-9400
AY-3-9410
AY-5-9500
AY-5-9800

7

Push Button Telephone Dialler Circuit

FEATURES

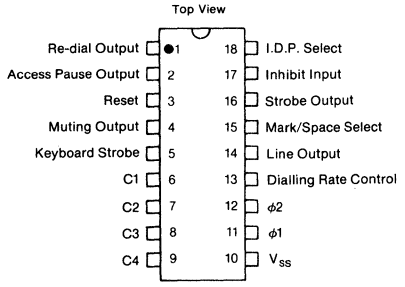
- 20 Digit Storage
- Selectable dialling rate
- Selectable mark/space ratio
- Selectable Inter-Digital Pause
- Dynamic circuitry—less than 2 mw power consumption
- Re-dial of last number
- Access Pause Facility
- Companion Repertory Dialler chip (AY-5-9200)

DESCRIPTION

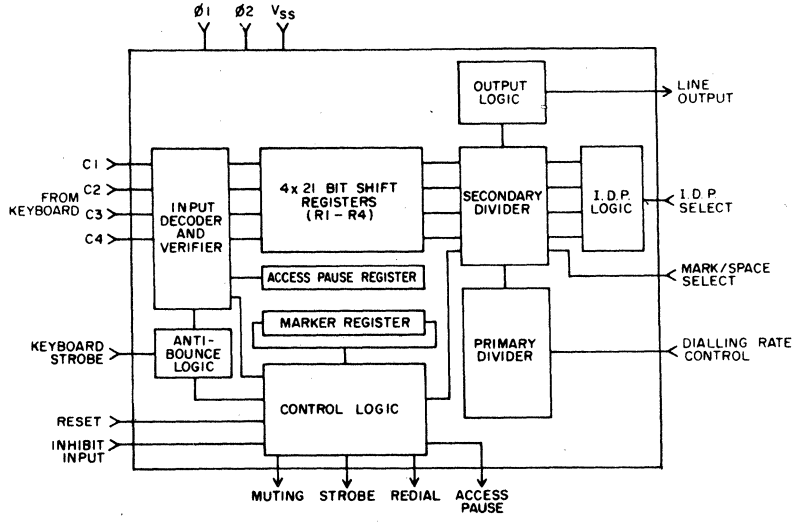
The AY-5-9100 Push Button Dialler provides all of the logic required to convert a push button input to a series of pulses suitable for simulating a telephone dial. Pulse repetition rate, interdigital pause, and mark-space ratio are all programmable. Outputs are provided for line pulsing and muting. An "inhibit input" is provided to allow storage of one number of up to 20 digits. An "Access pause" capability is provided to allow automatic operation with a PBX or WATS line system. The low (<2 mw) power consumption enables line-powered operation in a PBX or similar system. The AY-5-9100 may be operated alone or in conjunction with the AY-5-9200 repertory dialler.

PIN CONFIGURATION

18 LEAD DUAL-IN-LINE



BLOCK DIAGRAM



PIN FUNCTIONS

Pin.No. Name/Description

1. Re-Dial Output
A logic "0" at this output indicates that redial mode has been selected.

2. Access Pause Output
A logic "0" at this output indicates that an access pause is required.

3. Reset
A logic "0" on this input clears all shift registers and resets all counters. Reset should be applied after power on to clear the device.

4. Muting Output
The muting output goes to logic "0" whenever data is being entered or transmitted. It returns to logic "1" when the access pause output turns on and when transmission is complete.

5. Keyboard Strobe
This is the common signal from all of the keys. A logic "0" on this input indicates that either the inhibit input or C1-C4 are to be read.

6.-9. C1-C4
These are the keyboard data inputs. They are encoded as follows to allow simple interface with a standard push button (2-of-7) keyboard.

Digit	Impulses	C1	C2	C3	C4
1	1	1	1	1	1
2	2	1	1	1	0
3	3	1	1	0	1
4	4	1	0	1	1
5	5	1	0	1	0
6	6	1	0	0	1
7	7	0	1	1	1
8	8	0	1	1	0
9	9	0	1	0	1
0	10	1	1	0	0
Access Pause	—	0	0	1	1

10. V_{SS}

11. $\phi 1$

12. $\phi 2$

13. Dialling Rate Control
This input controls the line pulsing frequency as follows: (See Note 1):

Input	Line Pulse Rate
$\phi 1$	600 p.p.s.
$\phi 2$	20 p.p.s
V_{SS}	10 p.p.s

Pin.No. Name/Description

14. Line Output
A logic "0" on this output is a line pulse "mark" or "break."

15. Mark/Space Select
The mark to space ratio is controlled by this input as follows:

Input	Mark	Space
$\phi 1$	70	30
$\phi 2$	50	50
Logic 0	66 ⅔	33 ⅓
Logic 1	60	40

These ratios are exact and do not depend on clock frequency.

16. Strobe Output
This output goes to logic "0" to indicate that a digit is being out-pulsed.

17. Inhibit Input
The inhibit input is used to inhibit out-pulsing and to place the device in re-dial mode.

The keyboard strobe must be taken to logic "0" at any time the inhibit input is strobed, except when an Access Pause is being signalled.

This input normally operates as a "toggle flip-flop". If it is taken to a logic "1" any time other than when an access pause is being signalled, the circuit will lock into the redial mode and the redial output will go to logic "0". The chip will remain in the re-dial mode until this input is taken to logic "1" again.

If the chip is cleared before inhibit is toggled, digits entered are accepted, but out-pulsing does not commence until the inhibit is re-strobed. If a number is being outpulsed when the inhibit is strobed, dialling ceases until the inhibit is re-strobed. If the inhibit is strobed when a dialling sequence is completed, the re-dial output goes to logic "0" and the number is stored. Re-strobing the inhibit starts the dialling sequence.

When an access pause is signalled, this input no longer operates as a toggle, but rather as a gate, with a logic "1" inhibiting further out-pulsing.

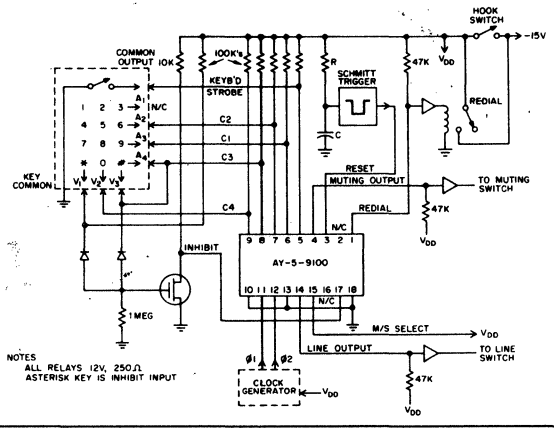
This input controls the inter-digital-pause as follows: (See Note 1):

Input	I.D.P. 10 p.p.s.	20 p.p.s.	600 p.p.s.
$\phi 2$	400 mSec	200 mSec	6.66 mSec
V_{SS}	800 mSec	400 mSec	13.33 mSec
$\phi 1$	1000 mSec	500 mSec	18.33 mSec

A pre-digital pause equal in length to the inter-digital pause precedes the first digit of any number.

NOTE:
1. Line Pulse Frequency and Inter-Digital Pause are specified with an 18 kHz clock frequency.

TYPICAL APPLICATION



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Input Voltages (with respect to V_{SS}) . . . . . −20V to +0.3V
Storage temperature. . . . . −65°C to +150°C
Operating temperature . . . . . −55°C to +80°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

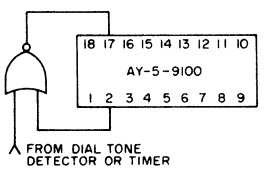
Standard Conditions (unless otherwise noted)
V_{SS} = 0V
T_A = −55°C to +80°C
Negative logic conventions are followed for this data sheet.

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
Clocks (see Fig.1)						
Logic '1'	$V\phi_L$	−13.5	—	−16.5	V	
Logic '0'	$V\phi_H$	+0.3	—	−1.0	V	Match clocks within 0.5V
Frequency	f	10	18	30	kHz	See Note 2
Capacitance	$C\phi$	—	90	150	pF	Each clock input, $V\phi$ = OV, f = 1MHz
Rise Time	t_r	.1	—	8	μs	
Fall Time	t_f	.1	—	4	μs	
Leakage	$I_L\phi$	—	—	30	μA	$V\phi$ = −16.5, T_A = +80°C
Pulse Width	$t\phi_{PW}$	5	—	40	μs	
Pulse Separation	$t\phi_{PS}$	5	—	40	μs	
All Outputs (Note 3)						
On Resistance (Logic '0')	R_{ON}	—	—	1	kΩ	V_{OH} = −1 volt
Off Leakage (Logic '1')	I_{LO}	—	—	10	μA	V_{OL} = −10V. T_A = 25°C
Line Output (See Fig.3)						
Strobe-Line Delay	t_p	—	—	3	ms	
Line-Strobe Delay	t_o	33	—	—	ms	MARK/SPACE = 66 2/3–33 1/3 (t_o increases for other MARK/SPACE RATIOS)
Muting Output (See Fig.3, 4)						
Line-Muting Delay	t_m	33	—	—	ms	MARK/SPACE = 66 2/3–33 1/3 (t_m increases for other MARK/SPACE RATIOS)
All Inputs (Except Reset)						
Logic '1'	V_{IL}	−4.0	—	−16.5	V	
Logic '0'	V_{IH}	+0.3	—	−1.0	V	
Leakage	I_{LI}	—	—	1	μA	V_I = −16.5, T_A = 25°C
Rise and Fall Time	t_r, t_f	—	—	10	μs	
Capacitance	C_I	—	—	5	pF	V_I = OV, F = 1MHz
Keyboard Strobe Input (See Fig.2)						
Pulse Width	t_{KPW}	10	—	—	ms	Effective only when RESET input is at Logic '1'
Reset Input (See Fig.2)						
Logic '1'	V_{IL}	−4.0	—	−16.5	V	
Logic '0'	V_{IH}	+0.3	—	−1.0	V	
Leakage	I_{LI}	—	—	1	μA	Vin = −16.5, T_A = 25°C
Capacitance	C_I	—	—	5	pF	Vin = 0V, f = 1MHz
Fall Time	t_{Rf}	3	—	100	μs	
Delay Time	t_D	3	—	—	ms	After clocks reach full amplitude
Power	—	—	0.9	2	mW	$V\phi$ = 16.5V

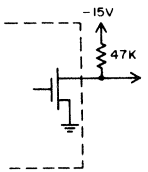
**Typical values are at +25°C and nominal voltages.

NOTES:
2. Line Pulse Rate depends upon frequency of clock input. Standard clock frequency is 18kHz.
3. Outputs require external pull-down resistors (47kΩ typical).

ACCESS PAUSE OPERATION



TYPICAL OUTPUT INTERFACE



OPERATION

The 4 bit code from the keyboard arrives on inputs C1-C4 of the Push Button Dialler. A fifth input from the keyboard, the Keyboard Strobe, is also required. In its quiescent state the five inputs are at logic 1 (−volts). A logic 0 on the Keyboard Strobe input indicates to the input circuitry that it is to read the data on C1-C4, thus allowing 1111 as an allowable code from the keyboard.

When a digit key is depressed the input logic detects the 1-0 transition on the Keyboard Strobe input. When this occurs a timer with a minimum count time of 8.5 mSec is started. If the common input is removed before this period has elapsed, the counter will be reset to its starting state. If the Keyboard Strobe input is stable for at least 8.5 mSec, the code is fed to the code verifier and converter.

If the code is invalid, it is ignored. If valid it is converted to the proper BCD code and written into recirculating shift registers R1-R4. If an access pause is decoded, it is written into the access pause register.

Simultaneous with the data being written into R1-R4, the muting output goes to logic "0", to disconnect the transmission circuitry. When all digits that have been keyed into the circuit have been dialled out the muting output returns to logic "1".

During dialling if an access pause is required, the muting output will reconnect the transmission circuitry so that the caller can listen for the dial tone and ensure himself that the system is functioning correctly.

The digit store has a capacity of 20 digits. The numbers are read non destructively allowing redial.

Four 21 bit registers hold the number in BCD format; the number is stored in parallel. A fifth register holds a marker bit (Signified as A) showing the first number entered. This fifth register has a gated 22nd bit allowing the marker bit (A) to be 'slipped' backwards one bit with respect to the number. Gating ensures that all numbers are sequentially entered, the first aligning itself with the marker A. When the first number is to be loaded into the counter, A is decoded in its 21st position and the parallel enable signal reads the first digit into the counter. Gating is enabled to allow A to be shifted through the 22nd bit of the marker store, so aligning itself with the next number to be dialled out. When A is decoded at the 21st bit and no number is in the stored digit register, A remains aligned in this state until 'redial' is depressed and the marker store goes into its 22nd bit mode until A aligns with the first digit.

Gating ensures that only 20 digits are entered into R1-4. One empty state at least is required to indicate to the system that a number is complete.

TIMING DIAGRAMS

Fig.1 Clock Waveforms

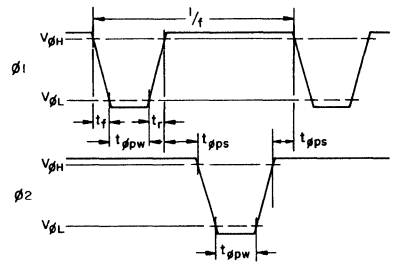


Fig.2 Reset and Keyboard Strobe Timing

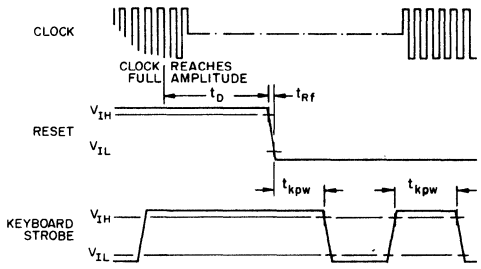


Fig.3 Line, Muting and Strobe Output Timing

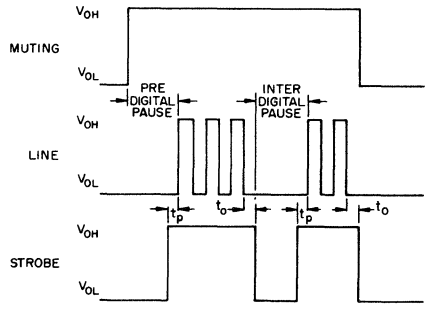
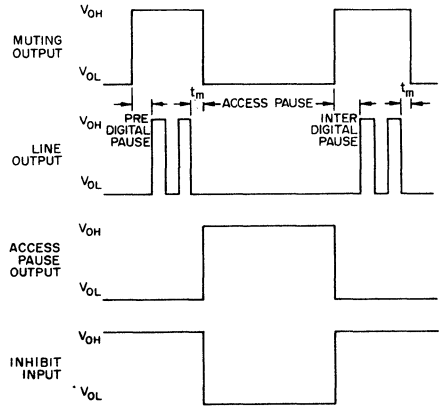


Fig.4 Line, Muting and Access Pause Output Timing



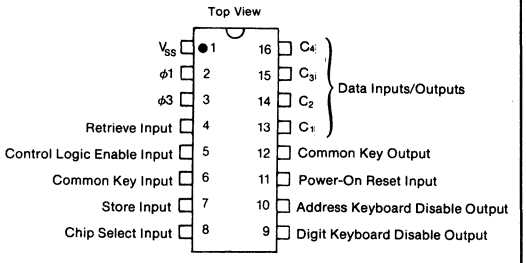
Repertory Dialler

FEATURES

- Stores 10 x 22 digit telephone numbers, including access pauses.
- Devices can be 'stacked' to give a store expandable in blocks of 10 numbers.
- Operates in conjunction with the AY-5-9100 Push-Button Dialler.
- Single or Dual Keyboard operation.
- Interfaces to standard MF Tone Dialler Keyboards.
- Applications in Repertory Diallers and Security Systems.
- Will operate MF Tone Diallers such as the AY-3-9400.
- Low power consumption, typically 2.25mW.

PIN CONFIGURATION

16 LEAD DUAL IN LINE



DESCRIPTION

The AY-5-9200 is a 10 number store designed to work in conjunction with the AY-5-9100 Push Button Telephone circuit to form a Repertory Dialler, each of the 10 numbers containing up to 22 digits or access pauses.

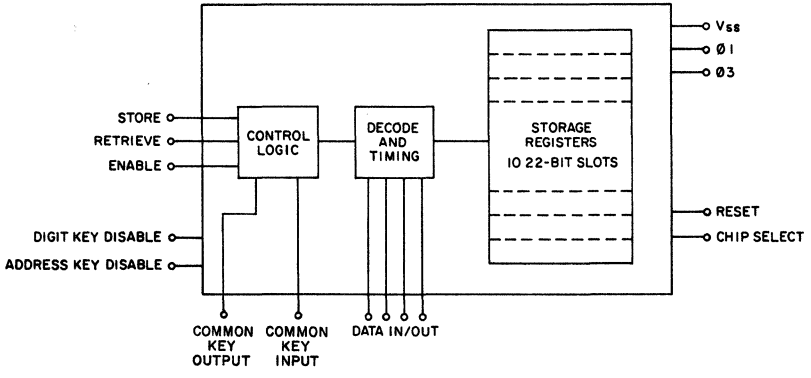
The keyboard, AY-5-9100 and as many AY-5-9200's as required are all connected to a 4 line data bus. Numbers for direct dialling are routed to the AY-5-9100, numbers to be stored go straight to the AY-5-9200. Numbers that are being retrieved are transmitted from the AY-5-9200 to the AY-5-9100 while control outputs from the AY-5-9200 determine the routing of the data.

The system may operate either with a single 12 button keyboard, which is used for both address and digit entry, or with separate address and digit keyboards. Single keyboard operation would normally be employed in a 10 number Repertory Dialling telephone. Dual keyboard operation is usual for 10 to 100 number Repertory Diallers.

The AY-5-9200 may also be used in MF tone dialling systems, the output data rate being directly compatible.

Four phase logic is used to achieve minimum power consumption, the circuits being manufactured using the MTNS P-channel nitride MOS process.

BLOCK DIAGRAM



Pin.No.	Name	Function
1	V_{SS}	This is the ground and substrate connection and is used as a reference for all the electrical parameters.
2-3	Clocks $\phi 1$, $\phi 3$	These inputs form the two supply clocks, and alternate negative-going pulses are required. These are described in the Electrical Characteristics and fig. 1. Any deviation from the nominal 18KHz will result in a proportional modification of the on-chip timings.
4	Retrieve Input	The retrieve input must be taken to a logic '1' for at least 10ms to indicate when a retrieve operation is to be performed. Anti-bounce logic is provided on this input.
5	Control Logic Enable Input	This input must be taken to a logic "1" for the duration of any store or retrieve operation. The control logic is reset when the input returns to logic 'O'. Anti-bounce is provided for this input.
6	Common Key Input	This input is taken from the common contact on all keyboards. A '1' to '0' transition will indicate a key closure. Anti-bounce is provided to ensure only a single depression is read.
7	Store Input	This input must be taken to a logic '1' for the duration of any store operation. Anti-bounce logic is provided for both logic transitions.
8	Chip Select Input	When at logic '0' all inputs and outputs (except for Common Key input and output) are inhibited. It may be permanently wired to logic '1' if only one AY-5-9200 is used in the system.
9	Digit Keyboard Disable Output	The digit keyboard must be disabled while information is being transferred from the Store chip to the Push Button Dialler during a Retrieve operation. This output goes to a logic '0' during this period. In a single keyboard system this output is the one to be used.
10	Address Keyboard Disable Output	The address keyboard is to be disabled, both during a Retrieve operation when information is being transferred between chips and during the Store operation after an address has been allocated, until the Store operation is finished. This output goes to a logic '0' during these periods.
11	Power-On-Reset Input	An initial reset is required for clearing the chip when power is initially applied. This input must be held at a logic '0' initially, going to a logic '1' to activate the chips.
12	Common Key Output	This output is fed directly to the Common Key input of the associated AY-5-9100 Push Button Dialler and goes to a logic '0' to indicate a valid code signal. It controls the routing of data into the AY-5-9100. (See Function Description for further details.)
13-16	C_1 C_2 C_3 C_4	Data Input/Outputs. These four lines are connected to the system. Address and dialled digit information is input on these pins and dialling information is fed out from these pins to the Push-Button Dialler. The standard keyboard code accepted by the AY-5-9200 is shown below. When outputting information, the output is normally at a logic '1' and goes to a logic '0' for a data bit.

NOTE:
Chip Select, Retrieve, Control Logic Enable and an address can all be applied simultaneously to the Store Chip. Also Store and Control Logic Enable signals can be applied simultaneously.

KEYBOARD CODE

Digit	No. of Impulses	Code			
		C_1	C_2	C_3	C_4
1	1	1	1	1	1
2	2	1	1	1	0
3	3	1	1	0	1
4	4	1	0	1	1
5	5	1	0	1	0
6	6	1	0	0	1
7	7	0	1	1	1
8	8	0	1	1	0
9	9	0	1	0	1
0	10	1	1	0	0
Access Pause		0	0	1	1

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} . . . . . −20V to +0.3V
Storage temperature range. . . . . −65°C to +150°C
Ambient operating temperature range . . . . −55°C to +80°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS}=OV
Vϕ=−15±1.5V (see fig. 1 for waveform)
Clock frequency=18 KHz
Operating Temperature (T_A)=−55°C to +80°C
Negative logic conventions are followed for this data sheet.

Characteristic	Min.	Typ.**	Max.	Units	Conditions
Clock					
Logic '0' level	+0.3	—	−1	Volts	Note 1
Logic '1' level	−13.5	—	−16.5	Volts	
Frequency	10	18	30	KHz	
Rise Time (Tr)	0.1	—	4	μs	
Fall Time (Tf)	0.1	—	8	μs	
Width (Tw)	5	—	40	μs	At logic '1' min. level
Separation (Ts)	5	—	40	μs	At logic '0' max. level
Capacitance	—	70		pF	Per phase Vϕ=OV, f=1MHz (Note 2)
Leakage	—	—	10	μA	Vϕ=16.5V, T_A=25°C
Inputs					
Logic '0' level	+0.3	—	−1	Volts	
Logic '1' level	−5	—	−16.5	Volts	
Capacitance	—	—	5	pF	V_{IN}=OV, f=1MHz
Leakage	—	—	1	μA	V_{IN}=−16.5V, T_A=25°C
Common Key Input					
Pulse Width (Tc)	10	—	—	ms	At logic '0' max. level see fig. 2
Reset Input					
Pluse Width (Td)	3	—		ms	After clocks reach full amplitude
Fall Time (Te)	—	—	100	μs	Fig.2
Anti-bounce on all Inputs except Chip Select & Reset	4.2	—	—	ms	
Outputs					
All outputs including C_1 to C_4 when acting as outputs					
Logic '0' output current	0.6	—	—	mA	V_0=−1V
Logic '1' output leakage	—	—	10	μA	V_0=−10V
Digit Output Rate	—	8.35	—	Hz	
Power	—	2.25	—	mW	

**Typical values are at +25°C and nominal voltages.

NOTES:
1. Clock logic '0' levels should be within 0.5V of each other.
2. The effective dynamic clock capacitance while operating is 260pF.

TIMING DIAGRAMS

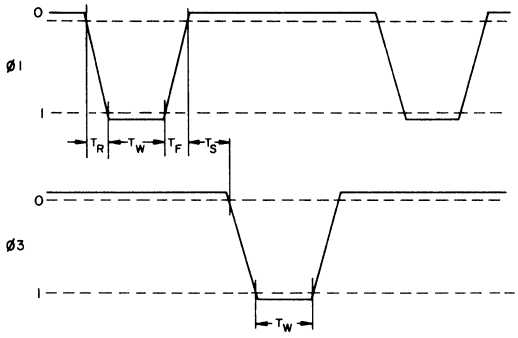


Fig.1 CLOCK WAVEFORMS

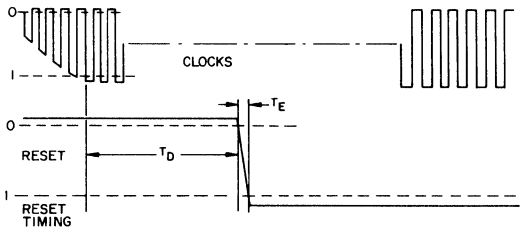


Fig.2 CLOCK WAVEFORMS WITH RESET TIMING

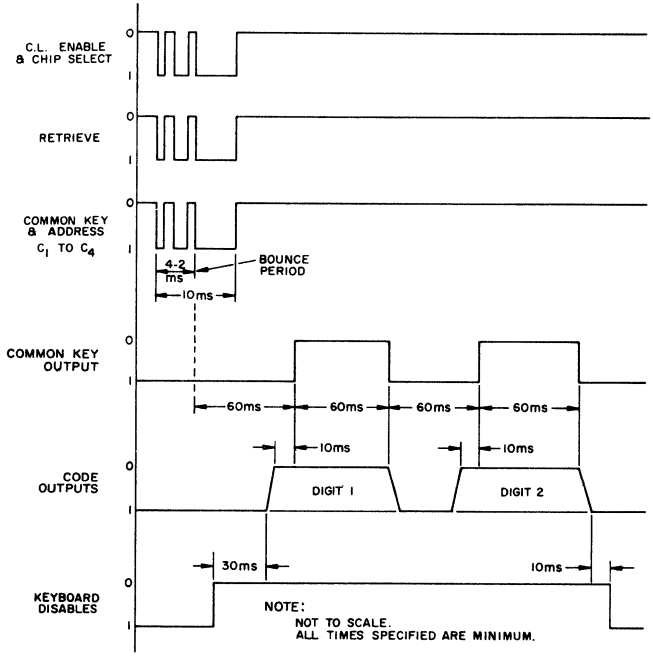


Fig.3 "RETRIEVE" WAVEFORMS

FUNCTION DESCRIPTION

The following description applies to a Push Button Repertory Dialler using the AY-5-9100 and AY-5-9200 circuits. The system provides normal push button telephone facilities with access pause and redialling, together with a repertory dialling store expandable in blocks of 10 numbers.

The AY-5-9100 is a standard Push Button Dialler circuit with normal dialling and redialling facilities. It also has the capability of storing access pauses and waiting until a dial tone is detected by external circuitry before dialling is recommenced. This chip can operate by itself when a storage facility is not required. A detailed description of this device is contained in the AY-5-9100 data sheet.

The AY-5-9200 contains all the control logic and store facility required to store ten telephone numbers. Each number may be up to 22 characters in length, each character being either a digit or access pause; a dynamic memory technique being used for the data storage. Digits, access pauses and memory addresses are entered into the AY-5-9200 as 4-bit codes on 4 input/output pins which are also connected to the digit input pins of the AY-5-9100 as in Figs.4 and 5. While data is being transferred between the AY-5-9200 and the AY-5-9100, the keyboards are externally disabled by signals generated by the AY-5-9200, so that further key depressions have no effect until the transfer of data has been completed. Further address inputs are inhibited until the call is terminated.

The digit keyboard common key output is routed through the control logic and depending on the state of the logic, the Common Key output to the Push Button Dialler chip is enabled or disabled. This prevents digits to be stored and memory addresses from entering the Push Button Dialler.

The Common Key output from the AY-5-9200 is controlled as follows:

	C.S.	C.L.E.	
Logic Level	'0'	'0'	Common output is a direct replica of Common input and digits are dialled directly by the AY-5-9100
Logic Level	'1'	'1'	Common signals to the Push Button Dialler are generated only as a number is being retrieved (see Fig. 3). After a retrieve operation, Common signals are gated through, allowing further dialling unless externally inhibited.
Logic Level	'0'	'1'	No Common signals are generated and the output device goes off.

The control logic operates so that the first key depression at the beginning of an operation determines the subsequent sequence. Invalid key depressions at a later stage in a sequence are then ignored by the control logic.

The system is expanded by connecting further AY-5-9200 chips to the busses and using the Chip Select input to enable the required chip.

When a separate address keyboard is to be used an address keyboard strobe can be fed to the 'Retrieve' input, thus allowing a single button depression when retrieving a number from the store.

OPERATION MODES

1. STORE OPERATION

DEPRESS STORE

This sets the logic into a store mode. This signal must be present throughout the store operation. Thus, either electrical or mechanical bistable switching is required, or the 'Store' button must remain depressed during the sequence. The Control Logic Enable and Chip Select inputs should be activated at the same time. The Common Key output is inhibited and the address and digit codes are routed into the AY-5-9200 chip. The order of application of the signals is not important, they may be applied simultaneously with Address if required.

DEPRESS ADDRESS (one digit)

The address code, if valid, is latched and the memory location associated with this address is cleared to prevent corrupting the new number with old information. The Common Key output remains disabled. The Address Keyboard is also disabled for the remainder of the Store operation.

ENTER NUMBER DIGITS (and Access Pauses)

The number to be stored is then entered using the digit keyboard, and is stored in the addressed location. The maximum allowable number of digits or access pauses is 22. Chip select must be at logic '1' during digit entry.

RELEASE STORE, CONTROL LOGIC ENABLE AND CHIP SELECT

This is accomplished by re-setting the electrical or mechanical bistable or releasing the Store button. The control logic is then reset and disabled.

2. RETRIEVE OPERATION

DEPRESS RETRIEVE

For separate address keyboard systems, this signal can be generated automatically with the address. The control logic is set in a retrieve mode and the address inputs are enabled. Control Logic Enable and Chip Select must be at logic '1' for the whole of the Retrieve operation, including the data transfer period. The Retrieve input must be returned to logic 'O' before the end of data transfer to prevent a repeat operation.

DEPRESS ADDRESS (Digit)

The address is decoded and latched, both keyboard disable outputs go active, disabling the keyboards. After a minimum period of 60mS, the first digit code is transmitted to the Push Button Dial chip together with a Common signal. The Common is stable for a minimum period of 60mS, the Common only being present while the code is stable. The data transmission continues at 60mS on, 60mS off until the whole number has been transferred, after which the chip is reset, the keyboard disable signals are removed and the Common signal is enabled to the Push Button Dialler chip. (See Fig. 3.)

3. ERASE OPERATION

This operation is basically a Store operation with no digits being input.

DEPRESS STORE

This sets up the logic as in the Store operation.

DEPRESS ADDRESS (Digit)

This then clears the decoded address.

RELEASE STORE

This is accomplished either by releasing 'Store' input, or resetting the mechanical or electrical 'Store' bistable.

4. RECALL AND NORMAL DIALLING

These are performed as for the Push Button Dialler on its own. See AY-5-9100 data sheet for full description.

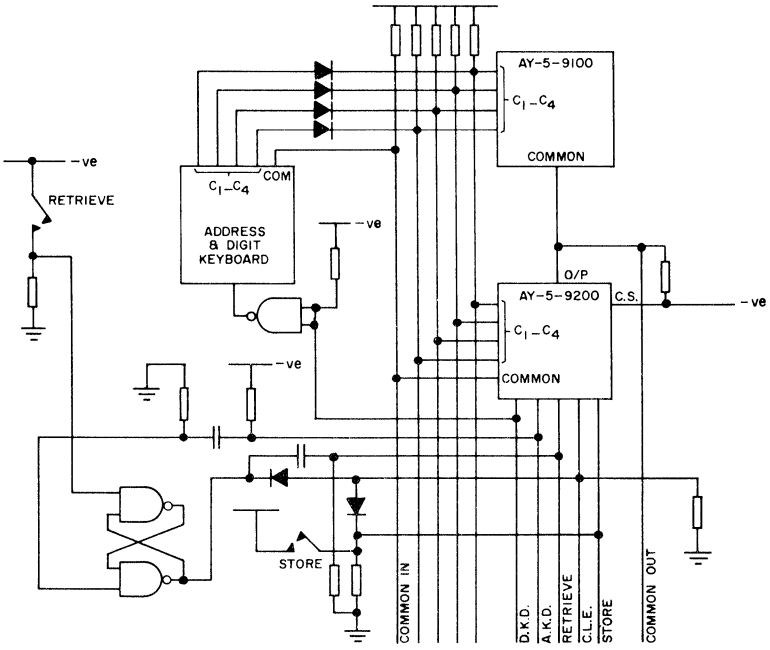


Fig.4 SINGLE KEYBOARD SYSTEM FOR REPERTORY DIALLER

Note for Figs.4 and 5
Logic: CD4011A (C-MOS)
Resistors: 100K
Capacitors: 0.1uF
Diodes: 1N914

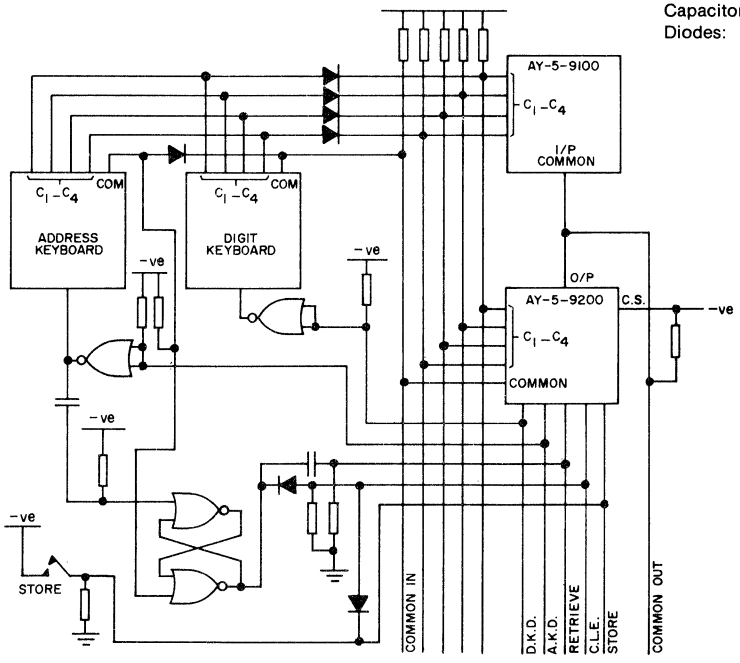


Fig.5 DUAL KEYBOARD SYSTEM FOR REPERTORY DIALLER

Telephone Coinbox Circuit

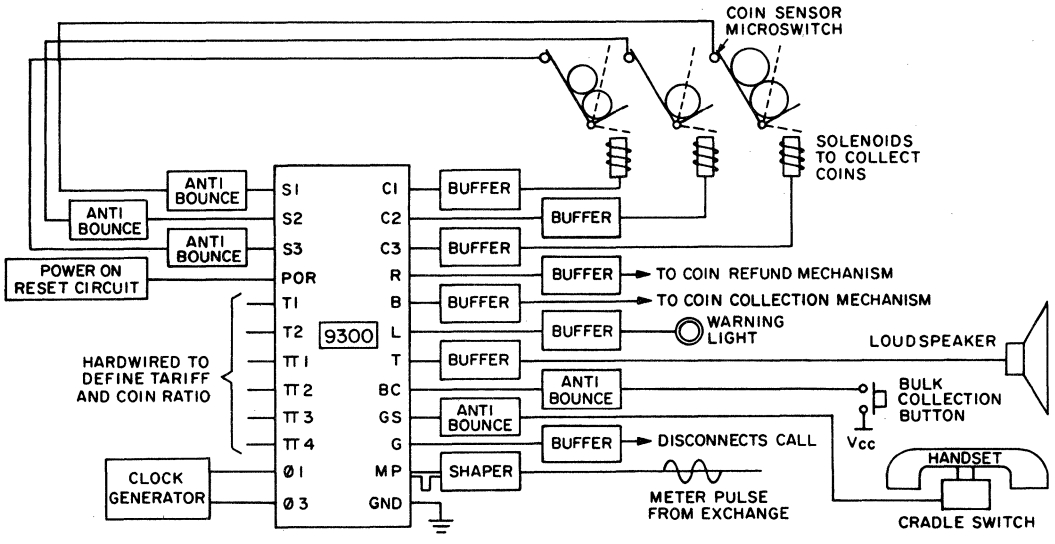
FEATURES

- Up to three coin denominations recognized.
- 16 coin value ratios selectable.
- 8 tariff rates selectable.
- Tone outputs for switch-on, coin input, bulk collect, last pay period, cut-off.
- Lamp outputs for last coin and last pay period.

DESCRIPTION

The AY-5-9300 is a P-Channel MOS integrated circuit designed to control the operation of a standard coinbox telephone. The device registers the insertion of coins and automatically debits the sum when a meter pulse is received. Lamp and tone signals are provided to inform the user and the exchange of the progress of the call. The use of four-phase dynamic logic provides very low power dissipation (2 mW typical). The AY-5-9300 is offered in a 24 pin dual-in-line package.

BLOCK DIAGRAM



TYPICAL COIN COLLECTION SYSTEM

Dual Tone Multi-Frequency Generator

FEATURES

- No tuning required, inherent accuracy±0.25%
- Uses low cost ceramic resonator
- 12 tone pairs (16 tone pairs and choice of high group pre-emphasis with AY-3-9410)
- Total harmonic distortion less than 5%
- Instant generation of tone outputs
- Low voltage drop
- Low power consumption (less than 35mW)
- Good thermal and voltage stability
- Keyboard lock out inhibits output if more than one key depressed
- N-channel ion implant construction
- High group pre-emphasis fixed at 3.52dB (6dB pre-emphasis available with AY-3-9410)
- Pre-emphasis can be varied by simple component adjustment.

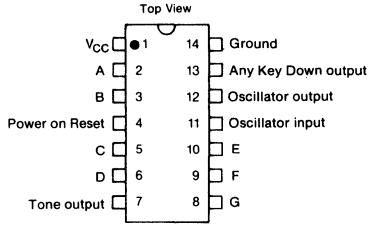
DESCRIPTION

The AY-3-9400/9410 MF Dialler generates all the tone pairs required for multifrequency touch tone dialling. The tones are generated from a single ceramic controlled master oscillator, ensuring high accuracy and stability of the output frequencies and eliminating the need for any adjustments. The digitally synthesised tones give precisely controlled characteristics.

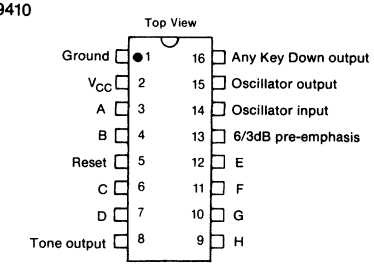
The AY-3-9400/9410 is fabricated using the ion implant N-channel low voltage process, and employs novel logic techniques to minimize power consumption and voltage drops. The circuit is suitable for operation direct from telephone line power, or it can be used with main power or battery supplies.

PIN CONFIGURATION

14 LEAD DUAL IN LINE
AY-3-9400



16 LEAD DUAL-IN-LINE
AY-3-9410



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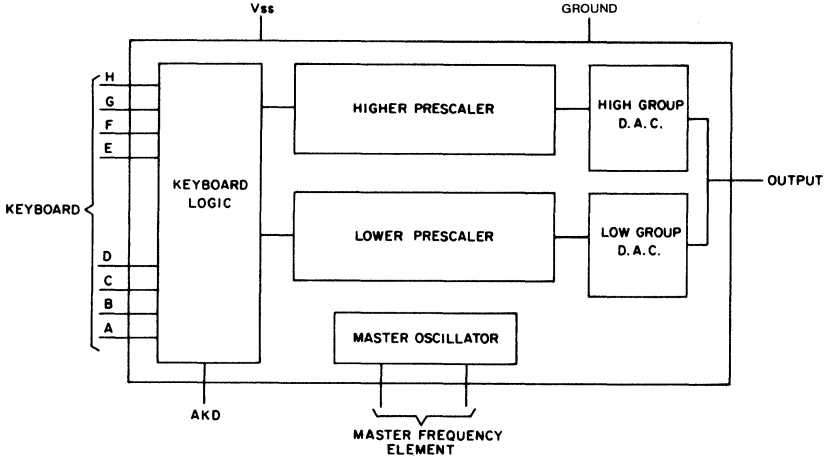


AY-3-9410

7

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to ground pin . . . . +10V to —0.3V
Storage temperature range . . . . . —65°C to +150°C
Ambient operating temperature range. . . . . —55°C to +80°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +3.5 to +8V
Fclock = 559.7KHz
Operating Temperature (T_A) -55°C to +80°C

Characteristic	Min	Typ**	Max	Units	Conditions
Input Logic '1'	+3.3	—	+8	Volts	logic '1' activates tone
Input Logic '0'	—0.3	—	+0.4	Volts	
Input pull down resistance	20	—	100	Kohm	resistor to ground
Input capacitance	—	—	10	pF	
Tone output Low Group	—	0.566	—	Vrms	V_{CC} = 4V, Note 1, Note 3
Tone output High Group	—	0.85	—	Vrms	V_{CC} = 4V, Note 1, Note 3
High group pre-emphasis	—	3.52	—	dB	
Output impedance	—	—	500	ohms	Note 2, Note 3
Any Key Down output					
On resistance	—	—	1	Kohm	Vout = +1V
Off Leakage	—	—	10	μA	Vout = +8V
Total Distortion	—	—	—23	dB	
Harmonic component	—	—	—30	dB	
Supply current	—	—	8	mA	V_{CC} = +3.5V
	—	—	10	mA	V_{CC} = +8V

**Typical values are at +25°C and nominal voltages.

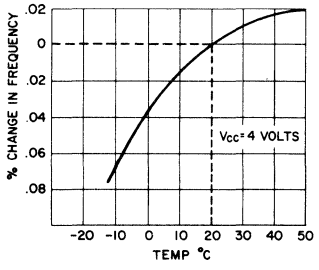
NOTE :
1. The amplitudes of the output signals are directly related to the V_{CC} supply voltage.
2. The chip output is intended to drive a low pass filter having an input impedance of greater than 8K ohms.
3. The output would be buffered to drive the line, the buffer can be arranged to have either a high impedance current output or a low impedance voltage output (See Figs.2a and 2b).

FREQUENCY OUTPUTS

All output frequencies are derived from a 559.7KHz master oscillator.
The output frequencies are as follows:

	Nominal frequency Hz	Actual Frequency Hz	Error %	Key
Low Group	697	695.28	—0.25	A
	770	768.82	—0.15	B
	852	850.61	—0.16	C
	941	940.68	—0.03	D
High Group	1209	1211.48	+0.21	E
	1336	1332.62	—0.25	F
	1477	1478.69	—0.25	G
	1633	1631.78	—0.07	H

TYPICAL CHARACTERISTIC CURVES



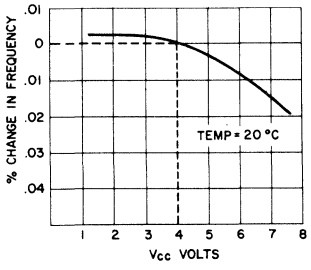


FIG1. OSCILLATOR CHARACTERISTICS

OPERATION

When a key is pressed the chip will immediately start operating, the output tones both starting from zero on the first negative half cycle. The first cycle will be of full amplitude assuming the power supply is at the correct level. If power is applied at the same time as a key is pressed, the power on reset circuit will operate, preventing spurious outputs.

When two or more keys are pressed together, one or both tones will be switched off. The tones will start from zero as soon as the extra keys have been released. When all keys are released, the tone outputs will immediately cease.

If only one key contact is made, a single tone corresponding to the closed contact will be output. The "Any Key Down" output goes to logic 'O' as soon as a key depression is recognized.

The tones are output on a single pin, as a mixture of pulse width moulated, constant amplitude square waves. This output signal is constructed into resultant sine waves in the external low pass filter. The approximation chosen yields a total harmonic distortion of less than 8%.

The amplitude of the output signal is directly proportional to the V_{CC} supply voltage.

A low pass filter buffer amplifier is used to remove switching noise and interface the tones to the line. There is an option of either the low impedance, constant voltage buffer (see fig.2a) or the higher impedance, constant current output (see fig. 2b).

NOTE:
Pre-emphasis selection for the AY-3-9410: Connect pin 13 to V_{CC} for 3dB high group pre-emphasis, or to ground for 6dB premphasis. The circuit is otherwise identical in operation to the AY-3-9400.

PERIPHERAL CIRCUITS

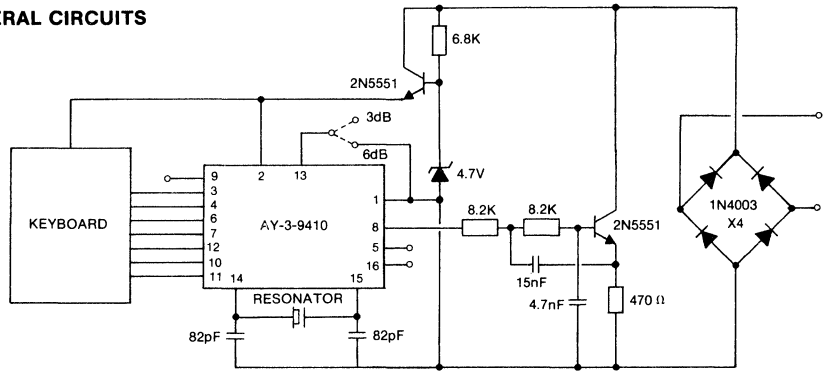


Fig.2a HIGH IMPEDANCE BUFFER

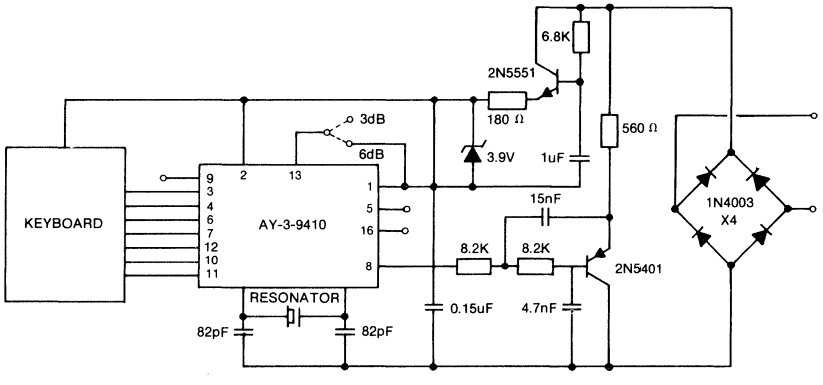


Fig. 2b LOW IMPEDANCE BUFFER

C-MOS Clock Generator

FEATURES

- Generates 2 phase clock from single power supply
- Operates with AY-5-9100 Push Button Dialler and AY-5-9200 Repertory Dialler
- Very Low power consumption, allowing use of line powered telephones
- Minimizes external components in Push Button Telephones
- Stable generation of clock frequencies

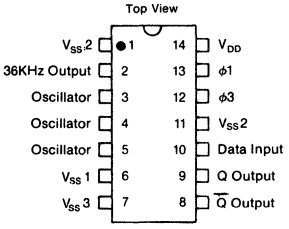
DESCRIPTION

The AY-5-9500 is a C-MOS circuit designed to generate the 2 phase clock required by the AY-5-9100 Push Button Telephone chip and the AY-5-9200 Repertory Dialler circuit.

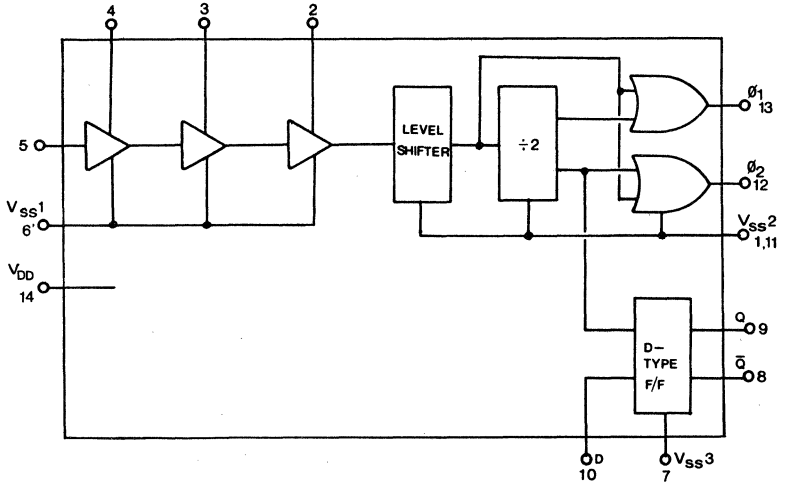
It consists of an RC oscillator, a level shifter, a 2 phase clock generator and driver, and a clocked D-type bistable. The RC oscillator is set by external components to run at 36KHz and is normally operated from a 4 Volt supply to minimise power consumption. The oscillator output is shifted and used to drive the 2 phase clock generator which is normally run on a 14 Volt supply. The D-type bistable is either used as a Reset generator for the AY-5-9100, or it is used to drive a Cockroft-Walton voltage multiplier to generate the 14 Volt supply.

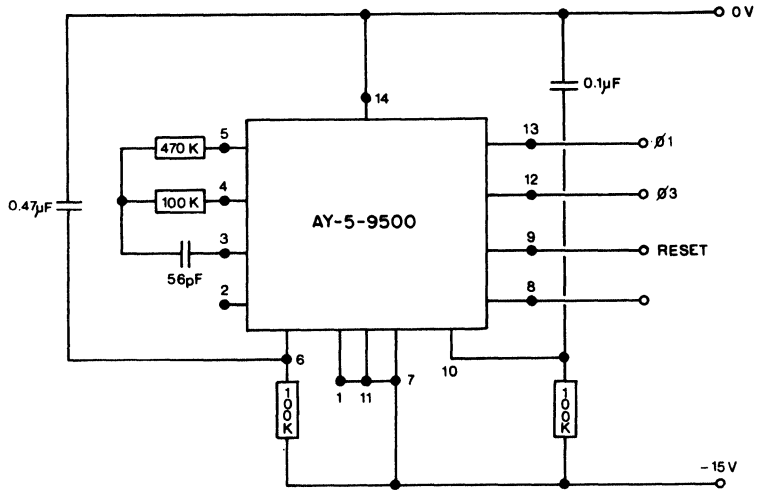
PIN CONFIGURATION

14 LEAD DUAL IN LINE

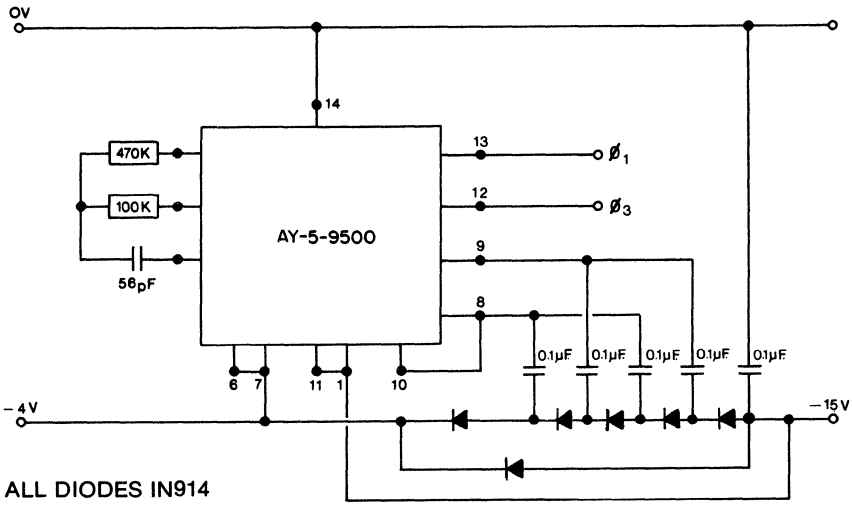


BLOCK DIAGRAM





SINGLE SUPPLY OPERATION



DC-DC CONVERTOR CONNECTION

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{DD} pin . . . . . −15V to +0.3V
Storage temperature range. . . . . −65° C to +150° C
Ambient operating temperature range . . . . . −55° C to +80° C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

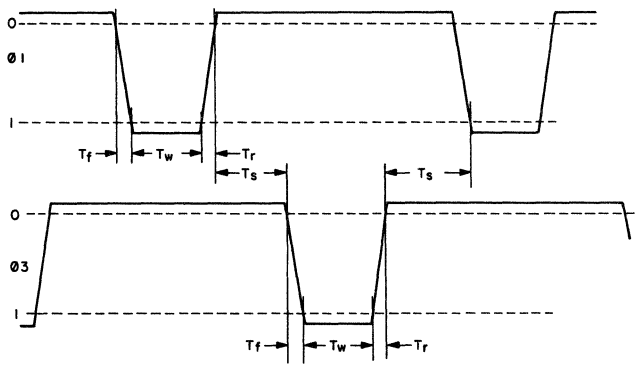
Standard Conditions (unless otherwise noted)

V_{DD} = OV
$V_{SS}1$ = −4 to −15V
$V_{SS}2$ = −4 to −15V
$V_{SS}3$ = −4 to −15V
F Clock = 36KHz ± 10%
Operating Temperature (T_A) = +20° C

Parameter	Min	Typ**	Max	Units	Conditions
CLOCK OUTPUTS					
Rise Time (Tr)	—	90	200	nS	At 360pF load
Fall Time (Tf)	—	120	250	nS	At 360pF load
Width (Tw)	10	—	—	μS	At 36KHz
Separation (Ts)	10	—	—	μS	At 36KHz
Stability	—	—	±5	%	With supply and temperature
OUTPUT 'ON' RESISTANCE					
$\phi 1, \phi 3$	—	0.3	2	KOhm	$V_{SS}2$ = −4V
Q, $\overline{Q}$	—	200	750	Ohm	$V_{SS}3$ = −4V
SUPPLY CURRENT					
At $V_{SS}1$	—	130	200	μA	$V_{SS}1$ = −4V
At $V_{SS}2$	—	100	200	μA	$V_{SS}2$ = −15V, 10pF load
At $V_{SS}3$	—	30	50	μA	$V_{SS}3$ = −15V

** Typical values are at +25° C and nominal voltages.

TIMING DIAGRAM



Multi-Frequency Receiver

FEATURES

- No tuning required; inherent discrimination, better than ± 0.1%.
- Digitally defined bandwidths with no inherent voltage or temperature drift.
- Fast aquisition of tones (typ. 15mS).
- Frequency correlation provides good S/N performance.
- Many programmable features provide wide applications.
- High reliability and low cost using P-channel process.
- On-chip analog amplifiers for analog preprocessing.
- Interfaces directly with the AY-5-9100 for M.F.—Strowger converters.
- Handshaking facility to interface directly with CP1600 microprocessor.
- Three-State code outputs.

DESCRIPTION

The AY-5-9800 is fabricated in P channel MTNS process thus minimizing cost and providing high reliability. The basic chip diagram is shown below. For analog preprocessing six amplifiers and two source followers are included on-chip, external components being used to determine the filter characteristics. The major functions are mask programmable thus giving a flexible system at a low cost.

The tone pair is separated into two individual tones using the analog circuitry, the separated tones being applied to the Schmidt triggers to square incoming signals which are then processed by the digital circuitry. The high and low group logic is similar; only the decode values for frequency recognition are different. The incoming signal is divided by two or three to eliminate the effects of changing mark/space ratio and its period counted by a timer which is clocked by the accurate 1MHz clock. If the period value is within encoded limits, the result is stored. Five cycles of incoming signal are stored and a decision is made with this information as to whether the tone is valid. A programmable logic array scans the five cycle store for both an "Acquire" criteria and "Release" criteria. If the "Acquire" criteria is exceeded (e.g. 4 out of 5), and the "Release" criteria is not reached (e.g. less than 2 out of 5), the frequency is deemed to be valid. If both high and low frequencies are detected, a time-out timer is started. This timer is mask programmable and will normally require 25mS of valid tone pair signal. Once this period has elapsed the Common Output pulses high, again for a preprogrammed period.

The Code Outputs and Common Output can be configured for a wide variety of systems. The normal device is packaged in a 28 lead DIP and provides four Three-State Code outputs suitable for microprocessor controlled systems and direct interfacing to the AY-5-9100 for MF-Strowger converters. Alternatively a 40 lead DIP device provides sixteen Three-State Outputs for direct MF receiver replacement. A hand-shaking interface is provided using the Interrogate input thus allowing very simple microprocessor interfacing. The outputs will directly drive low power TTL, CMOS or MOS and, being Three-State, can be bussed in large systems.

Input Clock—The recommended clock frequency is 1MHz which will then give a frequency detect range of 620—3400Hz with a discrimination of ±1 μS. Alternatively, the device can be reprogrammed to other clock frequencies above 10KHz as available. The discrimination of 1633Hz using a 1MHz clock will be better than ±0.1%. Any deviation of the 1MHz clock will result in a proportional deviation of the tone recognition bands.

Power-On-Reset—An external power-on reset is required which is used to reset all counters, etc. An on-chip resistor pulls this input to V_{SS}; and 0.1μF capacitor connected from the P.O.R. input to V_{DD} will provide automatic power-on-reset. This input can be used as a chip select putting all Three-State outputs into their high impedance state when held low.

Input Amplifiers—Input amplifiers are suitable for use in band-pass and general buffer amplifiers. They have an open loop gain of approximately 500 and are trimmed by a single 'Bias Input'.

Period Counters—The input frequency is interrogated by the period counter. Each counter has eight values decoded, these representing F1 low limit, F1 high limit, etc. Once a positive going edge is detected, the period counter is started and if the next positive going edge occurs during a time slot decode, the circuit deems the tone to be valid and a bistable indicating the tone decoded is set. Special logic is incorporated to prevent the counter from being continuously triggered in the presence of noise.

Status Register—The Status Register is a five bit register which is filled with 1's for an in-band signal but filled with 0's for out-of-band signals. With the data in this register a decision is performed which sets a bistable (Acquires the signal) or resets a bistable (Releases the signal). Thus by changing the preprogrammed acceptance standard, a direct trade-off between S/N ratio and stimulation rate can be obtained for different systems.

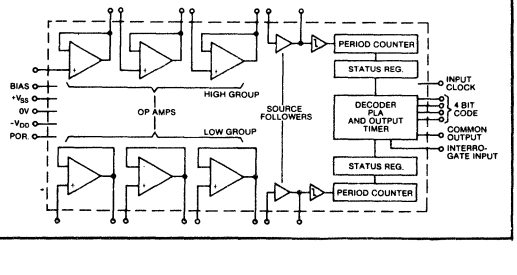
Output Logic—Once both high and low group tones have been detected valid, a preprogrammed timer is started. If the tone pair is still valid after the timer has counted out, the Common Output goes high for a preprogrammed period and the Code Outputs present the programmed outputs corresponding to the tone pair input.

If the Interrogate input is used for handshaking, the Code Outputs are only presented after the Interrogate input goes high; the interrogate input going low removes both the Codes and the Common Output.

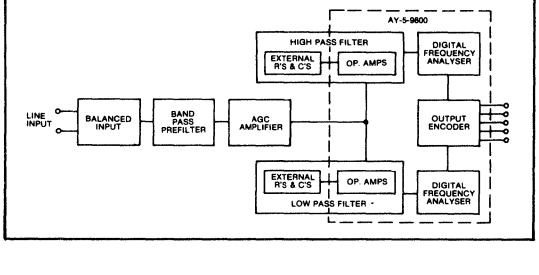
PROGRAMMABLE OPTIONS These options can all be provided by a single layer mask change.

- Programmable center frequencies
- Programmable accuracies
- Variable "Acquire" criteria (1 out of 5 to 5 out of 5)
  Variable "Release" criteria (1 out of 5 to 5 out of 5)
- Normally arranged for 2 of 8 detection, but can be reprogrammed for single tone (1 of 8) detection.
- Common output can be delayed by 1-32 mS after tones are detected valid.
- Common output pulse can be programmed from 1-31mS
- Output code can be any 4 bit code in 28 lead DIP or any 16 bit code in 40 lead DIP (e.g. 2 of 7, 1 of 12 etc.).

BLOCK DIAGRAM



SYSTEM DIAGRAM



GENERAL INSTRUMENT

AY-5-1013
AY-5-1013A
AY-6-1013
AY-3-1014A
AY-3-1015
AY-5-1016
AY-6-4016

8

UAR/T Universal Asynchronous Receiver/Transmitter

FEATURES

- DTL and TLL compatible—no interfacing circuits required—drives one TTL load.
- Fully Double Buffered—eliminates need for system synchronization, facilitates high-speed operation.
- Full Duplex Operation—can handle multiple baud rates (receiving-transmitting) simultaneously.
- Start Bit Verification—decreases error rate with center sampling.
- Receiver center sampling of serial input; 46% distortion immunity.
- High Speed Operation.
- Three-State Outputs—bus structure capability.
- Low Power-minimum power requirements.
- Input Protected—eliminates handling problems.

AY-5-1013/1013A
- GIANT P-channel nitride process.
- 0 to 30kbaud/0 to 40kbaud.
- Pull up resistors to V_{CC} on all inputs.

AY-6-1013
- GIANT P-channel nitride process.
- 0 to 20kbaud.
- Extended Operating Temperature Range:
  -40° C to +85° C (plastic package)
  -55° C to +125° C (ceramic package)
- Pull-up resistors to V_{CC} on all inputs.

AY-3-1014A/1015
- Single Supply Operation:
  +4.75V to +14V (AY-3-1014A)
  +4.75V to +5.25V (AY-3-1015)
- CMOS compatible (AY-3-1014A).
- 1½ stop bit mode.
- External reset of all registers.
- GIANT II N-channel Ion Implant Process.
- 0 to 30kbaud.
- Pull-up resistors to V_{CC} on all inputs (AY-3-1015).

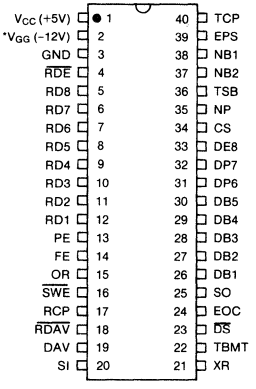
DESCRIPTION

The Universal Asynchronous Receiver/Transmitter (UAR/T) is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, one or two stop bits (1½ stop bit capability with the AY-3-1014A/1015), and either odd/even parity or no parity. In order to make the UAR/T universal, the baud, bits per word, parity mode, and the number of stop bits are externally selectable. The device is constructed on a single monolithic chip. All inputs and outputs are directly compatible with MTOS/MTNS logic, and also with TTL/DTL/CMOS logic without the need for interfacing components. All strobed outputs are three-state logic.

PIN CONFIGURATION

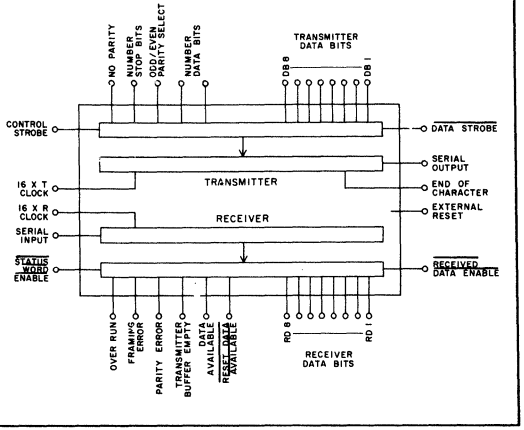
40 LEAD DUAL IN LINE

Top View



*Pin 2: AY-3-1014A/1015 — No Connection.

BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Name (Symbol)	Function
1	V_{CC} Power Supply (V_{CC})	+5V Supply
2	V_{GG} Power Supply (V_{GG})	−12V Supply (Not connected for AY-3-1014A/1015)
3	Ground (V_{GI})	Ground
4	Received Data Enable ($\overline{RDE}$)	A logic "O" on the receiver enable line places the received data onto the output lines.
5-12	Received Data Bits (RD8-RD1)	These are the 8 data output lines. Received characters are right justified: the LSB always appears on RD1. These lines have tri-state outputs; i.e., they have the normal TTL ouput characteristics when $\overline{RDE}$ is "O" and a high impedance state when $\overline{RDE}$ is "1". Thus, the data output lines can be bus structure oriented.
13	Parity Error (PE)	This lines goes to a logic "1" if the received character parity does not agree with the selected parity. Tri-state.
14	Framing Error (FE)	This line goes to a logic "1" if the received character has no valid stop bit. Tri-state.
15	Over-Run (OR)	This line goes to a logic "1" if the previously received character is not read (DAV line not reset) before the present character is transferred to the receiver holding register. Tri-state.
16	Status Word Enable ($\overline{SWE}$)	A logic "O" on this line places the status word bits (PE, FE, OR, DAV, TBMT) onto the output lines. Tri-state.
17	Receiver Clock (RCP)	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud.
18	Reset Data Available ($\overline{RDAV}$)	A logic "O" will reset the DAV line. The DAV F/F is only thing that is reset.
19	Data Available (DAV)	This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register. Tri-state. Fig.12,34.
20	Serial Input (SI)	This line accepts the serial bit input stream. A Marking (logic "1") to spacing (logic "O") transition is required for initiation of data reception. Fig.11,12,33,34.
21	External Reset (XR)	Resets all registers (except that the received data register is not reset in the AY-5-1013/1013A and AY-6-1013). Sets SO, EOC, and TBMT to a logic "1". Resets DAV, and error flags to "O". Clears input data buffer. Must be tied to logic "O" when not in use.
22	Transmitter Buffer Empty (TBMT)	The transmitter buffer empty flag goes to a logic "1" when the data bits holding register may be loaded with another character. Tri-state. See Fig.18,20,40,42.
23	Data Strobe ($\overline{DS}$)	A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of $\overline{DS}$. Data must be stable during entire strobe.
24	End of Character (EOC)	This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character. See Fig.17,19,39,41.
25	Serial Output (SO)	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic "1" when no data is being transmitted. See Fig.16.
26-33	Data Bit Inputs (DB1-DB8)	There are up to 8 data bit input lines available.
34	Control Strobe (CS)	A logic "1" on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic "1" level.
35	No Parity (NP)	A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic "O".
36	Number of Stop Bits (TSB)	This lead will select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits. For the AY-3-1014A/1015, the combined selection of 2 stop bits and 5 bits/character will produce 1½ stop bits.
37-38	Number of Bits/Character (NB2, NB1)	These two leads will be internally decoded to select either 5, 6, 7 or 8 data bits/character. NB2 NB1 Bits/Character 0 0 5 0 1 6 1 0 7 1 1 8
39	Odd/Even Parity Select (EPS)	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "O" will insert odd parity and a logic "1" will insert even parity.
40	Transmitter Clock (TCP)	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud.

TRANSMITTER OPERATION

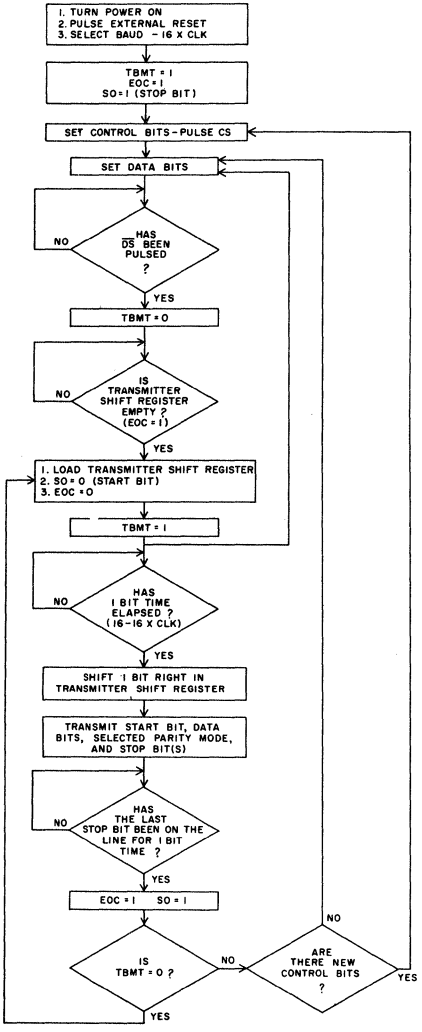


Fig.1

Initializing

Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud. The above conditions will set TBMT, EOC, and SO to logic "1" (line is marking).

After initializing is completed, user may set control bits and data bits with control bits selection normally occurring before data bits selection. However, one may set both $\overline{DS}$ and CS simultaneously if minimum pulse width specifications are followed. Once Data Strobe ($\overline{DS}$) is pulsed the TBMT signal will change from a logic "1" to a logic "O" indicating that the data bits holding register is filled with a previous character and is unable to receive new data bits, and transmitter shift register is transmitting previously loaded data. TBMT will return to a logic "1". When transmitter shift register is empty, data bits in the holding register are immediately loaded into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SO and EOC going to a logic "O", and TBMT will also go to a logic "1" indicating that the shifting operation is completed and that the data bits holding register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss in transmission speed due to double buffering (separate data bits holding register and transmitter shift register).

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired) and stop bit(s). When the last stop bit has been on line for one bit time, EOC will go to a logic "1" indicating that new character is ready for transmission. This new character will be transmitted only if TBMT is a logic "O" as was previously discussed.

RECEIVER OPERATION

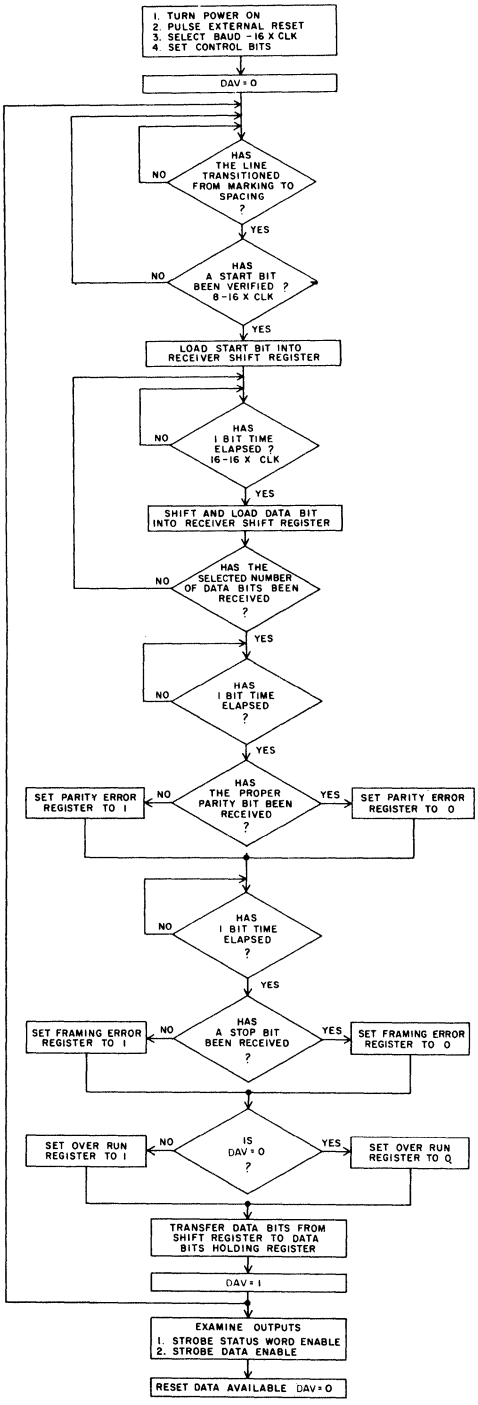


Fig.2

Initializing

Power is applied, external reset is enabled, and clock pulse is applied having a frequency of 16 times the desired baud. The previous conditions will set data available (DAV) to a logic ")".

After initializing is completed, user should note that one set of control bits will be used for both receiver and transmitter making individual control bit setting unnecessary. Data reception starts when serial input signal changes from Marking (logic "1") to spacing (logic "O") which initiates start bit. The start bit is valid if, after transition from logic "1" to logic "0", the SI line continues to be at logic "0", when center sampled, 8 clock pulses later. If, however, line is at a logic "1" when center sampling occurs, the start bit verification process will be reset. If the Serial Input line transitions from a logic "1" to a logic "0" (marking to spacing) when the 16x clock is in a logic "1" state, the bit time, for center sampling will begin when the clock line transitions from a logic "1" to a logic "0" state. After verification of a genuine start bit, data bit reception, parity bit reception and stop bit(s), reception proceeds in an orderly manner.

While receiving parity and stop bit(s) the receiver will compare transmitted parity and stop bit(s) with control data bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip flop and/or the framing error flip flop to a logic "1". It should be noted that if the No Parity Mode is selected the PE (parity error) will be unconditionally set to a logic "0".

Once a full character is received, internal logic looks at the data available (DAV) signal to determine if data has been the read out. If the DAV signal is at a logic "1" the receiver will assume data has not been read out and the over run flip flop of the status word holding register will be set to a logic "1". If the DAV signal is at a logic "0" the receiver will assume that data has been read out. After DAV goes to a logic "1", the receiver shift register is now ready to accept the next character and has one full character time to remove the received character.

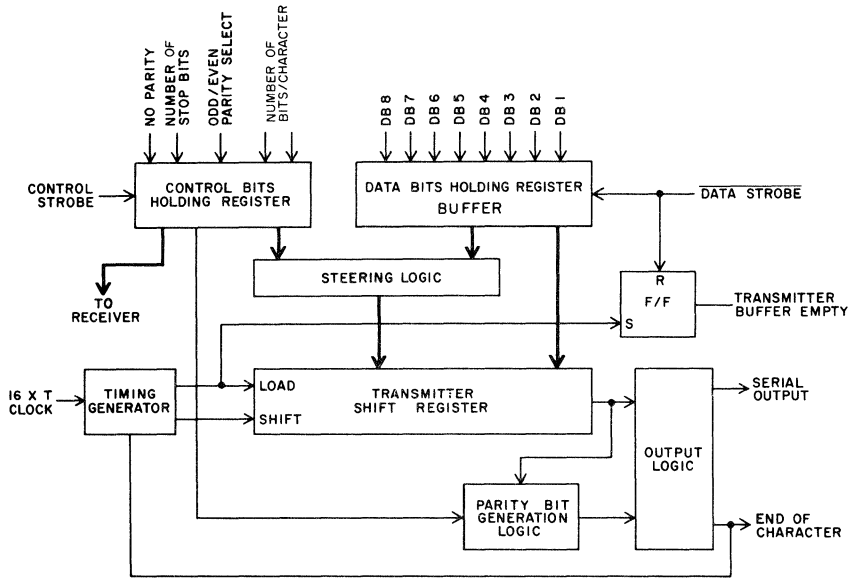


Fig.3 TRANSMITTER BLOCK DIAGRAM

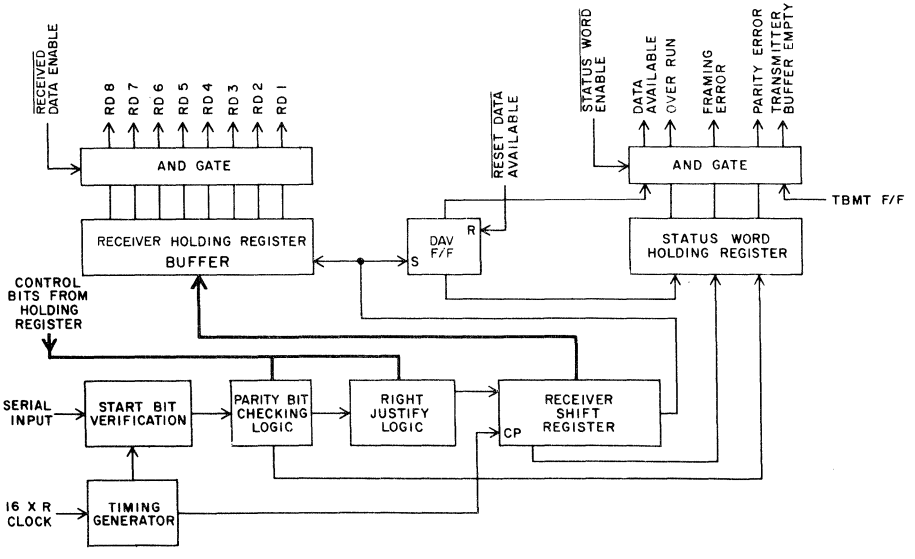


Fig.4 RECEIVER BLOCK DIAGRAM

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GG} (with respect to V_{CC}) . . . . . −20 to +0.3V
Clock and logic input voltages (with respect to V_{CC}) . . . . . −20 to +0.3V
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (soldering, 10 seconds) . . . . . +330°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

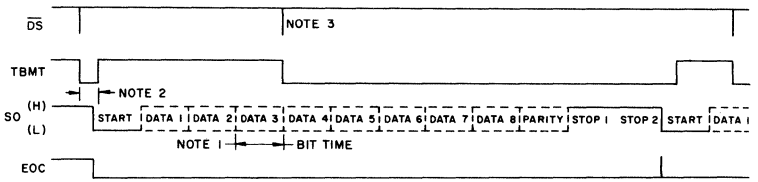
$V_{GG} = -12V \pm 5\%$
$V_{CC} = +5V \pm 5\%$
Temperature (T_A) = 0°C to +70°C (AY-5-1013/1013A)
−40 C to +85°C (AY-6-1013 Plastic Package)
−55C to +125°C (AY-6-1013 Ceramic Package)

Characteristic	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS					
Input Logic Levels					
Logic 0	0	—	0.8	volts	(1_{IL} = −1.6mA max.)
Logic 1	V_{CC} -1.5	—	V_{CC} +0.3	volts	Unit has internal pullup resistors
Input Capacitance					
All Inputs	—	—	20	pF	0 volts bias, f= 1MHz
Leakage Currents					
Three State Outputs	—	—	1.0	uA	0 volts
Data Output Levels					
Logic 0	—	—	+0.4	volts	I_{OL} = 1.6mA (sink)
Logic 1	V_{CC} -1.0	—	—	volts	I_{OL} = .3mA (source)
Output Capacitance	—	10	15	pF	
Short Ckt. Current	—	—	—	—	See Fig.25
Power Supply Current					
I_{GG} } 25°C,all inputs +5V	—	14	16	mA	AY-5-1013/1013A - See Fig.25
I_{GG} } 25°C,all inputs +5V	—	17	19	mA	AY-6-1013 - See Fig.25
I_{CC} } 25°C,all inputs +5V	—	18	20	mA	AY-5-1013/1013A - See Fig.26
I_{CC} } 25°C,all inputs +5V	—	21	23	mA	AY-6-1013
AC CHARACTERISTICS					T_A = 25°C, output load capacitance 50pF max.
Clock Frequency	DC	—	480	kHz	AY-5-1013
	DC	—	640	kHz	AY-5-1013A
	DC	—	360	kHz	AY-6-1013
Baud	0	—	30	k baud	AY-5-1013
	0	—	40	k baud	AY-5-1013A
	0	—	22.5	k baud	AY-6-1013
Pulse Width					
Clock Pulse	1.0	—	—	μs	AY-5-1013 - See Fig.9
	750	—	—	ns	AY-5-1013A - See Fig.9
	1.5	—	—	μs	AY-6-1013-See Fig.9
Control Strobe	300	—	—	ns	AY-5-1013/1013A-See Fig.15
	600	—	—	ns	AY-6-1013
Data Strobe	190	—	—	ns	AY-5-1013/1013A - See Fig.14
	250	—	—	ns	AY-6-1013
External Reset	500	—	—	ns	AY-5-1013/1013A - See Fig.13
	1.0	—	—	μs	AY-6-1016
Status Word Enable	500	—	—	ns	AY-5-1013/1013A - See Fig.21
	600	—	—	ns	AY-6-1013 - See Fig.21
Reset Data Available	250	—	—	ns	AY-5-1013/1013A - See Fig.22
	350	—	—	ns	AY-6-1013 - See Fig.22
Received Data Enable	500	—	—	ns	AY-5-1013/1013A - See Fig.21
	600	—	—	ns	AY-6-1013 - See Fig.21
Set Up & Hold Time					
Input Data Bits	0	—	—	ns	See Fig.14
Input Control Bits	0	—	—	ns	See Fig.15
Output Propagation Display					
TPD0	—	—	500	ns	AY-5-1013/1013A - See Fig.21 & 24
	—	—	650	ns	AY-6-1013 - See Fig.21 & 24
TPD1	—	—	500	ns	AY-5-1013/1013A - See Fig.21 & 24
	—	—	650	ns	AY-6-1013 - See Fig.21 & 24

**Typical values are at +25°C and nominal voltages.

8

TIMING DIAGRAMS



NOTE: SEE FIGURES 7, 8, 9 FOR DETAILS.

TRANSMITTER INITIALLY ASSUMED INACTIVE AT START OF DIAGRAM. SHOWN FOR 8 LEVEL CODE AND PARITY AND TWO STOPS.

1: BIT TIME = 16 CLOCK CYCLES.

2: IF TRANSMITTER IS INACTIVE THE START PULSE WILL APPEAR ON LINE WITHIN 1 CLOCK CYCLE OF TIME DATA STROBE OCCURS. SEE DETAIL.

3: SINCE TRANSMITTER IS DOUBLE BUFFERED ANOTHER DATA STROBE CAN OCCUR ANYWHERE DURING TRANSMISSION OF CHARACTER 1 AFTER TBMT GOES HIGH.

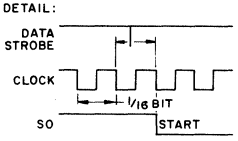


Fig.5 UAR/T TRANSMITTER TIMING

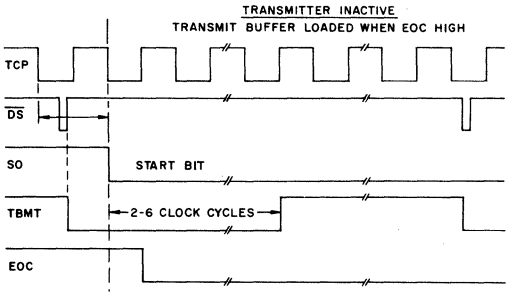


Fig.6 TRANSMITTER AT START BIT

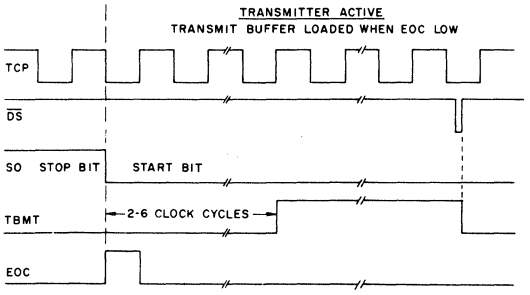
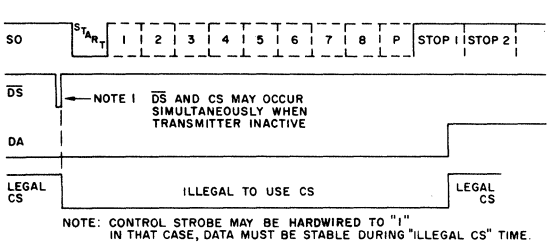
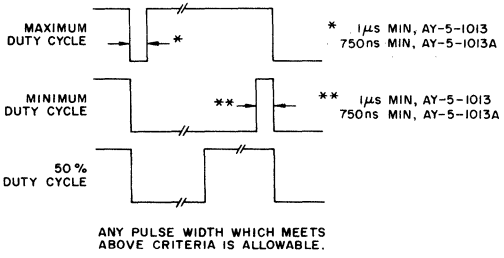


Fig.7 TRANSMITTER AT START BIT



NOTE: CONTROL STROBE MAY BE HARDWIRED TO "1" IN THAT CASE, DATA MUST BE STABLE DURING "ILLEGAL CS" TIME.

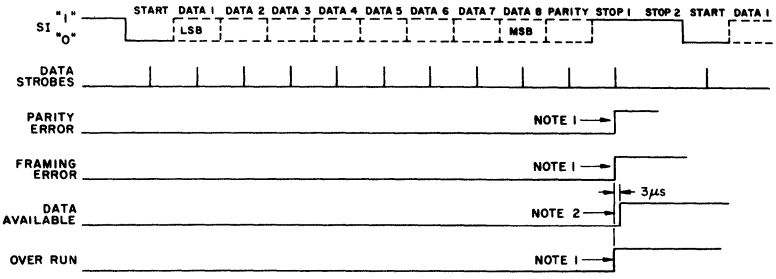
Fig.8 ALLOWABLE POINTS TO USE CONTROL STROBE



ANY PULSE WIDTH WHICH MEETS ABOVE CRITERIA IS ALLOWABLE.

Fig.9 ALLOWABLE TCP, RCP

TIMING DIAGRAMS



NOTES:
1. THIS IS THE TIME WHEN THE ERROR CONDITIONS ARE INDICATED, IF ERROR OCCURS.
2. DATA AVAILABLE IS SET ONLY WHEN THE RECEIVED DATA, PE, FE, OR HAS BEEN TRANSFERRED TO THE HOLDING REGISTERS. (SEE RECEIVER BLOCK DIAGRAM).
3. ALL INFORMATION IS GOOD IN HOLDING REGISTER UNTIL DATA AVAILABLE TRIES TO SET FOR NEXT CHARACTER.
4. ABOVE SHOWN FOR 8 LEVEL CODE PARITY AND TWO STOP. FOR NO PARITY, STOP BITS FOLLOW DATA.
5. FOR ALL LEVEL CODE THE DATA IN THE HOLDING REGISTER IS *RIGHT JUSTIFIED;* THAT IS, LSB ALWAYS APPEARS IN RDI (PIN 12).

Fig.10 UAR/T RECEIVER TIMING

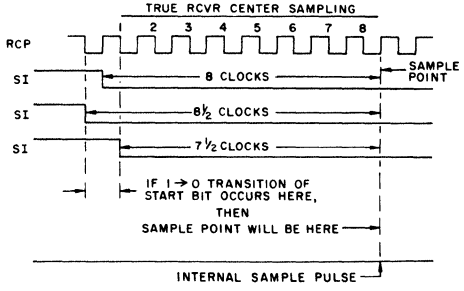


Fig.11

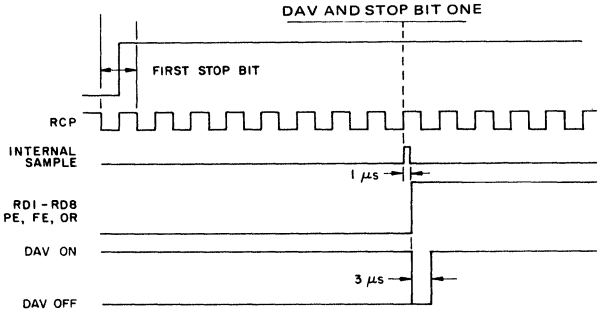
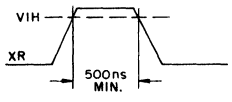


Fig.12 RECEIVER DURING 1st STOP BIT



WHEN NOT IN USE, XR MUST BE HELD AT GND.

XR RESETS EVERY REGISTER EXCEPT CONTROL REGISTER AND RECEIVED DATA. SO, TBMT, EOC ARE RESET TO 5V. ALL OTHER OUTPUTS RESET TO 0V.

Fig.13 XR PULSE

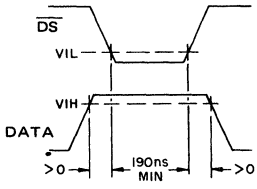
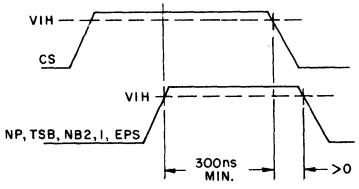
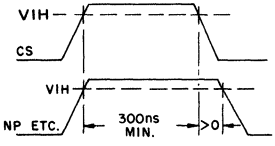


Fig.14 DS



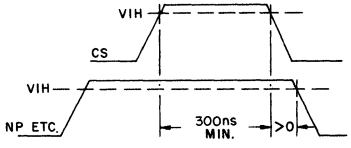
CONTROL BITS MUST BE STABLE FOR LAST 300ns OF CS.

Fig.15a CS



CONTROL STROBE AND CONTROL BITS MUST BE 300ns MINIMUM.

Fig.15b CS



LEADING EDGE OF DATA IS NOT CRITICAL AS LONG AS TRAILING EDGE AND PULSE WIDTH SPECS ARE OBSERVED.

Fig.15c CS

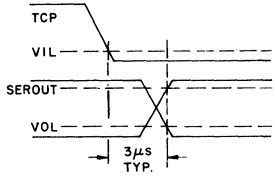


Fig.16

TIMING DIAGRAMS

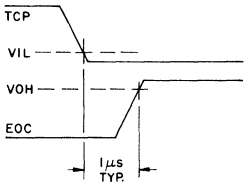


Fig.17 EOC TURN-ON

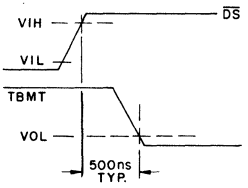


Fig.18 TBMT TURN-OFF

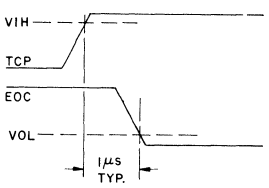


Fig.19 EOC TURN-OFF

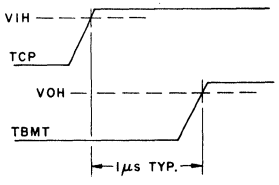


Fig.20 TBMT TURN-ON

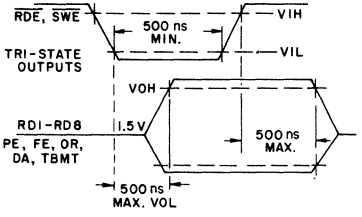


Fig.21 RDE, SWE

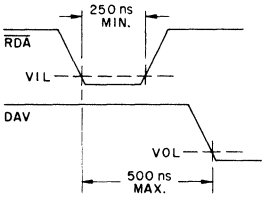


Fig.22 RDAV

TYPICAL CHARACTERISTIC CURVES

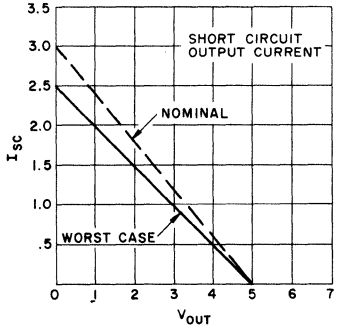


Fig.23 SHORT CIRCUIT OUTPUT CURRENT

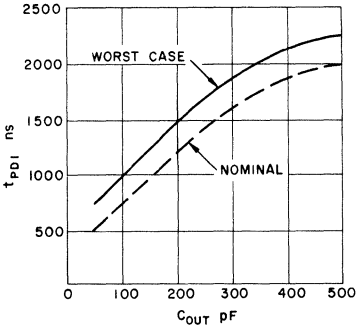


Fig.24 RE1, RD8, PE, FE, OR, TBMT, DAV

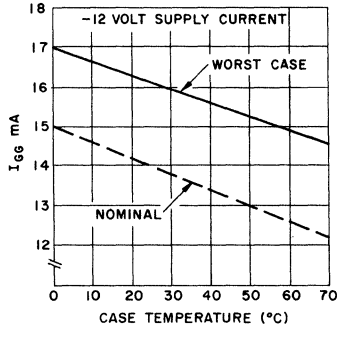


Fig.25 -12 VOLT SUPPLY CURRENT

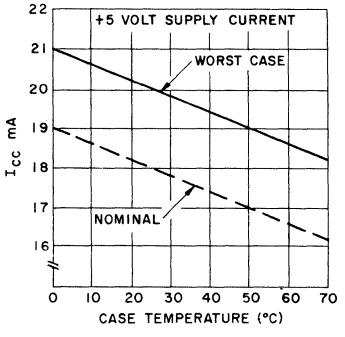


Fig.26 +5 VOLT SUPPLY CURRENT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} (with respect to V_{GI}) . . . . . −0.3 to +16V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature. . . . . 0°C to +70°C
Lead Temperature (Soldering, 10 sec) . . . . . +330°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

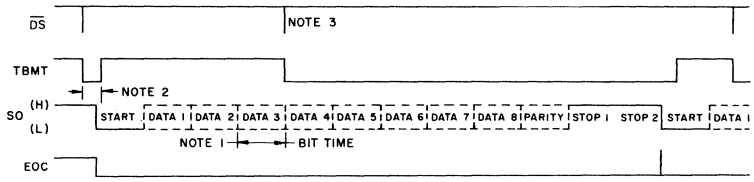
Standard Conditions (unless otherwise noted)

V_{CC} = +4.75 to +14V (AY-3-1014A)
V_{CC} = +4.75V to +5.25V (AY-3-1015)
Operating Temperature (T_A) = 0°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS					
Input Logic Levels					
Logic 0	0	—	0.8	volts	
Logic 1	2.0	—	V_{CC}+0.3	volts	AY-3-1015 has internal pull-up resistors to V_{CC}.
Input Capacitance					
All inputs	—	—	20	pF	0 volts bias, f = 1 MHz
Output Impedance					
Tri-State Outputs	1.0	—	—	MΩ	
Data Output Levels					
Logic 0	—	—	+0.4	volts	I_{OL} = 1.6 mA (sink)
Logic 1	2.4	—	—	volts	I_{OH} = -0.3 mA (source)
Output Capacitance	—	10	15	pF	
Short Ckt. Current	—	—	—	—	See Fig.45.
Power Supply Current					
I_{CC} at V_{CC} = +5V (AY-3-1014A)	—	18	20	mA	See Fig.47.
I_{CC} at V_{CC} = +14V (AY-3-1014A)	—	28	30	mA	See Fig.48.
I_{CC} at V_{CC} = +5V (AY-3-1015)	—	30	40	mA	
A.C. CHARACTERISTICS					T_A = 25°C, Output load capacitance 50 pF max.
Clock Frequency	DC	—	480	kHz	
Baud Rate	0	—	30	k baud	
Pulse Width					
Clock Pulse	3.0	—	—	μs	See Fig.31
Control Strobe	200		—	ns	See Fig.37
Data Strobe	200	—	—	ns	See Fig.36
External Reset	500	—	—	ns	See Fig.35
Status Word Enable	500		—	ns	See Fig.43
Reset Data Available	200	—	—	ns	See Fig.44
Received Data Enable	500	—	—	ns	See Fig.43
Set Up & Hold Time					
Input Data Bits	20	—	—	ns	See Fig36
Input Control Bits	20	—	—	ns	See Fig.37
Output Propagation Delay					
TPD0	—	—	500	ns	See Fig.43 & 46
TPD1	—	—	500	ns	See Fig.43 & 46

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS



NOTE: SEE FIGURES **28, 29, 30 FOR DETAILS.**

TRANSMITTER INITIALLY ASSUMED INACTIVE AT START OF DIAGRAM. SHOWN FOR 8 LEVEL CODE AND PARITY AND TWO STOPS.

1: BIT TIME = 16 CLOCK CYCLES.

2: IF TRANSMITTER IS INACTIVE THE START PULSE WILL APPEAR ON LINE WITHIN 1 CLOCK CYCLE OF TIME DATA STROBE OCCURS. SEE DETAIL.

3: SINCE TRANSMITTER IS DOUBLE BUFFERED ANOTHER DATA STROBE CAN OCCUR ANYWHERE DURING TRANSMISSION OF CHARACTER 1 AFTER TBMT GOES HIGH.

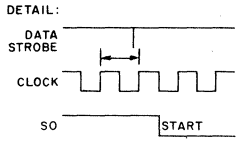


Fig.27 UAR/T-TRANSMITTER TIMING

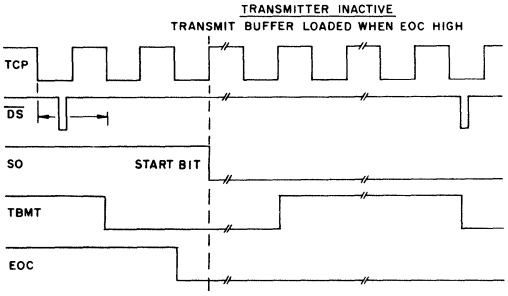


Fig.28 TRANSMITTER AT START BIT

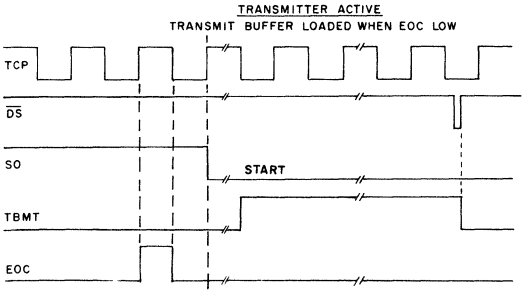
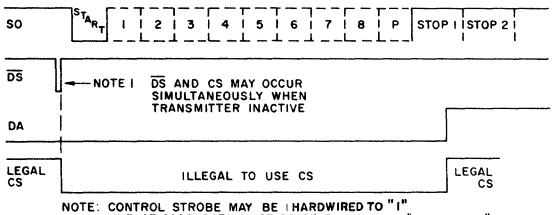
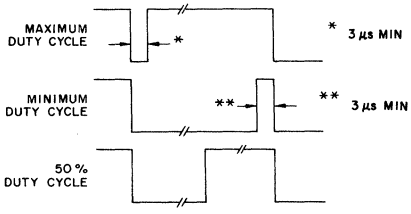


Fig.29 TRANSMITTER AT START BIT



NOTE: CONTROL STROBE MAY BE HARDWIRED TO "1" IN THAT CASE, DATA MUST BE STABLE DURING "ILLEGAL CS" TIME.

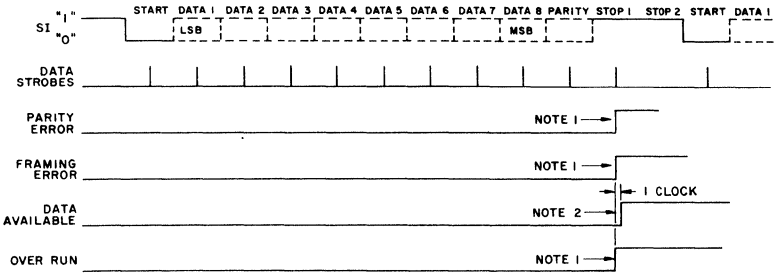
Fig.30 ALLOWABLE POINTS TO USE CONTROL STROBE



ANY PULSE WIDTH WHICH MEETS ABOVE CRITERIA IS ALLOWABLE.

Fig.31 ALLOWABLE TCP, RCP

TIMING DIAGRAMS



NOTES:

1. THIS IS THE TIME WHEN THE ERROR CONDITIONS ARE INDICATED, IF ERROR OCCURS.
2. DATA AVAILABLE IS SET ONLY WHEN THE RECEIVED DATA, PE, FE, OR HAS BEEN TRANSFERRED TO THE HOLDING REGISTERS. (SEE RECEIVER BLOCK DIAGRAM).
3. ALL INFORMATION IS GOOD IN HOLDING REGISTER UNTIL DATA AVAILABLE TRIES TO SET FOR NEXT CHARACTER.
4. ABOVE SHOWN FOR 8 LEVEL CODE PARITY AND TWO STOP. FOR NO PARITY, STOP BITS FOLLOW DATA.
5. FOR ALL LEVEL CODE THE DATA IN THE HOLDING REGISTER IS *RIGHT JUSTIFIED;* THAT IS, LSB ALWAYS APPEARS IN RDI (PIN 12).

Fig.32 UAR/T RECEIVER TIMING

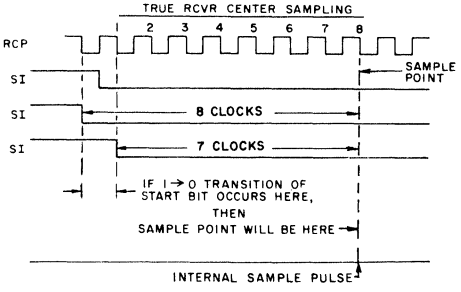


Fig.33

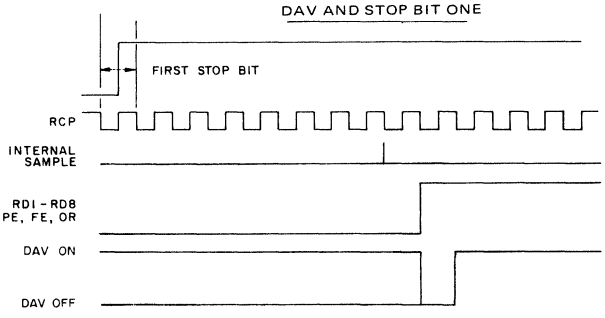
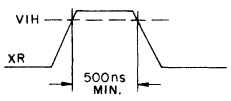


Fig.34 RECEIVER DURING 1ST STOP BIT



WHEN NOT IN USE, XR MUST BE HELD AT GND.

XR RESETS EVERY REGISTER, SO, TBMT, EOC ARE RESET TO 5V ALL OTHER OUTPUTS RESET TO OV.

Fig.35 XR PULSE

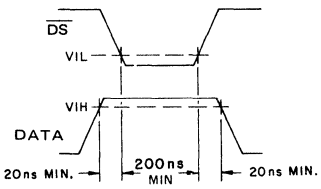
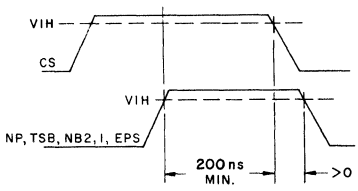
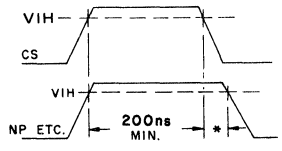


Fig.36 $\overline{DS}$



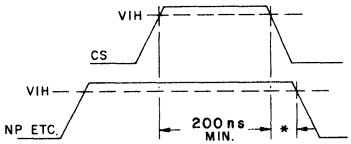
CONTROL BITS MUST BE STABLE FOR LAST 300ns OF CS.

Fig.37a CS



CONTROL STROBE AND CONTROL BITS MUST BE 300ns MINIMUM.

Fig.37b



LEADING EDGE OF DATA IS NOT CRITICAL AS LONG AS TRAILING EDGE AND PULSE WIDTH SPECS ARE OBSERVED.

* 20ns MIN.

Fig.37c

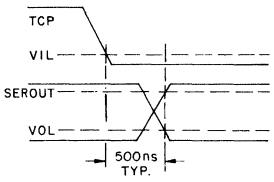


Fig.38 SEROUT

8

TIMING DIAGRAMS

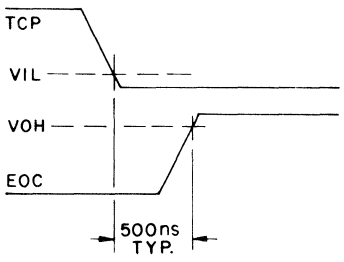


Fig.39 EOC TURN-ON

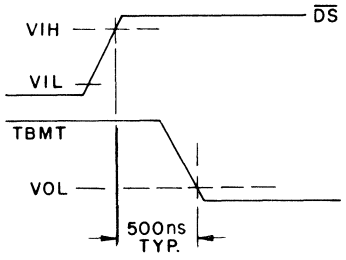


Fig.40 TBMT TURN-OFF

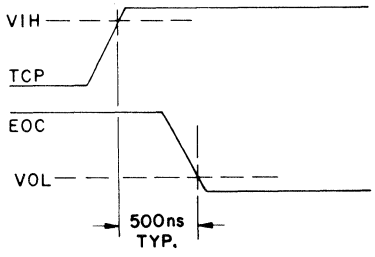


Fig.41 EOC TURN-OFF

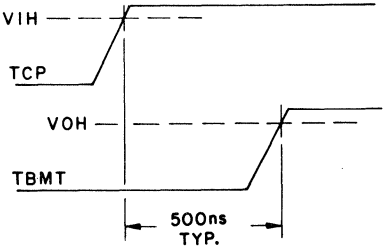


Fig.42 TBMT TURN-ON

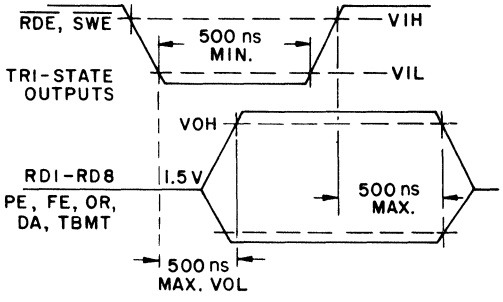


Fig.43 RDE, SWE

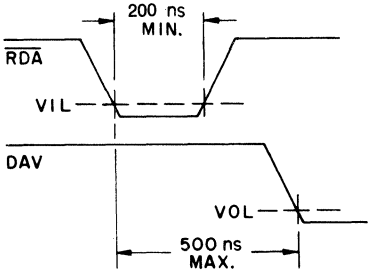


Fig.44 RDAV

TYPICAL CHARACTERISTIC CURVES

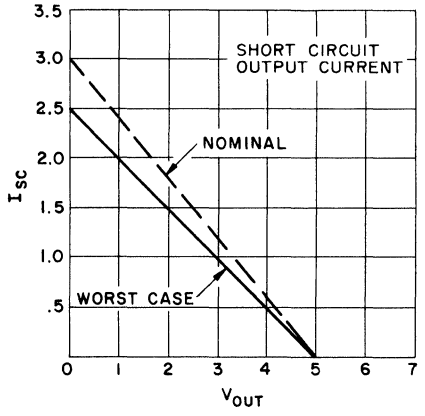


Fig.45 SHORT CIRCUIT OUTPUT CURRENT

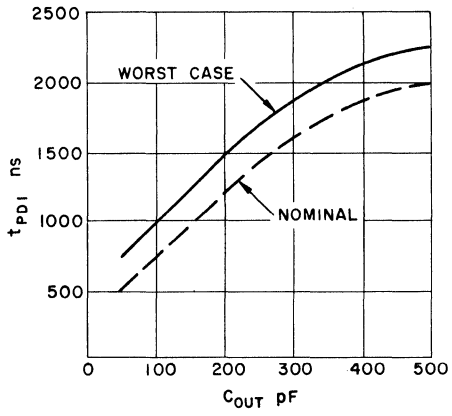


Fig.46 RD1-RD8, PE, FE, OR, TBMT, DAV

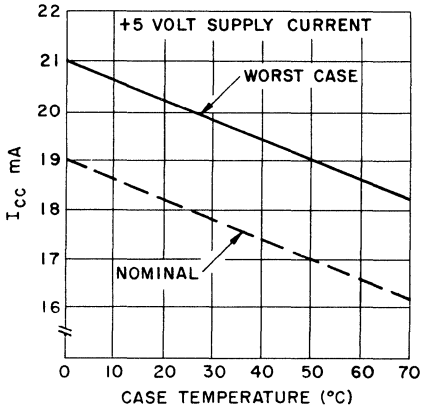


Fig.47 +5 VOLT SUPPLY CURRENT

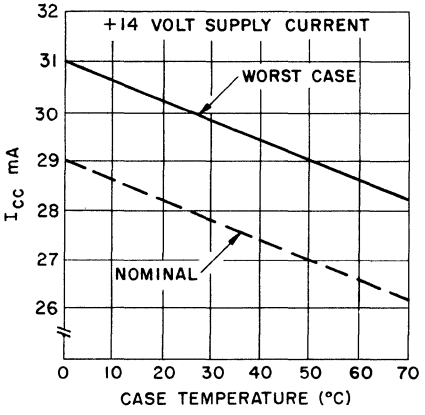


Fig.48 +14 VOLT SUPPLY CURRENT

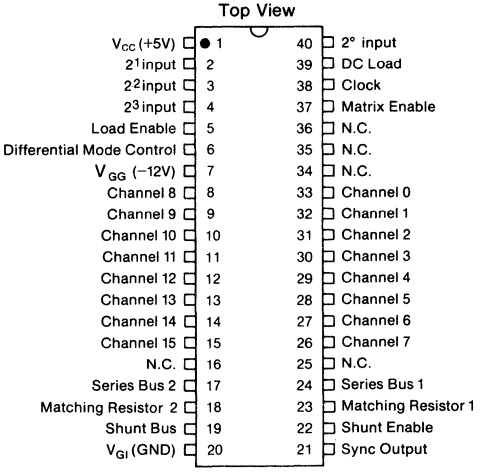
Random/Sequential Access Multiplexer

FEATURES

- Directly interfaces with TTL/DTL and MOS.
- Current or voltage modes of operation.
- Random or sequential access.
- Single ended or differential operation.
- Expandable in either the sequential or random access modes.
- Programmable length counter for sequential applications.
- DC to 2MHz operation.
- Extremely high off-resistance.
- Choice of Operating Temperature Ranges:
  AY-5-1016 — 0°C to +70°C
  AY-6-4016 — −55°C to +125°C
- Zener network protection on all input leads.

PIN CONFIGURATION

40 LEAD DUAL IN LINE

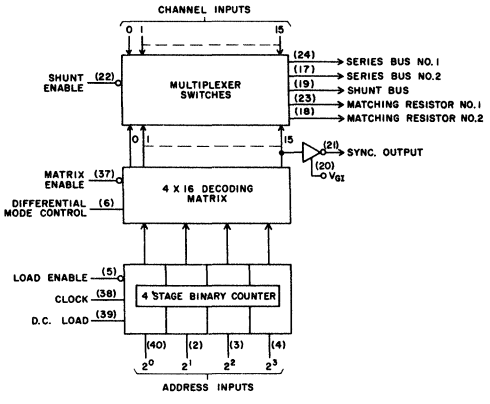


DESCRIPTION

The AY-5-1016 and AY-6-4016 are each a 16 Channel Random/Sequential Access Multiplexer containing a programmable 4 stage binary counter, a 4 × 16 decode matrix, and 16 single-pole double-throw switches.

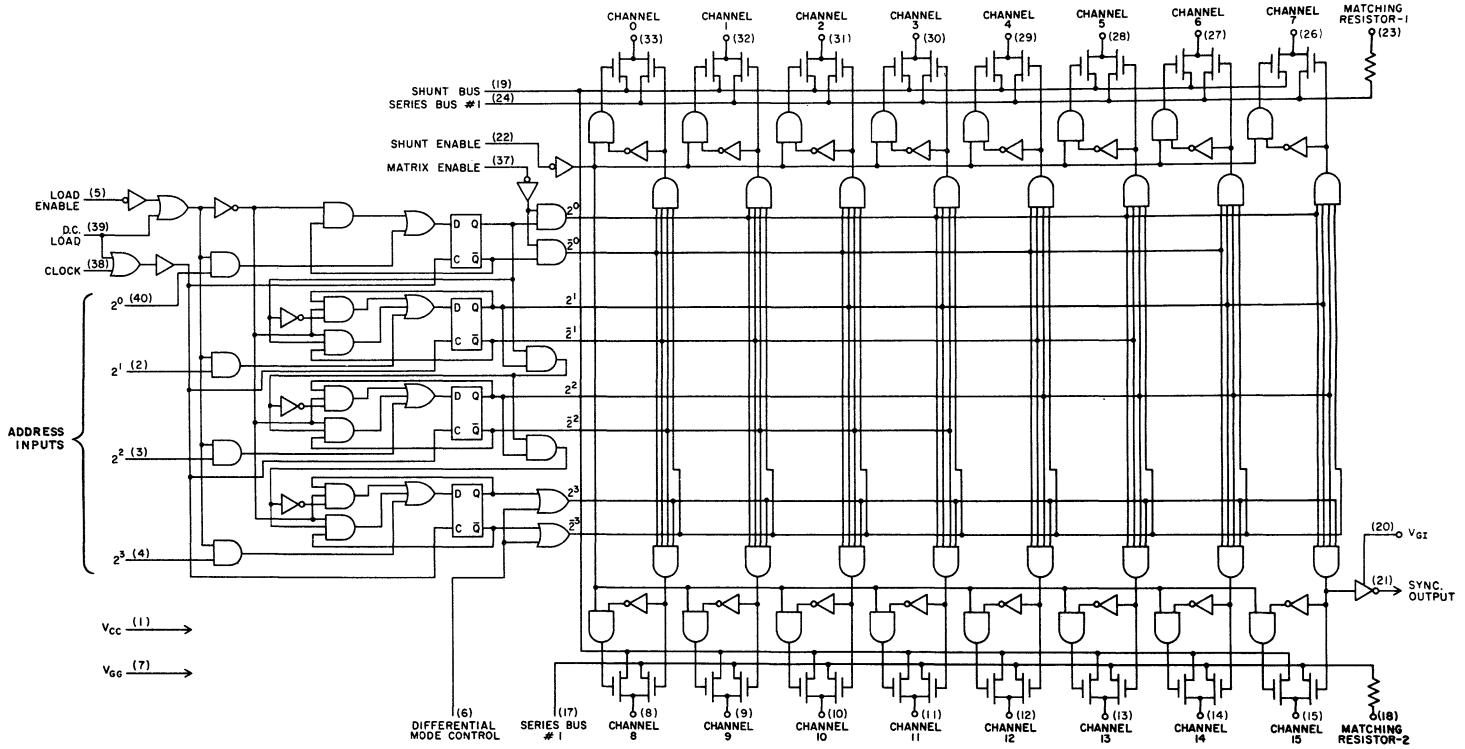
The Shunt Enable control line permits the selection of Current Mode or Voltage Mode operation and in conjunction with the Current Mode, matching resistors are provided to improve accuracy. The Differential Mode Control allows the switches to operate as eight ganged pairs, while the Matrix Inhibit line allows multiple AY-5-1016's (or AY-6-4016's) to be connected to form larger multiplexing arrays. The Load Enable control allows synchronous loading of the 4 address inputs on a low to high transition of the Clock. The DC load control is provided for asynchronous loading of the address inputs independent of the Clock and Load Enable inputs. The Sync Output occurs whenever Channel 15 is selected and is provided to allow expansion in the sequential mode of operation. Also by connecting the Sync Output to the Load Enable Input, the counter length can be programmed via the address inputs. Any desired length of from 1 to 16 states can be programmed in this manner.

BLOCK DIAGRAM



LOGIC DIAGRAM

( ) = Pin Numbers



NOTES:

1. Direct Address gated when either DC Load = "1" or Load Enable = "0".
2. DC Load gives permanent high clock.
3. Matrix Enable = "1" inhibits matrix.
4. Shunt Enable = "0" connects shunt FETS into circuit.
5. Differential Mode Control = "1" connects channels 8-15 ganged to channels 0-7.
6. Sync Output = "0" when channel 15 is accessed.

ELECTRICAL CHARACTERISTICS

Maximum Ratings

V_{GI} and V_{GG} (with respect to V_{CC}) . . . . . −20V to +0.3V
Clock and Logic Input Voltages (with respect to V_{CC}) . . . . . −20V to +0.3V
Bus Voltages (Bus 1, Bus 2, and Shunt Bus with respect to V_{CC}) . . . −20V to .3V
Matching Resistor Nodes (with respect to V_{CC}) . . . . . −20V to .3V
Storage Temperature . . . . . −55°C to +150°C
Operating Temperature Range: . . . . . 0°C to +70°C (AY-5-1016)
−55°C to +125°C (AY-6-4016)

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise stated)

V_{CC} = +5 Volts ±0.5 Volts (V_{CC} = Substrate voltage)
V_{GG} = −12 Volts ±1 Volt
V_{GI} = GND
Operating Temperature (T_A) = −0°C to +70°C (AY-5-1016)
−55°C to +125°C (AY-6-4016)

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Inputs (See Fig.1)					
Repetition Rate	DC	—	2.0	MHz	
Clock Pulse Width (ϕpw)	200	—	—	ns	at 2MHz, (See NOTE 1)
Clock Pulse Width (ϕpw)	1.0	—	—	μs	at 200Hz
Clock Pulse Delay (ϕd)	200	—	—	ns	See NOTE 1
Logic Levels					
Logic "0"	—	—	+0.8	V	
Logic "1"	V_{CC}−1.5	—	—	V	
Input Capacitance	—	12	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN} = +5V to −5V
Rise & Fall Time (tr, tf)	—	—	1.0	μs	at 100KHz
Rise & Fall Time (tr, tf)	—	—	50	ns	at 2MHz
Noise Immunity	+0.4	—	—	V	
Address Inputs (See Fig.1)					
Clock Lead Time	300	—	—	ns	
Logic Levels					
Logic "0"	—	—	+0.8	V	
Logic "1"	V_{CC}−1.5	—	—	V	
Input Capacitance	—	6	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN} = +5V to −5V
Noise Immunity	+0.4	—	—	V	
Load Enable Input (See Fig.1)					
Clock Lead Time	300	—	—	ns	
Logic Levels					
Logic "0"	—	—	+0.8	V	
Logic "1"	V_{CC}−1.5	—	—	V	
Input Capacitance	—	7	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN} = +5V to −5V
Noise Immunity	+0.4	—	—	V	
DC Load Input (See Fig.2)					
Pulse Width (90% points)	400	—	—	ns	
Logic Levels					
Logic "0"	—	—	+0.8	V	
Logic "1"	V_{CC}−1.5	—	—	V	
Input Capacitance	—	8	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN} = +5V to −5V
Noise Immunity	+0.4	—	—	V	

**Typical values are at +25°C and nominal voltages.
NOTE 1: ϕpw + ϕd ⩾ 500ns

TIMING DIAGRAMS

Fig.1

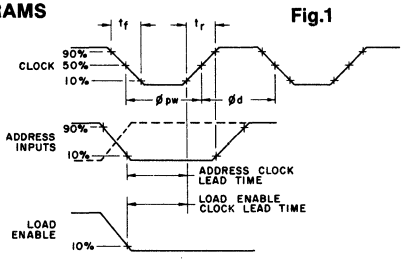
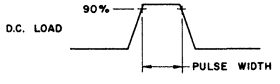


Fig.2



NOTE: Address Inputs and the Load Enable Input must be present during the 0 to 1 transition of the Clock.

Charateristic	Min	Typ**	Max	Units	Conditions
Shunt Enable					
Logic Levels					
Logic "0"	—	—	+0.8	V	
Logic "1"	V_{CC}–1.5	—	—	V	
Input Capacitance	—	6	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN} = +5V to –5V
Noise Immunity	+0.4	—	—	V	
Matrix Enable					
Response Time (See Fig. 3)					
T_{ON}	—	230	—	ns	} at 25°C Output voltage
T_{OFF}	—	120	—	ns	} response with10 MΩ, 10 pF load
Logic Levels					
Logic "0"	—	—	0.8	V	
Logic "1"	V_{CC}–1.5	—	—	V	
Input Capacitance	—	7	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN}= +5V to –V
Noise Immunity	+0.4	—	—	V	
Differential Mode Control					
Response Time (See Fig. 4)					
T_{ON}	—	200	—	ns	} at 25°C Output voltage
T_{OFF}	—	600	—	ns	} response with 10 MΩ, 10 pF load
Logic Levels					
Logic "0"	—	—	0.8	V	
Logic "1"	V_{CC}–1.5	—	—	V	
Input Capacitance	—	5	—	pF	
Input Impedance	1.0	—	—	MΩ	
Noise Immunity	0.4	—	—	V	
Series Switches					
R on (Current Mode)	—	460	750	Ohms	I_{IN} = 100 μA Series Bus 1 = Series Bus 2 = OV (V_{CC} –5V) T_A = 25°C V_{CC} = +5V V_{GG} = 12V
R on (Voltage Mode)	—	300	500	Ohms	V_{IN} = +5V, R_L = 300 KΩ T_A = 25°C V_{CC} = +5V V_{GG} = –12V
	—	460	750	Ohms	V_{IN} = OV, R_L = 300 KΩ T_A = 25°C V_{CC} = +5V V_{GG} = –12V
R off	—	5	—	GΩ	V_{IN} = V_{CC} –10V T_A = 25°C
Turn On Time	—	300	—	ns	Output Voltage Waveform with 10 MΩ, 10 pF load T_A = 25°C

**Typical values are at 25°C and nominal voltages.

TIMING DIAGRAMS

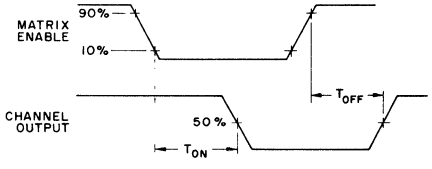


Fig.3

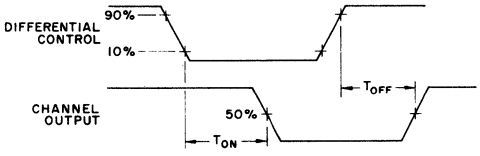


Fig.4

Characteristic	Min	Typ**	Max	Units	Conditions
Sync Output (See Fig.5)					
Logic "0"	—	—	+0.4	V	C = 10pF; I_{SINK} = 1.6mA min.; I_{OF} = 100 μA min. } Output Load
Logic "1"	V_{CC}–1.0	—	—	V	
Rise Time (tr)	—	110	—	ns	} at 25°C
Fall Time (tf)	—	40	—	ns	
Response Time					
tpd –	—	200	—	ns	} at 25°C
tpd +	—	160	—	ns	
Input Leakage					
Channels 0-15 (Per Channel)	—	1.0	10	nA	$V_{IN} = V_{CC}$ –5V at 25°C
Series Bus 1, 2	—	3.0	30	nA	$V_{BUS} = V_{CC}$ –5V at 25°C
Shunt Bus	—	3.0	30	nA	$V_{BUS} = V_{CC}$ –5V at 25°C
Shunt Switches					
R on	—	850	1300	Ohms	I_{IN} = 100 μA; Shunt Bus = OV; V_{CC} = +5V; V_{GG} = —12V; T_A = 25°C
	—	550	900	Ohms	I_{IN} = 100 μA; Shunt Bus = +5V; V_{CC} = +5V; V_{GG} = –12V; T_A = 25°C
R off	—	5	—	GΩ	$V_{IN} = V_{CC}$ –10V; T_A = 25°C
Turn On Time	—	300	—	ns	Output Voltage Waveform with 10 MΩ, 10 pF load; T_A = 25°C
Matching Resistors	—	460	750	Ohms	i_{IN} = 100 μA; V_{BUS} = OV
R on	—	300	500	Ohms	I_{IN}= 100 μA; V_{BUS} = +5V
Channel Input Capacitance, Channels 0-15 (Per Channel)	—	4	—	pF	
Power Consumption	—	200	—	mW	} Series MODE } V_{GG} = –12V; V_{CC} = +5V
	—	290	—	mW	} Shunt MODE
Current Drain					
I_{CC}	—	12	—	mA	} Series MODE } V_{GG} = –12V; V_{CC} = +5V
I_{GG}	—	12	—	mA	
I_{CC}	—	17	—	mA	} Shunt MODE
I_{GG}	—	17	—	mA	
Power Dissipation (Device)	—	—	600	mW	
Per Channel	—	—	100	mW	

**Typical values are at 25°C and nominal voltages.

TIMING DIAGRAMS

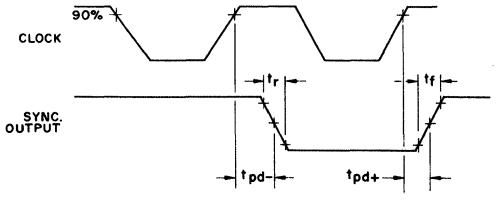
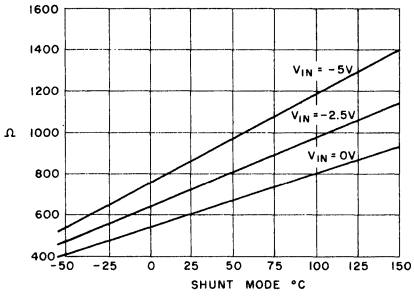
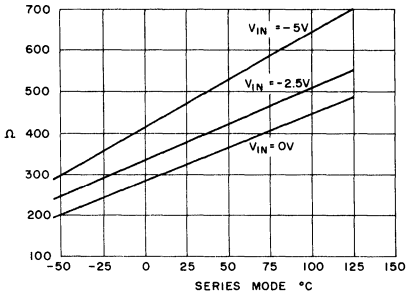
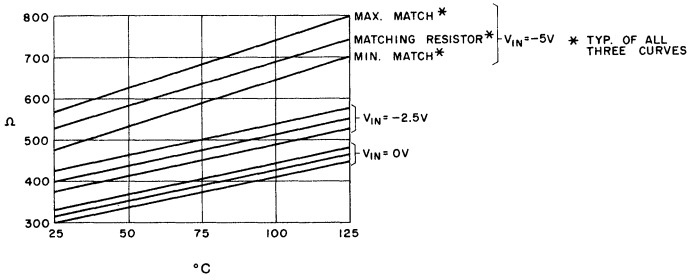


FIG.5

TYPICAL CHARCTERISTIC CURVES







8

GENERAL INSTRUMENT

MEM1056
MEM1056BCD
AY-5-3500
AY-5-3507
AY-5-3510
AY-5-4007
AY-5-4007A
AY-5-4007D
AY-5-4057
AY-5-5053
AY-5-5054

9

One Digit Counter/Display Driver

FEATURES

- Up/Down Presettable BCD Counter
- BCD-to-Seven Segment Decoding
- False Code Indication
- Direct Display Drive Capability
- Low Power Consumption
- No High Voltage Necessary

MEM1056
- Count Zero Indication
- Internal Storage Registers
- Decimal Point Indication
- Blanking Provision

MEM1056BCD
- Synchronous and Asynchronous Up/Down Counting
- Internal Storage Registers with BCD Outputs

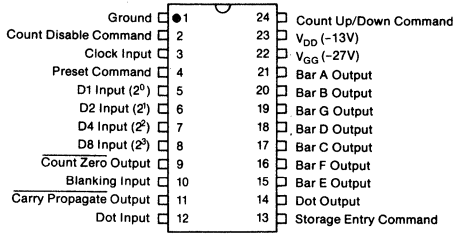
DESCRIPTION

The MEM1056 and MEM1056BCD are MTOS monolithic integrated circuits designed to operate in conjunction with a seven segment numeric indicator, such as the Tung-Sol Digivac S/G readout display tube. They contain a one decade up-down BCD counter, a storage register, a BCD-to-seven segment decoding matrix and display drivers.

PIN CONFIGURATION

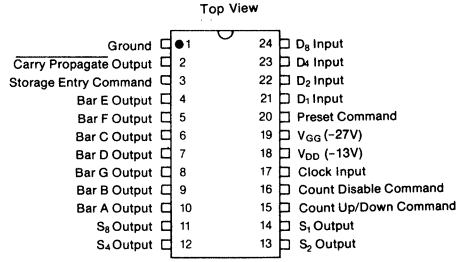
24 LEAD DUAL IN LINE
MEM1056

Top View

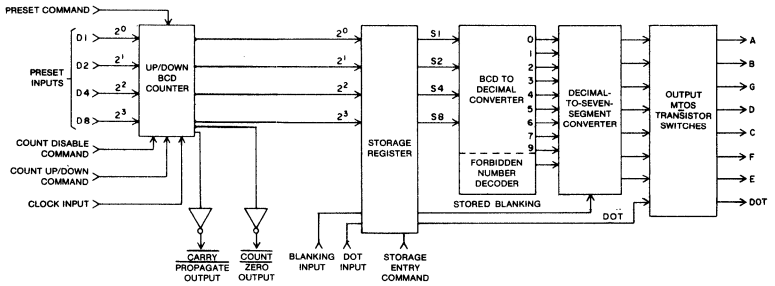


24 LEAD DUAL IN LINE
MEM1056BCD

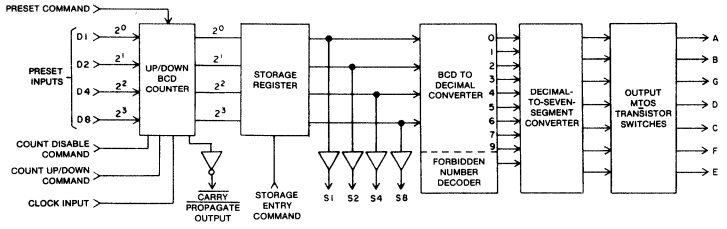
Top View



BLOCK DIAGRAM - MEM1056



BLOCK DIAGRAM - MEM1056BCD



3¾ Digit DVM Circuit

FEATURES

- Single Ramp Integration.
- Three measurement ranges 999, 1999, 2999.
- Dual Polarity.
- Reading Rate up to 70 measurements per second.
- Overrange indication, 2 most significant digits flash.
- Separate overrange output available on 1999 and 2999 ranges.
- Underrange output.
- Operating voltage 13V to 17V.
- Power consumption 30mW typical.
- 7 segment or BCD output.
- Controllable display brightness.
- Load enable freezes display.
- Hold input halts measurement.

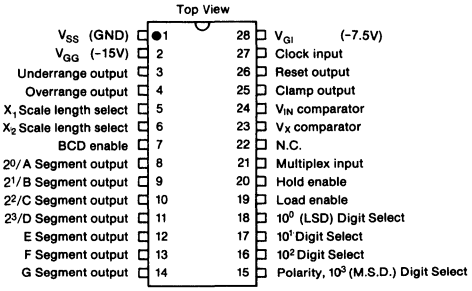
DESCRIPTION

The AY-5-3500 is a single ramp, dual polarity digital voltmeter chip having a selectable scale length of 999, 1999, 2999.

It is manufactured using the MTNS low voltage p-channel nitride technology. Low power dissipation achieved by the use of 4-phase logic with an "on chip" clock generator.

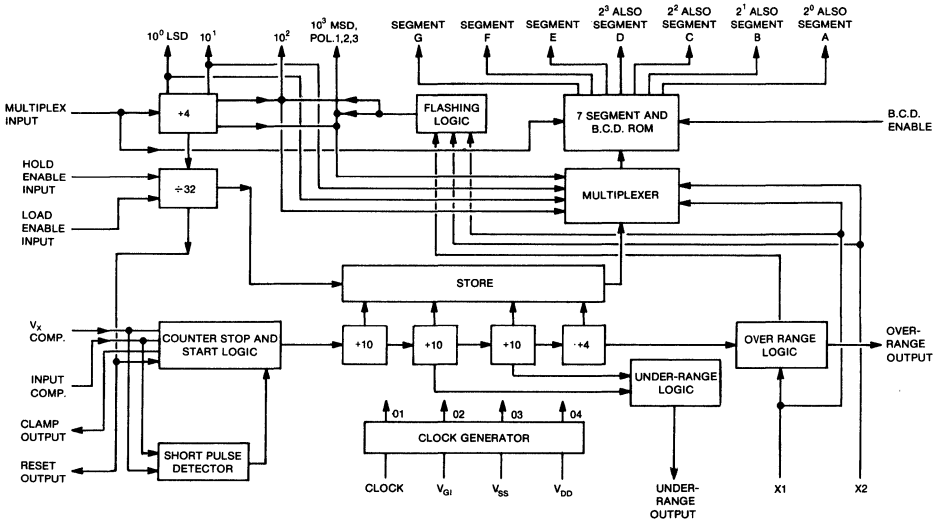
PIN CONFIGURATION

28 LEAD DUAL IN LINE



See next page for details of Pin Functions.

BLOCK DIAGRAM



PIN FUNCTIONS

OVERRANGE OUTPUT
This output goes to logic '1' as soon as an overrange count has been detected. It returns as logic '0' at the end of the measurement cycle.

It operates at 2000 on the 1999 range
It operates at 3000 on the 2999 range

MEASUREMENT CYCLE
The measurement cycle lasts 128 Multiplex clock periods. Data is transferred to the display store from clocks 113 to 120. The counters are reset from 121 to 128.

UNDERRANGE OUTPUT
The underrange output is a pulse from clock 105 to 112 if the reading is less than 259.

SCALE LENGTH SELECT

X1	X2	Scale
0	1	999
1	0	1999
0	0	2999

OVERRANGING

Range	Count	Display	Overrange Output
999	0XXX	XXX	0
	1XXX	1XXX } First	0
	2XXX	XXX } Two Digits	0
	3XXX	3XXX } Flash	0
1999	0XXX	XXX	0
	1XXX	1XXX	0
	2XXX	1XXX } First Two	1
	3XXX	3XXX } Digits Flash	1
2999	0XXX	XXX	0
	1XXX	1XXX	0
	2XXX	2XXX	0
	3XXX	3XXX } First Two Digits Flash	1

CLAMP OUTPUT
The clamp output goes to a logic '1' after 3 Counter clock periods following the input from the V_{IN} comparator. This output is used to switch off the V_{IN} comparator thus reducing the average input current by a factor of approx. 70. Fig.2 shows input waveforms without use of clamp output and Fig.3 shows waveforms with use of clamp output and timing for Clamp output.

BCD ENABLE
Logic '0' = BCD
Logic '1' = 7 segment

BCD OUTPUTS
The BCD outputs appear on the 7 segment output lines (Logic (1) is the Active Level); E, F, G are blanked to logic '0'
$A = 2^0$
$B = 2^1$
$C = 2^2$
$D = 2^3$

LOAD ENABLE
Logic '0' = Normal Operation
Logic '1' = Freeze Display

HOLD ENABLE
Logic '0' = Halts measurement cycle in reset state
Logic '1' = Normal Operation

RESET OUTPUT
Logic '1' resets ramp generator

NEGATIVE SIGN OUTPUT
Displayed on segment G output on 999 and 1999 ranges. Inhibited on 2999 range.

OPERATION
A linear stable ramp is generated and compared to zero volts and the input voltage in two comparators. The time between the changing of the comparator outputs is proportional to the magnitude of the input voltage, and the sequence of switching gives the polarity.

TIMING DIAGRAMS

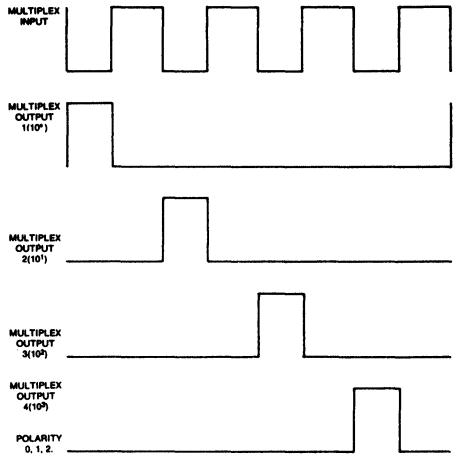


Fig.1 MULTIPLEX INPUT AND OUTPUT

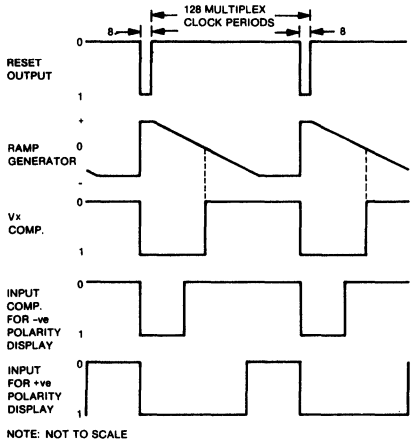


Fig.2 INPUT AND RESET OUTPUT

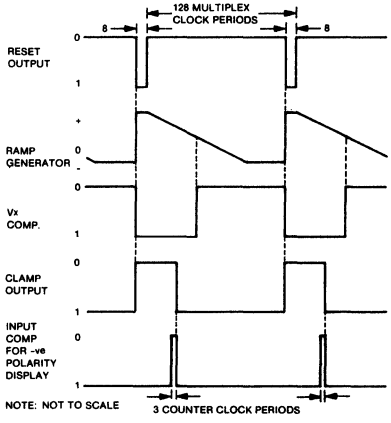
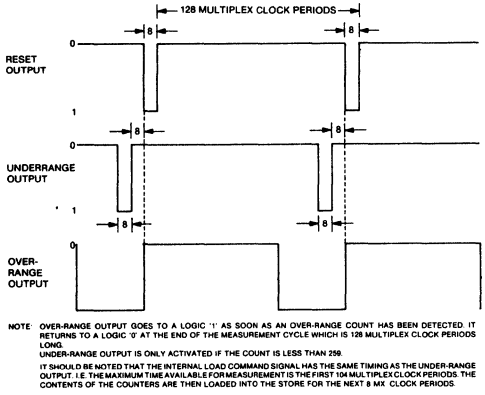


Fig.3 INPUT AND RESET OUTPUT TIMING DIAGRAM SHOWING CLAMP OUTPUT



NOTE: OVER-RANGE OUTPUT GOES TO A LOGIC '1' AS SOON AS AN OVER-RANGE COUNT HAS BEEN DETECTED. IT RETURNS TO A LOGIC '0' AT THE END OF THE MEASUREMENT CYCLE WHICH IS 128 MULTIPLEX CLOCK PERIODS LONG.
UNDER-RANGE OUTPUT IS ONLY ACTIVATED IF THE COUNT IS LESS THAN 259.
IT SHOULD BE NOTED THAT THE INTERNAL LOAD COMMAND SIGNAL HAS THE SAME TIMING AS THE UNDER-RANGE OUTPUT. I.E. THE MAXIMUM TIME AVAILABLE FOR MEASUREMENT IS THE FIRST 104 MULTIPLEX CLOCK PERIODS. THE CONTENTS OF THE COUNTERS ARE THEN LOADED INTO THE STORE FOR THE NEXT 8 MX. CLOCK PERIODS.

Fig.4 UNDER-RANGE AND OVER-RANGE OUTPUT

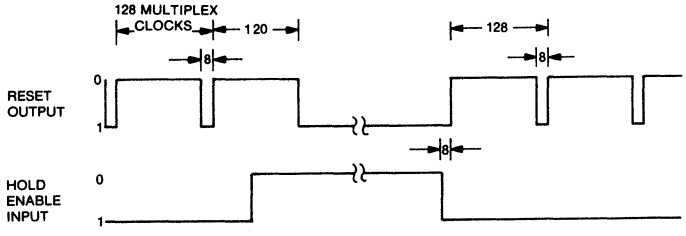


Fig.5 RESET OUTPUT WITH RESPECT TO HOLD ENABLE INPUT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin . . . . −20V to +0.3V
Storage temperature range. . . . . −65°C to +150°C
Ambient operating temperature range . . . . . 0°C to +70°C

*Exceeding these ratngs could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

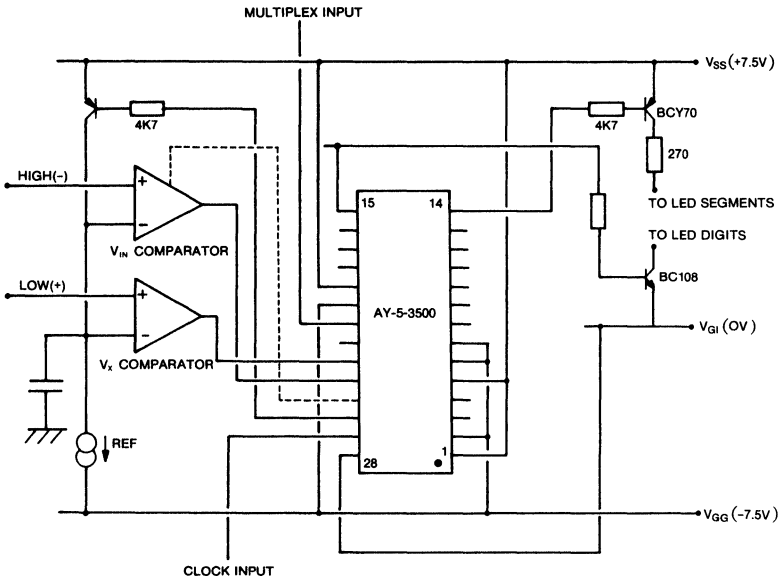
Standard Conditions (unless otherwise noted)

$V_{SS} = 0V$
$V_{GG} = -15 \pm 2V$
$V_{GI} = V_{GG}/2$ (Note 8)
Temperature (T_A) = 0°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Input					
Frequency	—	200	—	KHz	
Pulse width	1.5	—	—	μs	At logic '0' and '1' levels
Rise and Fall time	—	—	1	μs	
Logic '0' level	+0.3	—	−1	V	
Logic '1' level	−9	—	−17	V	
Multiplex Input					
Frequency	0.5	1.5	10	KHz	(See Note 1)
Pulse width	15	—	—	μs	At logic '0' and '1' levels (Note 2)
Logic '0' level	+0.3	—	−1	V	
Logic '1' level	−4	—	−17	V	
Control Inputs					
Logic '0' level	+0.3	—	−1	V	
Logic '1' level	−4	—	−17	V	
Leakage (all inputs)	—	—	1	μA	$V_{IN} = -10V$ at 25°C
Segment,Overrange, Underrange Outputs					
Logic '0'	—	—	30	KΩ	$V_{OUT} = -0.3V$ (Note 3)
Logic '1'	—	—	2	KΩ	$V_{OUT} = V_{GI} + 1V$ (Note 4)
Digit Select Outputs					
Logic '0'	—	—	1	KΩ	$V_{OUT} = -1V$ (Note 5)
Logic '1'	—	—	15	KΩ	$V_{OUT} = V_{GI} + 0.3V$ (Note 6)
Clamp and Reset Outputs					
Logic '0'	—	—	20	KΩ	$V_{OUT} = -0.2V$ (Note 3)
Logic '1'	—	—	5	KΩ	$V_{OUT} = V_{GI} + 1V$ (Note 7)
Supply Current	—	2	—	mA	$V_{GG} = -15V$ excluding output current

**Typical values are at +25°C and nominal voltages.

NOTE:
1. This gives a reading rate of typically 12 per second.
On the 2999 range, the maximum Multiplex clock frequency must be less than the Counter clock frequency divided by 64.
On the 1999 range, the maximum Multiplex clock frequency must be less than the Counter clock frequency divided by 42.
On the 999 range the maximum Multiplex clock frequency must be less than the Counter clock frequency divided by 21.
2. In 7 segment mode, outputs are energised when Multiplex input is at Logic '1'.
The display brilliance is therefore controlled by the input Mark-Space ratio.
3. Output device connected to V_{SS}.
4. Output device connected to V_{GI} segment energised.
5. Output device connected to V_{SS} digit selected.
6. Output device connected to V_{GI}.
7. Output device connected to V_{GI} Reset condition.
8. V_{GI} is only applied to the output drivers, thus its absolute value is not critical.



AY-5-3500 D.V.M. -FSD 999 COMMON CATHODE LED DISPLAY

9

3½ Digit DVM Circuit

FEATURES

- 3½ Decade Display (±1999 max. reading)
- Automatic Polarity Detection
- Overrange Indication

AY-5-3507
- Direct LED 7-Segment Drive
- Up to 10 readings per second

AY-3-3510
- BCD Outputs
- Up to 50 readings per second
- Chopper Output provided for oscillator synchronization or underrange indication

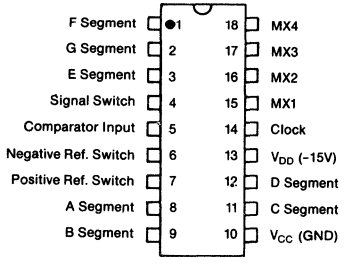
DESCRIPTION

The AY-5-3507 and the AY-5-3510 are MOS LSI circuits containing all the logic necessary for a 3½ Decade Digital Voltmeter utilizing Dual Ramp integration. Automatic polarity detection is incorporated as is automatic overrange indication. For the AY-5-3507, the outputs are multiplexed onto a 7-segment bus allowing easy interface to LE and similar displays. For the AY-5-3510 the outputs are multiplexed onto a BCD bus allowing easy interface to a wide variety of displays.

PIN CONFIGURATION

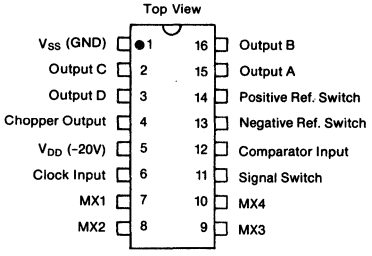
18 LEAD DUAL IN LINE
AY-5-3507

Top View



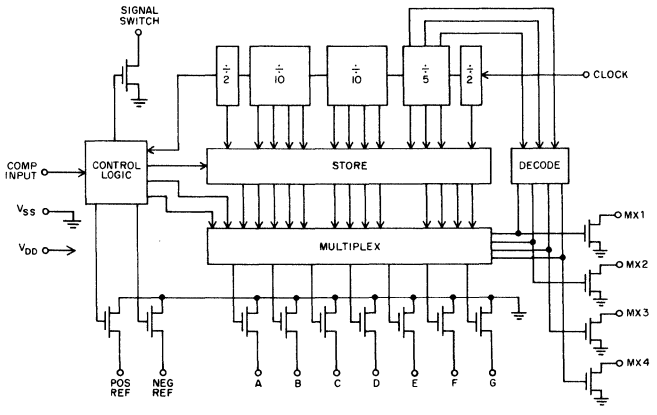
16 LEAD DUAL IN LINE
AY-5-3510

Top View

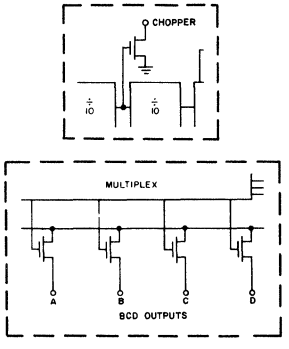


See next page for details of Pin Functions

BLOCK DIAGRAM



AY-5-3507



SAME AS AY-5-3507 EXCEPT AS MARKED ABOVE.

AY-5-3510

PIN FUNCTIONS

Name	Functions
COMPARATOR INPUT	A logic '0' level corresponds to a negative input signal. A logic '1' level corresponds to a positive input signal.
CLOCK INPUT	This signal should be supplied from an external oscillator giving a square wave signal.
REFERENCE SWITCH OUTPUTS	These outputs drive analog switches which connect the Reference Voltages to the Integrator. A logic '0' at the Comparator Input will be followed by a logic '1' at the Positive Reference Switch Output. A logic '1' at the Comparator Input will be followed by a logic '1' at the Negative Reference Switch Output.
SIGNAL SWITCH OUTPUT	This output will be at logic '1' during the time that the signal is connected to the integrator.
DISPLAY MULTIPLES OUTPUTS	Each output will be at logic '1' for 2 clock periods to display (see Fig. 4). The outputs selected will be as follows:— MX1 O/1, ±, Over-range MX3 Decade 2 (10^1) MX2 Decade 3 (10^2) MX4 Decade 1 (10^0)
AY-5-3507 SEGMENT OUTPUTS	The outputs of the 3 decade counters are presented sequentially on the outputs A, B, C, D, E, F, G. In the first multiplex position 1 is indicated by segments B and C,—is indicated by segment G, overrange by the flashing of segments A and D. 0, + and underrange are not indicated.
AY-5-3510 CHOPPER OUTPUT	This output is a square wave at 1/100 the clock input frequency. It can be used either to phase lock the clock oscillator to the mains or to provide a 5% FSD under-range signal.
AY-5-3510 DISPLAY OUTPUTS	The outputs of the 3 decade counters are presented on the outputs A, B C, D in BCD complement code. $A=2^0$, $B=2^1$, $C=2^2$, $D=2^3$. At MX1 time, the most significant digit is output on A with its complement on D, sign is output on B and over-range on C.

OPERATION

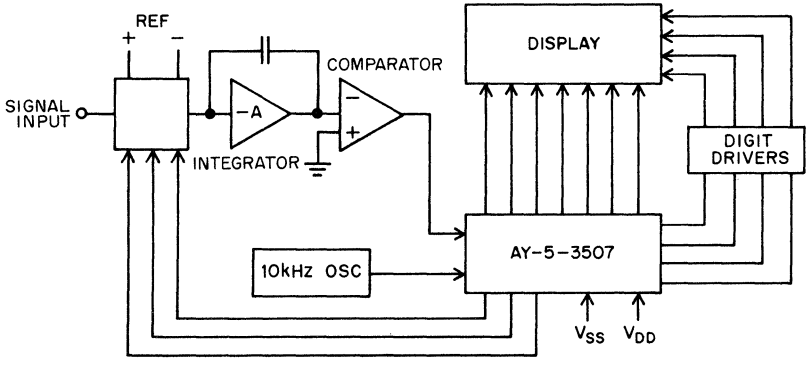
The operation of the circuit is as follows.

Initially the signal, and reference outputs are in the logic '0' state. The counter counts continuously and at the 1999 to 0000 transition a ÷2 is toggled driving the signal switch output to logic '1' turning on the signal switch. The integrator generates a ramp, the amplitude and polarity of which depend on the amplitude and polarity of the input signal. After a further 2000 clock pulses the ÷2 is toggled again. This stores the state of the comparator output in a D type flip flop (this signal represents the sign of the input signal). The appropriate reference switch is then energized to cause the integrator output to ramp back to zero. When the comparator output subsequently changes state the reference is switched off and the number in the counter is transferred to the store together with polarity information.

Should the input signal be so large that zero is not reached during one counter cycle, an overange flip flop will be set and will remain set until the next 1999 to 0000 transition of the counter. During overrange the main display will be set to 0000 and the overrange indicator will flash.

To minimize pin requirements, a time shared output is used. The display store output (including ±, 0/1 and overrange) is gated sequentially, a decade at a time, onto a common 7 line (AY-5-3507) or 4 line (AY-5-3510) output bus.

3½ DECADE DIGITAL VOLTMETER



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Maximum voltage between any pin and V_{SS} pin . . . . +0.3 to −20 V
Operating temperature range . . . . . 0°C to +70°C
Storage temperature range. . . . . −55°C to +150°C

*Exceeding these ratings could cause permanent damage. Functional operaton of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

	AY-5-3507	AY-5-3510
V_{CC}	GND	-
V_{SS}	-	GND
V_{DD}	−12 to −18V	−18 to -20V
Operating Temperature (T_A) =	0°C to +70°C	0°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
AY-5-3507					
DC CHARACTERISTICS					
Clock & Comparator Inputs					
Logic '0' Level	−6	—	−18	Volts	
Logic '1' Level	+0.3	—	−1	Volts	
Input Leakage	—	—	20	μA	V_{IN} = −15V, T_A = +25°C
Display Multiplex Outputs (Note 1)					
Logic '1' on resistance	—	1	2	KΩ	V_{OUT} = −2V
Logic '0' leakage current	—	—	20	μA	V_{OUT} = −15V
Switch Outputs (Note 1)					T_A = +25°C
Logic '1' on resistance	—	1.2	2.5	KΩ	V_{OUT} = −2V
Logic '0' leakage current	—	—	20	μA	V_{OUT} = −15V
Segment Outputs (Note 1)					T_A = +25°C
Logic '1' sink current V_{DD} = −12V	—	3	6	mA	V_{OUT} = −2V
V_{DD} = −15V	—	4.5	9	mA	V_{OUT} = −2V
V_{DD} = −18V	—	6	12	mA	V_{OUT} = −2V
Logic '0' leakage current	—	—	20	μA	V_{OUT} = −15V, T_A = +25°C
Supply Current	—	1.5	2.8	mA	V_{DD} = −12V
	—	4	8	mA	V_{DD} = −18V
AC CHARACTERISTICS					
Clock & Comparator Inputs					
Input Capacitance	—	5	—	pF	V_{IN} = 0V
Clock Frequency	DC	—	40	kHz	V_{DD} = −18V
	DC	—	10	kHz	V_{DD} = −12V
Display Multiplex Outputs					
Propagation delay	—	—	4	μs	from Clock positive edge
Segment Outputs					
Propagation delay	—	—	10	μs	from Multiplex output positive edge
AY-5-3510					
Clock & Comparator Inputs					
Logic '0' Level	−8	—	-20	Volts	
Logic '1' Level	+0.3	—	−1	Volts	
Input Capacitance	—	—	5	pf	V_{IN} = 0V
Input Leakage	—	—	20	μA	V_{IN} = −20V
Clock Frequency	DC	—	200	KHz	
Display Multiplex Outputs (Note 1)					
Logic '1' sink current	2	—	—	mA	V_{OUT} = −6V
Logic '0' leakage current	—	—	10	μA	V_{OUT} = −20V
Display & Switch Outputs (Note 1)					
Logic '1' sink current	0.7	—	—	mA	V_{OUT} = −4V
Logic '0' leakage current	—	—	10	μA	V_{OUT} = −20V
Supply Current	—	—	10.5	mA	V_{DD} = −20V

** Typical values are at +25°C and nominal voltages.

NOTE:
1. All outputs are single-ended ("open-drain"). External pull-down resistors are required.

TIMING DIAGRAMS

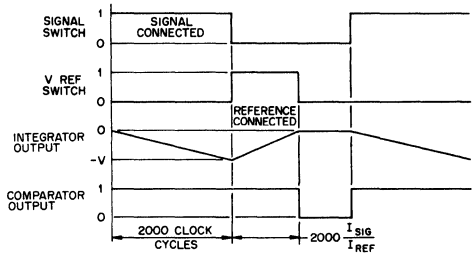


Fig.1

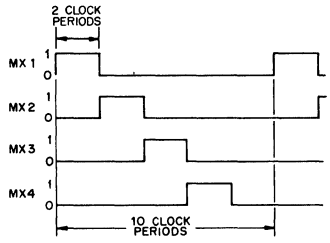


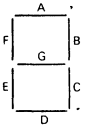
Fig.2 MULTIPLEX WAVEFORMS

TRUTH TABLES

AY-5-3507

7 SEGMENT OUTPUT TRUTH TABLE (MX2-MX4)

	Segment Output						
Digit	A	B	C	D	E	F	G
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	1	0	1	1



MX1 OUTPUT TRUTH TABLE

	Segment Output							
Display	A	B	C	D	E	F	G	
0	0	0	0	0	0	0	0	
1	0	1	1	0	0	0	0	
+	0	0	0	0	0	0	0	
−	0	0	0	0	0	0	1	
UR	0	0	0	0	0	0	0	
OR	1	0	0	1	0	0	0	Flashed

AY-5-3510

BCD OUTPUT TRUTH TABLE (MX2-MX4)

A	B	C	D	Digit Output
1	1	1	1	0
0	1	1	1	1
1	0	1	1	2
0	0	1	1	3
1	1	0	1	4
0	1	0	1	5
1	0	0	1	6
0	0	0	1	7
1	1	1	0	8
0	1	1	0	9

MX1 OUTPUT TRUTH TABLE

A	B	C	D	0/1	Polarity	Over-range
1	X	X	0	0		
0	X	X	1	1		
X	1	X	X		+	
X	0	X	X		−	
X	X	1	X			
X	X	0	X			OR

ANALOG CIRCUIT DIAGRAMS

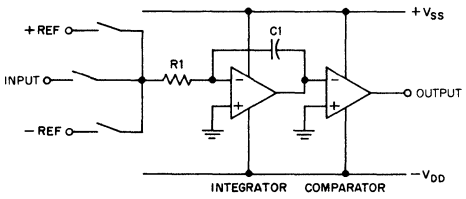


Fig.1 BASIC ANALOG CIRCUIT-AY-5-3507

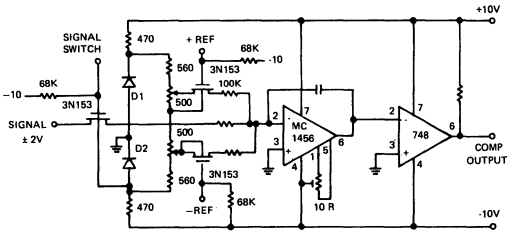


Fig.2 TYPICAL ANALOG CIRCUITRY-AY-5-3510

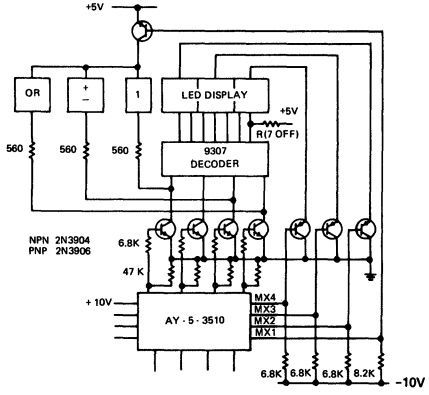


Fig.3 DISPLAY INTERFACE For AY-5-3510

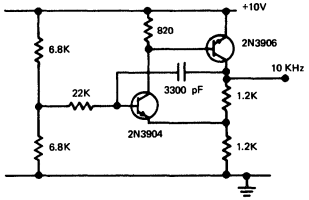


Fig.4 CLOCK OSCILLATOR-AY-5-3510

AY-5-4007
AY-5-4007A
AY-5-4007D

Four Digit Counter / Display Drivers

FEATURES

- Minimum interface required to drive most common types of LED, fluorescent, seven segment displays.
- Large output current capability on seven segment outputs, typically 25mA with 1V drop.
- Fully synchronous up/down counting operation.
- Look ahead carry for error free outputs when reversing count direction.
- Internal oscillator needing no external components for operating the digit select counter.
- Four digit select outputs with inversion control for display driving flexibility.
- Multiplexed BCD outputs and serial output from storage register is available.
- TTL/DTL compatible on inputs and outputs.
- Blanking action of Reset Input.
- Counting rate up to 600 KHz.

DESCRIPTION

The Four Digit Counter Display Driver is an LSI subsystem designed for application in counting display systems such as frequency counters, digital voltmeters, digital timers, event counters using 7 segment numeric displays. It contains a 4 decade up/down synchronous BCD counter, a storage register, multiplexing circuits, internal osciallator for digit selection and 7 segment decoder to count and display up to 9999.

Built-in control circuits provide flexibility of use with a minimum of external components.

The device is constructed on a single monolithic chip using MTNS P-channel enhancement mode transistors.

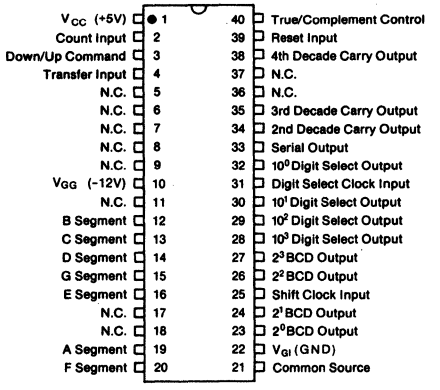
AY-5-4007, available in 40 Lead Dual In Line package, allows for all available functions.

The AY-5-4007 and AY-5-4007D incorporate the most commonly used features in 24 Lead Dual In Line packages.

PIN CONFIGURATION

40 LEAD DUAL IN LINE
AY-5-4007A

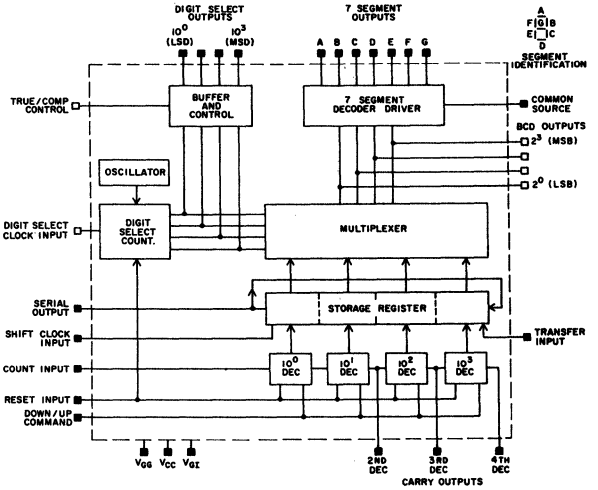
Top View



BLOCK DIAGRAM

AY-5-4007A shown:

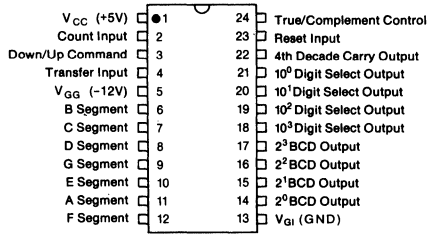
■ indicates functions available with the AY-5-4007D.



PIN CONFIGURATIONS

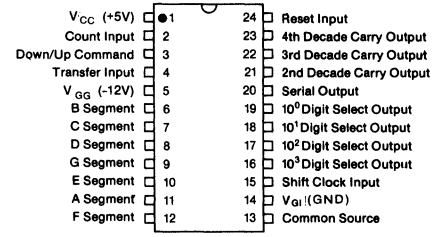
24 LEAD DUAL IN LINE
AY-5-4007

Top View



24 LEAD DUAL IN LINE
AY-5-4007D

Top View



NOTE: For AY-5-4007D, True/Complement control is internally connected to logic "0" level.

PIN FUNCTIONS

Name	Function
COUNT INPUT	Count Input operates the decade counters synchronously on the positive going edges (logic '0' to '1' transitions).
RESET INPUT	When this input goes to a logic '1' it resets the decade counters to 0000, forces the digit select counter to the MSD position and the Digit Select Outputs to 'not active' logic levels to blank the display. It must be present for a minimum of 10 uSec.
DOWN/UP COMMAND	The count direction depends upon the logic level on the DOWN/UP Command input. Logic '0' = Count UP. Logic '1' = Count DOWN.
2ND DECADE CARRY OUTPUT **3RD DECADE CARRY OUTPUT** **4TH DECADE CARRY OUTPUT**	Normally the Carry Outputs are at a logic '0' level; when activated a positive pulse is generated on the output line, which is identical with the Count Input causing the carry.
TRANSFER INPUT	Placing the Transfer Input at a logic '1' allows transfer of data from the decade counters to the storage register.
SHIFT CLOCK INPUT	This input is used to apply clock pulses to the storage register for serial shift operation. Normally Shift Clock is maintained at a Logic '1' and negative pulses are necessary to perform shift operation. Actual shifting of storage register data is done on the second edge (positive going) of each clock pulse. A Pull-up resistor is internally provided for the Shift Clock Input so that this line, if not used, may be left floating. Since the storage register is quasi-static in serial shift operation the width of negative pulses (at logic '0') has to be limited to 20uSec. During serial shift operation the Transfer Input must be at a logic '0'.
SERIAL OUTPUT	This is the serial output of the storage register. When serial shift operation is not performed the Serial Output is the least significant bit of the least significant digit of the storage register.
10^0 DIGIT SELECT OUTPUT (LSD) **10^1 DIGIT SELECT OUTPUT** **10^2 DIGIT SELECT OUTPUT** **10^3 DIGIT SELECT OUTPUT (MSD)**	These outputs provide sequentially an active logic level (logic '1' if the True/Complement Control is at a logic '1'; logic '0' if the True/Comlement Control is at a logic '0'), to specify which of the corresponding digits is selected and displayed, the remaining 3 Outputs being 'not active'. All the Digit Select Outputs are forced to a 'not active' logic level as long as the Reset Input is active.
2^0 BCD OUTPUT(LSB) **2^1 BCD OUTPUT** **2^2 BCD OUTPUT** **2^3 BCD OUTPUT(MSB)**	These outputs provide the Binary Coded Decimal representation of the digit being selected and displayed by the multiplexer. The truth table shows BCD Codification of these outputs.
"A" TO "G" SEGMENT	These outputs are programmed according to the truth table. Each output terminal is actually connected to the drain of the corresponding output transistor.
COMMON SOURCE	This is the common of the seven segment output transistors. When not externally available the corresponding terminal is internally tied to VGI (0V) line. It may be connected to any voltage between VSS and VDD according to requirements.
TRUE/COMPLEMENT CONTROL	This input controls the polarity of the Digit Select Outputs active logic level. When the TRUE/COMPLEMENT Control is at a logic '1', active level for the Digit Select Outputs is a logic '1', when at a logic '0' active level is a logic '0'.
DIGIT SELECT CLOCK INPUT	An external signal applied to this terminal overrides the internal ocillator. When the internal oscillator is used, this terminal must be left floating.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{CC}. . . . . −20 to +0.3V
Storage temperature range. . . . . −65°C to +150°C
Ambient operating temperature range . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of thse devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

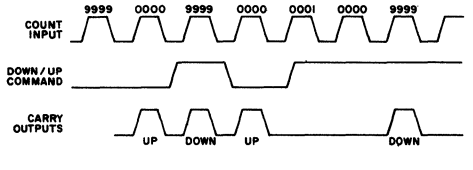
V_{CC} = +5.0 ±0.5V V_{GG} = −12V ±1V OR −7.0V ±0.5V
V_{GI} = 0V Operating Temperature (T_A) 0°C to +70°C

	V_{GG} = −12V ±1V			V_{GG} = −7V ±0.5V				
Characteristic	**Min**	**Typ****	**Max**	**Min**	**Typ****	**Max**	**Units**	**Conditions**
Inputs								
Logic '0'	V_{GG}	-	+0.8	V_{GG}	-	+0.8	Volts	See Fig. 4.
Logic '1'	V_{CC}−1.5	-	V_{CC}+0.3	V_{CC}−1.5	-	V_{CC}+0.3	Volts	
Capacitance	-	-	10.0	-	-	10.0	pF	V_{IN} = V_{CC} f=1MHz
Leakage	-	-	5.0	-	-	5.0	µA	V_{IN} − V_{CC} = −10V at 25°C
Repetition Rate	D.C.	-	600	D.C.	-	350	KHz	Square Wave
Pulse Width	0.7	-	-	1.0	-	-	µSec	Pulse either high or low
Tr & Tf	-	-	100			100	µSec	
True/Complement/ Control Input								
Input Current	10	40	100	10	-	50	µA	V_{IN} = V_{CC}
	10	25	50	10	-	25	µA	V_{IN} = V_{GI} See Fig. 5
Digit Select Clock								
Input Current	10	60	150	5	25	75	µA	V_{IN} = V_{CC} (Sink)
	50	250	1600	50	150	1000	µA	V_{IN} = V_{GI} (Source) See Fig. 3.
Internal Freq.	1.0	2.0	4.0	1.0	2.0	4.0	KHz	
External Freq.—Data only	D.C.	-	100	D.C.	-	50	KHz	
Display	D.C.	-	15	D.C.	-	7	KHz	Display Duty Cycle 25%
Shift Clock								
Frequency	D.C.	-	1	D.C.	-	0.8	MHz	
Pulse Width	0.4	-	1000	0.5	-	1000	µSec	See functional description
Input Current	20	100	400	10	30	200	µA	V_{IN} = V_{GI} (See Fig. 6)
Outputs—7 Segment (See Note 2)								
Leakage Current	-	-	10	-	-	10	µA	V_{OUT}—V_{CC} = −10V at 25°C
Device on Current	15	25	45	12	20	35	mA	V_{CS}—V_{OUT} = +1.0V at 25°C, V_{CS} = V_{CC}
Device on Current	12	18	27	7	11	17	mA	V_{CS}—V_{OUT} = −1.0V at 25°C, V_{CS} = V_{GI}
Power Dissipation (per segment at 25°C)	-	-	200	-	-	200	mW	See Note 1 & Fig. 1
Other Outputs								
Logic '0'	-	0.2	0.4	-	0.3	0.4	Volts	I_{OL} = 1.6mA with 10pF load
Logic '1'	V_{CC}−1.0	V_{CC}−0.65	-	V_{CC}−1.0	V_{CC}−0.65	-	Volts	I_{OL} = 50µA
Propagation Delay	-	-	1.0	-	-	1.5	µSec	Carry Output } See Fig. 2
			1.5	-	-	2.0	µSec	Serial Output }
Tr, Tf Rise, Fall Times	-	0.15	0.3	-	0.3	0.6	µSec	
Power								
I_{GG}	-	25	35	-	13	20	mA	(V_{CC} to V_{GG})

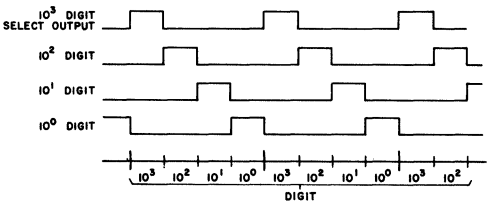
**Typical values are at +25°C and nominal voltages.

NOTES:
1. Derate Power Linearly to 100mW at 70°C.
2. See also Typical 7-Segment Output Curves, Figs.9, 11, & 13 (−12V ±1V)
   See also Typical 7-Segment Output Curves, Figs.10, 12, & 14 (−7V ±0.5V)

TIMING DIAGRAMS



CARRY OPERATION



DIGIT SELECT OPERATION
(True/Complement Control is at logic '1' level)

OPERATION

Decade Counters

The four decade counters are synchronously operated on the positive going edges of the Count Input; a single DOWN/UP Command controls the direction of counting. The edge-triggered structure of the master-slave flip-flops allows the count direction to be changed between count pulses at either Count Input level. A Reset Input resets decade counters to 0000.

Carry outputs are provided at the 2nd, 3rd and 4th decade; these outputs are activated when an overflow (in counting up) or an underflow (in counting down) condition exists in the corresponding decade counter. The carry output pulse is the same as the Count Input pulse causing the carry.

The look ahead design of the carry stages gives error free outputs when reversing the count direction.

Storage Register

Data in the decade counters is transferred to the storage register under control of the Transfer Input signal. The Transfer Input may be connected to a logic '1' for a continuous transfer and display operation.

The Storage register may also be operated as a parallel-in serial-out shift register. In this case clock pulses are to be provided to Shift Clock Input, the serial content of storage register is available on the Serial Output line, and recirculated back to the first stage input. A train of 16 clock pulses is needed to extract the full content of the register, least significant bit of least significant digit first. When operating the storage register serially, Transfer input is to be kept at a logic '0'.

Digit Select Counter and Multiplexer

The digit select counter is driven by a built in oscillator which requires no external components. The internal oscillator can be overridden by applying an external signal to the Digit Select Clock Input.

The digit select counter controls the multiplexer to route information from storage register to the 7 segment decoder drivers and to the BCD Outputs.

The counter scans from MSD (10^3 digit) to LSD (10^0 digit). Each of the four Digit Select Outputs is sequentially activated when the corresponding digit is selected and displayed.

The Digit Select counter is forced to MSD position and Digit Select Outputs are forced to 'not active' logic levels as long as Reset Input is active. This feature blanks the display when the device is being reset. The True/Complement Control inverts the Digit Select Outputs active logic level for flexibility of output interface circuitry.

Internal delay logic ensures that both 7 segment outputs and BCD outputs are valid before activation of the corresponding Digit Select Output to avoid "ghost images".

7 Segment Decoder Driver

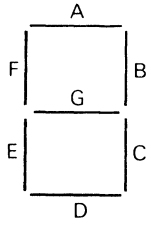
The 7 segment decoder drivers consist of very low impedance output transistors (typically 40 ohms) to minimize external interface components when driving 7 segment displays such as LEDs, fluorescents, incandescents, etc.

The 7 Segment Outputs are the drains of the corresponding output transistors, these outputs are programmed according to the truth table below. A Common Source terminal is also available to increase flexibility of use.

DIGIT	7 SEGMENT OUTPUT TRANSISTOR							BCD OUTPUT			
	A	B	C	D	E	F	G	MSB 2^3	2^2	2^1	LSB 2^0
0	*	*	*	*	*	*	–	0	0	0	0
1	–	*	*	–	–	–	–	0	0	0	1
2	*	*	–	*	*	–	*	0	0	1	0
3	*	*	*	*	–	–	*	0	0	1	1
4	–	*	*	–	–	*	*	0	1	0	0
5	*	–	*	*	–	*	*	0	1	0	1
6	*	–	*	*	*	*	*	0	1	1	0
7	*	*	*	–	–	–	–	0	1	1	1
8	*	*	*	*	*	*	*	1	0	0	0
9	*	*	*	*	–	*	*	1	0	0	1

LEGEND:
* output transistor ON
– output transistor OFF
0 logic '0'
1 logic '1'

SEGMENT IDENTIFICATION



7 SEGMENT AND BCD OUTPUTS TRUTH TABLE

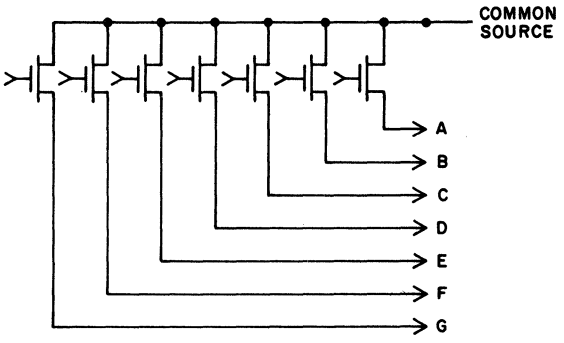


Fig.1 7-SEGMENT OUTPUTS

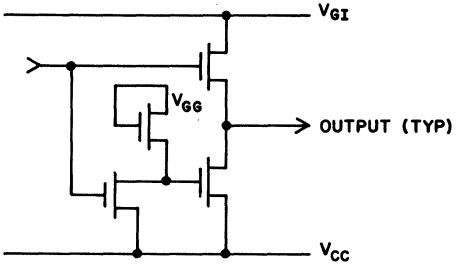


Fig.2 ALL OTHER OUTPUTS

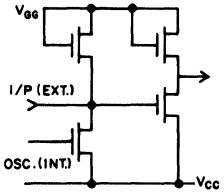


Fig.3 DIGIT SELECT CLOCK INPUT

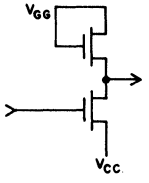


Fig.4 TYPICAL INPUT

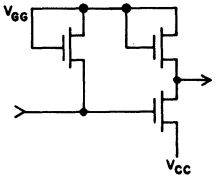


Fig.5 TRUE/COMPLEMENT INPUT

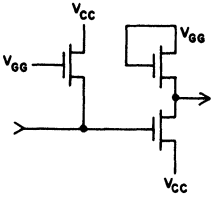


Fig.6 SHIFT CLOCK INPUT

CIRCUIT DIAGRAMS

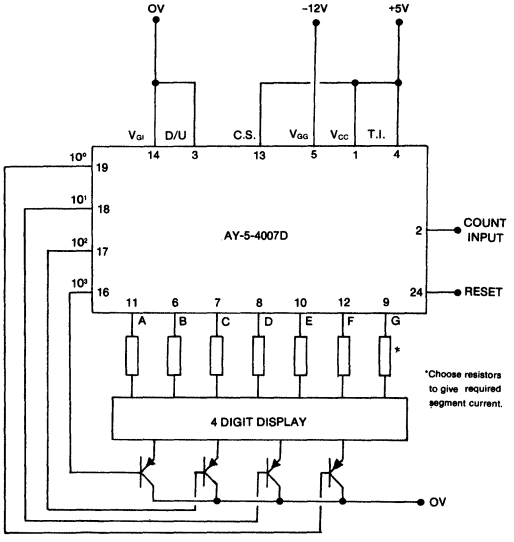


Fig.7 COMMON CATHODE LED DISPLAY

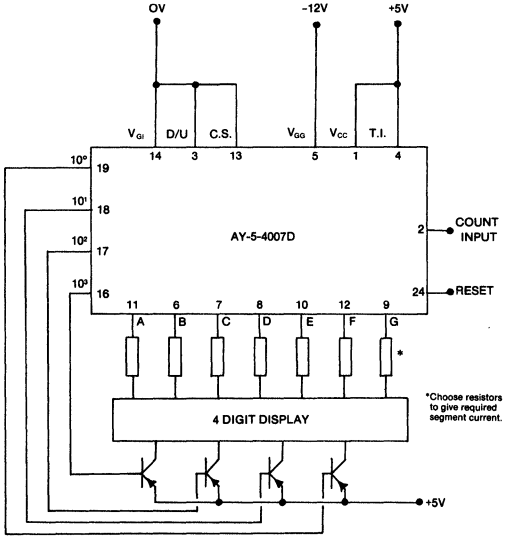


Fig.8 COMMON ANODE LED DISPLAY

TYPICAL CHARACTERISTIC CURVES

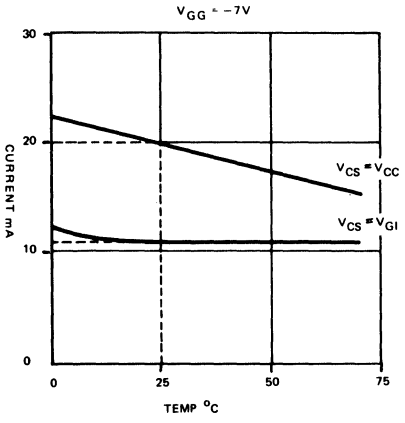


Fig.9

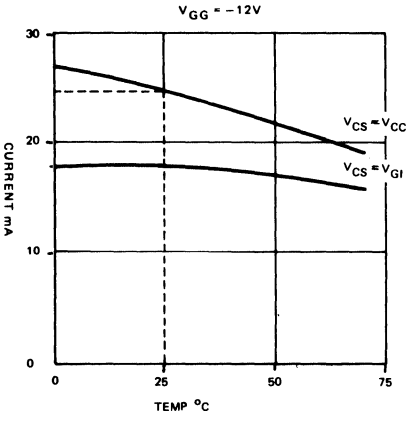


Fig.10

TYPICAL CURVES OF SEGMENT CURRENT VS. TEMPERATURE AT 1V ACROSS OUTPUT DEVICE

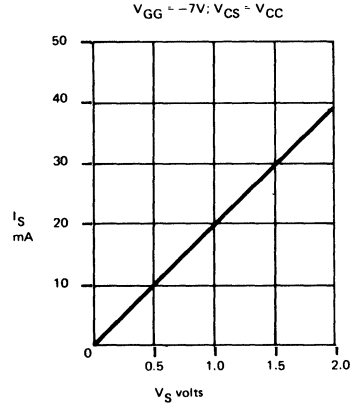


Fig.11

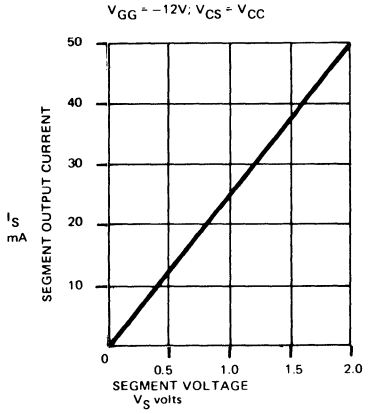


Fig.12

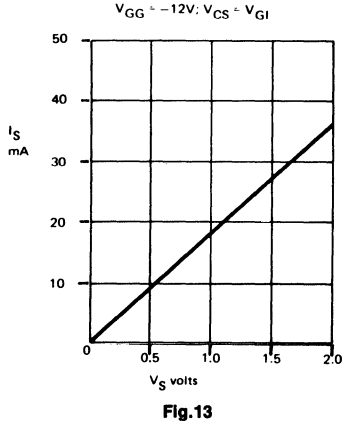


Fig.13

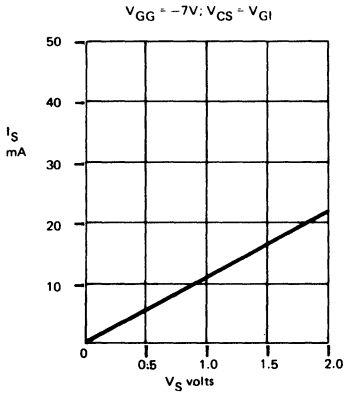


Fig.14

TYPICAL SEGMENT OUTPUT CURRENT V_S OUTPUT VOLTAGE AT +25°C

9

Four Digit Counter

FEATURES

- Fully static operation.
- Maximum clock input 500kHz.
- Reset input.
- Multiplexed outputs.
- Final Carry output and two intermediate carry outputs.
- TTL/DTL compatible inputs and outputs.

DESCRIPTION

The AY-5-4057 is a fully static four digit counter capable of accepting a count frequency of up to 500kHz. The four counters are connected in series, each having a 4-bit store associated with it. The counters change on the negative going clock transition, and the counter outputs are transferred to the 4-bit stores when the load control is taken to Logic '0'.

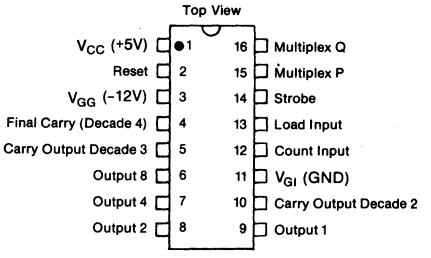
The count held in the four stores is strobed out in sequence by a signal derived from the 'Strobe Input'. The multiplexed BCD outputs are output in sequence and are capable of driving a decoder/driver. The 'Strobe Input' operates on a positive transition (0 to 1), and the multiplex outputs, P and Q are in a 2-bit binary sequence.

In addition to the count outputs, the device has a 'Final Carry Out-put' (CO 4) and two intermediate carry outputs, CO2 and CO3, from the second and third decades respectively.

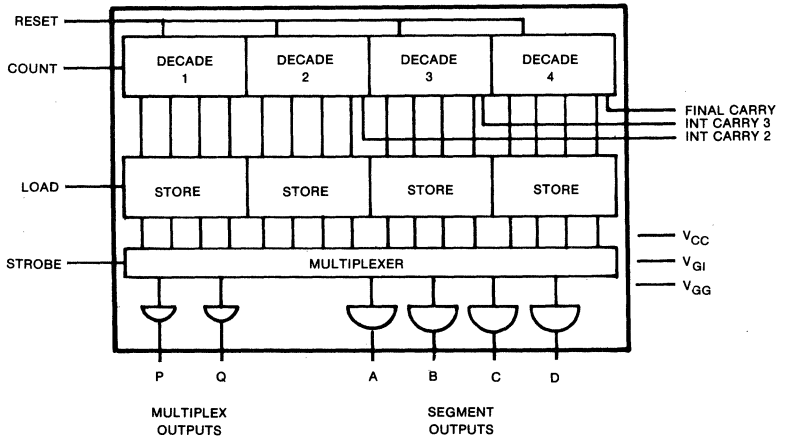
A reset line is provided to reset all four decades to the zero state.

PIN CONFIGURATION

16 LEAD DUAL IN LINE



BLOCK DIAGRAM

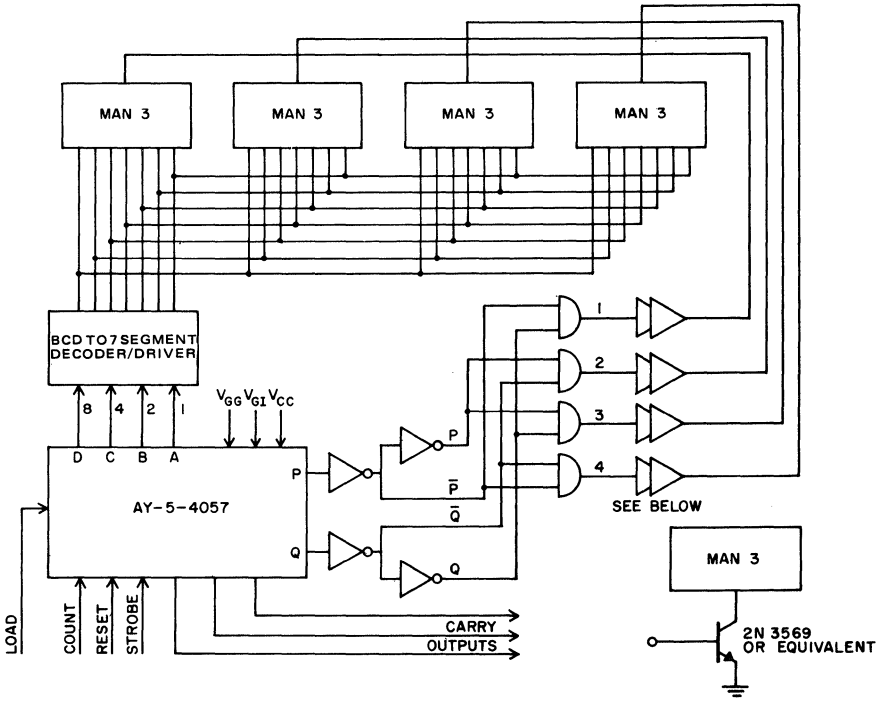


PIN FUNCTIONS

Name	Functions
COUNT INPUT	A negative going (1 to 0) signal on this input causes the counter to be incremented by one.
LOAD INPUT	A logic '0' level on this input causes the contents of the four counters to be transferred to the store. To store any one count, the load input must go to logic '0' a minimum of 800 nSec after the count pulse that sets up the count to be stored. (ts1 on timing diagram) and stay at logic '0' for a minimum of 1 μSec.
RESET	A logic '1' level applied to this input will reset all four counters to the all '0's state. (Store is not reset). A delay of 250 nSec must be allowed (ts2 of timing/diagram) after the reset goes to logic '0' before a count is started.
STROBE	A positive going ('0' to '1') signal on this input clocks the multiplex counter thereby causing the count to be output in the correct sequence.
P & Q OUTPUTS	The two Multiplex outputs P and Q, identify which decade is being output. P Q 1 0 Strobes decade 1 0 1 Strobes decade 2 1 1 Strobes decade 3 0 0 Strobes decade 4
***INTERMEDIATE CARRY (CO2)**	This output is generated by the second decade of the counter.
***INTERMEDIATE CARRY (CO3)**	This output is generated by the third decade of the counter.
***FINAL CARRY**	This output is generated by the fourth decade of the counter.

*All carry outputs go to logic '1' on count 8 and return to logic '0' on count 10.

COUNTER-DISPLAY INTERFACE



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Max. voltage between V_{CC} and any pin. . . . . −20V to 0.3V
Operating Temperature Range. . . . . 0°C to +70°C
Storage Temperature Range . . . . . −65°C to +150°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

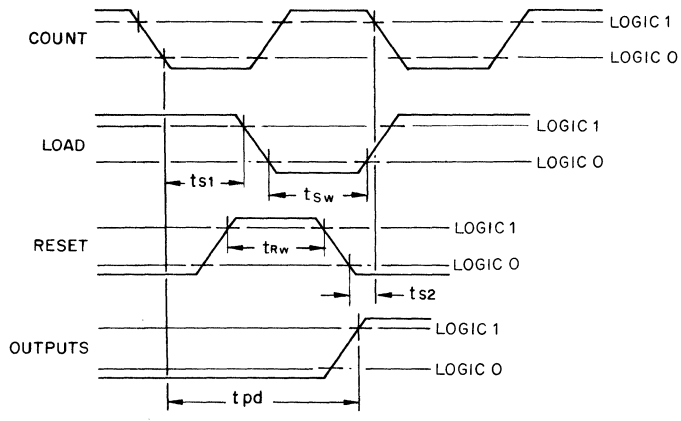
Standard Conditions (unless otherwise noted)

V_{GG} = −12V ±1V
V_{CC} = +5.0 ±0.5V
V_{GI} = OV

Operating Temperature (T_A) = 0°C to +70°C
Output Loading + 1 TTL Load
CL TOTAL = 10 pF

Characteristic	Min	Max	Units	Conditions
Count Input				
Repetition Rate	DC	500	kHz	
Rise/Fall Times	—	10	μs	
Logic '0'	—	+0.8	V	
Logic '1'	V_{CC}−1.5	—	V	
Input Capacitance	—	5	pF	$V_{IN}=V_{CC}$
Load Input				
Pulse Width t_{SW}	1.0	—	μs	
Set-up Time ts1	800	—	ns	
Logic '0'	—	+0.8	V	
Logic '1'	V_{CC}−1.5	—	V	
Input Capacitance	—	10	pF	$V_{IN}=V_{CC}$
Strobe Input				
Repetition Rate	DC	10	kHz	
Pulse Width	10	—	μs	
Rise/Fall Times	—	10	μs	
Logic '0'	—	+0.8	V	
Logic '1'	V_{CC}−1.5	—	V	
Input Capacitance	—	5.0	pF	$V_{IN}=V_{CC}$
Reset Input				
Pulse width t_{RW}	1	—	μs	
Set-up-Time ts2	250	—	ns	
Logic '0'	—	+0.4	V	
Logic '1'	V_{CC}−1.5	—	V	
Input Capacitance	—	10	pF	
Outputs				
Logic '0'	—	+0.4	V	I_{OL} = 1.6mA
Logic '1'	V_{CC}−1.0	—	V	I_{OH} = 100μA
Propagation delay tpd	—	2.0	μs	
Input Leakage	—	5.0	μA	$V_{in}=V_{CC}$−10V. at 25°C
Power	—	350	mW	

TIMING DIAGRAM



10 Bit D/A Convertor

FEATURES

- 10 Bit resolution.
- 8 Bit accuracy (linearity).
- Parallel or serial input.
- Simple external circuitry.
- Binary or 2's complement coding.
- Output inversion.
- TTL/CMOS compatible inputs.
- Monotonic output.
- 6.8mS settling time for 10 bits with 2nd order filter.
- 1.23mS settling time for 8 bits with 2nd order filter.

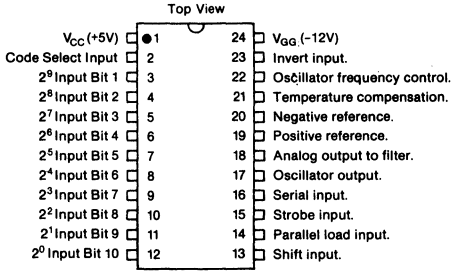
DESCRIPTION

The AY-5-5053 is a 10 bit D/A convertor employing the stochastic conversion technique, requiring no precision components other than a voltage reference.

The input can be either serial or parallel with Binary or 2's complement coding.

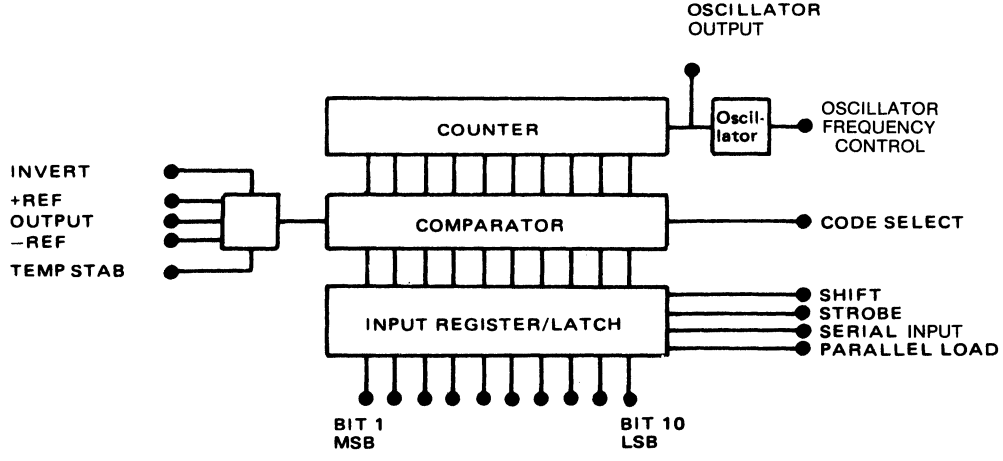
PIN CONFIGURATION

24 LEAD DUAL IN LINE



See next page for details of Pin Functions.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{CC} pin . . −20 to + 0.3 Volts
Ambient operating temperature range . . . . . 0°C to +70°C
Storage temperature range . . . . . −65°C to +150°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5V ± 0.5V
V_{GG} = −12V ± 0.5V
Positive reference = +4.5V
Negative reference = OV

Clock Frequency = 800KHz
R_T (temp comp) = 12K Ω 5%
R_L (linearity) = 270 Ω nom
R_O (osc. frequency) = 10K Ω nom

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Frequency	100	800	1000	KHz	
Voltage Stability	—	5	—	%/V	
Temp. Stability	—	0.2	—	%/°C	
Output Logic '0'	—	—	0.4	Volt	R_L =6.8K to V_{GG} I sink = 1.6mA
Output Logic '1'	V_{CC}−1	—	—	Volt	R_L =6.8K to V_{GG} I source = 100μA
Inputs					
Logic '0' Level	—	—	+0.8	Volts	
Logic '1' Level	V_{CC}−1.5	—	—	Volts	
Leakage Current	—	—	10	μA	$V_{IN} = V_{CC}$ −5V
Capacitance	—	—	10	pF	
Shift Clock Frequency	10	—	1000	KHz	
Resolution	—	10	—	Bits	
Differential Linearity	—		¼	LSB	
Linearity	—	0.5	2	LSB	After trimming at 0.5 FSD
Temperature Co-efficient	—	60	—	PPM/C°	Excluding reference and filter drift
Supply current	—	—	20	mA	(140mW)
Reference Current	—	—	100	μA	Max at ½FSD

**Typical values are at +25°C and nominal voltages.

TABLE 1 INPUT CODING

BINARY	2's COMPLEMENT	ANALOG OUTPUT
0000000000	1000000000	0
0000000001	1000000001	+LSB
0111111111	1111111111	½V ref — LSB
1000000000	0000000000	½V ref
1000000001	0000000001	½V ref + LSB
1111111111	0111111111	V ref — LSB

SETTLING TIME AND BANDWIDTH D/A CONVERTOR

NO. OF BITS	10		8		6	
Filter Type	1st Order	2nd Order	1st Order	2nd Order	1st Order	2nd Order
Filter time constant mSec	5.3	0.66	1.1	0.16	0.2	0.08
Settling time to ± ½ LSBmSec	45	6.8	7.7	1.23	0.8	0.32
Bandwidth Hz — 0.1%	1.35	14.8				
— 0.4%			13	118		
—1%					112	618
— 1dB	13.5	135	65	537	400	1784

PIN FUNCTIONS

Pin No.	Name	Function
1	V_{CC}	Positive power supply +5V
2	Code Select Input	Logic '0' gives Binary coding. Logic '1' gives 2's complement coding. (See table 1).
3-12	Bits 1-10 Input	Parallel data inputs. Bit 1 is MSB.
13	Shift Input	Clock input for serial mode. Data is shifted in on the '0' to '1' logic transition. In the parallel mode this input must be at logic '1'.
14	Parallel Load Input	In the parallel mode data is loaded into the data register when this input is at logic '1'. This input should be at logic '0' in parallel mode operation.
15	Strobe Input	A logic '1' on this input loads serial data into the data register. The data is latched when the input returns to logic '0'. This input should be at logic '0' in parallel mode operation.
16	Serial Input	Serial data input Bit 1 first.
17	Oscillation Output	TTL compatible oscillator output signal.
18	Analog Output	Analog output to low pass filter. This output is a stochastic pulse waveform having a mean amplitude equal to the required DC output level.
19	Positive Reference	+4.5V nominal reference of voltage.
20	Negative Reference	0V reference, connected to 0V via a 500 ohm variable resistance used to adjust the error at half scale to zero.
21	Temperature Compensation	This pin is connected to V_{GG} via a 12K ohm 5% resistor to achieve the stated temperature stability. The temperature stability can be improved by a factor of 4 by using an 18K Ω resistor in parallel with a DPGC49–39K Ω thermistor instead of the 12K Ω resistor.
22	Oscillator Frequency Control	This pin is connected to V_{GG} via a 50 K Ω variable resistor used to adjust the oscillator frequency to the required value.
23	Invert Input	A logic '1' on this input inverts the output.
24	V_{GG}	Negative power supply −12V.

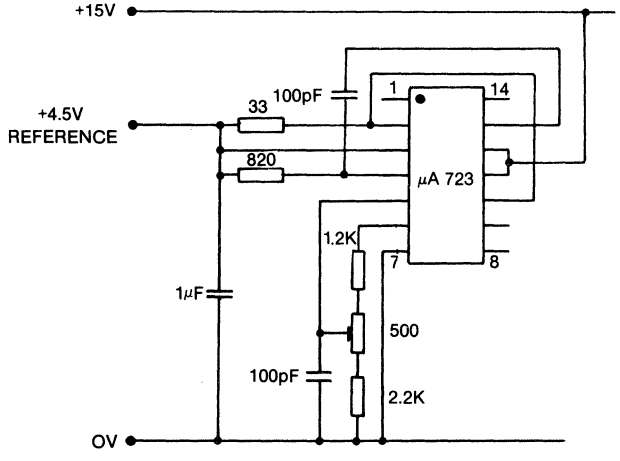
OPERATION

The binary word contained in the input register is compared with the output of a continuously cycling counter. The output of the comparator is high whenever the binary input is greater than the counter, this results in an output waveform which has a mean value equal to the desired analog output. This output is passed through a low pass filter to recover the DC level.

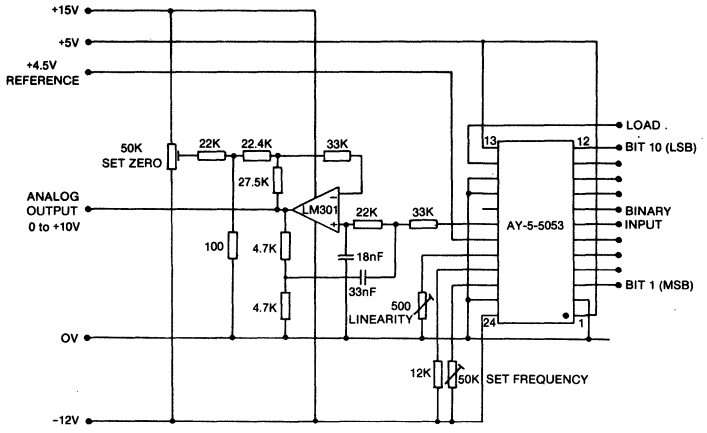
The counting sequence of the binary counter has been chosen to optimise the conversion characteristics and the frequency of the output noise to simplify the filtering.

MULTIPLIER OPERATION

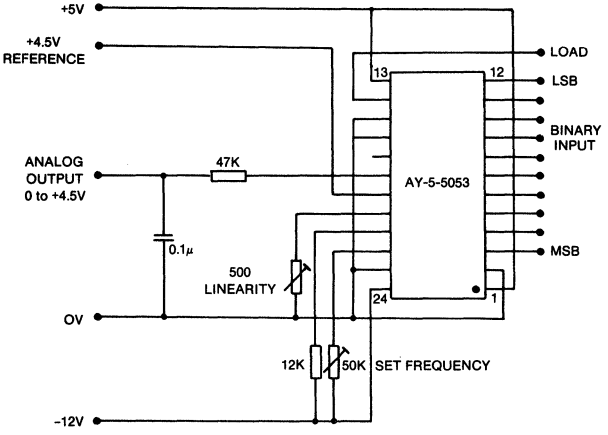
The AY-5-5053 may be used as a Digital—Analog multiplier by replacing the positive reference with the Analog multiplier. Input voltages in the range 0 to +4.5 volts may be used. The accuracy is of the order of 0.1% and the settling time is as for normal operation.



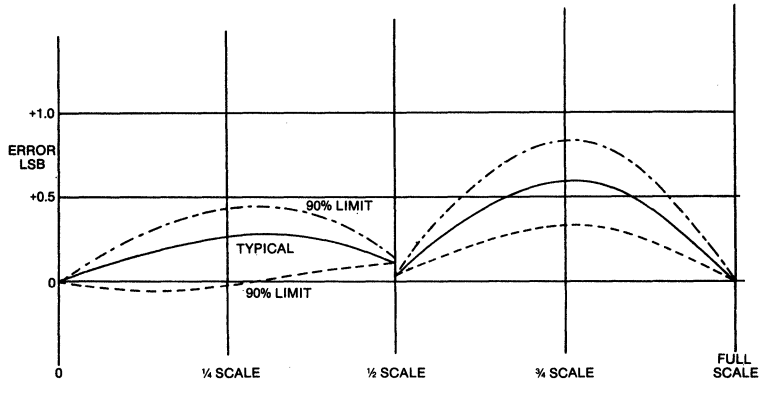
+4.5V REFERENCE SUPPLY



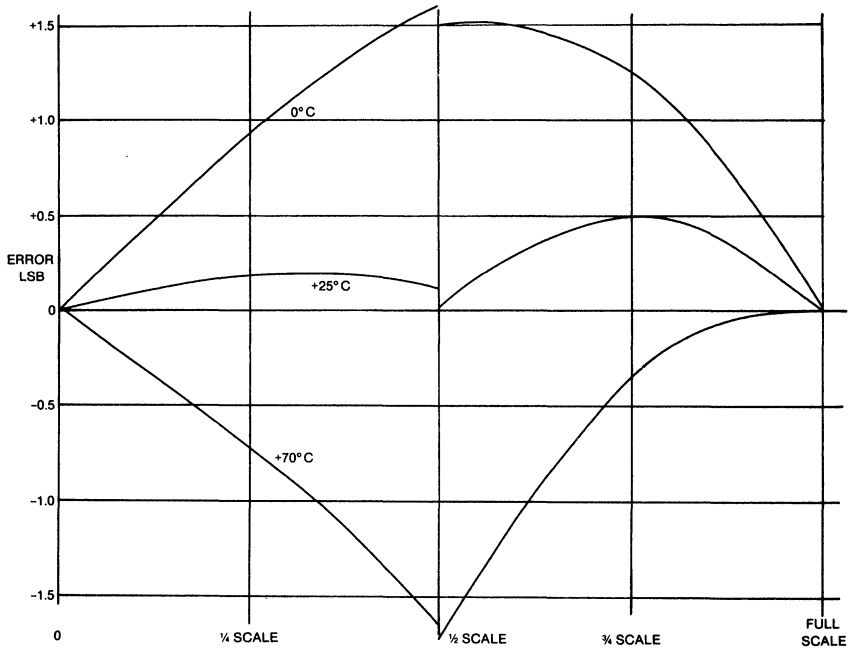
10 BIT D/A CONVERTOR PARALLEL INPUT SECOND ORDER FILTER 0 to +10V OUTPUT



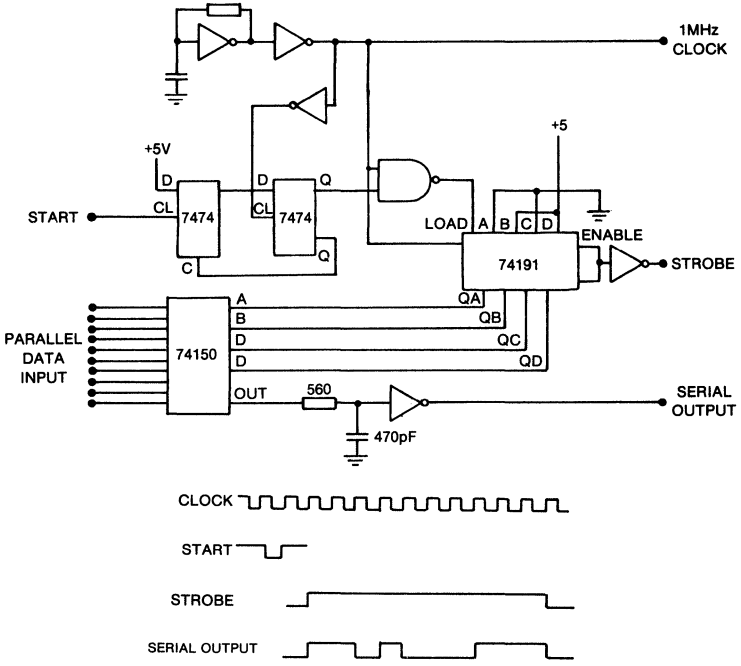
10 BIT D/A CONVERTOR FIRST ORDER FILTER



D/A CONVERTOR LINEARITY



D/A CONVERTOR TYPICAL TEMPERATURE STABILITY



SERIAL DATA TRANSMITTER FOR AY-5-5053 D/A CONVERTOR

10 Bit A/D Convertor Control

FEATURES

- 10 Bit Resolution
- 200mS settling time to ± ½ LSB
- Integral serial data transmitter 8/10 Bits with parity
- Parallel outputs
- TTL/MOS compatible inputs and outputs

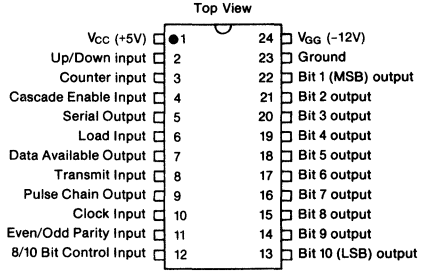
DESCRIPTION

The AY-5-5054 is designed to work in conjunction with the AY-5-5053 to form a 10 Bit A/D convertor. It consists of a 10 bit up/down counter, control logic and a serial data transmitter.

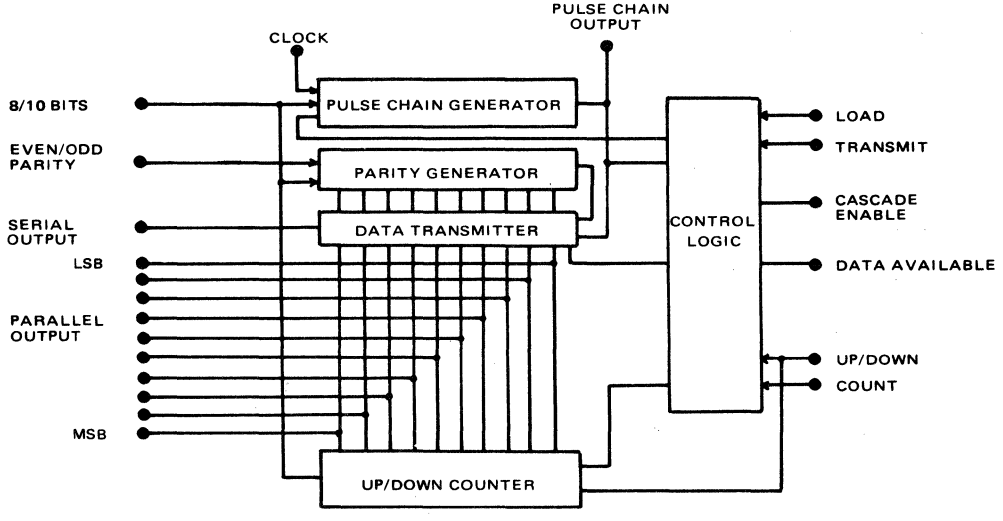
PIN CONFIGURATION

24 LEAD DUAL IN LINE

Top View



BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Name	Function
1	V_{CC}	Positive Power supply (+5V)
2	UP/DOWN	Controls direction of counting, at logic '1' for UP.
3	Counter Input	Clock input for UP/DOWN counter. Control logic inhibits the clock during UP/DOWN transition, during loading of the transmitter and when the counter has reached all '0's or all '1's.
4	Cascade Enable Output	This output goes to logic '1' at the end of data transmission for one clock cycle. It can be connected to the Transmit input of a second AY-5-5054, enabling a series of convertors to be interrogated sequentially using only one line.
5	Serial Output	Serial data output from transmitter, 8 or 10 bits plus parity. MSB first.
6	Load Input	A pulse to logic '1' on this input loads data into the transmitter. If data is being transmitted the command is stored until the transmission is complete.
7	Data Available Output	This output goes to logic '1' when valid data has been loaded into the transmitter. It returns to logic '0' when the transmission has been completed.
8	Transmit Input	A pulse to logic '1' on this input causes transmission to commence. The pulse must last at least one but no more than 8 clock periods.
9	Pulse Chain Output	A chain of 9 or 11 pulses is output on this line during data transmission. It would be used to clock data into the receiver.
10	Clock Input	Clock for the data transmitter 1MHz max.
11	Even/Odd Parity Input	Logic '1' gives even parity.
12	8/10 Bit Control Input	Logic '1' gives 8 bit data transmission.
13-22	Parallel Data Outputs	Connect to Parallel inputs of AY-5-5053.
23	Ground	
24	V_{GG}	Negative power supply (−12V).

A/D CONVERTOR RESPONSE TIME

1. SIMPLE TYPE – 1ST ORDER FILTER

NO. OF BITS	10	8	6
Filter time constant	4.5mSec	1.2mSec	0.3mSec
Clock frequency	10KHz	40KHz	160KHz
Settling time to $^1/_2$LSB	200mSec	50mSec	12.5mSec

2. VARIABLE CLOCK FREQUENCY TYPE

If the counter clock frequency is arranged to be proportional to the difference between the input voltage and the actual convertor output, the response speed can be considerably improved. In this case the system becomes a linear one and a 2nd order filter can be used without danger of oscillation.

NO. OF BITS	10	8
Filter time constant	0.66mSec	0.164mSec
Settling time to $^1/_2$LSB	1.5mSec	3mSec
Max. clock frequency	450KHz	1MHz

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin . . . −20 to +0.3 Volts
Ambient Operating Temperature range. . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these condition is not implied—operating ranges are specified below.

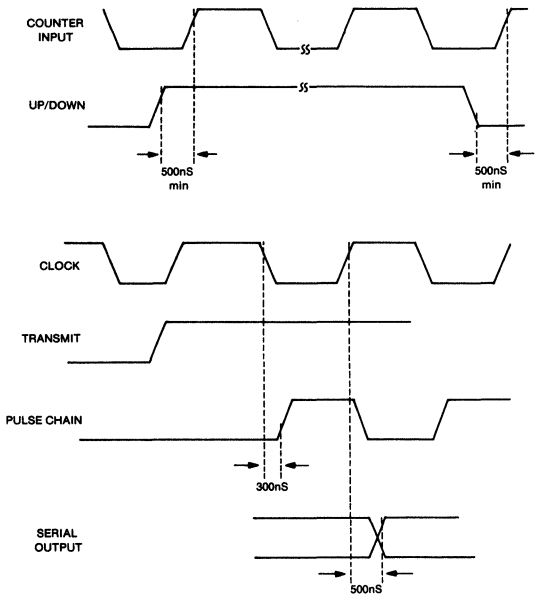
Standard Conditions (unless otherwise noted)

V_{CC} = +5 ±0.5V
V_{GG} = −12 ±0.5V
Operating Temperature (T_A) = 0°C to +70°C

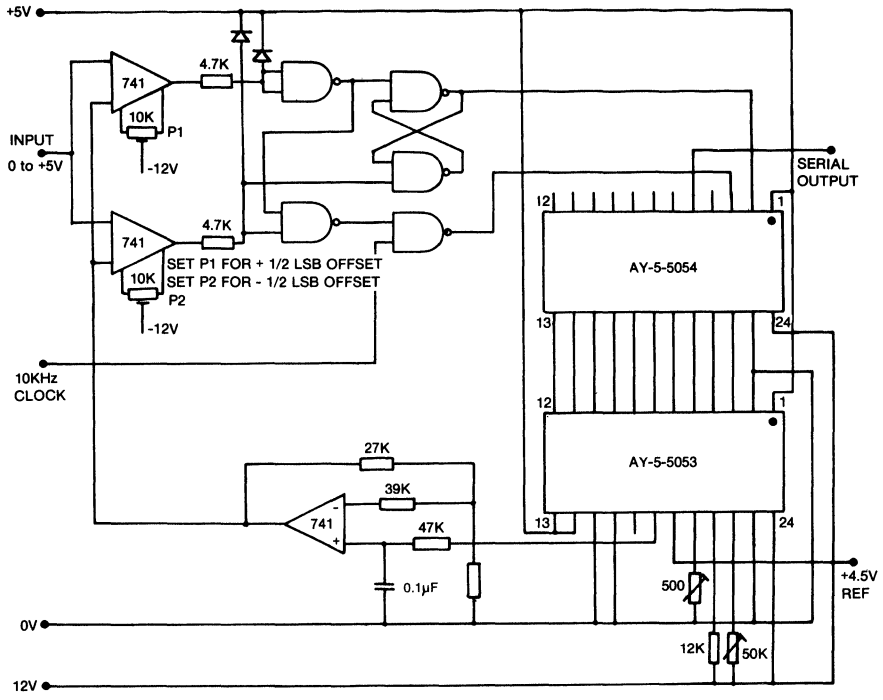
Characteristic	Min	Typ**	Max	Units	Conditions
Clock and Clock Inputs					
Logic '0' level	—	—	+0.8	Volts	
Logic '1' level	V_{CC}−1.5	—	V_{CC}+0.3	Volts	
Frequency	DC	—	1	MHz	
Capacitance	—	—	10	pF	
Leakage	—	—	10	μA	$V_{IN}=V_{CC}-10V$
Logic Inputs					
Logic '0' level	—	—	+0.8	Volts	
Logic '1' level	V_{CC}−1.5	—	V_{CC}+0.3	Volts	
Capacitance	—	—	10	pF	
Leakage	—	—	10	μA	$V_{IN}=V_{CC}-10V$
Output					
Logic '0' level	—	—	+0.4	Volts	I_{OL}=1.6mA
Logic '1' level	V_{CC}−1	—	—	Volts	I_{OH}=100μA
Power	—	240	—	mW	

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS



SIMPLE 10 BIT A/D CONVERTOR



GENERAL INSTRUMENT

CP1600
CP1600A
GIMINI
CC1600
GP1600
I/O1600
MC1600
PM1600
RM1600
RM1601
S1600
SAL1600
PIC1640
PIC1650
LP8000
LP6000
LP1030
LP1010
LP1000

10

16-Bit Single-Chip Microprocessor

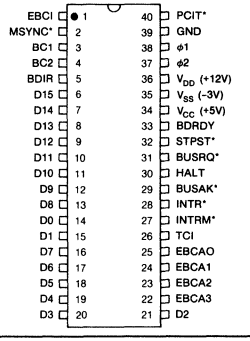
FEATURES

- 8 program accessible 16-bit general purpose registers
- 87 basic instructions
- 4 addressing modes: immediate, direct, indirect, relative
- Conditional branching on status word and 16 external conditions
- Unlimited interrupt nesting and priority resolution
- 16-bit 2's complement arithmetic & logic
- Status word: carry, overflow, sign, zero
- Direct memory access (DMA) for high speed data transfer
- 64k memory using single address
- TTL compatible/simple bus structure
- 600ns cycle time 3.3 MHz 2-phase clock—CP1600
- 400ns cycle time 5 MHz 2-phase clock—CP1600A

PIN CONFIGURATION

40 LEAD DUAL IN LINE

Top View



*ACTIVE LOW LEVEL

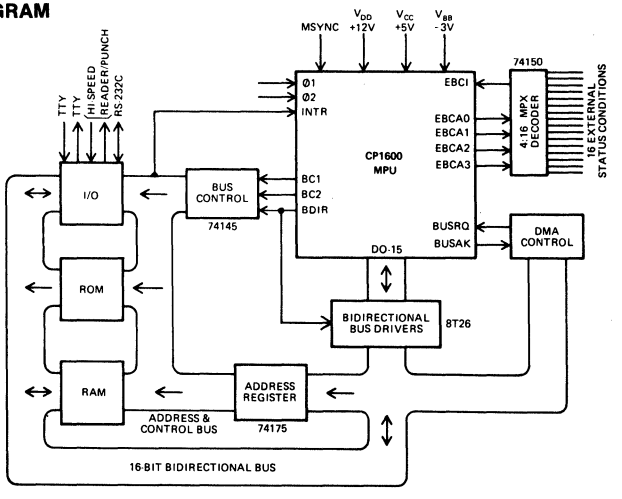
DESCRIPTION

The CP1600/1600A Microprocessor Units are compatible members of the Series 1600 MicroProcessor Products family. Each is a complete, 16-bit, single chip, high speed MOS-LSI Microprocessor. The Series 1600 family is fabricated with General Instrument's N-Channel Ion-Implant GIANT II process, insuring high performance with proven reliability and production history. All members of the Series 1600 family, including Programmable Interface Controllers, Read Only Memories, and Random Access Read/Write Memories are fully compatible with the CP1600/1600A.

The CP1600/1600A Microprocessor Units are designed for high speed data processing and real time applications. Using a 3.3 MHz 2-phase clock, the CP1600 completes a microcycle in 600 nanoseconds. The CP1600A, using a 5 MHz 2-phase clock, completes a microcycle in 400ns. Typical applications include programmable calculator systems, peripheral controllers, process controllers, intelligent terminals and instruments, data acquisition and digital communications processors, numerical control systems and many general purpose mini-computer applications. The Microprocessor can readily support a variety of peripheral equipment such as TTY, CRT display, tape reader/punch, A/D & D/A converter, keyboard, cassette tape, floppy disk, and RS-232C data communication lines.

The CP1600/1600A utilizes third generation minicomputer architecture with eight general purpose registers to achieve a versatile, sophisticated microcomputer system. The 16-bit word enables fast and efficient processing of alpha-numeric or byte oriented data. The 16-bit address capability permits access to 65,536 words in any combination of program memory, data memory, or peripheral devices. This single address space concept, combined with a powerful instruction set and microprogrammable Peripheral Interface devices, provides an efficient solution to microcomputer and many minicomputer-based product requirements.

CP1600 SYSTEM DIAGRAM



PROCESSOR SIGNALS

DATA BUS

D0-D15
Input/Output/High Impedance

Data 0-15: 16-bit bidirectional bus used to transfer data, addresses, and instructions between the microprocessor, memory, and peripheral devices.

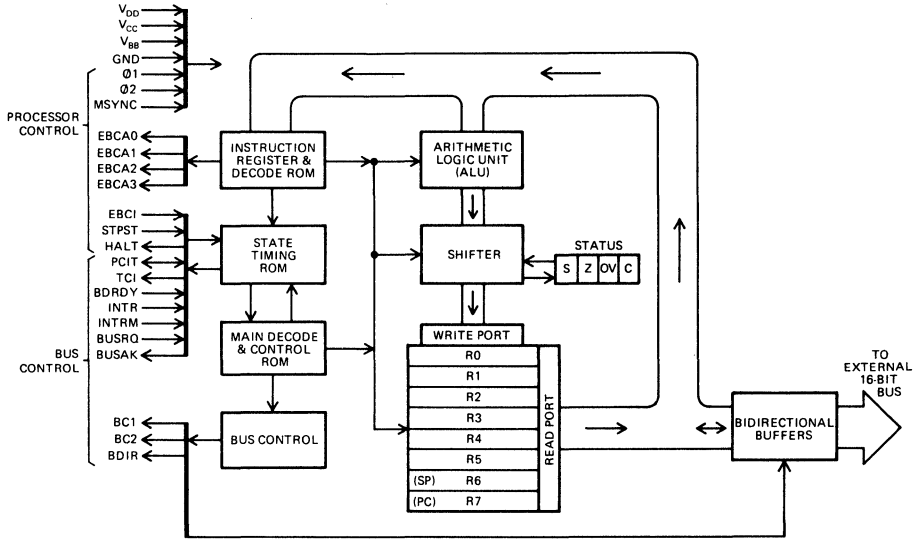
PROCESSOR CONTROLS

STPST
Input
STop-STart: Edge-triggered by negative transition; used to control the running condition of the microprocessor.
HALT
Output
HALT: indicates that the microprocessor is in a stopped mode.
MSYNC
Input
Master SYNC: Active low input synchronizes the microprocessor to the $\phi 1$, $\phi 2$ clocks during power-up initialization.
EBCA 0-3
Outputs
External Branch Condition Addresses 0-3: Address for one-of-16 external digital state tests via the BEXT (Branch on EXTernal) instruction.
EBCI
Input
External Branch Condition Input: Return signal from the one-of-16 selection made by EBCA 0-3.

BUS CONTROL SIGNALS

BDIR, BC1, BC2
Outputs
Bus DIRection, Bus Controls 1, 2: Bus control signals externally decoded to define the state of bus operations (see State Flow Diagram).
BUSRQ*
Input
BUSAK*
Output
BUS ReQuest, BUS AcKnowledge: BUSRQ* requests the microprocessor to relinquish control of the bus indefinitely. BUSAK* informs devices that the bus has been released.
BDRDY
Input
Bus Data ReaDY: causes the microprocessor to "wait" and resynchronize to slow memory and peripheral devices.
INTR*, INTRM*
INTeRupt, INTeRupt Masked: request the microprocessor to service an interrupt upon completion of current instruction.
TCI
Output
Terminate Current Interrupt: pulse outputted by the microprocessor in response to the TCI instruction.
PCIT
input/output
Program Counter Inhibit/Trap: As an input, inhibits incrementation of the Program Counter during the instruction fetch sequence. As an output, generates a pulse during execution of a Software INterrupt (SIN) instruction.

CP1600 INTERNAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD}, V_{CC}, GND and all other input/output voltages with respect to V_{BB} . . . . . −0.3V to +18.0V
Storage Temperature . . . . . −55°C to +150°C
Operating Temperature . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage to these devices. Functional operation at these conditions is not implied—operating conditions are specified below.

Standard Conditions: (unless otherwise noted)

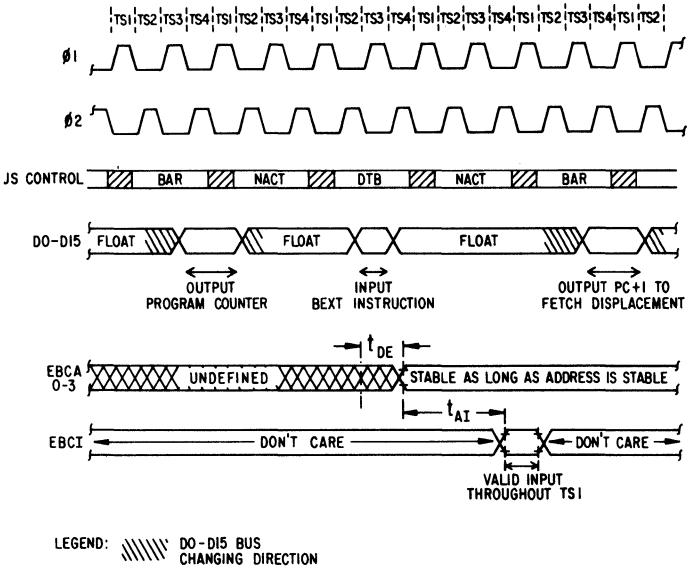
V_{DD}=+12V±5%, 70mA(typ)
V_{CC}=+5V±5%, 12mA(typ)
V_{BB}= −3V±10%, 0.2mA(typ)
Operating Temperature (T_A)=0°C to +70°C

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Inputs						
High	V_{IHC}	10.4	—	V_{DD}	V	
Low	V_{ILC}	0	—	0.6	V	
Logic Inputs						
Low	V_{IL}	0	—	0.65	V	
High (All Lines except BDRDY)	V_{IH}	2.4	—	V_{CC}	V	
High (Bus Data Ready Line See Note 1)	V_{IHB}	3.0	—	V_{CC}	V	
Logic Outputs						
High	V_{OH}	2.4	V_{CC}		V	I_{OH} = 100μA
Low (Data Bus Lines DO-D15)	V_{OL}	—	—	0.5	V	I_{OL} = 1.6mA
Low (Bus Control Lines, BC1,BC2,BDIR)	V_{OL}	—	—	0.45	V	I_{OL} = 2.0mA
Low (All Others)	V_{OL}	—	—	0.45	V	I_{OL} = 1.6mA
AC CHARACTERISTICS						
Clock Pulse Inputs, $\phi1$ or $\phi2$						
Pulse Width	$t_{\phi2}$, $t_{\phi2}$	120(CP1600) 70(CP1600A)	—	—	ns	
			—	—	ns	
Skew ($\phi1$, $\phi2$ delay)	t_{12}, t_{21}	0	—	—	ns	
Clock Period	t_{cy}	0.3(CP1600) 0.2(CP1600A)	—	2.0	μs	
Rise & Fall Times	tr, tf	—	—	15	ns	
Master SYNC:						
Delay from ϕ	tms	—	—	30	ns	
DO-D15 Bus Signals						
Output delay from $\phi1$ (float to output)	t_{BO}	—	—	120(CP1600) 70(CP1600A)	ns	1 TTL Load & 25 pF
Output delay from $\phi2$ (output to float)	t_{BF}	—	50	—	ns	
Input setup time before $\phi1$	t_{B1}	0	—	—	ns	
Input hold time after $\phi1$	t_{B2}	10	—	—	ns	
Bus Control Signals BC1,BC2,BDIR						
Output delay from $\phi1$	t_{DC}	—	—	120(CP1600) 70(CP1600A)	ns	
BUSAK Output delay from $\phi1$	t_{BU}	—	150	—	ns	
TCI Output delay from $\phi1$	t_{TO}	—	200	—	ns	
TCI Pulse Width	t_{TW}	—	300	—	ns	
EBCA output delay from BEXT input	t_{DE}	—	—	150	ns	
EBCA wait time for EBCI input	t_{AI}	—	—	400	ns	
CAPACITANCE						TA = +25°C; V_{DD} = +12V; V_{CC} = +5V; V_{BB} = −?V; $t\phi1$ $t\phi2$ = 120ns
$\phi1$, $\phi2$ Clock Input capacitance	C$\phi1$, C$\phi2$	—	20	30	pF	
Input Capacitance						
DO-D15	CIN	—	6	12	pF	
All Other	—	—	5	10	pF	
Output Capacitance						
DO-D15 in high impedance state	C_D	—	8	15	pF	

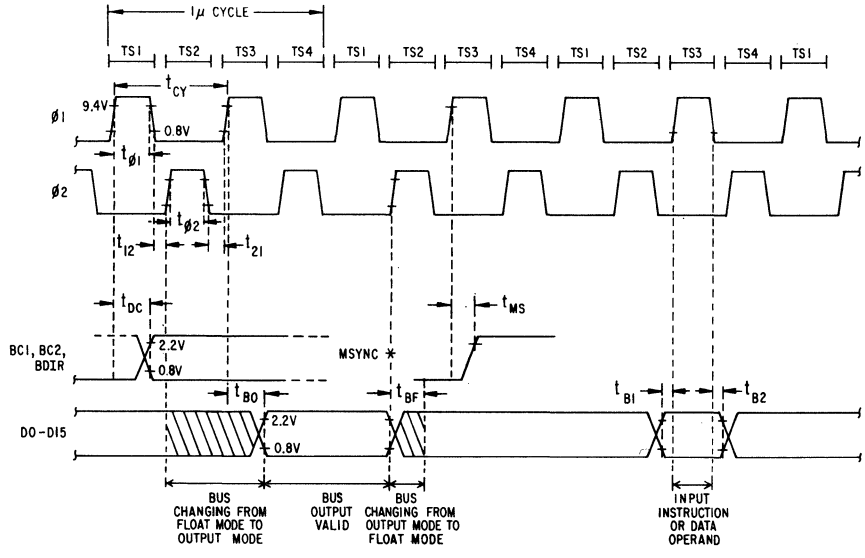
**Typical values are at +25°C and nominal voltages.

NOTE:
1. The Bus Data ReaDY(BDRDY) line is sampled during time period TSI after a BAR or ADAR bus control signal. BDRDY must go low requesting a wait state 50 ns before the end of TS1 and remain low for 50 ns minimum. BDRDY may go high asynchronously. In response to BDRDY, the CPU will extend bus cycles by adding additional microcycles up to a maximum of 40 μsec duration.

BUS TIMING DIAGRAM

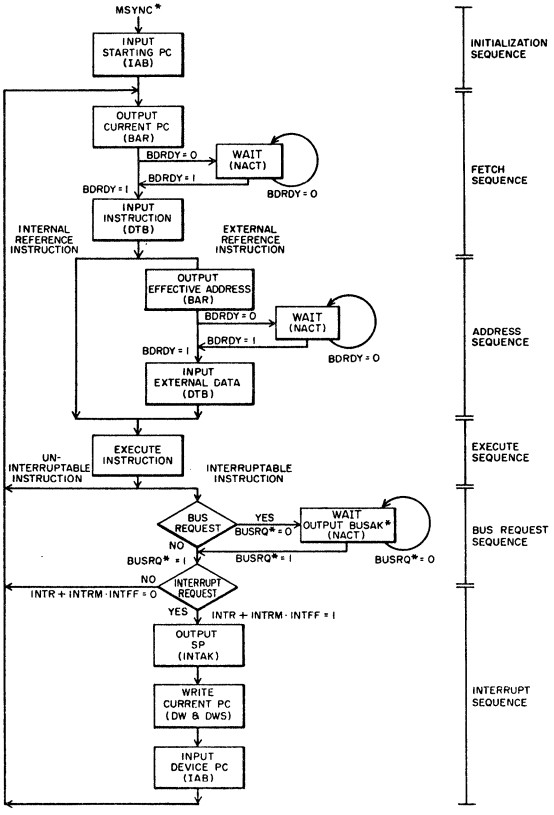


TYPICAL INSTRUCTION SEQUENCE



BRANCH ON EXTERNAL CONDITION INSTRUCTION

SIMPLIFIED STATE FLOW DIAGRAM



BUS CONTROL SIGNALS

BDIR	BC1	BC2	Signal	Decoded Function
0	0	0	NACT	No ACTion, D0-D15 = high impedance
0	0	1	IAB	Interrupt Address to Bus, D0-D15 = Input
0	1	0	ADAR	Address Data to Address Register, D0-D15 = high impedance
0	1	1	DTB	Data to Bus, D0-D15 = Input
1	0	0	BAR	Bus to Address Register
1	0	1	DWS	Data Write Strobe
1	1	0	DW	Data Write
1	1	1	INTAK	INTerrupt AcKnowledge

INSTRUCTION SET SUMMARY

		Mnemonics	Operation	Microcycles Dir.	Indr.	Imm.	Stack	Comments
External Reference Instructions	Arithmetic & Logic	ADD	ADD	10	8	8	11	
		SUB	SUBtract	10	8	8	11	
		CMP	CoMPare	10	8	8	11	Result not saved
		AND	logical AND	10	8	8	11	
		XOR	eXclusive OR	10	8	8	11	
	I/O	MVO	MoVe In	10	8	8	11	
		MVI	MoVe In	10	8	8	11	
Internal Register Instructions	Register to Register	ADDR	ADD contents of Registers	6				Add one cycle
		SUBR	SUBtract contents of Registers	6				if Register 6 or 7, except*.
		CMPR	CoMPare Registers by subtr.	6				Result not saved
		ANDR	logical AND Registers	6				
		XORR	eXclusive OR Registers	6				
		MOVR	MOVe Register	6				
	Single Register	CLRR	CLeaR Register	6				XORR with itself
		TSTR	TeST Register	6				
		JR	Jump to address in Register	7*				PC←(RRR)
		INCR	INCrement Register	6				
		DECR	DECrement Register	6				
		COMR	COMplement Register	6				One's Complement
		NEGR	NEGate Register	6				Two's Complement
		ADCR	ADd Carry Bit to Register	6				
		GSWD	Get Status WorD	6				
		NOP	No OPeration	6				Two Words
		SIN	Software INterrupt	6				Pulse to PCIT pin
		RSWD	Return Status WorD	6				
		PULR	PULl from stack to Register	11*				PULR=MVI @ R6
		PSHR	PuSH Register to stack	9*				PSHR=MVO @ R6
	Register Shift	SLL	Shift Logical Left	6				one or two position shift capability. Add two cycles for 2-position shift
		RLC	Rotate Left thru Carry	6				
		SLLC	Shift Logical Left thru Carry	6				
		SLR	Shift Logical Right	6				
		SAR	Shift Arithmetic Right	6				
		RRC	Rotate Right thru Carry	6				
		SARC	Shift Arithmetic Right thru Carry	6				
		SWAP	SWAP 8-bit bytes	6				2-position=SWAP twice
Control Instructions		HLT	HaLT	4				
		SDBD	Set Double Byte Data	4				Must precede external reference to double byte data
		EIS	Enable Interrupt System	4				
		DIS	Disable Interrupt System	4				
		TCI	Terminate Current Interrupt	4				Not Interruptible
		CLRC	CLeaR Carry to zero	4				
		SETC	SET Carry to one	4				
Jump Instructions		J	Jump	12				
		JE	Jump, Enable, interrupt	12				
		JD	Jump, Disable interrupt	12				
		JSR	Jump, Save Return	12				Return Address saved in R4, 5 or 6
		JSRE	Jump, Save Return & Enable	12				
		JSRD	Jump, Save Return & Disable Interrupt	12				
Conditional Branch Instructions		B	unconditional Branch	7				Displacement in PC+1
		BC, BLGE	Branch on Carry, C=1	7				PC←PC±Displacement
		BNC, BLLT	Branch on No Carry, C=0	7				Add 2 cycles if test condition
		BOV	Branch on OVerflow, OV=1	7				is true.
		BNOV	Branch on No OVerflow, OV=0	7				
		BPL	Branch on PLus, S=0	7				
		BMI	Branch on Minus, S=1	7				
		BZE, BEQ	Branch on ZEro or EQual	7				Z=1
		BNZE, BNEQ	Branch if Not ZEro or Not EQual	7				Z=0
		BLT	Branch if Less Than	7				S¥OV=1
		BGE	Branch if Greater than or Equal	7				S¥OV=0
		BLE	Branch if Less than or Equal	7				ZV(S¥OV)=1
		BGT	Branch if Greater Than	7				ZV(S¥OV)=0
		BUSC	Branch if Sign ≠ Carry	7				C¥S=1
		BESC	Branch if Sign = Carry	7				C¥S=0
		BEXT	Branch if External condition is True	7				4 LSB of Instruction are decoded to select 1 of 16 external conditions.

1 MICROCYCLE = 2 CLOCK CYCLES

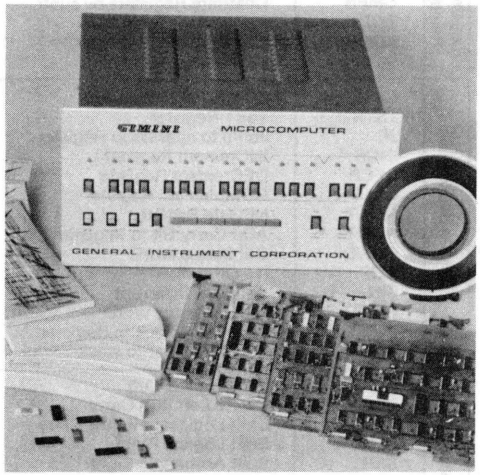
10

16-Bit Microcomputer System

FEATURES

- Built around the General Instrument's CP1600 MOS N-Channel Microprocessor.
- Complete microcomputer system to enable rapid program development.
- Separate Data, Address and Control Buses.
- Up to 65K memory space.
- Unlimited DMA channels.
- Nested interrupt system with full priority resolution.
- Includes— MC1600 Microcomputer Module
  RM1601 8K RAM Memory Module
  1/01600 TTY High Speed Reader Punch Interface Module
  CC1600 Control Console (Operator's Front Panel) and Control Console Module
  CF1600 Card File
  CA1600 TTY/EIA Cable Assembly
  CA1601 Reader/Punch Cable Assembly
  A full set of Software necessary to prepare and debug programs.

GIMINI MICROCOMPUTER



DESCRIPTION

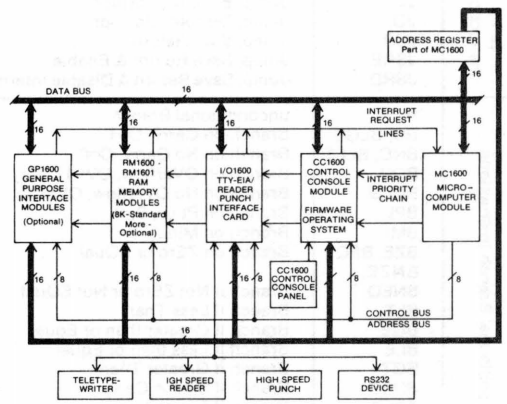
To simplify microprocessor hardware and software development, speed the product design cycle, and support product prototyping, a microcomputer development system and its associated components are a must. The Series 1600 family fills these requirements with the GIMINI Microcomputer—a versatile, general purpose, stand alone computer system built with the Series 1600 Semiconductor Components.

The GIMINI utilizes a totally modular design allowing the system designer maximum configurability. The system provides direct addressing to 65K words, unlimited DMA channels, and a multi-line/multi-level nested interrupt system with full priority resolution and self-identifying addresses. All control and timing signals as well as data and address buses are fully buffered and available for use in expanding memory or designing specialized I/O interfaces.

The basic hardware includes a card cage, front panel, and four printed circuit boards: the MC1600 Microcomputer Module, the RM1601 8Kx16 RAM Memory Module, the CC1600 Control Console and Control Console Module, and the 1/01600 TTY-EIA/High Speed Reader Punch Interface Module. Up to 9 additional cards of any type can be added as required. With the addition of a TTY and a high speed reader/punch, the GIMINI becomes a test bed for customer designed interfaces and related hardware as well as a full program preparation facility. Its resident On-Line Debug Program allows testing of hardware and software directly on the system in real time and also totally eliminates the annoying bootstrap procedure. The On-Line Software Package provides the necessary program preparation aids, such as the Assembler, Text Editor, the Relocating/Linking Loader and the Object Module Linker.

For the small volume user or those that want to avoid tooling and testing costs, all of the card level modules of the GIMINI are available on an OEM basis for further system integration.

BLOCK DIAGRAM



GIMINI Accessories

FEATURES

CF1600 CARD FILE
- 13-position
- P.C. backplane with wirewrap capability
- Rack-mountable
- Cards are keyed to connectors
- 10.5" high x 19.0" wide x 12.0" deep

EX1600 EXTENDER CARD
- For use with all GIMINI cards
- Two 70-pin connectors

WW1600 WIREWRAP CARD
- 126 16-pin positions
- Power and ground planes provided
- 10 Test points on edge of card

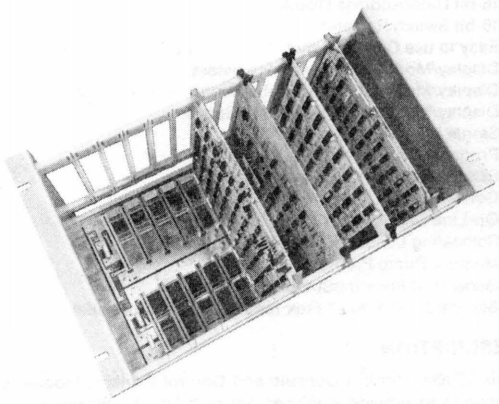
PS1600 POWER SUPPLY
- Provides all required voltages for the GIMINI Microcomputer System.
- +5V at 12A; +12V at 3A; -12V at 3A capability.
- 1% line and load regulation.
- Remote sensing capability.

CA1600 TTY/EIA CABLE ASSEMBLY
- 6-ft. cable for connecting I/01600 Interface Module to TTY or EIA compatible device.

CA1601 READER PUNCH CABLE ASSEMBLY
- 6-ft. Cable for connecting 1/01600 Interface Module with high speed reader-punch.

CA1602 GP1600 MODULE CABLE ASSEMBLY
- 6-ft. cable for connecting GP1600 Interface Module with external device.

CARD FILE



CF1600 CARD FILE

SLOT	CARD
1	MC1600 Microcomputer Module
2	CC1600 Control Console Module
3-12	Memory or I/O Cards
13	I/01600 TTY-EIA/Reader-Punch Interface Module

DESCRIPTION

The CF1600 Card File is designed to house up to 13 cards of the GIMINI family. The MC1600 Microcomputer Module, the CC1600 Control Console Module, and the I/O1600 TTY-EIA/Reader-Punch Interface Module each have one assigned position. The 10 remaining positions are available for memory modules, general purpose input-output cards, or special interface cards.

The printed circuit backplane parallels the power supply rails and the data, address and control buses for all 13 cards. There are separate voltage and voltage sense lines on the P.C. backplane for the +12V, -12V and +5V supplies. The bus system can be extended to another card file by wirewrapping or soldering a ribbon cable to one of the rear connectors.

The EX1600 Extender Card can be used with any other card of the GIC1600 family.

The WW1600 Wirewrap Card contains 126 16-pin sockets for prototyping special interface cards. Power and ground planes are provided.

The PS1600 Power Supply provides all the power necessary to run the GIMINI Microcomputer System. The user has 2A of +12V and 2A of -12V available to him for extra memories and interfaces. He also has 9A of +5V available to him if his system uses one RM1601 8K RAM Memory Module. Special power supply configurations are available upon request.

The CA1600 TTY/EIA Cable Assembly is a 6' cable that has a 10-pin 3M connector to interface with the I/O1600 TTY-EIA/Reader-Punch Interface Module on one end. The other end is split into two sections: one is left unterminated for connection to a TTY; the other is terminated in a 25-pin data connector for connection to an EIA device.

The CA1601 Reader/Punch Cable Assembly is a 6' cable that has a 34-pin 3M connector to interface with the I/O1600 TTY-EIA/Reader-Punch Interface Module on one end. The other end is split into two sections: both are terminated in 25-pin data connectors, one for connection to the reader and the other for connection to the punch.

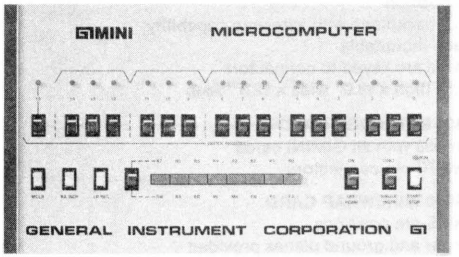
The CA1602 GP1600 Module Cable Assembly is a 6' cable that has a 34-pin 3M connector to interface with the GP1600 General Purpose Interface Module on one end. The other end is unterminated.

Control Console and Control Console Module

FEATURES

- 16-bit Data/Address Display
- 16-bit Switch Register
- Easy to use Control Panel:
  Display/Modify all 8 internal registers.
  Display/Modify the CPU Status Word.
  Display/Modify all 65K Memory Space.
  Single Instruction operation.
  Program Counter Inhibit capability
- ROM based Operating System:
  Conversational Monitor
  On-Line Debug Program/Software Breakpoints
  Relocating Loader (Eliminates Bootstrap)
  Memory Dump Program
  General Utilities/Input-Output Drivers
- Standard 19" × 10½" rack mountable Control Panel

CONTROL CONSOLE



DESCRIPTION

The CC1600 Control Console and Control Console Module is designed to provide a convenient method of controlling and monitoring the GIMINI System. The CC1600 consists of a front panel and a printed circuit module that are connected with two 34 pin flexible cables. The module contains the control logic to handle all front panel commands as well as the required interrupt logic to interface with the Microcomputer Module.

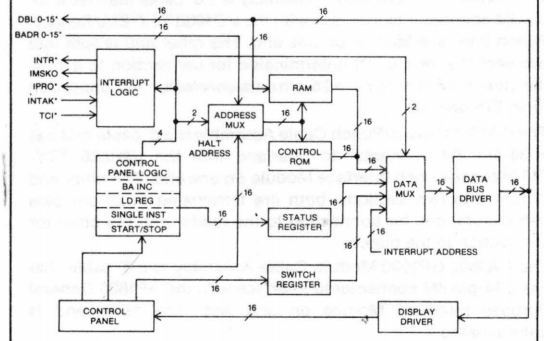
The Control Console Module consists of six control ROMs, scratch pad memory (256x16), a 16-bit Switch Register, a 16-bit Display Register, and the control logic to service any front panel request.

All functional operations for the Control Console are performed by the execution of program stored in the control ROMs. Pressing any action switch on the Control Console results in an interrupt request to the CP1600. After this interrupt is acknowledged, the CC1600 supplies the starting address of the Control Console service routine which performs the required function. In addition, the program automatically stores all CP1600 register in the scratch pad memory which is accessible via front panel selection. Consequently, whenever the CP1600 is in the HALT mode, the Control Console has direct access to all updated CP1600 information.

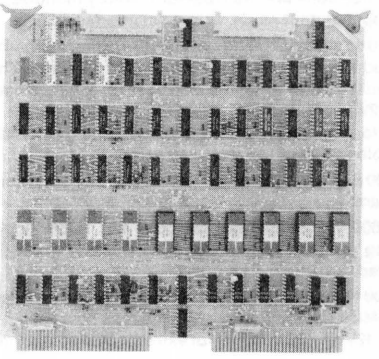
The control ROMs also contain all the firmware necessary for the development of micro-processor based systems. An On-Line Debug program is included so that software breakpoints and memory search routines may be executed. The system monitor allows the user to maintain conversational control via teletype interaction. The Relocating Loader can be used to input data from either a TTY or High Speed Reader, while the Memory Dump program allows any block of memory to be punched onto paper tape.

The Control Console Module is packaged on a 9.75" x 9.25" P.C. board, which mates with a dual 70-pin connector. It also interfaces with two 34-pin connectors for connection to the control console. Its operating temperature is 0° C to 55° C. It requires +5V ±5% at 1.0A.

BLOCK DIAGRAM



CONTROL CONSOLE MODULE



General Purpose Interface Module

FEATURES

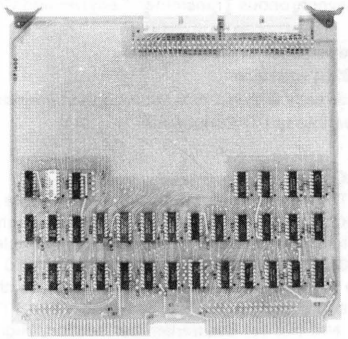
- 1 16-bit Addressable Input Port
- 1 16-bit Addressable Output Port
- 2 Addressable Status Registers
- Interfaces directly with MC1600 Module
- Space provided for sockets for I/O Control Logic
- Full Interrupt Capability.

DESCRIPTION

The GP1600 General Purpose Interface Module has two software addressable ports: one 16-bit input port and one 16-bit output port. Each port has an associated 4-bit status register that is addressable via program control. Provision is made so that the peripheral device can be operated on an interrupt or polling basis. Address decoding for the module is provided on the card although specific port assignments are determined by backplane selection. It is therefore possible to use up to eight GP1600 in a given system.

Connection to a given peripheral device is accomplished by a flat ribbon cable. Dual 34 pin connectors are mounted at the top end of the module. Space has been provided to accommodate wire wrap sockets so that specific interface circuitry may be incorporated on the module. Control and data signals have been brought out to wire wrap pins to facilitate prototype development.

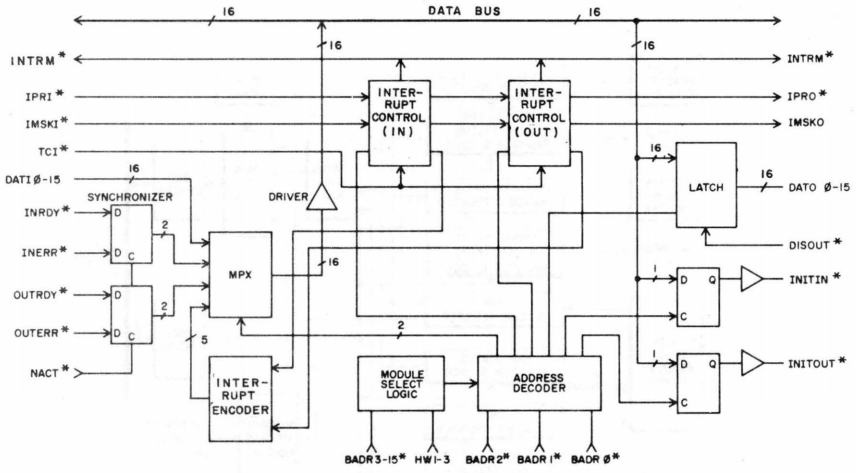
GENERAL PURPOSE INTERFACE MODULE



The module will accept dual-in-line package components mounted in standard wire wrap sockets. Locations for 14, 16, 22, 24 pin sockets are available.

The GP1600 General Purpose I/O Module is a 9.75" x 9.25" printed circuit card. Its operating temperature range is 0°C to 55°C.

BLOCK DIAGRAM



TTY-EIA/Reader-Punch Interface Module

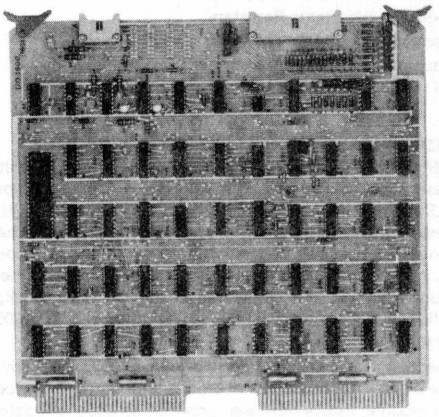
FEATURES

- Teletype Asynchronous Transmitter-Receiver and Control (UAR/T)
- High Speed Reader/Punch Controller
- EIA (RS-232C) Interface
- Interfaces directly with MC1600 Microcomputer Module
- TTL Compatible to I/O Peripherals

DESCRIPTION

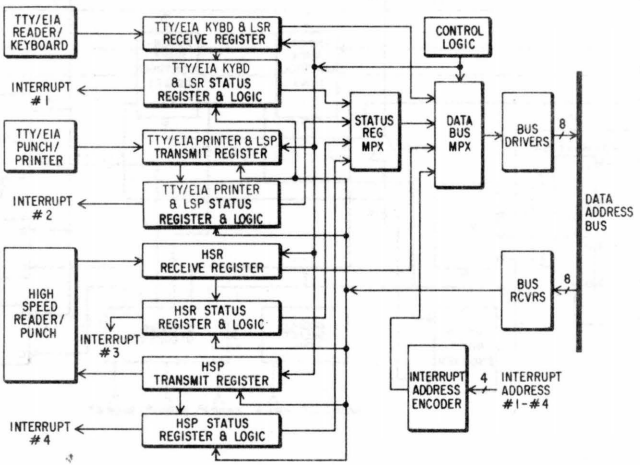
The I/O1600 TTY-EIA/Reader-Punch Interface Module handles full duplex communication between a Teletype, High Speed Reader/Punch combination or any RS-232C compatible device and the MC1600 Microcomputer Module. The I/O1600 Module has complete interrupt capability with four separate channels: two for the receiver section, High Speed Reader and TTY Reader/Keyboard; and two for the transmitter section, High Speed Punch and TTY Punch/Printer. These four interrupt channels operate independently with the receiver sections taking priority over the transmitter sections on simultaneous interrupts. The High Speed Reader/Punch has a higher priority than the TTY. Electrically, the I/O1600 Module has a 20 mA current loop for TTY operation and a TTY reader control line which allows the microprocessor to control the Teletype reader during on-line operation. The High Speed Reader/Punch interface controls a high speed Reader/Punch combination capable of reading paper tape at 300 characters per second and punching tape at 60 characters per second. The I/O1600 module also provides the additional capability of interfacing with any RS-232C compatible terminal.

TTY-EIA/READER-PUNCH INTERFACE MODULE



The I/O Module is a 9.75" × 9.25" P.C. board, which mates with a dual 70 pin connector. It also interfaces with a 10 pin connector for the TTY and a 34 pin connector for the high speed reader/punch. Its operating temperature is 0°C to 55°C. It requires +5V±5% at .5A, +12V±5% at .2A and −12V±5% at .2A.

BLOCK DIAGRAM



Microcomputer Module

FEATURES

- Complete microcomputer module with system clocks, memory interface, and fully buffered Address, Data, and Control Buses
- Built with General Instrument's CP1600 MOS N-Channel microprocessor
- Two Phase CPU Clock
- Direct and Register Addressing up to 65K memory space
- Memory stack pointer
- Two Programmable Interrupt Lines/Multi-Level and Self Identifying
- DMA Channel Capability
- 16 External Sense Conditions for Conditional Branching
- Generalized Initialization Logic
- Real Time Clock Interrupt
- Power Fail Interrupt

DESCRIPTION

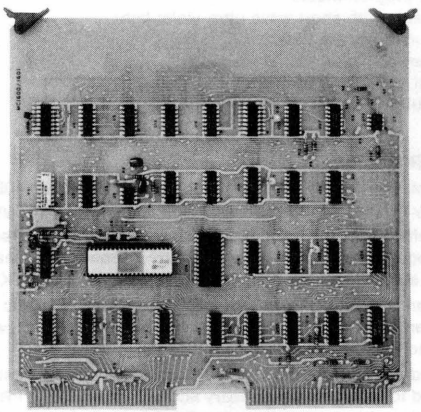
The MC1600 Microcomputer Module is a complete 16-bit parallel processing unit. It contains the hardware necessary to interface with memory and I/O. This is the main module in the GIMINI System.

The Microcomputer Module is designed around the CP1600, a 16-bit microprocessor on a chip. The MC1600 contains a 16-bit wide Bidirectional Bus Driver, Address Register and Driver, Bus Control Decoder-Driver, Crystal Oscillator, Clock Driver, an External Branch Multiplexer, A Real Time Clock Interrupt and a Power Fail Interrupt.

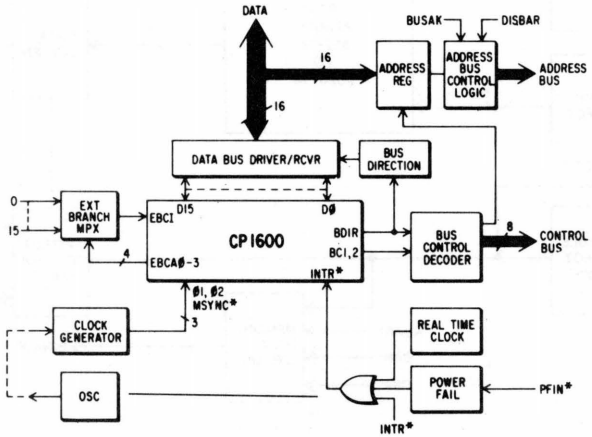
Two line, multi-level interrupt capability and Direct Memory Access are provided on this module. In response to an interrupt, the microcomputer automatically saves the current Program Counter on the Memory Stack, resolves interrupt priority and vectors to the device's interrupt service address. The direct memory access capability allows an alternate source to access memory or I/O while temporarily suspending processor operation. At the completion of a DMA operation, normal program execution continues in normal fashion.

The Microcomputer Module is a 9.75" × 9.25" P.C. board, which mates with a dual 70 pin connector. Its operating temperature range is 0°C to 55°C. It requires +5V±5% at .5A, +12V±5% at .1A and −12V±5% at 4 ma.

MICROCOMPUTER MODULE



BLOCK DIAGRAM:



10

PROM Memory Module

FEATURES

- Provides sockets for up to sixteen PROMs (4096×16)
- Static Memory - no clocks required
- Field programmable
- Erasable with short wave ultra-violet light
- 1 μs max. access time
- Buffered TTL inputs - 1 load
- Open collector TTL output - 30 loads
- Module decoding for 65K memory expansion

DESCRIPTION

The PM1600 PROM Memory Module is a standard 4096×16 memory module for use in the GIMINI Microcomputer System.

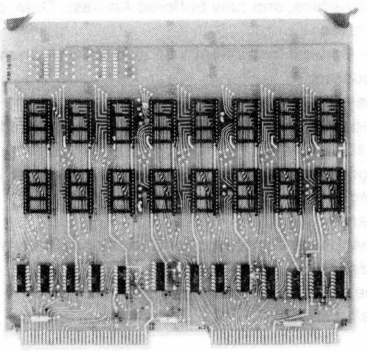
It is useful during the initial product design phase before freezing the program for a production quantity of lower cost masked ROMs, such as General Instrument's 16K RO-3-8316A(2K×8).

This memory module has sixteen sockets for 4096-bit static read-only memories. Each row of 8 rows will provide 512 16-bit words of memory. Each row contains 2 PROMs.

The Address bus inputs from the GIMINI to the memory card are buffered to provide the necessary address inputs to the PROMs. The sixteen data outputs from the PROMs are buffered onto the Data bus of the GIMINI System. For memories larger than 4K×16, decoding on the module allows addressing for a total of 65K memory.

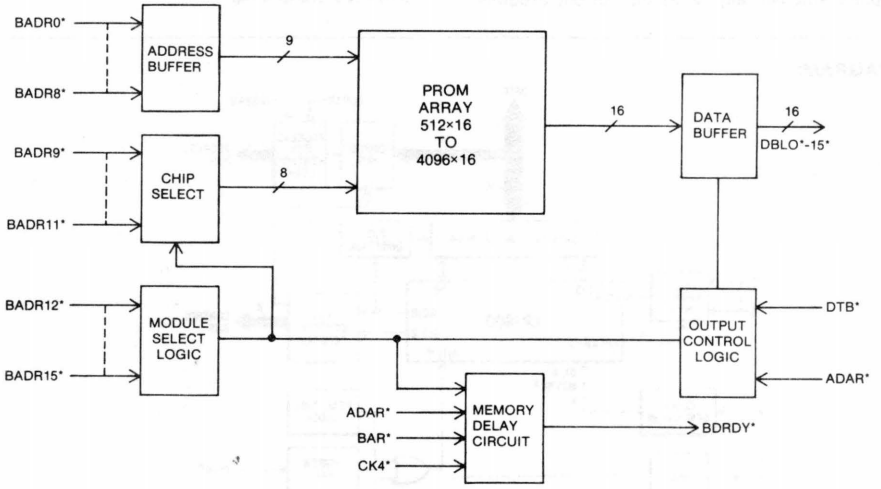
A special memory delay circuit is also provided on the board and is used to insure that the CP1600 microprocessor waits until stable data is available from the PROMs.

PROM MEMORY MODULE



The PM1600 PROM Memory Module is a 9.75"×9.25" P.C. board, which mates with a dual 70 pin connector. Its operating temperature range is 0° to 55°C. A board fully loaded with all 16 PROMs will require +5±5% at .5A and -12±5% at .5A.

BLOCK DIAGRAM



2Kx16 RAM Memory Module

FEATURES

- 2048—16-bit words per module
- Static memory, no clocks required
- Single +5 Volt Supply
- Byte or Word Capability
- Module decoding for 65K memory expansion
- 750 ns Read/Write Cycle Time
- Open Collector TTL Output—30 Loads
- Buffered TTL Inputs—1 Load

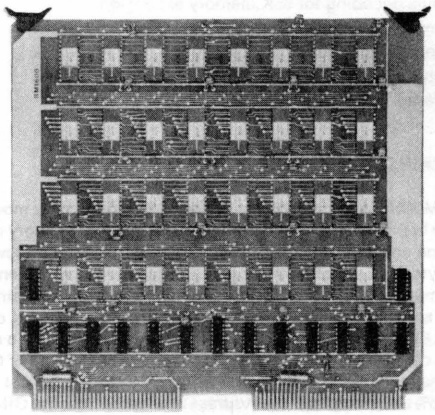
DESCRIPTION

The RM1600 Memory Card is a standard 2Kx16 memory module for use in the GIMINI Microcomputer System. This memory card contains address and data buffers, read/write circuits, low or high byte word selection logic, and is implemented with General Instrument's RA-3-4256B 1024 bit static Random Access Memory. There are thirty-two 22 pin 256x4 static RAM's packaged on a 9.75" x 9.25" x .062" printed circuit board, which mates with a dual 70 pin connector. Its operating temperature is 0° C to 55° C. It requires +5V ± 5% at 2.0A typical.

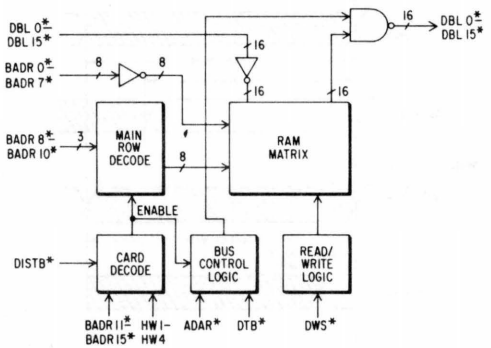
The Address bus inputs from the GIMINI to the memory card are buffered to provide the necessary address inputs to the RAM's. The sixteen data outputs from the RAM are buffered onto the Data bus of the GIMINI System.

If more than one 2K memory card is used in the GIMINI System, provisions are provided for proper selection of 2K increments, up to 65K (32 modules) memory space.

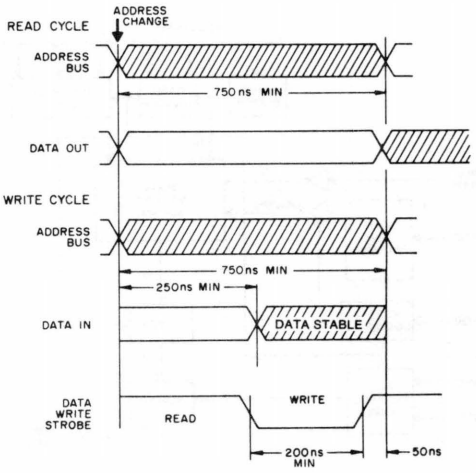
2KX16 RAM MEMORY MODULE



2Kx16 MEMORY CARD



TIMING DIAGRAMS



10

8Kx16 RAM Memory Module

FEATURES

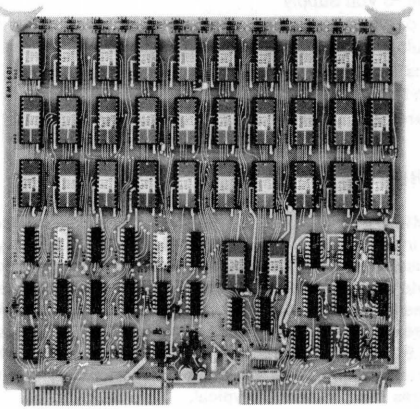
- 8192 — 16-bit words per module.
- Static memory, no clocks required.
- Byte or Word Capability.
- Module decoding for 65K memory expansion.
- 400 ns Read Time.
- 500 ns Cycle Time.
- Open Collector TTL Outputs—30 Loads
- Buffered TTL Inputs—1 Load

DESCRIPTION

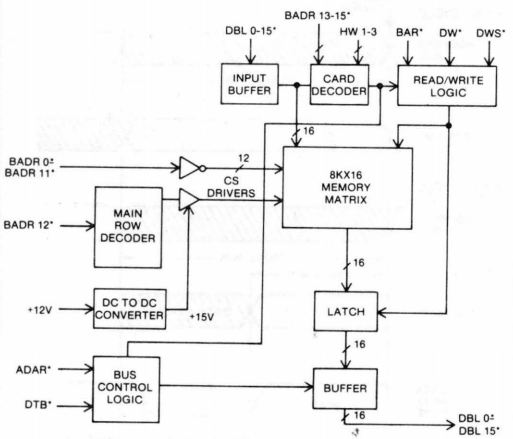
The RM1601 Memory Card is a standard 8Kx16 memory module for use in the GIMINI Microcomputer System. This memory card contains address and data buffers, read/write circuits, low or high byte word selection logic, and is implemented with General Instrument's RA-3-4402 4096 bit static Random Access Memory. There are thirty-two 22 pin 4Kx1 static RAM's packaged on a 9.75" x 9.25" x .062 printed circuit board, which mates with a dual 70 pin connector. Its operating temperature is 0° C to 55° C. It requires +5V ±5% at 0.5A typical, +12V ±5% at 0.5A typical and -12V ±5% at 0.1A typical. The Address bus inputs from the GIMINI to the memory card are buffered to provide the necessary address inputs to the RAM's. The sixteen data outputs from the RAM are buffered onto the Data bus of the GIMINI System.

If more than one 8K memory card is used in the GIMINI System, provisions are provided for proper selection of 8K increments, up to 65K (8 modules) memory space.

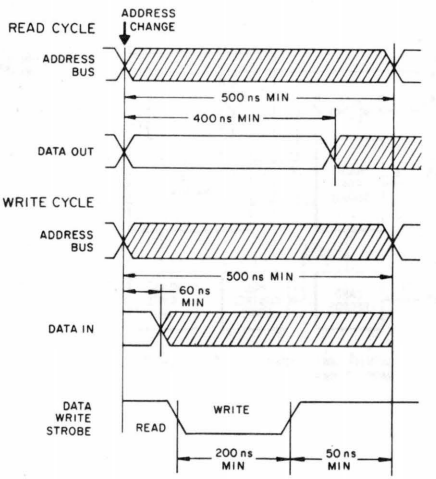
8KX16 RAM MEMORY MODULE



8K×16 MEMORY CARD



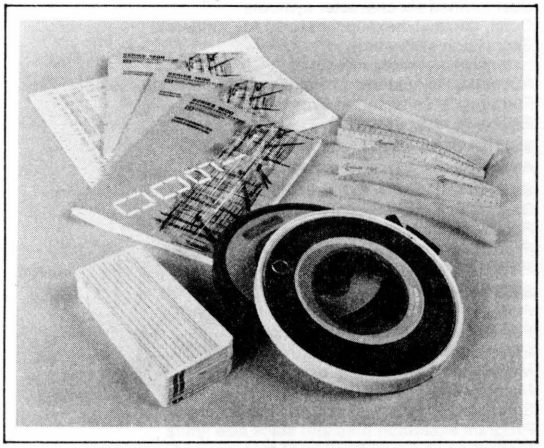
TIMING DIAGRAMS



Software

FEATURES

- Cross Software Package including Assembler/Simulator programs.
- On-Line Software Package for Program Preparation on Microcomputer.
- Resident Firmware in ROMS on Control Console Module in GIMINI Microcomputer allows conversational debugging of programs.
- Subroutine Library: Math packages, Code Conversion routines, String Operators, etc.



DESCRIPTION

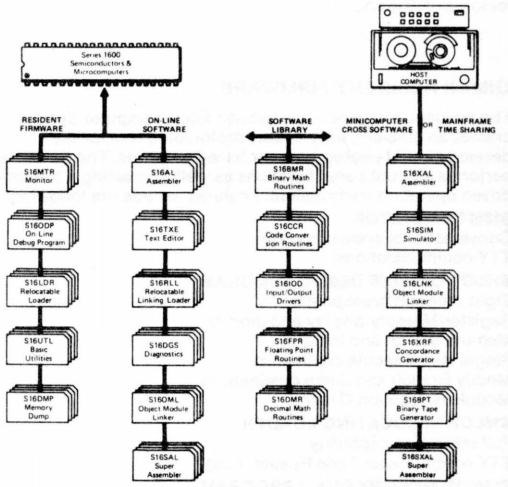
Software is fundamental to making every microprocessor come alive and the Series 1600 is no exception. The entire product family is supported by an extensive software system designed to make program development fast and efficient. Most important, the software structure is designed to grow with the hardware to insure a long term product continuity.

The Series 1600 Cross Software Package contains a versatile set of program preparation tools including compatible Assembler/Simulator programs operating at two different computer system levels—large machine or time share, or popular minicomputer systems. Each accepts Series 1600 assembly language statements as input and produce relocatable, linkable object code as output. In addition, the full microprocessor environment, including I/O operations, is simulated on the host machine so that complete program debugging and testing can be performed before committing to hardware. The combination of these features along with the ability to use a minicomputer as a host processor results in the lowest cost,easiest to use, Cross Software Package in the industry.

The GIMINI Microcomputer System also serves as a program preparation and hardware debug facility with the aid of its resident firmware and the On-Line Software Package. The resident firmware consists of a basic operating system containing a Monitor, the On-Line Debug Program, the Relocating Loader, the Memory Dump Program, and a number of other basic utility routines. The firmware also supports the system I/O with generalized routines for input/output from a TTY, high speed paper tape reader/punch, or any RS232 compatible device.

The On-Line Software Package includes the Symbolic Assembler, the Text Editor and the Relocating/Linking Loader, the Object Module Linker and the Super Assembler. The Object Module Linker provides the same features as S16LNK allowing generation of relocatable or absolute load modules on-line. The Super Assembler allows programs to be coded using high level procedure oriented statements while providing all the flexibility of basic assembly language.

SOFTWARE LINEUP



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S16XSFT CROSS SOFTWARE PACKAGE

The Series 1600 Cross Software Package is coded in low level Fortran IV and is specifically designed to operate in a 16-bit minicomputer environment. The Cross Software package has been installed on many popular minicomputer systems such as DGC NOVA and DEC PDP11. The Cross Software package has also been installed on many popular time-sharing computer systems.

S16XAL CROSS ASSEMBLER
Symbolic representation of all instructions
User defined six character symbols
Octal, decimal, hexadecimal and ASCII literals
Expression evaluation
Extensive assembly directives
Absolute, Relocatable or Relocatable/Linkable assembly
Full program and sorted symbol listing
Extensive error detection

S16XRF CONCORDANCE GENERATOR
Assembly symbol cross reference map

S16LNK OBJECT MODULE LINKER
Resolves global/external symbol linkages
Relocates and merges object modules
Produces relocatable/absolute load module
Produces load module map

S16SIM SIMULATOR
Full Series 1600 Instruction set simulation
Full 65K word memory simulation
I/O and interrupt simulation
Memory and/or Register breakpoints
Memory and/or Register traces
Simulated program execution time accumulation
Program execution time and stack size limits
Inspection and modification of memory and registers
Symbolic memory addressing

S16BPT BINARY PAPER TAPE GENERATOR

S16RTG ROM PATTERN TAPE GENERATOR

S16SXAL SUPER ASSEMBLER
High level procedure oriented instructions plus all features of S16XAL.

GIMINI RESIDENT FIRMWARE

The resident firmware in the GIMINI Microcomputer System creates an efficient, easy to use, prototyping tool for the development of microprocessor based products. The firmware performs all front panel functions as well as creating a terminal driven operating environment. Features include the following:

S16MTR MONITOR
Conversational system control
TTY communications

S160DP ON-LINE DEBUG PROGRAM
Eight program breakpoints
Register/Memory display and modify
Memory search and initialize
Single step/Execute commands
Modify Branch and Jump destinations
Module Relocation Origins

S16LDR RELOCATING LOADER
Full relocation capability
TTY or H.S. Paper Tape Reader input

S16MDP MEMORY DUMP PROGRAM
Punches in S16LDR format
TTY or H.S. Paper Tape Punch output
Generalized Code Conversions
TTY input/output driver
H.S. Paper Tape Reader/Punch driver

SERIES 1600 ON-LINE SOFTWARE PACKAGE

The Series 1600 On-Line Software Package is written in assembly language and runs on the GIMINI Microcomputer System. All programs are designed to be directly input/output compatible with the S16XSFT Cross Software Package so that either means of program preparation can be used interchangeably.

S16AL ASSEMBLER
Same features as S16XAL

S16TXE TEXT EDITOR
Multiple line buffering
Symbol search
Character, line, string editing

S16RLL RELOCATING/LINKING LOADER
Global and external symbol resolution
Full relocation capability
Loads and links multiple object modules
Memory map

S16DGS DIAGNOSTICS
Memory diagnostic
Instruction test
I/O Controller exerciser

S16OML OBJECT MODULE LINKER
Same features as S16LNK

S16SAL SUPER ASSEMBLER
High level procedure oriented instructions plus all features of S16AL.

SERIES 1600 SUBROUTINE LIBRARY

The Series 1600 Microprocessor System is supported by an extensive and growing library of useful subroutines designed to relieve the user of many time consuming software chores. All of Subroutine Library programs are written in Series 1600 Assembly Language making them both fast and effficient. They are compatible with both the Series 1600 Symbolic Cross Assembler (S16XAL) and the Series 1600 On-Line Assembler (S16AL). In addition, all library programs are designed to be directly compatible with hardware extensions to the Series 1600 product family so that increased performance can be achieved without software complications.

S16BMR BINARY MATH ROUTINES
Signed Multiply/Divide
Square Root
Double Precision Multiply/Divide
Double Precision Square Root

S16CCR CODE CONVERSION ROUTINES
Binary to BCD—BCD to Binary
Binary to ASCII—ASCII to Binary
Binary to HEX—HEX to Binary
Binary to OCTAL—OCTAL to Binary
Fixed to Floating—Floating to Fixed

S16IOD INPUT/OUTPUT DRIVERS
TTY Input/Output
H.S. Paper Tape Reader/Punch Input/Output
Byte Table Pack—Byte Table Unpack

S16FPR FLOATING POINT ROUTINES
Floating Add/Subtract
Floating Multiply/Divide
I/O Conversion

S16DMR DECIMAL MATH ROUTINES
Decimal Add/Subtract
Decimal Multiply/Divide
Decimal Square Root
Decimal Compare

Super Assembly Language

FEATURES

- High level operations: LET, GOTO, GO@, CALL, IF, IF-THEN, IF-THEN-ELSE, DO, DO-FOR, DO-WHILE.
- Array subscripting
- Literal representation in Binary, Octal, Decimal, Hexadecimal and character notation.
- Symbolic representation of all CP1600 instructions.
- Directives for:
  - Controlling register utilization of high level operations
  - Controlling storage allocation
  - Initializing storage
  - Specifying character strings
  - Declaring a program entry point
  - Declaring global and external symbols
  - Declaring a program entry point
  - Specifying assembly output form
  - Controlling conditional assemblies
- Absolute and Relocatable load module output
- Absolute and Relocatable linkable object module output
- Program listing
- Extensive error diagnostics

DESCRIPTION

The General Instrument Super Assembly Language enables the CP1600 user to implement programs at a procedural level using FORTRAN-like statements rather than at the machine level of conventional assembly languages. Super Assembly Language includes LET, IF, CALL, DO, GOTO, and GO@ high level operations as well as all the instruction mnemonics and assembly directives of basic CP1600 assembly language. Super Assembly Language provides both the novice and the experienced programmer with the convenience and efficiency of procedural level programming while retaining the flexibility and economy of basic assembly language. Many applications can be completely coded using the high level operations, but when required, basic assembly statements can be intermixed freely with high level statements. The CP1600 Super Assembly Language is based on the popular high level programming languages, FORTRAN and BAIC.

The Super Assembler Program converts source programs written in CP1600 Super Assembly Language into binary machine code. This conversion process is accomplished by making two passes through a source program. The Super Assembler Program also produces a listing of the assembled program; the full instruction expansion into machine assembly language for each high level statement may be printed on the listing, if the expanded listing option is selected by the user.

HIGH LEVEL STATEMENTS

GOTO

The GOTO statement is used to transfer program control unconditionally to a specified destination.

Ex.: GOTO SCAN

GO@

The GO@ statement is used to transfer program control unconditionally indirectly through a specified storage designator to a destination. The destination is defined by the current contents of the storage designator.

Ex.: GO@ TABLE (I)

CALL

The CALL statement is used to transfer program control to a subroutine. Arguments, i.e., parameters to be passed to the subroutine, follow the subroutine name enclosed in parenthesis and separated by commas.

EX.: CALL SQRT(I,J)

LET

The LET statement is used to perform data transfers, arithmetic computations and logical operations involving constants, variables and subscripted variables. Addition, subtraction, multiplication, division, negation and logical NOT, AND, exclusive OR and inclusive OR operations may be performed using the LET statements.

EX.: LET X = .NOT. Y .AND. Z * 5

IF

The IF statement is used to perform tests on single quantities and make comparisons between two quantities. The quantities may be constants, variables, assembly expressions and subscripted variables. An IF statement may be of three types: arithmetic, conditional or relational. The arithmetic IF is used to test a quantity for negative, zero and positive and directly transfer to a corresponding destination. The conditional IF is used to test a quantity for positive, negative, zero and non-zero and the relational IF is used to compare two quantities. The conditional and relational IF statements may execute a GOTO statement if true. They may also cause a THEN-ELSE (THEN, if true and ELSE, if false) sequence of instructions to be executed. The THEN-ELSE capability is a feature not found in FORTRAN or BASIC and is similar to the IF-THEN-ELSE facilities in more powerful languages such as ALGOL, COBOL and PL/I.

```
EX.: IF ANSWR .ZERO. GO TO NEXT
     IF QUANT .EQ. LIMIT THEN
     CALL SQRT(A)
     END

EX.: IF A .EQ. 2 THEN
     LET B=5
     ELSE
     LET B=6
     END
```

DO

The DO statement is used to perform looping and iterative operations by causing a sequence of statements between the DO statement and a corresponding CONT (CONTinue) statement to be executed repeatedly. Such a statement sequence is known as a DO loop. DO loops may be nested i.e., contain other DO loops up to a depth of four levels. When DO loops are nested, inner loops terminate before outer loops. DO loops may be controlled by FOR or WHILE conditions.

```
EX.:  ABC   DO ABC FOR I = INIT, MAX, INCR
            IF (TBL (I) .EQ. QTY) GO TO GETOUT
            CONT

EX.:  XYZ   DO XYZ WHILE QTY .GT. LIM
            LET K = K .AND. MASK
            LET QTY = K + INCR
            CONT
```

10

Programmable Interface Controller

FEATURES

- User Microprogrammable
- Intelligent Controller for Peripheral Interfacing
- 32 8-Bit Registers
- 256×12-Bit ROM for Microprogram
- Arithmetic Logic Unit
- 2 Sets of 8 User Defined Peripheral Input/Output Lines
- Real Time Clock Counter
- Self contained Oscillator
- Simple Interfacing to Microprocessor

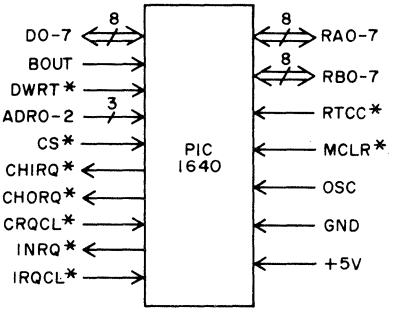
DESCRIPTION

The PIC1640 MOS/LSI circuit array is a byte oriented microprogrammable interface controller designed to satisfy the requirements for low cost peripheral device interfacing. The array is part of the Series 1600 Microprocessor System and also has applicability as an I/O controller in many other computer product families. The array is a complete single chip controller with internal ROM microprogram defining the overall functional characteristics and operational waveforms on each of the general purpose input/output lines. The array can be programmed to scan keyboards, drive multiplexed displays, interface magnetic tape cassettes, control printers, implement communication line disciplines, and interface a host of other low to medium speed peripheral devices. Because of its microprogrammable architecture, the PIC1640 is a truly intelligent controller as opposed to a simple interface adapter.

The PIC1640 is fabricated with N-Channel Ion Implant technology resulting in a high performance product with proven reliability and production history. Only a single 5 volt power supply is required for operation, and an on-chip oscillator provides the operating clock with only an external R/C network to establish the frequency. Inputs and outputs are TTL compatible. The PIC1640 is supplied in a 40 pin dual-in-line package.

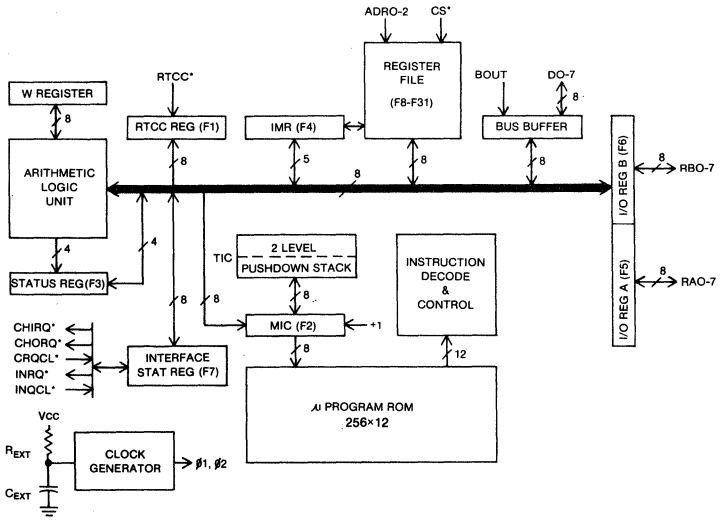
PIN CONFIGURATION

40 LEAD DUAL IN LINE



The Programmable Interface Controller family (PIC1640/1650 and all extensions) is supported by an extensive software and hardware package. The software package includes Cross Assembler/Simulator programs designed to run at both the large machine on time share and minicomputer system levels. The hardware package includes a TTL prototype emulator board with which the user can verify, in his actual system, the microprogram in PROM before committing it to mask tooling. For added flexibility, the board can also fit into the GIMINI developmental system such that the PIC microprogram can be stored in RAM and accessed as memory as part of the CP1600 microprocessor address space. Thus, on-line changes in code can be implemented without the inconvenience of reburning PROMs.

BLOCK DIAGRAM



PIN FUNCTIONS

Signal/Function

D0-7 (Input/output/high impedance
Bidirectional Data Bus lines 0 to 7. Used by the PIC1640 to send and receive data and control information to the Series 1600 microprocessor.

BOUT (Input)
Data Bus direction control. Driven directly by the Series 1600 microprocessor to control the direction and state of the tri-state buffers on D0-7.

DWRT* (Input)
Data Write pulse. Read/write control to the internal registers of the PIC 1640.

ADRO-2 (Input)
Address Bus lines 0 to 2. Used to select one out of 8 internal 8-bit registers for reading or writing data or control information.

CS* (Input)
Chip Select. Used to select one PIC 1640 out of a number of others connected to a common bus. Also used to provide synchronization to bus operations.

CHIRQ* (output)
Channel Output Request. Used to request data channel input mode service from the Series 1600 microprocessor.

CRQCL* (Input)
Channel Request Clear. Input to the PIC 1640 to clear channel service.

INRQ* (output)
Interrupt Request. Used by the PIC 1640 to request an interrupt from the Series 1600 microprocessor.

IRQCL* (Input)
Interrupt Request Clear. Input to the PIC 1640 to clear the request for interrupt service.

OSC (Input)
Oscillator. This input can be driven by an external oscillator if a precise frequency of operation is required or an external R/C network can be used to set the frequency of operation of the internal clock generator. The maximum OSC frequency is 4MHz.

MCLR* (Input)
Master Clear. Used to initialize the internal ROM microprogram to address 377_8.

RTCC* (Input)
Real Time Clock Counter. Used by the microprogram to keep track of elapsed time between events. The maximum RTCC* frequency is 1MHz.

RA0-7, RB0-7 (Input/output)
User programmable I/O. These lines can be inputs and/or outputs and are under direct control of the microprogram for use as control signals to the peripheral devices.

ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC1640 controller is based on a register file concept with very simple, low level, microcommands designed to emphasize bit, byte, and register transfer operations. The primary purpose of the PIC is to perform logical processing, basic code conversions, formatting, and to generate fundamental timing and control signals for I/O devices. The emphasis is on control and interface functions as opposed to computing functions.

Internally, the PIC1640 is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a Control ROM composed of 256 microcontrol words each 12 bits in width.

The Register File is divided into two functional groups: operational registers and general registers. The operational registers are addressed as F0 to F7 (the first 8 of the total of 32 file registers) and include among others the Real Time Clock Counter Register, the Status Register, the Micro Instruction Counter (MIC), and I/O Registers A and B (RA and RB). The general registers are addressed as F8 to F31 and are used for data and control information under command of the microinstructions. The last 8 of the general registers (F24 to F31) are also addressable via the interface port to the Series 1600 bus structure providing a direct communications path between the controller and the host Series 1600 microprocessor. These 8 registers effectively form a set of "mailbox" slots that are addressable as locations within the address space of the host microprocessor as well as by the controller microprogram. The allocation of these shared memory locations to specific functions is done completely by program convention. Typical examples might be as buffers for multi-byte data strings, check sum characters, special error code patterns, sync or control characters, and general bit flags for control purposes.

The Logic Unit contains one temporary working register and gating to perform Boolean functions between data held in the working register and any file register. Emphasis is placed on logical operations and bit manipulations as opposed to arithmetic functions.

The Control ROM contains the operational program for the rest of the logic within the controller. Sequencing of microinstructions is controlled via the Instruction Counter (MIC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, or loading computed addresses into the MIC accessed as one of the file registers. In addition, an on-chip pushdown stack is employed with the return address register (TIC) serving as the top element of the stack. This permits easy to use subroutine nesting.

REGISTER FILE ARRANGEMENT

File	Function
F0	Not a physically implemented register. F0 calls for the contents of the Instruction Modification Register (low order 5 bits) to be used to select a file register.
F1	Real Time Clock Counter Register. This register can be loaded by the microprogram but will always read as 377_8.
F2	Micro Instruction Counter (MIC).
F3	Status Word Register **1 | 1 | 1 | 1 | RTCB | Z | DC | C** RTCB: Cleared when Real Time Clock is loaded; set when Clock count reaches zero. C: Stores the carry out on arithmetic operations, and acts as a bit link on rotate operations. DC: Stores the carry out of low order digit on arithmetic operations. Z: Set if the result of the arithmetic operations is zero.
F4	Instruction Modification Register (IMR). Low order 5 bits only are used. The IMR is useful in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits read as a logic "1".
F5	I/O Register A (RA)
F6	I/O Register B (RB)
F7	Interface Status Register (ISR). Bits in this file can request interrupt and channel service from the host microprocessor when appropriate. **0 | 0 | 0 | 0 | 0 | CI | CO | I** I: Set under microcode control to request interrupt service (INRQ*) from the host microprocessor. Cleared by MCLR* and IRQCL*. CO: Set under microcode control to request channel output mode service (CHORQ*) from the host microprocessor. Cleared by MCLR* and CRQCL*. CI: Set under microcode control to request channel input mode service (CHIRQ*) from the host microprocessor. Cleared by MCLR* and CRQCL*.
F8-F23	General Registers for use by microprogram.
F24-F31	General Registers and "mailbox locations" for external communications with the host CPU.These are selected by ADR0-2.

INSTRUCTION SET SUMMARY

(The instruction execution time is 1 μsec, except if a conditional test is true or if the MIC register is changed as a result of an instruction. In these two cases, the instruction execution time is 2 μsec.)

LITERAL and CONTROL

(4) (8)

OP CODE	8-BIT LITERAL

W Specifies working register

		STATUS
Load W	Literal→W	—
And W	Literal "AND" W→W	Z
Or W	Literal "OR" W→W	Z
Xor W	Literal "EX OR" W→W	Z
Return & Load W	Literal→W & TIC↑→MIC	—
Jump & Store	MIC→TIC↓& Literal→MIC	—
Jump	Literal→MIC	—

NOTE: ↓ and ↑ mean push and pop the TIC stack, respectively.

BIT OPERATIONS

(4) (3) (5)

OP CODE	BIT #	FILE #

Bit No. field specifies 1 of 8 bit positions.
Bit No. field specifies 1 of 32 file registers.

		STATUS
Bit Set	1→Bit No., File No.	—
Bit Clear	0→Bit No., File No.	—
Bit Test Skip Set	If Bit No., File No. test is true,	—
Bit Test Skip Clear	then MIC + 2→MIC, else MIC + 1→MIC	—

FILE OPERATIONS

(6) (1) (5)

OP CODE	R	FILE #

R field specifies result to be replaced in W or File No. File No. field specifies 1 of 32 file registers.

And	W "AND" File→R	Z
OR	W "OR" File→R	Z
XOR	W "OR" File→R	Z
Add	W + File→R	C,DC,Z
Move W	W→R	—
Increment F	F + 1→R	Z
Complement F	F—→R	Z
Move File	F→R	Z
Subtract File	F + W + 1→R	C,DC,Z
Decrement File Skip Zero	F-1→R; Skip if zero result	—
Rotate Right File	$F_n \rightarrow R_n$ - 1; $F_0 \rightarrow C$; $C \rightarrow R_7$	C
Rotate Left File	$F_n \rightarrow R_n$ + 1; $F_7 \rightarrow C$; $C \rightarrow R_0$	C
Swap Halves File	$F_{0-3} \leftrightarrow F_{4-7} \rightarrow R$	—
Increment File Skip Zero	F + 1→R; Skip if zero result	—
Clear File	0→R	Z
Decrement File	F - 1→R	Z

Programmable Interface Controller

FEATURES

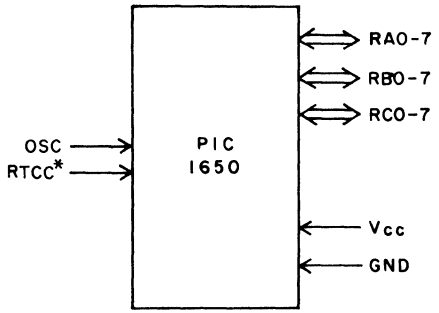
- User Microprogrammable
- Intelligent Controller for Stand-Alone Applications
- 32 8-Bit Registers
- 512×12-Bit ROM for Microprogram
- Arithmetic Logic Unit
- 2 Sets of 8 User Defined Peripheral Input/Output Lines
- Real Time Clock Counter
- Self contained Oscillator
- Simple Interfacing to Microprocessor

DESCRIPTION

The PIC1650 MOS/LSI circuit array is a byte oriented microprogrammable controller designed to satisfy the requirements for a low-cost, stand-alone 8-bit micro-computer. The array is a complete chip controller with an internal customer-defined ROM microprogram specifying the overall functional characteristics and operational waveforms on each of the general purpose input/output lines. The array can be programmed to scan keyboards, drive multiplexed displays, control vending machines, control traffic lights, control printers and to control automatic gasoline pumps. Since it contains ROM, RAM, I/O as well as the central processing unit on one device, the PIC1650 is truly a complete 8-bit micro-computer on one chip.

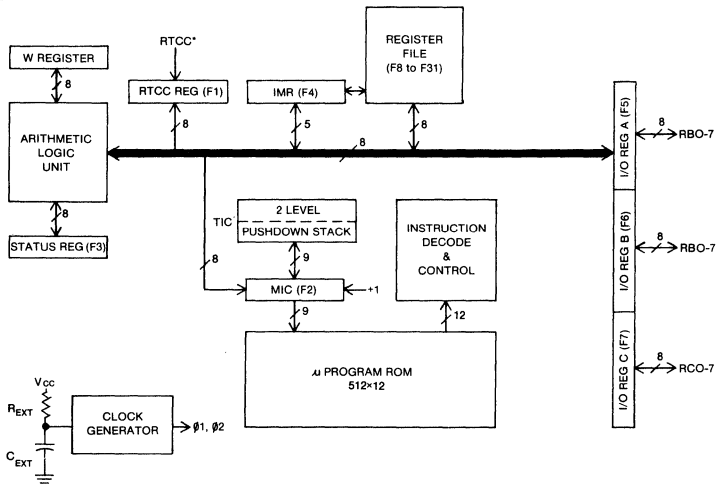
The PIC1650 is fabricated with N-Channel Ion Implant technology resulting in a high performance product with proven reliability and Production history. Only a single +5 volt power supply is required for operation, and an on-chip oscillator provides the operating clock with only an external R/C network to establish the frequency. Inputs and outputs are TTL compatible. The PIC1650 is supplied in a 28 dual-in-line package.

PIN CONFIGURATION



The Programmable Interface Controller family (PIC1640/1650 and all extensions) is supported by an extensive software and hardware package. The software package includes Cross Assembler/Simulator programs designed to run at both the large machine on time share and minicomputer system levels. The hardware package includes a TTL prototype emulator board with which the user can verify, in his actual system, the microprogram in PROM before committing it to mask tooling. For added flexibility, the board can also fit into the GIMINI developmental system such that the PIC microprogram can be stored in RAM and accessed as memory as part of the CP1600 microprocessor address space. Thus, on-line changes in code can be implemented without the inconvenience of reburning PROMs.

BLOCK DIAGRAM



PIN FUNCTIONS

Signal	Function
OSC (input)	Oscillator input. This signal can be driven by an external oscillator if a precise frequency of operation is required or an external R/C network can be used to set the frequency of operation of the internal clock generator. The maximum OSC frequency is 4 MHz.
RTCC* (input)	Real Time Clock Counter. Used by the microprogram to keep track of elapsed time between events. The maximum RTCC* frequency is 1 MHz.
RA0-7, RB0-7, RC0-7 (input/output)	User programmable input/output lines. These lines can be inputs and/or outputs and are under direct control of the microprogram.

ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC 1650 controller is based on a register file concept with very simple, low level, microcommands designed to emphasize bit, byte, and register transfer operations. The primary purpose of the PIC is to perform logical processing, basic code conversions, formatting, and to generate fundamental timing and control signals for I/O devices. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC1650 is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a Control ROM composed of 512 microcontrol words each 12 bits in width.

The Register File is divided into two functional groups: operational registers and general registers. The operational registers are addressed as F0 to F7 (the first 8 of the total of 32 file registers) and include among others the Real Time Clock Counter Register, the Status Register, the Micro Instruction Counter (MIC), and I/O Registers A, B and C (RA, RB and RC). The general registers are addressed as F8 to F31 and are used for data and control information under command of the microinstructions.

The Logic Unit contains one temporary working register (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

The Control ROM contains the operational program for the rest of the logic within the controller. Sequencing of a microinstructions is controlled via the Micro Instruction Counter (MIC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, or loading computed addresses into the MIC. In addition, an on-chip pushdown stack is employed with the return address register (TIC) serving as the top element of the stack. This permits easy to use subroutine nesting. Application of the +5V power supply initializes the ROM microprogram to address 777_8.

REGISTER FILE ARRANGEMENT

FILE	FUNCTION
F0	Not a physically implemented register. F0 calls for the contents of the Instruction Modification Register (low order 5 bits) to be used to select a file register.
F1	Real Time Clock Counter Register. This register can be loaded by the microprogram but will always read as 377_8.
F2	Micro Instruction Counter (MIC).
F3	Status Word Register.

1	1	1	1	RTCB	Z	DC	C

RTCB: Cleared when Real Time Clock is loaded; set when clock count reaches zero.

C: Stores the carry out on arithmetic operations, and acts as a bit link on rotate operations.

DC: Stores the carry out of low order digit on arithmetic operation.

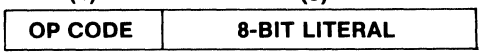
Z: Set if the result of the arithmetic operations is zero.

F4	Instruction Modification Register (IMR). Low order 5 bits only are used. The IMR is useful in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits read as a logic "1".
F5	I/O Register A (RA)
F6	I/O Register B (RB)
F7	I/O Register C (RC)

INSTRUCTION SET SUMMARY

(The instruction execution time is 1 μsec, except if a conditional test is true or if the MIC register is changed as a result of an instruction. In the two cases, the instruction execution time is 2 μsec.)

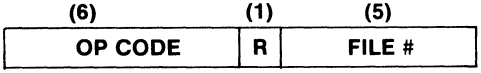
LITERAL and CONTROL



W Specifies working register		STATUS
Load W	Literal→W	—
And W	Literal "AND" W→W	Z
Or W	Literal "OR" W→W	Z
Xor W	Literal "EX OR" W→W	Z
Return & Load W	Literal→W & TIC↑→MIC	—
Jump & Store	MIC→TIC↓& Literal→MIC	—
Jump	Literal→MIC	—

Note: ↓ and ↑ mean push and pop the TIC stack, respectively.

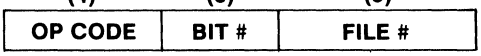
FILE OPERATIONS



R field specifies result to be replaced in W or File No. File No. field specifies 1 of 32 file registers.

And	W "AND" File →R	Z
OR	W "OR" File →R	Z
XOR	W "OR" File →R	Z
Add	W + File →R	C,DC,Z
Move W	W →R	—
Increment F	F + 1 →R	Z
Complement F	F —→R	Z
Move File	F →R	Z
Subtract File	F + W + 1→R	C,DC,Z
Decrement File Skip Zero	F-1→R; Skip if zero result	—
Rotate Right File	$F_n \rightarrow R_n$ - 1; $F_0 \rightarrow C$; $C \rightarrow R_7$	C
Rotate Left File	$F_n \rightarrow R_n$ + 1; $F_7 \rightarrow C$; $C \rightarrow R_0$	C
Swap Halves File	$F_{0-3} \leftrightarrow F_{4-7} \rightarrow R$	—
Increment File Skip Zero	F + 1→R; Skip if zero result	—
Clear File	0 →R	Z
Decrement File	F - 1→R	Z

BIT OPERATIONS



Bit No. field specifies 1 of 8 bit positions.
Bit No. field specifies 1 of 32 file registers.

		STATUS
Bit Set	1→Bit No., File No.	—
Bit Clear	0→Bit No., File No.	—
Bit Test Skip Set	If Bit No., File No. test is true,	—
Bit Test Skip Clear	then MIC + 2→MIC, else MIC + 1→MIC	—

10

8-Bit Microprocessor System

FEATURES

- 2 Chip Minimum System (plus clock)
- 48 Accessible 8 Bit Internal Registers
- 48 Basic Instructions
- Binary and Decimal Arithmetic Capability
- Direct and Indirect Input Output Capability
- Automatic subroutine nesting on memory devices
- Family of development devices

DESCRIPTION

The Series 8000 Logic Processor System is designed to perform any digital function using far fewer packages than a TTL or CMOS implementation. Typically a 100 package system can be reduced to a three chip solution of LP8000 Processor, LP6000 Program Memory and LP1030 Clock Generator (two 40 lead DIP plus one 8 lead DIP). The consequent savings in development and production costs and increased reliability give the user many of the advantages of a customized LSI solution but without the restriction that it must be a high volume product.

The System is fabricated with General Instrument's P-channel Nitride Process which has a proven reliability and production history. All members of the Series 8000 family including Read Only Memories, General Purpose Input Output and Memory interace parts are fully compatible with each other.

The LP8000 Logic Processor Unit itself is a complete 8-bit single chip MOS-LSI Microprocessor. It has a modern computer architecture with forty eight general purpose internal registers. This, coupled with a binary and decimal capability arithmetic unit, allows a versatile and sophisticated implementation of a microcomputer system. The 8-bit Data highway is supplemented by a 6-bit Address bus to give a 14-bit address capability which permits access to 16,384 words in combination of program memory, data memory or peripheral devices. The address space consists of 64 "modules" which can be either 256 words of memory or one 8-bit bidirectional I/O port.

LOGIC PROCESSOR - LP (Part number LP8000)

The logic processor (LP) is the heart of the Series 8000 system. It performs all of the arithmetic and logical functions required and also controls all activities occurring in the Series 8000 system. It has 48×8 bit working registers and an 8 bit input/output interface to which external peripherals may be attached directly.

PROGRAM MEMORY - PM (Part number LP 6000)

The program memory PM contains a 1K x 8 bit memory which stores the user's program. This chip also includes the program counter which points to the current address. It is arranged at the top of a four word hardware stack which is controlled by the LP for subroutine nesting. Two directly addressable 8 bit I/O interfaces are included, so that a minimum system consisting of one LP and one PM has 24 I/O leads. Extra PMs can be connected to the main system bus, up to a maximum of 16K words. Each PM and I/O interface can be addressed by the LP, the module addresses being programmed at the same time as the customer's program.

MEMORY INTERFACE CHIP - MIC (Part number LP 1000)

The memory interface chip consists of an 11 bit program counter at the top of four word hardware stack. The address output are TTL compatible and enable any external 2K×8 bit memory to be addressed. Other circuits allow the MIC to interface directly to the Series 8000 system without any external components. It is intended for use when breadboarding systems or when using non-standard memory, e.g. diode matrix, core, etc.

The memory area can be extended by using several MIC/external memory combinations. The addresses are selected by hardwiring pins to V_{GG} or V_{CC}.

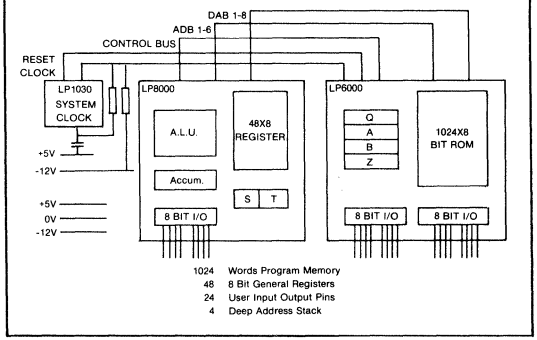
INPUT/OUTPUT BUFFER - IOB (Part number LP 1010)

The input/output buffer consists of two addressable 8 bit I/O interfaces. The addresses are selected by hardwiring pins to Vgg or V_{CC}.

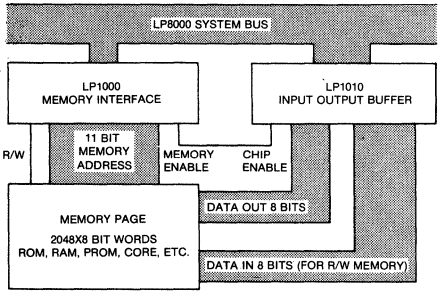
CLOCK GENERATOR - CG (Part Number LP1030)

The Series 8000 needs only an 800KHz clock, a power-on-reset signal to clear and synchronize the system and two power supplies. Virtually all external components may be eliminated by using the clock generator (CG). The frequency of the built in oscillator is determined by an external resistor or can be optionally over-ridden by an input from an external oscillator. A data synchronizing signal ϕ_{3N} is provided to act as an oscilloscope trigger and as a Data Valid signal for exteral hardware.

COMPLETE MINIMUM SYSTEM



MEMORY IMPLEMENTATION FOR DEVELOPMENT SYSTEMS



PIN FUNCTIONS

Processor Signals

DAB 1-8
Bidirectional 8-lead precharged data bus, used in conjunction with address bus to implement 14-bit address word.
ADB 1-6
Push pull 6-lead address bus. This 6-bit word specifies the memory 'module' address and the 8-bit data bus specifies the 1 of 256 'intra module address'.

Processor Control Signals

CIO
Indicates direction of data flow on data bus.
CDA
Indicates if data bus is carrying data or address information.
CQZ
Used to select the Q counter or Z register for memory addressing.
CRA
Used to control the internal address stack.

Peripheral Signals

PEB 1-8
This is a bidirectional 8-bit latched input/output port with an open drain output configuration. In the case of the LP8000 chip the 8-bit port is organised such that only bits 5-8 are bidirectional, bits 1-4 are only available as inputs. For all other chips in the family the peripheral interfaces are 8-bit all bidirectional.

Drive Requirements

CLOCK
A single phase high level clock is required by the system and this would normally be provided by the LP1030 Clock Generator. The clock frequency used can be selected between 500 and 800KHz. With an 800KHz clock the machine provides a 5μSec machine cycle time.
RESET
This is a clock synchronized high level signal, normally provided by the LP1030 Clock Generator.
POWER
V_{CC} +5 Volt supply
V_{GI} 0 Volt (GND) supply
V_{GG} −12 Volt supply

PIN CONFIGURATIONS

40 LEAD DUAL IN LINE
LP8000 LOGIC PROCESSOR

Top View

V_{CC}	1	40	V_{GI}
Power on Reset	2	39	V_{GG}
Clock	3	38	CRA
Not Used	4	37	CQZ
Not Used	5	36	CDA
Data Bus 8	6	35	CIO
Data Bus 7	7	34	Not Used
Data Bus 6	8	33	Not Used
Data Bus 5	9	32	Not Used
Data Bus 4	10	31	Not Used
Data Bus 3	11	30	Not Used
Data Bus 2	12	29	Not Used
Data Bus 1	13	28	Not Used
Peripheral Bus 8	14	27	Address Bus 6
Peripheral Bus 7	15	26	Address Bus 5
Peripheral Bus 6	16	25	Address Bus 4
Peripheral Bus 5	17	24	Address Bus 3
Peripheral Bux 4	18	23	Address Bus 2
Peripheral Bus 3	19	22	Address Bus 1
Peripheral Bus 2	20	21	Peripheral Bus 1

40 LEAD DUAL IN LINE
LP6000 PROGRAM MEMORY

Top View

V_{CC}	1	40	Peripheral Bus A1
Data Bus 1	2	39	Peripheral Bus A2
Data Bus 2	3	38	Peripheral Bus A3
Data Bus 3	4	37	Peripheral Bus A4
Data Bus 4	5	36	Peripheral Bus A5
Data Bus 5	6	35	Peripheral Bus A6
Data Bus 6	7	34	Peripheral Bus A7
Data Bus 7	8	33	Peripheral Bus A8
Data Bus 8	9	32	Peripheral Bus B1
Not Used	10	31	Peripheral Bus B2
Power on Reset	11	30	Peripheral Bus B3
Address Bus 1	12	29	Peripheral Bus B4
Address Bus 2	13	28	Peripheral Bus B5
Address Bus 3	14	27	Peripheral Bus B6
Address Bus 4	15	26	Peripheral Bus B7
Address Bus 5	16	25	Peripheral Bus B8
Address Bus 6	17	24	V_{GI}
Clock	18	23	V_{GG}
CDA	19	22	CRA
CIO	20	21	CQZ

8 LEAD DUAL IN LINE
LP1030 CLOCK GENERATOR

Top View

V_{CC}	1	8	Reset Output
Timing Input	2	7	ϕ_{SN} Output
Synchronizing Input	3	6	Clock Output
Reset Input	4	5	V_{GG}

40 LEAD DUAL IN LINE
LP1010 INPUT/OUTPUT BUFFER

Top View

V_{CC}	1	40	Peripheral Bus A1
Data Bus 1	2	39	Peripheral Bus A2
Data Bus 2	3	38	Peripheral Bus A3
Data Bus 3	4	37	Peripheral Bus A4
Data Bus 4	5	36	Peripheral Bus A5
Data Bus 5	6	35	Peripheral Bus A6
Data Bus 6	7	34	Peripheral Bus A7
Data Bus 7	8	33	Peripheral Bus A8
Data Bus 8	9	32	Peripheral Bus B1
Chip Select	10	31	Peripheral Bus B2
Power on Reset	11	30	Peripheral Bus B3
Address Bus 1	12	29	Peripheral Bus B4
Address Bus 2	13	28	Peripheral Bus B5
Address Bus 3	14	27	Peripheral Bus B6
Address Bus 4	15	26	Peripheral Bus B7
Address Bus 5	16	25	Peripheral Bus B8
Address Bus 6	17	24	PAD 4
Clock	18	23	V_{GG}
CDA	19	22	PAD 3
CIO	20	21	PAD 2

A pair of adjacent addresses is selected by PAD 4, PAD 3 and PAD 2 in the range 48 to 63, e.g. 011 selects peripheral addresses 54 and 55.

40 LEAD DUAL IN LINE
LP1000 MEMORY INTERFACE

Top View

V_{CC}	1	40	V_{GI}
Data Bus 1	2	39	V_{GG}
Data Bus 2	3	38	Address Bit 11
Data Bus 3	4	37	Address Bit 10
Data Bus 4	5	36	Address Bit 9
Data Bus 5	6	35	Address Bit 8
Data Bus 6	7	34	Address Bit 7
Data Bus 7	8	33	Address Bit 6
Data Bus 8	9	32	Address Bit 5
Power on Reset	10	31	Address Bit 4
Address Bus 1	11	30	Address Bit 3
Address Bus 2	12	29	Address Bit 2
Address Bus 3	13	28	Address Bit 1
Address Bus 4	14	27	Clock
Address Bus 5	15	26	$\overline{R}/W$
Address Bus 6	16	25	Memory Enable
PAD 4	17	24	MIC Enable
PAD 5	18	23	CRA
PAD 6	19	22	CQZ
CIO	20	21	CDA

10

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All pins with respect to V_{cc} . . . . . −20V to +0.3V
Storage Temperature . . . . . −55°C to +150°C
Operating Temperature . . . . . 0°C to +75°C

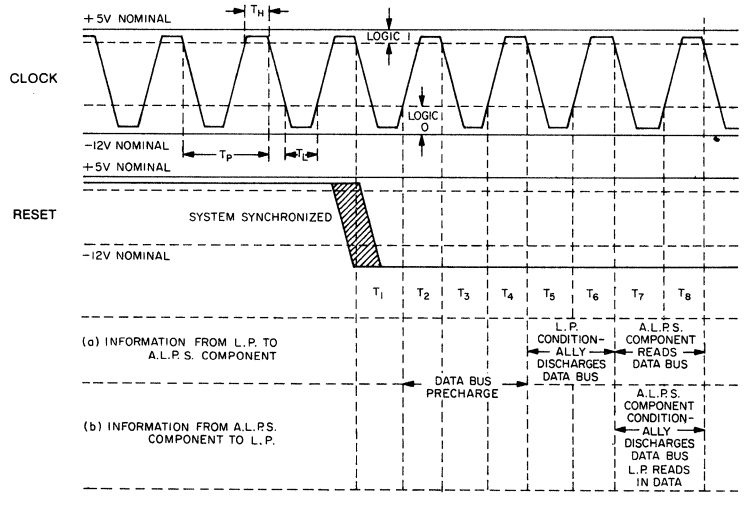
*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5V ±0.25V
V_{GI} = GND (substrate at V_{CC})
V_{GG} = −12V ±1V

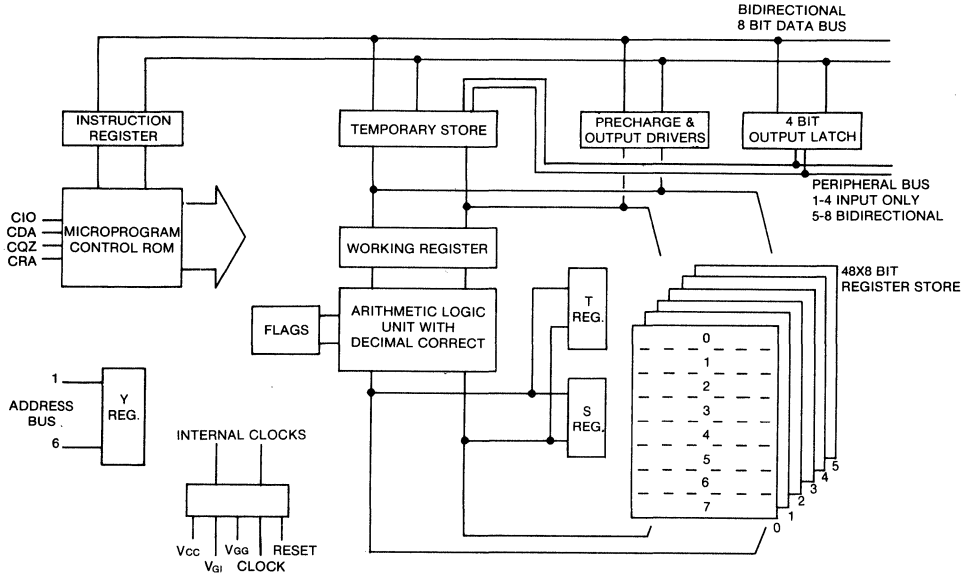
Characteristic	Min	Max	Units	Conditions
Clock Frequency	500	800	KHz	—
Machine Cycle Time	5	8	μs	—
Clock and Reset Input				
Logic '1'	Vcc −1.5	—	Volts	—
Logic '0'	—	−9.5	Volts	—
Data Bus				
Input Conditions				
Logic '1'	V_{CC} −1.5	—	Volts	—
Logic '0'	—	+0.8	Volts	—
Output Conditions				
Logic '1'	V_{CC} −1.0	—	Volts	Capacitive load
Logic '0'	—	+0.4	Volts	only, maximum 275pF
Control & Address Bus				
Logic '0'	V_{CC} −1.5	—	Volts	—
Logic '1'	—	+0.8	Volts	—
Address Bus				
Logic '0'	V_{CC} −1.0	—	Volts	Capacitive load
Logic '1'	—	−7.0	Volts	200pF
Peripheral Bus				
Logic '1'	V_{CC} −1.5	—	Volts	—
Logic '0'	—	+0.8	Volts	—
Output ON Current IOB	2	—	mA	Vds = 1 Volt
Other Devices	1	—	mA	Vds = 1 Volt
Output OFF Current				
All Devices	—	1	uA	Vin − Vgg at 25°C
Power Consumption LP 8000	—	1000	mW	—
All other chips	—	500	mW	—

TIMING DIAGRAMS

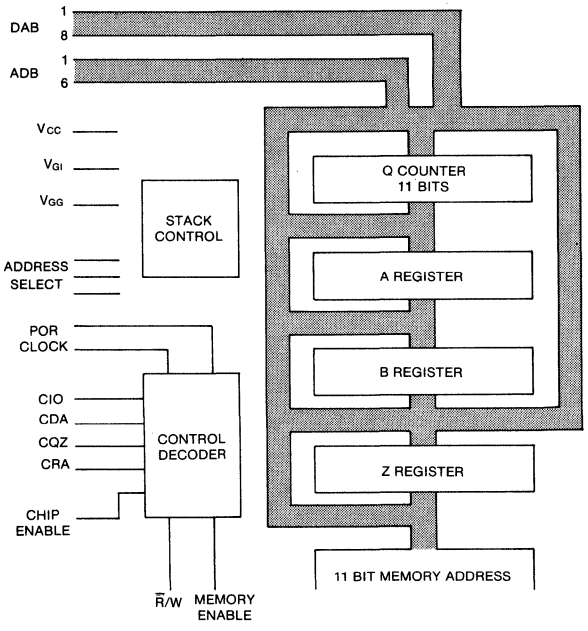


	Mnemonics	Operation	Cycles	Comments
INTERNAL REGISTER INSTRUCTION	LAR	Load Accumulator from Register	1	These instructions are used to manipulate the contents of the accumulator with one of the 48 internal registers. They have a four bit argument and direct addressing is assumed for 0-11 but indirect for 12, 13, and 14. For indirect addressing the register address is held in S,T. Argument 12 gives register pointed to by S & T; 13 gives the same then S is decremented. 14 also addresses via S & T and then S is incremented.
	SAR	Store Accumulator in Register	1	
	DEC	Decrement Register by one *	1	
	ADR	BCD Add Accumulator with Register *	2	
	BAD	Binary Add Accumulator with Register	1	
	AND	Logical AND Accumulator with Register	1	
	EOR	Exclusive OR Accumulator with Register	1	
		*The results of these operations are stored in the respective register. The result of all other operations is stored in the accumulator.		
REGISTERS S&T	LSS	Load S with Short (3-bit) Literal	1	
	LST	Load T with Short (3-bit) Literal	1	
	SAT	Store Accumulator in Register T	1	Lower order bits (1-3) of accumulator are copied in register T.
	SST	Store Accumulator in Registers S & T	1	Bits (1-3) of accumulator copied in register S, bits (4-6) copied in register T.
EXTERNAL REFERENCE INSTRUCTIONS	LAL	Load Accumulator with 8-bit Literal	2	
	LAS	Load Accumulator with 4-bit Literal	1	
	ALL	Logical AND, Accumulator with 8-bit Literal	2	
	ORL	Logical OR, Accumulator with 8-bit Literal	2	
	EOL	Exclusive OR, Accumulator with 8-bit Literal	2	
	ALA	Add Accumulator with 8-bit Literal	2	
	CMP	Compare Accumulator with 8-bit Literal	2	
	LIX	Load Accumulator Indirect Module X	4	The lower six bits of the X and Y registers are used to address 256-bit modules of data and program respectively. The 8-bit data bus is used to provide the intra-module address. These three instructions respectively fetch or store data using the address in the register to specify the module.
	LIY	Load Accumulator Indirect Module Y	4	
	SIX	Store Accumulator Indirect Module X	3	
SIMULATOR & ADDRESS CONTROL REGISTERS	SAX	Store Accumulator in Register X	1	Used in normal register operation and also for setting up module addresses for program and data manipulation.
	SAY	Store Accumulator in Register Y	1	
	LAX	Load Accumulator from Register X	1	
	LAY	Load Accumulator from Register Y	1	
	SZX	Store Accumulator in Z Register Module X	3	Used to set Q Counter or Z register of required module.
	SZY	Store Accumulator in Z Register Module Y	3	
	SQX	Store Accumulator in Q Counter Module X	3	The Y register points to the active program module, the X register points to an alternative module or a data space.
	SQY	Store Accumulator in Q Counter Module Y	3	
	SAV	Store Accumulator in Register V	1	These four instructions allow direct access to the internal registers which are masked by the operand code used for indirect addressing i.e. 12, 13,
	SAW	Store Accumulator in Register W	1	
	LAV	Load Accumulator in Register V	1	
	LAW	Load Accumulator in Register W	1	
	CLA	Clear Accumulator to Zeros	1	
SHIFT	LSA	Shift Accumulator Left 1-bit	1	Carry Flag set unconditionally
	RSA	Shift Accumulator Right 1-bit	1	Carry Flag cleared unconditionally
	LSN	Shift Accumulator Left 4-bits	1	
	RSN	Shift Accumulator Right 4-bits	1	
INPUT/OUTPUT INSTRUCTIONS	LAM	Load Accumulator from Module Direct	2	The indirect I/O operations use the X register for module addressing. The SAX instruction is used to set up the system for the indirect mode.
	SAM	Store Accumulator in Module Direct	3	
	LIM	Load Accumulator from Module Indirect	4	
	SIM	Store Accumulator in Module Indirect	3	
JUMP WITHIN2K PAGE	JMP	Jump Unconditional	3	
	JIZ	Jump if all Zeros	3/2	3 if true, 2 if false
	JNZ	Jump if not all zeros	3/2	
	JIP	Jump if sign bit positive	3/2	
	JRS	Jump if Register S not equal to seven	3/2	Used to sequence through a 'page' of internal registers.
	JCS	Jump if carry bit set	3/2	
	JCN	Jump if carry bit not set	3/2	
SUBROUTINE INSTRUCTIONS	GOS	Go to Subroutine	3	Program counter automatically stored in memory chip stack.
	RET	Return from Subroutine	2	

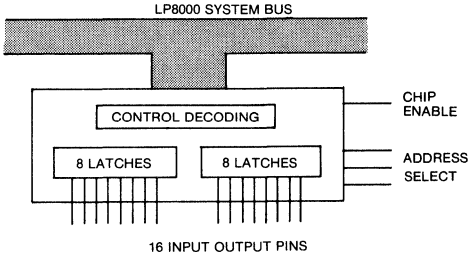
INTERNAL BLOCK DIAGRAM OF LP8000 CHIP



LP1000 MEMORY INTERFACE CHIP



LP1010 INPUT/OUTPUT BUFFER



(Open Drain Configuration
TTL Compatible with Pull
Down Resistors)

DEVELOPMENT FAMILY

A production system may consist of only a Logic Processor, LP8000, and ROM, LP6000, (plus Clock Generator, LP1030). However, the practical development family which complements the LP8000 allows the user to implement his hardware and software in a real time replacement mode for his final mask programmed product. LP1000 and LP1010 parts, plus PROM, can directly replace the LP6000 ROM. Indeed the development family may well be used as the complete solution for short run multi-variety systems.

DEVELOPMENT SUPPORT

Circuits

LP 8000 systems use only a small number of integrated circuits for cost effective implementation. For development and pre-production LP 1000 (Memory Interface Circuit) and LP 1010 (Input-Output Buffer) can be used with PROM, EAROM or RAM to replace the final mask-programmed ROM (see diagram). The system using PROM or EAROM behaves identically with the final mask-programmed ROM version. When the program has been proved, the LP1000, LP1010, and PROM/EAROM can all be replaced by LP 6000 to give the final low-cost system using perhaps as few as two 40 lead DIPs (LP 8000 + LP 6000), and one 8 lead DIP (LP 1030). Small production runs, or systems needing extensive RAM memory can remain with LP 1000 and LP 1010.

Prototype System

To simplify hardware and software development and help speed the users product design cycle time, a complete hardware prototype development system is available to support the Series 8000 family. The GIC 8000 Microcomputer System provides a test bed for user designed interfaces and related hardware as well as a program preparation facility with resident, on-line hardware and software debug aids. The users program can be tested and modified under real time operating conditions. To make program development fast and efficient, peripheral interfaces and their related software including TTY high speed reader, high speed punch and serial line printer are included on the prototype system. In addition, all of the card level modules of this system, ranging from complete microcomputers to memory or I/O modules, are available on an OEM basis for further system integration.

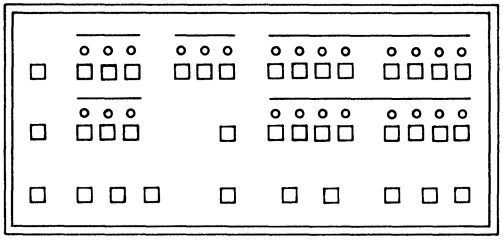
Software

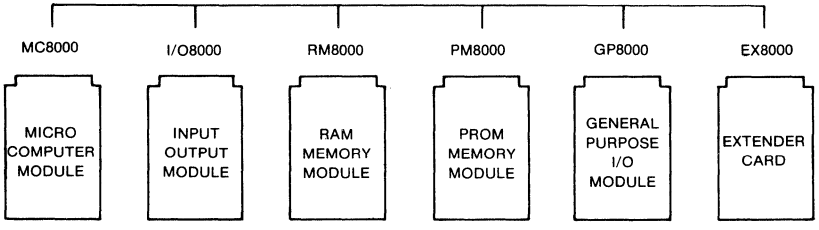
For pure program development to check the flow of instructions, a complete assembler and simulator written in FORTRAN IV is available for operation on minicomputer systems or on internal or external time share networks.

Manual

A manual describing complete hardware aspects of Series 8000, and details of the program preparation software is available from all General Instrument Microelectronics Sales Offices, Agencies, and Distributors.

SERIES 8000 DEVELOPMENT SYSTEM/MODULES





10

GENERAL INSTRUMENT

RA-3-4256
RA-3-4256A
RA-3-4256B
RA-3-4200
RA-3-4402

11

RA-3-4256
RA-3-4256A
RA-3-4256B

1024 Bit Static Random Access Memories

FEATURES

- 256 x 4 Organization
- Single +5 Volt Supply
- True TTL Compatability
- Static Operation—no clocks required
- 500ns Access Time: RA-3-4256
- 650ns Access Time: RA-3-4256A, RA-3-4256B
- Separate Data Input and Output Lines
- Low Power
- Three State Outputs—under control of Chip Select signals
- Power Down State: RA-3-4256, RA-3-4256A
- Zener Protected Inputs

DESCRIPTION

The General Instrument RA-3-4256, RA-3-4256A and RA-3-4256B are 1024 bit, high-speed static random access memories organized as 256 4-bit words. Low voltage N-channel ion implant technology results in true TTL compatibility from a single 5 volt supply, and static operation. These devices are extremely useful in small read-write memory systems for terminals, peripherals, microcomputers, and a wide variety of portable equipment.

The RA-3-4256 and RA-3-4256A can also utilize a back bias substrate and split supply for applications where a low standby power drain is required. These devices may be switched to the power down state under system control with no danger of memory storage errors.

The RA-3-4256B's 22-pin package, which has a 0.4" width, permits tight packing density on printing circuit cards.

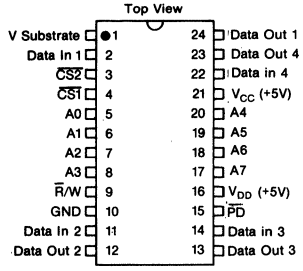
	RA-3-4256	RA-3-4256A	RA-3-4256B
Package	24-pin	24-pin	22-pin
No. of Chip Select Inputs	2	2	1
Power Down Capability	Yes	Yes	No
Max Access Time	500ns	650ns	650ns

PIN CONFIGURATIONS

24 LEAD DUAL IN LINE

RA-3-4256/RA-3-4256A

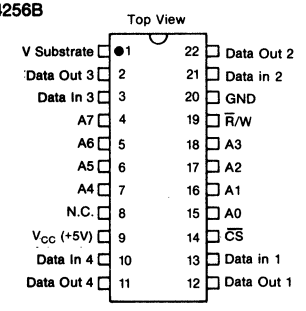
Top View



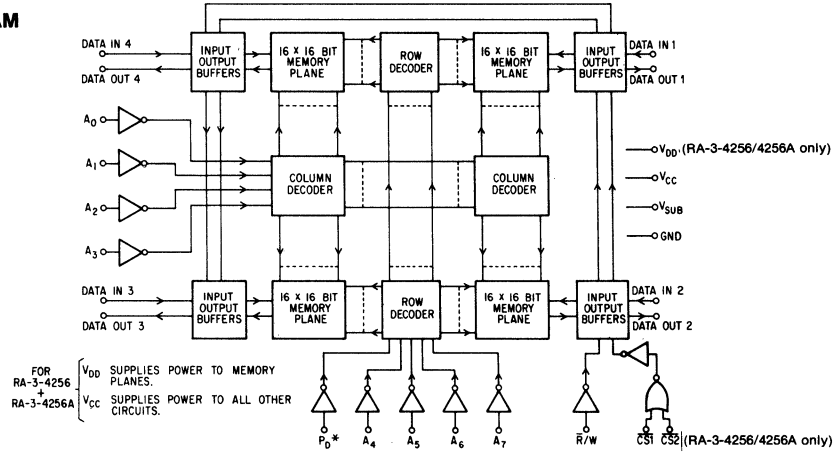
22 LEAD DUAL IN LINE

RA-3-4256B

Top View



BLOCK DIAGRAM



POWER DOWN OPERATION

The RA-3-4256 and RA-3-4256A bring out, to separate pins, the circuit Substrate, the memory plane supply (V_{DD}) and the peripheral circuit's power supply (V_{CC}). These three connections, plus the Power Down input, allow extremely flexible control of the memory during standby and/or reduced voltage and power dissipation operation.

In a static memory the memory cell is a flip flop and, in order to retain information, one side of the flip flop must be on continuously. Thus the static memory power dissipation is higher than for a dynamic memory and techniques for reducing this dissipation when the device is in the standby condition become attractive for the system user.

The power down pin ($\overline{PD}$ pin 15) isolates the memory from the address decoders, so that incorrect data cannot be written into the memory when V_{CC} is not within its specified limits. Even if V_{DD} is maintained by a battery, if V_{CC} falls in a manner such that the $\overline{R}/W$ circuitry considers itself to be in a write mode for a short interval of time, then false data will be written into the memory. To prevent this from happening, $\overline{PD}$ is driven low by a signal (Power Down In) that senses V_{CC} is going below its allowable range; this is usually done by monitoring the power supply's AC input voltage. Fig. 1 shows the timing required before V_{CC} falls, to preserve a memory with a battery backup on V_{DD}.

To prevent miswriting a data word, the fall of the $\overline{PD}$ signal must not intersect the $\overline{R}/W$ pulse. Otherwise, the write operation may not be complete at a given address when $\overline{PD}$ falls. The fall of $\overline{PD}$ during the $\overline{R}/W$ pulse would prevent that address (and all others) from having access to the memory section of the device. The external gating in Fig. 1b disallows $\overline{PD}$ from falling during a write operation.

Battery backup for V_{DD} can be accomplished as shown in Fig. 2. The germanium power transistor (2N3612) is used here as a power diode. For a card with 10 RA-3-4256's, V_{DD} would draw a maximum current of 500 mA. The 2N3612 would have a maximum collector emmiter voltage drop of .25 v dc at 500 mA base current. During normal operation, if V_{CC} varied from 4.75 to 5.25 volts, V_{DD} would vary from 4.5 to 5.00 volts, which is within the operating specification. In the power down mode, V_{DD} would be supplied by the 5v standby battery. The battery voltge could fall from 5v to 4.5v (which would be from 4.25V to 3.75V for V_{DD} because of the silicon diode) and still keep the memory alive.

Once the memory is powered down so that the total supply current is reduced by a factor of 2 (since V_{CC} = 0 and is not drawing any current), I_{DD} can be reduced in half by placing −5 volts on V_{SS} — pin 1. This back-biases the substrate which reduces the current drawn in each flip-flop in the memory during this memory hold state. The −5 volts on V_{SS} can only be used to retain the information in the memory and must be removed (V_{SS} = 0) before writing into or reading from the memory.

Thus, using the power down mode and placing −5 volts on the substrate, total power dissipated would be reduced 75%, from a maximum of 500mW (5v × 100 mA) to 125 mW (5v × 25 mA).

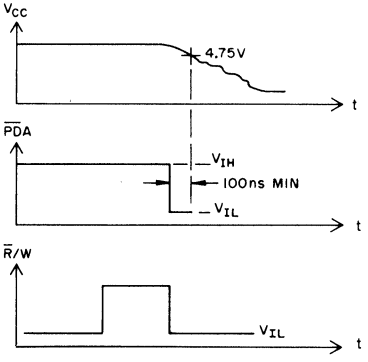


Fig.1a POWER DOWN TIMING

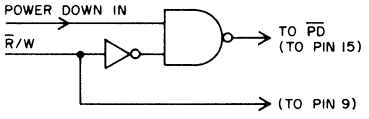


Fig.1b POWER DOWN GATING

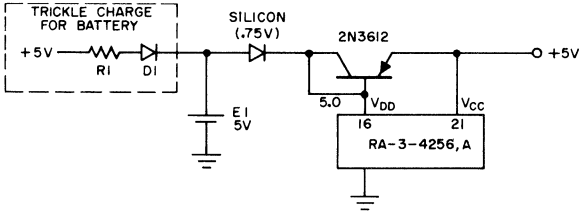


Fig.2 BATTERY STANDBY SCHEMATIC

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ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC}, V_{DD} and input voltages (with respect to GND) ....-0.3V to +8.0V
Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

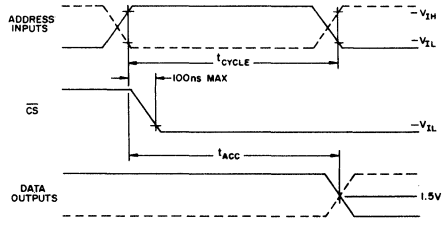
Standard Conditions (unless otherwise noted)

V_{CC} = +5V ±5% (V_{CC} is the peripheral circuitry supply for the RA-3-4256/4256A and the power supply for RA-3-4256B.)
V_{DD} = +5V ±10% (V_{DD} is the memory call supply for the RA-3-4256/4256A.)
$V_{Substrate}$ = GND
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL Load, C_{LTOTAL} = 100pF

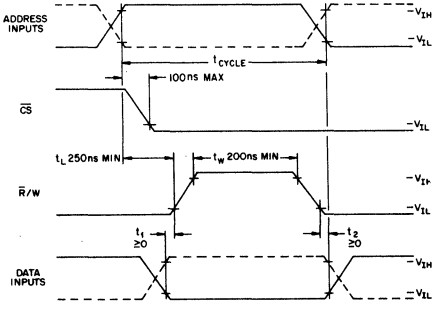
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Input load current (all inputs)	I_{IN}	—	—	10	μA	V_{IN}=0V to 5.25V
Output leakage current	I_{LOH}	—	—	10	μA	V_{OUT}=4.0V
Output leakage current	I_{LOL}	—	—	−10	μA	V_{OUT}=0.4V
Input low voltage	V_{IL}	—	—	0.65	V	
Input high voltage	V_{IH}	2.2	—	—	V	
Output low voltage	V_{OL}	—	—	0.40	V	I_{OL}=1.6mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH}=100μA
Input capacitance (all inputs)	C_{IN}	—	5	—	pF	f=1 MHz
Output capacitance (all outputs)	C_{OUT}	—	10	—	pF	f=1 MHz
Total Power Supply Current	I_{DD} & I_{CC}	—	60	100	mA	RA-3-4256, RA-3-4256A
Power Supply Current	I_{CC}	—	30	50	mA	RA-3-4256, RA-3-4256A
Power Supply Current	I_{DD}	—	30	50	mA	RA-3-4256, RA-3-4256A
Power Supply Current	I_{CC}	—	60	100	mA	RA-3-4256B
AC CHARACTERISTICS						
Access Time RA-3-4256	T_{ACC}	—	—	500	ns	
Cycle Time RA-3-4256	T_{CYCLE}	500	—	—	ns	
Access Time RA-3-4256A	T_{ACC}	—	—	650	ns	See Timing Diagrams
Cycle Time RA-3-4256A	T_{CYCLE}	650	—	—	ns	
Access Time RA-3-4256B	T_{ACC}	—	—	650	ns	
Cycle Time RA-3-4256B	T_{CYCLE}	650	—	—	ns	
POWER DOWN DC CHARACTERISTICS (RA-3-4256 & RA-3-4256A ONLY):						
Power Down Sink Current	I_{PD}	—	—	100	μA	V_{PD}=0.4V
Memory hold voltage	V_{DD}	3.75	—	7.0	V	V_{CC}=0
Substrate Power Supply	V_{SS}	−5	—	0	V	−5V in Power Down Mode only
Substrate Power Supply Current	I_{SS}	—	20	100	μA	V_{SS}=−5V, V_{CC}=0

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS

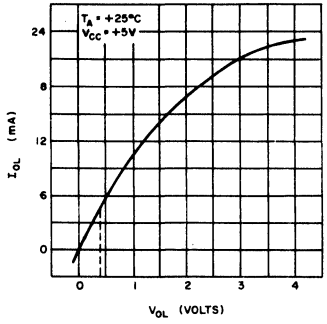


READ ACCESS

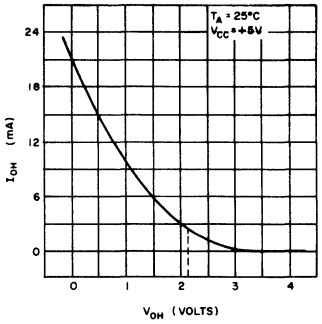


WRITE CYCLE

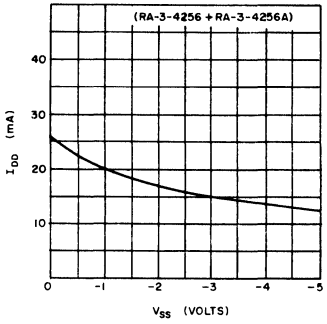
TYPICAL CHARACTERISTIC CURVES



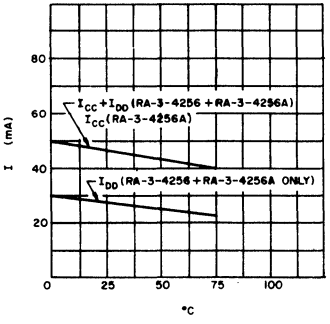
TYPICAL OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



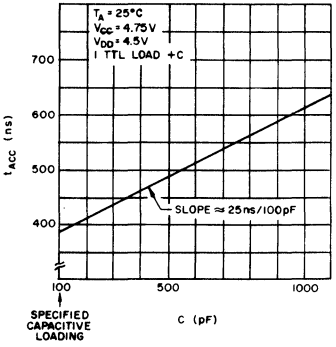
TYPICAL OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



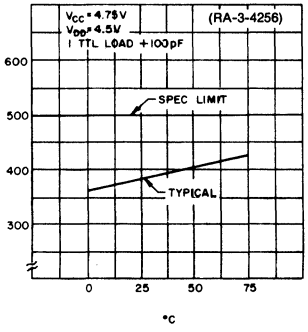
TYPICAL I_{DD} VS. V_{SS} (for memory hold during power down)



TYPICAL POWER SUPPLY CURRENT VS. TEMPERATURE



T_{ACC} (Typical) VS. CAPACITIVE LOADING



T_{ACC} VS. TEMPERATURE

11

4096 Bit Static Random Access Memory

FEATURES

- 4096×1 Organization
- Static Memory-no refresh required
- TTL Compatible Inputs (except CS)
- TTL Compatible Output
- Wire-Or'able Output-under control of a 'Chip Select' input
- High Speed: 215ns access time, 400ns cycle time
- Low Power: typically 450mW operating, 35mW standby
- Pin and Voltage Compatible with Popular 22 pin 4K Dynamic RAMs

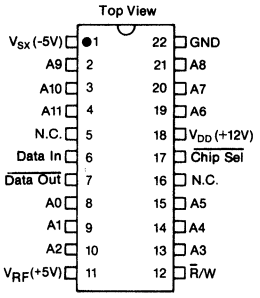
DESCRIPTION

The General Instrument RA-3-4200 is a 4096 bit static Random Access Memory ideally suited for memory system applications where there is an advantage in utilizing a static memory without sacrificing the high speeds that current dynamic memories offer. The RA-3-4200 is fabricated in GI's advanced GIANT II N-channel Ion Implant process and features a fully static memory cell to eliminate the need for any refresh or charge-pump circuitry and TTL compatibility except for a +12Volt Chip Select which dynamically accesses the memory.

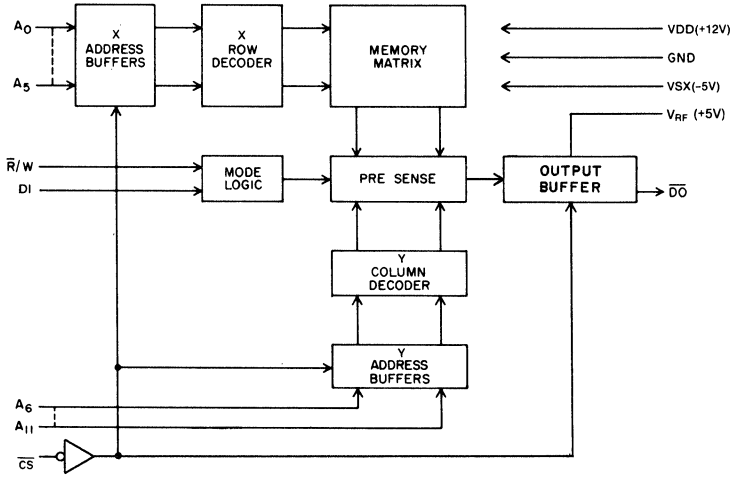
The RA-3-4200 is a direct replacement in pin connection and operation for the EM&M/SEMI 4200.

PIN CONFIGURATION

22 LEAD DUAL IN LINE



BLOCK DIAGRAM



OPERATION

The 4096 static bits of memory are organized in an array of 64 rows by 64 columns. The memory cells are loaded or interrogated by simultaneously decoding the X address A_0 through A_5 for the rows (see Block Diagram) and the Y address A_6 through A_{11} for the columns. Each column contains a presense amplifier, the outputs of which are "OR-ed" and connected to the output TTL buffer. Each bit or memory cell is a standard flip flop consisting of R_1, R_2, Q2D and Q4D with two access devices Q1D and Q3D (See Figure 1). The load resistors R_1 and R_2 are 60 megohms typical and connect to the V_{DD} supply. Q1D and Q3D are used to connect the cell to the sense lines whenever the X access line is high. In the read mode the cell pulls one of the sense lines low from its normally high state. The selected presense circuit detects the differential voltage on the sense lines and amplifies it. In the write mode one sense line is forced low by the presense circuit and the selected cell assumes the state of the sense lines.

Chip Select

The Chip Select controls the operation of the memory. When the Chip Select input is high the input address buffers, decoders, sensing circuits and output stages are held in the "off" state and power is supplied only to the memory elements. When the Chip Select input is pulled low, the memory is enabled. The Chip Select negative going edge clocks the TTL logic level addresses, $\overline{R}/W$, and data input into "D" type flip flops, and enables the output stage.

Data Output

While Chip Select is high, the output is high impedance to allow "wire-or" connections. When Chip Select goes low, the output data will be presented within the specified access time, and will remain until Chip Select goes high again. The output data signal is specified to drive any TTL series with good noise immunity at a fan-out of 1. Output data is inverted with respect to the input data.

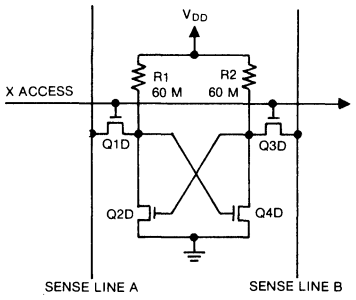


Fig.1 MEMORY CELL

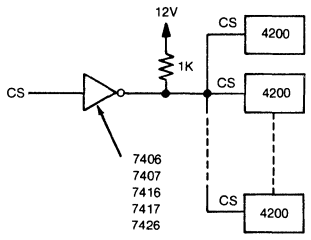


Fig.2 TYPICAL CHIP SELECT DRIVER

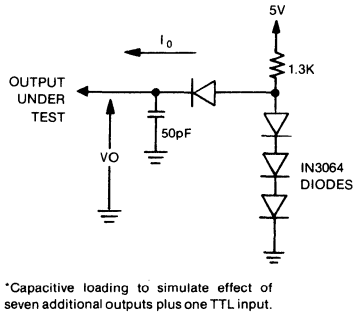


Fig.3 OUTPUT TEST LOAD

Battery Operation/Power Failure Data Retention

The memory cells (because they are cross coupled high impedance static cells) will retain data down to V_{DD} = 4V.

Input Circuits — $\overline{R}/W$ Select, Data In and Address Input

The input signal is latched by Chip Select and can change after the specified hold time. The inputs can be driven from standard TTL open collector outputs with pull-up resistors. The input does not put any DC loading on the TTL driver.

Read/Write Mode Select

To WRITE, the $\overline{R}/W$ Input should be high prior to Chip Select. To READ, the $\overline{R}/W$ Input should be low prior to Chip Select. When Chip Select goes low, $\overline{R}/W$ is latched into a register.

Data In

During a WRITE cycle the Data In (either high or low) should be stable prior to Chip Select. When Chip Select goes low, $\overline{R}/W$ is latched into a register.

Address

Addresses should be stable prior to Chip Select. When Chip Select goes low all addresses are latched into an Address Register.

ABSOLUTE MAXIMUM RATINGS (See Note 1) (Referenced to GND)

Rating	Sym	Value	Unit
Supply Voltages	V_{DD}	−.5 to +15	Vdc
	V_{RF}	+.5 to +7	Vdc
	V_{SX}	+.5 to −7	Vdc
Input & Output Voltages (Except Chip Select)	V_I, V_O	V_{SX} to +15	Vdc
Chip Select Input Voltage	V_{CS}	V_{SX} to +15	Vdc
Power Dissipation	P_D	1.6 (Note 2)	W
Operating Ambient Temperature Range	T_{AMB}	0 to +70	°C
Storage Temperature Range	—	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended or maximum voltages for extended periods of time could affect device reliability.

NOTE 2: At 25°C ambient Derate 13.5m W/°C.

RECOMMENDED OPERATING CONDITIONS T_{AMB} = 0°C to 70°C

Parameter	Sym	Min	Nom	Max	Unit
Supply Voltage	V_{DD}	11.4	12.0	12.6	Vdc
Output Reference Voltage	V_{RF}	4.75	5.0	5.25	Vdc
Substrate Voltage	V_{SX}	−4.5	−5	−5.5	Vdc
Input High Level	V_{IH}	3	—	5.25	Vdc
Input Low Level	V_{IL}	0	—	0.8	Vdc
Chip Select High Level	V_{CH}	V_{DD}−3	V_{DD}	V_{DD}+3	Vdc
Chip Select Low Level	V_{CL}	0	—	0.5	Vdc

DC ELECTRICAL CHARACTERISTICS (Full Operating Voltage and Temperature Range Unless Otherwise Noted)

Characteristics	Sym	Min	Typ	Max	Unit	Conditions
Input Current	I_{IN}	0	±10	±100	μA	V_{IN} = 0.5V or 5.0V
Chip Select Input Current	I_{CS}	—	±10	±100	μA	v_{CS} = 0.5V or 12V
Output "Low" Voltage	V_{OL}	—	0.3	0.5	Vdc	I_O = 2.0mA Fig. 5
Output "High" Voltage	V_{OH}	2.7	3.5	V_{RF}	Vdc	I_O = 500 μA Fig. 5
Output Current (Unselected)	I_{DO}	—	—	−50	μA	V_{OL} = 2.7V, V_{CS} +12V
Supply Current (Selected and Averaged over one cycle)	I_{DD}	—	36	50	mA	V_{DD} +12V
CSW = 215 nsec						V_{RF} = +5V
TC = 400 nsec						V_{SX} = −5V
For Other Conditions, See Fig.3						T_{AMB} = +25°C
Supply Current (Unselected) T_{AMB} = +25°C	I_{DDU}	—	2	5	mA	V_{DD} = +12V
Supply Current (Unselected) T_{AMB} = +70°C	I_{DDU}	—	4.5	15	mA	V_{RF} = +5V
Substrate Current	I_{SX}	—	2.2	−3	mA	V_{SX} = −5V
Reference Supply Current	I_{RF}	—	50	100	μA	V_{CS} = +12V
Standby Current at Reduced Voltages T_{AMB} = +25°C	I_{DDS}	—	0.8	2	mA	V_{CS} = 4V to 15V V_{DD} = 4V
Standby Current at Reduced Voltages T_{AMB} = +70°C	I_{DDS}	—	1.8	6	mA	V_{SX} = −5V±10% V_{RF} = OV

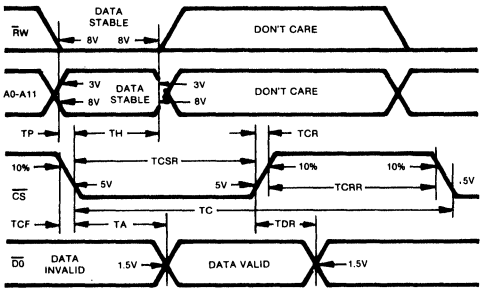
AC ELECTRICAL CHARACTERISTICS (Full Operating Voltage and Temperature Range Unless Otherwise Noted)

Characteristics	Sym	Min	Typ	Max	Unit	Fig
Chip Select Read Pulse Width	T_{CSR}	215ns	—	1ms	—	1
Chip Select Write Pulse Width	T_{CSW}	215ns	—	1ms	—	2
Chip Select Rise and Fall Time	T_{CR}, T_{CF}	—	10	50	ns	1&2
Set Up Time	Tp	0	—		ns	1&2
Access Time	T_A	—	—	215	ns	1
Cycle Time, T_{CR} T_{CF} = 10ns (Read or Write)	T_C	400	—	—	ns	1&2
Data Hold Time	T_H	100	—	—	ns	1&2
Output Recovery Time	T_{DR}	10	15	—	ns	1
Read Recovery Time	T_{CRR}	150	—	—	ns	1
Write Recovery Time	T_{CWR}	150	—	—	ns	2

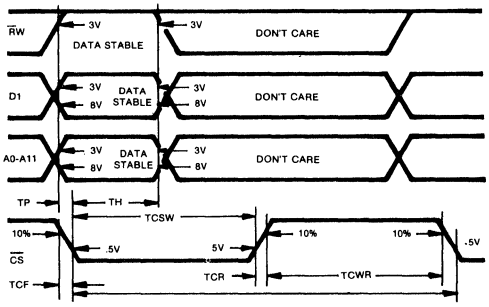
CAPACITANCE (Over Full Temperature Range and Worst Case Voltage Conditions)

Characteristics	Sym	Min	Typ	Max	Unit	Conditions
Input Capacitance (Except Chip Select)	C_{IN}	—	6	—	pF	V_{IN} = 24V
Input Capacitance Chip Select	C_{CS}	—	20	—	pF	V_{CS} = 12V or 0V
Ouptut Capacitance	C_O	—	8'	—	pF	V_O = 2V V_{CS} = 12V

TIMING DIAGRAMS

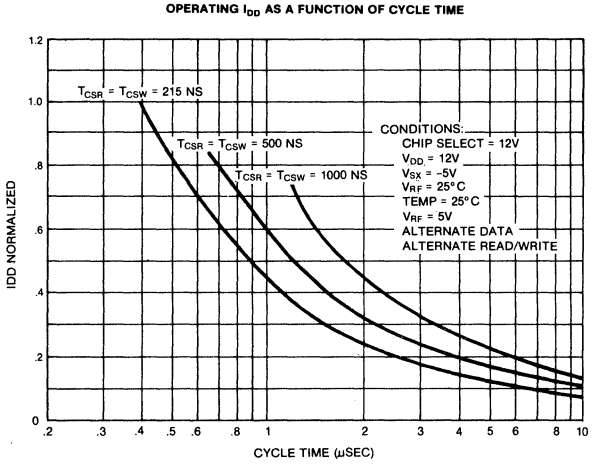


READ CYCLE



WRITE CYCLE

TYPICAL CHARACTERISTIC CURVE



OPERATING I_{DD} AS A FUNCTION OF CYCLE TIME

11

4096 Bit Static Random Access Memory

FEATURES

- 4096×1 Organization
- Static Memory-no refresh required
- TTL Compatible Inputs (except CS)
- Differential Output-two complementary Data Output signals are provided.
- Wire-Or'able Outputs-under control of a 'Chip Select' input.
- High Speed: 200ns access time, 350ns cycle time.
- Low Power: typically 400mW

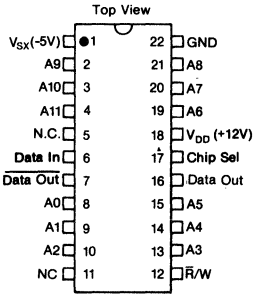
DESCRIPTION

The General Instrument RA-3-4402 is a 4,096 bit static Random Access Memory ideally suited for memory system applications where there is an advantage in utilizing a static memory without sacrificing the high speeds that current dynamic memories offer. The RA-3-4402 is fabricated in GI's advanced GIANT II N-channel Ion Implant process and features a fully static memory cell to eliminate the need for any refresh or charge-pump circuitry and TTL compatibility except for a +12Volt Chip Select which dynamically accesses the memory.

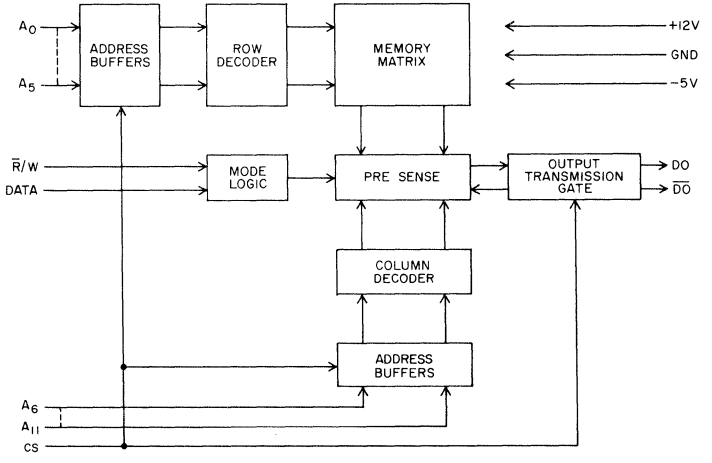
The RA-3-4402 is a direct replacement in pin connection and operation for the EM&M/SEMI 4402.

PIN CONFIGURATION

22 LEAD DUAL IN LINE



BLOCK DIAGRAM



OPERATION

The 4096 static bits of memory are organized in an array of 64 rows by 64 columns. The memory cells are loaded or interrogated by simultaneously decoding the X address A0 through A5 for the rows (see Block Diagram) and the Y address A6 through A11 for the columns. Each column contains a presense amplifier, the outputs of which are "OR-ed" and connected to the output stage. Each bit or memory cell is a standard flip flop consisting of R1, R2 Q2D, and Q4D with two access devices Q1D and Q3D (See Figure 1). The load resistors R1 and R2 are 60 megohms typical and connect to the V_{DD} supply. Q1D and Q3D are used to connect the cell to the sense lines whenever the X access line is high. In the read mode the cell will pull one of the sense lines low from its normally high state. The selected presense circuit will detect the differential voltage on the sense lines and amplify it. In the write mode one sense line is forced low by the presense circuit and the selected cell assumes the state of the sense lines.

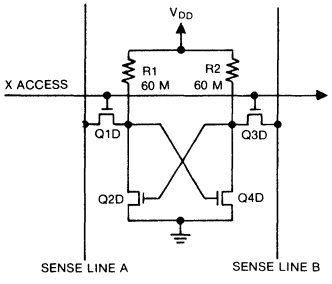


Fig.1 MEMORY CELL

Chip Select
The chip select controls the operation of the memory. When the chip select is low the input address buffers, decoders, sensing circuits and output stages are held in the "off" state and power is supplied only to the memory elements. When the Chip Select goes high the memory is enabled. The Chip Select pulse clocks the TTL logic level addresses, $\overline{R}/W$, and data input into "D" type flip flops and enables the output stage.

Data Output
One of the two outputs will source current (DO for data originally input at V_{IH}, $\overline{DO}$ for data originally input as V_{IL}). With the output load as shown in Figure 2, the voltage at the output sourcing current (V_{OH}) will approach a value between 0.35V and 2V (typically 1V) above ground. The voltage at the other output (V_{OL}) will be below 100 mV. A differential amplifier is used to detect the polarity of the signal. A differential output of 25mV (V_{OUT}) or more is considered a valid output.

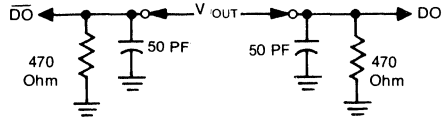


Fig.2 OUTPUT LOAD

Battery Operation/Power Failure Data Retention
The memory cells (because they are cross coupled high impedance static cells) will retain data down to $V_{DD} = 4V$. At $V_{DD} = 4V$, the typical power dissipated is 1μw/bit.

Input Circuits — R/W Select, Data In and Address Input
The input signal is latched by Chip Select and can change after Chip Select is high. The inputs can be driven from standard TTL open collector outputs with pull-up resistors. The input does not put any DC loading on the TTL driver.

Read/Write Mode Select
To WRITE, the $\overline{R}/W$ Input should be HIGH prior to Chip Select. To READ, the $\overline{R}/W$ Input should be LOW prior to Chip Select. When Chip Select is high, $\overline{R}/W$ is latched into a register.

Data In
During a WRITE cycle the Data In (either HIGH or LOW) should be stable prior to Chip Select. When Chip Select is high, Data In is latched into a register.

Address
Addresses should be stable prior to Chip Select. When Chip Select is HIGH all addresses are latched into an Address Register.

ABSOLUTE MAXIMUM RATINGS (See Note 1) (Referenced to GND)

Rating	Sym	Value	Unit
Supply Voltages	V_{DD}	−0.5 to +15	Vdc
	V_{SX}	+0.5 to +7	Vdc
Input & Output Voltages (except Chip Select)	V_1, V_0	V_{SX} to +15	Vdc
Chip Select Input Voltage	V_{CS}	V_{SX} to +15	Vdc
Power Dissipation	P_D	1.6 (Note2)	W
Operating Ambient Temperature Range	T_{AMB}	0 to +70	°C
Storage Temperature Range	T_{STG}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Note 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMEND OPERATING CONDITIONS. Exposure to higher than recommended or maximum voltages for extended periods of time could affect device reliability.

Note 2: At +25° C ambient, Derate 13.5m W/° C.

RECOMMENDED OPERATING CONDITIONS T_A = 0° C to +70° C

Parameter	Sym	Min	Nom	Max	Unit
Supply Voltages	V_{DD}	11.4	12	12.6	V
	V_{SX}	−4.5	−5	−5.5	V
Logic Levels:					
Input High Voltage (except Chip Select)	V_{IH}	3	—	5.25	V
Input Low Voltage (except Chip Select	V_{IL}	0	—	0.7	V
Chip Select High Voltage	V_{CH}	V_{DD}	V_{DD}+1V	V_{DD}+2V	V
Chip Select Low Voltage	V_{CL}	0	—	1	V

DC ELECTRICAL CHARACTERISTICS (Full Operating voltage & temperature range unless otherwise noted)

Characteristics		Sym	Min	Typ	Max	Unit
Input Current (except Chip Select)	V_{IH} = 5.0V (V_{CS} = V_{CH})	I_{IH}	—	5	25	μA
	V_{IL} = 0.5V (V_{CS} = V_{CH})	I_{IL}	—	−5	−25	μA
Unselected Input Current (V_{CS} = V_{CL}) V = 2.4V		I_{IU}	—	5	25	μA
Chip Select High Input Current, DC (V_{CS} = 12V)		I_{CH}	—	30	40	mA
Chip Select High Input Current, (Pulse Peak) V_{CS} = 12V T_{CR} = 25ns		I_{CP}	—	70	—	mA
Chip Select Low Input Current (V_{CS} = 1V)		I_{CL}	—	2	3	ma
Supply Current, (T_{AMB} = 25°C, V_{DD}, V_{SX} = nominal; all VI = max V_{IL}: DO, DO terminated as shown in Figure 2)	Unselected (Chip Select = 0 V)	I_{DDU} 25°C	—	1	5	mA
		I_{DDU} 70°C	—	3	15	mA
		I_{SXU}	—	−2	−3	mA
	Selected Chip Select = 12V, 50% duty cycle	I_{DD}	—	17.5	22.5	mA
		I_{SX}	—	−2	−3	mA
Standby Current at Reduced Voltages	25°C	I_{DDS}	—	.5	1.8	mA
V_{DD} = 4V, V_{SX} = 3V, V_{CS} = 0V	70°	I_{DDS}	—	1.5	5.3	mA
Substrate Current at Reduced Voltage	25°C V_{CS} = 0 VSX = −3	I_{SXS}	—	−1	−1.5	mA
Output Low Voltage Terminated per Figure 2 T_{csw} = 1μsec		V_{OL}	—	0	1	V
Output High Voltage Terminated per Figure 2 T_{csw} = 1μsec		V_{OH}	.35	1	2	V
Output Disabled Current V_{CL} = 0V, V_{OH} = 2V		I_{DO}	+10	—	−10	μA

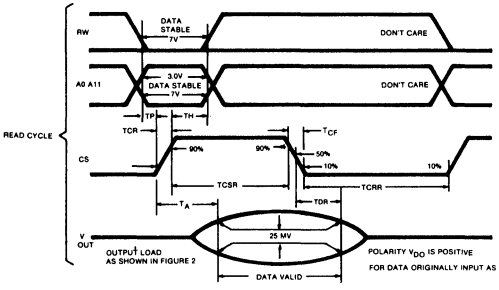
AC ELECTRICAL CHARACTERISTICS (Full Operating Voltage and Temperature Range Unless Otherwise Noted)

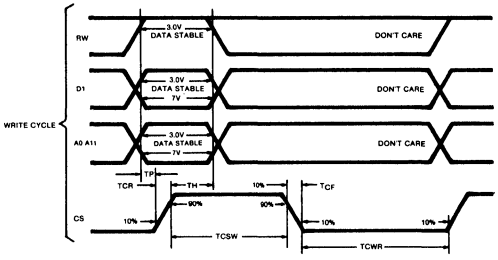
Characteristics	Sym	Min	Typ	Max	Unit
Chip Select Read Pulse Width	T_{CSR}	200	—	∞	ns
Chip Select Read Recovery Time	T_{CRR}	125	—	∞	ns
Chip Select Write Pulse Width	T_{CSW}	200	—	∞	ns
Chip Select Write Recovery Time	T_{CWR}	125	—	∞	ns
Chip Select Rise Time	T_{CR}	—	10	50	ns
Chip Select Fall Time	T_{CF}	—	10	50	ns
Set Up Time	T_P	10	—	—	ns
Hold Time (Address and Data)	T_H	50	—	—	ns
Access Time (T_{CR} = 10ns)	T_A	—	—	200	ns
Cycle Time (Read or Write, T_{CR} = 10ns, T_{CF} = 10ns)	T_C	350	—	—	ns
Data Recovery	T_{DR}	10	15	—	ns

CAPACITANCE (Over Full Temperature Range and Worst Case Voltage Conditions)

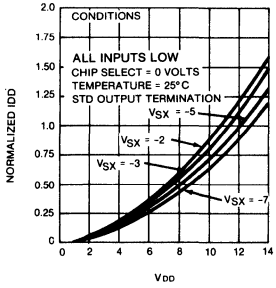
Characteristics	Sym	Min	Typ	Max	Unit
Input Capacitance (except Chip Select) V_I = 2.4V, V_{CS} = 12V	C_I	—	6	—	pF
Chip Select Input Capacitance	C_{CS}	—	50	—	pF
Output Capacitance (V_O = 2.0V. V_{CS} = 0)	C_O	—	5	—	pF

TIMING DIAGRAMS

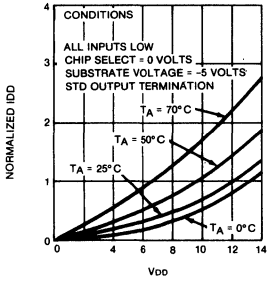




TYPICAL CHARACTERISTIC CURVES



I_{DD} VS. V_{DD} AT VARIABLE V_{SX}



I_{DD} VS. V_{DD} AT VARIABLE TEMPERATURE

11

GENERAL INSTRUMENT

ER1105
ER1400
ER2050
ER2401
ER2800
ER3400

12

1024 Bit Electrically Alterable Read Only Memory

FEATURES

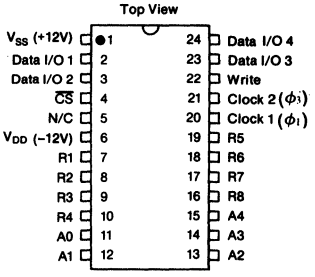
- 256 x 4 Organization
- 5-Bit Binary Column Address
- One of 8 Line Row Address
- Electrically Erasable by Row
- Electrically Reprogrammable
- 10 ms/4-Bit Word Write Time
- 2 μs Access Time
- Minimum Data Retention: 200×10^9 Read Accesses/Word between Refresh
- Chip Select Input
- Unpowered Nonvolatile Data Storage—10 Years

DESCRIPTION

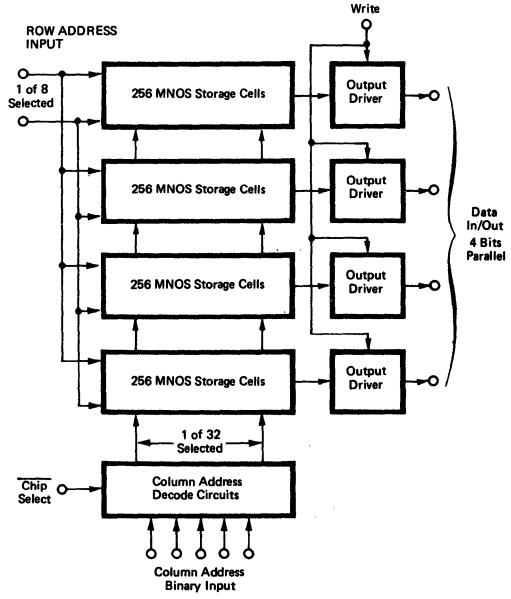
The ER1105 is a 256-word by 4-bit, electrically erasable and reprogrammable ROM that takes advantage of the unique properties of P-channel MNOS technology. Data is written into the device by tunneling a charge into the oxide-nitride interface at the gate insulator of MNOS memory transistors. This is accomplished by applying a -24 V , 10 ms row input pulse. The resulting charge trapped in the gate insulator causes a change in the threshold voltage of the memory transistors that is sensed during subsequent readout. Data is erased by applying a +30V, 100ms pulse to the row inputs. There are 8 blocks of 32 words×4 bits, each block being separately alterable.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Supply voltage (V_{DD}) relative to V_{SS} . . . . . +0.3 to -30V
Input voltage (except row input) relative to V_{SS} . . . . . +0.3V to -30V
Row input voltage relative to V_{SS} . . . . . +35V to -35V
Operating ambient temperature . . . . . -25°C to +70°C
Storage temperature . . . . . -65°C to +150°C
Soldering temperature of leads (10 seconds) . . . . . +300°C
Thermal resistance chip to ambient . . . . . 80° C/Watt
Power dissipation . . . . . 500 mW

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specifed below.

Standard Conditions (unless otherwise noted)

NOTE: This data sheet assumes negative logic.

V_{SS} = +12V±5%
V_{DD} = -12V±5%
Operating Temperature (T_A) = -25°C to +70°C

Characteristic	Symbol	Min.	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Input leakage current (all Inputs except row inputs)	I_{IN}	—	—	-1	μA	at V_{IN}=-15V, all other pins grounded, T_A=+25°C
Row input leakage current	I_R	—	—	-1	μA	at V_{IN}=±30V, all other pins grounded, T_A=+25°C
Input load current (all Inputs except row inputs)	I_B	—	—	-20	μA	at V_{IN}=-27V, all other pins grounded, T_A=+25°C
V_{DD} power supply current	I_{DD}	—	-9	-12	mA	at V_{DD} relative to V_{SS}=-24V, T_A=+25°C
ϕ_1/ϕ_3 input high voltage	$V_{IH}\phi$	V_{SS}—1.5	—	V_{SS}+0.3	V	
ϕ_1/ϕ_3 input low voltage	$V_{IL}\phi$	V_{DD}	—	V_{SS}—22	V	
Read Cycle						
Column address and chip select input high voltage	V_{IH1}	V_{SS}—1.5	—	V_{SS}+0.3	V	
Column address and chip select input low voltage	V_{IL1}	V_{DD}	—	V_{SS}—9.0	V	
Row input high voltage	V_{IH2}	V_{SS}—1.5	—	V_{SS}+0.3	V	
Row input low voltage	V_{IL2}	V_{SS}—13.0	—	V_{SS}—10.0	V	
Data output high voltage	V_{OH1}	V_{SS}—1.0	—	V_{SS}—0.5	V	R_{LOAD}=6.8K returned to V_{DD}
Data output low voltage	V_{OL1}	V_{DD}	—	—	V	R_{LOAD}=6.8K returned to V_{DD}
Erase Cycle						
Row input high erase voltage	V_{IHE}	V_{SS}+28	—	V_{SS}+32	V	
Write Cycle						
Col. add., $\overline{CS}$, and write input high voltage	V_{IH3}	V_{SS}—1.5	—	V_{SS}+0.3	V	
Col. add., $\overline{CS}$, and write input low voltage	V_{IL3}	V_{DD}	—	V_{SS}—9.0	V	
Row input high write voltage	V_{IH4}	V_{SS}—1.5	—	V_{SS}+0.3	V	
Row input low write voltage	V_{IL4}	V_{SS}—26	—	V_{SS}—22	V	
Data in high voltage	V_{IH5}	V_{SS}—1.5	—	V_{SS}+0.3	V	
Data in low voltage	V_{IL5}	V_{DD}	—	V_{SS}—22	V	

**Typical values are at +25°C and nominal voltages.

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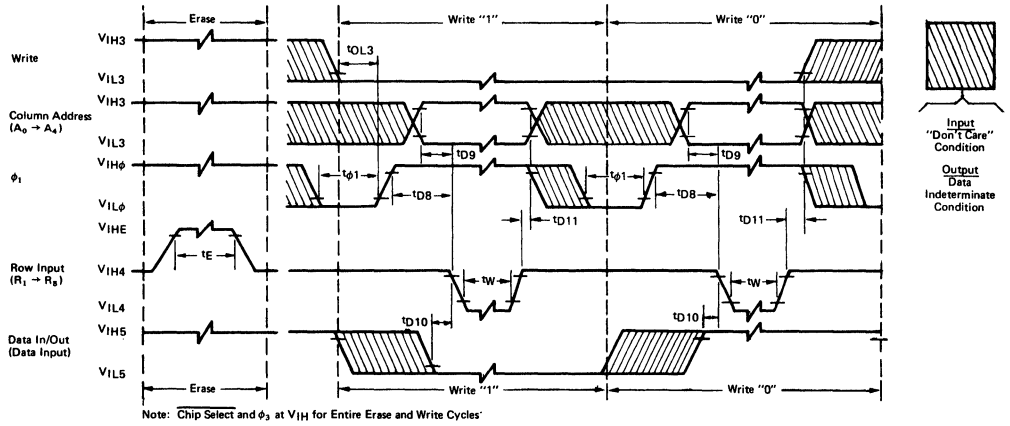
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ**	Max	Units	Conditions
AC CHARACTERISTICS						
Read Cycle						
Access time	t_A	—	—	2.0	μs	R_{LOAD}=6.8K to V_{DD} C_{LOAD}=20pf.
Cycle time	t_C	3.5	—	—	μs	
ϕ_1 pulse width	$t\phi_1$	0.5	—	—	μs	Rise and fall times ≤100 ns
ϕ_3 pulse width	$t\phi_3$	0.5	—	—	μs	Rise and fall times ≤100 ns
Column address change to row input rise delay	t_{D1}	0.7	—	—	μs	
ϕ_1 fall to row input rise delay	t_{D2}	0.0	—	—	μs	
Row input rise to ϕ_3 rise delay	t_{D3}	0.3	—	—	μs	
ϕ_3 rise to data output delay	t_{D4}		—	0.4	μs	R_{LOAD}=6.8K to V_{DD}, C_{LOAD}=20pf.
Row input fall to ϕ_1 rise delay	t_{D5}	0.0	—	—	μs	
ϕ_3 fall to ϕ_1 rise delay	t_{D6}	0.0	—	—	μs	
Row input fall to column address and/or CS change delav	t_{D7}	0.0	—	—	μs	
ϕ1, chip select, and column address overlap	t_{OL1}	0.2	—	—	μs	
ϕ_3 and row input overlap	t_{OL2}	0.2	—	—	μs	
Row input pulse rise time	t_{RR}	0.5	—	—	μs	
Number of read accesses/word subsequent to data being written	N_R	200×10^9	—	—		
Erase Cycle						
Row input erase pulse width	t_E	100	—	—	ms	
Write Cycle						
ϕ_1 pulse width	$t\phi_1$	0.5	—	—	μs	
Row input write pulse width	t_W	5	10	15	ms	
ϕ_1 fall to row input write pulse rise delay	t_{D8}	0.0	—	—	μs	
Column address change to row input write pulse rise delay	t_{D9}	0.7	—	—	μs	
Data input change to row input write pulse rise delay	t_{D10}	0.0	—	—	μs	
Row input write pulse fall to ϕ_1 rise delay	t_{D11}	0.0	—	—	μs	
ϕ_1 and write input overlap	t_{OL3}	0.2	—	—	μs	
Number of times word may be rewritten	N_W	—	—	1×10^6		
Capacitance						
Row input capacitance	C_R	32	37	42	pf	V_{IN}=V_{SS} Volts f=1 MHz All other pins grounded (V_{SS})
Column address capacitance	C_C	—	5	7	pf	
Write input capacitance	C_W	—	3	7	pf	
ϕ_1 capacitance	$C\phi_1$	—	3	7	pf	
ϕ_3 capacitance	$C\phi_3$	—	2	7	pf	
Data In/Out capacitance	C_D	—	4	7	pf	
Chip Select capacitance	C_S	—	5	7	pf	

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS



Note: $\overline{\text{Chip Select}}$ and ϕ_3 at V_{IH} for Entire Erase and Write Cycles.

Fig.1 ERASE AND WRITE CYCLE

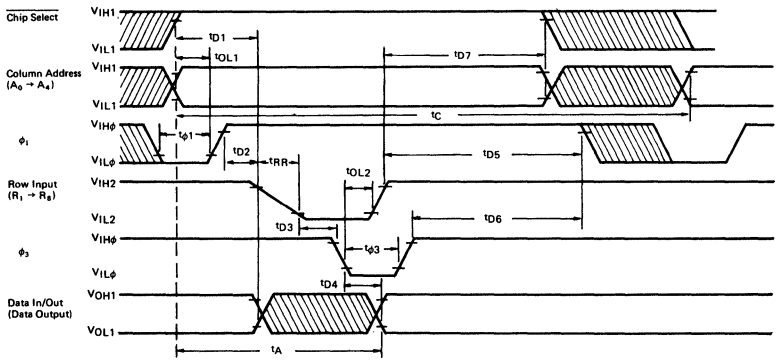


Fig.2 READ CYCLE

12

APPLICATION EXAMPLE:
Figure 4 illustrates a 1024-word by 4-bit memory implementation employing four 1105 EAROM's in a wire-OR'd configuration. Each row input is driven by individual external row driver circuits, shown in figure 5. Erase voltage and write voltage, required as inputs to the row driver circuits, are generated by the circuits shown and need be implemented only once per system (as indicated in figure 4) unless selective erasure by row is desired.

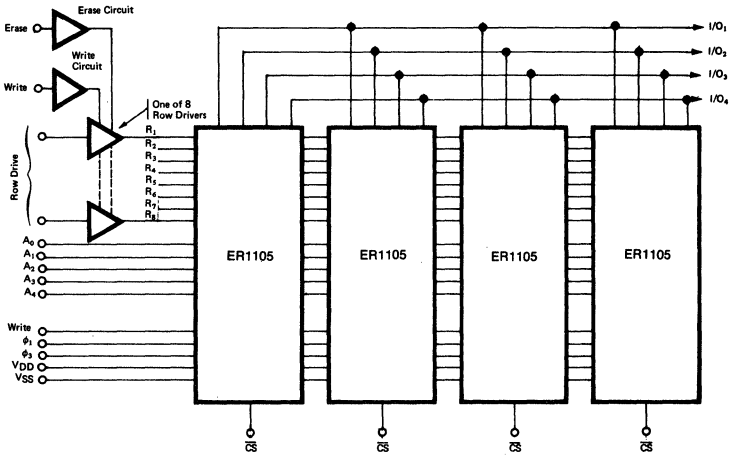


Fig.4 1024 WORD X 4 BIT MEMORY

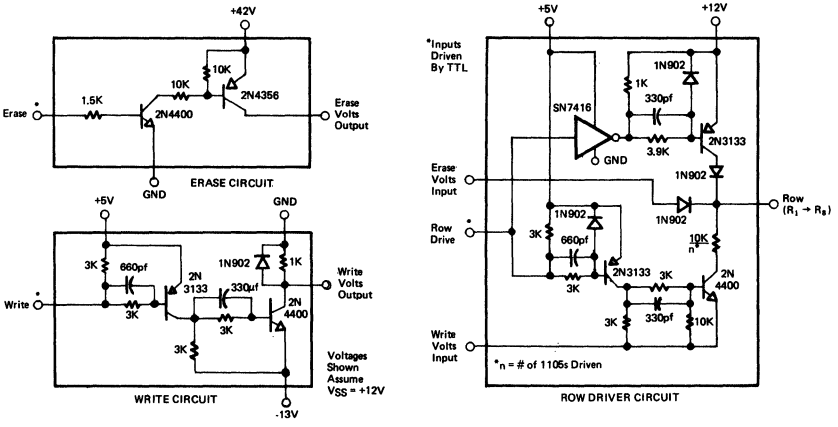


Fig.5 SUGGESTED ROW, ERASE AND WRITE CIRCUITS

1400 Bit Electrically Alterable Read Only Memory

FEATURES

- 100 Word x 14 bit organization
- Word alterable
- 10 years unpowered data storage
- Write/Erase time 100ms/word
- Single -35 volt supply
- No voltage switching required
- MOS compatible signal levels

DESCRIPTION

The ER1400 is a serial input/output 1400 bit electrically erasable and reprogrammable ROM, organized as 100 words of 14 bits each. Data and address are communicated in serial form via a one-pin bidirectional bus.

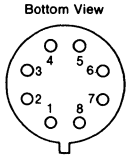
Addressing is by two consecutive one-of-ten codes.

Mode selection is by a 3 bit code applied to C1, C2 and C3.

Data is stored by internal negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 1400 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

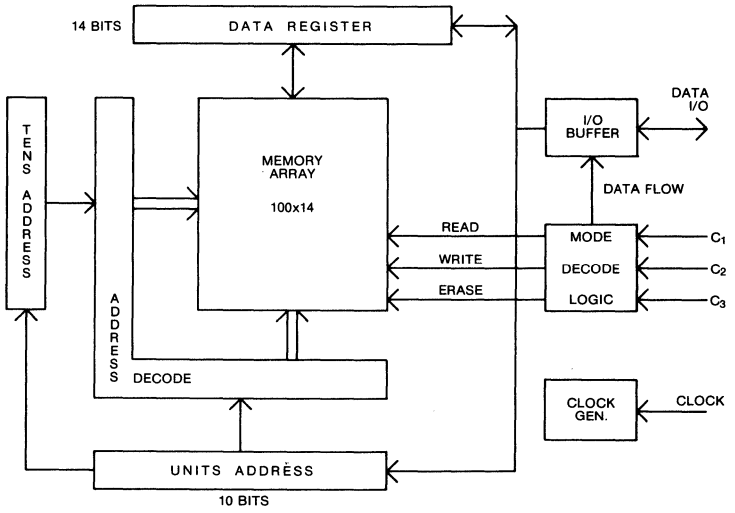
PIN CONFIGURATION

8 LEAD TO-8



1. Data I/O
2. V_M
3. V_{SS}
4. V_{GG}
5. Clock
6. C1
7. C2
8. C3

BLOCK DIAGRAM



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PIN FUNCTIONS

Pin No.	Name	Function
1	Data	In the Accept Address and Accept Data modes, this pin is an input pin for address and data respectively. In the Shift Data Out mode this pin is an output pin designed to drive MOS. In Standby, Read, Erase and Write, this pin is left floating.
2	V_M	Used for testing purposes only. Should be left unconnected for normal operation.
3	V_{SS}	Chip substrate. Normally connected to ground.
4	V_{GG}	DC supply. Normally connected to -35 volt supply.
5	Clock	14KHZ timing reference.
6,7,8	C1, C2, C3	Mode control pins. Their operation is as follows:

C1	C2	C3	Function
0	0	0	Standby - contents of Address and Data Register remains unchanged. Output buffer is left floating.
0	1	1	Accept Address - Data presented at the I/O pin is shifted into the Address Register with each clock pulse.
1	0	0	Read - The address word is read from memory into the data register.
1	0	1	Shift Data Out - The output driver is enabled and the contents of the Data Register are shifted out one bit with each clock pulse.
0	1	0	Erase - The word stored at the addressed location is erased to all zeros.
1	1	1	Accept Data - The data register accepts serial data presented at the I/O pin. The Address Register remains unchanged.
1	1	0	Write - The word contained in the Data Register is written into the location designated by the Address Register.
0	0	1	Not Used

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs
(except V_{GG}) with respect to V_{SS} ..... -20V to +0.3V
V_{GG} with respect to V_{SS} ..... -40V
Storage temperature (No Data Retention) ..... -65°C to +150°C
Storage temperature (with Data Retention)
Operating ..... -25° to +75°C
Unpowered ..... -65°C to +80°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = GND
V_{GG} = -35V
Operating Temperature (T_A) = 0°C to +70°C

Characteristics	Symbol	Min	Typ**	Max	Units
DC CHARACTERISTIC					
Input logic "1"	VIL	V_{SS}-15.0	—	V_{SS}-8	Volts
Input logic "0"	VIH	V_{SS}-1.0	—	V_{SS}+0.3	Volts
Output logic "1" (1 meg, 100 pf load)	VOL	—	—	V_{SS}-12.0	Volts
Output logic "0"	VOH	V_{SS}-1.0	—	V_{SS}+0.3	Volts
Power		—	—	300	mW
AC CHARACTERISTIC					
Clock Frequency	fϕ	11.2	14.0	16.8	KHz
Write time	tw	16.0	20.0	24.0	ms
Erase	te	16.0	20.0	24.0	ms
Rise, fall time	tr, tf	—	—	1.0	μs
Propagation delay	tpw	—	—	20.0	μs

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS

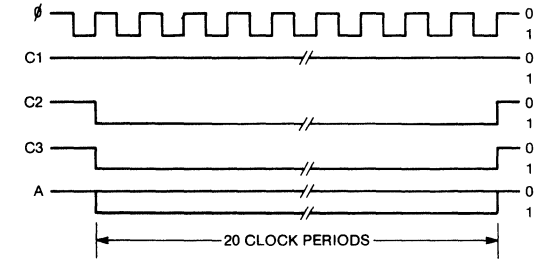

Fig.1 ACCEPT ADDRESS

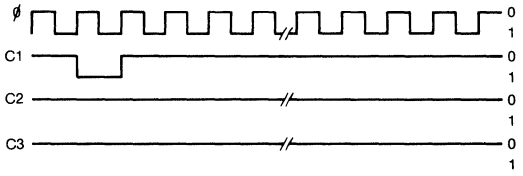

Fig.2 READ

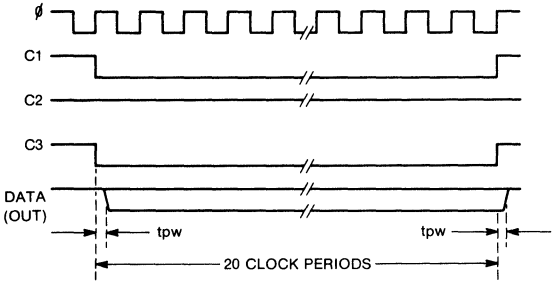

Fig.3 SHIFT DATA OUT

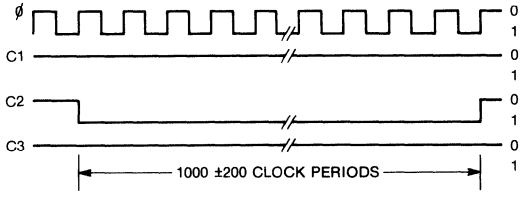

Fig.4 ERASE

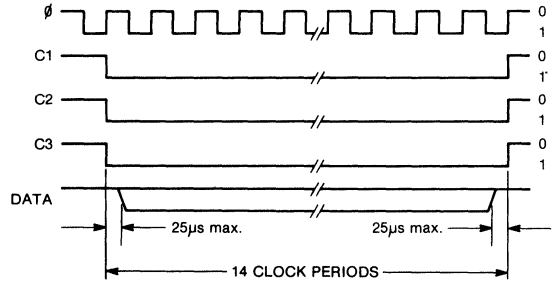

Fig.5 ACCEPT DATA

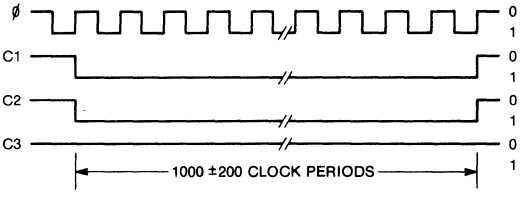

Fig.6 WRITE

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512 Bit Electrically Alterable Read Only Memory

FEATURES

- 32x16 Organization
- 5-Bit Addressing
- TTL Compatible
- Chip Select
- Word Alterable
- 10 Year Unpowered Data Storage
- 6 Microseconds Typical Access Time
- Write/Erase Time 100ms/word
- +5, -28V Supplies
- No Voltage Switching Required

DESCRIPTION

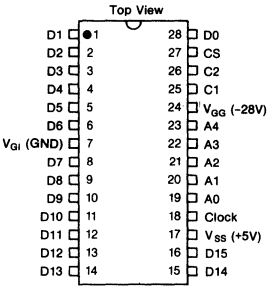
The ER2050 is a fully decoded 32 x 16 electrically erasable and reprogrammable ROM. Write, erase, and read voltages are switched internally via a 2-bit code applied to C1 and C2.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface at the gate insulator of the 512 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

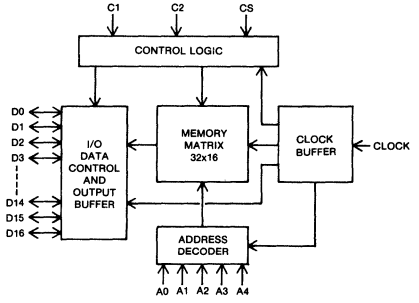
Two TTL compatible control pins switch voltages internally for write, read and erase control.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



BLOCK DIAGRAM



PIN FUNCTIONS

A_0-A_4	5-Bit Word Address
D_0-D_{15}	Data input and output pins
CS	Chip Select. Chip selected at logic 1. When chip select is at logic "0", outputs are open circuit, read, write and erase are disabled. Power is reduced.
C1, C2	Mode Control Inputs C1 C2 1 1 Hold Mode: output data from previous read operation stored at output pins. 0 1 Erase Mode: stored data is erased at addressed location. 1 0 Read Mode: addressed data read after clock pulse. Output data retained at output pins until next read operation. 0 0 Write Mode: input data written at addressed location. Clock not required. Note: Care must be exercised to ensure that CS is held at logic "0" during power up or power down to protect all addresses from spurious write or erase inputs.
CLK	Clock Input. Pulse to logic "1" for read operation.
V_{SS}	Substrate supply. Normally at +5 volts.
V_{GI}	Ground Input
V_{GG}	Power Supply Input. Normally at -28 volts.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs (with respect to V_{SS}) ..... -35V to +0.3V
Storage temperature ..... -65°C to +150°C
Soldering temperature of leads (10 seconds) ..... +300°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = +5V±5%
V_{GG} = -28V±5%
V_{GI} = GND
Operating Temperature (T_A) = 0°C to +70C

Characteristic	Symbol	Min	Typ**	Max	Units
DC CHARACTERISTICS					
Input Logic "1"	V_{IH}	V_{SS}-1.5	—	V_{SS} +0.3	Volts
Input Logic "0"	V_{IL}	-10.0	—	+0.8	Volts
Output Logic "1"	V_{OH}	V_{SS}-1.5	—	—	Volts
Output Logic "0" (I_{OL} = 1.5mA)	V_{OL}	—	—	+0.8	Volts
Power Supply Current					
Read	I_{GG}	—	-7.0	-8.5	mA
Write	I_{GG}	—	-6.0	-7.5	mA
Erase	I_{GG}	—	-4.0	-5.5	mA
AC CHARACTERISTICS					
Access Time	t_{acc}	—	6.0	10.0	µsec
Clock Width	t_{pw}	750	—	—	nsec
Write Time	t_w	100	—	—	msec
Erase Time	t_e	100	—	—	msec
Address-Clock Time	t_{cc}	100	—	—	nsec
Write/Erase-Address Time	t_{ce}	1	—	—	µsec
Address-Write/Erase Time	t_{aw}	50	—	—	nsec
Clock Period	t_c	10.0	—	—	µsec
Number of read accesses/ word between refresh	N_{RA}	10^{11}	—	—	—
Number of times word may be rewritten	N_w	—	—	10^6	—

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS

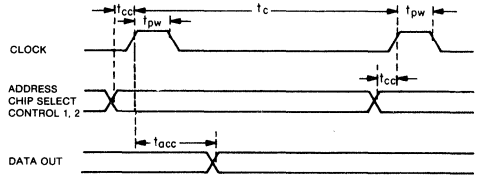


Fig. 1 READ TIMING

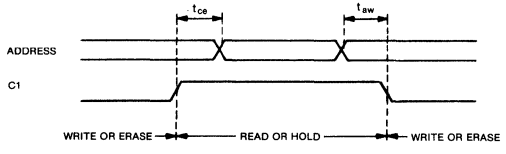


Fig. 2 WRITE/ERASE TO READ/HOLD TIMING

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4096 Bit Electrically Alterable Read Only Memory

FEATURES

- 1024 x 4 Organization
- 10-Bit Binary Addressing
- 2 Chip Select Inputs
- Electrically Reprogrammable
- 2 μs Access Time
- 20 ms/4-bit Word Write Time
- 100 ms Simultaneous Erasure of All Data
- Minimum Data Retention—2 x 10^{11} Read Accesses/Word Between Refresh
- Three-State Outputs
- Unpowered, Nonvolatile Data Storage—10 Years at +70°C
- Control, Address and Data Inputs TTL Compatible with Pull-Up Resistors

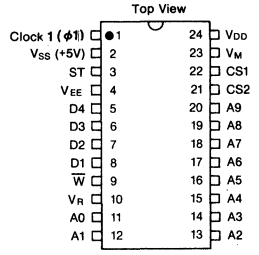
DESCRIPTION

The ER2401 is a fully decoded, 1024 x 4-bit electrically erasable and reprogrammable ROM utilizing second-generation MNOS epitaxial processing technology.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface at the gate insulator of the 4096 MNOS memory transistors. When the writing voltage is removed, the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

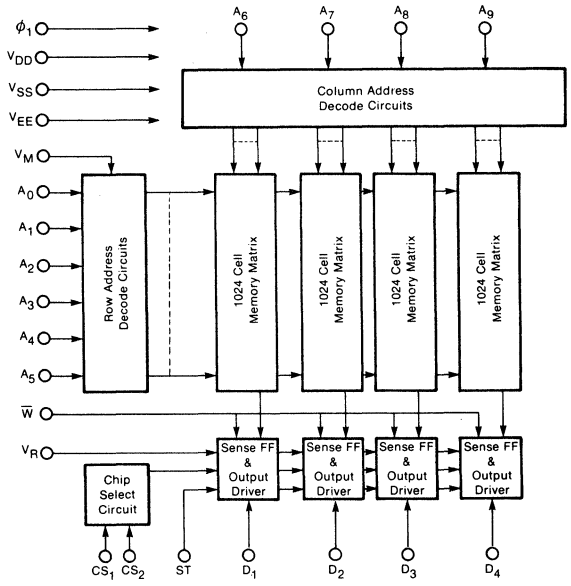
PIN CONFIGURATION

24 LEAD DUAL IN LINE



Stored data may be accessed a minimum of 2 x 10^{11} times without refresh and is non-volatile in the unpowered state in excess of ten years. Data is erased by applying a −28V pulse to the erase substrate of the device. Data can be erased and rewritten up to a maximum of 10^6 times.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs or outputs relative to V_{SS} . . . . . +0.3V to -30V
Operating ambient temperature . . . . . 0°C to +70°C
Storage temperature . . . . . -65°C to +150°C
Soldering temperature of leads (10 seconds) . . . . . +300°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

RECOMMENDED OPERATING CONDITIONS, T_A = 0°C to +70°C

Symbol	Parameter	Erase Mode			Write Mode			Read Mode			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{DD}	Supply Voltage	4.75	V_{SS}	V_{SS}+0.3	V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-20	V_{SS}-19	V_{SS}-18	V
V_{SS}	Substrate supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_M	Memory voltage	—	V_{SS}	—	V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-10.5	V_{SS}-10	V_{SS}-9.5	V
V_R	Reference voltage	—	V_{SS}	—	V_{SS}	V_{SS}	V_{SS}	V_{SS}-20	V_{SS}-19	V_{SS}-18	V
V_{EEH}	Erase substrate input high	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V
V_{EEL}	Erase substrate input low	V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V
V_{WH}	Write control input high	V_{SS}-29	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_{WL}	Write control input low	V_{SS}-29	—	V_{SS}-4.4	V_{SS}-29	—	V_{SS}-4.4	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
$V\phi_H$	ϕ_1 input high voltage	—	V_{SS}	—	V_{SS}-0.8	V_{SS}	V_{SS}+0.3	V_{SS}-0.8	V_{SS}	V_{SS}+0.3	V
$V\phi_L$	ϕ_1 input low voltage	Not Applicable			V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-25	V_{SS}-19	V_{SS}-18	V
V_{STH}	Strobe input high voltage	—	V_{SS}	—	Not Applicable			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_{STL}	Strobe input low voltage	Not Applicable			V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-25	V_{SS}-19	V_{SS}-18	V
V_{IH}	Address and CS input high	Don't Care			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_{IL}	Address and CS input low	Don't Care			V_{DD}	—	V_{SS}-4.4	V_{DD}	—	V_{SS}-4.4	V
V_{DH}	Data input high voltage	Don't Care			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	Not Applicable			V
V_{DL}	Data input low voltage	Don't Care			V_{DD}	—	V_{SS}-4.4	Not Applicable			V

STATIC ELECTRICAL CHARACTERISTICS, T_A = 0°C to +70°C (NO EXTERNAL LOADS EXCEPT AS NOTED)

Symbol	Parameter	Conditions All Pins at V_{SS} Unless Noted	Min	Typ	Max	Unit
I_{IN}	Input leakage current (except pins 1, 2, 4, 5, 6, 7, 8, and 24) at V_{SS}-15V	$\phi 1=V_{DD}=V_{SS}$-20	—	—	-2.0	μA
$I\phi_1$	ϕ_1 leakage current at V_{SS}-29V	$V_{DD}=V_{SS}$-29, ST=W=V_{SS}-25	—	—	-200	μA
I_O	Output leakage current at V_{SS}-15V	Chip deselected	—	—	-10.0	μA
I_{EEL}	Erase substrate leakage current at V_{SS}-28V	W=ST=V_{SS}-25	—	—	-200	μA
I_{DD1}	V_{DD} supply current - read mode at V_{SS}-19V	Outputs open (See Figure 6)	—	8.5	12	mA
I_{DD2}	V_{DD} supply current - write mode at V_{SS}-28V	Outputs open (See Figure 5)	—	18	25	mA
I_{OH}	Data output high current - TTL load	One Series 7400 TTL load with R_S=2KΩ, $V_{CC}=V_{SS}$	-2.0	—	—	mA
I_{OL}	Data output low current - TTL load	(See TTL Notes)	+3.2	—	—	mA
V_{OH}	Data Output high voltage - MOS		V_{SS}-1.5	—	—	V
V_{OL}	Data Output low voltage — MOS	C_L=100 pF	—	—	V_{SS}-10	V
T_S	Unpowered nonvolatile data storage	Typical write conditions	10	—	—	Years

CAPACITANCE AT V_{IN} = V_{SS}, ALL OTHER PINS GROUNDED (V_{SS}), f=1 MHz

Symbol	Parameter	Min	Typ	Max	Unit
C_I	Address and chip select input capacitance	—	5	7	pf
C_W	Write control input capacitance	—	10	20	pf
C_{ST}	Strobe input capacitance	—	10	15	pf
$C\phi_1$	ϕ_1 Input Capacitance	—	40	50	pf
C_{EE}	Erase substrate capacitance	—	600	700	pf
C_D	Data input/output capacitance	—	6	10	pf

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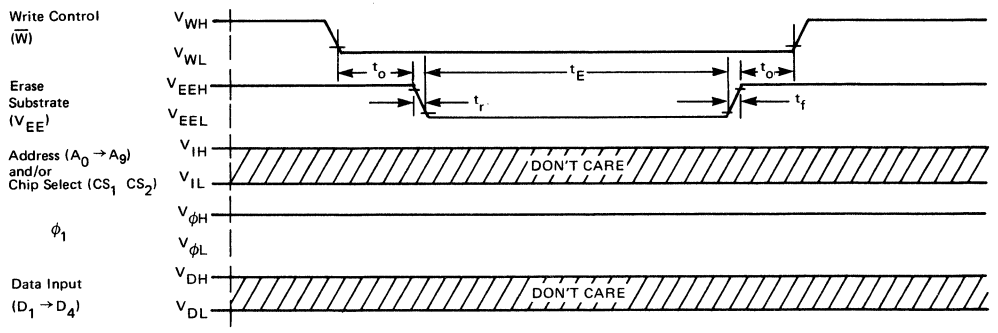
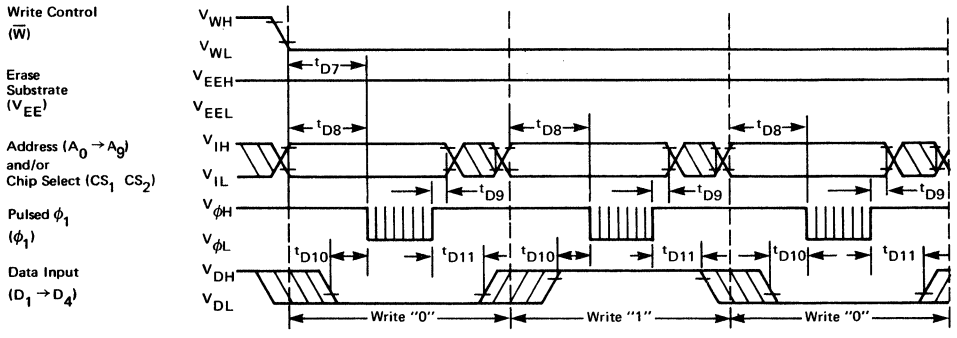
ERASE CYCLE CHARACTERISTICS, T_A = 0°C to +70°C

Symbol	Parameter	Min	Typ	Max	Units
t_E	V_{EE} erase pulse width	100	—	1000	ms
t_r, t_f	V_{EE} rise time, V_{EE} fall time	0.01	—	1.0	ms
t_o	Write-erase overlap	10	—	—	μs



WRITE CYCLE CHARACTERISTICS, T_A=0°C to +70°C ($ST=V_{DD}$) (SEE NOTE 3)

Symbol	Parameter	Min	Typ	Max	Units
$N_{\phi W}$	Number of ϕ_1 write pulses at 100 μs ±10%, 5 μs min. dead time between pulses)	100	200	300	Pulses
t_{D7}	Write control rise to pulsed ϕ_1 rise delay	500	—	—	ns
t_{D8}	Address change and chip select fall to pulsed ϕ_1 rise delay	500	—	—	ns
t_{D9}	Pulsed ϕ_1 fall to address and chip select change delay	0.0	—	—	μs
t_{D10}	Data input change to pulsed ϕ_1 rise delay	0.0	—	—	μs
t_{D11}	Pulsed ϕ_1 fall to data input change delay	0.0	—	—	μs
N_W	Number of times word may be rewritten	—	—	10^6	—

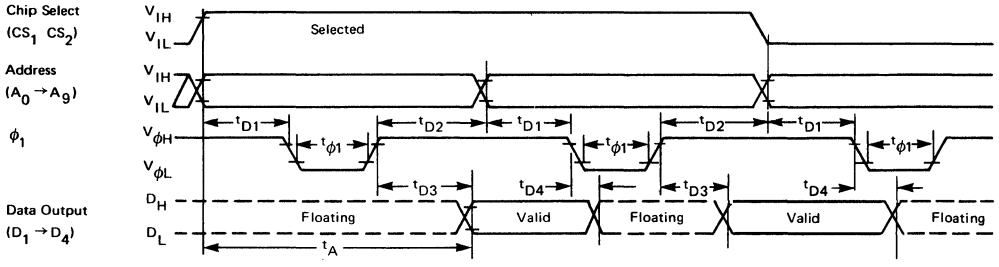


NOTES:

1. Due to the dynamic nature of the circuit a "ϕ_1 NOT" time in excess of 40 μsec. may result in a floated output condition. Consequently data must be resampled with a 40 μsec. time period following the fall of ϕ_1 to ensure its validity.
2. Several seconds may be required following a programming operation for the circuit to become operable in the read mode. If data is to be verified immediately following programming, a forward current of +1 mA ±10% may be forced into the erase substrate junction (Pin 4, V_{EE}), for a period not to exceed 10 milliseconds, to quickly dissipate charge trapped at internal circuit nodes.
3. Maximum power dissipation occurs during programming. When programming multichip systems where the application of programming voltages is required for several minutes, forced air cooling is recommended to reduce package temperature. Power is not reduced when chip is deselected.
4. All typical values are at +25° C and nominal voltages.

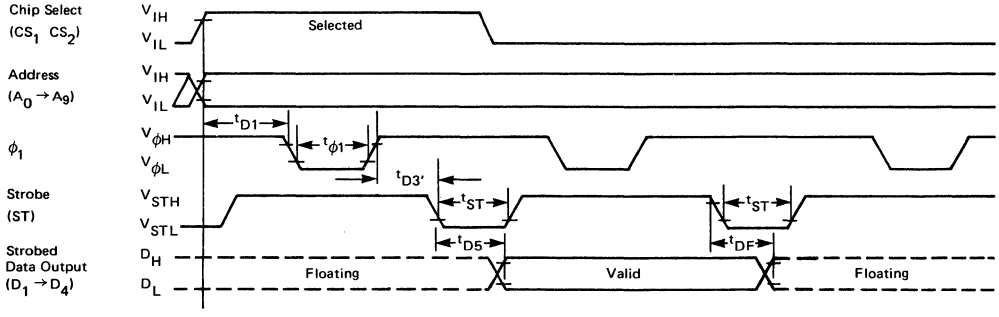
READ CYCLE CHARACTERISTICS FOR NON-STROBED OPERATION, T_A= 0°C to +70°C (ST = V_{DD})

Symbol	Parameter (See Figures 1 through 4)	Min	Typ	Max	Units
T_A	Access time (strobe=V_{DD})	—	—	2.0	μs
$t_{\phi 1}$	Pulse width (rise and fall times ≤50 ns) (See Note 1)	850	—	2000	ns
t_{D1}	Address and chip select change to ϕ_1 rise delay	400	—	—	ns
t_{D2}	ϕ_1 Fall to address and chip select change delay	0.0	—	—	μs
t_{D3}	ϕ_1 Fall to data output valid delay (See Notes 1 and 2)	—	—	750	ns
t_{D4}	ϕ_1 Rise to floated output delay	—	—	300	ns
N_{RA}	Number of read accesses/word between refresh	2×10^{11}	—	—	—



READ CYCLE CHARACTERISTICS FOR STROBED OPERATION, T_A=0°C to +70°C

Symbol	Parameter (See Figure 1 through 4)	Min	Typ	Max	Units
$t_{\phi 1}$	ϕ_1 Pulse width (rise and fall times ≤50 ns) (See Note 1)	850	—	2000	ns
t_{D1}	Address and chip select change to ϕ_1 rise delay	400	—	—	ns
t_{D3}	ϕ_1 Fall to strobe rise delay	0.75	—	—	μs
t_{ST}	Strobe pulse width (rise and fall ≤50 ns)	500	—	—	ns
t_{D5}	Strobe rise to strobed data output valid delay (see notes 1 and 2)	—	—	500	ns
t_{DF}	Strobe rise to strobed floated output on deselect delay	—	—	300	ns
N_{RA}	Number of read accesses/word between refresh	2×10^{11}	—	—	—



TYPICAL OPERATING CHARACTERISTICS, T_A = +25°C and +70°C, R_S = 2K Ohms, V_{SS} = OV

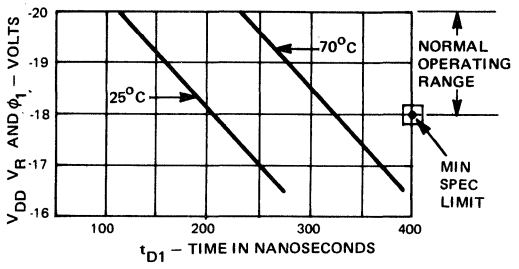


Fig.1 TYPICAL ϕ1 DELAY IN NANOSECONDS VS. POWER SUPPLY VOLTAGE

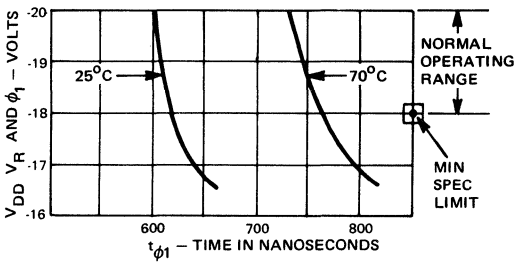


Fig.2 TYPICAL ϕ1 WIDTH IN NANOSECONDS VS. POWER SUPPLY VOLTAGES

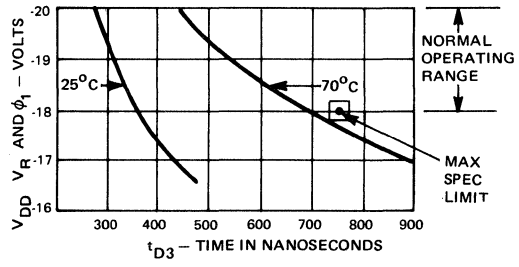


Fig.3 TYPICAL DATA SETUP TIME IN NANOSECONDS VS. POWER SUPPLY VOLTAGES

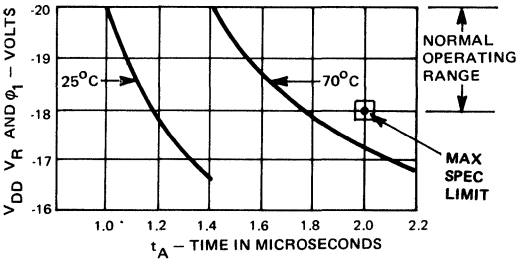


Fig.4 TYPICAL ACCESS TIME IN MICROSECONDS VS. POWER SUPPLY VOLTAGES

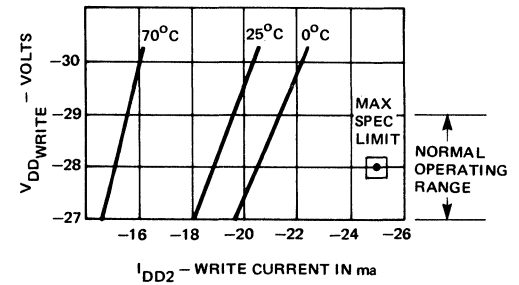


Fig.5 TYPICAL WRITE CURRENT IN MILLIAMPS VS. POWER SUPPLY VOLTAGES

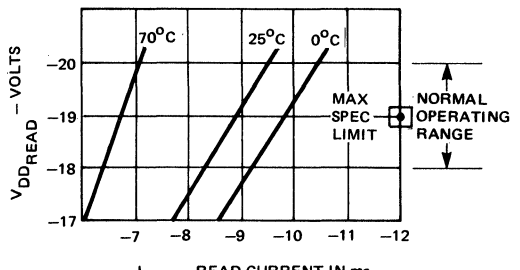


Fig.6 TYPICAL READ CURRENT IN MILLIAMPS VS. POWER SUPPLY VOLTAGE

PIN FUNCTIONS

Chip Select (CS1, CS2)
Both must be in the high state to enable the data output terminals or write data into the device.

Data Input/Output (D1—D4)
D1 through D4 are bidirectional data terminals. Data are entered on these terminals during the write cycle and read out during the read cycle. When deselected, these terminals are in a floating condition.

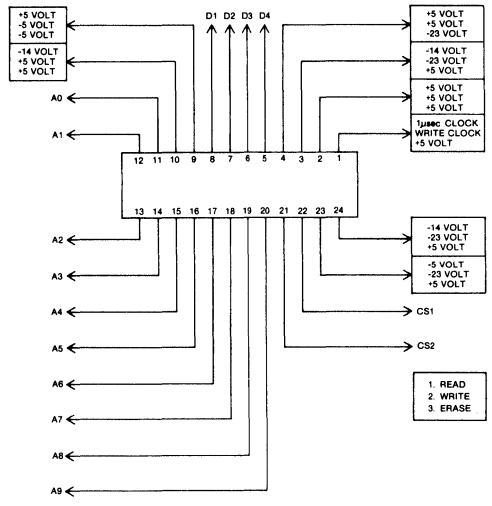
Write Control ($\overline{W}$)
The write control terminal must be in the low state in order to write data into the device.

Strobe (ST)
A strobe input is provided for delayed data clockout. In applications where this feature is not desired, the strobe terminal should be maintained at VDD throughout the entire read cyle. The ST input is high-level and not TTL-compatible.

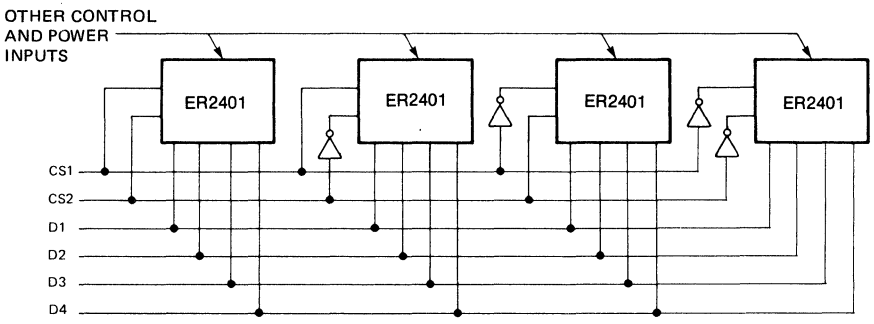
Phase One (ϕ1)
During the write operation, multiple 100μs pulses must be applied to the ϕ1 terminal to fully shift the memory transistor threshold voltge to its most negative state. This is required for voltage bootstrapping in the row-selection circuitry. The ϕ1 input is high level and not TTL-compatible.

NOTE: All control, address and data inputs are TTL-compatible with pull-up resistors.

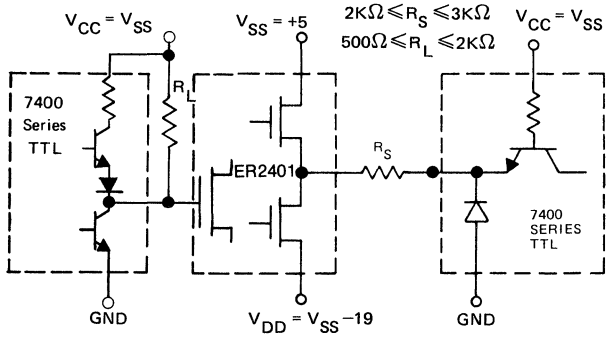
ER2401 OPERATION



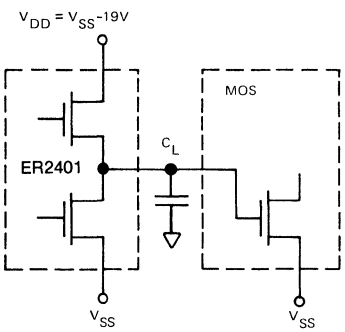
A 4096 x 4 EAROM SUBSYSTEM ORGANIZATION



TTL INTERFACE



MOS INTERFACE



12

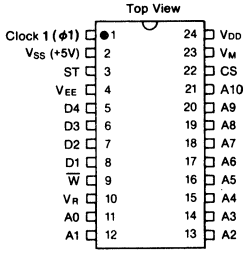
8192 Bit Electrically Alterable Read Only Memory

FEATURES

- 2048 x 4 Organization
- 11-Bit Binary Addressing
- Chip Select Input
- Electrically Reprogrammable
- 2 μs Access Time
- 20 ms/4-bit Word Write Time
- 100 ms Simultaneous Erasure of All Data
- Minimum Data Retention—2 x 10^{11} Read Accesses/Word Between Refresh
- Three-State Outputs
- Unpowered, Nonvolatile Data Storage—10 Years at +70°C
- Control, Address and Data Inputs TTL Compatible with Pull-Up Resistors

PIN CONFIGURATION

24 LEAD DUAL IN LINE



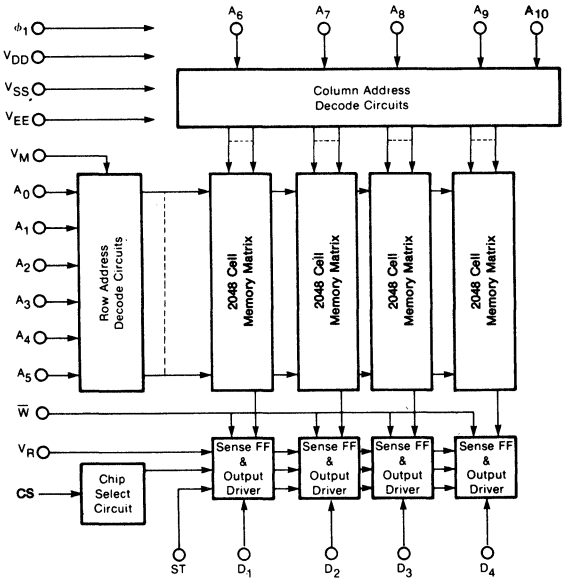
DESCRIPTION

The ER2800 is a fully decoded, 1024 x 4-bit electrically erasable and reprogrammable ROM utilizing second-generation MNOS epitaxial processing technology.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface at the gate insulator of the 8192 MNOS memory transistors. When the writing voltage is removed, the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

Stored data may be accessed a minimum of 2 x 10^{11} times without refresh and is non-volatile in the unpowered state in excess of ten years. Data is erased by applying a −28V pulse to the erase substrate of the device. Data can be erased and rewritten up to a maximum of 10^6 times.

BLOCK DIAGRAM



4096 Bit High Speed Electrically Alterable Read Only Memory

FEATURES

- 1024 x 4 Organization
- 10-Bit Addressing
- TTL Compatible
- Chip Select
- Word Alterable
- 10 Year Unpowered Data Storage
- 600ns Typical Access Time
- Write Time — 100μs/word
  Erase Time — 1ms/word
- +5, -12 volt supply for read
- -30 volt supply for write/erase
- No Voltage Switching Required
- 22 Pin Package

DESCRIPTION

The ER3400 is a fully decoded 1024 x 4 electrically erasable and reprogrammable ROM. Write, erase, and read voltages are switched internally via a 2-bit code applied to C1 and C2.

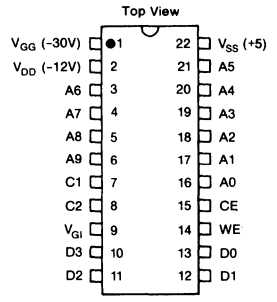
Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface at the gate insulator of the 4096 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

+5 volt and -12 volt supplies are required for read operation. An additional -30 volt supply is required for write and erase.

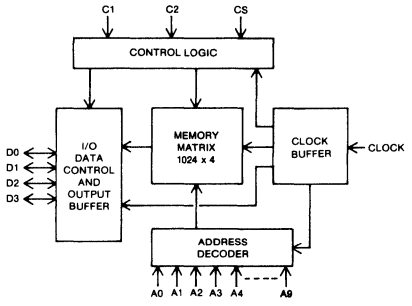
Two TTL compatible control pins switch voltages internally for write, read and erase control.

PIN CONFIGURATION

22 LEAD DUAL IN LINE



BLOCK DIAGRAM



PIN FUNCTIONS

A_0-A_4	5-Bit Word Address
D_0-D_{15}	Data input and output pins
$\overline{CS}$	Chip Select. Chip selected at logic 0. When chip select is at logic "1", outputs are open circuit, read, write and erase are disabled. Power is reduced.
C1, C2	Mode Control Inputs $\overline{C1}$ $\overline{C2}$ 1 1 Block Erase Mode: erase operation performed on all words. 0 1 Word Erase Mode: stored data is erased at addressed location. 1 0 Read Mode: addressed data read after clock pulse. Output data retained at output pins until next read operation. 0 0 Write Mode: input data written at addressed location. Clock not required. Note: Care must be exercised to ensure that CS is held at logic "0" during power up or power down to protect all addresses from spurious write or erase inputs.
V_{SS}	Substrate supply. Normally at +5 volts.
V_{GI}	Ground Input
V_{DD}	Power Supply Input. Normally at -12 volts.
V_{GG}	Power Supply Input. Normally at -30 volts.
WE	Write data strobe.

12

GENERAL INSTRUMENT

RO-6-1024/4
RO-7-1024/4
RO-6-1024/8
RO-7-1024/8
RO-5-1302
RO-6-2048/4
RO-7-2048/4
RO-6-2048/8
RO-7-2048/8
RO-3-2560
RO-3-4096
RO-3-5120
RO-5-8192
RO-3-8316A
RO-3-8316B
RO-3-9316A
RO-3-9316B
RO-3-16384
RO-3-20480

1024 Bit Static Read Only Memories

FEATURES

- Static operation. No clock required.
- Access time typically 1 μsec.
- Three-State output for wired AND capability.
- Chip enable control.
- Input, Output directly interface with DTL/TTL.
- Choice of Operating Temperature Ranges—
  RO-7: 0°C to +70 °C
  RO-6: -55°C to +125°C

DESCRIPTION

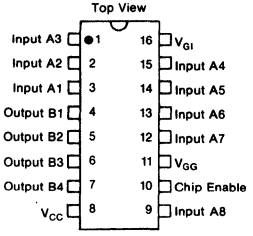
The RO-6-1024/4, RO-7-1024/4, RO-6-1024/8 and RO-7-1024/8 are 1024 bit static Read Only Memories belonging to a standard family of DTL/TTL compatible circuits which are constructed using low threshold silicon nitride passivated P-channel enhancement mode field effect transistors.

The RO-6-1024/4 is packaged in a 16 lead ceramic Dual In Line.The RO-7-1024/4 is the plastic version of this device. The memory organization is 256×4 bit words.

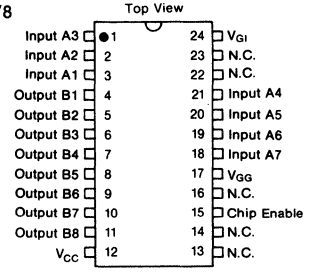
The RO-6-1024/8 is packaged in a 24 lead ceramic Dual In Line.The RO-7-1024/8 is the plastic version of this device. The memory organization is 128×8 bit words.

PIN CONFIGURATIONS

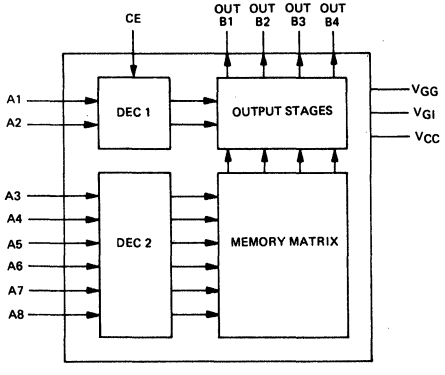
16 LEAD DUAL IN LINE
RO-6/7-1024/4



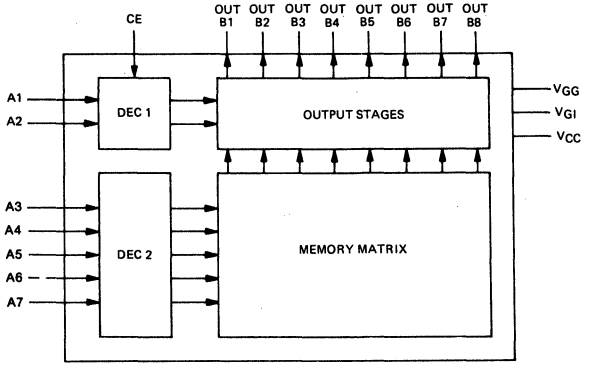
24 LEAD DUAL IN LINE
RO-6/7-1024/8



BLOCK DIAGRAMS



RO-6/7-1024/4



RO-6/7-1024/8

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GI} & V_{GG} (with respect to V_{CC}) . . . . . −20V to +0.3V
Clock & logic inputs (with respect to V_{CC}) . −20V to +0.3V
Storage Temperature. . . . . −55°C to +150°C
Operating Temperature . . . . . −55°C to +125°C (RO-6-1024/4/8)
. . . . . 0°C to +70°C (RO-7-1024/4/8)

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

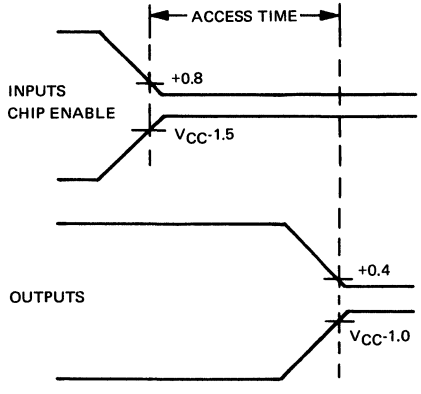
Standard Conditions (unless otherwise noted)

V_{CC} = +5V ± 0.5V
V_{GG} = −12V ± 1V
V_{GI} = GND
(Substrate at V_{CC})
Operating Temperature (T_A) = −55°C to +125°C (RO-6-1024/4/8)
= 0°C to +70°C (RO-7-1024/4/8)

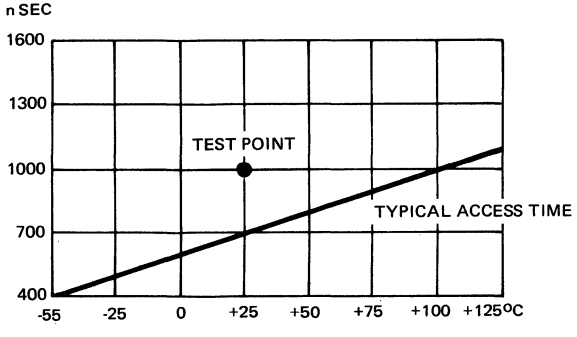
Characteristics	Min.	Typ.**	Max	Units	Conditions
Data Inputs					
Logic "0" level	—	—	+0.8	V	
Logic "1" level	V_{CC}−1.5	—	—	V	
Noise Immunity	0.4	—	—	V	
Input Leakage	—	—	1.0	μA	Measured at $V_{IN} = V_{GG}$ at 25°C
Input capacitance	—	5	—	pF	Measured at $V_{IN} = V_{CC}$
Data Outputs					
Logic "0" level	—	—	+0.4	V	I_{OL} = 1.6 mA
Logic "1" level	V_{CC}−1.0	—	—	V	I_{OH} = 100 μA
Access Time					
Address	—	—	1.0***	μs	Measured at 25°C
Chip enable	—	—	1.0***	μs	Measured at 25°C

**Typical values are at +25°C and nominal voltages
*** Testing Conditions

TIMING DIAGRAM



TYPICAL CHARACTERISTIC CURVE



ACCESS TIME VS. TEMPERATURE

2048 Bit Static Read Only Memory

FEATURES

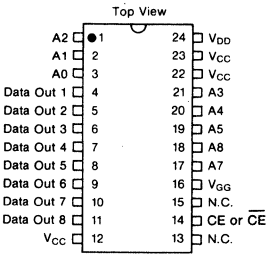
- Static Operation. No clock required.
- Access time typically 1.2 usec.
- Three-state output for wired AND capability.
- Chip enable control.
- Input, Output directly interface with DTL/TTI.

DESCRIPTION

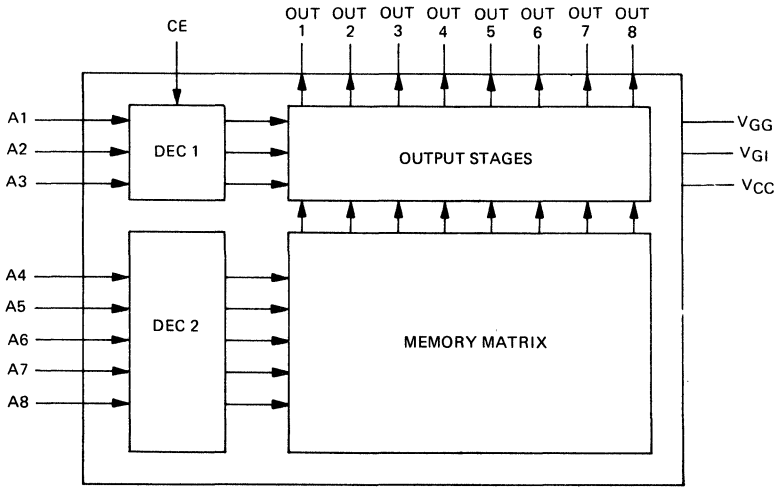
The RO-5-1302 is a 2048 bit fully static Read Only Memory belonging to a standard family of DTL/TTL compatible circuits which are constructed using low threshold silicon nitride passivated P-channel enhancement mode field effect transistors. The RO-5-1302 is packaged in a 24 lead Dual In Line. The memory organization is 256×8 bit words.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GI} & V_{GG} (with respect to V_{CC}) . . . . . −20V to +0.3V
Clock & logic inputs (with respect to V_{CC}) . . . . . −20V to +0.3V
Storage Temperature. . . . . −55°C to +150°C
Operating Temperature. . . . . 0° to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

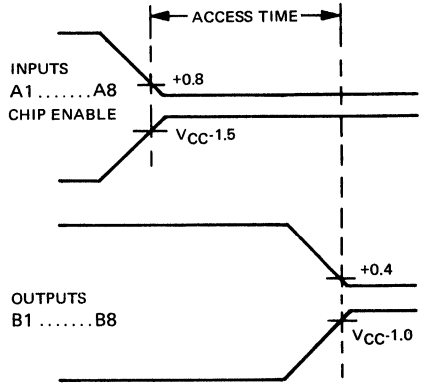
Standard Conditions (unless otherwise noted)

V_{CC} = +5V ± 0.5V
V_{GG} = −12V ± 1V
V_{GI} = GND
(Substrate at V_{CC})
Operating Temperature (T_A) = 0°C to +70°C

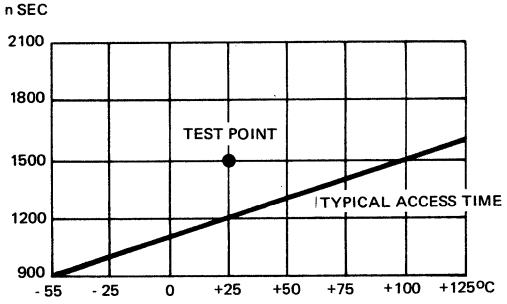
Characteristics	Min	Typ**	Max	Units	Conditions
Data Inputs					
Logic "0" level	—	—	+0.8	V	
Logic "1" level	V_{CC}−1.5	—	—	V	
Noise immunity	0.4	—	—	V	
Input leakage	—	—	1.0	μA	Measured at $V_{IN} = V_{GG}$ at 25°C
Input capacitance	—	5	—	pF	Measured at $V_{IN} = V_{CC}$
Data Outputs					
Logic "0" level	—	—	+0.4	V	I_{OL} = 1.6 mA
Logic "1" level	V_{CC}−1.0	—	—	V	I_{OH} = 100 μA
Access Time					
Address	—	1.2	1.5***	μs	Measured at 25°C
Chip enable	—	0.8	1.5***	μs	Measured at 25°C

**Typical values are at +25°C and nominal voltages
***Testing Conditions

TIMING DIAGRAM



TYPICAL CHARACTERISTIC CURVE



ACCESS TIME VS. TEMPERATURE

13

2048 Bit Static Read Only Memories

FEATURES

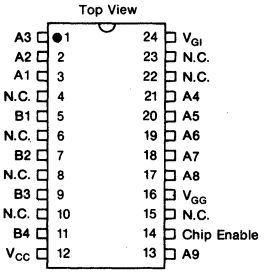
- Static Operation. No clock required.
- Access time typically 1.2 usec.
- Three-state output for wired AND capability.
- Chip enable control.
- Input, Output directly interface with DTL/TLL.
- Choice of Operating Temperature Ranges—
  RO-7: 0°C to +70°C
  RO-6: -55° to +125°C

DESCRIPTION

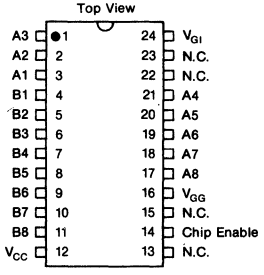
The RO-6-2048/4, RO-7-2048/4, RO-6-2048/8 and RO-7-2048/8 are 2048 bit fully static Read Only Memories belonging to a standard family of DTL/TTL compatible circuits which are constructed using low threshold silicon nitride passivated P-channel enhancement mode field effect ransistors. The RO-6-2048/4 is packaged in a 24 lead ceramic Dual In Line. The RO-7-2048/4 is the plastic version of this device. The memory organization is 512×4 bit words.
The RO-6-2048/8 is packaged in a 24 lead ceramic Dual In Line. The RO-7-2048/8 is the plastic version of this device. The memory organization is 256×8 bit words.

PIN CONFIGURATIONS

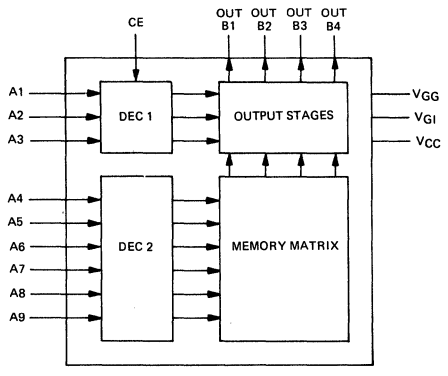
24 LEAD DUAL IN LINE
RO-6/7-2048/4



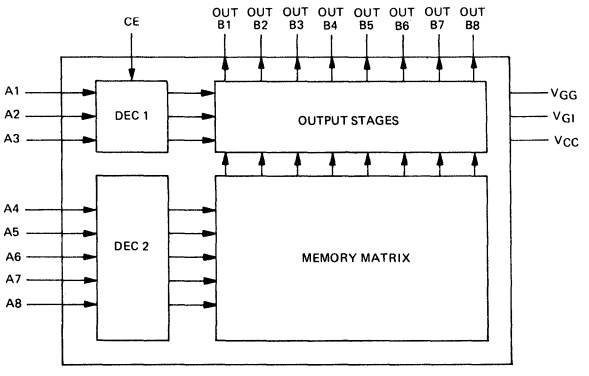
24 LEAD DUAL IN LINE
RO-6/7-2048/8



BLOCK DIAGRAM



RO-6/7-2048/4



RO-6/7-2048/8

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GI} & V_{GG} (with respect to V_{CC}) . . . . . −20V to +0.3V
Clock & logic inputs (with respect to V_{CC}) . −20V to +0.3V
Storage Temperature. . . . . − 55°C to +150°C
Operating Temperature. . . . . −55°C to +125°C (RO-6-2048/4/8)
. . . . . 0°C to +70°C (RO-7-2048/4/8)

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

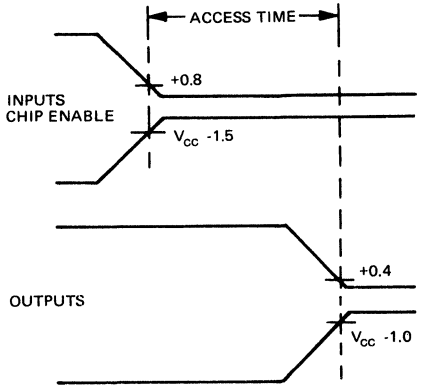
Standard Conditions (unless otherwise noted)

V_{CC} = +5V ± 0.5V
V_{GG} = −12V ± 1V
V_{GI} = GND
(Substrate at V_{CC})
Operating Temperature (T_A) = -55°C to +125°C (RO-6-2048/4/8)
= 0°C to +70°C (RO-7-2048/4/8)

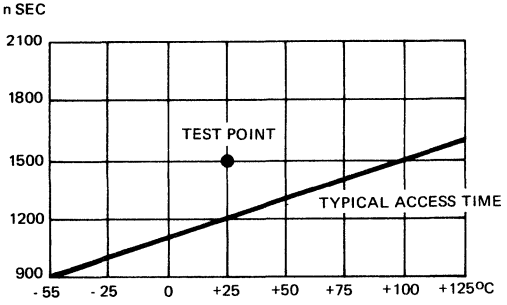
Characteristics	Min	Typ**	Max	Units	Conditions
Data Inputs					
Logic "0" level	—	—	+0.8	V	
Logic "1" level	V_{CC}−1.5	—	—	V	
Noise immunity	0.4	—	—	V	
Input leakage	—	—	1.0	μA	Measured at $V_{IN} = V_{GG}$ at 25°C
Input capacitance	—	5	—	pF	Measured at $V_{IN} = V_{CC}$
Data Outputs					
Logic "0" level	—	—	+0.4	V	I_{OL} = 1.6 mA
Logic "1" level	V_{CC}−1.0	—	—	V	I_{OH} = 100 μA
Access Time					
Address	—	1.2	1.5***	μs	Measured at 25°C
Chip enable	—	0.8	1.5***	μs	Measured at 25°C

**Typical values are at +25°C and nominal voltages
***Testing Conditions

TIMING DIAGRAM



TYPICAL CHARACTERISTIC CURVE



ACCESS TIME VS. TEMPERATURE

2560 Bit Static Read Only Memory

FEATURES

- 512×5 Organization—ideal for many general purpose applications.
- Single +5 Volt Supply.
- TTL Compatible—all inputs and outputs.
- Static Operation—no clocks required.
- 450ns Maximum Access Time
- 175mW Maximum Power
- Three-State Outputs—under the control of an 'Output Inhibit' input to simplify memory expansion.
- Totally Automated Custom Programming.
- Zener Protected Inputs
- Glass Passivation Protection

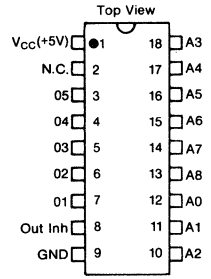
DESCRIPTION

The General Instrument RO-3-2560 is a 2560 bit static Read-Only Memory organized as 512 five bit words and is ideally suited for many general purpose memory applications. Fabricated in GI's advanced GIANT II N-channel Ion-Implant process to enable operation from a single +5 Volt power supply, the RO-3-2560 can store a full 512 words of 5 bits each.

The RO-3-2560 is one of a family of 512 word Read-Only Memories offered by General Instrument; two others are the RO-3-4096, with a 512×8 memory organization, and the RO-3-5120, with a 512×10 memory organization.

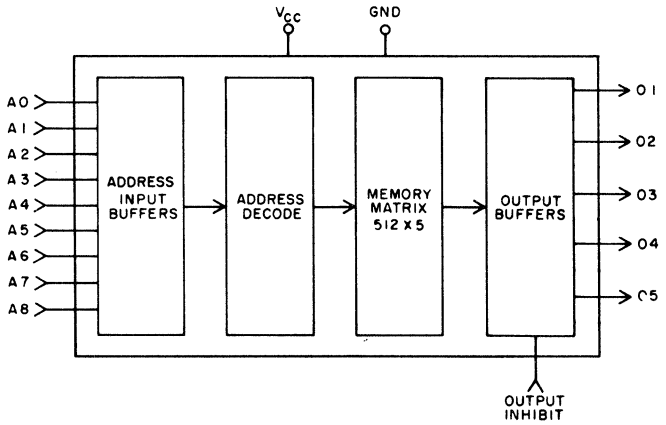
PIN CONFIGURATION

18 LEAD DUAL IN LINE



A separate publication, "RO-3-2560 Custom Coding Information," available from GI Sales Offices, describes the punched card and truth table format for custom programming of the RO-3-2560 memory.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . . . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

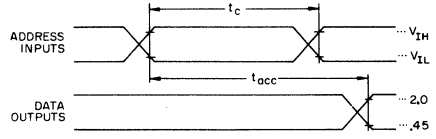
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±5%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL load, $C_{L\ TOTAL}$ = 50pF

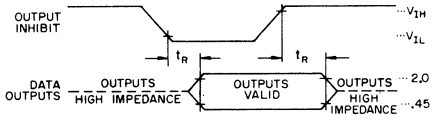
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Output Inhibit Inputs						
Logic "1"	V_{IH}	2.2	—	—	V	
Logic "0"	V_{IL}	—	—	0.65	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.2	—	—	V	I_{OH} = 100μA
Logic "0"	V_{OL}	—	—	0.45	V	I_{OL} = 1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power						
I_{CC}	—	—	25	33	mA	Outputs Open
AC CHARACTERISTICS						
Inputs						
Cycle Time	t_C	400	—	—	ns	
Capacitance	C_I	—	5	8	pF	f = 1MHz
Data Outputs						
Access Time	t_{ACC}	75	250	450	ns	
Inhibit Response Time	t_R	—	150	200	ns	
Capacitance	C_O	—	8	10	pF	f = 1MHz

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS



ACCESS TIME (ADDRESS TO OUTPUT-
OUTPUT INHIBIT AT LOGIC '0')



INHIBIT RESPONSE TIME
(ADDRESS INPUTS STABLE)

13

4096 Bit Static Read Only Memory

FEATURES

- 512×8 Organization
- Single +5 Volt Supply
- TTL/DTL Compatible
- Static Operation—no clocks required
- 500ns. Maximum Access Time
- 150 mW Typical Power
- Tri-State Outputs—under conrol of 'Output Inhibit' signal
- Totally Automated Custom Programming
- Zener Protected Inputs
- Glass Passivation Protection

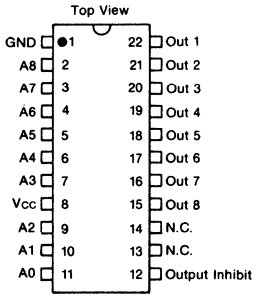
DESCRIPTION

The General Instrument RO-3-4096 is a 4096 bit static Read-Only-Memory. It is organized as 512 eight bit words and requires 9 bits of addressing. An 'Output Inhibit' function is provided to simplify the connection of several ROMs to a common bus. The RO-3-4096 is constructed on a single monolithic chip utilizing low-voltage N-channel Ion Implant technology.

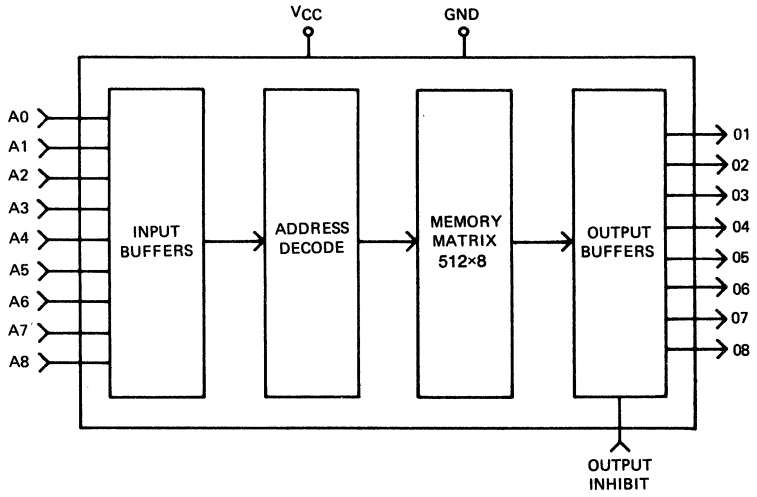
A separate publication, "RO-3-4096 Custom Coding Information," available from GI Sales Offices, describes the punched card and truth table data format for custom programming of the RO-3-4096 memory.

PIN CONFIGURATION

22 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage to this device. Functional operation at these conditions is not implied—operating conditions are specified below.

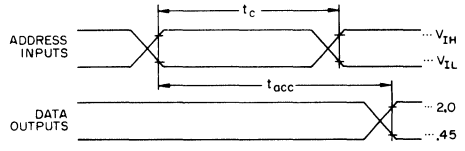
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ± 5%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL load, C_L total = 50 pF.

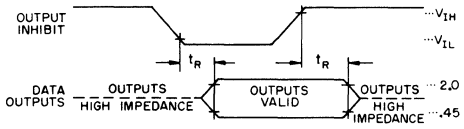
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Output Inhibit Inputs						
Logic "1"	V_{IH}	2.2	—	—	V	
Logic "0"	V_{IL}	—	—	0.65	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.2	—	—	V	I_{OH}=100μA
Logic "0"	V_{OL}	—	—	0.45	V	I_{OL}=1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power						
I_{CC}	—	—	30	45	mA	
AC CHARACTERISTICS						
Inputs						
Cycle Time	t_C	500	—	—	ns	
Capacitance	C_L	—	5	8	pF	f = IMHz
Data Outputs						
Access Time	t_{ACC}	—	350	500	ns	
Inhibit Response Time	t_R	—	—	200	ns	
Capacitance	C_O	—	8	10	pF	f = IMHz

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS



ACCESS TIME (ADDRESS TO OUTPUT-OUTPUT INHIBIT AT LOGIC "0")



INHIBIT RESPONSE TIME (ADDRESS INPUTS STABLE)

13

5120 Bit Static Read Only Memory

FEATURES

- 512×10 Organization
- Single +5 Volt Supply
- TTL/DTL Compatible
- Static Operation—no clocks required
- 500ns Maximum Access Time
- 150mW Typical Power
- Three-State Outputs—under control of 'Output Inhibit' signal
- Totally Automated Custom Programming
- Zener Protected Inputs
- Glass Passivation Protection

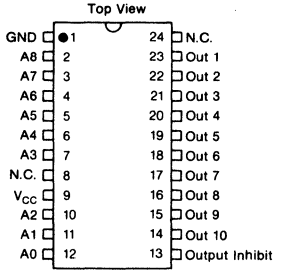
DESCRIPTION

The General Instrument RO-3-5120 is a 5120 bit static Read-Only-Memory. It is organized as 512 ten bit words and requires 9 bits of addressing. An 'Output Inhibit' function is provided to simplify the connection of several ROMs to a common bus. The RO-3-5120 is constructed on a single monolithic chip utilizing low-voltage N-channel Ion Implant technology.

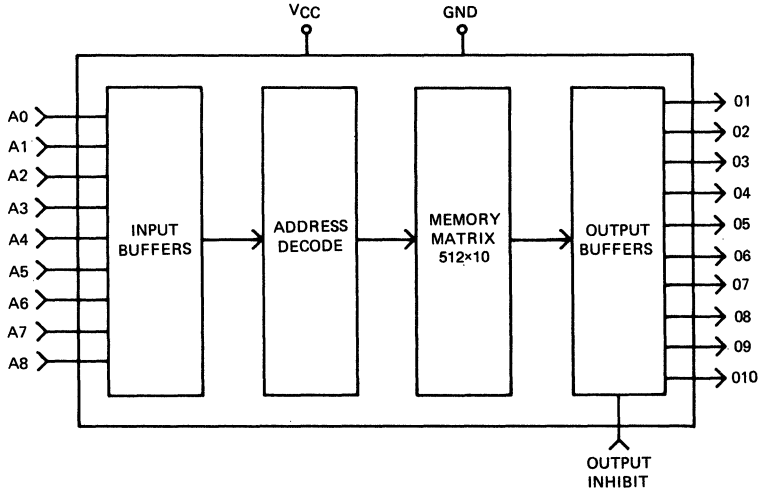
A separate publication, "RO-3-5120 Custom Coding Information," available from GI Sales Offices, describes the punched card and truth table data format for custom programming of the RO-3-5120 memory.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRIC CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . . . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

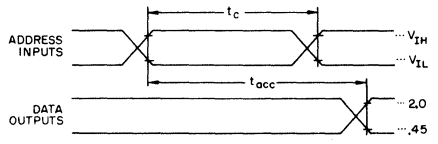
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±5%
Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL Load, $C_{L\ TOTAL}$ = 50pF.

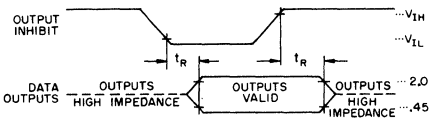
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Output Inhibit Inputs						
Logic "1"	V_{IH}	2.2	—	—	V	
Logic "0"	V_{IL}	—	—	0.65	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.2	—	—	V	I_{OH} = 100μA
Logic "0"	V_{OL}	—	—	0.45	V	I_{OL} = 1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current						
I_{CC}	—	—	30	45	mA	Outputs open
AC CHARACTERISTICS						
Inputs						
Cycle Time	t_C	500	—	—	ns	
Capacitance	C_I	—	5	8	pF	f = 1MHz
Data Outputs						
Access Time	t_{ACC}	—	350	500	ns	
Inhibit Response Time	t_R	—	—	200	ns	
Capacitance	C_O	—	8	10	pF	f = 1MHz

**Typical values are at +25°C and nominal voltages

TIMING DIAGRAMS



ACCESS TIME (ADDRESS TO OUTPUT—OUTPUT INHIBIT AT LOGIC '0')



INHIBIT RESPONSE TIME (ADDRESS INPUTS STABLE)

13

8192 Bit Read Only Memory

FEATURES

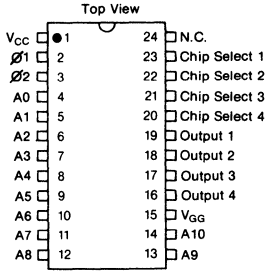
- 2048×4 Organization
- 1.2μs Typical Access Time
- TTL/DTL Compatibility—Inputs and clocks TTL/DTL compatible without external interfacing components.
- Programmable Chip Select—Simplifies design of large memory systems.
- Totally Automated Mask Generation—"RO-5-8192/Custom Coding Information", describing punched card and truth table data specification, is available from GI Sales Offices.
- Zener Protected Inputs
- Glass Passivation Protection

DESCRIPTION

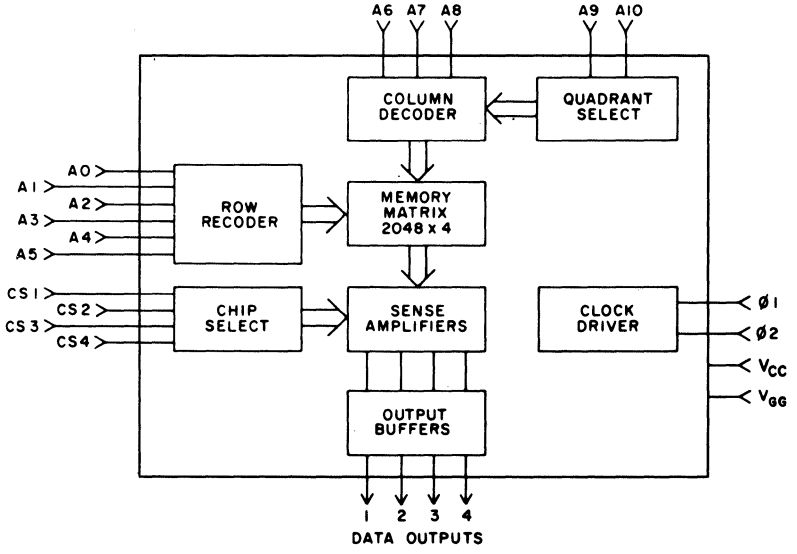
The General Instrument RO-5-8192 is an 8192-bit dynamic Read Only Memory. It is organized as 2048 four bit words and requires 11 bits of addressing. Additional features such as programmable chip select are provided for greater system flexibility. The RO-5-8192 is constructed on a single monolithic chip utilizing MTNS P-channel enhancement mode transistors. The RO-5-8192 is available pre-programmed as a 4 bit random number generator.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GG}, clock and input voltages (with respect to V_{CC}) . . . . . −20V to +0.3V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±5%
V_{GG} = −12 Volts ±5%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: R_L = 6.8K to V_{GG}, C_L TOTAL = 100pf.

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Inputs						
Logic "1"	$V\phi_H$	V_{CC}−1.5	—	—	V	
Logic "0"	$V\phi_L$	—	—	+0.8	V	
Leakage	$I_{L\phi}$	—	—	1.0	μA	$V_{IN} = V_{CC}$−9V, T_A = +25°C
Address, Chip Select Inputs						
Logic "1"	V_{IH}	V_{CC}−1.5	—	—	V	
Logic "0"	V_{IL}	—	—	+0.8	V	
Leakage	I_{LI}	—	—	1.0	μA	$V_{IN} = V_{CC}$−9V, T_A = +25°C
Quadrant Enable Inputs[2]						
Logic "1"	V_{OH}	V_{CC}−1.5	—	—	V	
Logic "0"	V_{OL}	—	—	+0.8	V	
Data Outputs						
Logic "1"	V_{OH}	V_{CC}−1.5	—	—	V	ONE TTL LOAD
Logic "0"	V_{OL}	—	—	V_{CC}−4.5	V	ONE TTL LOAD
Power						
I_{GG}	—	—	275	400	mW	
AC CHARACTERISTICS						
Clock Inputs						
Cycle Time	$t_{\phi C}$	2	—	100	μs	
ϕ1 Pulse Width	$t_{\phi 1pw}$	800	—	—	ns	$t_{\phi 1pw}$-$t_{\phi 2Id} \geq$400ns
ϕ_1 Pulse Separation	$t_{\phi 1ps}$	1200	—	—	ns	
ϕ_2 Lead Time	$t_{\phi 2Id}$	400	—	—	nS	
ϕ_2 Lag Time	$t_{\phi 2Ig}$	400	—	—	nS	
Rise and Fall Times	t_R,t_F	—	—	50	nS	
Capacitance	$C\phi$	—	8	10	pF	1MHz, T_A = +25°C
Inputs						
Set Up Time	t_{DS}	200	—	—	nS	
Hold Time	t_{DH}	200	—	—	nS	
Capacitance	C_I	—	5	7.5	pF	1MHz, T_A = +25°C
Data Outputs						
Propagation Delay	t_{PD}	—	0.6	1	μS	
Access Time	t_{ACC}	—	1.2	1.6	μS	(See Note)
Capacitance	C_O	—	3	5	pF	1MHz, T_A = +25°C

**Typical values are at +25°C and nominal voltages.

NOTE:
Access Time is defined as t_{DS} (min.) + $t_{\phi 2Ig}$ (min.) + t_{PD} (max.)

13

LOGIC DEFINITION

Logic "1" = +5V DC or the more positive voltage
Logic "0" = 0V DC or the more negative voltage

CHIP SELECT

The RO-5-8192 is provided with four programmable bits of chip select. Constructing large memory systems with more than one 8K ROM simply requires wire-working the ROM outputs and assigning different chip select codes to each ROM chip (when a chip is not selected, its outputs are at a logic "0"—the output device is off). In addition, cascading ROMs with the same chip select code provides additional bits per word.

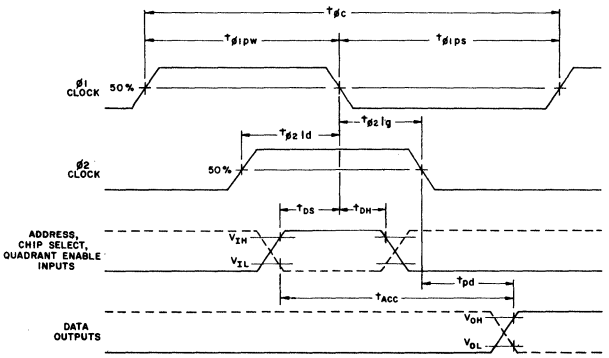
The four chip select bits are permanently programmed into the ROM at the same time as the custom data pattern. 31 different chip select codes are possible—16 unique codes and 15 additional with "don't care" variations (in the following x = 0 or 1):

CS1	CS2	CS3	CS4		
X	X	X	X	—	16 codes
DC	X	X	X	—	8 codes
DC	DC	X	X	—	4 codes
DC	DC	DC	X	—	2 codes
DC	DC	DC	DC	—	1 code

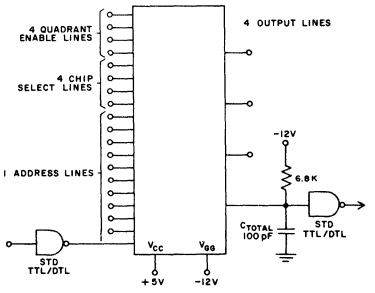
CUSTOM BIT PATTERNS

General Instrument makes use of proven computer techniques to provide fast and accurate generation of custom bit patterns. All necessary material, including the data pattern mask, test data and check lists (for customer verification), ae computer-generated and cross-checked. For the full details on data specification, request the booklet "RO-5-8192/Custom Coding Information" from any GI Sales Office.

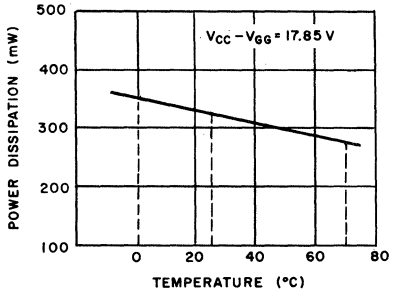
TIMING DIAGRAM



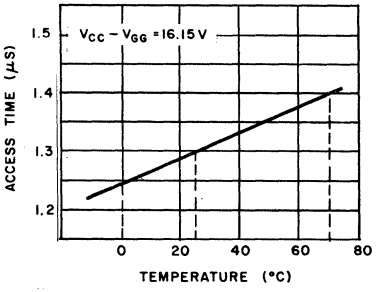
INTERFACE CIRCUIT—TTL/DTL



TYPICAL CHARACTERISTIC CURVES



POWER DISSIPATION vs. TEMPERATURE



ACCESS TIME vs. TEMPERATURE

16384 Bit Static Read Only Memories

FEATURES

- 2048×8 Organization—ideal for microprocessor memory systems.
- Single +5 Volt Supply
- TTL Compatible—all inputs and outputs.
- Static Operation—no clocks required.
- 450ns Maximum Access Time: RO-3-8316B/9316B
- 850ns Maximum Access Time: RO-3-8316A/9316A
- Three-Stage Outputs—under the control of three mask-programmable Chip Select inputs to simplify memory expansion.
- Totally Automated Custom Programming.
- Zener Protected Inputs.
- Glass Passivation Protection.

DESCRIPTION

The General Instrument RO-3-8316A/8316B and RO-3-9316A/9316B are 16,384 static Read Only Memories organized as 2048 eight bit words and are ideally suited for microprocessor memory applications. Fabricated in GI's advanced GIANT II N-channel Ion-Implant process to enable operation from a single +5 Volt power supply, the RO-3-8316A/8316B and RO-3-9316A/9316B offer the best combination of high performance, large bit storage, and simple interfacing of any MOS Read-Only Memories available today.

The RO-3-8316A/8316B are direct replacements in pin connection and operation for the Intel 8316A and 2316A.

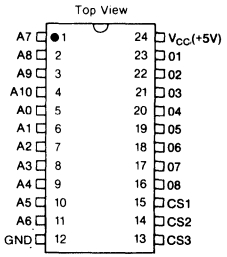
The RO-3-9316A/9316B pin configuration is identical to that of the Intel 2708 8K EPROM.

A separate publication, "RO-3-8316A/8316B and RO-3-9316A/9316B Custom Coding information," available from GI Sales Offices, describes the punched card and truth table format for custom programming.

PIN CONFIGURATION

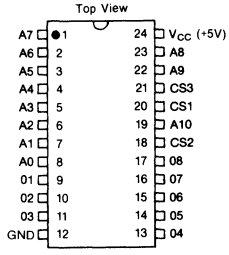
24 LEAD DUAL IN LINE

RO-3-8316A/8316B

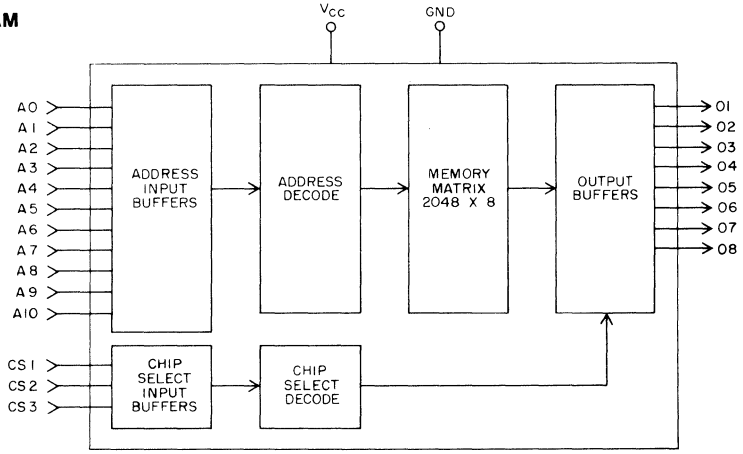


24 LEAD DUAL IN LINE

RO-3-9316A/9316B



BLOCK DIAGRAM



13

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±5%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL load, $C_{L\ TOTAL}$ = 30pF.

RO-3-8316A/9316A and RO-3-8316B/9316B

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Chip Select, Latch Inputs						
Logic "1"	V_{IH}	2.2	—	—	V	
Logic "0"	V_{IL}	—	—	0.65	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.2	—	—	V	I_{OH} = 100μA
Logic "0"	V_{OL}	—	—	0.45	V	I_{OL} = 1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current						
I_{CC}	—	—	50	85	mA	Outputs open (RO-3-8316A/9316A)
	—	—	90	110	mA	Outputs open (RO-3-8316B/9316B)

RO-3-8316A/9316A

AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	800	—	—	ns	
Capacitance	C_I	—	5	8	pF	f=IMHz
Data Outputs						
Access Time	t_{ACC}	—	600	850	ns	
Chip Select Response Time	t_R	—	200	300	ns	
Capacitance	C_O	—	8	10	pF	f=IMHz

RO-3-8316B/9316B

AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	400	—	—	ns	
Capacitance	C_I	—	5	8	pF	f=IMHz
Data Outputs						
Access Time	t_{ACC}	—	350	450	ns	
Chip Select Response Time	t_R	—	100	200	ns	
Capacitance	C_O	—	8	10	pF	f=IMHz

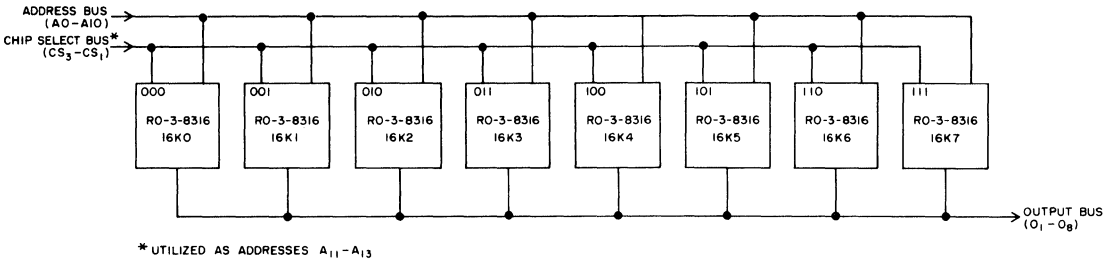
**Typical values are at +25°C and nominal voltages.

TYPICAL SYSTEM APPLICATION

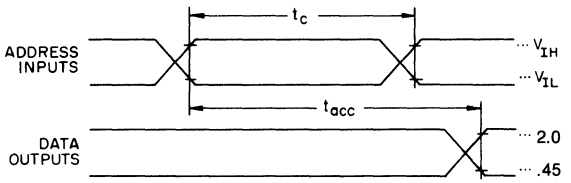
A complete system of 16K words of ROM (8 bits/word) is easily obtained without any external address decoding by making use of programmable chip select features and by wiring the outputs of eight different RO-3-8316's as shown in the figure below.

CHIP SELECT TABLE

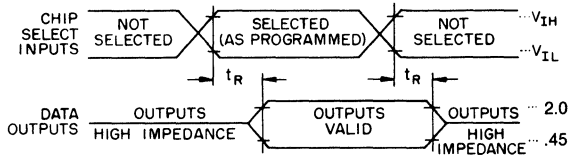
CS 3	CS 2	CS 1	DEVICE SELECTED
0	0	0	16K0
0	0	1	16K1
0	1	0	16K2
0	1	1	16K3
1	0	0	16K4
1	0	1	16K5
1	1	0	16K6
1	1	1	16K7



TIMING DIAGRAMS



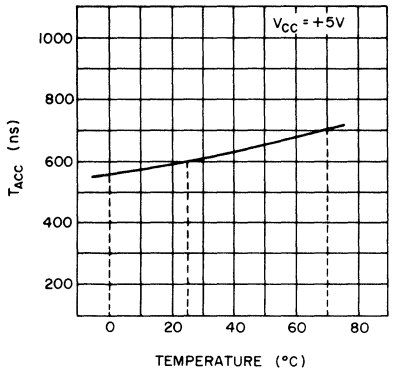
ACCESS TIME (ADDRESS TO OUTPUT—CHIP SELECTED)



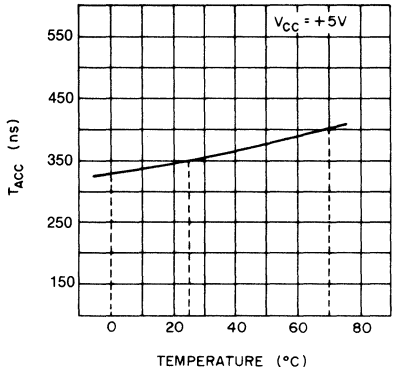
CHIP SELECT RESPONSE TIME (ADDRESS INPUTS STABLE)

13

TYPICAL CHARACTERISTIC CURVES

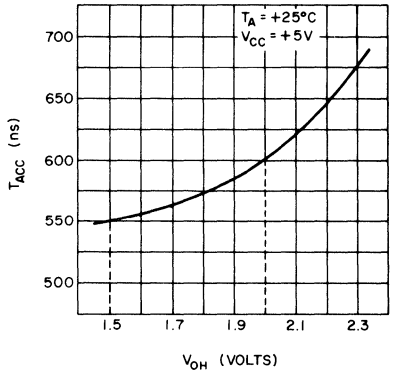


RO-3-8316A/9316A

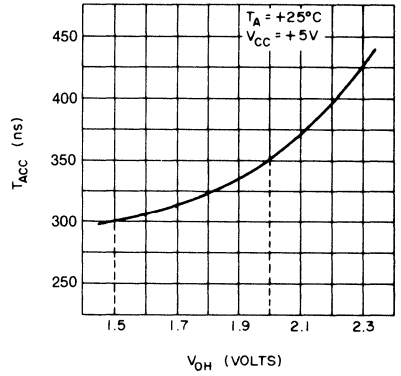


RO-3-8316B/9316B

Fig.1 ACCESS TIME VS. TEMPERATURE

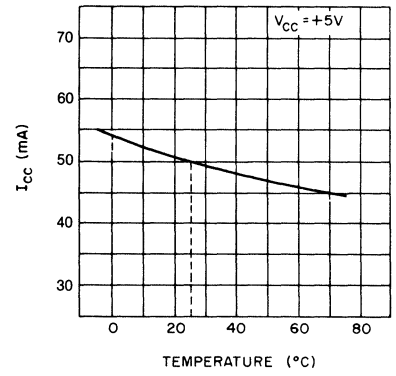


RO-3-8316A/9316A

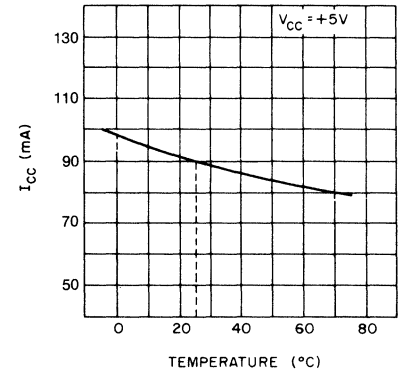


RO-3-8316B/9316B

Fig.2 ACCESS TIME VS. OUTPUT VOLTAGE



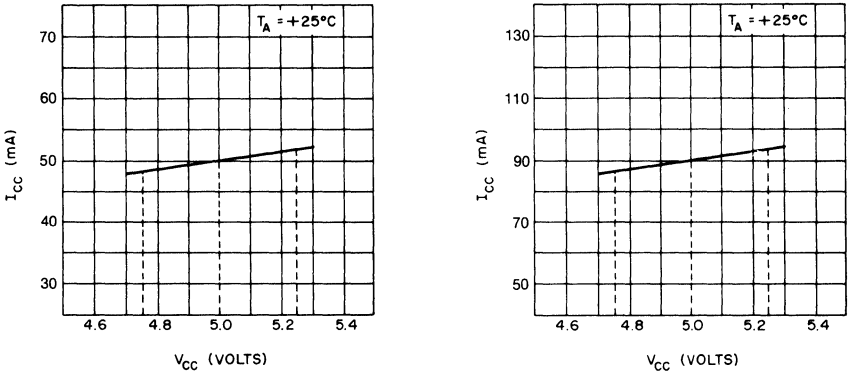
RO-3-8316A/9316A



RO-3-8316B/9316B

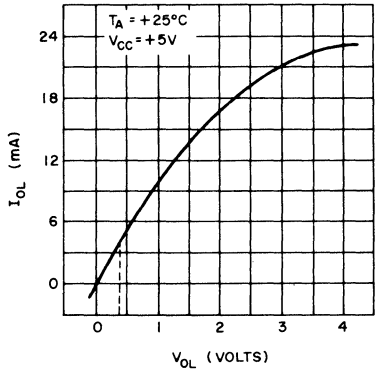
Fig.3 POWER SUPPLY CURRENT VS. TEMPERATURE

TYPICAL CHARACTERISTIC CURVES



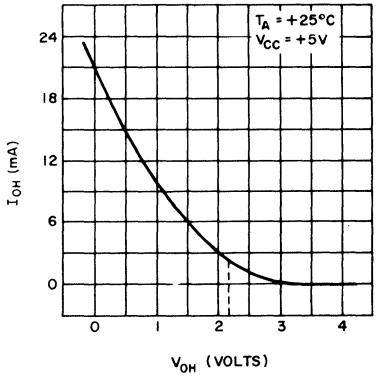
RO-3-8316A/9316A **RO-3-8316B/9316B**

Fig.4 POWER SUPPLY CURRENT VS. SUPPLY VOLTAGE



RO-3-8316A/8316B, RO-3-9316A/9316B

Fig.5 OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



RO-3-8316A/8316B, RO-3-9316A/9316B

Fig.6 OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE

16384 Bit Static Read Only Memory

FEATURES

- 4096×4 Organization
- Single +5 Volt Supply
- TTL/DTL Compatible
- Static Operation—no clocks required
- Address/Chip Select Latch Input—may be used to gate in new Address or Chip Select Inputs
- 1 μs Maximum Access Time
- 250 mW Typical Power
- Three-State Outputs—under control of 3 programmable Chip Select Inputs.
- Totally Automated Custom Programming
- Zener Protected Inputs
- Glass Passivation Protection

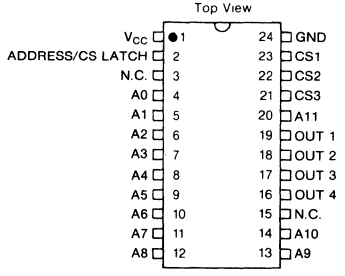
DESCRIPTION

The General Instrument RO-3-16384 is a 16,384 bit static Read-Only-Memory. It is organized as 4096 four bit words and requires 12 bits of addressing. Three programmable Chip Select inputs are provided to simplify the connection of several ROMs to a common bus. The RO-3-16384 is constructed on a single monolithic chip utilizing low-voltage N-channel Ion Implant technology.

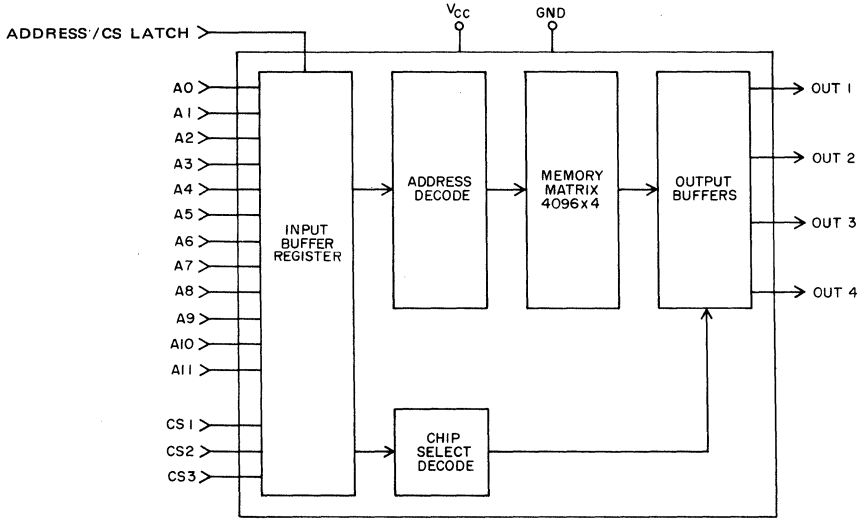
A separate publication, "RO-3-16384 Custom Coding Information," available from GI Sales Offices, describes the punched card and truth table data format for custom programming of the RO-3-16384 memory.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . . . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

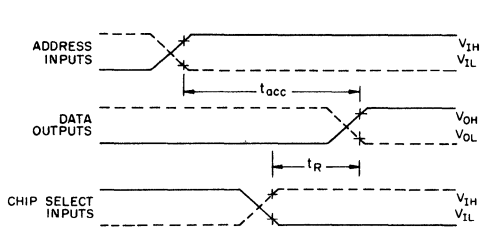
Standard Conditions: (unless otherwise noted)

V_{CC} = +5 volts ± 5%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL load, $C_{L\ total}$ = 50 pF.

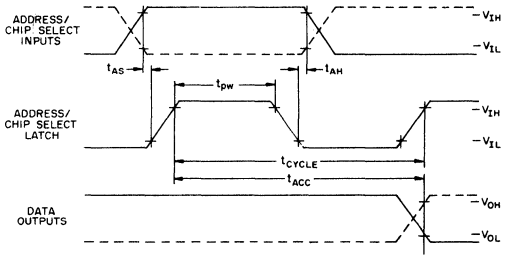
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Chip Select, Latch Inputs						
Logic "1"	V_{IH}	2.2	—	—	V	
Logic "0"	V_{IL}	—	—	0.65	V	
Leakage	I_{LI}	—	—	10′	μA	
Data Outputs						
Logic "1"	V_{OH}	2.2	—	—	V	I_{OH} = 100μA
Logic "0"	V_{OL}	—	—	0.45	V	I_{OL} = 1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current						
I_{CC}	—	—	50	65	mA	Outputs open
AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	1.0	—	—	μs	
Set-up Time	t_{AS}	0	—	—	ns	
Hold Time	t_{AH}	200	—	—	ns	
Capacitance	C_I	—	5	8	pF	f = 1MHz
Latch Input						
Pulse Width	t_{PW}	200	—	—	ns	
Data Outputs						
Access Time	t_{ACC}	—	0.7	1.0	μs	
Chip Select Response Time	t_R	—	200	300	ns	Latch at +5V
Capacitance	C_O	—	8	10	pF	f = 1MHz

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS



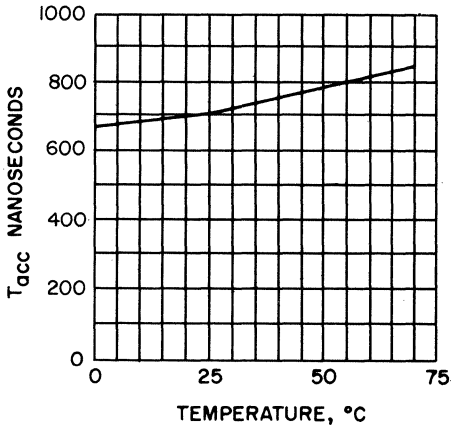
WITH LATCH INPUT HELD AT +5V

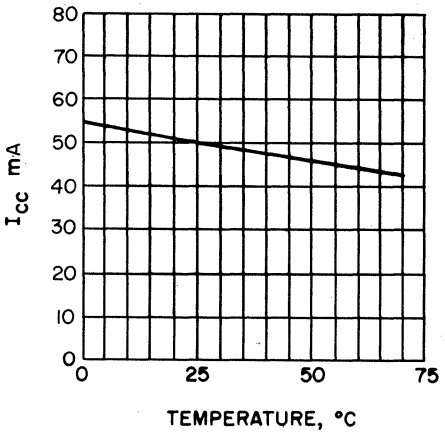


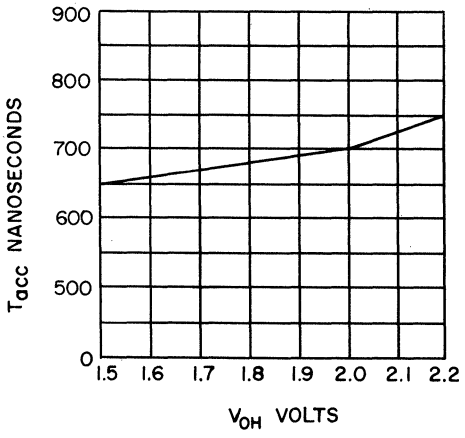
WITH LATCH INPUT UTILIZED

13

TYPICAL CHARACTERISTIC CURVES







20480 Bit Static Read Only Memory

FEATURES

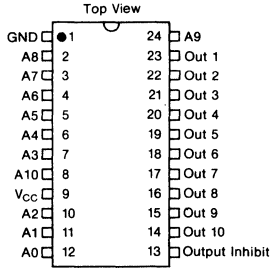
- 2048×10 Organization—ideal for microprocessor memory systems.
- Single +5 Volt Supply.
- TTL/DTL Compatible
- Static Operation—no clocks.
- 500ns Maximum Access Time
- 250mW Typical Power
- Three-State Outputs—under control of Output Inhibit.

DESCRIPTION

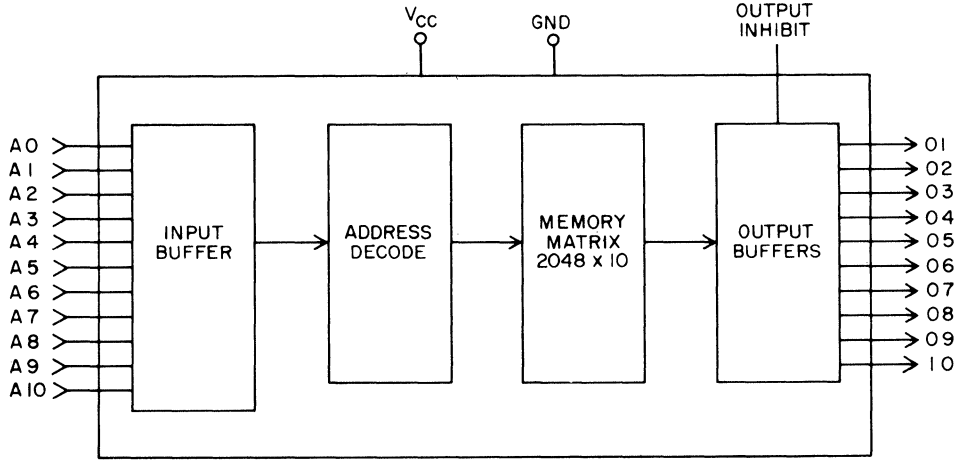
The General Instrument RO-3-20480 is a 20,480 bit static Read Only Memory ideally suited for microprocessor memory applications. Fabricated in GI's advanced GIANT II N-channel Ion-Implant process to enable operation from a single +5 Volt power supply, the RO-3-20480 offers high performance, large bit storage, and simple interfacing.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



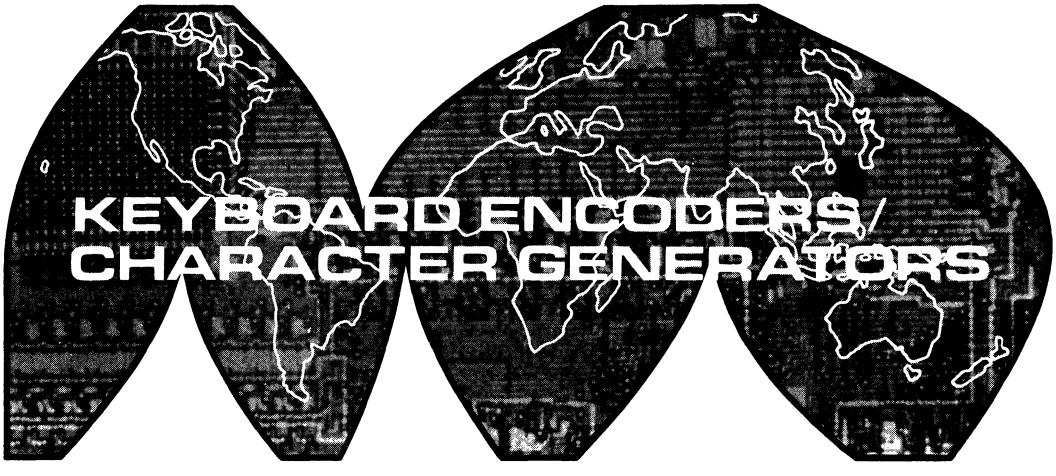
BLOCK DIAGRAM



13

GENERAL INSTRUMENT

AY-5-2376
AY-5-3600
RO-5-2240S
RO-3-2513
RO-5-5184



KEYBOARD ENCODERS/ CHARACTER GENERATORS

Keyboard Encoder

FEATURES

- One integrated circuit required for complete keyboard assembly.
- Outputs directly compatible with TTL/DTL or MOS logic arrays.
- External control provided for output polarity selection.
- External control provided for selection of odd or even parity.
- Two key roll-over operation.
- N-key lockout.
- Programmable coding with a single mask change.
- Self-contained oscillator circuit.
- Externally controlled delay network provided to eliminate the effect of contact bounce.
- Static charge protection on all input and output terminals.
- Entire circuit protected by a layer of glass passivation.

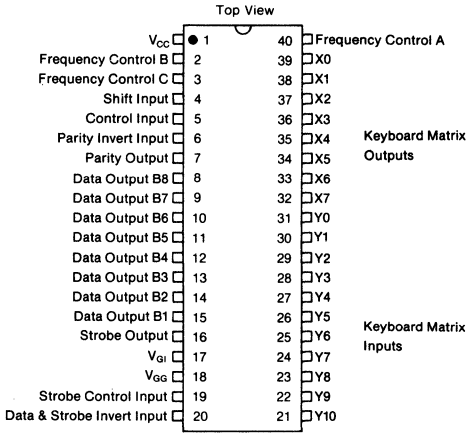
DESCRIPTION

The General Instrument AY-5-2376 is a 2376 Bit Read Only Memory with all the logic necessary to encode single pole single throw keyboard closures into a usable 9-bit code. Data and strobe outputs are directly compatible with TTL/DTL or MOS logic arrays without the use of any special interface components.

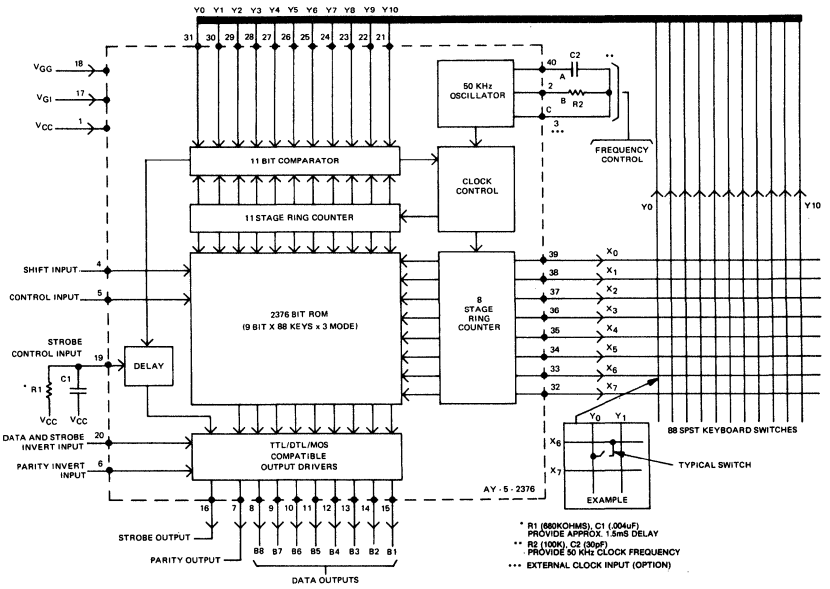
The AY-5-2376 is fabricated with MTNS technology and contains 2942 P-channel enhancement mode transistors on a single monolithic chip.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



BLOCK DIAGRAM



OPERATION

The AY-5-2376 contains (see Block Diagram), a 2376-bit ROM, 8-stage and 11-stage ring counters, an 11-bit comparator, an oscillator circuit, an externally controllable delay network for eliminating the effect of contact bounce, and TTL/DTL/MOS compatible output drivers.

The ROM portion of the chip is a 264 by 9 bit memory arranged into three 88-word by 9-bit groups. The appropriate levels on the Shift and Control Inputs selects one of the three 88-word groups; the 88-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control Inputs with the two ring counters.

The external outputs of the 8-stage ring counter and the external inputs to the 11-bit comparator are wired to the keyboard to form an X-Y matrix with the 88-keyboard switches as the crosspoints. In the standby condition, when no key is depressed, the two ring counters are clocked and sequentially address the ROM; the absence of a Strobe Output indicates that the Data Outputs are 'not valid' at this time.

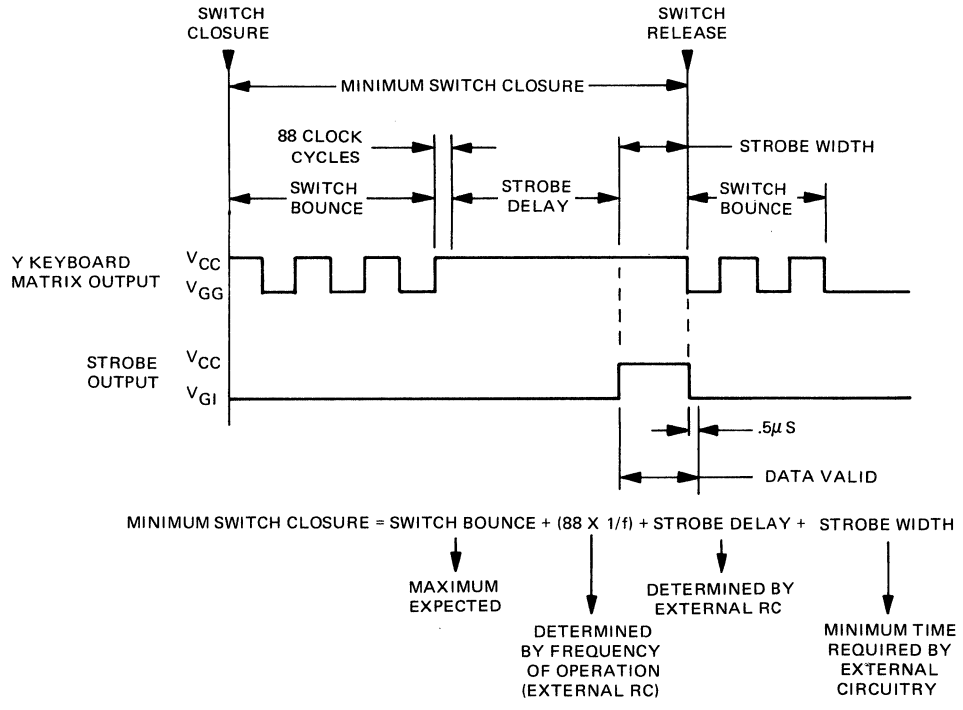
When a key is depressed, a single path is completed between one output of the 8-stage ring counter (X0 thru X7) and one input of the 11-bit comparator (Y0-Y10). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 11-stage ring counter. When this occurs, the comparator generates a signal to the clock control and to the Strobe Output (via the delay network). The clock control stops the clocks to the ring counters and the Data Outputs (B1-B9) stabilize with the selected 9-bit code, indicated by a 'valid' signal on the Strobe Output. The Data Outputs remain stable until the key is released.

As an added feature two inputs are provided for external polarity control of the Data Outputs. Parity Invert (pin 6) provides polarity control of the Parity Output (pin 7) while the Data and Strobe Invert Input (pin 20) provides for polarity control of Data Outputs B1 thru B8 (pins 8 thru 15) and the Strobe Output (pin 16).

SPECIAL PATTERNS

Since the selected coding of each key is defined during the manufacture of the chip, the coding can be changed to fit any particular application of the keyboard. Up to 264 codes of up to 8 bits (plus one parity bit) can be programmed into the AY-5-2376 ROM covering most popular codes such as ASCII, EBCDIC, Selectric, etc., as well as many specialized codes. The ASCII code is available as a standard pattern.

TIMING DIAGRAM



14

ELECTRICAL CHARACTERISTICS

Maximum Ratings

V_{GI} and V_{GG} (with respect to V_{CC}) . . . . . −20V to +0.3V
Logic input voltages (with respect to V_{CC}) . . . −20V to +0.3V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature Range . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

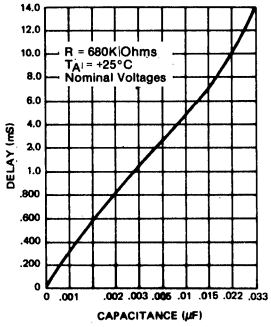
V_{CC} = +5 Volts ± 0.5 Volts, V_{GG} = −12 Volts ± 1.0 Volts, V_{GI} = GND. | (V_{CC} = Substrate Voltage) Operating Temperature (T_A) = 0°C to +70°C

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
Clock Frequency	f	10	50	100	KHz	See Block diagram footnote** for typical R - C values
Data Input (Shift, Control, Parity invert, data & strobe invert).						
Logic "0" Level	V_{I0}	V_{GG}	—	+0.8	V	
Logic "1" Level	V_{I1}	V_{CC}−1.5	—	V_{CC}+0.3	V	
			—			
Shift & Control Input Current	$I_{INS,C}$	15	36	60	μA	V_I=+5V
		8	16	30	μA	V_I= 0V
Data, Parity Invert Input Current	$I_{IND,P}$	—	.01	1	μA	V_I=−5V to +5V
X Output (X_0-X_7)						
Logic "1" Output Current	I_{XI}	—	0	—	μA	$V_{OUT} = V_{CC}$
		80	150	400	μA	$V_{OUT} = V_{CC}$ −1.3V
		140	300	800	μA	$V_{OUT} = V_{CC}$ −2.0V
		250	700	1500	μA	$V_{OUT} = V_{CC}$ −5V
		500	1500	3000	μA	$V_{OUT} = V_{CC}$ — 10V
Logic "0" Output Current	I_{XO}	15	30	80	μA	$V_{OUT} = V_{CC}$
		13	27	65	μA	$V_{OUT} = V_{CC}$ −1.3V
		12	25	60	μA	$V_{OUT} = V_{CC}$ −2.0V
		5	10	40	μA	$V_{OUT} = V_{CC}$ −5V
		—	1	20	μA	$V_{OUT} = V_{CC}$ −10V
Y Input (Y_0-Y_{10})						
Trip Level	V_Y	V_{CC} −5	V_{CC} −3	V_{CC}−2	V	Y Input Going Positive
Hysteresis	ΔV_Y	.5	.9	1.4	V	Note 1
						Note 2
Selected Y Input Current	I_{YS}	30	60	160	μA	$V_{IN} = V_{CC}$
		26	54	130	μA	$V_{IN} = V_{CC}$ −1.3V
		24	50	120	μA	$V_{IN} = V_{CC}$ −2.0V
		10	20	80	μA	$V_{IN} = V_{CC}$ −5V
		—	2	20	μA	$V_{IN} = V_{CC}$ −10V
Unselected Y Input Current	I_{YU}	15	30	80	μA	$V_{IN} = V_{CC}$
		13	27	65	μA	$V_{IN} = V_{CC}$ −1.3V
		12	25	60	μA	$V_{IN} = V_{CC}$ −2.0V
		5	10	40	μA	$V_{IN} = V_{CC}$ −10V
Input Capacitance	C_{IN}	—	3	10	pf	at 0V
Switch Characteristics						
Minimum Switch Closure	—	—	—	—	—	See Timing Diagram
Contact Closure Resistance	Z_{CC}	—	—	300	Ω	
	Z_{CO}	1×10^7	—	—	Ω	
Strobe Delay						
Trip Level (Pin 19)	V_{SD}	V_{CC}−4	V_{CC}−3	V_{CC}−2	V	
Hysteresis	V_{SD}	.5	.9	1.4	V	See Note 1
Quiescent Voltage (Pin 19)		−3	−5	−8	V	With 680KΩ to V_{SS}
Data Output (B_1-B_8)						
Logic "0"	—	—	—	0.4	V	I_{OL} = 1.6ma
Logic "1"	—	V_{CC}−1	—	—	V	I_{OH}−100μa
Power						
I_{CC}	—	—	5	10	mA	V_{CC} = +5V
I_{GG}	—	—	5	10	mA	V_{GG} = −12V

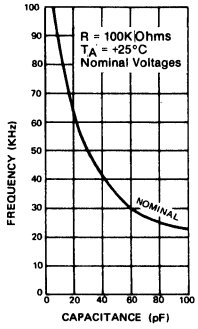
**Typical values at +25° C and nominal voltages.

NOTE 1. Hysteresis is defined as the amount of return required to unlatch an input.
2. Guaranteed number of X & Y loads which may be applied to an X output = eleven.

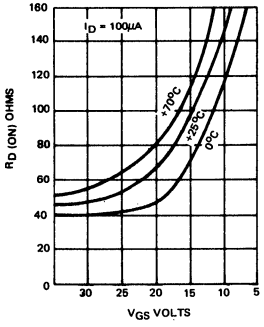
TYPICAL CHARACTERISTIC CURVES



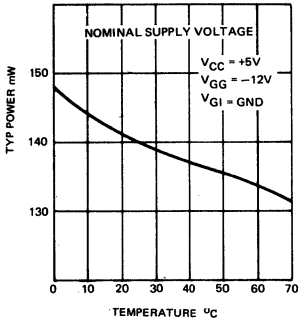
STROBE DELAY VS. C1



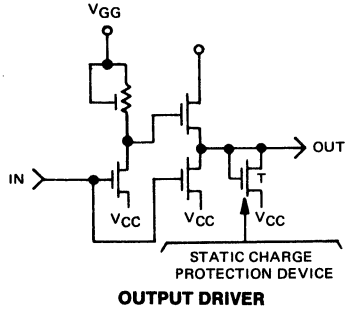
OSCILLATOR FREQUENCY VS. C2



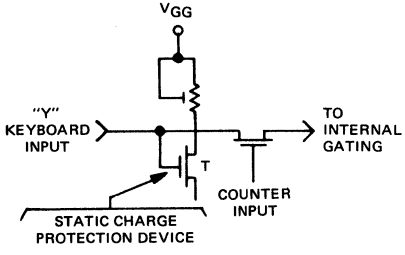
TYPICAL OUTPUT ON RESISTANCE (R_{DON}) VS. GATE BIAS VOLTAGE (V_{GS})



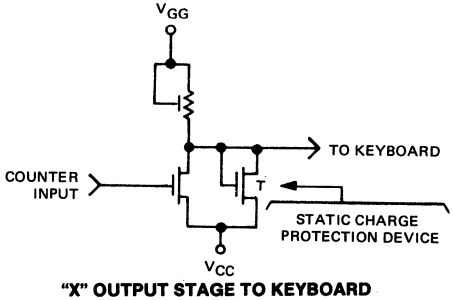
TYPICAL POWER CONSUMPTION (mW) VS. TEMP (C°)



OUTPUT DRIVER



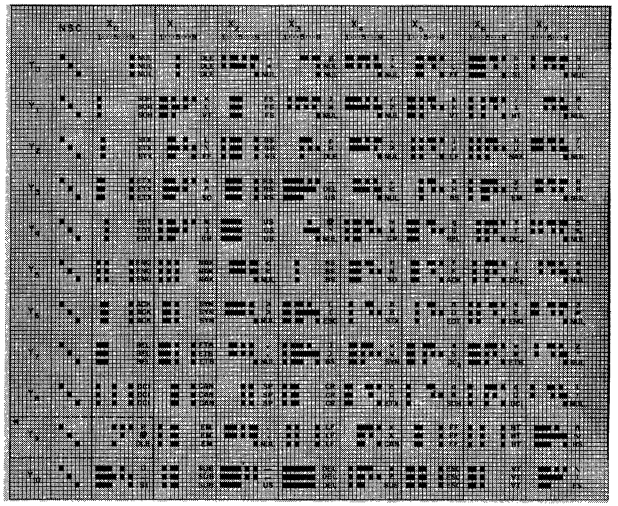
"Y" INPUT STAGE FROM KEYBOARD



"X" OUTPUT STAGE TO KEYBOARD

14

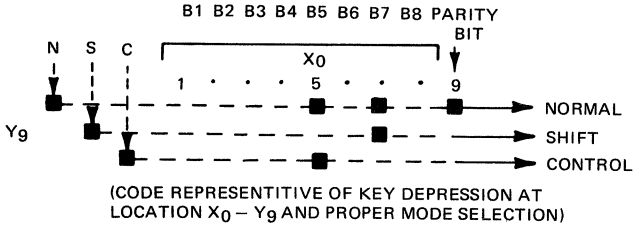
STANDARD CODE ASSIGNMENT CHART



Illustrated using a Logic "O" on the Data and Strobe Invert Input (Pin 20) and the Parity Invert Input (Pin 6).

NOTE 1: This code is an 8 bit ASCII code (B1-B8). Output B9 is included as an odd parity bit operating on outputs B1-B7.

*EXAMPLE



N = NORMAL MODE
S = SHIFT MODE
C = CONTROL MODE
■ = OUTPUT LOGIC "1". (SEE DATA B1 – B8)
LOGIC "1" = +5V
LOGIC "0" = GND

TRUTH TABLES

DATA (B1-B8) INVERT TRUTH TABLE

DATA AND STROBE INVERT INPUT (PIN 20)	CODE ASSIGNMENT CHART	DATA OUTPUTS (B1-B8)
1	1	0
0	1	1
1	0	1
0	0	0

PARITY INVERT TRUTH TABLE

PARITY INVERT INPUT (PIN 6)	CODE ASSIGNMENT CHART	PARITY OUTPUT (PIN 7)
1	1	0
0	1	1
1	0	1
0	0	0

STROBE INVERT TRUTH TABLE

DATA AND STROBE INVERT INPUT (PIN 20)	INTERNAL STROBE	STROBE OUTPUT (PIN 16)
1	1	0
0	0	0
1	0	1
0	1	1

MODE SELECTION

$\overline{S}\ \overline{C}$ = N
$\overline{S}$ C = S
S $\overline{C}$ = C
S C = C

Keyboard Encoder

FEATURES

- One integrated circuit required for complete keyboard assembly.
- N key rollover or lock out operation.
- Quad mode operation.
- Lock out/rollover selection under external control (option).
- Self-contained or slave oscillator circuit.
- 10 output data bits available.
- Outputs directly compatible with TTL/DTL or MOS logic arrays.
- Output data buffer register included.
- Output enable provided (option).
- External data complement control provided (option).
- Pulse or level data ready output signal provided (option).
- "Any Key Down" output provided (option).
- Externally controlled delay network provided to eliminate the effect of contact bounce.
- Programmable coding with a single mask change.
- Static charge protection on all input and output terminals.
- Entire circuit protected by a layer of glass passivation.

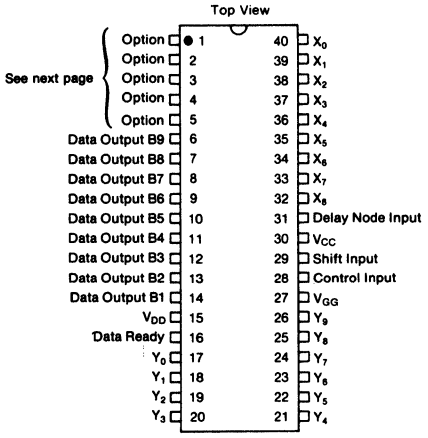
DESCRIPTION

The General Instrument AY-5-3600 is a Keyboard Encoder containing a 3600 bit Read Only Memory and all the logic necessary to encode single pole single throw keyboard closures into a usable 10 bit code. Data, Any Key Down and Data Ready outputs are directly compatible with TTL/DTL or MOS logic arrays without the need for any special interface components.

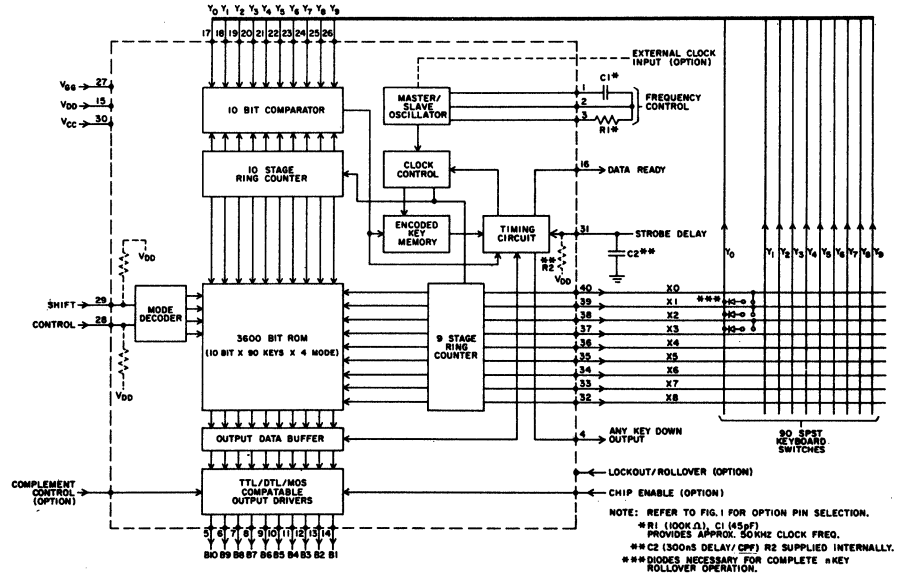
The AY-5-3600 is fabricated with MTNS technology and contains 5000 P channel enhancement mode transistors on a single monolithic chip.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



BLOCK DIAGRAM



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CUSTOM CODING INFORMATION

The custom coding information for General Instrument's AY-5-3600 Keyboard Encoder ROM should be transmitted to General Instrument in the form of 80 column punched cards. Each ROM pattern requires 92 cards (1 title card, 1 circuit option card and 90 ROM pattern cards). (See Note 1)

If it is not possible to supply punched cards, then the Truth Table should be completed (See Note 1). However, there would be a substantial savings in both the coding charge and turn-around time if punched cards were used. Upon receipt of the punched cards or the Truth Table, General Instrument will prepare a computer-generated Truth Table which will be returned to the user for verification.

NOTE 1: Card and Truth Table format available upon request.

PIN OPTIONS

Pins 6-40 of the AY-5-3600 are permanently assigned. The functions assigned to pins 1-5 depend on which functional options are selected from the following:

External Clock
—requires one package pin to input an external clock source.
Internal Oscillator
—requires three package pins interconnected with an external RC network to develop the clock required.
Lockout/Rollover (LO/RO)
—requires one package pin to externally select N-Key Lockout or N-Key Rollover. LO = +5V, RO = GND.
Complement Control (CC)
—requires one package pin to externally control the logic state of the data bits (B1-B10) and, if required, the Data Ready output.
Chip Enable (CE)
—requires one package in to control the data bits (B1-B10) and, if required, the Data Ready and Any Key Output.
Any Key Output (AKO)
—requires one package pin to indicate a key depression.
Output Data Bit 10 (B10)
—requires one package pin when ten data bits are required to encode each key.

Select the pin options desired:
External Clock + 4 of the following functions
OR
Internal Oscillator + 2 of the following functions
LO/RO, CC, CE, AKO, BIO

The following chart lists the pin assignments according to the functions selected above:

PIN 1	PIN 2	PIN 3	PIN 4	PIN 5
External Clock	LO/RO	CC	CE	AKO
External Clock	LO/RO	CC	CE	BIO
External Clock	LO/RO	CC	AKO	BIO
External Clock	LO/RO	CE	AKO	BIO
External Clock	CC	CE	AKO	BIO
Internal Oscillator			LO/RO	CC
			LO/RO	CE
			LO/RO	AKO
			LO/RO	BIO
			CC	CE
			CC	AKO
			CC	BIO
			CE	AKO
			CE	BIO
			AKO	BIO

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} and V_{GG} (with respect to V_{CC}) . . . . . −20V to +0.3V
Logic input voltages (with respect to V_{CC}) . . . . . −20V to +0.3V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature Range. . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±0.5 Volts
V_{GG} = −12 Volts ±1.0 Volts, V_{DD} = GND
(V_{CC} = Substrate Voltage)
Operating Temperature (T_A)= 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
Clock Frequency	f	10	50	100	KHz	See Block diagram footnote* for typical R-C values
External Clock Width		7	—	—	μs	
Data & Clock Input (Shift, Control, Compliment Control, Lockout/Rollover, Chip Enable & External Clock)						
Logic "0" Level	V_{I0}	V_{GG}	—	+0.8	V	
Logic "1" Level	V_{I1}	V_{CC}–1.5	—	V_{CC}+0.3	V	
Shift & Control Input Current	I_{NSC}	75	95	120	μA	V_I = +5V
X Output (X_0-X_8)						
Logic "1" Output Current	I_{X1}	40	170	400	μA	V_{OUT} = V_{CC} (See Note 2)
		600	1300	2500	μA	V_{OUT} = V_{CC}–1.3V
		900	1600	3500	μA	V_{OUT} = V_{CC}–2.0V
		1500	3800	6000	μA	V_{OUT} = V_{CC}–5V
		3000	6000	10000	μA	V_{OUT} = V_{CC}–10V
Logic "0" Output Current	1_{XO}	8	15	50	μA	V_{OUT} = V_{CC}
		6	11	35	μA	V_{OUT} = V_{CC}–1.3V
		5	10	30	μA	V_{OUT} = V_{CC}–2.0V
		2	5	15	μA	V_{OUT} = V_{CC}–5V
		—	0.5	5	μA	V_{OUT} = V_{CC}–10V
Y Input (Y_0-Y_9)						
Trip Level	V_Y	V_{CC}–5	V_{CC}–3	V_{CC}–2	V	Y Input Going Positive (See Note 2)
Hysteresis	ΔV_Y	0.5	0.9	1.4	V	(See Note 1)
Selected Y Input Current	I_{YS}	18	36	100	μA	V_{IN} = V_{CC}
		14	28	90	μA	V_{IN} = V_{CC}–1.3V
		13	25	80	υA	V_{IN} = V_{CC}–2.0V
		6	12	60	μA	V_{IN} = V_{CC}–5V
		—	1	30	μA	V_{IN} = V_{CC}–10V
Unselected Y Input Current	I_{YU}	9	18	50	μA	V_{IN} = V_{CC}
		7	14	45	μA	V_{IN} = V_{CC}–1.3V
		6	13	40	μA	V_{IN} = V_{CC}–2.0V
		3	6	30	μA	V_{IN} = V_{CC}–5V
		—	0.5	15	μA	V_{IN} = V_{CC}–10V
Input Capacitance	C_{IN}	—	3	10	pF	at 0V (All Inputs)
X-Y Precharge Characteristics	ϕP	1500	3500	5000	μA	V = V_{CC}
		200	600	1500	μA	V = V_{CC}–5 (See Note 2)
Switch Characteristics						
Minimum Switch Closure	—	—	—	—	—	See Timing Diagram
Contact Closure Resistance	Z_{CC}	—	—	300	Ω	
	Z_{CO}	1×10^7	—	—	Ω	
Strobe Delay						
Trip Level (Pin 31)	V_{SD}	V_{CC}–4	V_{CC}–3	V_{CC}–2	V	
Hysteresis	V_{SD}	0.5	0.9	1.4	V	(See Note 1)
Quiescent Voltage (Pin 31)		–3	–5	–9	V	With Internal Switched Resistor
Data Output (B1-B10), Any Key Down Output, Data Ready						
Logic "0"	—	—	—	0.4	V	I_{OL} = 1.6m A
Logic "1"	—	V_{CC}–1	—	—	V	I_{OH} = 1.0m A
	—	V_{CC}–2	—	—	V	I_{OH} = 2.2m A
Power						
I_{CC}	—	—	8	12	mA	V_{CC} = +5V
I_{GG}	—	—	8	12	mA	V_{GG} = –12V

**Typical values are at +25° C and nominal voltages.

NOTE
1. Hysteresis is defined as the amount of return required to unlatch an input.
2. Precharge of X outputs and Y inputs occurs during each scanned clock cycle.

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OPERATION

The AY-5-3600 contains (see Block Diagram), a 3600 bit ROM, 9-stage and 10-stage ring counters, a 10 bit comparator, timing circuitry, a 90 bit memory to store the location of encoded keys for n key rollover operation, an externally controllable delay network for eliminating the effect of contact bounce, an output data buffer, and TTL/DTL/MOS compatible output drivers.

The ROM portion of the chip is a 360 by 10 bit memory arranged into four 90-word by 10-bit groups. The appropriate levels on the Shift and Control Inputs selects one of the four 90-word groups; the 90-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control Inputs with the two ring counters.

The external outputs of the 9-stage ring counter and the external inputs to the 10-bit comparator are wired to the keyboard to form an X-Y matrix with the 90-keyboard switches as the crosspoints. In the standby condition, when no key is depressed, the two ring counters are clocked and sequentially address the ROM, thereby scanning the key switches for key closures.

When a key is depressed, a single path is completed between one output of the 9-stage ring counter (X0 thru X8) and one input of the 10-bit comparator (Y_0-Y_9). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 10-stage ring counter.

N KEY ROLLOVER

— When a match occurs, and the key has not been encoded, the switch bounce delay network is enabled. If the key is still depressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears, a one is stored in the encoded key memory and the scan sequence is resumed. If a match occurs at another key location, the sequence is repeated thus encoding the next key. If the match occurs for an already encoded key, the match is not recognized. The code of the last key encoded remains in the output data buffer.

N KEY LOCKOUT

— When a match occurs, the delay network is enabled. If the key is still depressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears and the remaining keys are locked out by halting the scan sequence. The scan sequence is resumed upon key release. The output data buffer stores the code of the last key encoded.

SPECIAL PATTERNS

— Since the selected coding of each key and all the options are defined during the manufacture of the chip, the coding and options can be changed to fit any particular application of the keyboard. Up to 360 codes of up to 10 bits can be programmed into the AY-5-3600 ROM covering most popular codes such as ASCII, EBCDIC, Selectric, etc., as well as many specialized codes. The ASCII code in conjunction with internal oscillator, 10 data outputs and any key down output, is available as a standard pattern (See Figure 2) for special patterns and options.

TIMING DIAGRAM

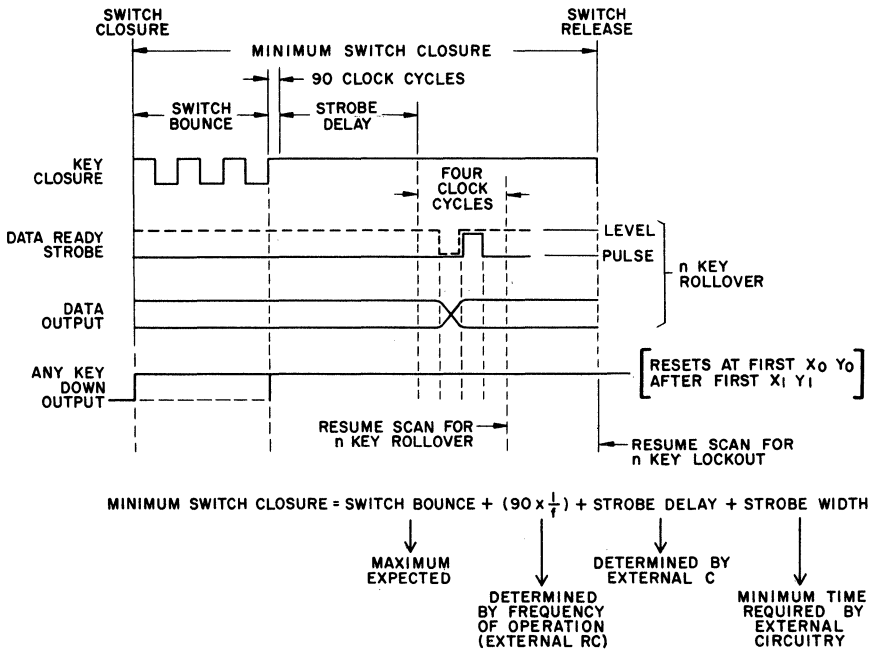
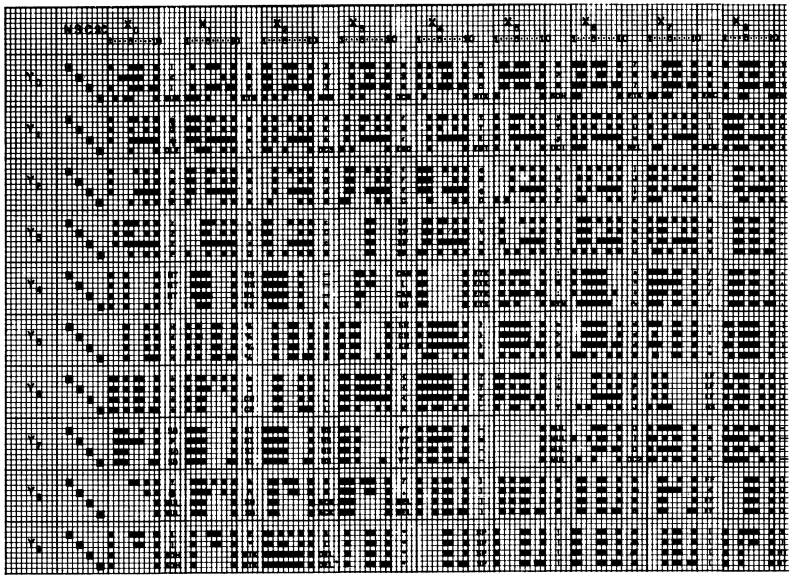
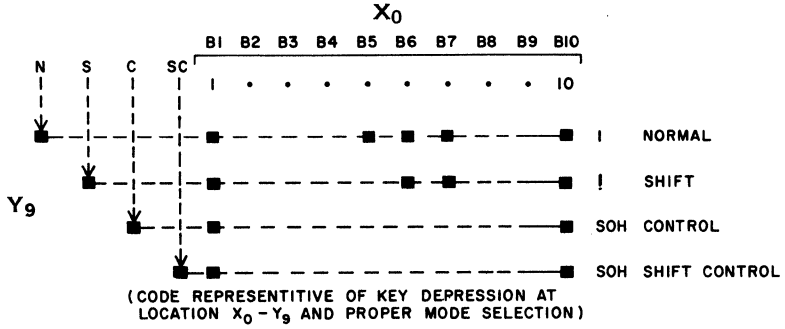


Fig.1

CONFIGURATION & CODE OF STANDARD ENCODER



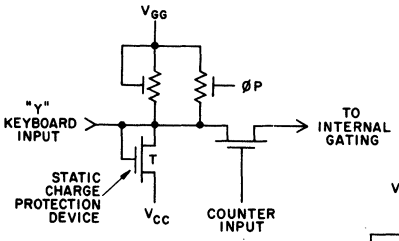
EXAMPLE



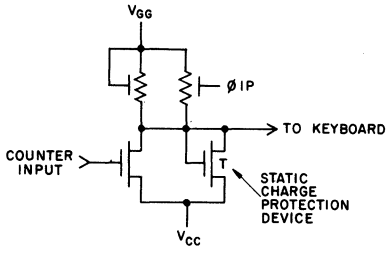
N = NORMAL MODE
S = SHIFT MODE
C = CONTROL MODE
SC = SHIFT CONTROL
■ = OUTPUT LOGIC "1" (SEE DATA B1-B10)
LOGIC "1" = V_{CC}
LOGIC "0" = V_{DD}
} TRUE OUTPUTS

MODE SELECTION			
$\bar{S}$	$\bar{C}$	=	N
S	$\bar{C}$	=	S
$\bar{S}$	C	=	C
S	C	=	SC

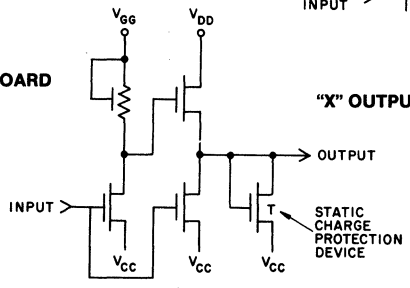
Fig.3



"Y" INPUT STAGE FROM KEYBOARD



"X" OUTPUT STAGE TO KEYBOARD



OUTPUT DRIVER

NOTE: Output driver capable of driving one TTL load with no external resistor.
Capable of driving two TTL loads using an external 6.8KΩ resistor to V_{GG}.

TYPICAL CHARACTERISTIC CURVES

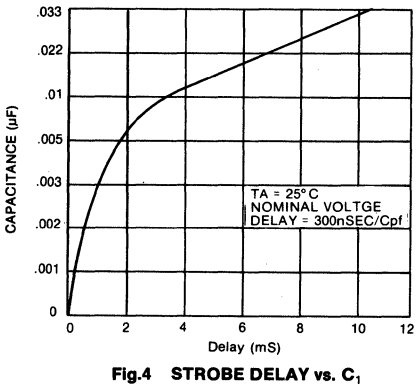


Fig.4 STROBE DELAY vs. C_1

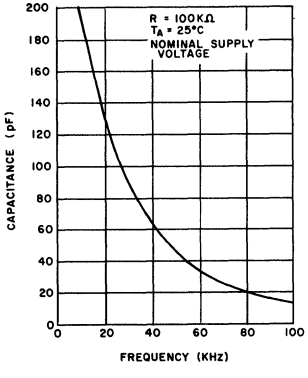


Fig.5 OSCILLATOR FREQUENCY vs. C_2

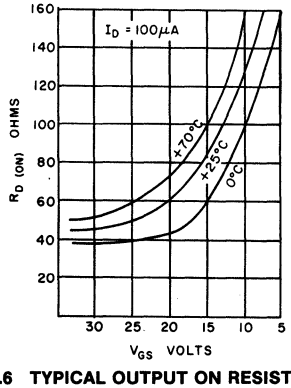


Fig.6 TYPICAL OUTPUT ON RESISTANCE (R_{DON}) vs. GATE BIAS VOLTAGE (V_{GS})

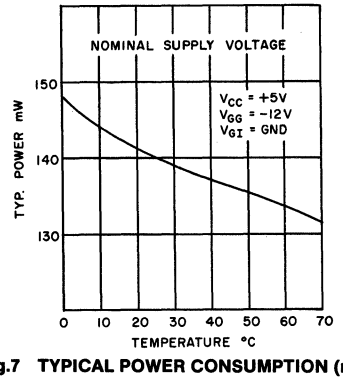


Fig.7 TYPICAL POWER CONSUMPTION (mW)

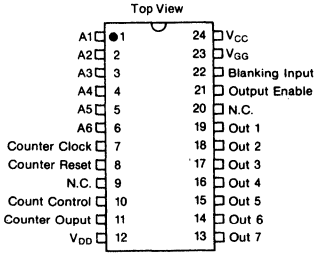
Character Generator

FEATURES

- FULL TTL/DTL COMPATIBILITY
  No external interfacing components required.
- 1 μs TYP. ACCESS TIME/STATIC OPERATION
  The output data remains valid as long as the input data/internal counter remain unchanged.
- COLUMN OUTPUT
  2240 bits of storage organized as 64 5×7 dot matrix characters with column by column output.
- INTERNAL COUNTER
  Provides sequential column selection from a single counter clock input.
- COUNT CONTROL
  Allows the selection of either one or two column intercharacter spacing.
- COUNTER OUTPUT
  Provides an "update" signal for external character address registers.
- BLANKING AND OUTPUT ENABLE
  Provide full output control without affecting any other ROM function.
- ZENER PROTECTED INPUTS
- GLASS PASSIVATION PROTECTION

PIN CONFIGURATION

24 LEAD DUAL IN-LINE

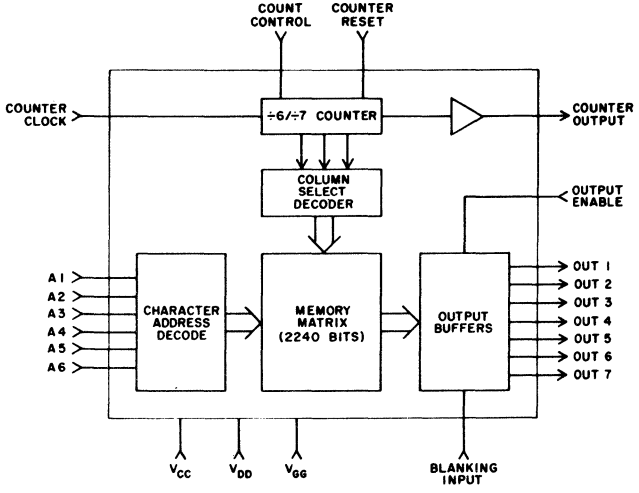


DESCRIPTION

The General Instrument RO-5-2240S is a 2240 bit Read Only Memory organized as a 320 words × 7 bits character generator (64 characters, each having 5 columns of 7 bits). Column by column character data is provided for vertical scan display applications. An internal counter and a full complement of control signals allow for the greatest system design flexibility. The RO-5-2240S is constructed on a single monolithic chip utilizing P-channel enhancement mode transistors.

The memory is available with custom character coding or preprogrammed with ASCII encoded characters having the fonts shown on Page 2 of this data sheet.

BLOCK DIAGRAM



14

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GG} and V_{DD} with respect to V_{CC} . . . . . −20V to +0.3V
Inputs with respect to V_{CC} . . . . . −20V to +0.3V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±0.25 Volts (V_{CC} is the substrate voltage)
V_{GG} = −12 Volts ±0.6 Volts
V_{DD} = GND
Operating Temperature (T_A) = 0°C to +70°C
One TTL load (C_L total = 15 pF)

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Inputs (Note 1)						
Logic 1 Level	V_{IH}	V_{CC}−1.5	—	—	Volts	
Logic 0 Level	V_{IL}	—	—	+0.8	Volts	
Leakage	I_{LI}	—	—	10	μA	$V_{in} = V_{CC}$−6V, T_A = 25°C
Count Control						
÷6 Operation	V_{ICC}	−12.6	−12.0	−11.4	Volts	Returned to V_{GG} for ÷ 6 operation.
÷ 7 Operation	V_{ICC}	+4.75	+5.0	+5.25	Volts	Returned to V_{CC} for ÷ 7 operation
Leakage	I_{LCC}	—	—	10	μA	$V_{in} = V_{CC}$ − 6V, T_A = 25°C
Outputs (Note 2)						
Logic 1 Level	V_{OH}	2.8	—	—	Volts	I_{OH} = 100 μA
Logic 0 Level	V_{OL}	—	—	0.4	Volts	I_{OL} = 1.6 mA
Power						
Supply Current	I_{GG}	—	20	40	mA	Outputs unconnected,
Supply Current	I_{SS}	—	20	40	mA	f_{clk} = 200 KHz
AC CHARACTERISTICS						
Counter Clock						
Frequency	f_{clk}	DC	—	200	KHz	
Pulse Width	$t_{clk(0)}$	2.0	—	—	μs	
Pulse Delay	$t_{clk(1)}$	2.0	—	—	μs	$t_{r(clk)} + t_{clk(0)} + t_{r(clk)}$
Rise and Fall Times	$t_{r(clk)}, t_{f(clk)}$	—	—	100	ns	$+t_{clk}(0) \geqslant 5\mu$sec
Counter Reset						
Pulse Width	t_{rp}	1.0	—	—	μs	
Pulse Delay	t_{crd}	0.4	—	—	μs	Note (3)
Capacitance (Note 1)	C_{in}	—	—	10	pF	1 MHz, T_A = +25°C
Outputs						
Address to Output Delay	t_{AO}	—	1.0	1.5	μs	
Clock to Output Delay	t_{CO}	—	1.0	1.5	μs	
Clock to Counter Output Delay	t_{CCO}	—	1.0	1.5	μs	
Blanking/Unblanking Delay	t_{BO}	—	1.0	1.5	μs	
Output Enable/Disable Delay	t_{OEO}	—	1.0	1.5	μs	
Counter Reset Delay	t_{CRO}	—	1.0	1.5	μs	
Reset to Counter Output Delay	t_{CRCO}	—	1.0	1.5	μs	
Output Rise and Fall Time	t_r, t_f	—	—	0.3	μs	

**Typical values are at +25°C and nominal voltages.

NOTES:
1. These parameters apply to the character address, counter clock, counter reset, blanking, and output enable inputs.
2. These parameters apply to both the data outputs and counter output.
3. The counter clock must not make a negative transition within the period t_{crd}, before or after a positive counter reset transition. The counter reset negative edge may occur any time.

OPERATING DESCRIPTION

Character selection is achieved by presenting a six-bit binary word at the Character Address inputs. Column selection is achieved by clocking an internal counter from the Counter Clock input. Column information appears sequentially at the seven Data Outputs, beginning with the left-most column.

Two additional column positions, aside from the five required for character presentation, are available for spacing between adjacent characters. The Count Control input is used to determine whether one or both positions will be used. Between characters, the Data Outputs are high (+5V), the "no-dot" condition. The Counter Reset input is available to reset the counter into the last (sixth or seventh) state.

The Counter Output is provided to synchronize other system components to the ROM internal counter. An output appears corresponding to the last (sixth or seventh) counter state and can be conveniently used to clock an external input data register.

The Blanking Input allows all Data Outputs to be driven high (+5V) without affecting any other ROM function. Data Outputs can also be open-circuited for wire-ORed operation by use of the Output Enable input.

Memory operation is static; refresh clocks are not required to maintain output information. The Counter Clock input is used only to select columns and need not be pulsed continuously.

OPERATING NOTES

The following table summarizes the RO-2240S input control states and corresponding drive levels:

Count Control
÷6 ..... −12
÷7 ..... +5V

Counter Reset
Operate ..... +5V
Reset ..... OV

Blanking Input
Unblank ..... +5V
Blank* ..... OV

Output Enable
Enable ..... +5V
Disable** ..... OV

* All data outputs high (+5V)
**All data outputs open-circuited

TIMING DIAGRAMS

Timing diagram (1) shows the time relationships between character address, data output, counter clock and counter output during typical operation of an RO-5-2240S character generator. An output sequence from the RO-5-2240S-001 is shown to help clarify operation. This sequence can be seen from the top rows (OUT_1) of the characters "I" and "N".

	"I"						"N"				
OUT_1	1	0	0	0	1	1	1	0	1	1	1	0
	1	1	0	1	1	1	1	0	1	1	1	0
	1	1	0	1	1	1	1	0	0	1	1	0
	1	1	0	1	1	1	1	0	1	0	1	0
	1	1	0	1	1	1	1	0	1	1	0	0
	1	1	0	1	1	1	1	0	1	1	1	0
OUT_7	1	0	0	0	1	1	1	0	1	1	1	0
	COUNT OF 7											

All timing relationships shown in diagram (1) apply to any other output or combination of characters as well.

Relevant input conditions assumed but not shown in timing diagram (1) are as follows:

Count Control, +5V
Counter Reset, +5V
Blanking Input, +5V
Output Enable, +5V

Had the Count Control input been at −12V, the counter sequence would have been six positions instead of seven and the Counter Output would have been high during the sixth position.

New character addresses are shown coinciding with the rising edge of the Counter Output waveform in diagram (1). This condition was selected to demonstrate use of the Counter Output to advance an external input register to a new character address. Character addresses can be changed at any other time as well. Timing diagram (2) depicts output response to a character address change when, for example, the counter is stationary in one of the five character column positions.

Timing diagrams (3) through (6) show timing relationships for the Counter Reset, Blanking Input, and Output Enable. The "open" condition in (6) implies that both the pull-up and pull-down devices in each data output push-pull buffer are turned off.

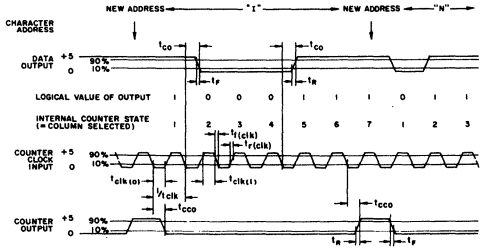


Fig.1

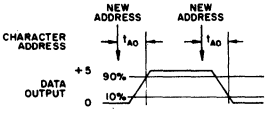


Fig.2

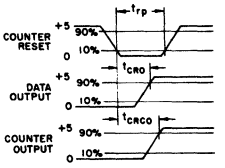


Fig.3

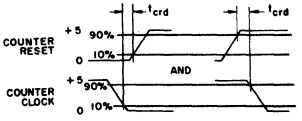


Fig.4

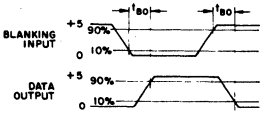


Fig.5

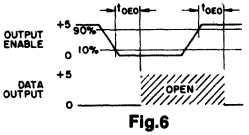


Fig.6

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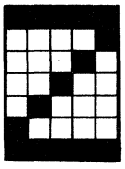
CODING AND CHARACTER FONTS

The RO-5-2240S-001 is a pre-programmed member of the RO-5-2240S series with ASCII encoding and the character fonts shown on the right. A logic "1" represents an input or output voltage equal to V_{SS} (+5V) and a logic "0" represents a voltage equal to V_{DD} (0V).

An example demonstrating the correspondence of device outputs and sequence to the 5×7 dot matrix fonts is shown below:

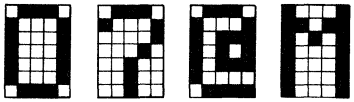
	1	2	3	4	5
OUT_1 →	0	0	0	0	0
OUT_2 →	1	1	1	1	0
OUT_3 →	1	1	1	0	1
OUT_4 →	1	1	0	1	1
OUT_5 →	1	0	1	1	1
OUT_6 →	0	1	1	1	1
OUT_7 →	0	0	0	0	0

output sequence



The RO-5-2240S-002 is pre-programmed with a character font identical to the font for the RO-5-2240S-001 below with the exception of the characters '0', '?', '@', and 'M'.

The RO-5-2240S-002 font for these characters is shown below:



RO-5-2240S-001

A_4	A_3	A_2	A_1	ROW	A_6 A_5 = 1 0 (COL 2)	1 1 (COL 3)	0 0 (COL 4)	0 1 (COL 5)
0	0	0	0	0				
0	0	0	1	1				
0	0	1	0	2				
0	0	1	1	3				
0	1	0	0	4				
0	1	0	1	5				
0	1	1	0	6				
0	1	1	1	7				
1	0	0	0	8				
1	0	0	1	9				
1	0	1	0	10				
1	0	1	1	11				
1	1	0	0	12				
1	1	0	1	13				
1	1	1	0	14				
1	1	1	1	15				

Character Generator

FEATURES

- 64×8×5 Organization — ideal for systems requiring a row scan 5×7 dot matrix character generator
- Single +5 Volt Supply
- TTL Compatible — all inputs and outputs
- Static Operation — no clocks required
- 450ns Maximum Access Time
- 175mW Maximum Power
- Three-State Outputs — under the control of an 'Output Inhibit' input to simplify memory expansion
- Standard ASCII (RO-3-2513/CGR-001) or Totally Automated Custom Programming Available
- Zener Protected Inputs
- Glass Passivation Protection

DESCRIPTION

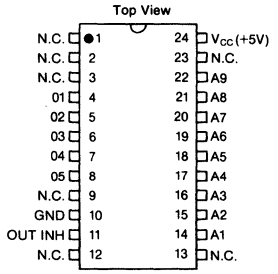
The General Instrument RO-3-2513 is a 2560 bit static Read-Only Memory organized as 512 five bit words and is ideally suited for use as a Character Generator. Fabricated in GI's advanced GIANT II N-channel Ion-Implant process to enable operation from a single +5 Volt power supply, the RO-3-2513 can store, for high speed raster scan CRT displays, a full 64 characters in a standard 5×7 dot matrix format.

The RO-3-2513 is available pre-programmed with ASCII encoded 5×7 characters (GI part no. RO-3-2513/CGR-001) a direct replacement in pin connection, operation, and character font for the Signetics 2513/CM2140.

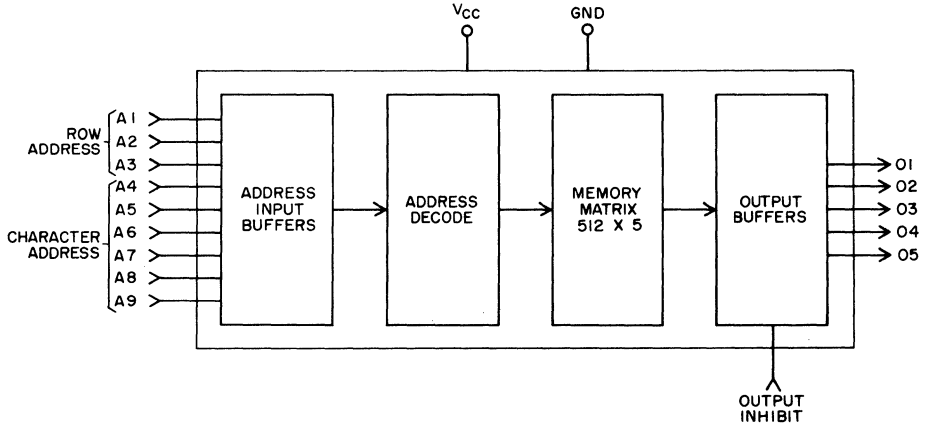
A separate publication, "RO-3-2513 Custom Coding Information," available from GI Sales Offices, describes the punched card and truth table format for custom programming of the RO-3-2513 memory.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage to this device. Functional operation at these conditions is not implied—operating conditions are specified below.

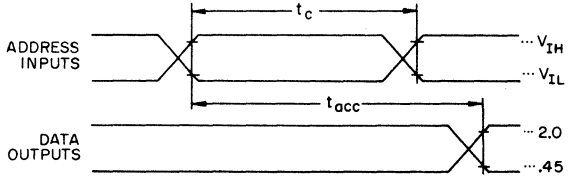
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±5%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL load, $C_{L\ TOTAL}$ = 50pF.

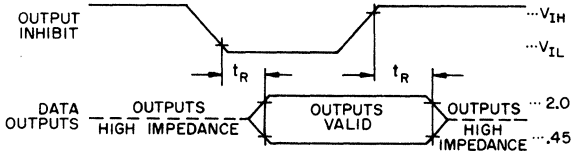
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Output Inhibit Inputs						
Logic "1"	V_{IH}	2.2	—	—	V	
Logic "0"	V_{IL}	—	—	0.65	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.2	—	—	V	I_{OH} = 100μA
Logic "0"	V_{OL}	—	—	0.45	V	I_{OL} = 1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current						
I_{CC}	—	—	25	33	mA	Outputs open
AC CHARACTERISTICS						
Inputs						
Cycle Time	t_C	400	—	—	ns	
Capacitance	C_I	—	5	8	pF	f = 1MHz
Data Outputs						
Access Time	t_{ACC}	75	250	450	ns	
Inhibit Response Time	t_R	—	150	200	ns	
Capacitance	C_O	—	8	10	pF	f = 1MHz

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS



A. ACCESS TIME (ADDRESS TO OUTPUT-OUTPUT INHIBIT AT LOGIC '0')



B. INHIBIT RESPONSE TIME (ADDRESS INPUTS STABLE)

RO-3-2513-001 STANDARD PATTERN CHARACTER FORMAT

The RO-3-2513/CGR-001 is a pre-programmed version of the RO-3-2513 series with ASCII encoding and the character font shown below. A logic "1" represents an input or output voltage nominally equal to Vcc(+5V) and a logic "0" represents a voltage nominally equal to GND (0V).

An example demonstrating the correspondence of device outputs and addressing sequence to the 5×7 dot matrix font is shown below:

CHARACTER ADDRESS

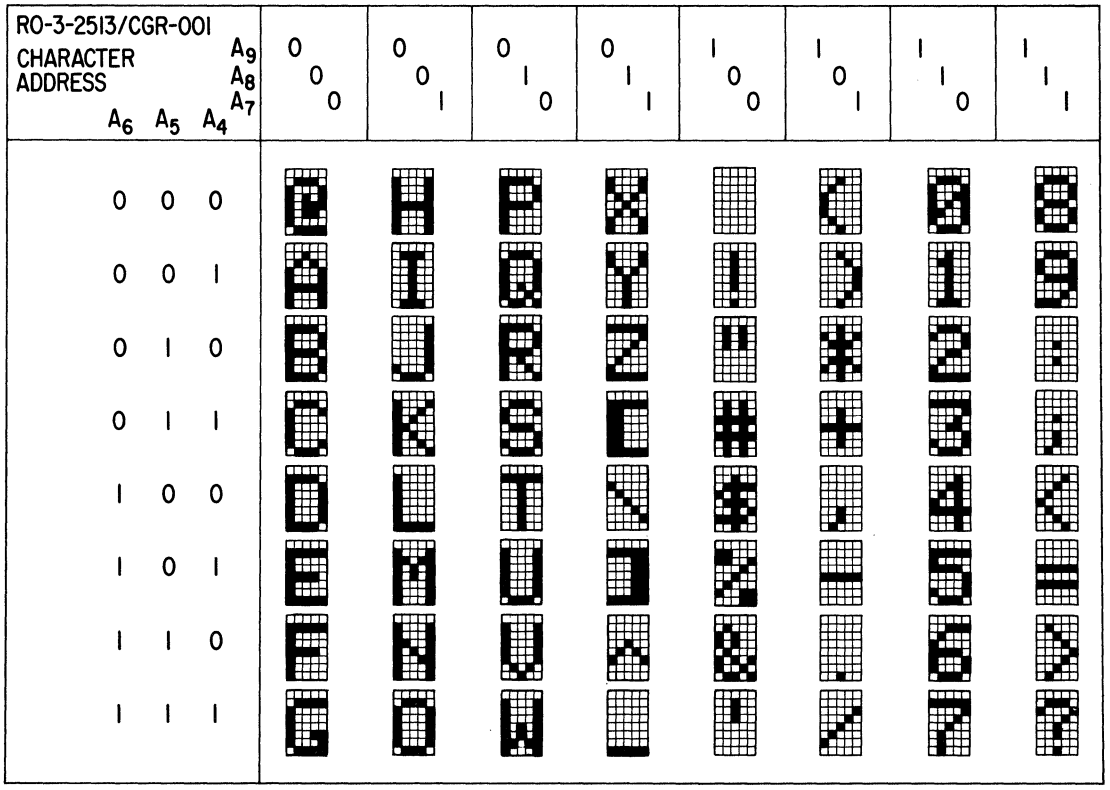
RO-3-2513/CGR-001 ADDRESS BIT	A9	A8	A7	A6	A5	A4
ASCII BIT	6	5	4	3	2	1
ASCII 'S' CHARACTER	0	1	0	0	1	1

ROW ADDRESS

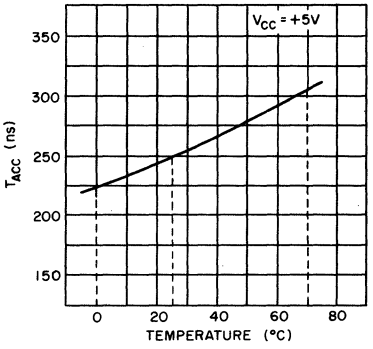
A_3	A_2	A_1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

OUTPUTS

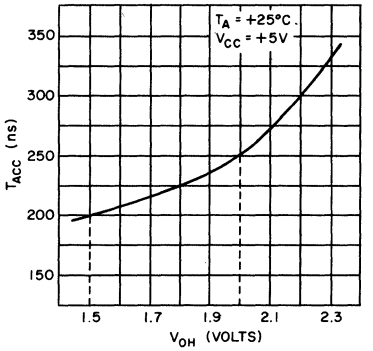
O_5	O_4	O_3	O_2	O_1
0	0	0	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	0	0
0	1	1	1	0
0	0	0	0	1
1	0	0	0	1
0	1	1	1	0



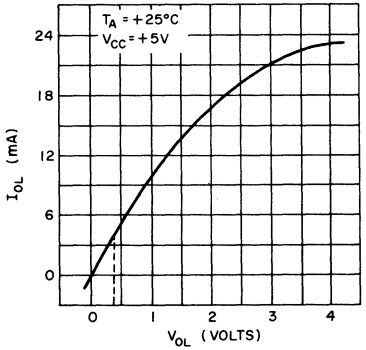
TYPICAL CHARACTERISTIC CURVES



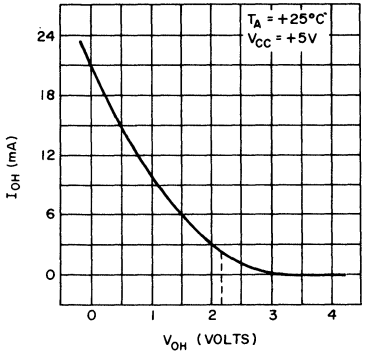
ACCESS TIME vs. TEMPERATURE



ACCESS TIME vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

Character Generator

FEATURES

- Designed to drive Needle Printers.
- Internal counter provides sequential column scanning.
- Forward/Reverse Control for left to right and right to left printing capability.
- Carry Output available for synchronization.
- Three-State output configuration.
- Two mask programmable Output Enable pins to allow memory expansion.
- ASC II coded standard part, RO-5-5184-3000.
- Mask programmable counter length to allow flexibility in character organization.

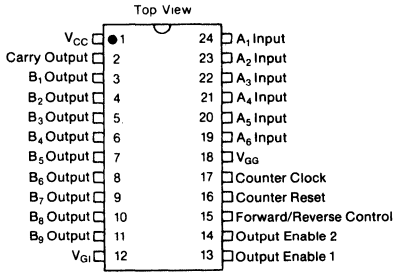
DESCRIPTION

The RO-5-5184 is a 5184 bit Static Read Only Memory organized as 64 permanent storage locations of 81 bits each (9×9 character matrix). Six address lines are used for the selection of 64 different characters. An internal ring counter is provided for column scanning; column information appears sequentially on the 9 output lines. A Counter Reset Input is available to initialize the sequential scanning. A Carry Output is provided to synchronize external circuitry to the internal column counter. The Forward/Reverse Control allows scanning from left to right or from right to left.

The 9 output lines have tri-state configuration. Two mask programmable Output Enable pins are provided for expansion up to a 5184 × 4 bit system without external logic.

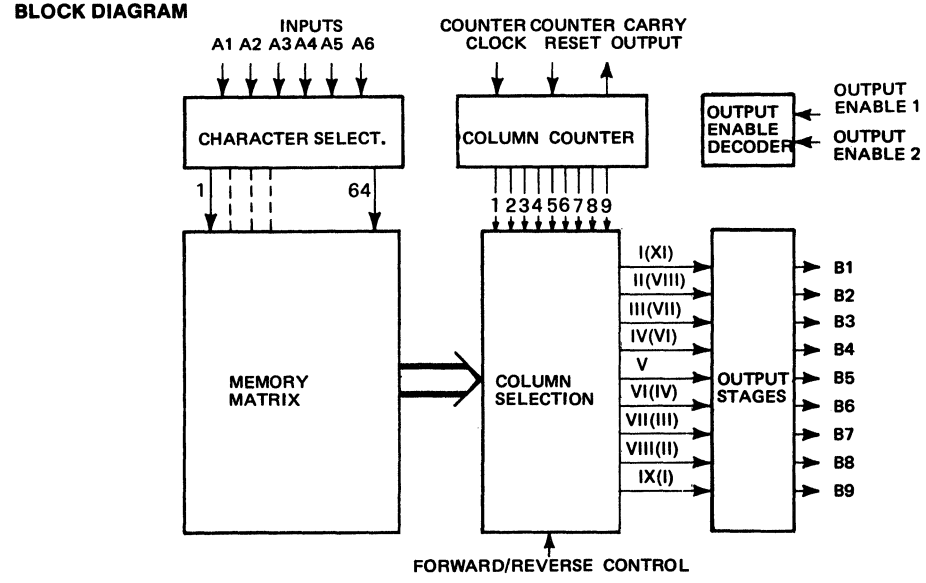
PIN CONFIGURATION

24 LEAD DUAL IN LINE



Low threshold P-channel enhancement mode metal gate technology is used for input/output direct TTL compatibility. All inputs are zener protected.

BLOCK DIAGRAM



14

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{CC} . . . . . −20V to +0.3V
Temperature Range . . . . . −55°C to +125°C
Operating Temperature . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage to this device. Functional operation at these conditions is not implied — operating conditions are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5V ±0.5V
V_{GI} = GND
V_{GG} = −12V ±1V

Characteristics apply over temperature range unless otherwise stated.

Characteristic	Min	Typ**	Max	Units	Conditions
Counter Clock Input					
Repitition Rate	D.C.	350	200	KHz	
Pulse Width, ϕw	1.2	—	—	μSec	At a logic '1' level
Pulse Separation, ϕs	1.2	—	—	μSec	At a logic '0' level
Rise & Fall Times, tr, tf	—	—	1.0	μSec	
Logic '0' Level, V_{IL}	—	—	+0.8	Volts	
Logic '1' Level, V_{IH}	V_{CC}−1.5	—	—	Volts	
Input Leakage, I_{IN}	—	—	10	μA	Measured at $V_{IN} = V_{CC}$−10V at 25°C
Input Capacitance, C_{IN}	—	10	—	pF	$V_{IN} = V_{CC}$, f = 1MHz
Address Inputs					
Logic '0' Level, V_{IL}	—	—	+0.8	Volts	
Lotic '1' Level, V_{IH}	V_{CC}−1.5	—	—	Volts	
Input Leakage, I_{IN}	—	—	10	μA	Measured at $V_{IN} = V_{CC}$−10V at 25°C
Input Capacitance, C_{IN}	—	10	—	pF	$V_{IN} = V_{CC}$, f= 1MHz
Reset Input					
Counter Clock to Reset					
Pulse delay, t_{CRD}.	1.0	—	—	μSec	Fig.1
Reset pulse width	3.0	—	—	μSec	Fig.2
Data Outputs					
Logic '0' Level, V_{OL}	—	—	0.4	Volts	I_{OL} = 1.6mA
Logic '1' Level, V_{OH}	V_{CC}−1.0	—	—	Volts	I_{OH} = 100 μA
Clock to Output delay time, t_{CO}	—	2.5	3.5	μSec	
Clock to Carry Output delay time, t_{CC}	—	1.5	2.5	μSec	Figs. 3,4,5,6,7, & 8
Address to Output delay time, t_{AO}	—	2.5	3.5	μSec	1 TTL, 10pF load
Reset to Output delay time, t_{RES}	—	2.5	5.0	μSec	T_A = 25°C
Forward/Reverse to Output delay time, t_{FRO}	—	2.5	3.5	μSec	
Output Enable delay time, t_{OEO}	—	1.5	2.5	μSec	
Power Consumption, P_D	—	250	—	mW	T_A = 25°C

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS

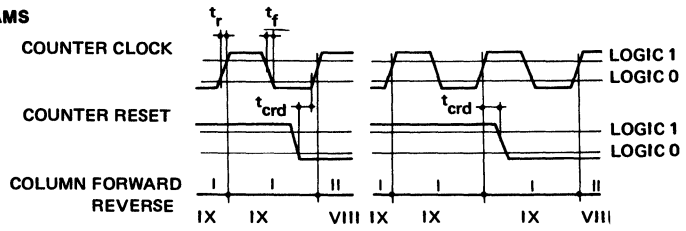


Fig.1 CLOCK TO RESET DELAY TIME

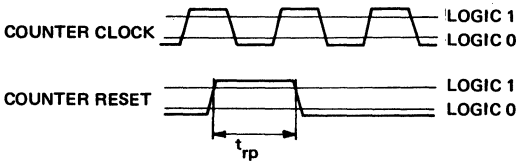


Fig.2 RESET PULSE WIDTH

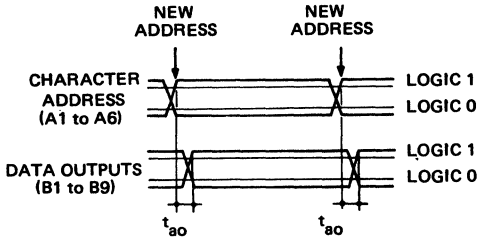


Fig.3 ADDRESS TO OUTPUT DELAY TIME

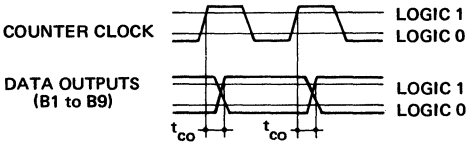


Fig.4 CLOCK TO OUTPUT DELAY TIME

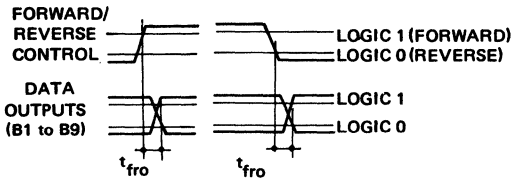


Fig.5 FORWARD/REVERSE TO OUTPUT DELAY TIME

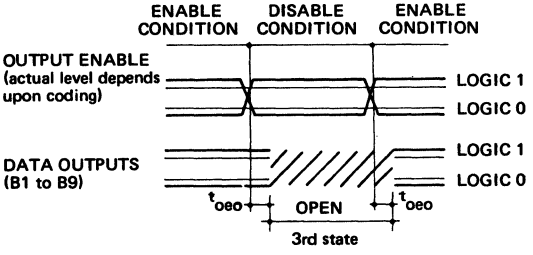


Fig.6 OUTPUT ENABLE TO OUTPUT DELAY TIME

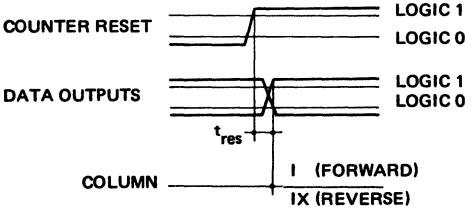


Fig.7 RESET TO OUTPUT DELAY TIME

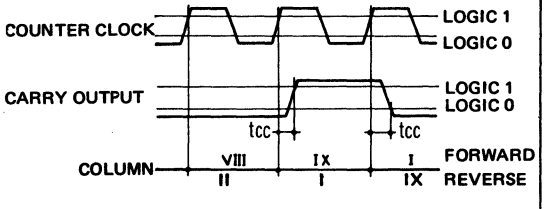


Fig.8 CLOCK TO CARRY DELAY TIME

14

OPERATION

CHARACTER SELECTION

Six address inputs are provided for selection of the 64 different characters. The address inputs are binary weighted (A_I is the LSB).

COLUMN SELECTION

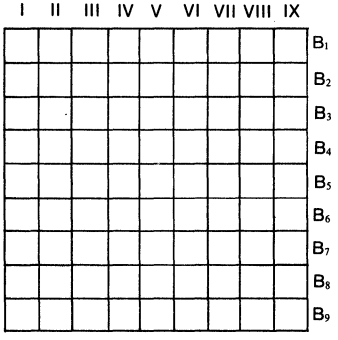
Column selection depends upon Forward/Reverse Control which permits the scanning of characters either from the first (I) to the last (IX) or from the last (IX) to the first (I) column as shown in fig.9. By changing line by line the logic value of Forward/Reverse control printing alternatively left to right or right to left is possible (see fig.10).

This feature allows faster printing by eliminating the fly back dead time between lines. The logic level of Forward/Reverse Control has to be constant "1" for left to right scanning and constant "0" for right to left scanning.

Fig.9 COLUMN SELECTION

FORWARD				REVERSE			
Count Reset	Column Count. State	Charact. Column	Carry Outp.	Count Reset	Column Count. State	Charact. Column	Carry Outp.
0	1	I	0	0	1	IX	0
0	2	II	0	0	2	VIII	0
0	3	III	0	0	3	VII	0
0	4	IV	0	0	4	VI	0
0	5	V	0	0	5	V	0
0	6	VI	0	0	6	IV	0
0	7	VII	0	0	7	III	0
0	8	VIII	0	0	8	II	0
0	9	IX	1	0	9	I	1
0	1	I	0	0	1	IX	0
0	2	II	0	0	2	VIII	0
—	—	—	—	—	—	—	—
—	—	—	—	—	—	—	—
—	—	—	—	—	—	—	—
0	8	VIII	0	0	8	II	0
0	9	IX	1	0	9	I	1
1	1	I	0	1	1	IX	0
1	1	I	0	1	1	IX	0
1	1	I	0	1	1	IX	0

CHARACTER MATRIX



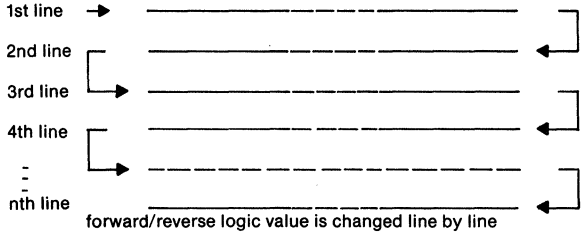


Fig.10 FORWARD/REVERSE PRINTING

OUTPUT ENABLE DECODER

Two Output Enable lines are provided for chip selection, when a chip is not selected the outputs are disabled (high impedance).

Output Enable signals are internally decoded by a mask programmable decoder to minimize logic for memory expansion.

The output enable code assigned to different RO-5-5184 is permanently programmed into the ROM at the same time as the custom data pattern.

A system of $4 \times 5184 = 20736$ bit character generator needing no external enable logic is easily obtained wiring the outputs of four different RO-5-5184 together as shown on fig.11.

OUTPUT ENABLE CODING						
RO-5-5184	Output Enable 1	Output Enable 2	DEVICE SELECTION			
			A	B	C	D
A	0	0	selected	—	—	—
B	1	0	—	selected	—	—
C	0	1	—	—	selected	—
D	1	1	—	—	—	selected

COLUMN COUNTER

This counter operates on the positive going edges of the Counter Clock.

Each counter cell is implemented with a cross coupled flip-flop so that the counter position is fully static.

Carry Output is active (logic '1') when the counter is in the last position, to indicate that a character has been fully scanned.

When active (logic '1') the Counter Reset Input resets the counter in the first position to initialise the scanning.

The counting length is mask programmable, it is possible to program any length between five and nine.

OUTPUT STAGES

Nine TTL compatible Outputs (B_1 to B_9) are provided to show the memory content.

The Tri-state configuration of output stages allows bus structure for memory expansion under the control of Output Enable signals.

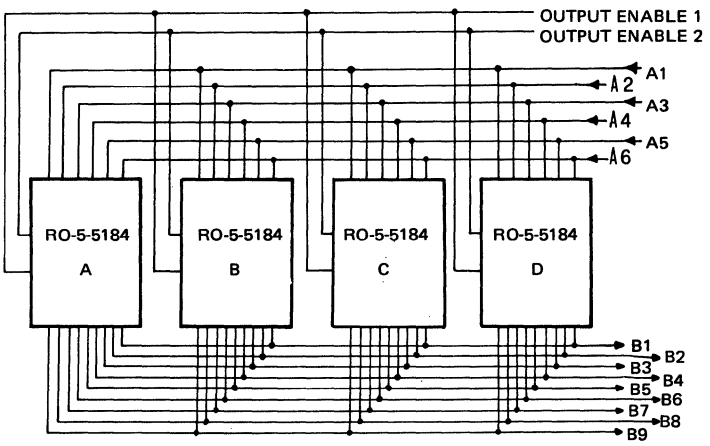
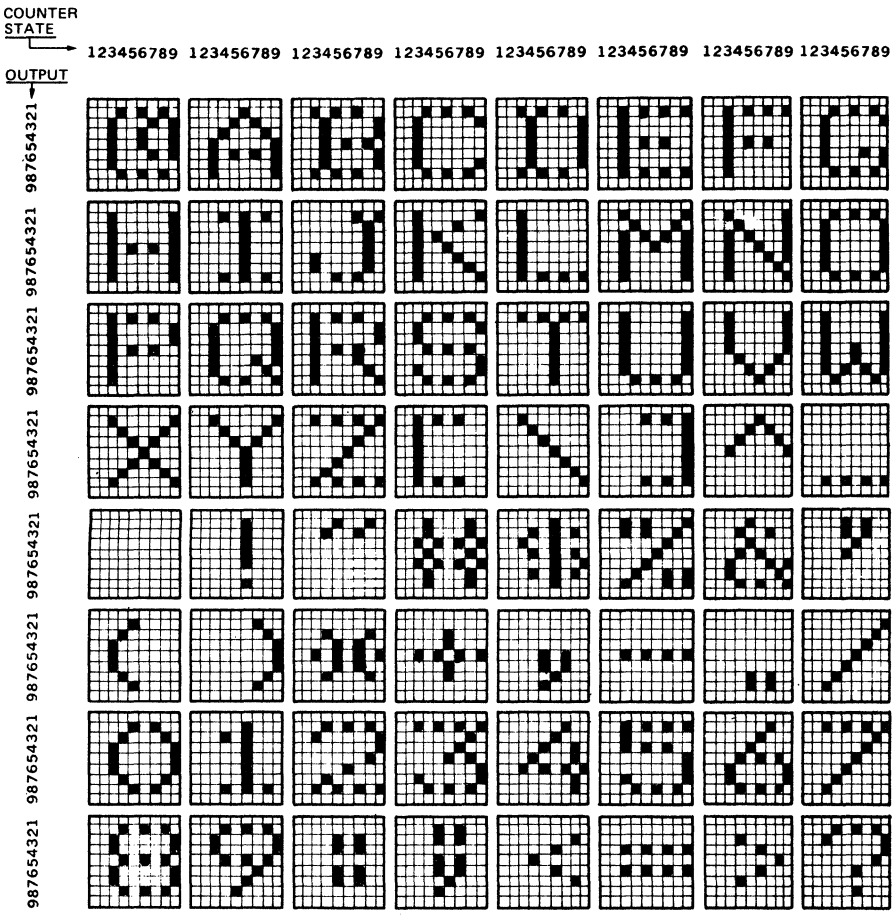


Fig. 11

RO-5-5184-050 STANDARD PATTERN CHARACTER FORMAT

INPUT ADDRESS									
	A 1	0	1	0	1	0	1	0	1
	A 2	0	0	1	1	0	0	1	1
	A 3	0	0	0	0	1	1	1	1



SHADED SQUARE	+5	0
BLANK SQUARE	0	+5
DESIRED OUTPUT VOLTAGE	X	

OUTPUT ENABLE 1	0	+5	0	+5
OUTPUT ENABLE 2	0	0	+5	+5
DEVICE SELECTED	X			

RO-5-5184-3000 STANDARD PATTERN CHARACTER FORMAT

INPUT ADDRESS									
	A 1	0	1	0	1	0	1	0	1
	A 2	0	0	1	1	0	0	1	1
	A 3	0	0	0	0	1	1	1	1

A6 A5 A4

COUNTER STATE → 123456789 123456789 123456789 123456789 123456789 123456789 123456789 123456789

OUTPUT ↓ 987654321

000

001

010

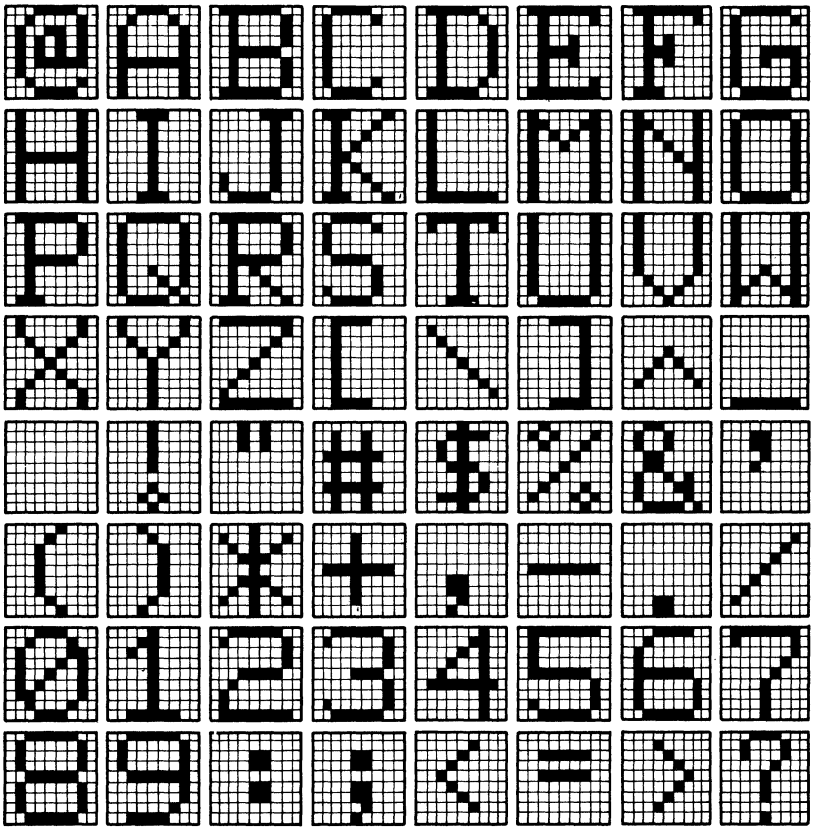
011

100

101

110

111

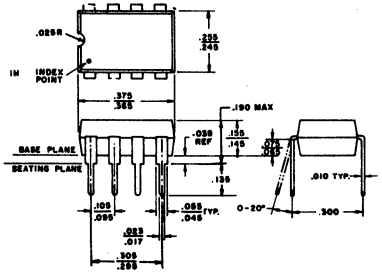


SHADED SQUARE	+5	0
BLANK SQUARE	0	+5
DESIRED OUTPUT VOLTAGE		×

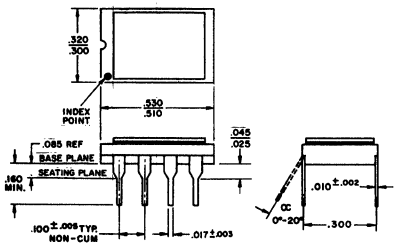
OUTPUT ENABLE 1	0	+5	0	+5
OUTPUT ENABLE 2	0	0	+5	+5
DEVICE SELECTED				×

PACKAGE OUTLINES / SALES OFFICES

8 LEAD DUAL IN LINE

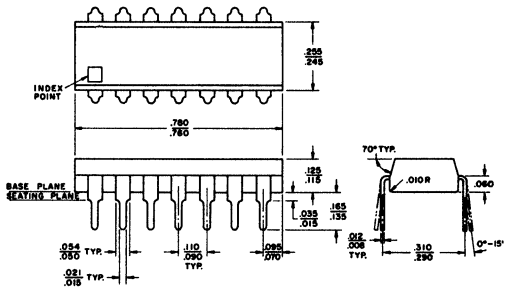


PLASTIC

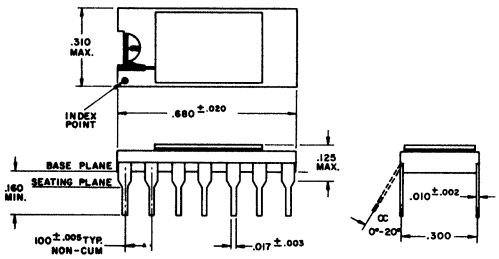


CERAMIC

14 LEAD DUAL IN LINE

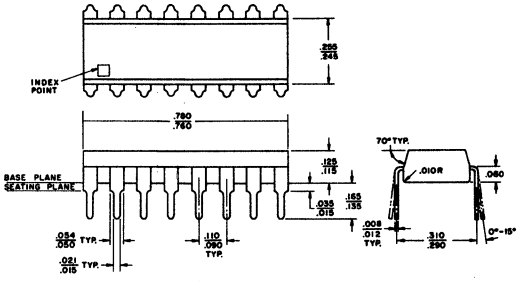


PLASTIC



CERAMIC

16 LEAD DUAL IN LINE



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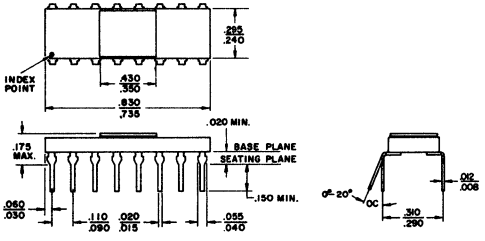
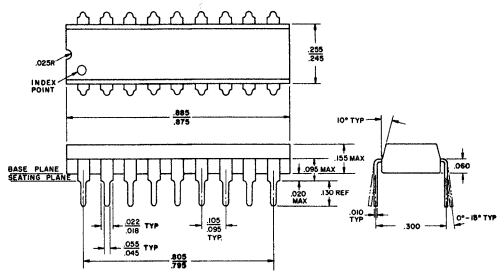


CERAMIC

15

PACKAGE OUTLINES

18 LEAD DUAL IN LINE



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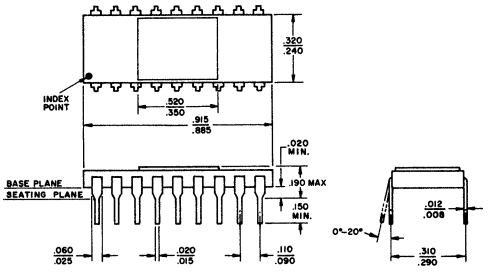
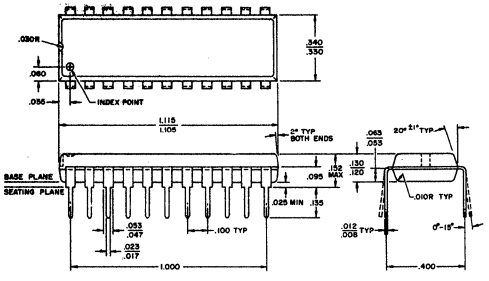


CERAMIC

22 LEAD DUAL IN LINE



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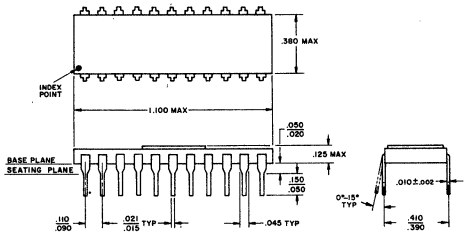
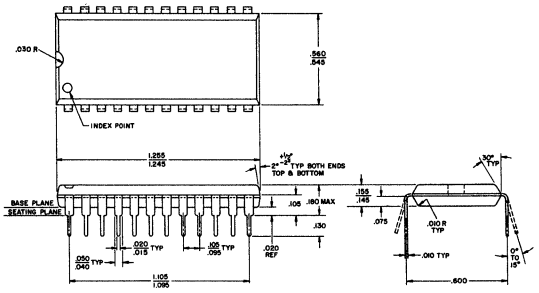


CERAMIC

24 LEAD DUAL IN LINE



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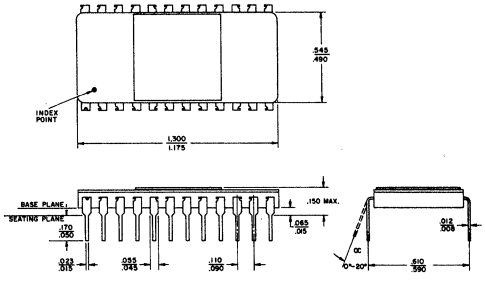
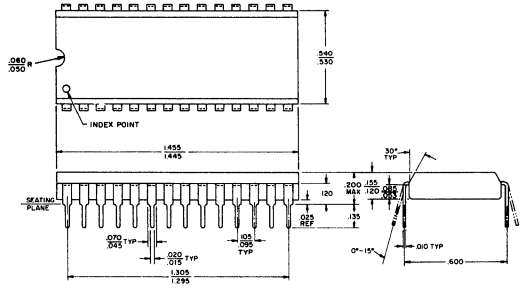


CERAMIC

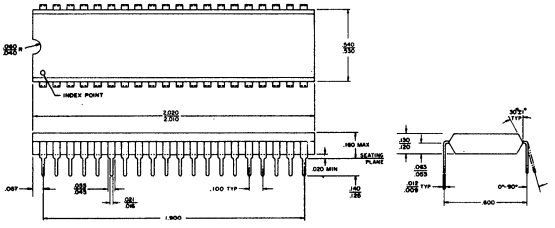
28 LEAD DUAL IN LINE



PLASTIC

CERAMIC

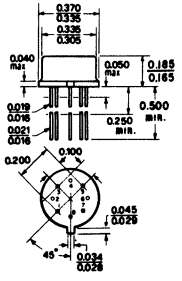
40 LEAD DUAL IN LINE



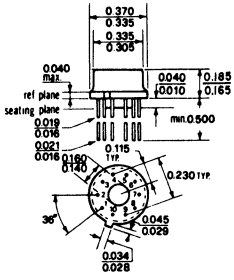
PLASTIC

CERAMIC

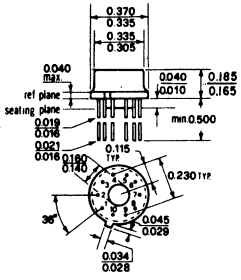
8 LEAD (.200 P.C.)



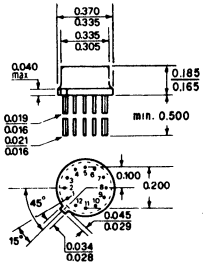
8 LEAD (.230 P.C.)



10 LEAD



12 LEAD



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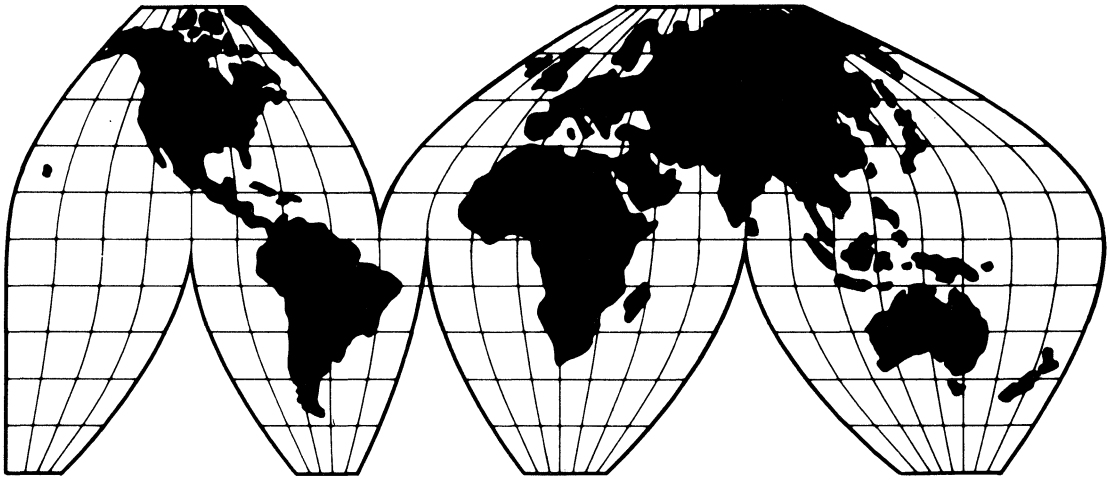

SALES REPRESENTATIVES

UNITED STATES

ALABAMA

20th Century Marketing
P.O. Box 6127—Hertz Sky Ctr.
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El Segundo, CA 90245
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PM Sales
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CONNECTICUT

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7315 Ashcroft
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Lenert
1420 Hutchins Avenue
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2150 South 300 West
Salt Lake City, UT 84115
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Diplomat
2280 South Main St.
Salt Lake City, UT 84115
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Telex: 02-29697

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Future Electronics Corp.
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Portsmouth
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Semicomps Ltd.
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St. Albans, Herts
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Semiconductor Specialists Ltd.
Premier House, Fairfield Road
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SOUTH AFRICA

Metlionics (PTY) Ltd.
P.O. Box 39690
Bramley 2018
Tel: 40-7746, Telex: 43-4852

TERMS OF SALE

1. INVOICE TERMS

(a) All orders are subject to the final acceptance by Seller's credit department.

(b) All shipments are F.O.B., Seller's plant, unless otherwise stated hereon.

(c) The Seller reserves the right to make shipments in part or in whole, and the Seller's Invoices for such shipments shall be accepted and paid as rendered without regard to whether or not the balance of the order is shipped.

2. PRICES

(a) Prices are based upon shipments being made F.O.B. Seller's plants.

(b) Prices do not include any Municipal, State, or Federal sales, use, excise or similar taxes. Consequently, in addition to the prices specified, the amount of any present or future sales, use, excise, or any other tax that may be imposed shall be paid by the Purchaser, or in lieu thereof the Purchaser will provide the Seller with a tax exemption certificate acceptable to the taxing authorities.

(c) The price of the merchandise covered by this order is based upon the Seller's interpretation of the Purchaser's specifications.

(d) The Seller reserves the right to invoke a minimum billing charge of $100.00.

(e) Seller reserves the right to invoke a minimum cancellation charge of $50.00.

3. DELIVERY SCHEDULE

(a) Dates of shipment are approximate and are subject to the Seller's ability to conform to same, but Seller shall not incur any liability, consequential or otherwise, due to delay or failure to deliver for any reason. All orders are accepted subject to delays occasioned by labor, strikes, fires, war, or floods, accidents at factory, or any causes whatever beyond the Seller's control. Delivery schedules are predicated upon the Seller's ability to acquire materials, tools, dies and equipment, where necessary. In the event of any such delay beyond the Seller's control, the date of delivery of this order shall be extended by a period approximately equal to the time lost by reason of the delays.

(b) If the Seller does not receive a schedule from the Purchaser promptly, the rate and schedule of shipments will be set by the Seller.

(c) Subject to change, based upon delay in prompt receipt of approval of sample.

(d) Subject to change upon any modification of specifications previously agreed upon, or delay in submission of specification acceptable to Seller.

(e) Seller reserves the right to overship or undership a quantity totalling 5% of the last scheduled release of any order for non-standard parts.

4. SHIPMENT

(a) Unless specified the Seller will select the mode of transportation and the Seller will not be responsible for differences in cost between one mode and another.

(b) The Seller is not responsible for damage or loss in transit and any such claims are to be placed by the Purchaser with the carrier, where shipment is made F.O.B. Seller's plant.

5. INSPECTION AND ACCEPTANCE

(a) It is understood that the conditions of the Purchaser's inspection or test of the material covered by this order shall be mutually agreed upon and the Seller reserves the right to inspect any material which the Purchaser claims to be defective on the Purchaser's premises and decide whether or not it should be replaced. Any required repairs which the Seller's inspection determines to be the Purchaser's responsibility will be made at the Purchaser's expense and at the Seller's option on the Purchaser's premises.

(b) If the material covered by this order is proven defective and the Seller was notified of such defects in writing within twenty days from the date of shipment, the Seller will be responsible only for the costs of repair or replacement of the Seller's product, and in no event will Seller be liable for any damage consequential or otherwise or for an amount in excess of the price (at the time of adjustment) of the defective item(s). The Seller will not be responsible for any charges resulting from the use of defective material.

(c) No material may be returned for credit and no material may be returned to the Seller for correction without the Seller's prior written approval, but if such unauthorized return shipments are made to the Seller, the Seller reserves the right to refuse the shipment or to accept it, and in the latter case, the shipment will be held as the Purchaser's property and without responsibility to the Seller.

(d) All claims, including claims for shortages must be made within five (5) days after receipt of shipment, except as otherwise contained in this Terms of Sale.

6. TOOLS

Payment of the Seller's charges for tools, dies, jigs, fixtures, etc. and/or equipment required for the production of this or other orders does not convey ownership of such items to the Purchaser nor the right to remove them from the Seller's plant, as such charges do not represent prices that would be charged for the sale of such items and oftentimes represent the costs of modifications and/or additions to standard tools or equipment.

7. CANCELLATION

Cancellation of this order for any reason whatsoever will be accepted only upon terms that will fully indemnify the Seller.

8. REMEDIES OF THE SELLER

(a) If, at the Purchaser's request or for any other reason for which the Purchaser is responsible, production or shipment of this order is held or delayed, the Seller reserves the right to immediately invoice the Purchaser for same in accordance with the provisions of Clause 7 above and payment is to be made promptly in accordance with this Terms of Sale. Should the Purchaser release the hold or remove the cause for delay and the Seller agrees to reinstate the order, the schedule of delivery will be set by the Seller in accordance with the requirements of the Seller's then existing factory schedule.

(b) If, in the Seller's judgment, the Purchaser's financial condition at any time does not justify continuance of production or shipment of the material covered by this or any other of the Purchaser's orders, the Seller reserves the right to require full or partial payment in advance and/or to withhold further shipments and stop production, in which case the conditions of Cancellation Clause 7 above will apply.

(c) If payment of the Seller's invoice(s) for shipments in part or in whole is not made promptly and in compliance with this Terms of Sale above, the Seller reserves the right to withhold further shipments and/or stop production and, at the Seller's option, to require full payment in accordance wih Clause 7 of this Terms of Sale. If, as a result of the purchaser's failure to pay the Seller's invoice(s) promptly, the Seller stops production of this order and later agrees to reinstate it, the scheduled rate of delivery will be set by the Seller in accordance with the requirements of the Seller's then existing factory schedule.

(d) If at any time prior to the date of initial production and/or shipment, of this order or at any subsequent time during the course of this order, there shall be filed by or against the Purchaser in any Court, pursuant to any statute either of the United States or of any State or Municipality a petition of bankruptcy or insolvency, or for reorganization, or for the appointment of a receiver or trustee of all or a portion of the Purchaser's property, or if the Purchaser makes an assignment for the benefit of creditors, this order shall ipso facto be cancelled and terminated and, in which event, neither the Purchaser nor any person claiming through or under the Purchaser or by virtue of any statute or an order of any Court shall be entitled to any rights of the Purchaser's order and the Seller reserves the right to impose all applicable conditions of this Terms of Sale, including Cancellation Clause 7 above, as well as to retain as partial liquidated damages any payments, security, deposits or monies received by the Seller from the Purchaser or others in the Purchaser's behalf against this order. Should the receiver, trustee, the operating committee, or other similar agency desire to reinstate this order or any uncompleted portion thereof, the Seller reserves the right to either refuse or accept such requests for reinstatement and, in the latter case, to determine what appropriate credits, if any, are to be issued to offset charges previously made as herein above in this clause provided for. If the Seller elects to reinstate the order it is subject to this Terms of Sale and the schedule and rate of delivery will be set by the Seller in accordance with the requirements of the Seller's then existing factory schedule.

(e) If the Seller accepts notes, trade acceptances or other paper as part or entire payment for this order, all shall become due at the Seller's option, upon default in the payment of any one of them, and the Seller reserves the right to impose the conditions of Cancellation Clause 7 above.

9. The terms and conditions of this order acknowledgment supersede the Purchaser's order, and no variation of this agreement shall be valid unless same be in writing signed by a duly authorized officer of the Seller.

10. General Instrument Corporation, warrants its devices against defects in material and workmanship for a period of ninety (90) days in the case of entertainment type devices, or one (1) year in case of all other devices, from the date of shipment provided they are used within their voltage and current limits and under conditions specified by General Instrument Corporation. Adjustments if any are subject to clauses 5(a), (b), and (c) of the Seller's Standard Terms of Sale, and devices returned to factory for adjustment must be shipped with all transportation charges prepaid.

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