MB86965

FUJITSU

ETHERCOUPLER CONTROLLER

ABBREVIATED DATA SHEET

BELL MICRO

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JGUST 1992

FEATURES

- Provides interface to the I/O bus of PC/XT™/AT® or compatible computers
- Optional, generic host interface to connect to industry-standard buses
- Interface to serial EEPROM for Node ID and option storage allows construction of jumperless adapter cards
- Allows automatic selection of nonconflicting I/O address for self-installing
- High-performance, packet-buffer architecture pipelines data for highest throughput
- On-chip buffer management unit controls buffer pointers to reduce software overhead and improve performance
- Hash filter for multicast packet reception
- Manchester encoder/decoder tolerates input jitter up to ±18 ns
- Fully compliant with ISO/ANSI/IEEE 8802-3 specifications
- Automatic AUI/10BASE-T selection
- Integrated pulse shaper, and transmit and receive filters
- Selectable 100 and 150Ω termination for shielded or unshielded twisted-pair cable
- Powerdown mode to reduce power dissipation in battery-powered equipment
- Low-power CMOS technology
- Single 5-volt power supply
- 160-pin plastic quad flat package (PQFP)

GENERAL DESCRIPTION

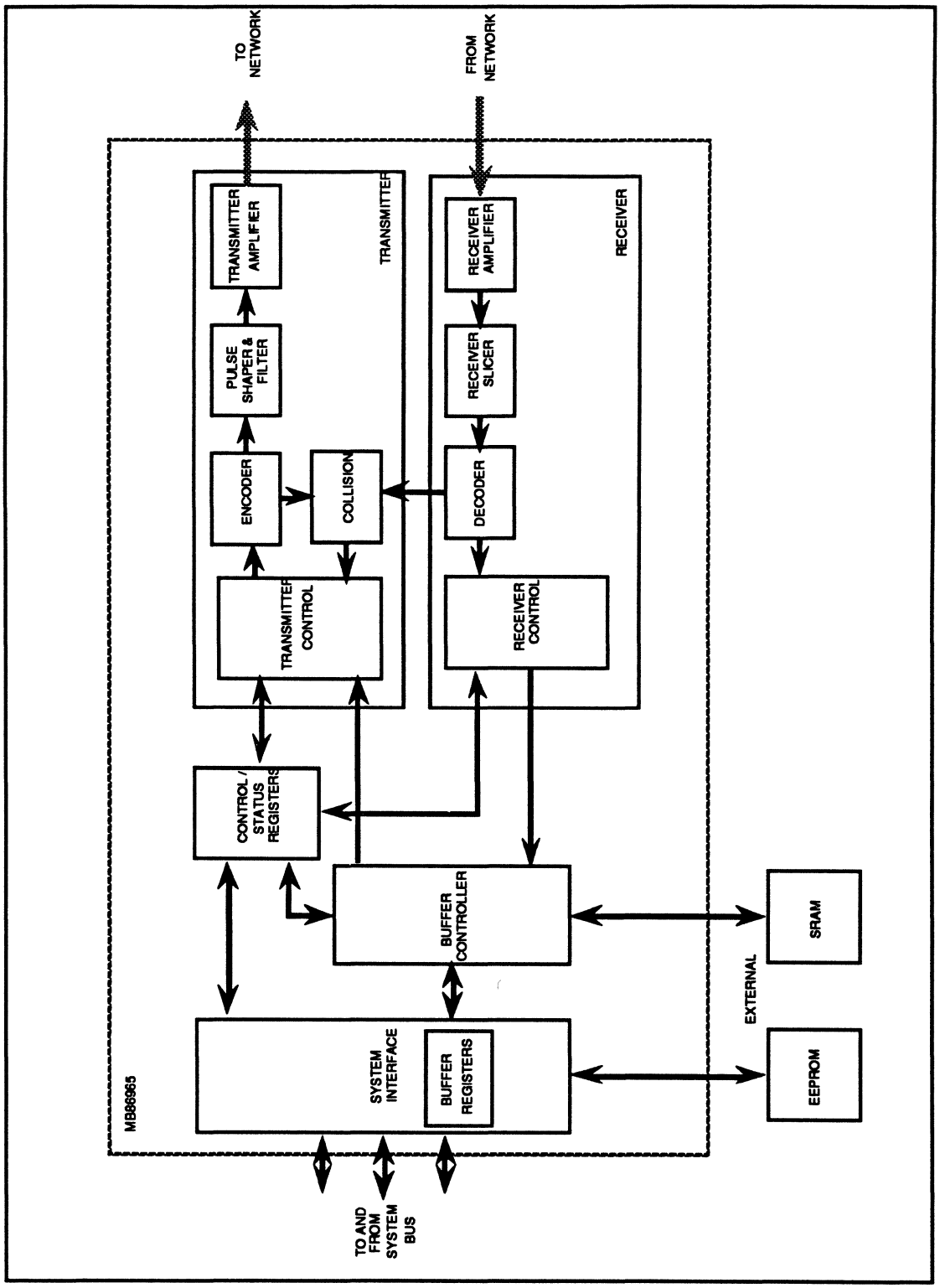
The MB86965 EtherCoupler Controller is a high-performance, highly integrated monolithic device that incorporates a network controller with buffer management, Manchester encoder/decoder, 10BASE-T transceiver with on-chip transmit and receive filters, and bus interface for a PC/XT/AT/ISA bus.

EtherCoupler allows implementation of adapter solutions with as few as four chips. With its optional native bus mode for use directly on a microprocessor bus, it is ideal for use on daughter and motherboards, as well as expansion-bus adapter boards.

An EEPROM can be interfaced to the chip for storage of Ethernet ID and configuration settings. EtherCoupler is designed to operate in a jumperless setting, thus eliminating the jumpers typically used to configure the system after applying power.

The buffer management architecture of the MB86965 allows packet data to access a buffer memory area simultaneously from the host and from the network media. The network controller updates all receive and transmit pointers internally to reduce the software overhead needed to control these operations, which results in superior benchmark speed and application performance.

EtherCoupler's transmit buffer is programmable as a single 2-kbyte bank or as two banks of 2, 4, or 8 kbytes each. This buffer chains multiple data packets and transmits them to the network from a single transmit command, thereby offering greater design flexibility and throughput. A ring buffer that can be sized from 4 to 62 kbytes, depending on the amount of available memory used for the transmit buffer, captures the receive packets.



Block Diagram

The MB86965 performs pulse shaping and filtering internally, which eliminates the need for external filtering components and reduces overall system cost. EtherCoupler is compatible with shielded and unshielded twisted-pair cables and provides outputs for receive, transmit, collision and link test LEDs. The twisted pair receive threshold can be reduced to allow an extended range between nodes in low-noise environments. Its wide range of features makes EtherCoupler the ideal device for 10BASE-T twisted-pair Ethernet.

Possible configurations for the system bus interface include I/O mapping, memory mapping and DMA access, or a combination of these. With a 20 Mbyte/s bandwidth, the EtherCoupler system bus interface allows use of full throughput capacity of its packet-buffering architecture. EtherCoupler bus modes are selectable, thereby providing big or little endian byte-ordering, permitting efficient data interface with most microprocessors and higher-level protocols.

The Fujitsu high-speed, low-power CMOS process is used to manufacture of the MB86965. The device is furnished in a 160-pin plastic quad flat package.

PIN CONFIGURATION

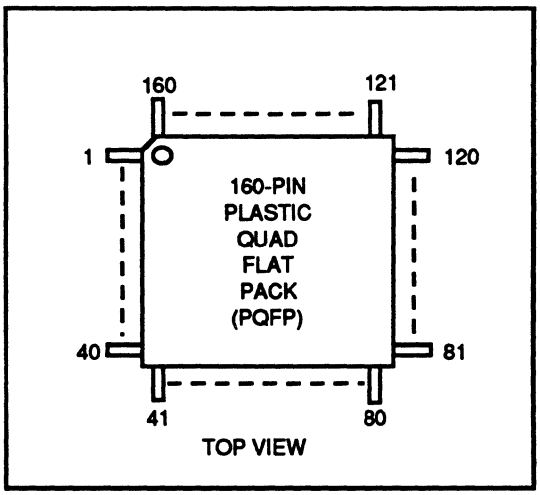


Figure 1 is a block diagram illustrating the application of the MB86965 in an add-in adapter card for an ISA bus-based personal computer. The serial EEPROM provides storage for I/O base address, boot PROM address and interrupt channel as well as the Ethernet node ID. One or two 8-bit bidirectional transceivers provide data buffering between the Ethercoupler and the 8- or 16-bit system bus. A single SRAM, typically 8 or 32 Kbytes, implements the local packet buffer, while an optional boot PROM allows use of the adapter in diskless environments, where the driver program must be loaded from the network. The EtherCoupler provides interfaces to 100- or 150-ohm twisted pair (10BASE-T) as well as a direct AUI capability (10BASE5). An optional coaxial transceiver interface, such as Fujitsu's MBL8392A, provides additional capability for Thin Ethernet (10BASE2) networks. The MB86965 directly drives several LEDs which provide indication of adapter operational status.

For complete information on a typical adapter design, request the Hardware Reference Manual for the DK86965 EtherCoupler Designer Kit from your authorized Fujitsu Microelectronics sales representative or distributor. A Hardware Design Kit, HD86965, including schematics in electronic format, board layouts and Gerber tape for printed circuit card construction is also available for purchase at a nominal price.

TYPICAL APPLICATION

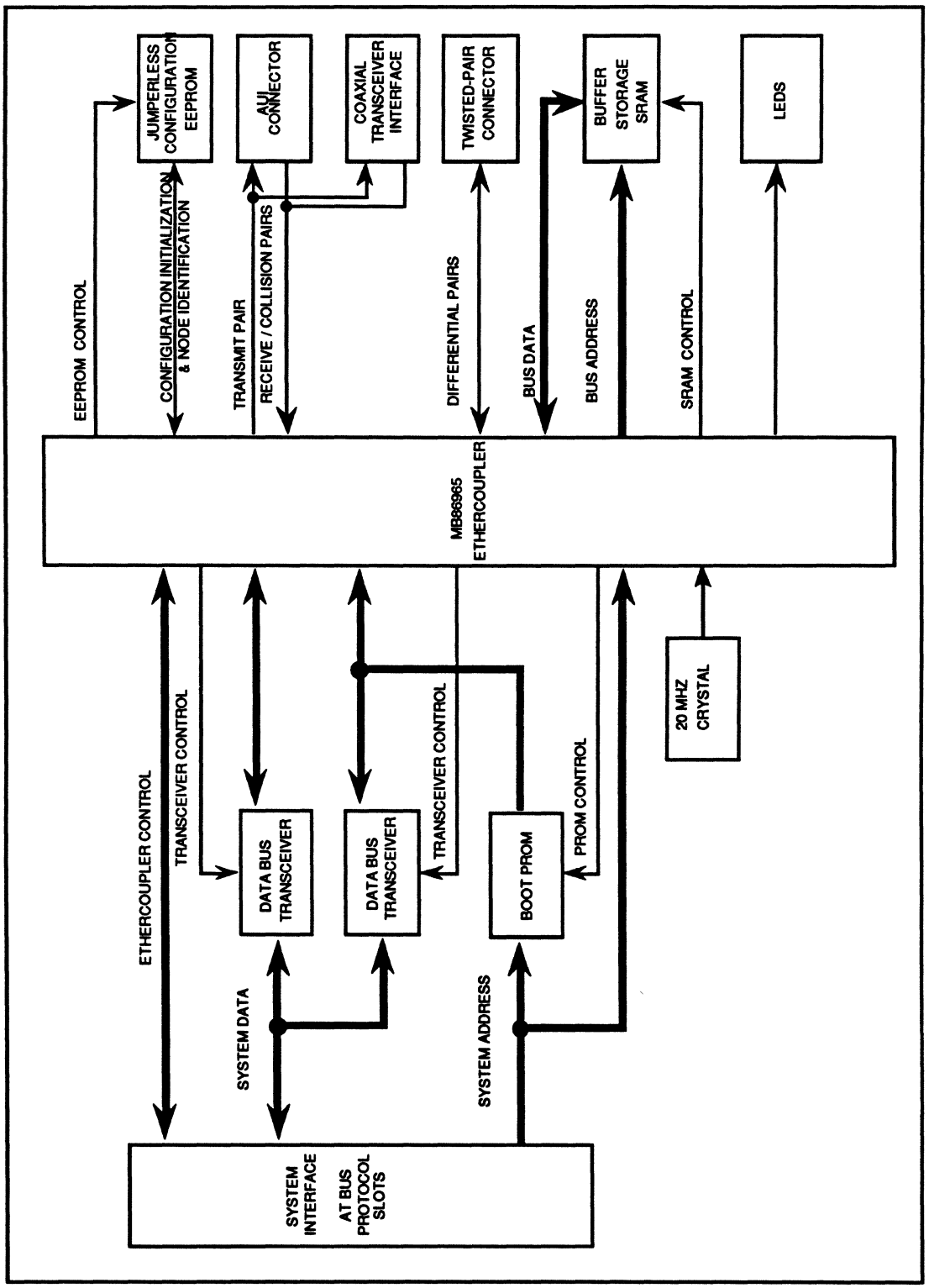


Figure 1. Typical Application, Block Diagram

PIN ASSIGNMENTS AND DESCRIPTIONS

LOGIC CONVENTION

Unless otherwise noted, a positive logic (active high) convention is assumed throughout this document, whereby the presence at a pin of a higher, more-positive voltage (nominally 5 VDC) causes assertion of the signal. An underscore, e.g., RDY indicates that the signal is asserted in the low state (nominally 0 volts). Dual function pins have their alternate function enclosed in parenthesis, e.g., IOCHRDY(RDY)

Whenever a signal is separated into numbered bits, e.g., BD7, BD6, BD5, BD4, BD3, BD2, BD1 and BD0, the family of bits may also be shown collectively, e.g., as BD<7:0>.

PIN ASSIGNMENTS

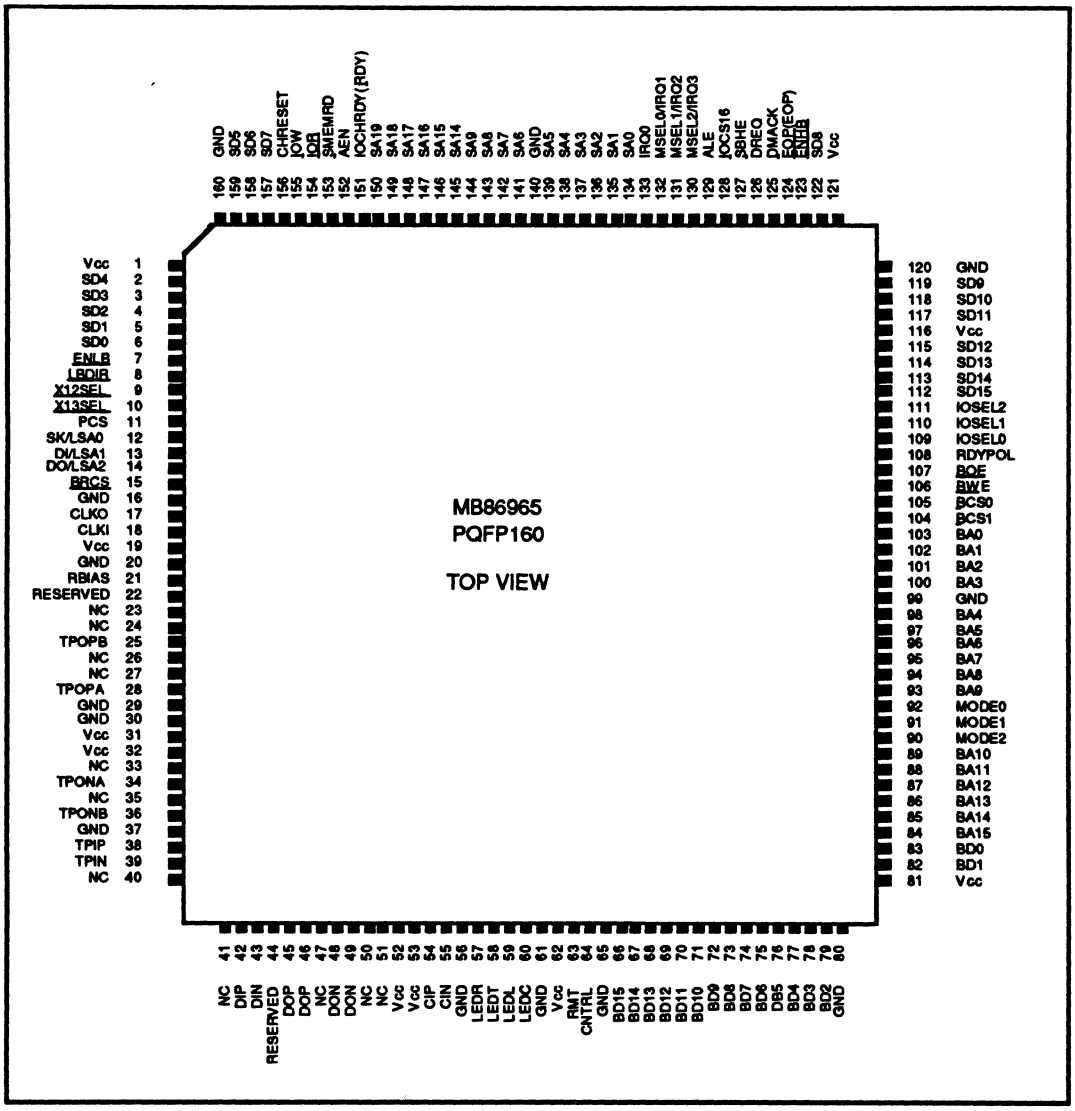


Figure 2. MB86965 Pin Assignments

PIN DESCRIPTIONS

System Bus Interface Pins

PIN NO.	SYMBOL	TYPE	DESCRIPTION
112–115, 117–119, 122, 157–159, 2-6	SD<15:12>, SD<11:9>, SD<8>, SD<7:5>, SD<4:0>	I/O	**SYSTEM DATA:** All data, command, and status transfers take place over this bus.
150–145	SA<19:14>	I	**SYSTEM ADDRESS:** High-order system address.
144–141, 139–134	SA<9:6>, SA<5:0>	I	**SYSTEM ADDRESS:** Low-order system address.
156	CHRESET	I	**CHIP RESET:** Resets the chip internal pointers and initializes internal registers and logic.
154	$\overline{IOR}$	I	**INPUT/OUTPUT READ:** Active low signal from the system bus which indicates that the current bus cycle is a read operation.
155	$\overline{IOW}$	I	**INPUT/OUTPUT WRITE:** Active low signal from the system bus which indicates that the current bus cycle is a write operation.
153	$\overline{SMEMRD}$	I	**SYSTEM MEMORY READ:** Active low signal from the system bus which indicates that the current bus cycle is a memory-read operation.
152	AEN	I	**ADDRESS ENABLE:** When asserted indicates that a DMA transfer is taking place.
124	$\overline{EOP}$(EOP)	I	**END OF PROCESS:** When asserted by the DMA controller, indicates that an entire packet has been transferred between buffer memory and the host system.
129	ALE	I	**ADDRESS LATCH ENABLE:** Provided by the system to latch valid addresses.
125	$\overline{DMACK}$	I	**DMA ACKNOWLEDGE:** Active low signal which indicates that the DMA controller is ready to transfer data between the host system and the EtherCoupler buffer memory.
127	$\overline{SBHE}$	I	**SYSTEM BUS HIGH ENABLE:** Active low. This pin is the byte/word control line. It is used only when EtherCoupler is configured for a 16-bit data bus by the SB/SW bit, DLCR6<5>. It allows word, upper byte only or lower byte only transfers. The address select pin SA0 is is used with $\overline{SBHE}$ for byte or word transfers as follows:

SB/SW	$\overline{SBHE}$	SA0	FUNCTION
0	0	0	Word transfer
0	0	1	Byte transfer on upper half of data bus (SD15-8)
0	1	0	Byte transfer on lower half of data bus (SD7-0)
0	1	1	Reserved

			X	X	X	Byte transfer (SD7-0)
111–109	IOSEL<2:0>	I	**INPUT/OUTPUT BLOCK ADDRESS SELECT:** Sets the base address at which the controller is located, as follows:			
			IOSEL2	**IOSEL1**	**IOSEL0**	**I/O BASE ADDRESS**
			0	0	0	260 – 27F
			0	0	1	280 – 29F
			0	1	0	2A0 – 2BF
			0	1	1	240 – 25F
			1	0	0	340 – 35F
			1	0	1	320 – 33F
			1	1	0	380 – 39F
			1	1	1	300 – 31F
90–92	MODE<2:0>	I	**MODE SELECT:** EtherCoupler configuration mode selection.			
			MODE2	**MODE1**	**MODE0**	**CONFIGURATION**
			0	0	0	The bus is in ISA mode, with an EEPROM that stores initial parameters, and configuration that is set for jumperless operation.
			0	0	1	With jumpers and EEPROM.
			0	1	0	With jumpers and IDPROM.
			0	1	1	Generic processor interfacing to buses other than ISA.
			1	X	X	RESERVED.
15	BRCS	O	**BOOT ROM CHIP SELECT:** Active low signal which indicates that the current memory access is to BOOT ROM.			
133	IRQA	O	**INTERRUPT REQUEST:** One of four interrupt request lines which indicate that EtherCoupler requires host attention after successful transmission or reception of a packet, or if any error conditions occur, including an EOP after the completion of the DMA cycle.			
130–132	IRQD, IRQC, IRQB	O	**INTERRUPT REQUEST,** in jumperless mode: three of four interrupt request lines which indicate that EtherCoupler requires host attention after successful transmission or reception of a packet, or if any error conditions occur, including an EOP after completion of DMA cycle.			
	MSEL<2:0>	I	**MEMORY SELECT,** in jumper select mode: sets BOOT ROM location base address.			
			MSEL2	**MSEL1**	**MSEL0**	**ROM ADDRESS RANGE**
			0	0	0	C4000 – C7FFF

			0	0	1	C8000 – CBFFF
			0	1	0	CC000 – CFFFF
			0	1	1	D0000 – D3FFF
			1	0	0	D4000 – D7FFF
			1	0	1	D8000 – DBFFF
			1	1	0	DC000 – DFFFF
			1	1	1	Decode disabled
126	DREQ	O	**DMA REQUEST:** Issued to the DMA controller to indicate that EtherCoupler has data available to be read in its receive buffer, or is ready to accept data into its transmit buffer.			
151	IOCHRDY(RDY)	O	**INPUT/OUTPUT CHANNEL READY:** This signal indicates to the host that EtherCoupler is ready to complete the requested read or write operation. Polarity of this pin is programmed by RDYPOL, pin 108.			
128	IOCS16	O	**INPUT/OUTPUT 16-BIT CHANNEL SIZE:** Active low signal which indicates that present data transfer is 16-bit I/O cycle.			
123	ENHB	O	**ENABLE DATA HIGH:** Active low signal which enables the system data transceiver high byte.			
7	ENLB	O	**ENABLE DATA LOW:** Active low signal which enables the system data transceiver low byte.			
8	DIR	O	**TRANSCEIVER DIRECTION:** Active low signal sets the external transceiver direction, from chip to system (read operation). Active high signal sets the external transceiver direction from system to chip (write operation).			
9	X12SEL	O	**SELECT CONFIGURATION REGISTER 1:** Active low signal pulse to read the jumper configuration register 1, located at address 0X12.			
10	X13SEL	O	**SELECT CONFIGURATION REGISTER 2:** Active low signal pulse to read the jumper configuration register 2, located at address 0X13.			
12	SK/LSA0	O	**EEPROM SHIFT CLOCK/LATCHED ADDRESS 0:** With IDPROM option, the pin provides one of three latched address lines to the IDPROM. With EEPROM option, this signal shifts data in and out of the EEPROM.			
13	DI/LSA1	O	**EEPROM DATA IN/LATCHED ADDRESS 1:** With IDPROM option, the pin provides one of three latched address lines to the IDPROM. With EEPROM option, this is serial data going to the EEPROM.			
14	DO/LSA2	I/O	**EEPROM DATA OUT/LATCHED ADDRESS 2:** With IDPROM option, the pin provides one of three latched address lines to the IDPROM. With EEPROM option, this is serial data coming from the EEPROM.			
11	PCS	O	**PROM CHIP SELECT:** High signal selects EEPROM. Low signal selects IDPROM.			

108	RDYPOL	I	**READY LINE POLARITY SELECT:** Controls polarity of IOCHRDY signal at pin 151, where 0 is active low READY and 1 is active high READY.
63	RMT	O	**REMOTE RESET:** When RMT RST bit DLCR5<2> is set high, this pin follows RMT 0900H bit DLCR1<4>, which indicates that a complete special packet with type field = 0900H has been received. This is intended for use as a remotely controlled hardware function from other nodes in the network.
64	CNTRL	O	**CONTROL:** This pin is intended as a hardware control pin programmable by the system software. Complement of CNTRL, DLCR4<2>.

Buffer Memory Interface Pins

PIN NO.	SYMBOL	TYPE	DESCRIPTION
66–79, 82–83	BD<15:2>, BD<1:0>	I/O	**BUFFER MEMORY DATA BUS:** Data lines between SRAM buffer memory and EtherCoupler. This data bus is configurable for an 8-bit or 16-bit data size by BB/BW bit, DLCR6<4>.
84–89, 93–98, 100-103	BA<15:10>, BA<9:4>, BA<3:0>	O	**BUFFER MEMORY ADDRESS BUS:** These lines address up to 64 kbytes of buffer memory.
104	BCS1	O	**BUFFER RAM CHIP SELECT 1:** Active low signal which is the chip select for the most significant byte of the buffer memory.
105	BCS0	O	**BUFFER RAM CHIP SELECT 0:** Active low signal which is the chip select for the least significant byte of the buffer memory.
106	BWE	O	**BUFFER WRITE ENABLE:** Active low signal which is the write enable to the buffer memory, and is generated during memory write cycles.
107	BOE	O	**BUFFER OUTPUT ENABLE:** Active low signal which is the output enable to the buffer memory, and is generated during memory read cycles.

Power and Transceiver Interface Pins

PIN NO.	SYMBOL	TYPE	DESCRIPTION
1,19,31, 32,52,53, 62,81, 116,121	V_{CC}	I	**POWER SUPPLY:** +5 Volts for analog and digital circuits.
16,20,29,30, 37,56, 61,65,80,99, 120,140, 160	GND	I	**GROUND:** digital and analog ground.
45,46	DOP	O	**AUI TRANSMIT PAIR:** A differential output driver pair for the AUI transceiver DO circuits. The output is Manchester encoded.
48,49	DON	O	
42	DIP	I	**AUI RECEIVE PAIR:** A differential input driver pair for the AUI transceiver DI circuits. The input is Manchester encoded.
43	DIN	I	
54	CIP	I	**AUI COLLISION PAIR:** A differential input driver pair for the AUI transceiver CI circuits. The input is collision signalling or signal-quality error (SQE).
55	CIN	I	
28	TPOPA	O	**TWISTED-PAIR OUTPUT:** A differential driver pair output to the twisted-pair cable. The output is pre-equalized so that no external filter is required.
34	TPONA	O	
25	TPOPB	O	**TWISTED-PAIR OUTPUT:** A differential driver pair output to the twisted-pair cable. The output is pre-equalized so that no external filter is required.
36	TPONB	O	
38	TPIP	I	**TWISTED-PAIR INPUT:** A differential input pair from the twisted-pair cable.
39	TPIN	I	
60	LEDC	O	**COLLISION LED:** Open-drain driver for the collision indicator. Output is pulled low during collision.
59	LEDL	O	**LINK LED:** Open-drain driver for link integrity indicator. Output is pulled low during link test pass.
58	LEDT	O	**TRANSMIT LED:** Open-drain driver for transmit indicator. Output is pulled low during transmit.
57	LEDR	O	**RECEIVE LED:** Open-drain driver for the receive indicator. Output is pulled low during receive.
21	RBIAS	I	**BIAS RESISTOR:** Used to control the bias of the operating circuit.
17	CLKO	O	**CRYSTAL OSCILLATOR:** A 20-MHz crystal must be connected between these pins. See Figure 4.
18	CLKI	I	
22, 44	RESERVED	–	Not used.

SYSTEM CONFIGURATION

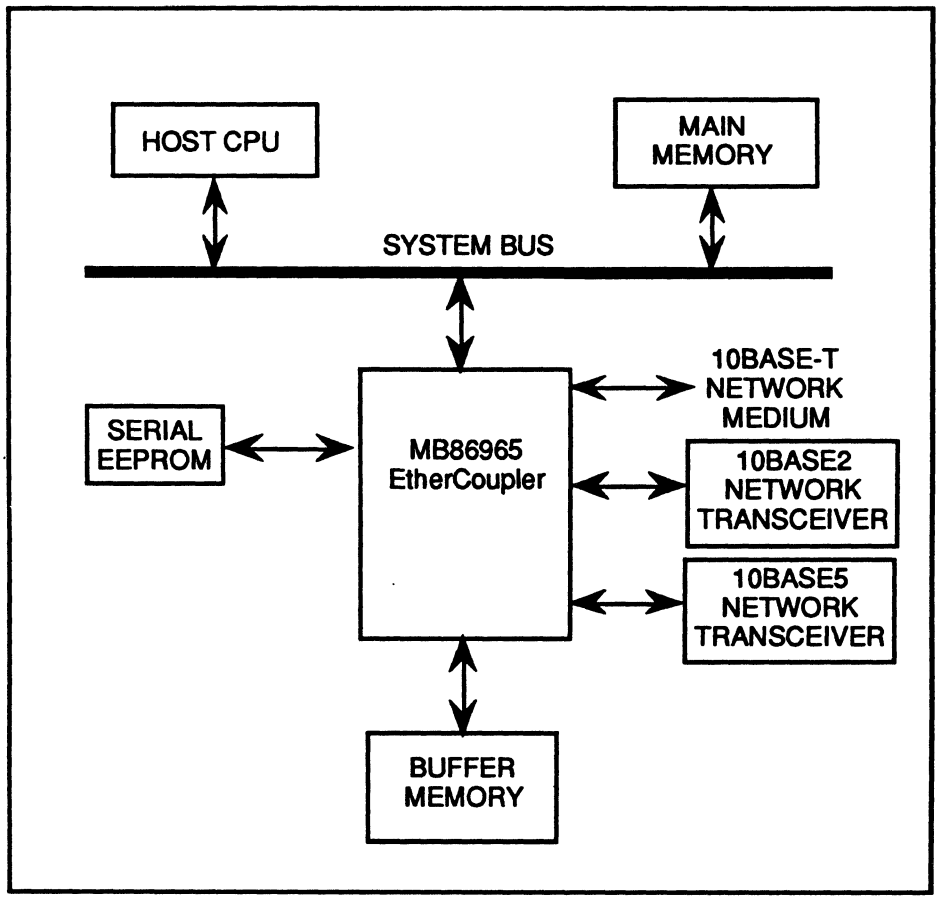


Figure 3. System Configuration, Simplified Block Diagram

As shown in Figure 3, EtherCoupler allows a highly integrated system configuration. EtherCoupler's architecture and high level of integration facilitate packet management and storage, and eliminate the need for a local microprocessor.

EtherCoupler connects with the host system bus to provide command and status interfaces as well as packet data access. The host processor can directly access command and status registers when mapped into the host I/O or memory space. Data packets to be transmitted to the media initially transfer from host memory through an EtherCoupler port into a dedicated buffer memory where they are temporarily stored until transmitted. Buffer memory initially stores received data packets that are later transferred to the host memory.

Refer to the section on Control and Status Registers for identification of control and status bits of the data link control registers, DLCR0 through DLCR7, and buffer memory port register pair, BMPR8 and BMPR9.

CONNECTION TO LAN MEDIA

Connection to the LAN media can be accomplished by on-board connection to a shielded or unshielded twisted pair, through the on-chip 10BASE-T transceiver.

CRYSTAL OSCILLATOR

The clock rate of 10 Mbits/s specified by the international LAN standard, ISO/ANSI/IEEE 8802-3, derives from an on-chip oscillator that is controlled by a crystal connected across pins 17 and 18 (CLKO and CLKI).

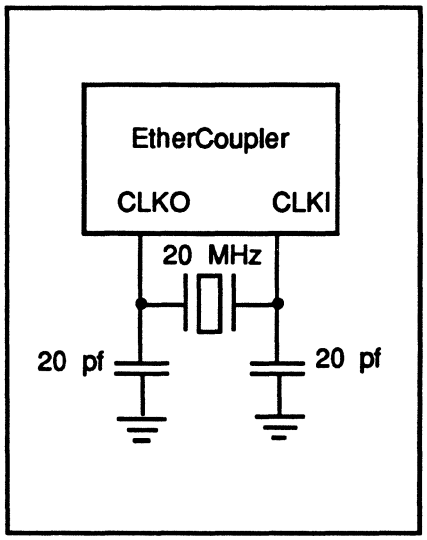


Figure 4. Crystal Oscillator Connection

Capacitance specified by the crystal manufacturer must be connected across pins 17 and 18 to ground, as shown in Figure 4, to stabilize the effects of stray capacitance that may vary crystal frequency.

The 20-MHz clock also serves as an internal phase-locked loop (PLL) reference for decoder clock recovery. Internal clocks shut down when the PWRDN bit, DLCR7<5>, is asserted for power down mode.

ELECTRICAL CHARACTERISTICS

OPERATIONAL SPECIFICATIONS

Absolute Maximum Ratings

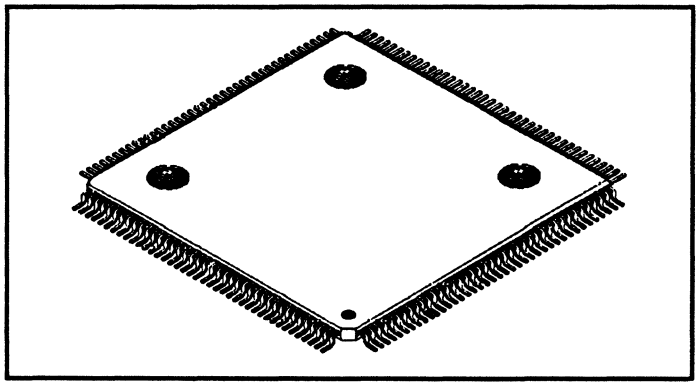
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	MAXIMUM	UNITS
V_{CC}	Supply voltage	−0.5	6.0	V
V_{IN}	Input voltage	−0.5	V_{CC}+ 0.5	V
V_{OUT}	Output voltage	−0.5	V_{CC}+ 0.5	V
I_{ODF}	Differential output current on DOP pins		−40	ma
V_{IDC}	Input DC voltage on DIP and CIP	−0.5	16	V
V_{ODC1}	Output DC voltage on DOP without transformer	−0.5	14	V
V_{ODC2}	Output DC voltage on DOP with transformer	−0.5	16	V
T_{BIAS}	Temperature under bias	−25	+85	°C
T_{STG}	Storage temperature	−40	+125	°C
PWR	Power dissipation		425	mw

Permanent device damage may occur if absolute maximum ratings are exceeded. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. No more than one output may be shorted to ground of V_{CC} at a time for a maximum duration of one second.

Recommended Operating Conditions

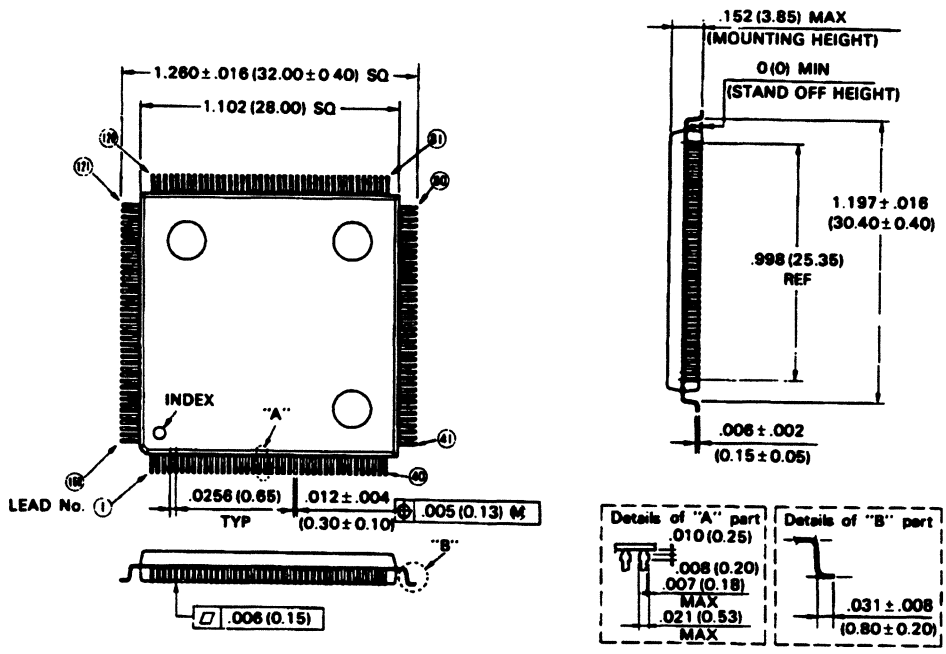
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
V_{DD}	Supply Voltage	4.75		5.25	V
V_{IH}	Logic input high voltage	2.2			V
V_{IL}	Logic input low voltage			0.8	V
R_L	Driver load resistors (across DOP and DON)	77	78	79	Ω
R_T	Termination resistors (two in series across DIP and CIP)	38.6	39	39.4	Ω
C_T	Termination bypass capacitors (between junction of termination resistors, ground)		0.1		µF
C_{OSC}	Oscillator load capacitors	12	20	38	pF
f_{XTAL}	Crystal oscillator frequency	19.999	20	20.001	MHz
T_A	Operating temperature	0		70	°C

ORDERING INFORMATION



160-pin Plastic Flat Package

160-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-160P-M03)



Dimensions in inches (millimeters)

TRADEMARKS

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