MB86701/701A

PLUG AND PLAY ISA CONTROLLER (PPIC)

PRELIMINARY DATA SHEET

MARCH 1995

FEATURES

- Provides Plug and Play compatibility for ISA add-in cards
- Conforms to Plug and Play ISA Specification v1.0a
- Can be used in non Plug and Play environment
- Serial interface for resource EEPROM including support for storage and retrieval of Plug and Play data structures and user defined data.
- Support for two DMA channels and two interrupt lines
- Interrupts routed to any of 11 ISA bus interrupt channels
- Programmable interrupt input polarity
- DMA routed to any of 7 ISA bus DMA channels
- Four chip select outputs - two I/O, two memory
- Generates /IOCS16 and /MEMCS16 control signals
- Four general purpose I/O lines
- Maps memory to fixed address for FIFO string moves
- 144-pin SQFP (MB86701), 120-pin PQFP (MB86701A)
- 5 volt power supply
- Low power CMOS technology

BENEFITS

- Provides auto-configuration of cards when installed in Plug and Play systems
- Reduces cost of customer support by reducing or totally eliminating installation-related problems
- Eliminates jumpers, switches and corresponding decoding logic
- Eliminates the need for special hardware and software related to proprietary schemes for software configuration
- Adds Plug and Play functionality to existing board designs with a minimum of re-engineering

GENERAL DESCRIPTION

The MB86701/701A Plug and Play ISA Controller (PPIC) is a single-chip solution offering all the hardware resources required to build ISA cards compliant with the Plug and Play ISA Specification v1.0a. An external serial EEPROM stores card resource requirements information and can also store additional user-defined data, such as an Ethernet ID or manufacturing traceability information. Configuration information provided by the Plug and Play software is stored in registers as defined in the specification. The MB86701/701A performs all I/O and memory address decoding as well as interrupt and DMA request routing. Stored configuration information is decoded to properly route interrupt and DMA requests. Users may direct card DMA to any of seven DMA channels on the ISA bus and interrupts to any of eleven interrupt channels on the ISA bus. Two separate DMA channels and two separate interrupts lines for logical devices are supported.

The PPIC also provides additional features not required by the specification that can enhance card performance and reduce cost. For example, a four-bit I/O port is provided with lines that are independently configurable as input or output. These lines allow control of functions such as media selection for a LAN card or monitoring of external events.

The following table summarizes the basic capabilities of the MB86701/701A:

RESOURCE	CAPABILITIES
Logical Devices	1
Interrupts	
Number	2
Levels Supported	3, 4, 5, 6, 7, 9, 10, 11, 12, 14, 15
DMA Channels	
Number	2
Levels Supported	0, 1, 2, 3, 5, 6, 7
I/O Chip Selects	
Number	2
Decode	16 bits
Window Size	16, 32, 64 or 128 bytes
Base Address	Any multiple of the window size
Memory Chip Selects	
Number	2
Decode	24 bits
Window Size	Can be specified as a range or an upper address
Base Address	Any multiple of 256 bytes
I/O Port	
Number of Lines	4
Type	Each line is independently programmable as an input or an output

A unique feature of the MB86701/701A allows the mapping of any access to a user-defined memory window into a single user-defined address on the logical device side of the chip. This is done by providing a single output composed of two of the chip select signals, while simultaneously providing combined read and write strobes. This allows driver software to use memory-reference instructions to access a fixed-address register on the card and thus improves data-transfer performance. For example, this feature can be used to move a sector of data to or from a FIFO on a SCSI card using string or block move instructions instead of a loop of I/O instructions.

The MB86701/701A is fabricated using a low-power CMOS process and is available in 120- and 144-pin quad flat packages.

PIN ASSIGNMENT - MB86701 (144-PIN SQFP)

PIN NO.	PIN NAME	TYPE (1)	PIN NO.	PIN NAME	TYPE (1)	PIN NO.	PIN NAME	TYPE (1)	PIN NO.	PIN NAME	TYPE (1)
1	NC	-	37	NC	-	73	NC	-	109	NC	-
2	NC	-	38	NC	-	74	NC	-	110	NC	-
3	NC	-	39	NC	-	75	NC	-	111	NC	-
4	GND	-	40	GND	-	76	GND	-	112	GND	-
5	IRQ11	O 12	41	IRQ3	O 12	77	IRQ6	O 12	113	IRQ15	O 12
6	SD7	I/O 24	42	/DMACKB	O 4	78	IOCHRDY	O24(2)	114	SA1	I
7	SA12	I	43	SD3	I/O 24	79	DI	O 4	115	DRQ7	O 24
8	SA13	I	44	/IOW	I	80	SK	O 4	116	SA2	I
9	SA14	I	45	/IOR	I	81	EEPCS	O 4	117	SA3	I
10	SA15	I	46	/MEMR	I	82	DO	I (PU)	118	SA4	I
11	SA16	I	47	/MEMW	I	83	/MCS1	O 4	119	SA5	I
12	DMARQA	I (PD)	48	ADD0	O 4	84	VDD	-	120	SA6	I
13	BALE	I	49	IRQ4	O 12	85	IRQ7	O 12	121	IRQ14	O 12
14	GND	-	50	GND	-	86	GND	-	122	GND	-
15	SD6	I/O 24	51	SD2	I/O 24	87	DRQ1	O 24	123	DRQ6	O 24
16	DMARQB	I (PD)	52	ADD1	O 4	88	LA17	I	124	SA7	I
17	RDY	I (PU)	53	ADD2	O 4	89	LA18	I	125	SA8	I
18	INTA	I (PD)	54	ADD3	O 4	90	LA19	I	126	SA9	I
19	VDD	-	55	VDD	-	91	VDD	-	127	VDD	-
20	/READ	O 4	56	/ACTIV	I (PU)	92	LA20	I	128	SA10	I
21	/WRITE	O 4	57	GND	-	93	LA21	I	129	SA11	I
22	/IOCS0	O 4	58	SD1	I/O 24	94	LA22	I	130	AEN	I
23	SD5	I/O 24	59	RESET_DRV	I (PD)	95	DRQ2	O 24	131	DRQ5	O 24
24	GND	-	60	GND	-	96	GND	-	132	GND	-
25	/RESET	O 4	61	IRQ5	O 12	97	IRQ9	O 12	133	IRQ12	O 12
26	IRQ10	O 12	62	ADD4	O 4	98	LA23	I	134	PIO3	I/O 4 (PU)
27	/IOCS1	O 4	63	ADD5	O 4	99	/DACK3	I	135	PIO2	I/O 4 (PU)
28	/MCS0	O 4	64	/DACK7	I	100	/DACK2	I	136	PIO1	I/O 4 (PU)
29	INTB	I (PD)	65	/DACK6	I	101	/DACK1	I	137	PIO0	I/O 4 (PU)
30	/CS	O 4	66	SD0	I/O 24	102	/DACK0	I	138	DRQ0	O 24
31	SD4	I/O 24	67	ADD6	O 4	103	DRQ3	O 24	139	/IOCS16	O 8(2)
32	/DMACKA	O 4	68	/DACK5	I	104	NEC	I (PU)	140	BCLK	I
33	/MEMCS16	O 8(2)	69	VDD	-	105	SA0	I	141	VDD	-
34	NC	-	70	NC	-	106	NC	-	142	NC	-
35	NC	-	71	NC	-	107	NC	-	143	NC	-
36	NC	-	72	NC	-	108	NC	-	144	NC	-

Note:

1. Numeric suffix indicates output current capability. See DC Characteristics. (PU) indicates internal pull-up resistor, (PD) indicates internal pull-down resistor.
2. Open drain outputs.

ORDERING CODE

PACKAGE STYLE	V_{CC} = +5V 5%, T_A = 0 to + 70°C
144-pin Plastic Flat Package	MB86701PFV-G

FUJITSU

PIN ASSIGNMENT - MB86701A (120-PIN PQFP)

PIN NO.	PIN NAME	TYPE (1)	PIN NO.	PIN NAME	TYPE (1)	PIN NO.	PIN NAME	TYPE (1)	PIN NO.	PIN NAME	TYPE (1)
1	GND	-	31	GND	-	61	GND	-	91	GND	-
2	SD7	I/O 24	32	IRQ3	O 12	62	SD0	I/O 24	92	IRQ15	O 12
3	SA12	I	33	/DMACKB	O 4	63	IOCHRDY	O 24(2)	93	DRQ7	O 24
4	SA13	I	34	SD3	I/O 24	64	DI	O 4	94	SA2	I
5	MCS0	O 4	35	/IOW	I	65	SK	O 4	95	SA3	I
6	SA14	I	36	/IOR	I	66	EEPCS	O 4	96	SA4	I
7	SA15	I	37	/MEMR	I	67	GND	-	97	IRQ14	O 12
8	SA16	I	38	/MEMW	I	68	DRQ1	O 24	98	SA5	I
9	DMARQA	I (PD)	39	ADD0	O 4	69	LA17	I	99	SA6	I
10	SD6	I/O 24	40	IRQ4	O 12	70	LA18	I	100	IRQ12	O 12
11	GND	-	41	GND	-	71	LA19	I	101	GND	-
12	BALE	I	42	SD2	I/O 24	72	IRQ6	O 12	102	DRQ6	O 24
13	DMARQB	I (PD)	43	GND	-	73	LA20	I	103	SA7	I
14	RDY	I (PU)	44	ADD1	O 4	74	LA21	I	104	SA8	I
15	INTA	I (PD)	45	VDD	-	75	LA22	I	105	SA9	I
16	/READ	O 4	46	/ACTIV	I (PU)	76	GND	-	106	VDD	-
17	VDD	-	47	SD1	I/O 24	77	DRQ2	O 24	107	SA10	I
18	/WRITE	O 4	48	RESET_DRV	I (PD)	78	IRQ9	O 12	108	SA11	I
19	/IOCS0	O 4	49	GND	-	79	LA23	I	109	PIO3	I/O 4 (PU)
20	SD5	I/O 24	50	IRQ5	O 12	80	/DACK3	I	110	GND	-
21	IRQ10	O 12	51	ADD2	O 4	81	/DACK2	I	111	PIO2	I/O 4 (PU)
22	GND	-	52	ADD3	O 4	82	/MCS1	O4	112	AEN	I
23	/RESET	O 4	53	ADD4	O 4	83	IRQ7	O12	113	DRQ5	O24
24	/IOCS1	O 4	54	ADD5	O 4	84	/DACK1	I	114	PIO1	I/O 4 (PU)
25	INTB	I (PD)	55	/DACK7	I	85	/DACK0	I	115	PIO0	I/O 4 (PU)
26	/CS	O4	56	/DACK6	I	86	DRQ3	O24	116	DRQ0	O 24
27	SD4	I/O 24	57	ADD6	O 4	87	NEC	I (PU)	117	/IOCS16	O 8(2)
28	/DMACKA	O 4	58	/DACK5	I	88	SA0	I	118	BCLK	I
29	/MEMCS16	O 8(2)	59	DO	I (PU)	89	SA1	I	119	IRQ11	O12
30	VDD	-	60	VDD	-	90	VDD	-	120	VDD	-

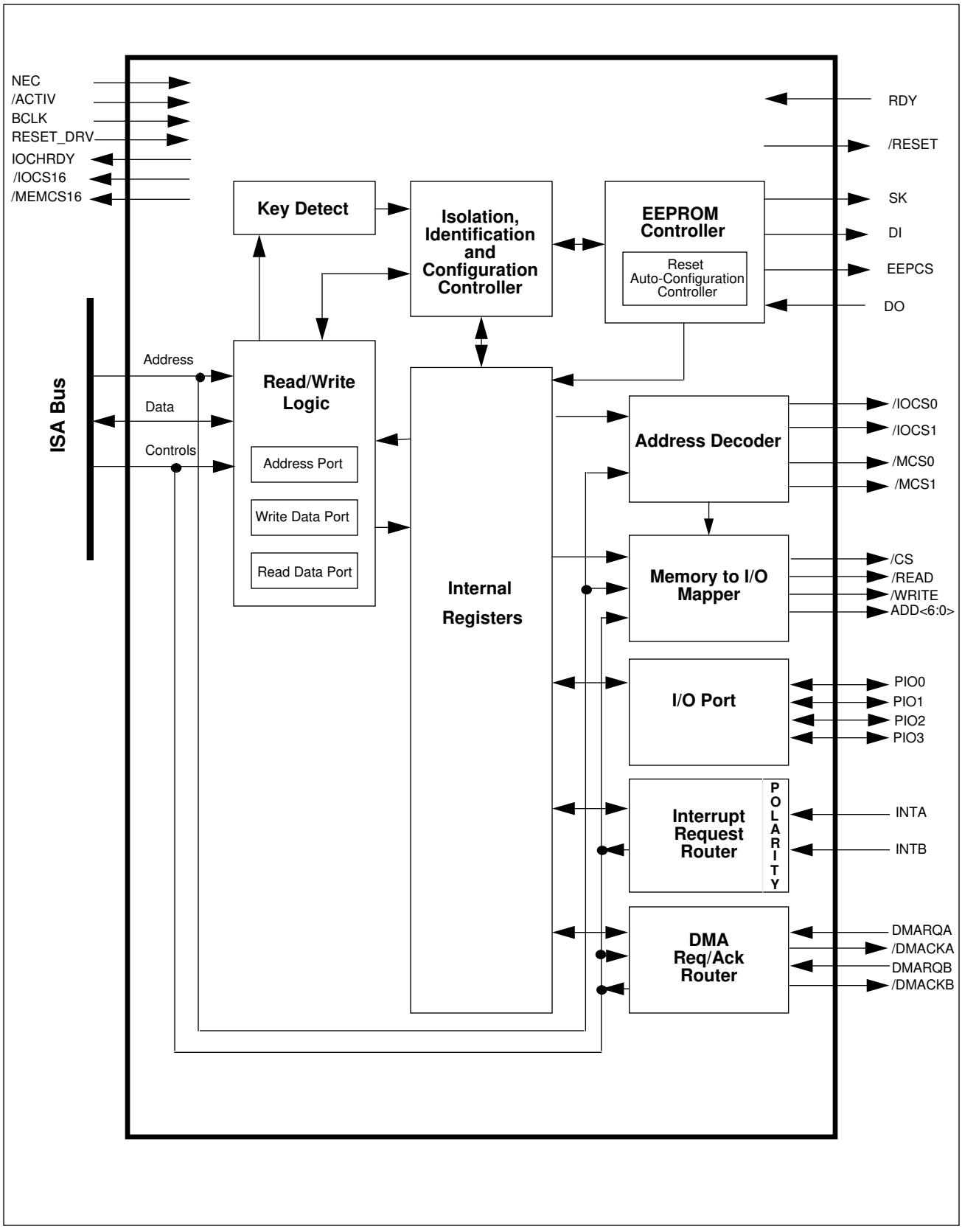
Note:

1. Numeric suffix indicates output current capability. See DC Characteristics. (PU) indicates internal pull-up resistor, (PD) indicates internal pull-down resistor.
2. Open drain outputs.

ORDERING CODE

PACKAGE STYLE	V_{CC} = +5V 5%, T_A = 0 to + 70°C
120-pin Plastic Flat Package	MB86701APF-G

BLOCK DIAGRAM



LOGIC CONVENTION

Unless otherwise noted, a positive logic (active high) convention is assumed throughout this document, whereby the presence at a pin of a higher, more positive voltage (nominally 5VDC) causes assertion of the signal. A preceding slash, e.g., /RESET, indicates that the signal is asserted in a low state (nominally 0 volts). Whenever a signal is separated into numbered bits, e.g., ADD6, ADD5, ADD4, ADD3, ADD2, ADD1, ADD0, the family of bits may also be shown collectively, e.g., as ADD<6:0>.

SIGNAL DESCRIPTIONS

ISA BUS INTERFACE SIGNALS

SYMBOL	TYPE	DESCRIPTION
RESET_DRV	I	**CHIP RESET**: Resets the chip and initializes internal registers and logic. When this signal is asserted, the MB86701/701A enters the *Wait for Key* state.
SA<16:0>	I	**SYSTEM ADDRESS**: Inputs are connected to the corresponding signals from the system bus.
LA<23:17>	I	**LATCHED ADDRESS**: Inputs are connected to the corresponding signals from the system bus.
SD<7:0>	I/O	**SYSTEM DATA**: All data, command and status transfers take place over this bus.
/IOR	I	**I/O READ**: Active low signal from the system bus which indicates that the current bus cycle is an I/O read operation.
/IOW	I	**I/O WRITE**: Active low signal from the system bus which indicates that the current bus cycle is an I/O write operation.
/MEMR	I	**SYSTEM MEMORY READ**: Active low signal driven by the current bus owner to indicate that the current bus cycle is a memory read operation.
/MEMW	I	**SYSTEM MEMORY WRITE**: Active low signal driven by the current bus owner to indicate that the current bus cycle is a memory write operation.
AEN	I	**ADDRESS ENABLE**: Input signal from the system bus. When low, indicates that an I/O slave may respond to addresses and I/O commands on the system bus.
BALE	I	**BUS ADDRESS LATCH ENABLE**: Active high input signal driven by the platform CPU to indicate when the ADDRESS and AEN signal lines are valid.
IRQ3-7, IRQ9-12, IRQ14-15	O	**INTERRUPT REQUEST**: Output to the system bus indicates that the controller chip is requesting an interrupt. Pins not configured as outputs are in the three-state condition.
BCLK	I	**SYSTEM BUS CLOCK**: A clock driven by the platform circuitry.
DRQ0-3, DRQ5-7	O	**DMA REQUEST**: Issued to the external DMA controller to indicate that the peripheral device is ready to transfer data. Used for both read and write operations. Pins not configured as outputs are in the three-state condition.

ISA BUS INTERFACE SIGNALS

SYMBOL	TYPE	DESCRIPTION
/DACK0-3, /DACK5-7	I	**DMA ACKNOWLEDGE**: Active low signal from the system bus indicating that the DMA acknowledge cycle is in progress.
IOCHRDY	O	**I/O CHANNEL READY**: Open drain output to the system bus which when high indicates that the addressed I/O device is ready for the bus transaction. The output is driven low when negated.
/IOCS16	O	**I/O CHIP SELECT 16**: Open drain output to the system bus which is asserted (low) to indicate that the addressed I/O window (IOCS0 or IOCS1) supports 16-bit data transfers. The user controls whether this signal is asserted for a specific chip select through values stored in the EEPROM. /IOCS16 will be asserted for any assertion of /IOCS0 if bit 1 of address 0x00F in the EEPROM is programmed to a '1', and for any assertion of /IOCS1 if bit 2 of address 0x00F in the EEPROM is programmed to a '1'.
/MEMCS16	O	**MEMORY CHIP SELECT 16**: Open drain output to the system bus which is asserted (low) to indicate that the addressed memory window supports 16-bit data transfers. This signal is asserted for a specific address through values stored in the Plug and Play standard registers. /MEMCS16 will be asserted for any assertion of /MCS0 if bit 1 of register 0x42 is programmed to a '1' by the Plug and Play configuration software, and for any assertion of /MCS1 if bit 1 of register 0x4A is programmed to a '1' by the Plug and Play configuration software. Note that the assertion of /MEMCS16 is based only on the comparison of the LA<23:17> signal lines against the corresponding values stored for the two chip selects. Thus, the output will be asserted for the entire 128K address block within which the chip select lies. The entire block must be either all 8 bits or all 16 bits. Problems may arise if only a portion of the block is associated with the 16-bit resource and another portion with an 8-bit resource.

EEPROM BUS INTERFACE SIGNALS

SYMBOL	TYPE	DESCRIPTION
DI	O	**EEPROM DATA IN**: Serial data to the EEPROM from the PPIC.
SK	O	**EEPROM SHIFT CLOCK**: Signal generated by the PPIC to shift data in and out of the EEPROM.
EEPCS	O	**EEPROM CHIP SELECT**: A high signal selects the EEPROM for read and write operations.
DO	I	**EEPROM DATA OUT**: Serial data from the EEPROM to the PPIC.

DEVICE INTERFACE SIGNALS

SYMBOL	TYPE	DESCRIPTION
/IOCS0	O	**I/O DESCRIPTOR 0 CHIP SELECT**: Can be used by any device that needs an I/O space.
/IOCS1	O	**I/O DESCRIPTOR 1 CHIP SELECT**: Can be used by any device that needs an I/O space.
/MCS0	O	**MEMORY DESCRIPTOR 0 CHIP SELECT**: Can be used by any device that needs memory space.
/MCS1	O	**MEMORY DESCRIPTOR 1 CHIP SELECT**: Can be used by any device that needs memory space.
/CS	O	**COMPOSITE CHIP SELECT**: Active low output used in conjunction with /READ, /WRITE and ADD<6:0> to perform the memory window to register address mapping function. It is the logical-OR of /MCS0 and /IOCS0 and is asserted when either of those signals is asserted.

DEVICE INTERFACE SIGNALS

SYMBOL	TYPE	DESCRIPTION
/READ	O	**COMPOSITE READ**: An active low signal that is used in conjunction with /CS to indicate that the current transfer between the host system and the device is a read cycle. The signal is composed of the /IOR input signal while /IOCS0 and /IOCS1 are active and the /MEMR signal while /MCS0 is active.
/WRITE	O	**COMPOSITE WRITE**: An active low signal that is used in conjunction with /CS to indicate that the current transfer between the host system and the device is a write cycle. The signal is composed of the /IOW input signal while /IOCS0 and /IOCS1 are active and the /MEMW signal while /MCS0 is active.
PIO<3:0>	I/O	**GENERAL PURPOSE I/O PINS**: Each of these pins can be programmed to be an input or an output. The signal direction is programmed via the I/O Data Direction Register, 0x21. The state of the pin is controlled by writing the data into the I/O Data Register, 0x20 (values for pins programmed as inputs are ignored). Writing a “1” sets the output high, while writing a “0” sets the output low. The current state of the pins can be determined by reading the I/O Data Register.
NEC	I	**NEC COMPATIBILITY**: When high, changes address of the ADDRESS and WRITE_DATA ports to 0x0259 and 0x0A59, respectively, to provide compatibility with NEC98 series computers. When low, the addresses of the two ports are 0x0279 and 0x0A79, respectively.
ADD<6:0>	O	**REGISTER ADDRESS**: Outputs used in conjunction with /CS, /READ and /WRITE to perform the memory window to register address mapping function. While the /IOCS0 portion of /CS is active the pins output the ISA bus address from the SA<6:0> inputs. While the /MCS0 portion of /CS is active, these pins output the corresponding contents of the Mapped Register Address Register.
RDY	I	**READY**: Input from the I/O device which goes low at the beginning of a read or write cycle and is set high when the peripheral controller is ready to complete the requested transaction.
/ACTIV	I	**ACTIVATE**: If this pin is tied low, register 0x30<0>, the Activate bit, will be set to the Activate state (1) immediately after the default values are loaded into the configuration registers from the EEPROM upon reset. The state of this pin is ignored at all other times. This input has an internal pull-up resistor and can be left open if activate after reset is not required.
/RESET	O	**BOARD RESET**: An active low output to the board produced in response to receipt of RESET_DRV on the ISA bus or if a reset command is issued by writing a “0x07” to the Configuration Control Register, 0x02.
INTA,INTB	I	**INTERRUPT REQUEST**: Inputs from the I/O controller which indicate that it is requesting an interrupt. The MB86701/701A can accept active high or active low interrupt inputs. For INTA, setting 0x014<6> of the EEPROM to a ‘0’ specifies an active high input and setting it to a ‘1’ specifies an active low input. For INTB, 0x015<6> performs the same function.
DMARQA, DMARQB	I	**DMA REQUEST**: Inputs from the controller indicating that it is requesting bus ownership to transfer data.
/DMACKA, /DMACKB	O	**DMA ACKNOWLEDGE**: Active low signal to the I/O controller indicating that a DMA acknowledge cycle is in progress. Produced in response to receipt of /DACK from the system bus.
GND	-	**GROUND**: Signal and power ground.
VDD	-	**POWER SUPPLY**: +5 volts 5%.

FUNCTIONAL DESCRIPTION

The MB86701/701A is a generic Plug and Play device which when attached to ISA compatible controllers enables them to operate in the Plug and Play environment. In the Plug and Play environment users may plug peripheral cards such as LAN cards, graphics adapters or hard-disk controllers into their machines and system software configures each card automatically at power-up time. The need for configuration jumpers and switches on the adapter card is eliminated and installation of cards becomes more user friendly.

The MB86701/701A is based on the Plug and Play ISA Specification v1.0a and meets all ISA timing specifications as well.

The Plug and Play concept is built around the following four states: (1) *Wait for Key* (2) *Sleep* (3) *Isolation* and (4) *Configuration*. At power up, the cards begin in the *Wait for Key* state, awaiting the initiation key with outputs disabled. Once the initiation key is received, the *Sleep* state begins. The card remains in the *Sleep* state until it receives a Wake[CSN] command with the parameter data set to zero upon which the *Isolation* state is entered. After the card is isolated, it receives a unique Card Select Number (CSN). Once the CSN is written, the card moves into the *Configuration* state and its resources are read. All cards in a system follow the same procedure until their resource requirements are known.

Note: The following sections provide a brief overview of the Plug and Play configuration process. Please refer to the Plug and Play ISA specification for additional information. Copies of this specification are available from Fujitsu upon request. Contact your local Fujitsu sales office, representative or distributor.

Plug and Play Card Configuration Sequence

The MB86701/701A PPIC contains all the hardware resources required to allow the card to be identified and auto-configured by the Plug and Play software resident in the host system.

The auto configuration process consists of the following steps:

- All Plug and Play ISA cards are placed in the *Sleep* state.
- All Plug and Play ISA cards are isolated one at a time.
- As each card is isolated, assign a handle and read the card's resource data structure
- After the resource requirements and capabilities are determined for all cards, the handle is used to place the card in *Configuration* state and assign conflict free resources to each card.
- All Plug and Play ISA cards are activated and removed from *Configuration* state.

The Plug and Play software uses three 8-bit I/O ports to execute a set of commands that identify and configure devices. A sequence of data writes to one of the ports, referred to as the initiation key, is used to enable the Plug and Play logic on all cards in the system.

Because all Plug and Play cards can respond to the same I/O port addresses, an isolation mechanism is required for the Plug and Play software to address each card independently. During *Isolation*, an isolation protocol is used to read a unique identifier on each card to isolate one Plug and Play card at a time. Following *Isolation*, the Plug and Play software assigns each card a handle (CSN) which is used to address that unique Plug and Play card. The software then reads the resource data structure which describes the resources supported and those requested by functions on the card.

When all resource capabilities and demands of the cards are known, the process of resource arbitration is invoked to determine resource allocation to each ISA card. A conflict detection mechanism is invoked to insure that resources assigned are not in conflict with standard ISA cards.Then, using the previously assigned handle, each Plug and Play card is placed in the *Configuration* state and the card is configured with the allocated resources through the Plug and Play standard registers. If the resources requested are not reconfigurable, equivalent resources will be supported. The resource data structure will inform the arbiter that the requested resources cannot be assigned to other Plug and Play cards in the system.

The command set also supports the ability to activate or deactivate the functions on the card.

Once the configuration is completed, Plug and Play cards are removed from the *Configuration* state and placed in normal system operation mode. To enter the *Configuration* state again, the initiation key must be re-issued. This process prevents accidental erasure of the configuration information.

State Summary

The Plug and Play logic is quiescent on power up (*Wait for Key* state) and must be enabled by software. A predefined series of writes to the ADDRESS port places the Plug and Play logic into *Sleep* state. This is referred to as the initiation key. The write sequence is decoded by on-card logic, and if the proper series of I/O writes is detected, the auto-configuration ports are enabled. If the data does not match, the internal logic is reinitialized and the PPIC remains in the *Wait for Key* state.

On each ISA card there exists an 8-bit register called the Card Select Number (CSN) register (0x06) used to select one or more ISA cards when those cards are in certain states. The CSN mechanism allows a wide variety of devices to manage their configuration and control. The CSN register is set to 0x00 on all cards on power up. Once a card has been isolated, the CSN on that card is assigned a unique value which enables the Plug and Play software to select this card later in the configuration process, without going through the protocol again.

The four Plug and Play states (see Figure 1) are summarized as follows:

- *Wait for Key* - Upon power-up reset and *Wait for Key* commands, all cards enter this state. No commands are active in this state until the initiation key is detected on the ISA bus. It is the default state for Plug and Play cards during normal system operation. After configuration and activation, software should return all cards to this state.While in the *Wait for Key* state, cards do not respond to any access to their auto-configuration ports until the initiation key is detected. All ISA accesses from the Plug and Play interface to the cards are ignored.
- *Sleep* - Plug and Play cards wait for a Wake[CSN] command in this state. Based on the write data and the value of the CSN on each card, this command will selectively enable one or more cards to the *Isolation* or *Configuration* states. To exit this state, the value of the write data bits[7:0] of the Wake[CSN] command must match the card's CSN. If the write data for Wake[CSN] is zero, then all cards that have not been assigned a CSN will enter the *Isolation* state. If the write data for the Wake[CSN] command is nonzero, then the one card whose assigned CSN matches the parameter of the Wake[CSN] command will enter the *Configuration* state.
- *Isolation* - The first time the cards enter the *Isolation* state, it is necessary to set the READ_DATA port address using the Set RD_DATA port command. Seventy-two pairs of reads are performed to the Serial Isolation register to isolate a card. If the

checksum read from the card is valid, then one card has been isolated. The isolated card remains in the *Isolation* state. All other cards which have failed the isolation protocol will return to the *Sleep* state. The isolated card is assigned a unique value called the Card Select Number (CSN) and transitions to the *Configuration* state. The Wake[0] command causes the card to transition back to the *Sleep* state and all cards with a CSN value of zero transition to the *Isolation* state. This entire process is repeated until all Plug and Play cards are detected.

- *Configuration* -In this state, the card responds to all configuration commands including reading the card's resource configuration information and programming the card's resource selections. Only one card may be in this state at a time.

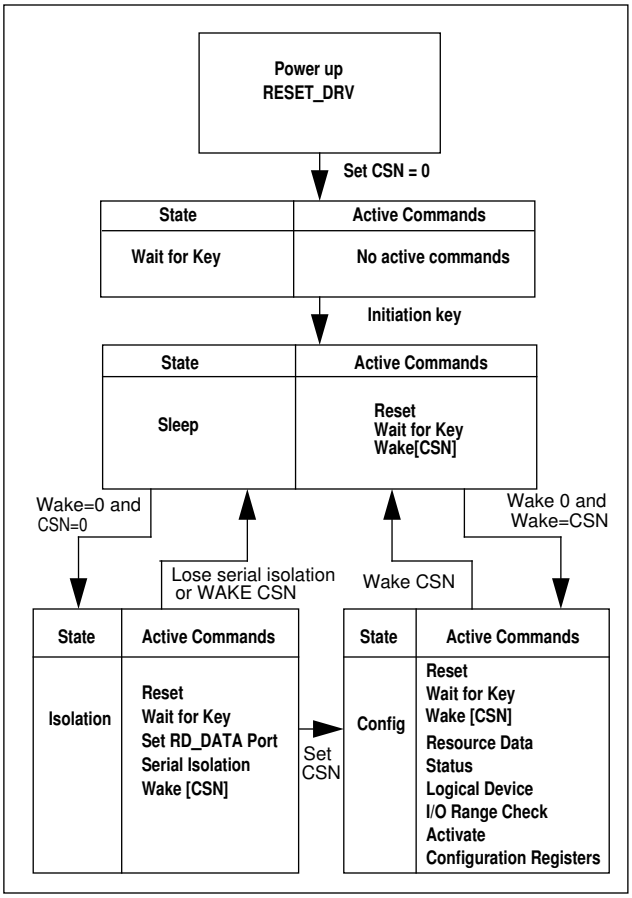


Figure 1. Plug and Play Configuration Process States

Notes:

1. CSN = Card Select Number.
2. RESET_DRV causes a state transition from the current state to *Wait for Key* and sets all CSNs to zero. All logical devices are set to their power-up configuration values.
3. The *Wait for Key* command causes a state transition from the current state to *Wait for Key.*

Auto-Configuration Ports

Three 8-bit ports are used by the software to access the configuration space on each Plug and Play ISA card. The ports are listed in Table 1. These registers are used by the Plug and Play software to issue commands, check status, access the resource data information, and configure the Plug and Play hardware. The ports have been chosen to avoid conflicts in the installed base of ISA functions, while at the same time minimizing the number of ports needed in the ISA I/O space.

Table 1. Auto-Configuration Ports

PORT NAME	LOCATION	TYPE
ADDRESS	0x0279(1)	Write-only
WRITE_DATA	0x0A79(2)	Write-only
READ_DATA	Relocatable in range 0x0203 to 0x03FF	Read-only

Notes:

1. Address is 0x0259 if NEC input is asserted.
2. Address is 0x0A59 if NEC input is asserted.

The three auto-configuration ports use a 12-bit ISA address decode. The ADDRESS and WRITE_DATA ports are located at fixed addresses. The WRITE_DATA port is located at an address alias of the ADDRESS port. The READ_DATA port, which is the only readable auto-configuration port, is relocatable within the I/O range from 0x0203 to 0x03FF. The address of the READ_DATA port is assigned by the system software and is set by writing the proper value to Plug and Play control register 0x00 (Set RD_DATA Port command). The isolation protocol verifies that the location selected for the READ_DATA port is free of conflict.

The Plug and Play registers within the PPIC are accessed by writing the address of the desired register to the ADDRESS port, followed by a read of data from the READ_DATA port or a write of data to the WRITE_DATA port. A write to the ADDRESS port may be followed by any number of WRITE_DATA or READ_DATA accesses to the same register location without the need to write to the ADDRESS port before each access.

Obtaining The Device Configuration

The driver or other application software requires a mechanism to determine the configuration information in order to communicate with the card. An Application Programming Interface (API) exists to provide the required data. Called the Plug and Play Configuration Manager API, it is documented in the "Plug and Play Device Driver Developer's Guide" (Intel Publication Number 485473-001) or equivalent documentation provided by the supplier of the Plug and Play system software. Also see "Plug and Play Device Driver Interface for Microsoft Windows 3.1 and MS-DOS" (available on the Plug and Play forum on CompuServe).

The API requires only two calls to retrieve configuration:

- **CM_GetVersion** verifies the presence of the Configuration Manager.
- **CM_GetConfig** retrieves the configuration information from an indexed, system wide table. This information includes READ_DATA port address, Card Select Number (CSN) and resource allocation for each configured device.

The Configuration Manager also provides a Configuration Access (CA) support interface. Two calls associated with this interface of particular interest are:

- **CA_GetVersion** verifies the presence of the Configuration Access support interface.
- **CA_PnPISA_Get_Resource_Data** retrieves the resource data stored in the EEPROM connected to the MB86701/701A and can be used to obtain the data stored in the "Vendor Defined" resource data types.

MB86701/701A REGISTERS

Table 2. MB86701/701A Register Set

				ACCESS BY STATE			
ADD	**STD**	**DESCRIPTION**	**DEF**	**WT KEY**	**SLEEP**	**ISOL**	**CONFIG**
0x00	X	Set READ_DATA Port	0x00			W	
0x01	X	Serial Isolation	0x00			R	
0x02	X	Configuration Control	0x00		W	W	W
0x03	X	Wake[CSN]	0x00		W	W	W
0x04	X	Resource Data	0x00				R
0x05	X	Status	0x00				R
0x06	X	Card Select Number	0x00			W	R
0x07	X	Logical Device Number	0x00				R
0x20		PIO Data	0x00				R/W
0x21		PIO Data Direction	0x00				W
0x22		EEPROM Write Enable	0x00				W
0x23		EEPROM Write Data Low	0x00				W
0x24		EEPROM Write Data High	0x00				W
0x25		PnP State	0x00				R
0x26		EEPROM Command	0x00				W
0x30	X	Activate	Note 4				R/W
0x31	X	I/O Range Check	0x00				R/W
0x40	X	Memory Base Address 0 [23:16]	EE 0x001				R/W
0x41	X	Memory Base Address 0 [15:8]	EE 0x000				R/W
0x42	X	Memory Control 0	EE 0x002				R/W
0x43	X	Mem Upper Limit/Range 0 [23:16]	EE 0x004				R/W
0x44	X	Mem Upper Limit/Range 0 [15:8]	EE 0x003				R/W
0x48	X	Memory Base Address 1 [23:16]	EE 0x006				R/W
0x49	X	Memory Base Address 1 [15:8]	EE 0x005				R/W
0x4A	X	Memory Control 1	EE 0x007				R/W
0x4B	X	Mem Upper Limit/Range 1 [23:16]	EE 0x009				R/W
0x4C	X	Mem Upper Limit/Range 1 [15:8]	EE 0x008				R/W
0x60	X	I/O Base Address 0 [15:8]	EE 0x00B				R/W
0x61	X	I/O Base Address 0 [7:0]	EE 0x00A				R/W
0x62	X	I/O Base Address 1 [15:8]	EE 0x00D				R/W
0x63	X	I/O Base Address 1 [7:0]	EE 0x00C				R/W
0x70	X	Interrupt Request Level 0	EE 0x014				R/W
0x71	X	Interrupt Request Type 0	EE 0x014				R/W
0x72	X	Interrupt Request Level 1	EE 0x015				R/W
0x73	X	Interrupt Request Type 1	EE 0x015				R/W
0x74	X	DMA Channel 0	EE 0x012				R/W
0x75	X	DMA Channel 1	EE 0x013				R/W
Note 1		I/O Range 0	EE 0x010				
Note 2		I/O Range 1	EE 0x011				
Note 3		Memory Mapped Register Address	EE 0x00E				

Note 1. See Table 11.

Note 2. See Table 12.

Note 3. See Table 13.

Note 4: Default value = (EE0x00F<0>) OR (NOT(/ACTIV)).

Operation of the PPIC is controlled by values written into registers within the device while other registers provide device status. The register set consists of a combination of Plug and Play standard registers and vendor defined registers. Table 2 is a map of the user-accessible registers implemented in the MB86701/701A. In this table, an "X" in the STD column indicates that this is a standard PnP register and is described in the Plug and Play ISA specification (Appendix A). The table also provides default values (DEF) and defines, for each Plug and Play state, the type of access available. Exceptions to the specification are detailed in Table 3. Vendor-defined registers contained in the PPIC are described in Tables 4 to 13.

As previously described, the registers are accessed for read and write operation via the ADDRESS, WRITE_DATA and READ_DATA auto-configuration ports (see Table 1). The ADDRESS and WRITE_DATA ports have defined ISA addresses. In a PnP system, the READ_PORT address is normally assigned by the PnP system software during *Isolation*. In that environment, the address of the READ_DATA port can be determined by using the CM_GetConfig call to the Configuration Manager as previously described. In a non-PnP system, the READ_DATA port address will have been assigned by the configuration utility used to configure the card, and can be determined as appropriate for that software.

Table 3. MB86701/701A Standard PnP Register Exceptions

ADD	EXCEPTION
0x07	The MB86701/701A supports only a single logical device. The Logical Device Number Register is read-only and returns a value of 0x00 when read.
0x71,0x73	Bit<0> does not perform any function. The type of interrupt (level or edge) cannot be controlled by the MB86701/701A and will depend entirely on the type of input signal supplied at the INTA and INTB inputs.

Table 4. PIO Data (0x20)

BIT	DESCRIPTION
<3:0>	These bits correspond to the PIO<3:0> pins of the MB86701/701A. If the pin is enabled as an output via the PIO Data Direction Register, writing a "1" to a bit sets the corresponding output high and writing a "0" sets the output low. Data written to pins set as inputs has no effect. A read of this register provides the current state of the pins.
<7:4>	Not implemented. Return "0" when read.

Table 5. PIO Data Direction (0x21)

BIT	DESCRIPTION
<3:0>	These bits correspond to the PIO<3:0> pins of the MB86701/701A. Writing a "1" to a bit sets the corresponding pin as an output, while writing a "0" sets the pin as an input.
<7:4>	Not implemented. Return "0" when read.

Table 6. EEPROM Write Enable/Write Disable (0x22)

BIT	DESCRIPTION
<0>	Setting this bit to a "1" enables writes to the serial EEPROM, clearing it disables such writes. After setting or clearing this bit, a 0x00 command must be issued to the Resource Data Register to transfer the enable/disable command to the EEPROM. The EEPROM will remain write enabled (or disabled) until another enable/disable command is issued.
<7:1>	Not implemented.

Table 7. EEPROM Write Data Low (0x23)

BIT	DESCRIPTION
<7:0>	The lower byte of the word which is to be written into the EEPROM at the next EEPROM write operation.

Table 8. EEPROM Write Data High (0x24)

BIT	DESCRIPTION
<7:0>	The upper byte of the word which is to be written into the EEPROM at the next EEPROM write operation.

Table 9. MB86701/701A PnP State (0x25)

BIT	DESCRIPTION
<0>	0 = The MB86701/701A is not in the *Wait for Key* state. 1 = The MB86701/701A is in the *Wait for Key* state.
<1>	0 = The MB86701/701A is not in the *Sleep* state. 1 = The MB86701/701A is in the *Sleep* state.
<2>	0 = The MB86701/701A is not in the *Isolation* state. 1 = The MB86701/701A is in the *Isolation* state.
<3>	0 = The MB86701/701A is not in the *Configuration* state. 1 = The MB86701/701A is in the *Configuration* state.
<7:4>	Not implemented. Return “0” when read.

Table 10. EEPROM Command (0x26)

BIT	DESCRIPTION
<7:0>	Writing 0x00 into this register causes a write enable/disable command to be sent to the serial EEPROM. Register 0x22 must be set/cleared before this command is issued. See Table 6. Writing a 0x01 into this register initiates an EEPROM write cycle, causing the contents of registers 0x23 and 0x24 to be written into the EEPROM. The EEPROM must have been write enabled before this command is issued.

Table 11. I/O Range 0(1)

BIT	DESCRIPTION
<1:0>	Define the Register window size for I/O chip select 0. 00 = 16 bytes 01 = 32 bytes 10 = 64 bytes 11 = 128 bytes
<7:2>	Not implemented.

Note:
1. This internal register is not user accessible. It is automatically loaded at reset with the value stored in byte 0x010 in the EEPROM.

Table 12. I/O Range 1(1)

BIT	DESCRIPTION
<1:0>	Define the Register window size for I/O chip select 1. 00 = 16 bytes 01 = 32 bytes 10 = 64 bytes 11 = 128 bytes
<7:2>	Not implemented.

Note:
1. This internal register is not user accessible. It is automatically loaded at reset with the value stored in byte 0x011 in the EEPROM.

Table 13. Memory Mapped I/O Register Address(1)

BIT	DESCRIPTION
<6:0>	This value specifies the lower 7-bits of the register address for the memory-to-I/O mapping function. The value is output on the ADD<6:0> outputs of the MB86701/701A whenever the /MCS0 output is asserted.
<7>	Not implemented.

Note:
1. This internal register is not user accessible. It is automatically loaded at reset with the value stored in byte 0x00E in the EEPROM. See Memory to I/O Mapping Section of data sheet.

Control Register Summary

Plug and Play cards respond to commands written to Plug and Play registers as well as certain ISA bus conditions. These commands are summarized below:

- RESET_DRV - This is the ISA bus reset signal. Upon detection of this signal, the Plug and Play card enters the *Wait for Key* state and all CSNs are reset to 0x00. Power-up values are loaded from non-volatile memory to the configuration registers. The logical device becomes active if the /ACTIV pin is low or if the Activate Register default value in the EEPROM is set to 0x01.

  Note: The software must delay 1 msec after RESET_DRV before accessing the auto-configuration ports.

- Config Control Register - The Config Control Register consists of three independent commands which are activated by writing a “1” to their corresponding register bits. These bits are automatically reset to “0” by the hardware after the commands execute.

  -Reset command - The Reset command is sent to the Plug and Play cards by writing a value of 0x01 to the Config Control register. All Plug and Play cards in any state, except those in *Wait for Key*, respond to this command. This command performs a reset function on all logical devices. This resets the contents of configuration registers to their default state. The configuration registers for all logical devices are loaded with their power up values from non-volatile memory. The READ_DATA port, CSN and Plug and Play state are preserved.

-Wait for Key command - The Wait for Key command is sent to the Plug and Play cards by writing a value of 0x02 to the Config Control register. All Plug and Play cards in any state will respond to this command. The CSNs are preserved and no logical device status is changed.

-Reset CSN command - The Reset CSN command is sent to the Plug and Play cards by writing the value of 0x04 to the Config Control register. All Plug and Play cards in any state except *Wait for Key* will reset their CSN to 0x00.

-Writing 0x07 to the Config Control Register is equivalent to a RESET_DRV event.

Note: The software must delay for 1 ms after the Reset command before accessing the auto-configuration ports.

- Set RD_DATA Port Command - This command is used in the *Isolation* state and sets the address of the READ_DATA port. Write data bits [7:0] are used as ISA I/O bus address bits[09:02]. The ISA bus address bits[1:0] are fixed at binary "11". The ISA bus address bits[15:10] are fixed at binary '"000000".

  Note: After a RESET_DRV or Reset CSN command, this register is considered uninitialized and must be reinitialized.
- Serial Isolation Register - A read from the Serial Isolation Register causes Plug and Play cards in the *Isolation* state to respond to the ISA bus read cycle.
- Card Select Number - A Card Select Number is uniquely assigned to each Plug and Play card when the card has been isolated and is the only card in the *Isolation* state. An unidentified card is assigned a value of zero. Valid Card Select Numbers for identified ISA cards range from 1 to 255 and must be assigned sequentially starting from 1. The Card Select Number is used to select a card via the Wake[CSN] command. The Card Select Number on all ISA cards is set to zero on a RESET_DRV or Reset CSN command. The CSN is never set to zero using the CSN register.
- Wake[CSN] Command - This command is used to bring ISA cards in the *Sleep* state into either the *Isolation* state or the *Configuration* state. A Wake[CSN] command with a parameter of zero will force all cards without a CSN to enter the *Isolation* state. A Wake[CSN] command with a parameter other than zero will force a card with a matching CSN to enter the *Configuration* state. Any card in the *Isolation* or *Configuration* state that receives a Wake[CSN] command with a parameter that does not match its CSN will transition to the *Sleep* state. All Plug and Play cards function as if their 72-bit serial identifier and their resource data come from a single serial device. The pointer to this data is reset to the beginning whenever a card receives a Wake[CSN] command that has a non-zero CSN value.
- Resource Data Register - One byte of resource data from the Plug and Play card is returned upon a read of this register when in the *Configuration* state. This data is always returned byte sequentially and the Status register must be read to confirm that resource data is available before the register can be read.
- Status register - Bit[0] of the status register indicates that the next byte of resource data is available to be read. If this bit is one, then data is available, otherwise resource data is not yet available. The Plug and Play software will poll this location until bit[0] is set, then the next data byte from the Resource Data register is read.
- Logical Device Number Register - This register is used to select the logical device on which the configuration commands to follow will operate. The MB86701/701A supports only a single logical device, so this register is not implemented. A read of this register returns 0x00.
- I/O Range Check Register - This register allows the Plug and Play software to determine if another card conflicts with the I/O port range that has been assigned to a logical device. The I/O range check works by having all I/O ranges that would be used by a logical device return 0x55 then 0xAA on I/O read commands. The Plug and Play software performs reads to all the ports that would be used by the logical device and verifies that the correct data is returned. If a conflict is detected, then the Plug and Play software relocates the I/O range of the logical devices a new location. Setting bit[1] of this register enables the I/O range check logic. Setting bit[0] forces the logical device to respond to I/O reads within its assigned I/O range with the value 0x55. If bit[0] is cleared, then the logical device responds to reads within its assigned I/O range with the value of 0xAA. This function operates only when bit[0] of the Activate register is not set.
- Activate register - The Activate register is a read/write register that is used to activate a logical device. An active logical device responds to all ISA bus cycles as allowed by its normal operation. Bit[0] is the activate bit. If it is set to "1" then the logical device is active, otherwise it is inactive.

I/O PORT

The MB86701/701A is equipped with a four-bit general purpose I/O port, PIO<3:0>, which can be used to control or monitor external events. Each of these pins can be programmed to be an input or an output. The signal direction is programmed via the I/O Data Direction Register, 0x21. The state of the pin is controlled by writing the data into the I/O Data Register, 0x20 (values for pins programmed as inputs are ignored). Writing a "1" sets the output high, while writing a "0" sets the output low. The current state of the pins can be determined by reading the I/O Data Register.

EEPROM

The PPIC interfaces to the serial EEPROM through a four-wire interface as described in the Signal Descriptions section of this data sheet. The EEPROM is an industry standard 93C56 or equivalent, a 2048-bit device which is internally organized as 128 words by 16 bits (smaller devices in this family can also be used).

It should be noted that the data is internally stored in the EEPROM in a bit-reversed format. That is, the least significant bit of the lower byte of data is stored in the most significant bit of the EEPROM word, while the most significant bit of the upper byte of data is stored in the least significant bit of the EEPROM word, as shown in the example below. This rearrangement of data is not important if the EEPROM is programmed via the PPIC, but must be considered if the EEPROM is programmed by other means.

DATA UPPER BYTE								DATA LOWER BYTE							
1	0	1	1	0	0	1	1	0	1	0	1	1	0	1	0

DATA IN EEPROM															
0	1	0	1	1	0	1	0	1	1	0	0	1	1	0	1

EEPROM Memory Map

The memory map of the EEPROM is shown in Table 14. Upon reset, an internal pointer to the EEPROM is initialized to address the first word of the EEPROM and the default configuration values (0x000 - 0x015) are read and automatically loaded into the appropriate registers, as detailed in Table 15. In the *Isolation* state, an additional nine bytes (0x016 - 0x01E, the Plug and Play Serial Identifier) are read from the EEPROM and loaded into an internal shift register for use during the card identification and isolation process. At this point, the internal pointer is pointing to the first byte of the card's resource data structure, 0x01F. When the card enters the *Configuration* state in response to the card winning the serial isolation protocol and having a CSN assigned, the resource data will be read and used as an input to the resource allocation process performed by the system software. If the card enters the *Configuration* state directly in response to the Wake[CSN] command, the nine byte serial identifier must be read first before the card's resource data is accessed because the pointer to the Serial EEPROM is reset to 0x16 in response to the Wake[CSN] command where the CSN matches the card's CSN and does not equal zero.

Table 14. EEPROM Memory Map

BYTE ADDRESS	CONTENTS
0x000 . . 0x015	**Default values for configuration registers.** See Table 15.
0x016 . . . . . 0x01E	**Serial Identifier** See Plug and Play Specification v1.0a, Table 2 and Section 6.1: Vendor ID Serial Number Checksum
0x01F 0x1FF	**Resource Data.** See Plug and Play Specification v1.0a, Section 6.1: PnP Version Number Identifier String Logical Device ID Resource Data Optional Vendor Defined Data(1) End Tag Optional Vendor Defined Data(2)

Notes:

1. Vendor defined data inserted as part of the Resource data must use standard formats per sections 6.2.2.10 and 6.2.3.4. of the PnP specification.
2. Vendor defined data inserted following the End Tag may use any format.

Table 15. Default Register Values in EEPROM

BYTE ADDRESS	CONTENTS
0x000	Reg. 0x41: Mem Base Add 0 [15:8]
0x001	Reg. 0x40: Mem Base Add 0 [23:16]
0x002	Reg. 0x42: Memory Control 0
0x003	Reg. 0x44: Mem Range 0 [15:8] or Mem Upper Limit 0 [15:8]
0x004	Reg. 0x43: Mem Range 0 [23:16] or Mem Upper Limit 0 [23:16]
0x005	Reg. 0x49: Mem Base Add 1 [15:8]
0x006	Reg. 0x48: Mem Base Add 1 [23:16]
0x007	Reg. 0x4A: Memory Control 1
0x008	Reg. 0x4C: Mem Range 1 [15:8] or Mem Upper Limit 1 [15:8]
0x009	Reg. 0x4B: Mem Range 1 [23:16] or Mem Upper Limit 1 [23:16]
0x00A	Reg. 0x61: I/O Base Add 0 [7:0]
0x00B	Reg. 0x60: I/O Base Add 0 [15:8]
0x00C	Reg. 0x63: I/O Base Add 1 [7:0]
0x00D	Reg. 0x62: I/O Base Add 1 [15:8]
0x00E	Mapped Reg. Address(1)
0x00F	Bit[0]: Reg. 0x30<0> = Activate Bit[1]: '1' = Assert /IOCS16 for /IOCS0 Bit[2]: '1' = Assert /IOCS16 for /IOCS1
0x010	I/O Range 0(1)
0x011	I/O Range 1(1)
0x012	Reg. 0x74: DMA Channel 0
0x013	Reg. 0x75: DMA Channel 1
0x014	Interrupt Request 0: Bits[3:0] = Reg. 0x70: Int. Level Bits[5:4] = Reg. 0x71: Int. Type Bit[6] = 0: INTA is active high Bit[6] = 1: INTA is active low
0x015	Interrupt Request 1: Bits[3:0] = Reg. 0x72: Int. Level Bits[5:4] = Reg. 0x73: Int. Type Bit[6] = 0: INTB is active high Bit[6] = 1: INTB is active low

Notes:

1. "Vendor Defined" registers not described in the Plug and Play Specification. See Register Descriptions section of this data sheet.

Reading Data from the EEPROM

In order to read the contents of the EEPROM, the PPIC must be placed into the *Configuration State*. If this state is entered from the *Isolation State*, the read address pointer will be pointing to the first byte of the Resource Data, byte 0x1F. If the *Configuration State* is entered directly from the *Sleep State*, the read address pointer will be pointing to the first byte of the Serial Identifier, byte 0x016.

The flow chart in Figure 2 outlines the process of reading data from the EEPROM. Data is read sequentially from the Resource Data Register, one byte at a time, starting at the address specified above. Note that the Status Register must be polled before each read of the Resource Data Register to assure that the data from the EEPROM has been obtained and is ready to be read

.

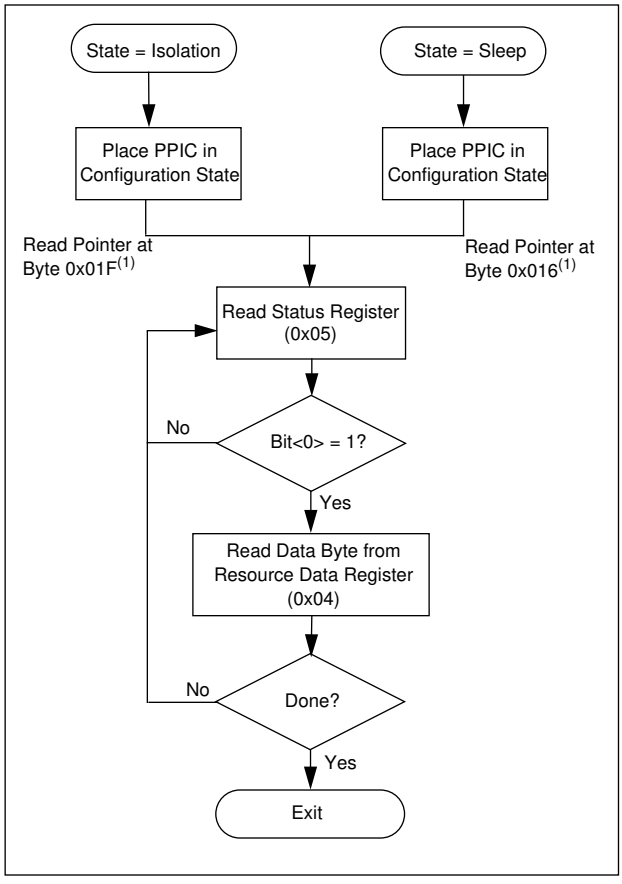


Figure 2. Reading Data from the EEPROM

Note:

1. Refer to Section 4.5 of the ISA Plug and Play Specification

Writing Data to the EEPROM

In order to write data into the EEPROM, the PPIC must be placed into the *Configuration State*. The PPIC contains a write address pointer which is set to point to address 0x000 in the EEPROM upon reset. Note that this pointer is separate from the read address pointer and is not affected by any EEPROM data read operations.

The flow chart in Figure 3 outlines the EEPROM write process. First, the EEPROM is write enabled. Data is then written sequentially, one word at a time, starting from address 0x000. As a final step, a Write Disable command is sent to the EEPROM to protect the data from any inadvertent writes. Note that a timeout equal to or longer than the specified EEPROM write cycle time (typically 10 ms) is required after the write command for each word of data.

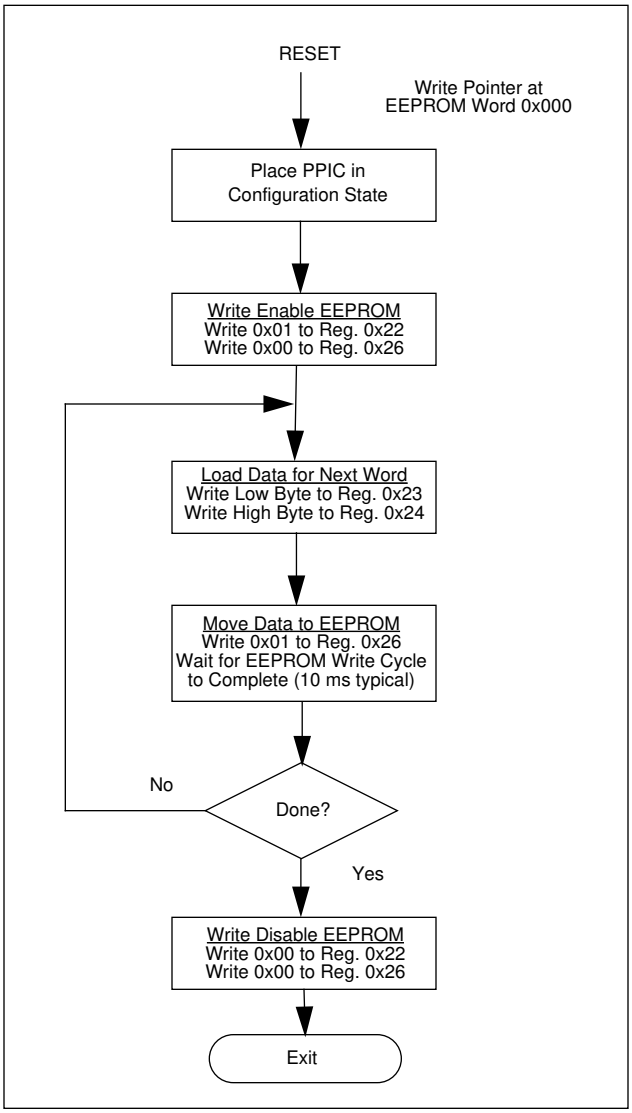


Figure 3. Writing Data into the EEPROM

MEMORY TO I/O MAPPING

In some applications, there is a FIFO or other local buffer that must be filled or emptied by the driver software. The MB86701/701A provides a special function that can improve system performance in such cases. Figure 4 illustrates the operation of this memory to I/O mapping function, which transforms any access to a specified memory window into an access to a specified I/O address. This allows the user of memory reference instructions such as string or block moves to move the data between the host and the peripheral device. Since these instructions normally execute faster than a loop of I/O reference instructions, system performance is improved.

The function employs the ADD<6:0>, /CS, /READ and /WRITE signals from the PPIC. ADD<6:0> is a value stored in an internal register which is loaded at reset from the default values stored in the EEPROM. It specifies the port offset (1-127) from I/O Base Address 0 and can be located inside or outside the I/O Range associated with that address. /CS is an active low composite chip select which is the logical-OR of IOCS0 and MCS0. MCS0 corresponds to the memory window which is to be mapped into {I/O Base Address 0 + offset} while IOCS0 defines the I/O window for normal I/O register access. While the /IOCS0 portion of /CS is active the ADD<6:0> pins output the ISA bus address from the SA<6:0> inputs and while the /MCS0 portion of the /CS is active these pins output the contents of the offset register. /READ and /WRITE are active low read and write strobes generated by the PPIC. These signals are composed of the /IOR (/IOW) input signal while /IOCS0 and /IOCS1 are active and the /MEMR (/MEMW) signal while /MCS0 is active.

To use this function, connect /CS to the chip select input of the I/O controller, the appropriate number of outputs from ADD<6:0> to the lower address lines, and /READ and /WRITE to the read and write inputs, respectively. Any system access to the window specified by Memory Base Address 0 and its corresponding range will now access the specified I/O register.

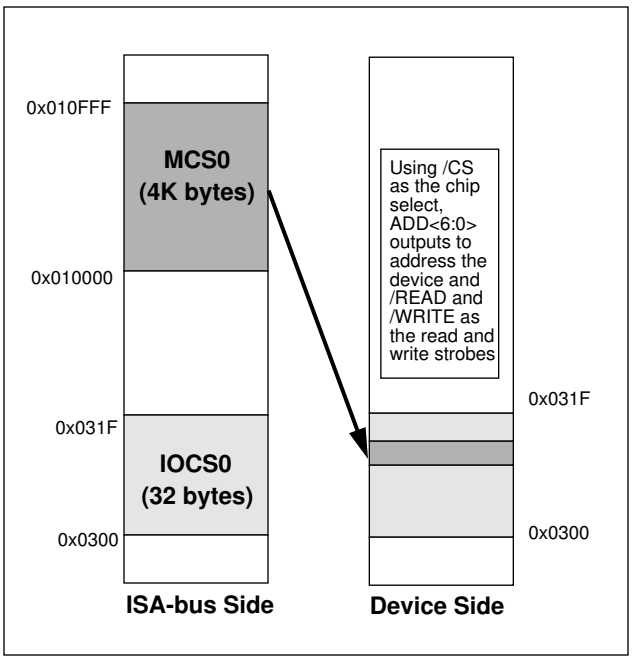


Figure 4. Memory to I/O Mapping Function Example

APPLICATIONS

Figures 5 and 6 illustrate typical applications of the MB86701/701A.

In Figure 5, the PPIC is combined with Fujitsu's MB86964 Ethernet controller with Twisted Pair transceiver to form a highly integrated Plug and Play ready Ethernet adapter card. The MB86964 uses one I/O chip select and one interrupt. A memory chip select is used to address the boot PROM or flash memory.

A SCSI controller implementation is shown in Figure 6. Here one I/O chip select and one interrupt are used by Fujitsu's MB86601 SCSI Protocol Controller. The associated dual port FIFO uses /CS, /READ, /WRITE and the ADD outputs to provide the memory I/O mapping function in order to improve data transfer performance between the host and the card. The remaining memory chip select is used to address the boot PROM or flash memory.

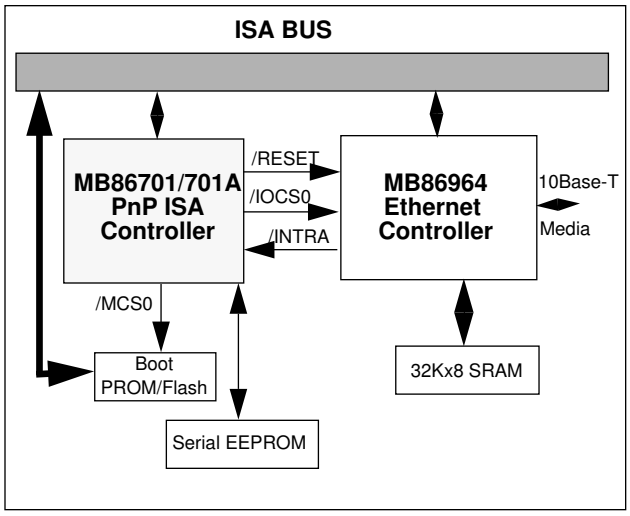


Figure 5. Typical MB86701/701A Application - Ethernet Controller

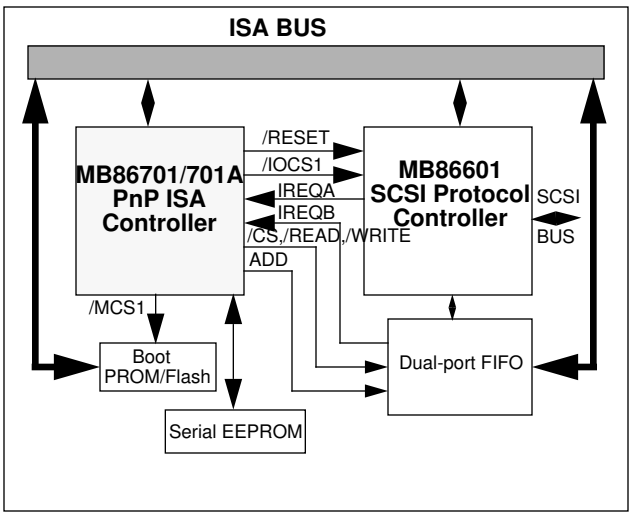


Figure 6. Typical MB86701/701A Application - SCSI Controller

DC CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER DESCRIPTION	MIN	MAX	UNITS
V_{DD}	Supply Voltage	-0.3	6.0	V
V_{IN}	Input Voltage	-0.3	V_{DD} + 0.3	V
V_{OUT}	Output Voltage	-0.3	V_{DD} + 0.3	V
T_{STG}	Storage Temperature	-40	+125	^{o}C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER DESCRIPTION	MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage	4.75		5.25	V
V_{IH}	High Level Input Voltage	2.4			V
V_{IL}	Low Level Input Voltage			0.4	V
T_A	Operating Temperature	0		+70	^{o}C

DC CHARACTERISTICS

SYMBOL	PARAMETER DESCRIPTION	CONDITION	MINIMUM	TYPICAL	MAXIMUM	UNIT
V_{IL}	Low Level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.2		V_{DD}	V
V_{OL1}(1)	Low Level Output Voltage	I_{OL} = 4mA	0		0.4	V
V_{OH1}(1)	High Level Output Voltage	I_{OH} = -2mA	4.0		V_{DD}	V
V_{OL2}(2)	Low Level Output Voltage	I_{OL} = 8mA	0		0.4	V
V_{OL3}(3)	Low Level Output Voltage	I_{OL} = 12mA	0		0.4	V
V_{OH3}(3)	High Level Output Voltage	I_{OH} = -4mA	4.0		V_{DD}	V
V_{OL4}(4)	Low Level Output Voltage	I_{OL} = 24mA	0		0.4	V
V_{OH4}(4)	High Level Output Voltage	I_{OH} = -8mA	4.0		V_{DD}	V
I_L	Input Leakage Current		-10		10	uA
I_{CCS}	Static Power Supply Current				100	uA
I_{CCA}	Active Power Supply Current				100	mA

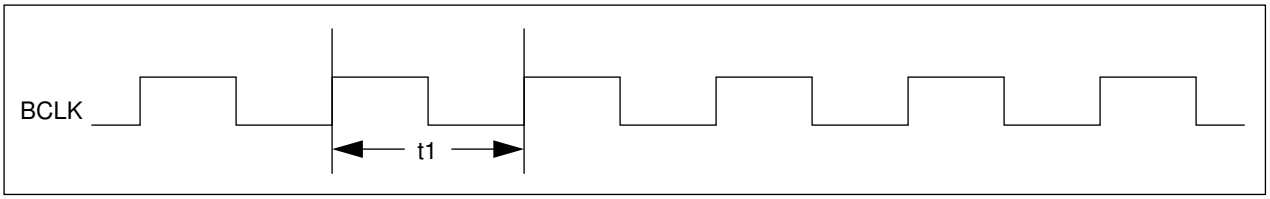
Notes:

1. Applies to O 4 and I/O 4 type outputs. See Pin Assignment Table.
2. Applies to O8 type outputs.
3. Applies to O 12 type outputs. See Pin Assignment Table.
4. Applies to O 24 and I/O 24 type outputs. See Pin Assignment Table

TIMING DIAGRAMS

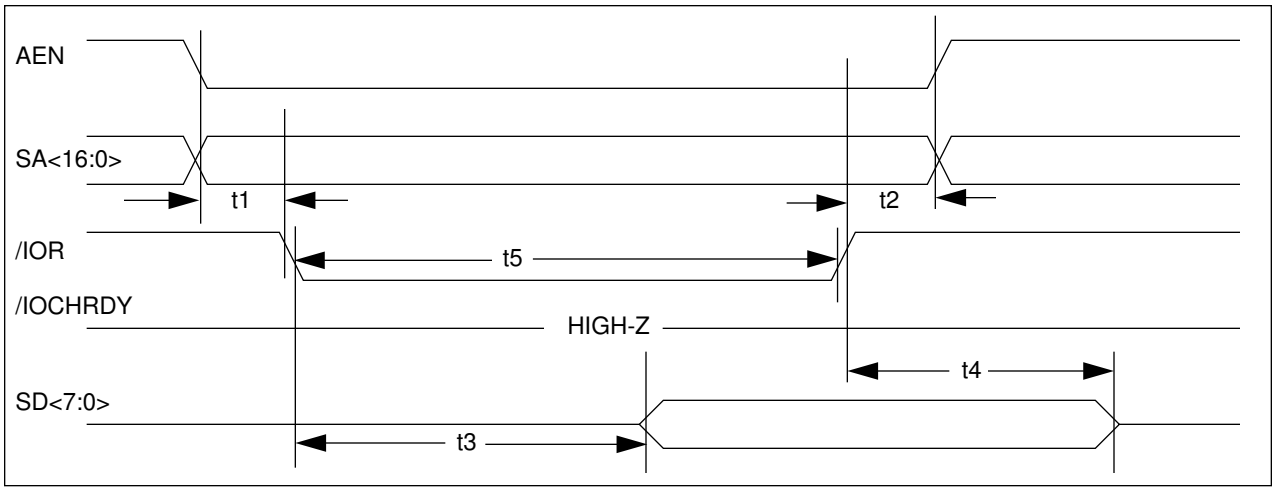
ALL SPECIFICATIONS ARE VALID OVER THE RECOMMENDED OPERATING CONDITIONS UNLESS OTHERWISE NOTED.

Table 15. BCLK Timing



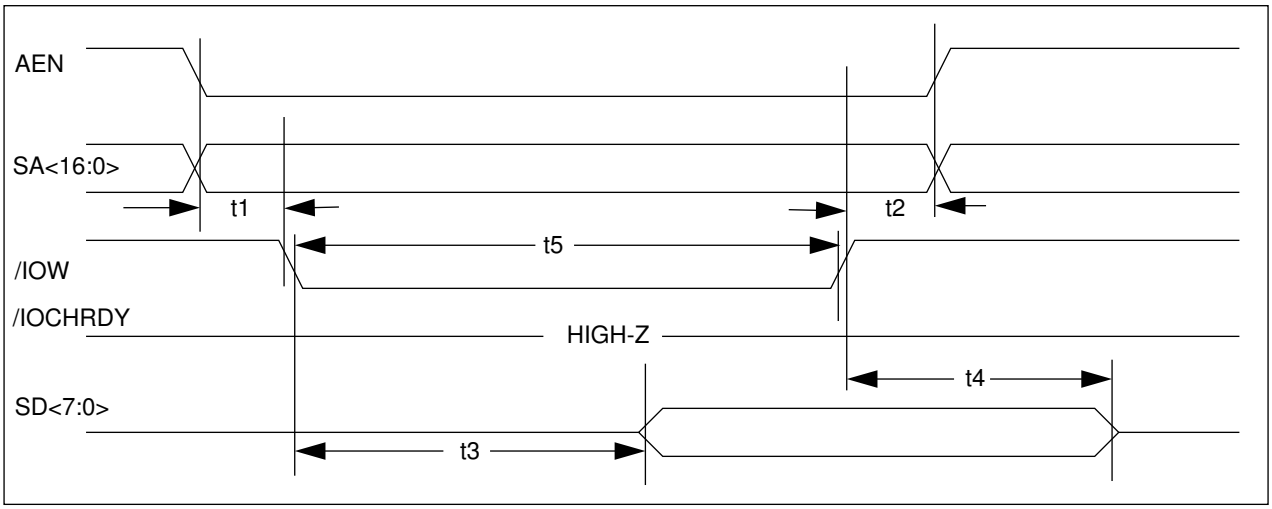
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t1	BCLK clock period	83.3	120	166.7	ns

Table 16. Internal Register Read Cycle



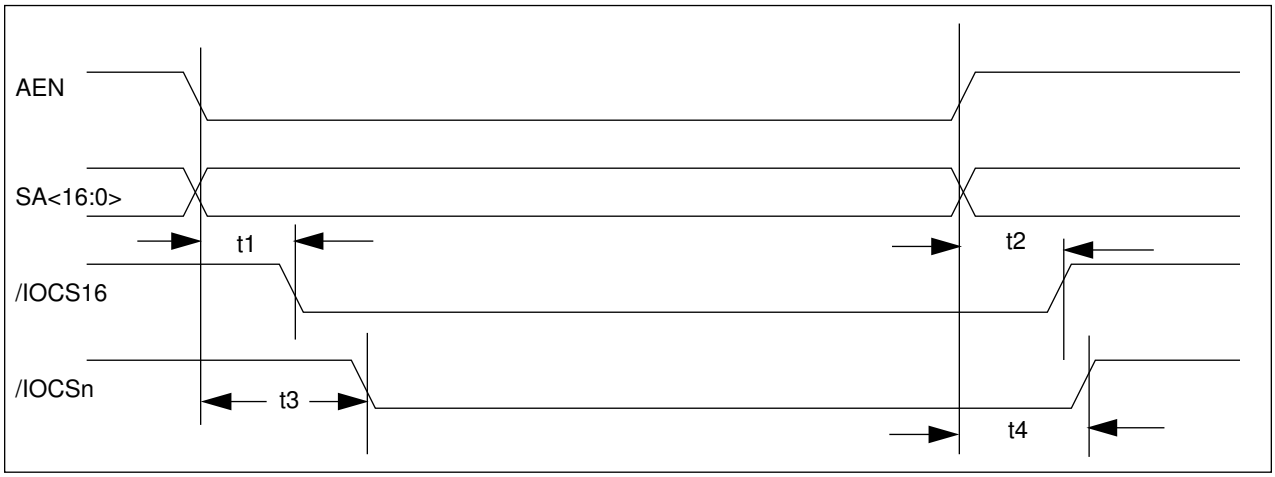
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t1	AEN low, SA<16:0> valid to /IOR low	89			ns
t2	/IOR high to AEN high, SA<16:0> invalid	40			ns
t3	/IOR low to SD<7:0> valid		7	20	ns
t4	/IOR high to SD<7:0>	3	7		ns
t5	/IOR low time	4			BCLKs

Table 17. Internal Register Write Cycle



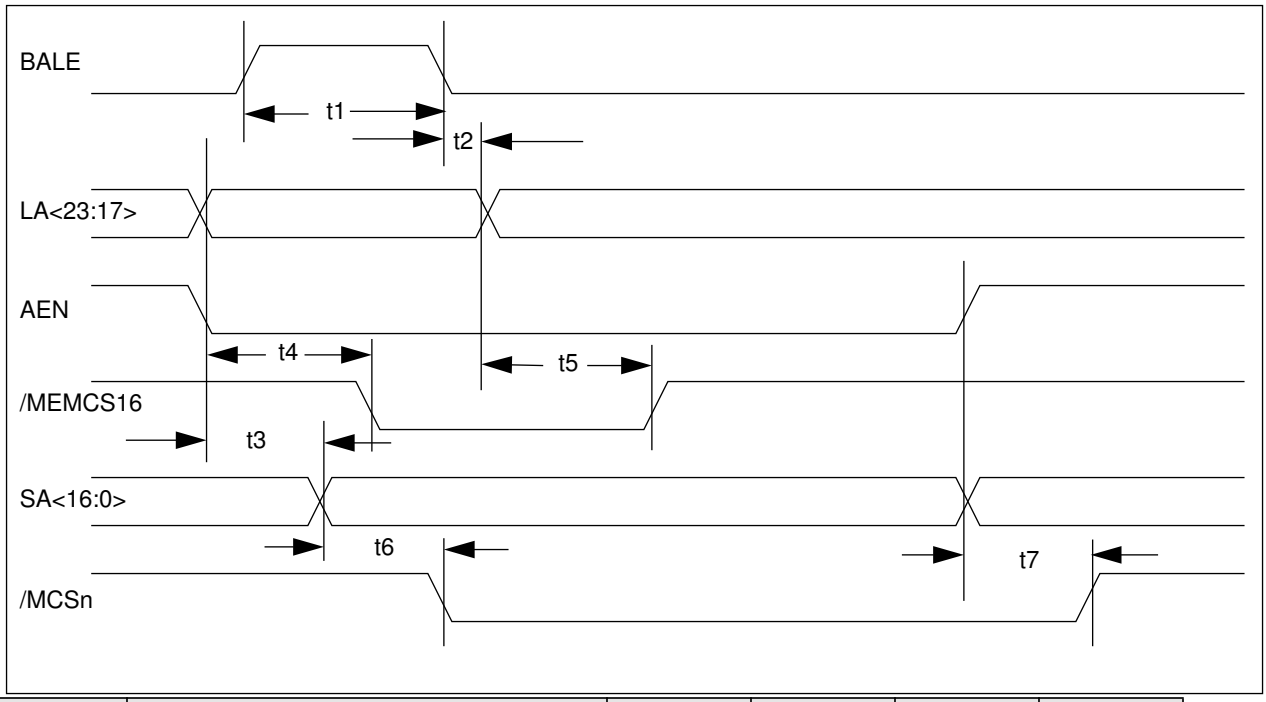
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t1	AEN low, SA<16:0> valid to /IOW low	89			ns
t2	/IOW high to AEN high, SA<16:0> invalid	40			ns
t3	/IOW low to SD<7:0> valid	-4			ns
t4	/IOW high to SD<7:0> invalid	0			ns
t5	/IOW low time	4			BCLKs

Table 18. I/O Chip Select Generation Cycle



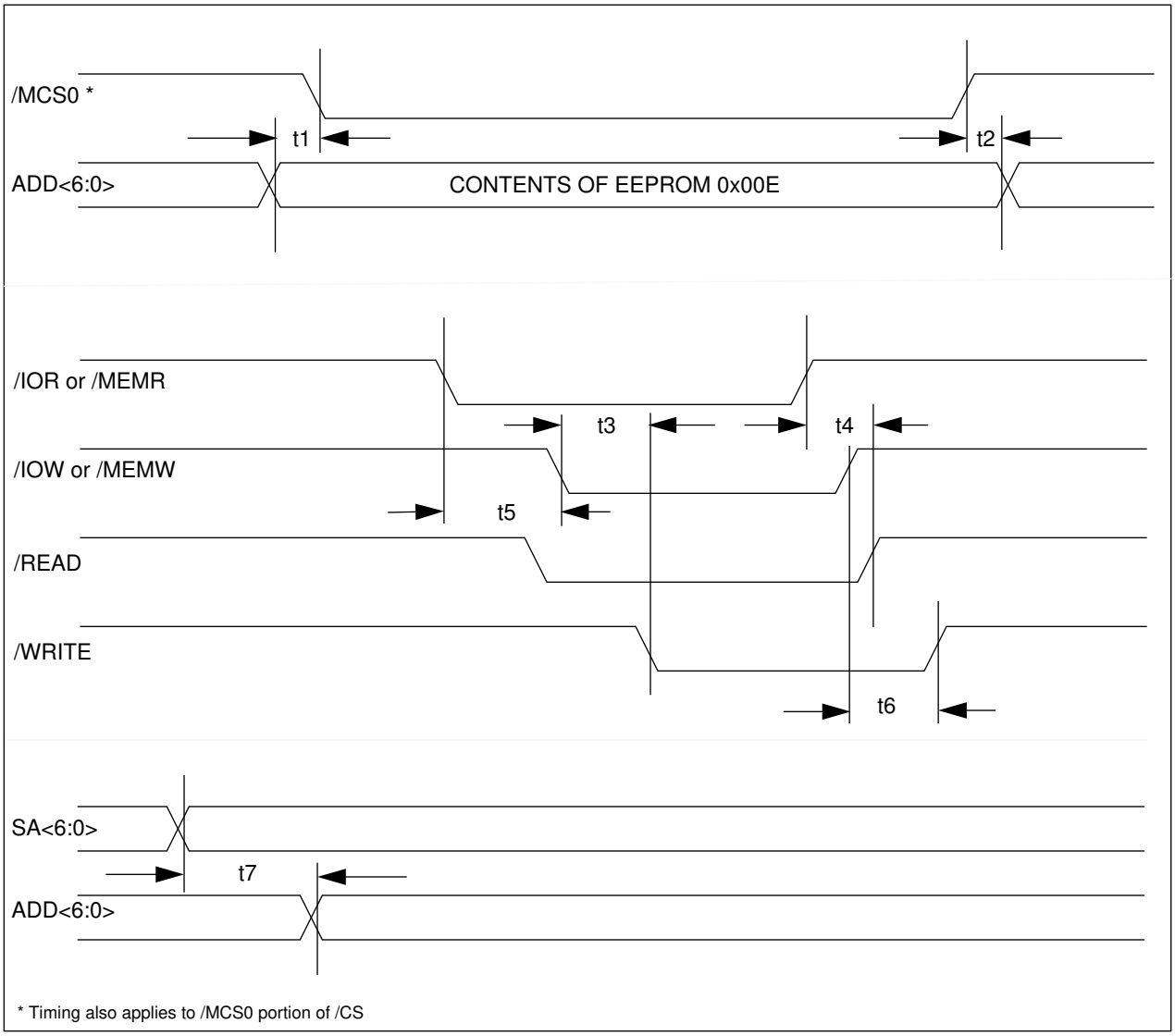
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t1	AEN low, SA<16:0> valid to /IOCS16 low			28	ns
t2	AEN high, SA<16:0> invalid to /IOCS16 high	3	7		ns
t3	AEN low, SA<16:0> valid to /IOCSn low (depends on pull-up resistor value)		11	28	ns
t4	AEN high, SA<16:0> invalid to /IOCSn high	3	7		ns

Table 19. Memory Chip Select Generation Cycle



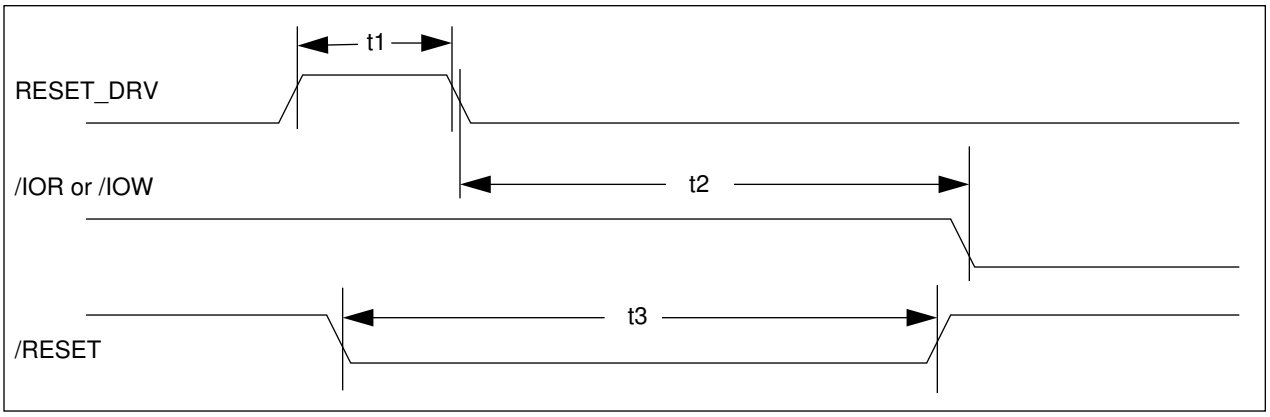
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UN
t1	BALE pulse width	48			ns
t2	BALE low to LA<23:17> invalid	15			ns
t3	AEN low, LA<23:17> valid to SA<16:0> valid	0			ns
t4	LA<23:17> valid to /MEMCS16 low		8	18	ns
t5	LA<23:17> invalid to /MEMCS16 high (depends on pull-up resistor value)	3	8		ns
t6	SA<16:0> valid to /MCSn low		12	30	ns
t7	AEN high, SA<16:0> invalid to /MCSn high	3	10		ns

Table 20. Memory Mapping Signal Timing



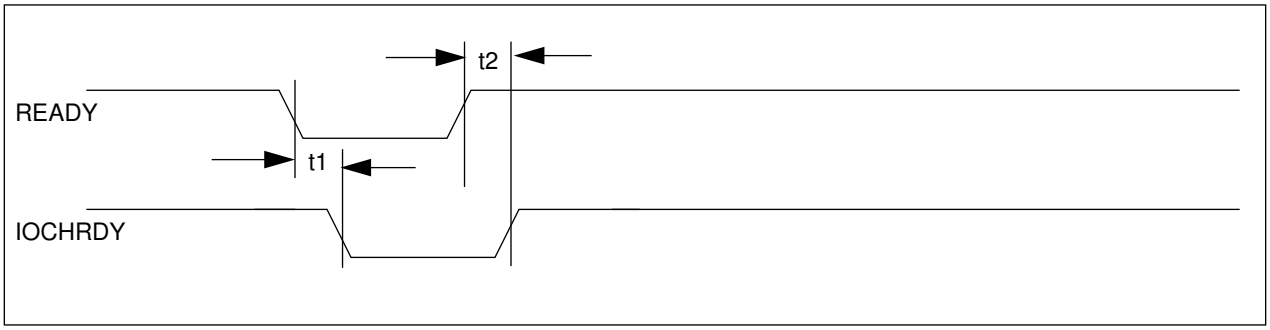
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t1	ADD<6:0> valid to /MCS0 low	1			ns
t2	/MCS0 high to ADD<6:0> invalid	0			ns
t3	/IOW or /MEMW low to /WRITE low		6	16	ns
t4	/IOR or /MEMR high to /READ high	2	7		ns
t5	/IOR or /MEMR low to /READ low		6	15	ns
t6	/IOW or /MEMW high to /WRITE high	0	6	16	ns
t7	SA<6:0> valid to ADD<6:0> valid		14	33	ns

Table 21. RESET_DRV Timing



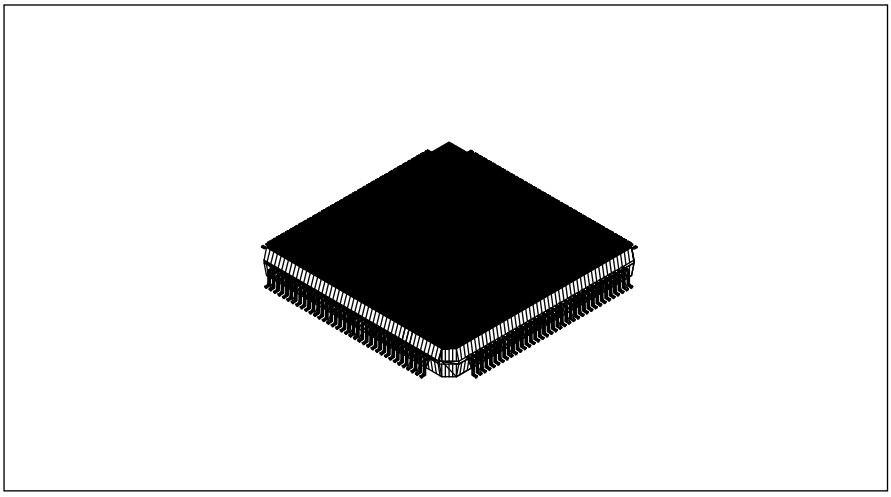
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t1	RESET_DRV pulse width	4			BCLKs
t2	RESET_DRV low to first /IOR or /IOW low for an internal MB86701/701A register	1,000			us
t3	/RESET output pulse width		8,192		BCLKs

Table 22. IOCHRDY Timing

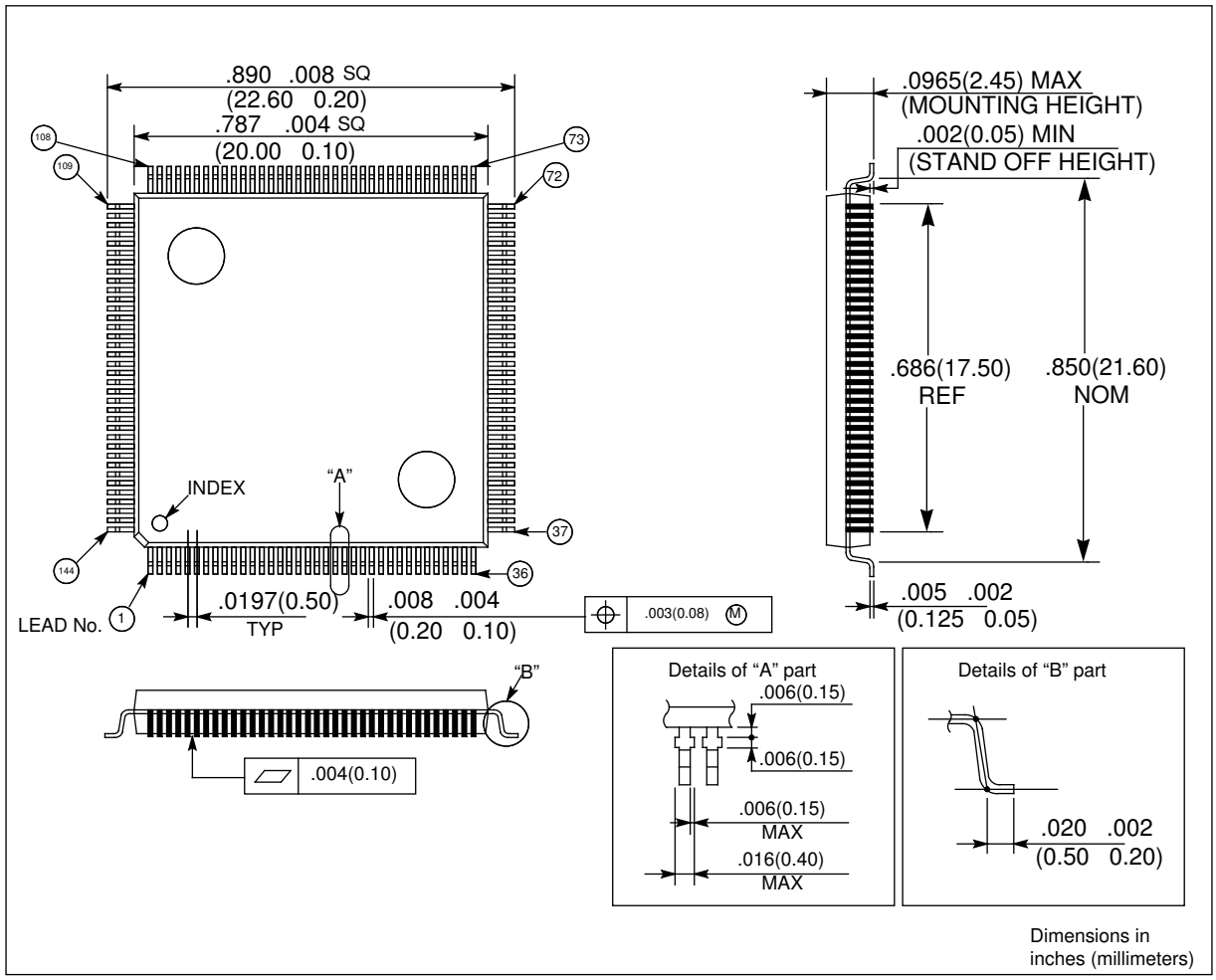


SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t1	READY low to IOCHRDY low		8	16	ns
t2	READY high to IOCHRDY high (depends on pull-up resistor value)		8	16	ns

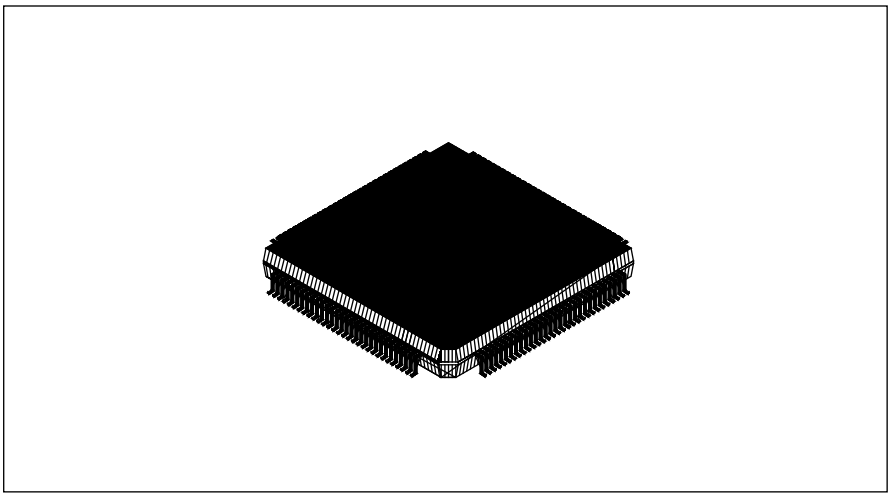
PACKAGE INFORMATION - MB86701



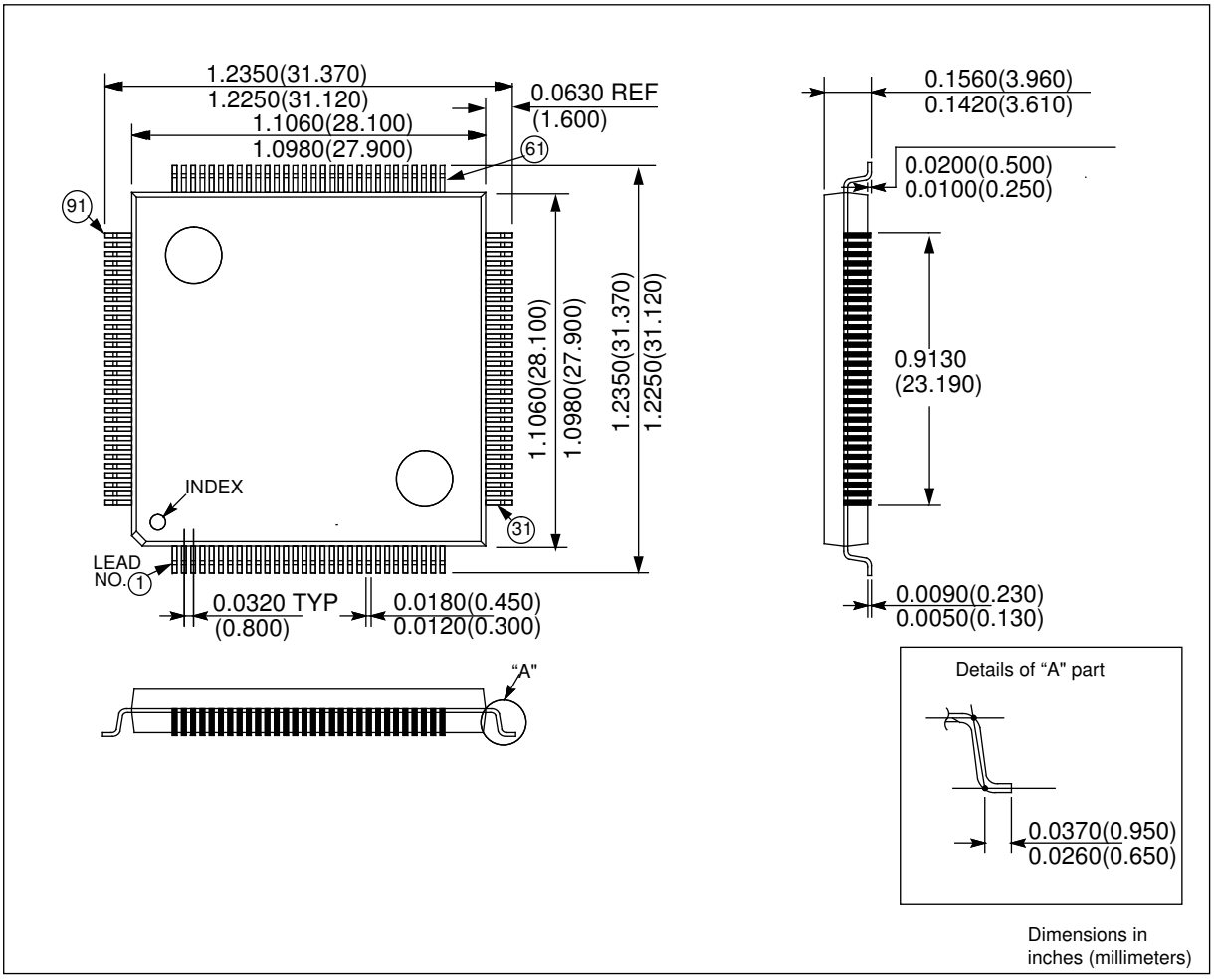
144-LEAD PLASTIC FLAT PACKAGE



PACKAGE INFORMATION - MB86701A



120-LEAD PLASTIC FLAT PACKAGE



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