CIRRUS LOGIC

CL-SH351

Product Bulletin

FEATURES

Microcontroller Interface:

- Supports high-speed microcontroller interfaces (e.g., 16-MHz 8051, 12-MHz 68HC11, 30-MHz HPC460X3)

SCSI Interface:

- Supports SCSI-2 Initiation and Target modes
- Supports asynchronous DMA/PIO transfers up to 3 MBytes/sec.
- Supports synchronous DMA/PIO transfers up to 10 MBytes/sec.
- Supports up to 15-byte synchronous transfer offsets and 13 programmable transfer periods
- Controls synchronous transfer overrun/underrun
- Controls arbitration, selection, and reselection in hardware
- Detects selected and reselected conditions automatically
- Integrates 48-mA SCSI bus drivers in the interface
- Provides control for the external differential driver option

Sector Formatter:

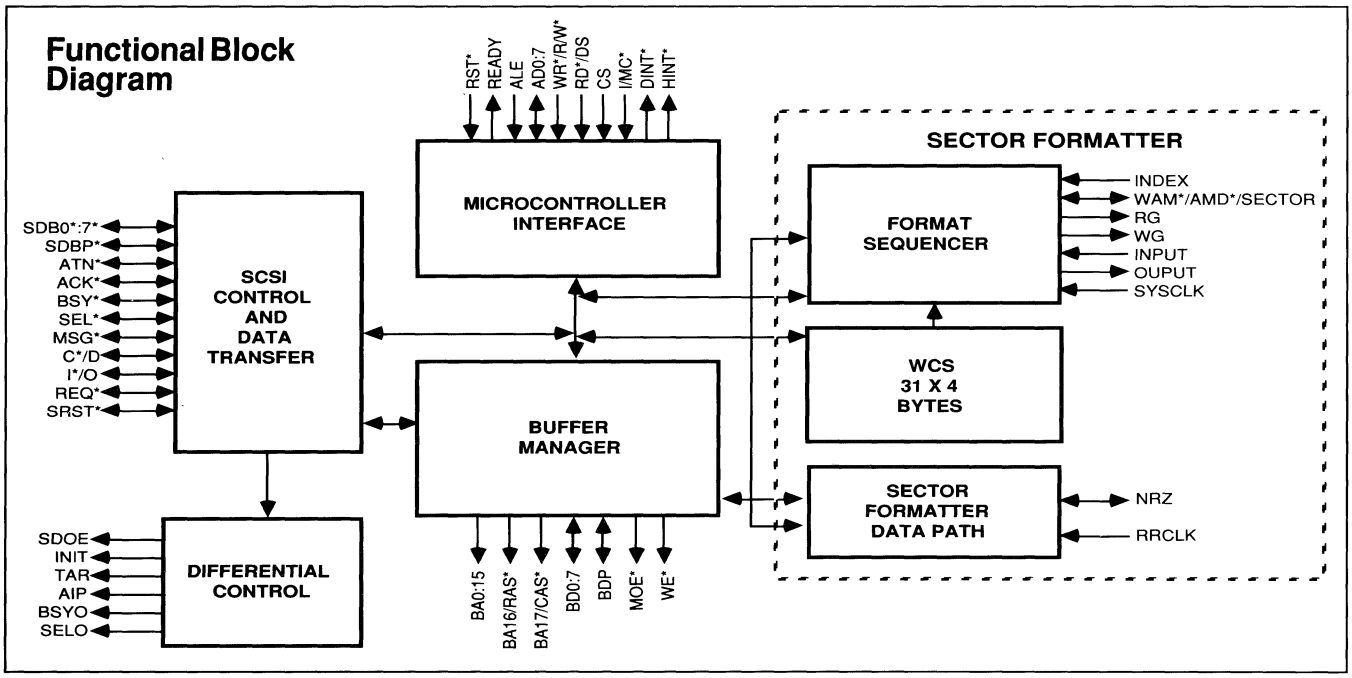
- Programmable Format Sequencer Writable Control Store (WCS-31 x 4 bytes)
- Supports up to 32-MHz NRZ data rates *(cont.)*

High-performance Synchronous/Asynchronous Integrated SCSI Disk Controller

OVERVIEW

The CL-SH351 is a VLSI component that provides the majority of the hardware necessary to build a Small Computer System Interface (SCSI) Winchester disk controller. The CL-SH351 design combines a high-speed local microcontroller port, extensive hardware support for the SCSI interface, a two-channel Buffer Manager, and an advanced Sector Formatter. With the addition of only a few discrete components for the device-level interface, the CL-SH351, along with a local microcontroller, system ROM and RAM, and an optional data separator, completes a disk controller subsystem with high performance at a low overall cost. *(cont.)*

Functional Block Diagram



FEATURES (cont.)

- Allows split data field processing for embedded servo and zoned designs
- Provides selectable 16-bit CRC or 32/56-bit ECC with proprietary error correction hardware †

Buffer Manager:

- Dual-channel, circular buffer control with priority resolution
- Direct buffer addressing up to 256 KBytes of SRAM and 1 MByte of DRAM
- Permits concurrent buffer memory throughput up to 14 MBytes/sec. in DRAM page mode and 15 MBytes/sec. for SRAM
- Odd-parity data verification between the SCSI bus and the Sector Formatter

Technology:

- 100-pin Quad Flat Pack (QFP) package
- Advanced, low-power, double-metal CMOS technology

OVERVIEW (cont.)

A local microcontroller provides the CL-SH351 with initial operating parameters that include disk sector format, the type and size of buffer memory, and SCSI Host control. During data transfer operations, the CL-SH351 requires only minimal intervention from the local microcontroller. The microcontroller-to-CL-SH351 communication path is a multiplexed address and data bus similar to that provided by the Intel® 8051- and the Motorola® 68HC11-class of controllers. (There is a configuration signal available to allow for either family of data control signal methods). The CL-SH351 has centralized status registers with interrupt capability. These features allow firmware designers flexibility in writing polled loops or interrupt handlers that provide real-time process control critical in embedded controller drive applications.

The SCSI Host interface is designed for compliance with the proposed SCSI-2 specification and supports synchronous transfer capability of up to 10 Mbytes/sec. This ensures long-term compatibility for both the hardware and the firmware developed around the CL-SH351. The SCSI interface logic includes integrated high-current (48-mA) drivers for the single-ended option, as well as signals for control of the external logic necessary to implement the differential transceiver option. Both the asynchronous and synchronous transfer protocols are supported in either Initiator or Target mode. Routine bus control operations, such as arbitration, selection and reselection, are automatically sequenced in hardware. This method of implementing the SCSI interface makes the SCSI protocol firmware extremely flexible and very efficient.

The Sector Formatter provides the disk data and control functions. The Sector Formatter is capable of handling NRZ data rates up to 32 Mbits/sec. The Sector Formatter is subdivided into a Format Sequencer and the Sector Formatter Data path. The Format Sequencer uses a 31-word-by-4-byte Writable Control Store (WCS) to hold a user-written program. This program contains the control information for the disk track and sector format. The Sector Formatter Data path consists of the NRZ data handling circuitry that includes the serializer/deserializer (SERDES), the ECC and CRC error control logic, the SERDES parity logic, and the data signals to the Buffer Manager interface.

The Buffer Manager controls the flow of data between the host and disk interfaces. These interfaces store and retrieve data from the buffer memory using interleaved access cycles. The actual buffer memory may be implemented with static or dynamic RAM devices. The CL-SH351 Buffer Manager is programmable to provide all of the necessary address and control signals for RAM devices of varying access times. Up to 256 KBytes of SRAM can be directly addressed by the CL-SH351. As much as 1 MByte of DRAM is directly supported by the CL-SH351, with specific control for 64K, 256K, and 1-Mbit devices. In DRAM mode, refresh is generated automatically through a third channel to the buffer memory, in addition to the concurrent disk and host accesses.

† A U.S. patent has been issued on Cirrus Logic's proprietary 56-bit ECC.

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PIN DESCRIPTION

Symbol	*Pin Number*	*Type*	*Description*
Microcontroller Interface Pins			
DINT*	17	O, OD, Z	Disk Interrupt
CS	18	I	Chip Select
WR*/R/W*	19	I	Write Strobe/Read/Write
RD*/DS	20	I	Read Strobe/Data Strobe
READY	21	O	Ready
I/MC*	24	I	Intel/Motorola
HINT*	28	O, OD, Z	Host Interrupt
AD0:7	34-30, 27, 23-22	I/O	Local Microcontroller Address/Data Bus
ALE	35	I	Address Latch Enable
RST*	40	I	Reset
SCSI Bus Interface Pins			
SDB0*:7*	52-54, 57, 59-62	I/O, Z	SCSI Data Bus
SDBP*	64	I/O, OD	SCSI Data Bus Parity
ATN*	68	I/O, OD	SCSI Attention
BSY*	69	I/O, OD	SCSI Busy
ACK*	70	I/O	SCSI Acknowledge
SRST*	72	I/O, OD	SCSI Reset
MSG*	73	I/O, OD	SCSI Message
SEL*	76	I/O, OD	SCSI Select
C*/D	77	I/O, OD	SCSI Command/Data
REQ*	78	I/O	SCSI Request
I*/O	79	I/O, OD	SCSI Input/Output
SCSI Bus Control Pins			
SDOE	50	O	SCSI Data Bus Output Enable
INIT	55	O	Initiator
TAR	56	O	Target
AIP	63	O	Arbitration in Progress
BSYO	67	O	Busy Out
SELO	71	O	Select Out
Buffer Manager Interface Pins			
BA17/CAS*	5	O	Buffer Memory Address 17/Column Address Strobe
BA16/RAS*	14	O	Buffer Memory Address 16/Row Address Strobe
MOE*	15	O	Memory Output Enable
WE*	16	O	Write Enable
MCE*	29	O	Memory Chip Enable
SYSCLK	41	I	System Clock
BD0:7	83-87, 89, 92-93	I/O	Buffer Memory Data Bus
BDP	94	I/O	Buffer Memory Data Parity
BA0:15	95-100, 3-4, 6-13	O	Buffer Memory Address Lines
Sector Formatter Interface Pins			
INPUT	36	I	Format Sequencer Input
INDEX	37	I	Index
WAM*/AMD*/SECTOR	39	I/O	Write Address Mark/Address Mark Detect/Sector
RG	43	O	Read Gate
WG	44	O	Write Gate
RRCLK	45	I	Read Reference Clock
NRZ	46	I/O	Non-return to Zero
OUTPUT	47	O	Format Sequencer Output
Power and Ground Pins			
BGND	1, 2, 88	N/A	Buffer Ground Pins
LGND	25, 26, 42	N/A	Logic Ground Pins
N/C	48, 80, 81	N/A	No Connection; Reserved for Future Use
+5V	38, 51, 90, 91	N/A	Power Supply (+5) Pins
SGND	49, 58, 65-66	N/A	High Current SCSI Ground Pins
	74, 75, 82		

Note: (*) denotes negative true signal. I indicates input pin; O indicates output pin; I/O indicates input/output pin; OD indicates open drain output pin; Z indicates tri-state output or input/output pins. All unused input pins must be tied to GND or VDD appropriately. SGND, BGND and LGND are connected to three separate ground rings internally.

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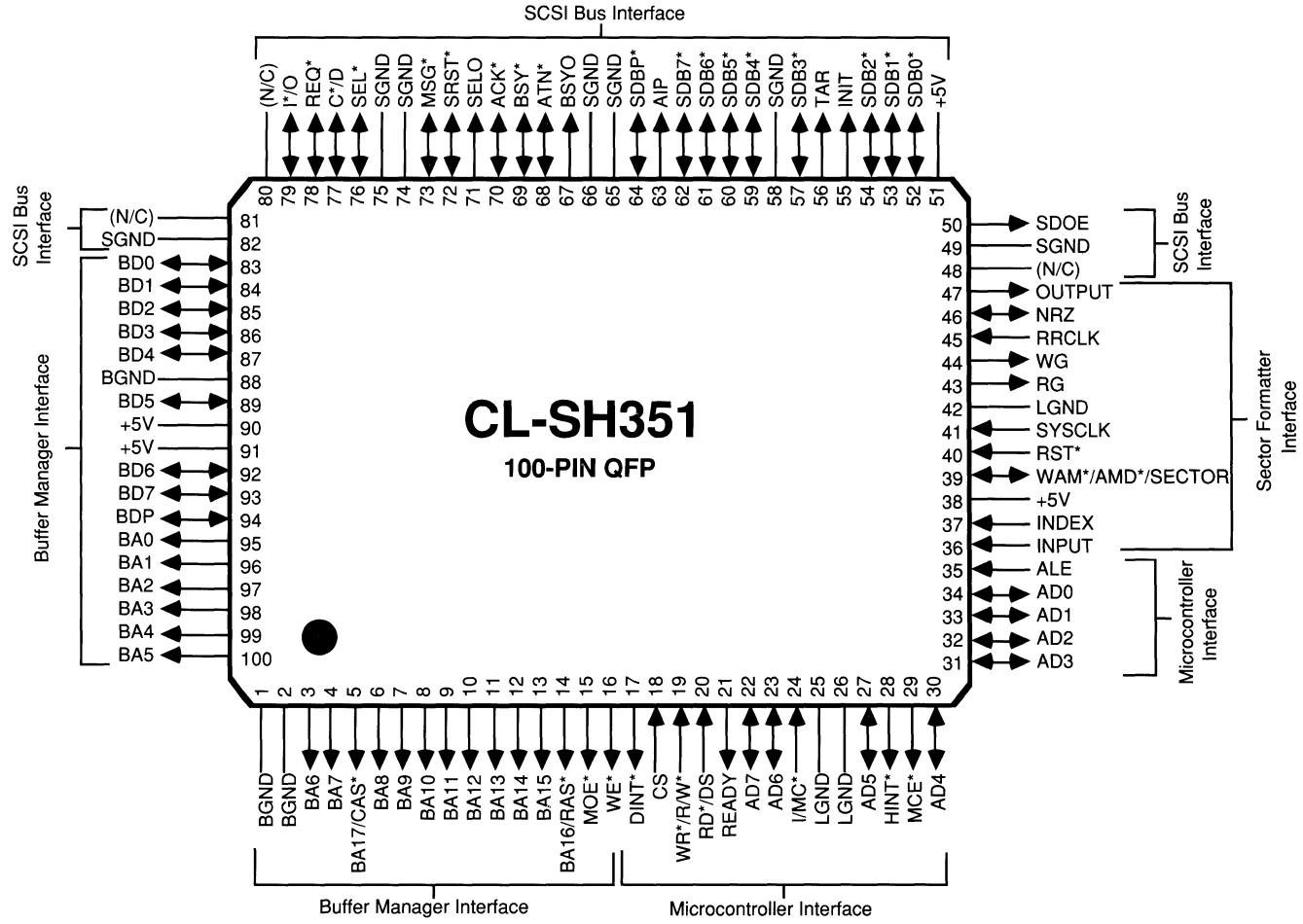
ADVANTAGES

Unique Features	Benefits
• *Programmable wait states for microcontroller*	Allows the fastest microcontrollers to operate without degrading bus performance.
• *Pin-configurable microcontroller data control interface*	Allows for direct connect to Intel- or Motorola-style microcontrollers.
• *Separate disk and host microcontroller interrupts*	Supports faster, more direct interrupt processing by microcontroller.
• *15-byte offset in synchronous mode*	Greater flexibility for synchronous data transfer negotiations.
• *16-byte FIFO for automatic PIO transfers*	Decreases command and information transfer overhead.
• *External differential SCSI bus support*	Allows connection to any SCSI system with longer cable lengths.
• *Two Buffer Manager DMA channels*	Enables read-look-ahead for high performance.
• *Direct 256K SRAM and 1M DRAM addressing*	Increases buffer size alternatives to support caching.
• *Odd through parity buffer verification*	Improves data integrity between host and disk data transfers.
• *Variable buffer segmentation logic*	Allows protected data segments in buffer.
• *Advanced-programmable branch conditions in the Writable Control Store (WCS) program*	Supports flexible, automated defect management and retry algorithms.
• *Conditional Format Sequencer execution of up to four paths*	Supports end-of-track, retry and defect management code.
• *Programmable read synchronization timeout*	Simplifies ID and Data Field searches.
• *ECC hardware correction circuitry*	Enables high-speed ECC correction within a sector time period.
• *Multiple data field processing within the ECC*	Provides support for embedded servo drives, zoned drives and large defect skipping.



*Denotes negative true signal.

100-pin Quad Flat Pack (QFP) Pin Diagram

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The Company

Cirrus Logic, Inc., is a leading supplier of high-integration peripheral controller circuits for mass storage, graphics, and data communications. The company also produces state-of-the-art software and firmware to complement its product lines. Cirrus Logic technology is used in leading-edge personal computers, engineering workstations, and office automation.

The Cirrus Logic formula combines proprietary S/LA™† IC design automation with system design expertise. The S/LA design system is a proven tool for developing high-performance logic circuits in half the time of most semiconductor companies. The results are better VLSI products, on-time, that help you win in the marketplace.

Cirrus Logic's extensive quality assurance program — one of the industry's most stringent — ensures the utmost in product reliability. Talk to our systems and applications specialists; see how you can benefit from a new kind of semiconductor company — Cirrus Logic.

† U.S. Patent No. 4,293,783

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