

# Errata for *PlayCD™ CL480 MPEG System Decoder User's Manual*

92-0480-102

September 29, 1994

This document describes changes to the *PlayCD™ CL480 MPEG Video Decoder User's Manual* (PN 92-0480-101). The changes are divided into (1) Known Hardware Errata, (2) Known Microcode Errata, (3) Text and Picture Changes, and (4) Addressing Considerations.

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The following list describes the problems that are expected to be present in the ES1.3 revision CL480 parts. These problems will be corrected by version ES2 silicon available in December 1994.

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## Known Hardware Errata

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### 1.1 Optional ROM is no longer Optional

Due to space limitations in the 4-Mbit DRAM used with the CL480, the 32K of space for microcode will not be sufficient. Therefore, portions of microcode will need to be loaded from ROM during normal operation. This loading will be handled by the CL480 and will not require any host intervention. However, all CL480 designs must boot from ROM and therefore must include at least a 27C512, 64K ROM, connected to the DRAM interface as shown in the CL480 User's Manual.

## Known Hardware Errata

### 1.2 Signal Polarity

In ES1.3, the video interface *VOE* pin and the host interface *R/W* pin are documented as active high signal polarity (*VOE* and  $\overline{R/W}$ ). In version 2.0 of the silicon and subsequent versions, these signals will have active low polarity ( $\overline{VOE}$  and  $\overline{R/W}$ ).

Workaround: If the external host connects its  $\overline{R/W}$  signal to the CL480's  $\overline{R/W}$  signal and/or the board toggles *VOE*, the board should be designed with an inverter(s), which can be replaced with a zero-ohm resistor for ES2.

### 1.3 $\overline{DTACK}$ Timing

On host interface read cycles, the CL480 signals availability of data by asserting  $\overline{DTACK}$  low. However, in version 1.3,  $\overline{DTACK}$  may go low several nanoseconds before the data is valid.

Suggested Workaround: Place a flip-flop clocked by *GCLK* between the CL480 and the host on the  $\overline{DTACK}$  signal in order to further delay  $\overline{DTACK}$ . If  $\overline{DTACK}$  is being read by a programmable I/O of the host, the host software can delay reading the most significant byte of data until some time slightly after  $\overline{DTACK}$  goes low.

### 1.4 ROM Read Cycle Timing

In ES1.3, the CL480 releases the ROM chip enable signals at the same time that data is latched into the CL480.

Suggested workaround : Slow down the  $\overline{CE}[1:0]$  signal with an RC network such as a 1K-ohm series resistor and a 50 pF capacitor to ground. The user should program the ROM access time to be 2 *GCLKs* longer than otherwise necessary.\*\*

### 1.5 Video Bus YCbCr Pin Assignments

When the video unit of ES1.3 is in 16-bit YCbCr mode, the CbCr[7:0] outputs are on pins *VD*[7:0] and the Y[7:0] outputs are on pins *VD*[15:9]. In 8-bit YCbCr mode on ES1.3, the video data is on pins *VD*[15:8]. In ES2, YCbCr video data is output as shown in the CL480 databook (PN 92-0480-101). There is no change in the pins for RGB mode.

Suggested workaround: For YCbCr mode, place jumpers on the board.

### 1.6 Voltage Range

The minimum voltage that ES1.3 will recognize as a "1" on an input is over 2V when the CL480 is operating at 2.7V. To compensate for this, ES1.3 must operate at 3V to 3.6V if the chip is receiving TTL voltage levels.

### 1.7 I<sup>2</sup>S Support

The data format for Philips' I<sup>2</sup>S CD data input format is not supported on ES1.3 but is included in ES2. A programmable logic device could be used to convert the I<sup>2</sup>S format to a format supported on ES1.3.

The following list contains the differences between the behavior of microcode version 1.00 and its description given in the CL480 manual (PN 92-0480-101). These differences will be corrected by version 2.0 microcode available in February 1995.

- Host interface signal must be enabled (HOST\_ENA = 1).
- "Starting layer" variable option of the Play() command (mentioned in the Play() command description on page 12-20 and in the DRAM Configuration Area on page 12-8) is not supported. After reset or the Reset() command, microcode assumes CD-DA format and will switch to CD-ROM mode only after detection of a sector sync.
- Scan() command is not supported. Applications should use successive Play() and Pause() commands instead.
- SetBorderColor(), SetWindow(), FlushBitstream() and Inquire-BufferFullness() commands are not supported.
- DisplayStill(start1, start2) is not supported (but the other two DisplayStill() commands are supported).
- The GOP-V, SEQ-V, SCN and END-V interrupt events of the SetInterruptMask() command are not supported.

This section of this errata contains descriptions, repeated in their entirety where practical, with typographical conventions used as follows:

- Material that is being deleted is shown with a strikethrough mark; for example: ~~this comes out~~.
- New material is always underlined; for example: this is new.

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## 2 Known Microcode Errata

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## 3 Text and Picture Changes

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## Addressing Considerations

There are two CL480 manual text changes, numbered 1 and 2:

1. The polarity and address of the *Int* bit of the *HOST\_int* register given in the text on page 10-5 should be changed as follows:

(normal) 0x0F

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<i>Res</i>							<i>Int</i>	<i>Res</i>							

  

Field	Bit	Default	Description
<i>Int</i>	9	<del>output</del> -inout	Interrupt request

*If you want to change the Int bit: (1) read out the entire register, 0xFEFF; (2) AND the value that you want to write with 0xFEFF, 0xFDFF, and then (3) write back this register.*

2. The text which describes the two memory chip-enable pins should be changed as follows: On page 9-20, the signal shown on pin 33,  $\overline{MCE}_{[1]}$ , should instead be shown as  $\overline{MCE}[1]$ . Likewise, both memory chip-enable signals should be shown as  $\overline{MCE}[0]$  and  $\overline{MCE}[1]$  as they appear for pins 32 and 33, respectively, in Table 9-16 on page 9-22.

### 4 Addressing Considerations

Register addresses (Chapter 10) are shown in the manual as 16-bit (word) addresses, while DRAM locations (Section 12.3) are shown as byte addresses. Since access to all CL480 on-chip registers and off-chip (local) DRAM must be 16-bits in length, you must convert the DRAM byte addresses to word addresses by dividing them by two.