Application Note 17

Clock Sources on the VIDC20 Graphics Controller

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Change Log

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1 Introduction

In order to facilitate the high resolution screen modes that VIDC20 is capable of producing, a suitable high frequency clock must be applied. As the screen mode is changed, the pixel rate must also change. This can be done via the various clock inputs, by the on-chip *pre-scaler*, or by using an external *voltage controlled oscillator* in conjunction with the on-chip phase comparator, to form a phase-locked-loop (PLL).

It is intended that most systems be built with a phase-locked-loop system. The required circuitry is simple, and allows a high degree of flexibility. The advantages are that all the necessary clock frequencies can be derived from the one circuit, and so the requirement for multiple on-board crystals and clock switching circuitry is eliminated.

Please refer to the VIDC20 data sheet while reading this application note.

2 Clock Sources

VIDC20 has 3 primary inputs for its pixel clock: **hclk**, **vclki**, and **rclk**. The intention is that **vclki** and **rclk** be used to drive the phase comparator, and that **hclk** only used to provide the highest frequency clock, if this frequency is above the maximum VCO frequency.

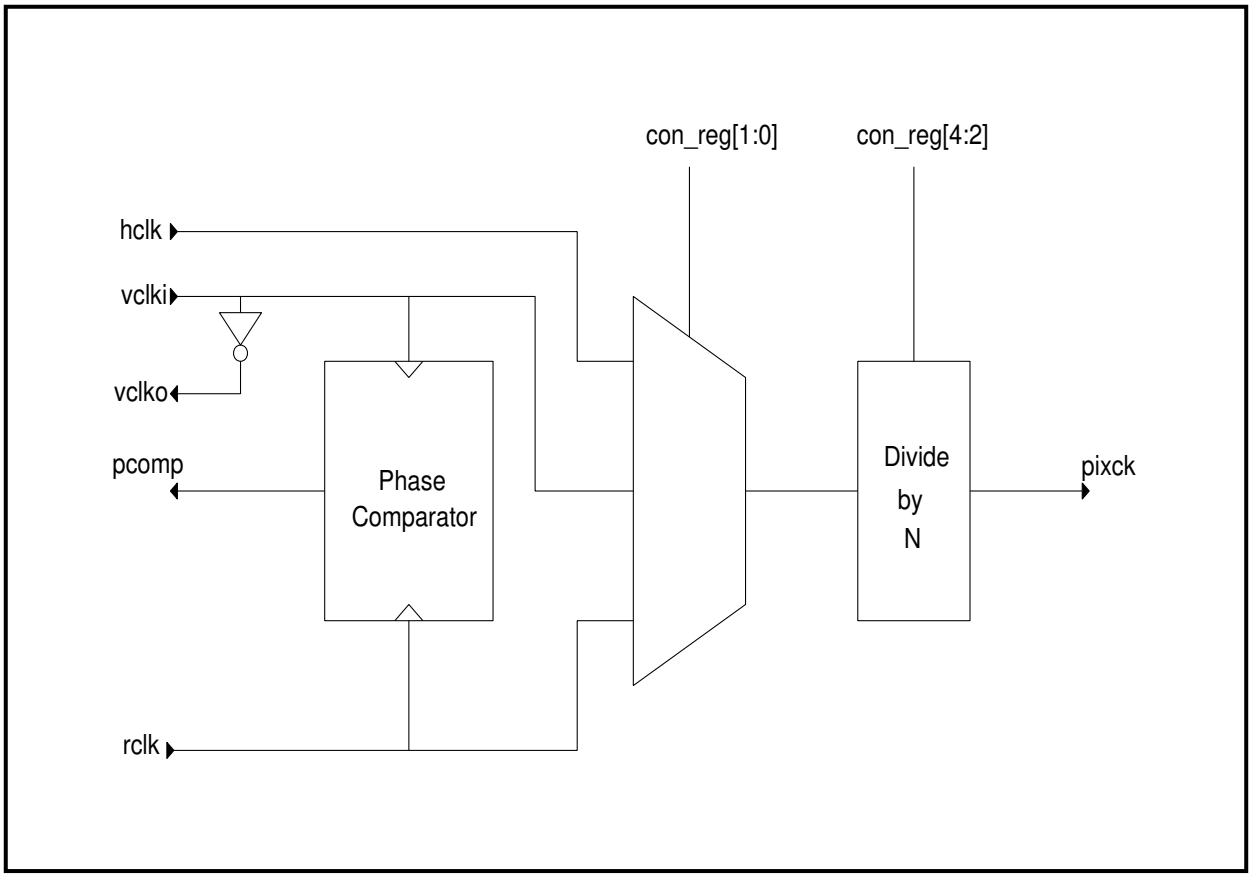

Figure 2-1: VIDC20 Internal Clock System

In addition to the pixel clock senses, there are two other clock inputs, **busclk** and **sclk**. **busclk** is independent of the pixel rate and is used to time DMA data transfers when in synchronous operation. This clock runs synchronous to the memory system, typically at 16MHz.

sclk can be used to drive the sound system. The VIDC10 compatible sound system expects to be run from 16MHz. This can be provided directly from **sclk**, or by applying 24MHz on **rclk** (there is a divide-by-1.5 in the sound system). The digital sound system may run at a different frequency, (low MHz range), and this must be applied directly on **sclk**. The pixel clock source is selected by programming bits 0 and 1 of the control register. The pixel clock selected can then be passed through a pre-scaler which can divide the clock by between 1 and 8. This is done by programming bits 2 to 4 of the control register. Refer to ❍*Figure 2-2: Control Register*.

Note that any unused clock pin should be tied LOW.

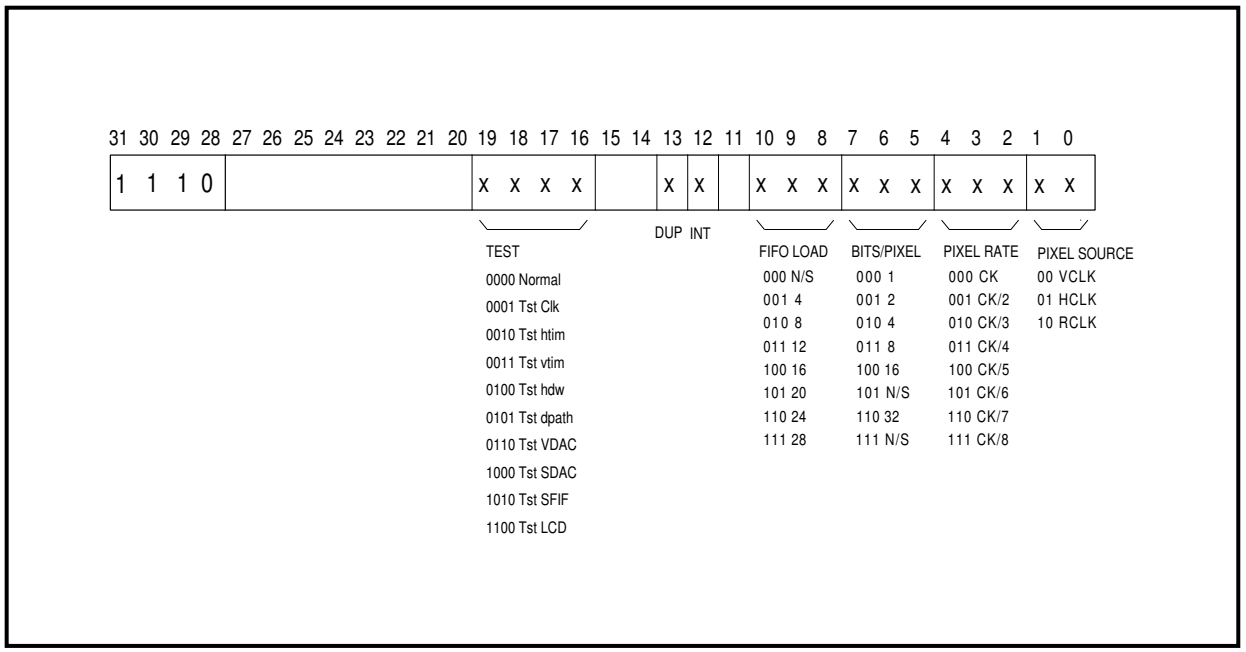

Figure 2-2: Control Register

3 Using the Phase Comparator

VIDC20 contains a phase comparator which, in conjunction with an external voltage controlled oscillator (VCO), can be used to build a phase-locked-loop. The phase comparator comprises two counters and a phase detector. The counters are pre-loadable down counters, one clocked from **rclk**, and the other clocked from **vclki**. The moduli of the counters is programmed in the Frequency Synthesizer Register.

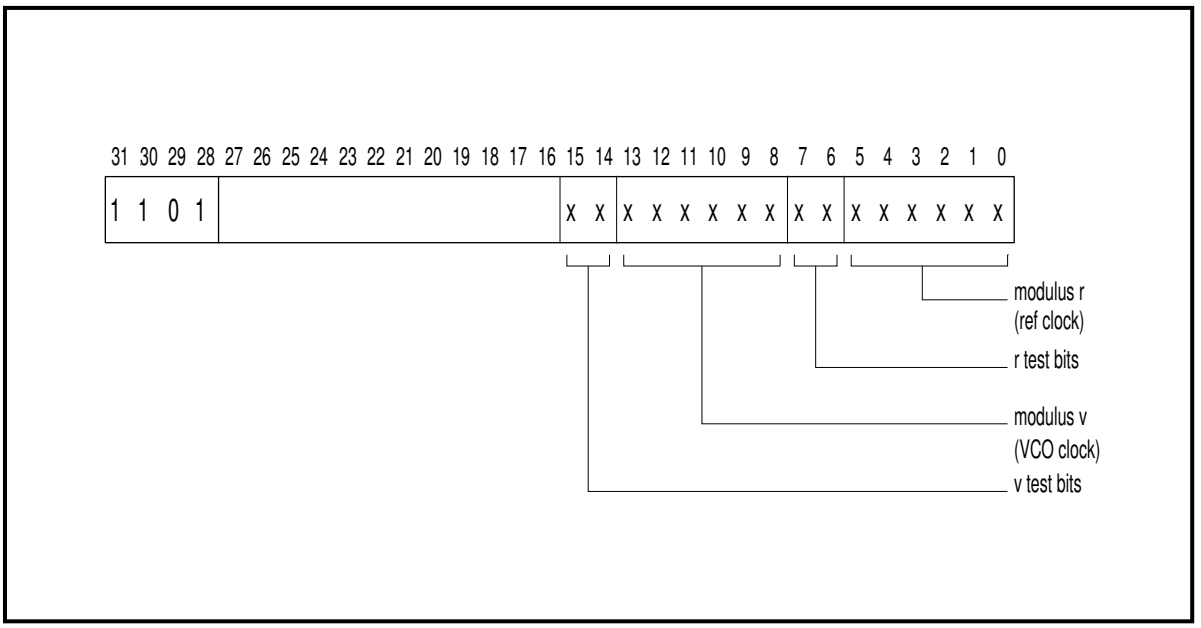

Figure 3-3: Frequency Synthesizer Register

In this register, the test bits have the following meaning:

bit [6] — force **pcomp** HIGH and driven

bit [7] — clear r-modulus counter

bit [14] — force **pcomp** LOW and driven

bit [15] — clear v-modulus counter

These bits are only programmed during test and at reset (see section *4 Phase Comparator Reset* on page 5). The **rclk** input provides a reference clock which is recommended to be 24MHz. The **vclki** input is driven from the output of the VCO, and it is this which is selected as the pixel clock.

The VCO is driven by VIDC20's **pcomp** output, which for most of the time is at the tri-state value. When the VCO's frequency needs to be increased, **pcomp** goes high, and vice-versa for when the frequency needs to be decreased. The **pcomp** output needs to be filtered before applying to the VCO.

The choice of filter and VCO are left to the user. A very simple and effective system can be built using an 74AC04 inverter pack, and a very simple LC filter. The filtered VCO output controls the operating voltage of the 74AC04 device. This system is shown in *Figure 3-4: Suggested VCO/PLL Circuit* on page 4, and gives an enormous range of frequencies (LF to hundreds of MHz). Since the output of this VCO is AC coupled, **vclki** needs to be biased at the mid voltage point. This is done by connecting a large resistor between **vclki** and **vclko** (**vclko** is the inversion of **vclki**).

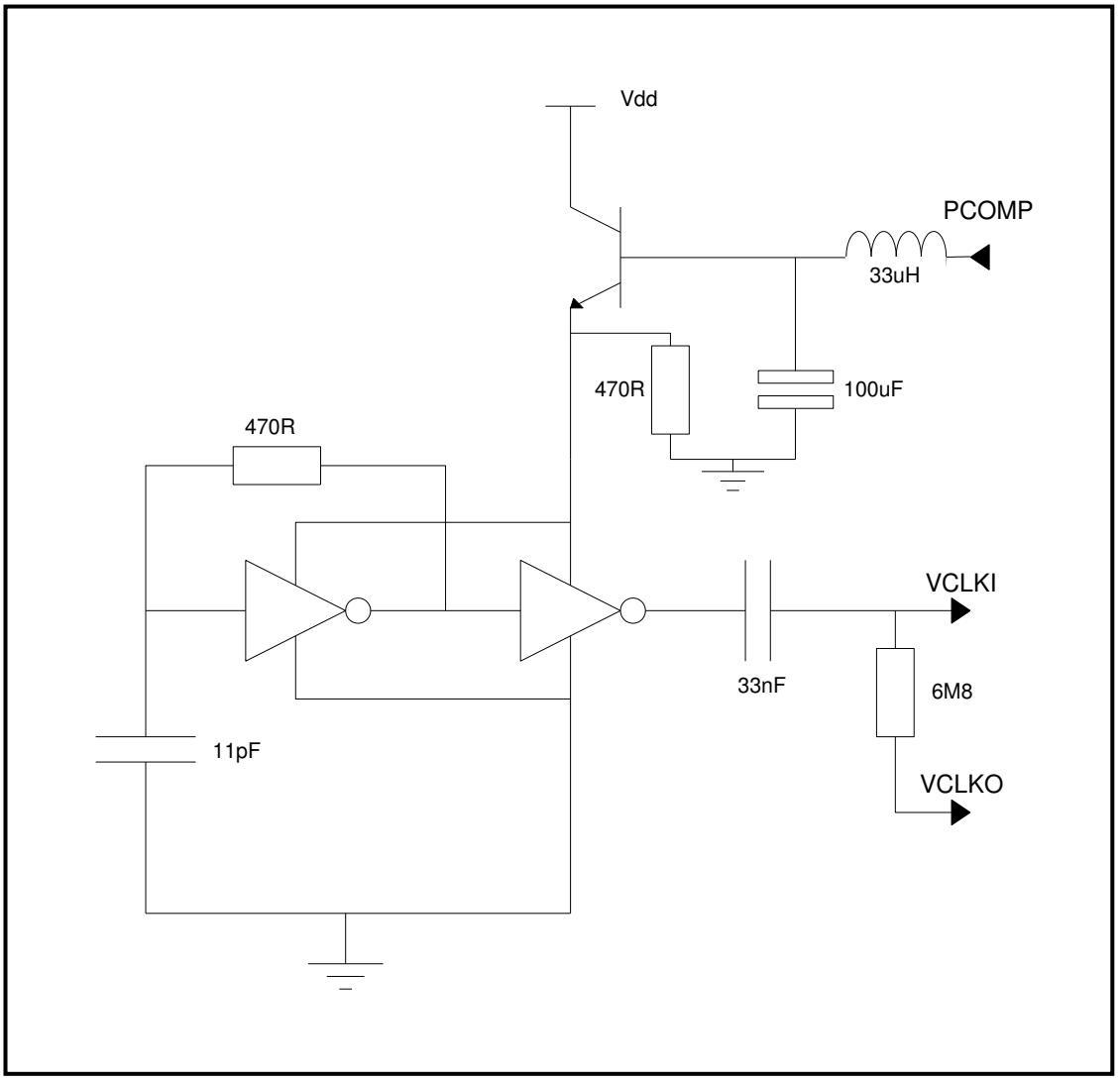

Figure 3-4: Suggested VCO/PLL Circuit

The actual frequency of the VCO is determined by the ratio of the v-modulus to the r-modulus as follows.

$$F_{vco} = F_{ref} \times \frac{\text{V-modulus}}{\text{R-modulus}}$$

(Note that for a modulus of r, r-1 is programmed, and likewise for the v-modulus.)

Table 3-1: Voltage Controlled Oscillator Response gives a list of useful frequencies with corresponding values of r and v moduli, assuming a reference frequency of 24MHz. There are many values of r and v which give the same ratio. The lower the values, the more frequently the output of the VCO will be updated and so the r and v values should be chosen to suit the response of the filter.

r-modulus	v-modulus	VCO Frequency/MHz
3	1	8.0
4	2	12.0
3	2	16.0
2	2	24.0
41	43	25.171
50	59	28.320
3	4	32.0
2	3	36.0
31	58	44.903
12	35	70.0

Table 3-1: Voltage Controlled Oscillator Response

4 Phase Comparator Reset

The phase comparator and VCO form a closed loop feedback system which has potential for going unstable. If the system powers up in the state where the **pcomp** output is trying to drive the VCO's output higher and higher, it will very quickly reach a frequency which the phase comparator cannot resolve and recovery will be impossible.

To avoid this, the following reset procedure must be applied carefully:

1. The Frequency Synthesizer Register test bits can be used to force the phase comparator's output either HIGH or LOW. Program bits 15, 14 and 7 HIGH and bit 6 LOW soon after power up.
2. Program the r- and v-moduli with values such that r is greater than v. This forces the VCO's frequency to decrease.

When the real pixel rate is to be programmed, it should be done in two steps:

1. The values of the r- and v-moduli should be programmed, but the test bits left in the initialisation state.
2. All the test bits should be cleared.

The VCO will then ramp up to its operating frequency. Subsequently, a change of frequency can be achieved simply by reprogramming the r- and v-moduli.

5 VIDC10 Compatibility

The simplest use of VIDC20 will be in VIDC10 upgrades, and backwards compatibility is provided for this. VIDC10 requires pixel rates of 8, 12, 16 and 24MHz, and it is not necessary to build a phase-locked-loop system just for this.

All the required frequencies can be catered for by using a 48MHz clock and a simple *divide-by-2* circuit. The 48MHz is applied to the **vclki** input, and the 24MHz, from the divide-by-2, is applied to the **rclk** input. In this way, the VIDC10 compatible sound system will work at all of the old sample rates without modification.

With **vclki** selected as the pixel clock, the pixel rates can all be produced by programming the pre-scaler accordingly. This also allows a 48MHz pixel rate screen to be displayed.

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