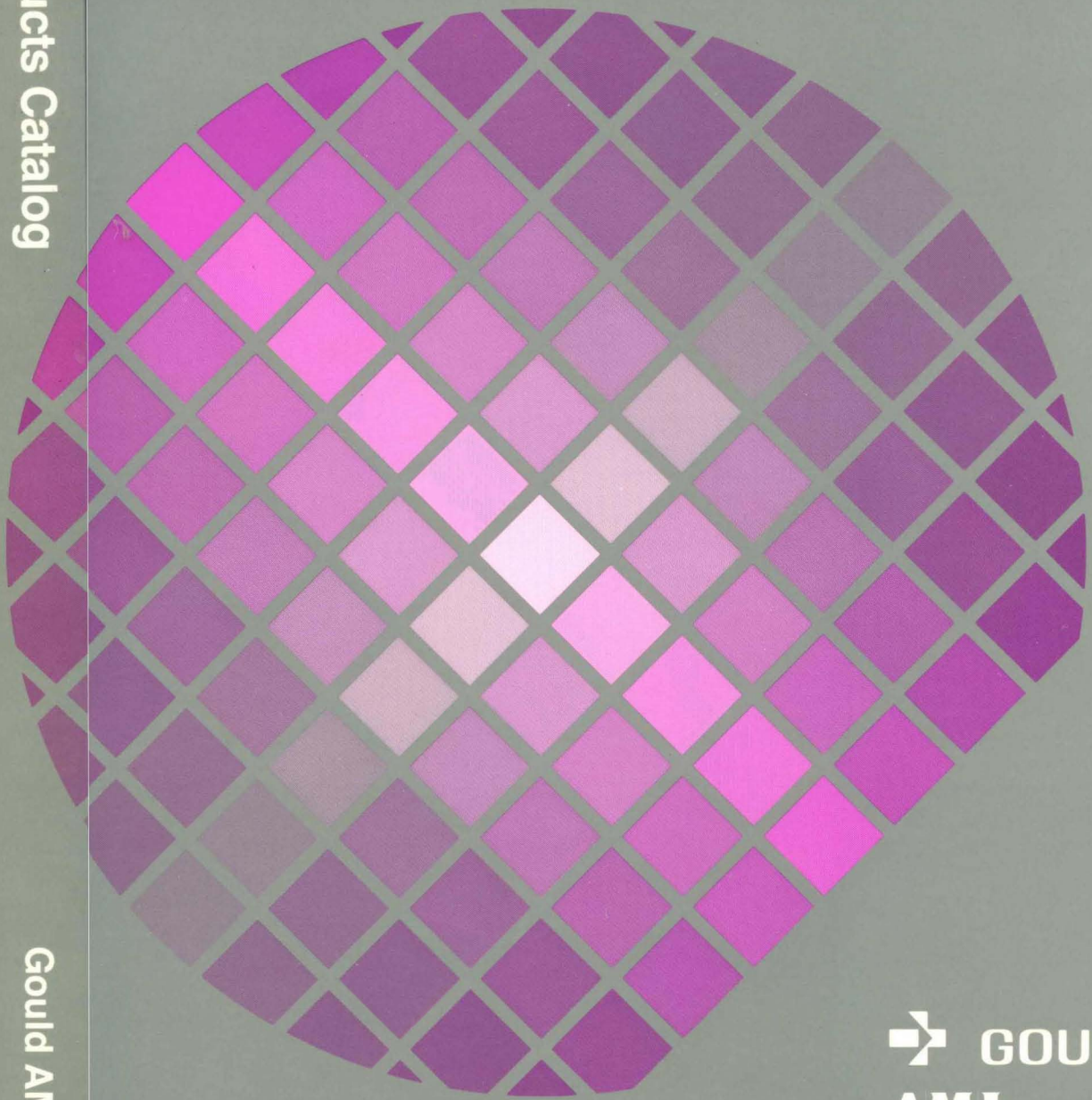
1990 Products Catalog



GOULD

AMI Semiconductors

1990 Products Catalog

Gould AMI

1990 Products Catalog

Gould AMI
2300 Buckskin Road
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Telephone: (208) 233-4690

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Introduction

Gould AMI, a division of Gould, Inc., is headquartered in Pocatello, Idaho and is the semiconductor industry leader in the design and manufacture of application specific integrated circuits. It manufactures special circuits for leading computer manufacturers, telecommunications companies, automobile manufacturers, consumer and military product companies worldwide.

Gould AMI has always focused on customer needs. As the original architect of Application Specific Integrated Circuit (ASIC) technology, Gould has a rock solid foundation and knows that great service, short development spans, good first silicon, competitive production prices, and the highest quality product are what it takes to keep our customers competitive. From the early days of hand-drawn custom through the CAE/CAD boom, to today's silicon compilers, Gould has been providing custom, semicustom and standard product solutions for over 20 years, longer than any other ASIC vendor.

While extensive quality assurance programs are utilized, the Gould belief is that quality must be "built-in" to a product, not "inspected-in." This is a critical element in the philosophy of Gould AMI. Statistical Process Control (SPC) is the tool which has been implemented throughout the company to assure that quality products are produced and the improvement process is on-going. The company leads all other U.S. semiconductor manufacturers in the implementation of SPC.

Gould brings to its customers what is known as the ASIC continuum. This is a complete range of ASIC design styles which will allow each of its customers to have the optimum solution suited to his unique application. The ASIC continuum includes: programmable logic in the form of Electrically Erasable Programmable Logic devices (EEPLDs), gate arrays, standard cells and cell-based custom designs supported by industry-leading cell compilers, and silicon foundry services. Gould engineers and marketers work with each customer to select the type of ASIC that best meets the requirements of his system.

Our E^2PLDs are desirable for lower volume production or low gate-density requirements. Gould's HCMOS gate arrays provide solutions for a variety of high-performance applications with gate-counts up to 40K. For higher production volume requirements or mega cell implementation, Gould's standard cell and cell-based circuits are especially cost effective.

Along with being the leading designer of custom VLSI, Gould is a leading innovator in combining digital and analog circuitry on a single silicon chip, and is a recognized leader of standard products based on switched capacitor filter technology.

Gould provides components for station equipment, PABX and Central Office Switching systems, data communications, and advanced digital signal processing (DSP) applications.

The company also provides ROMs, ranging from 16K to 1 Meg.

Gould offers silicon foundry services including water fabrication, assembly and final test. Originally founded as an MOS company, Gould currently offers process flexibility with more than 30 high-speed, low-power CMOS processes which span 1.25-micron to the mature 5-micron processes.

Gould offers one of the broadest package selections available in the industry. Over 250 standard packaging alternatives, all meeting JEDEC standards, are available to meet your individual circuit requirements.

Gould operates an assembly and test operation in Manila, Philippines. Regional sales offices and representatives are extensive; please see listing in the last section.

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AMI Semiconductors

Table of Contents

GOULD

AMI Semiconductors

Information furnished by Gould AMI in this publication is believed to be accurate. Devices sold by Gould are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale only. Gould makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Gould makes no warranty of merchantability or fitness for any purposes. Gould reserves the right to discontinue production and change specifications and prices at any time and without notice.

Advanced Product Description means that this product has not been produced in volume, the specifications are preliminary and subject to change, and device characterization has not been done. Therefore, prior to programming or designing this product into a system, it is necessary to check with Gould for current information.

Preliminary means that this product is in limited production, the specifications are preliminary and subject to change. Therefore, prior to programming or designing this product into a system, it is necessary to check with Gould for current information.

These products are intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability application, such as military, medical life-support or life-sustaining equipment are specifically **not** recommended without additional processing by Gould for such application.

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Indices

GOULD

AMI Semiconductors

Indices

Alpha/Numerical Index

Indices

Functional Index

GOULD

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ASIC Products

ASIC Products

Gould AMI was the first company to recognize the need for custom integrated circuits in the mid-1960's, and to pioneer the development of application-specific integrated circuits (ASICs). With more than twenty years' dedication to providing ASIC system solutions, Gould AMI has more experience than any other vendor of ASICs.

The company now offers a continuum of ASIC products, ranging from CMOS programmable logic devices to complex cell-based custom ICs. This spectrum of offerings provides customers with a full range of ASIC choices, so that the optimum solution for an application can be selected.

Gould AMI's ASIC technology allows system designers to tailor their systems and reduce the number of parts in their products by combining multiple memory and processing functions on a single device, instead of mixing and matching several standard parts. The result: smaller board sizes, lower final product cost and higher reliability. ASIC users also benefit by greater product differentiation due to custom tailoring and higher security ensured by an ASIC's resistance to duplication.

CMOS EEPLDs

User-programmable digital devices ideal for small and medium-scale integration

Electrically erasable programmable logic devices are ideal for small and medium-scale integration system design in low-volume production. Our lowest development cost ASICs, these devices deliver plenty of performance and offer a surprising measure of versatility and customer-control.

Built using our unique PEEL™ (Programmable Electrically Erasable Logic) technology, these PLDs are user-programmable, so there's no pre-production customer design and development risk. You may use PC-based or industry-standard PLD programmers to configure the macrocells and, if necessary, to repeatedly erase and reconfigure them.

The table below can help you select the right PLD for you. See the PLD section later in this catalog for detailed data sheets.

Gould AMI's CMOS PLD Family

Part No.	Architecture	Complexity	Speed	Replaces
18CV8	20 pin E2PLD	74 product terms x 36 input array	25ns Tpd	Bipolar PLDs
18CV8-15	20 pin E2PLD	74 product terms x 36 input array	15ns Tpd	Bipolar PLDs
20CG10	24 pin E2PLD	92 product terms x 44 input arrays	25ns Tpd	20V8, 20G10
22CV10Z	24 pin E2PLD	132 product terms x 44 inputs	25ns Tpd	Bipolar PLDs Zero power mode
22CV10	24 pin E2PLD	132 product terms x 44 inputs	25ns Tpd	Bipolar PLDs
PEEL 153	20 pin E2PLD	42 product terms x 36 inputs 10 sum terms x 32 product terms	30ns Tpd	Bipolar PLS153
PEEL 173	24 pin E2PLD	42 product terms x 44 inputs 10 sum terms x 32 product terms	30ns Tpd	Bipolar PLS173
PEEL 253	20 pin E2PLD	42 product terms x 36 inputs 20 sum terms x 42 product terms	30ns Tpd	Bipolar PLS 153 PEEL 153
PEEL 273	24 pin E2PLD	42 product terms x 44 inputs 20 sum terms x 42 product terms	30ns Tpd	Bipolar PLS 173 PEEL 173

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Gate Arrays

Semi-finished digital chips provide high performance for medium volume production with quick development

- 1.25-micron and 2.0-micron Double Metal CMOS Processes
- Basic Logic, Interface, MSI and 7400 Functions
- Custom RAMs and ROMs available in 1.25-micron gate arrays
- Artificial Intelligence Software Services Available for Netlist Translation and Gate Reduction

Gate arrays provide solutions for a variety of high performance digital applications--at a low development cost and quick design time. If you need fast turn production runs, gate arrays may be the right ASIC for you.

Gate arrays are semi-finished digital circuits that contain patterns of uncommitted transistors pre-fabricated on silicon base wafers. Using any major CAE workstation at your own facility, you can use Gould AMI libraries to customize your design as a network of logic functions. With only the metal layers to fabricate, gate array development time is fast--typically four weeks.

Gould AMI's gate arrays are fabricated in a double metal, single poly, twin tub CMOS process. They offer the CMOS advantages of low power dissipation, broad power supply voltage range (2.5 to 5.5 Volts), and high noise immunity.

Over 600 macros in the process families include:

Basic functions:	Simple gates, clock drivers, flip/flops, latches
Interface functions:	TTL, CMOS Schmitt trigger, slew rate buffers, TTL with hysteresis
MSI functions:	Counters, multiplexers, decoders, adders
7400 functions:	Over 160 TTL compatible functions
Digital megacells:	RAMs

1.25-micron Gate Arrays

Array	Total Gates	Usable Gates	Programmable			Power Pins
			TAB	Fine Pitch	Standard Pitch	
GC 100K	100000	54000	438	324	250	12
GC 50K	51456	28300	312	236	184	12
GC 40K	35640	19602	260	194	154	12
GC 30K	31920	17556	246	184	142	12
GC 25K	25728	14150	220	166	132	12
GC 20K	19840	10912	196	146	116	12
GC 15K	15000	8250	168	128	100	12
GC 10K	10320	5676	136	100	84	12
GC 7K	6912	3801	116	84	68	12
GC 5K	5280	2904	98	72	56	12
GC 3K	2520	1386	72	52	40	12

2.0-micron Gate Arrays

Array Name	Equivalent Gates	Max. Usable Gates	Prog. Pins	Total Pins
GB1000D	1120	1008	60	68
GB2000D	2128	1978	76	84
GB3000D	3264	3099	100	108
GB4000D	4256	4086	112	120
GB6000D	5880	5680	132	144
GB8000D	7872	7637	168	184
GB10000D	9776	9483	192	208

Standard Cell Circuits

Analog and digital building blocks offer higher density and smaller size for medium to high volume needs

- 1.25 and 2-micron Double Metal CMOS Families
- 3-micron and 2-micron Double Poly, Double Metal CMOS Families
- Cells Created by Expert-based Cell Generator
- Basic Logic, Interface, MSI, 7400 and Megacell Functions
- 2-micron Process includes Analog Functions
- Tailor-made RAMs, ROMs and PLAs Available
- Artificial Intelligence Software Services Available for Digital Netlist Translation and Gate Reduction

Chips designed with these cells, offered in analog and digital formats, surpass gate array density and approach that of cell-based custom designs at half the development cost and development time. They're cost effective for medium to high-volume production.

Standard cells are pre-designed circuit building blocks whose functional, timing and performance parameters exist in Gould AMI's libraries. As with a gate array, you design a standard cell circuit by choosing logic functions from a library installed on a CAE workstation. But while a gate array design specifies only the final metal layers of a pre-fabricated silicon base, all of a standard cell's base and metal layers are custom fabricated from pre-characterized cells. This feature gives standard cells greater design flexibility, but requires an eight week development time.

A standard cell circuit also uses only the number of cells required for a design, whereas gate arrays seldom utilize all of the available cells. This means a smaller die size and lower cost to you for a given circuit function.

Gould AMI offers over 850 cells in its four standard cell families:

- 1.25-micron digital CMOS (CAB family)
- 2-micron digital CMOS (CBB family)
- 3-micron analog and digital CMOS (CCI family)
- 2-micron analog and digital CMOS (ABX family)

Digital Standard Cells

Both the CAB and CBB families use a double metal, single poly, twin tub CMOS process. They are intended primarily for 5 Volt operation but will operate down to 2.5 Volts.

Cells in these libraries include:

Basic functions:	simple gates, clock drivers, flip/flops. latches
Interface functions:	TTL, CMOS, Schmitt trigger, slew rate buffers, TTL with hysteresis
MSI functions:	counters, multiplexers, decoders, adders
7400 functions:	over 160 TTL compatible functions
Digital megacells:	barrel shifter, funnel shifter, RAM, ROM and PLA

Analog/Digital Standard Cells

The CCI family uses a 3-micron double metal, double poly, p-well CMOS process. It is intended primarily for analog and/or digital applications running at 10 Volts analog with 5 Volts digital operation.

Gould AMI's new ABX process is a 2-micron double poly, double metal process. This is Gould AMI's most flexible process, built on N or P-type starting material, with a range of 13 to 17 process layers. Ideal for mixed signal analog and digital applications, it can operate from 5 to 12 volts. Functions include electrically erasable ROMs, implant programmable ROMs and NPN and PNP bipolar transistors on board.

Cells in the CCI and ABX libraries include:

Basic functions:	simple gates, clock drivers, flip/flops, latches
Interface functions:	TTL, CMOS, Schmitt trigger
MSI functions:	counters, multiplexers, decoders, adders
7400 functions:	over 160 TTL compatible functions
Analog functions:	Op amps, A/D, D/A, comparators, switches, voltage references, input buffer and output buffer

Cell-based Custom

Most tailored ASIC solution--best for high performance, mixed signal or high volume needs

Cell-based custom chips use a combination of Gould's megacells, custom cells and standard cells to provide you with the ultimate in design tailoring and performance. This approach is ideal when you have a requirement for high speed, special interfaces, mixed analog/digital, or very high volume production runs.

Though their development costs and time are longer than with standard cells, cell-based custom circuits pack the most functions into the smallest area. Fewer custom chips need be used in a given design, thus saving board space. Custom devices also provide greater security because they are nearly impossible to copy.

Over twenty years' experience in custom design have given Gould AMI's design team the kind of engineering expertise that complex solutions demand. Particular areas of expertise are analog, mixed signal, high voltage and E2 applications. The following illustrate some examples of Gould AMI's answers to our customers' technical challenges.

Case History #1

A consumer products manufacturer is developing an instrumentation device that measures pressure, room dimensions and weight. The technical challenge? To reduce the number of discrete logic parts and consolidate into one device, which requires analog and digital functions on a single ASIC.

Gould AMI's Solution: A cell-based custom chip which incorporates LCD drivers, a comparator, a/d converters, gain stages and voltage references on a single chip, thus making the measuring device perform more reliably and reducing the number of components required. This saves the customer money in component costs, as well as assembly and inventory costs.

Case History #2

Problem: An automotive company needs a drop-in replacement for a device that nearest fuel, oil and temperature and displays the results on a car dashboard. The technical challenge? This smart device needs to be fast and super-accurate, with numerous features on a single densely packed chip. The customer also requires fault coverage to be 99%.

Gould AMI's solution: To integrate analog and digital blocks on a single custom chip. The analog portion of the circuit allows sampling of a greater number of bits, thus resulting in a faster, more accurate display. The integrated solution enables Gould AMI to meet the size, power, speed and accuracy requirements so that the device will drop right in to the customer's board.

Silicon Foundry Capabilities

Flexible and experienced foundry services for existing customer designs

Gould AMI 's foundry service is the solution for customers who have circuits ready for fabrication and need a primary or secondary manufacturing source. Fifteen years' experience in providing foundry services means well-documented process specifications and a flexible factory, with the ability to accomodate process variations for an existing customer design.

Foundry Steps

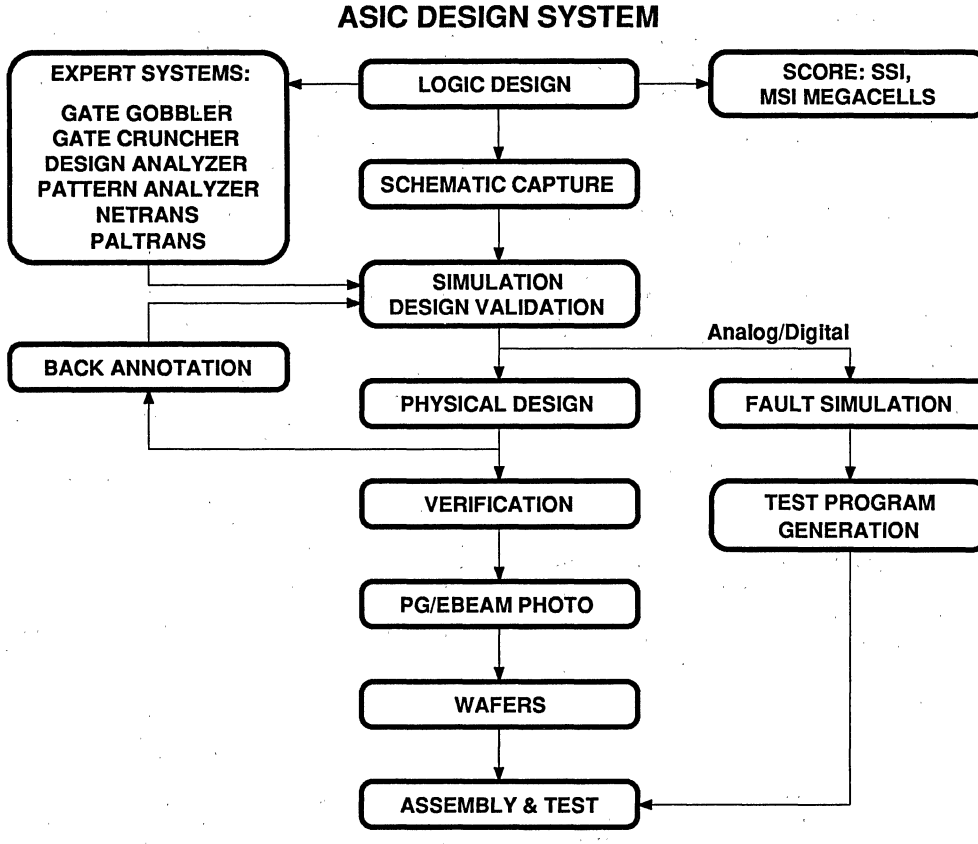
Gould AMI performs a thorough engineering review of your database tape to assure accurate input. After receiving your Calma II database tape, we generate both single level plots and a final layout tape and submit them for your approval. This verifies the design data transfer to the tooling tape--before you commit the design to silicon.

You'll then receive either untested protoypes or mapped wafers that met our visual and parametric process specifications. You'll inspect the sample to verify circuit functionality and performance. With your approval, we produce and assemble additional units that are tested rigorously with your test program (or one we generate from your specs). Gould AMI uses a variety of industry-standard and specialty testers, including Sentry, Gen-Rad, Teradyne, and LTX.

Gould AMI Process Technology Comparison

Process Family	Geometry	Maximum Voltage	Characteristics
CMOS	1.25 µ	5.5 Volts	Digital
CMOS	2.0 µ	5.0 to 12.0 Volts	Mixed Signal
CMOS	2.0 µ	5.5 Volts	Digital
CMOS	3.0 µ	5.0 to 10.0 Volts	Analog
CMOS	3.0 µ	5.5 Volts	Digital
CMOS	2.0 µ	5.5 Volts	EE Digital
CMOS	5.0 µ	5.5 Volts	Digital
CMOS	5.0 µ	5.5 Volts	Analog
CMOS	7.0 µ	5.5 Volts	Digital
CMOS	7.0 µ	5.5 Volts	Analog
NMOS	3.0 µ	5.5 Volts	Digital
NMOS	4.0 µ	5.5 Volts	Digital
NMOS	5.0 µ	5.5 Volts	Digital

Typical ASIC Development Flow



ASIC Software Services

Optional design services give you the power of choice and ease your designs

Unlike many ASIC vendors that accept only completed designs or finished netlists, Gould AMI is able to pick up an ASIC design at any stage, whether customers submit a partially finished design, a foundry-ready database tape, or a simple set of specifications. In order to ease logic design for its customers, Gould AMI has installed its analog and digital cell libraries on popular engineering workstations including Mentor Graphics, Daisy Systems, Intergraph, VALID Logic Systems, FutureNet and Viewlogic.

Gould AMI uses several advanced expert systems in-house, each of which taps the combined experience of Gould AMI's engineers to accelerate device layout and design optimization.

ASIC Products

ASIC Netlist Translation Services:

If a client has already designed a digital chip using another vendor's or their own proprietary tools, Gould AMI's NETRANS™ expert system will "translate" the netlist into Gould AMI-compatible form in just a few hours. This automated design transfer works independently of workstation libraries or processes, and can save customers thousands of dollars and weeks of precious time. For turning programmable logic device into gate arrays or standard cells, PALTRANS™ is the answer. PALTRANS converts standard programmable array logic (PAL), programmable electrically erasable logic (PEEL) and field programmable gate arrays (FPGAs) into netlists used to design gate array or standard cell ASICs. You can use an off-the-shelf PLD as a prototype for programming, debugging, and beta-testing logic designs, instead of first requiring the production of an ASIC. Engineers then use PALTRANS to convert the data into a netlist. In about eight hours, mask production can begin and an ASIC design is produced in two to three weeks.

Tools Speed Layout and Optimization

The SCORE™ cell compiler generates and tailors cells to a client's specific requirements in one-tenth the time required for hand-built cells.

Gate Gobbler, Gate Cruncher, Design Analyzer and Pattern Analyzer are artificial intelligence (AI) tools that assist with the conversion of conventional standard devices to CMOS ASICs.

By the end of 1989, Gould AMI will offer an Automatic Test Generation tool that will generate test vectors in a matter of hours, relieving designers of the task and saving at least six weeks for manual test generation This tool will automatically partition a circuit into a set of combinatorial functions and insert a scan path. Each function, seen as a distinct circuit, can be quickly and easily tested with an automatic test program generator employing the D-Algorithm.

Transitioning from standard TTL parts to ASICs can be fraught with difficulty, and when ASIC prototypes don't work, design re-work through traditional analysis and optimization techniques can take weeks or months. Gould AMI's AI tools minimize the delays caused by having to re-work a design through traditional analysis and optimization techniques. The tools incorporate a continually expanding knowledge base, applying Gould AMI's hundreds of engineering man-years to every job.

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Communication Products

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DTMF Tone Generator

S2559E/F

COMMUNI-CATION PRODUCTS

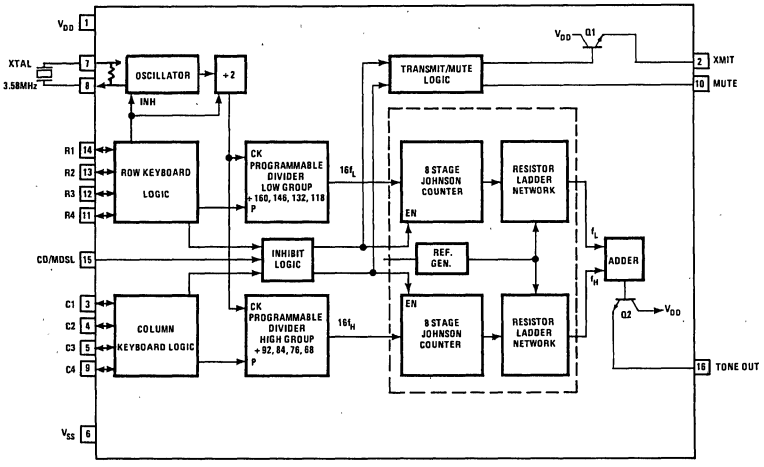
Features

- ☐ Wide Operating Supply Voltage Range: 2.5 to 10 Volts
- ☐ Low Power CMOS Circuitry Allows Device Power to be Derived Directly from the Telephone Lines or from Small Batteries, e.g., 9V
- ☐ Uses TV Crystal Standard (3.58MHz) to Derive all Frequencies thus Providing Very High Accuracy and Stability
- ☐ Mute Drivers On-Chip
- ☐ Interfaces Directly to a Standard Telephone Push-Button or Calculator Type X-Y Keyboard
- ☐ The Total Harmonic Distortion is Below Industry Specification
- ☐ Oscillator Resistor On Chip
- ☐ On-Chip Generation of a Reference Voltage to Assure Amplitude Stability of the Dual Tones Over the Operating Voltage and Temperature Range
- ☐ Single Tone as Well as Dual Tone Capability
- ☐ Two Options Available:
  - E: Mode Select
  - F: Chip Disable

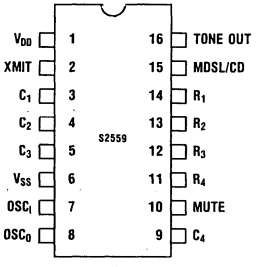
General Description

The S2559 DTMF Generator is specifically designed to implement a dual tone telephone dialing system. The device can interface directly to a standard pushbutton

Block Diagram



Pin Configuration



General Description (Continued)

telephone keyboard or calculator type X-Y keyboard and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinudsoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. A voltage reference is generated on the chip which is stable over the operating voltage and temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications. These features permit the S2559 to be incorporated with a slight modification of the standard 500 type telephone basic circuitry to form a pushbutton dual-tone telephone. Other applications of the device include radio and mobile telephones, remote control, Point-of-Sale, and Credit Card Verification Terminals and process control.

Absolute Maximum Ratings

DC Supply Voltage ($V_{DD} - V_{SS}$)	+10.5V
Operating Temperature	−0°C to +70°C
Storage Temperature	−30°C to +125°C
Power Dissipation at 25°C	1000mW
Input	$V_{SS} - 0.3 \leq V_{IN} \leq V_{DD} + 0.3$

S2559E/F Electrical Characteristics:

(Specifications apply over the operating temperature range of 0°C to +70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions			(V_{DD}-V_{SS}) Volts	Min.	Typ.	Max.	Units
	Supply Voltage							
V_{DD}	Tone Out Mode (Valid Key Depressed)				2.5		10.0	V
	Non Tone Out Mode (No Key Depressed)				1.6		10.0	V
	Supply Current							
I_{DD}	Standby (No Key Selected, Tone, XMIT and MUTE Outputs Unloaded)			3.0		0.3	30	μA
				10.0		1.0	100	μA
	Operating (One Key Selected, Tone, XMIT and MUTE Outputs Unloaded)			3.0		1.0	2.0	mA
				10.0		8	16.0	mA
	Tone Output							
S2559E/F V_{OR}	Single Tone Mode Output Voltage	Row Tone,	$R_L = 390\Omega$	3.5	335	465	565	mVrms
				5.0	380	540	710	mVrms
		Row Tone,	$R_L = 240\Omega$	10.0	380	550	735	mVrms
dB_{CR}	Ratio of Column to Row Tone (Dual Tone Mode) 2559E/F			3.5 – 10.0	1.0	2.0	3.0	dB
%DIS	Distortion* 2559E/F			3.5 – 10.0			7	%

S2559E/F Electrical Characteristics: (continued)

Symbol	Parameter/Conditions		(V_{DD}-V_{SS}) Volts	Min.	Typ.	Max.	Units
	XMIT, MUTE Outputs						
V_{OH}	XMIT, Output Voltage, High	(I_{OH}=15mA)	3.0	1.5	1.8		V
	(No Key Depressed)(Pin 2)	(I_{OH}=50mA)	10.0	8.5	8.8		V
I_{OF}	XMIT, Output Source Leakage Current, V_{OF}=0V		10.0			100	μA
V_{OL}	MUTE (Pin 10) Output Voltage, Low,		2.75		0	0.5	V
	(No Key Depressed), No Load		10.0		0	0.5	V
V_{OH}	MUTE, Output Voltage, High,		2.75	2.5	2.75		V
	(One Key Depressed) No Load		10.0	9.5	10.0		V
I_{OL}	MUTE, Output Sink	V_{OL}=0.5V	3.0	0.53	1.3		mA
	Current		10.0	2.0	5.3		mA
I_{OH}	MUTE, Output Source	V_{OH}=2.5V	3.0	0.17	0.41		mA
	Current	V_{OH}=9.5V	10.0	0.57	1.5		mA

*Distortion is defined as "the ratio of the total power of all extraneous frequencies, in the VOICE band above 500Hz, to the total power of the DTMF frequency pair".

Table 1. Comparisons of Specified vs Actual Tone Frequencies Generated by S2559

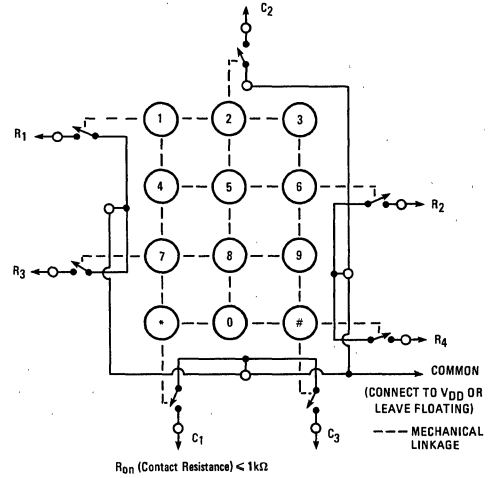
ACTIVE INPUT	OUTPUT FREQUENCY Hz		% ERROR SEE NOTE
	SPECIFIED	ACTUAL	
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1,209	1,215.9	+0.57
C2	1,336	1,331.7	−0.32
C3	1,477	1,417.9	−0.35
C4	1,633	1,645.0	+0.73

NOTE: % Error does not include oscillator drift.

Table 2. XMIT and MUTE Output Functional Relationship

OUTPUT RELEASED	'DIGIT' KEY DEPRESSED	'DIGIT' KEY	COMMENT
XMIT	V_{DD}	High Impedance	Can source at least 50mA at 10V with 1.5V max. drop
MUTE	V_{SS}	V_{DD}	Can source or sink current

Figure 1. Standard Telephone Push Button Keyboard



Circuit Description

The S2559 is designed so that it can be interfaced easily to the dual tone signaling telephone system and that it will more than adequately meet the recommended telephone industry specifications regarding the dual tone signaling scheme.

Design Objectives

The specifications that are important to the design of the DTMF Generator are summarized below: the dual tone signal consists of linear addition of two voice frequency signals. One of the two signals is selected from a group of frequencies called the "Low Group" and the other is selected from a group of frequencies called the "High Group". The low group consists of four frequencies 697, 770, 852 and 941 Hz. The high group consists of four frequencies 1209, 1336, 1477 and 1633 Hz. A keyboard arranged in a row, column format (4 rows x 3 or 4 columns) is used for number entry. When a push button corresponding to a digit (0 thru 9) is pushed, one appropriate row (R1 thru R4) and one appropriate column (C1 thru C4) is selected. The active row input selects one of the low group frequencies and the active column input selects one of the high group frequencies. In standard dual tone telephone systems, the highest high group frequency of 1633Hz (Col. 4) is not used. The frequency tolerance must be ± 1.0%. However, the S2559 provides a better than .75% accuracy. The total harmonic and intermodulation distortion of the dual tone must be less than 10% as seen at the telephone terminals. (Ref. 1.) The high group to low group signal amplitude ratio should be 2.0 ± 2dB and the absolute amplitude of the low group and high group tones must be within the allowed range. (Ref. 1.) These requirements apply when the telephone is used over a short loop or long loop and over the operating temperature range. The design of the S2559 takes into account these considerations.

Oscillator

The device contains an oscillator circuit with the necessary parasitic capacitances and feedback resistor on chip so that it is only necessary to connect a standard 3.58MHz TV crystal across the OSC_I and OSC_O terminals to implement the oscillator function. The oscillator functions whenever a row input is activated. The reference frequency is divided by 2 and then drives two sets of programmable dividers, the high group and the low group.

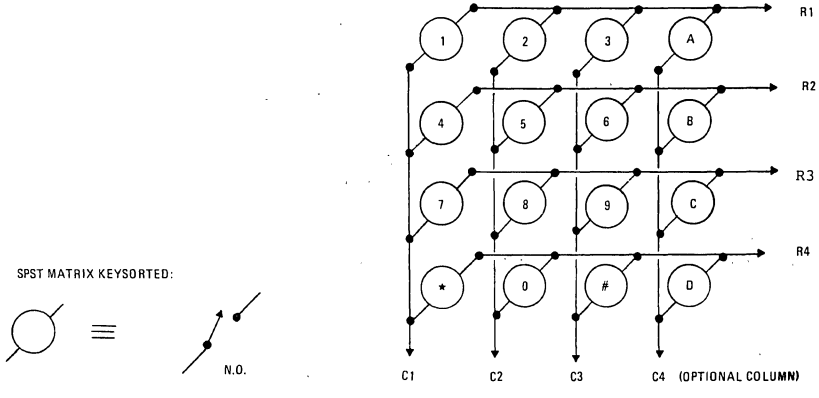
Keyboard Interface

The S2559 employs a calculator type scanning circuitry to determine key closures. When no key is depressed, active pull-down resistors are "on" on the row inputs and active pull-up resistors are "on" on the column inputs. When a key is pushed a high level is seen on one of the row inputs, the oscillator starts and the keyboard scan logic turns on. The active pull-up or pull-down resistors are selectively switched on and off as the keyboard scan logic determines the row and the column inputs that are selected. The advantage of the scanning technique is that a keyboard arrangement of SPST switches are shown in Figure 2 without the need for a common line, can be used. Conventional telephone push button keyboards as shown in Figure 1 or X-Y keyboards with common can also be used. The common line of these keyboards can be left unconnected or wired "high".

Logic Interface

The S2559 can also interface with CMOS logic outputs directly. The S2559 requires active "High" logic levels. Since the active pull-up resistors present in the S2559 are fairly low value (500Ω typ), diodes can be used as shown in Figure 3 to eliminate excessive sink current flowing into the logic outputs in their "Low" state.

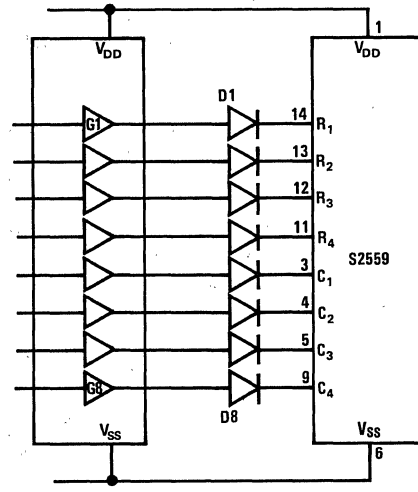
Figure 2. SPST Matrix Keyboard Arranged in the 2 of 8 Row, Column Format



Tone Generation

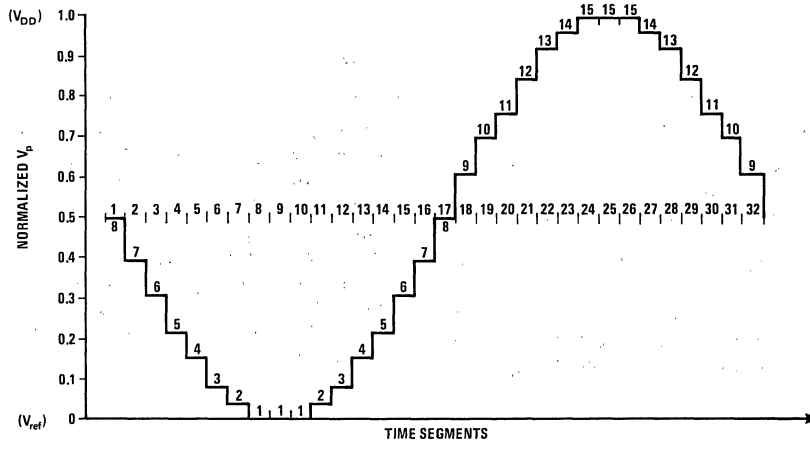
When a valid key closure is detected, the keyboard logic programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divide by 16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function (see Figure 3). This is done by connecting a weighted resistor ladder network between the outputs of the Johnson counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude V_P ($V_{DD} - V_{REF}$) of the stairstep function is fairly constant. V_{REF} is so chosen that V_P falls within the allowed range of the high group and low group tones.

Figure 3. Logic Interface for Keyboard Inputs of the S2559



G1 THRU G8 ANY TYPE CMOS GATE
D1 THRU D8 DIODES TYPE IN914

Figure 4. Stairstep Waveform of the Digitally Synthesized Sinewave



The individual tones generated by the sinewave synthesizer are then linearly added and drive a bipolar NPN transistor connected as emitter follower to allow proper impedance transformation, at the same time preserving signal level.

Dual Tone Mode

When one row and one column is selected dual tone output consisting of an appropriate low group and high group tone is generated. If two digit keys, that are not either in the same row or in the same column, are depressed, the dual tone mode is disabled and no output is provided.

Single Tone Mode

Single tones either in the low group or the high group can be generated as follows. A low group tone can be generated by activating the appropriate row input or by depressing two digit keys in the appropriate row. A high group tone can be generated by depressing two digit keys in the appropriate column, i.e., selecting the appropriate column input and two row inputs in that column.

Mode Select

The S2559E has a Mode Select (MDSL) input (Pin 15). When MDSL is left floating (unconnected) or connected to V_{DD}, both the dual tone and single tone modes are available. If MDSL is connected to V_{SS}, the single tone mode is disabled and no output tone is produced if an attempt for single tone is made. The S2559F does not have the Mode Select option.

Chip Disable

The S2559F has a Chip Disable input at Pin 15 instead of the Mode Select input. The chip disable for the S2559F is active "high." When the chip disable is active, the tone output goes to V_{SS}, the row, column inputs go into a high impedance state, the oscillator is inhibited and the MUTE and XMIT outputs go into active states. The effect is the device essentially disconnects from the keyboard. This allows one keyboard to be shared among several devices. The CD pin has an internal pull-down.

Quartz Crystal Specification (25° C ± 2°C)	
Operating Temperature Range: 0°C to +70°C	
Frequency	3.579545MHz
Frequency Calibration Tolerance	02 ± %
Load Capacitance	18pF
Effective Series Resistance	180 Ohms, max.
Drive Level-Correlation/Operating	2mW
Shunt Capacitance	7pF, max.
Oscillation Mode	Fundamental

MUTE, XMIT Outputs

The S2559E, F have a CMOS buffer for the MUTE output and a bipolar NPN transistor for the XMIT output. With no keys depressed, the MUTE output is "low" and the XMIT output is in the active state so that substantial current can be sourced to a load. When a key is depressed, the MUTE output goes high, while the XMIT output goes into a high impedance state. When Chip Disable is "high" the MUTE output is forced "low" and the XMIT output is in active state regardless of the state of the keyboard inputs.

Amplitude/Distortion Measurements

Amplitude and distortion are two important parameters in all applications of the Digital Tone Generator. Amplitude depends upon the operating supply voltage as well as the load resistance connected on the Tone Output pin. The on-chip reference circuit is fully operational when the supply voltage equals or exceeds 5 volts and as a consequence the tone amplitude is regulated in the supply voltage range above 5 volts. The load resistor value also controls the amplitude. If R_L is low the reflected impedance into the base of the output transistor is low and the tone output amplitude is lower. For R_L greater than 5kΩ the reflected impedance is sufficiently large and highest amplitude is produced. Individual tone amplitudes can be measured by applying the dual tone signal to a wave analyzer (H-P type 3581A) and amplitudes at the selected frequencies can be noted. This measurement also permits verification of the preemphasis between the individual frequency tones.

Distortion is defined as "the ratio of the **total** power of all extraneous frequencies in the **voiceband** above 500Hz accompanying the signal to the power of the frequency **pair.**" This ratio must be less than 10% or when expressed in dB must be lower than – 20dB.

(Ref. 1.) Voiceband is conventionally the frequency band of 300Hz to 3400Hz. Mathematically distortion can be expressed as:

$$\text{Dist.} = \frac{\sqrt{(V_1)^2 + (V_2)^2 + \ldots + (V_N)^2}}{\sqrt{(V_L)^2 + (V_H)^2}}$$

where $(V_1) \ldots (V_N)$ are extraneous frequency (i.e., intermodulation and harmonic) components in the 500Hz to

3400Hz band and V_L and V_H are the individual frequency components of the DTMF signal. The expression can be expressed in dB as:

$$DIST_{dB} = 20 \log \frac{\sqrt{(V_1)^2 + (V_2)^2 + \ldots (V_N)^2}}{\sqrt{(V_L)^2 + (V_H)^2}}$$

$$= 10\{\log[(V_1)^2 + \ldots (V_N)^2] - \log[(V_L)^2 + (V_L)^2 + (V_H)^2]\} \ldots (1)$$

An accurate way of measuring distortion is to plot a spectrum of the signal by using a spectrum analyzer (H-P type 3580A) and an X-Y plotter (H-P type 7046A). Individual extraneous and signal frequency components are then noted and distortion is calculated by using the expression (1) above. Figure 6 shows a spectrum plot of a typical signal obtained from a S2559 device operating from a fixed supply of 4Vdc and R_L = 10kΩ in the test circuit of Figure 5. Mathematical analysis of the spectrum shows distortion to be – 30dB (3.2%). For quick estimate of distortion, a rule of thumb as outlined below can be used.

"As a first approximation distortion in dB equals the difference between the amplitude (dB) of the extraneous component that has the highest amplitude and the amplitude (dB) of the low frequency signal." This rule of thumb would give an estimate of – 28dB as distortion for the spectrum plot of Figure 6 which is close to the computed result of – 30dB.

In a telephone application amplitude and distortion are affected by several factors that are interdependent. For detailed discussion of the telephone application and other applications of the 2559 Tone Generator, refer to the applications note "Applications of Digital Tone Generator."

Ref. 1: Bell System Communications Technical Reference, PUB 47001, "Electrical Characteristics of Bell System Network Facilities at the Interface with Voiceband Ancillary and Data Equipment," August 1976.

Figure 5. Test Circuit for Distortion Measurement

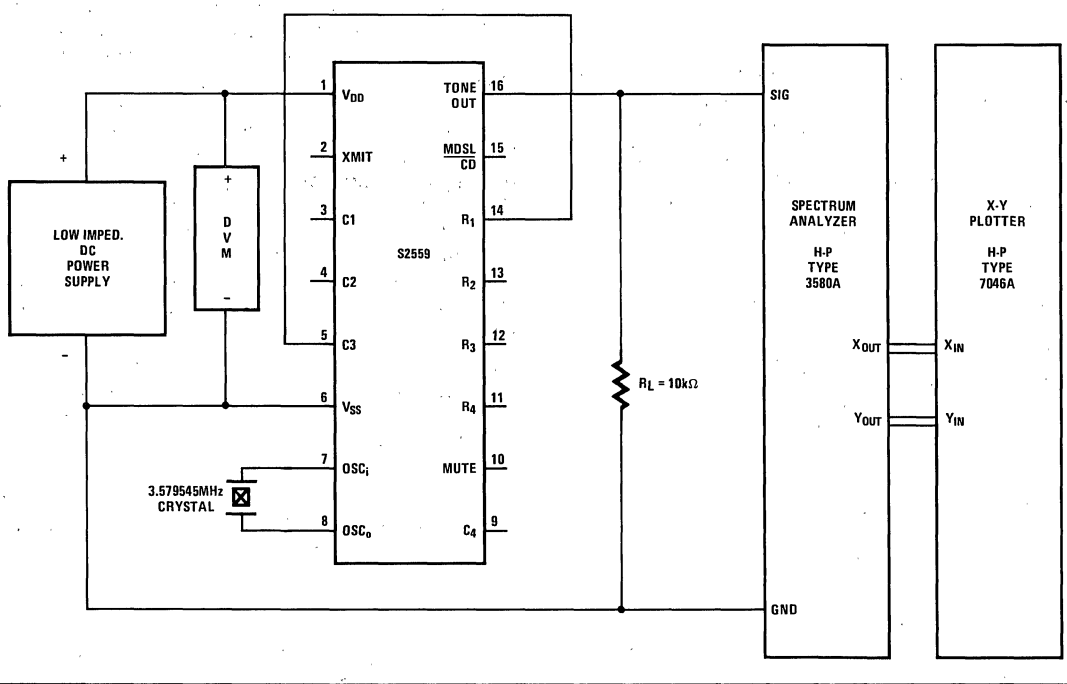
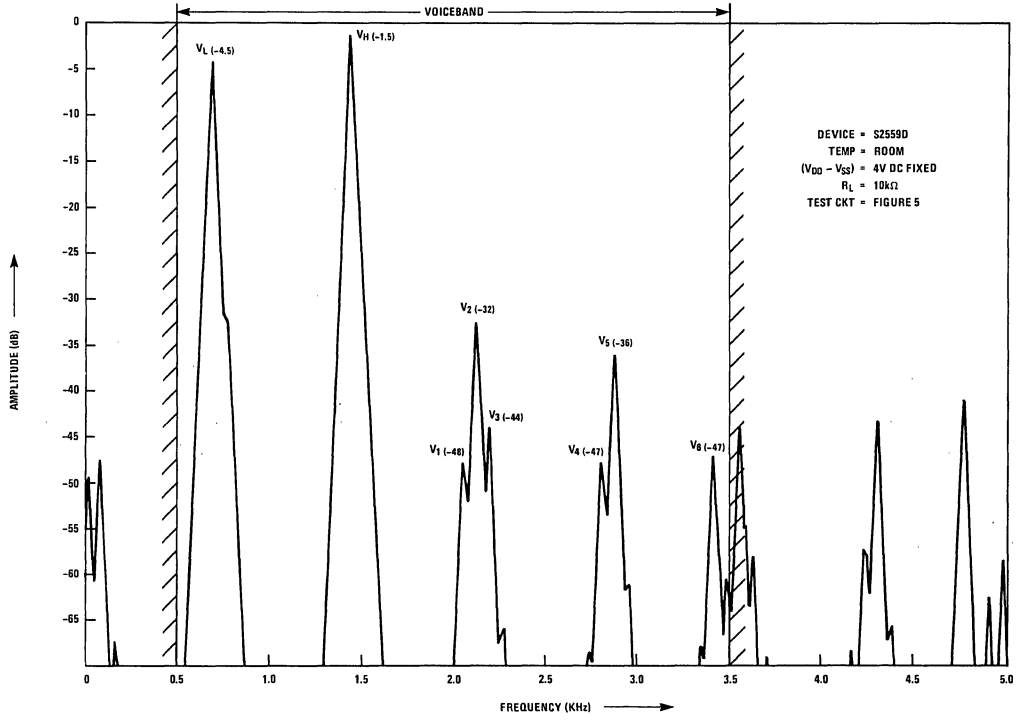


Figure 6. A Typical Spectrum Plot



An application note is also available describing the design considerations, test methods, and results obtained using the S2559 Tone Generator family in DTMF pushbutton telephones. Interface with type 500 and 2500 networks are discussed. Use in ancillary equipment is also covered. Please contact factory.

GOULD

AMI Semiconductors

Pulse Dialer

S2560A

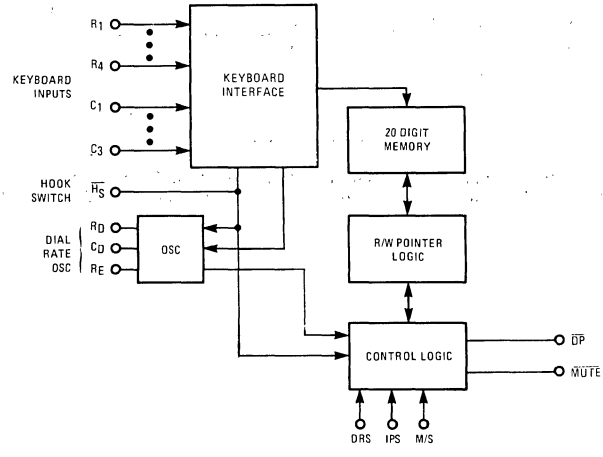
Features

- ☐ Low Voltage CMOS Process for Direct Operation from Telephone Lines
- ☐ Inexpensive R-C Oscillator Design Provides Better than ± 5% Accuracy Over Temperature and Unit to Unit Variations
- ☐ Dialing Rate Can be Varied by Changing the Dial Rate Oscillator Frequency
- ☐ Dial Rate Select Input Allows Changing of the Dialing Rate by a 2:1 Factor Without Changing Oscillator Components
- ☐ Two Selections of Mark/Space Ratios (33⅓/66⅔ or 40/60)
- ☐ Twenty Digit Memory for Input Buffering and for Redial with Access Pause Capability
- ☐ Mute and Dial Pulse Drivers on Chip
- ☐ Accepts DPCT Keypad with Common Arranged in a 2 of 7 Format; Also Capable of Interface to SPST Switch Matrix

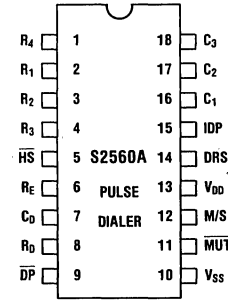
General Description

The S2560A Pulse Dialer is a CMOS integrated circuit that converts pushbutton inputs to a series of pulses suitable for telephone dialing. It is intended as a replacement for the mechanical telephone dial and can operate directly from the telephone lines with minimum interface. Storage is provided for 20 digits, therefore, the last dialed number is available for redial until a new number is entered. IDP is scaled to the dialing rate such as to produce smaller IDP at higher dialing rates. Additionally, the IDP can be changed by a 2:1 factor at a given dialing rate by means of the IDP select input.

Block Diagram



Pin Configuration



S2560A

Absolute Maximum Ratings:

Supply Voltage	+5.5V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Voltage at any Pin	V_{SS} −0.3V to V_{DD} +0.3V
Lead Temperature (Soldering, 10sec)	300°C

Electrical Characteristics:

Specifications apply over the operating temperature and $1.5V \leq V_{DD} - V_{SS} \leq 3.5V$ unless otherwise specified.

Symbol	Parameter	V_{DD}-V_{SS} (Volts)	Min.	Max.	Units	Conditions
	Output Current Levels					
I_{OLDP}	DP Output Low Current (Sink)	3.5	125		µA	V_{OUT} = 0.4V
I_{OHDP}	DP Output High Current (Source)	1.5 3.5	20 125		µA µA	V_{OUT} = 1V V_{OUT} = 2.5V
I_{OLM}	MUTE Output Low Current (Sink)	3.5	125		µA	V_{OUT} = 0.4V
I_{OHM}	MUTE Output High Current (Source)	1.5 3.5	20 125		µA µA	V_{OUT} = 1V V_{OUT} = 2.5V
I_{OLT}	Tone Output Low Current (Sink)	1.5	20		µA	V_{OUT} = 0.4V
I_{OHT}	Tone Output High Current (Source)	1.5	20		µA	V_{OUT} = 1V
V_{DR}	Data Retention Voltage		1.0		V	"On Hook" $\overline{HS}$ = V_{DD}. Keyboard open, all other input pins to V_{DD} or V_{SS}
I_{DD}	Quiescent Current	1.0		750	nA	
I_{DD}	Operating Current	1.5 3.5		100 500	µA µA	$\overline{DP}$, $\overline{MUTE}$ open, $\overline{HS}$ = V_{SS} ("Off Hook") Keyboard processing and dial pulsing at 10 pps at conditions as above
fo	Oscillator Frequency	1.5		10	kHz	
Δfo/fo	Frequency Deviation	1.5 to 2.5 2.5 to 3.5	−3 −3	+3 +3	% %	Fixed R-C oscillator components $50K\Omega \leq R_D \leq 750K\Omega$; $100pF \leq C_D{}^* \leq 1000pF$; $750k\Omega \leq R_E \leq 5M\Omega$ *300pF most desirable value for C_D
	Input Voltage Levels					
V_{IH}	Logical "1"		80% of ($V_{DD}-V_{SS}$)	V_{DD} +0.3	V	
V_{IL}	Logical "0"		V_{SS} −0.3	20% of ($V_{DD}-V_{SS}$)	V	
C_{IN}	Input Capacitance Any Pin			7.5	pF	

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leq V_I \leq V_{DD}$ as a maximum limit). This rule will prevent over-dissipation and possible damage of the input-protection diode when the device power supply is grounded. When power is first applied to the device, the device should be in "On Hook" condition ($\overline{HS}$ = 1). This is necessary because there is no internal power or reset on chip and for proper operation all internal latches must come up in a known state. In applications where the device is hard wired in "Off Hook" ($\overline{HS}$ = 0) condition, a momentary "On Hook" condition can be presented to the device during power up by use of a capacitor resistor network as shown in Figure 6.

Functional Description

The pin function designations are outlined in Table 1.

Oscillator

The device contains an oscillator circuit that requires three external components: two resistors (R_D and R_E) and one capacitor (C_D). All internal timing is derived from this master time base. To eliminate clock interference in the talk state, the oscillator is only enabled during key closures and during the dialing state. It is disabled at all other times including the "on hook" condition. For a dialing rate of 10pps the oscillator should be adjusted to 2400Hz. Typical values of external components for this are R_D and $R_E = 750k\Omega$ and $C_D = 270pF$. It is recommended that the tolerance of resistors to be 5% and capacitor to be 1% to insure a 10% tolerance of the dialing rate in the system.

Keyboard Interface (S2560A)

The S2560A employs a scanning technique to determine a key closure. This permits interface to a DPCT keyboard with common connected to V_{DD} (Figure 1), logic interface (Figure 2) and interface to a SPST switch matrix (Figure 7). A high level on the appropriate row and column inputs constitutes a key closure for logic interface. When using a SPST switch matrix, it is necessary to add small capacitors (30pF) from the column inputs to V_{SS} to insure that the oscillator is shut off after a key is released or after the dialing is complete.

OFF Hook Operation: The device is continuously powered through a 150kΩ resistor during Off hook operation. The DP output is normally high and sources base drive to transistor Q_1 to turn ON transistor Q_2. Transistor Q_2 replaces the mechanical dial contact used in the rotary dial phones. Dial pulsing begins when the user enters a number through the keyboard. The $\overline{DP}$ output goes low shutting the base drive to Q_1 OFF causing Q_2 to open during the pulse break. The $\overline{MUTE}$ output also goes low during dial pulsing allowing muting of the receiver through transistors Q_3 and Q_4. The relationship of dial pulse and mute outputs are shown in Figure 3.

ON Hook Operation: The device is continuously powered through a 10–20MΩ resistor during the ON hook operation. This resistor allows enough current from the tip and ring lines to the device to allow the internal memory to hold and thereby providing storage of the last number dialed.

The dialing rate is derived by dividing down the dial rate oscillator frequency. Table 2 shows the relationship of the dialing rate with the oscillator frequency and the dial rate select input. Different dialing rates can be derived by simply changing the external resistor value. The dial rate select input allows changing of the dialing rate by a factor of 2 without the necessity of changing the external component values. Thus, with the oscillator adjusted to 2400Hz, dialing rates of 10 or 20pps can be achieved. Dialing rates of 7 and 14pps similarly can be achieved by changing the oscillator frequency to 1680Hz.

The Inter-Digit Pause (IDP) time is also derived from the oscillator frequency and can be changed by a factor of 2 by the IDP select input. With IDP select pin wired to V_{SS}, an IDP of 800ms is obtained for dial rates of 10 and 20pps. IDP can be reduced to 400ms by wiring the IDP select pin to V_{DD}. At dialing rates of 7 and 14pps, IDP's of 1143ms and 572ms can be similarly obtained. If the IDP select is connected to the dial rate select pin, the IDP is scaled to the dial rate such that at 10pps an IDP of 800ms is obtained and at 20pps an IDP of 400ms is obtained.

The user can enter a number up to 20 digits long from a standard 3x4 double contact keypad with common (Figure 1). It is also possible to use a logic interface as shown in Figure 2 for number entry. Antibounce protection circuitry is provided on chip (min. 20ms) to prevent false entry.

Any key depressions during the on-hook condition are ignored and the oscillator is inhibited. This insures that the current drain in the on-hook condition is very low and used to retain the memory.

Normal Dialing

The user enters the desired numbers through the keyboard after going off hook. Dial pulsing starts as soon as the first digit is entered. The entered digits are stored sequentially in the internal memory. Since the device is designed in a FIFO arrangement, digits can be entered at a rate considerably faster than the output rate. Digits can be entered approximately once every 50ms while the dialing rate may vary from 7 to 20pps. The number entered is retained in the memory for future redial. Pauses may be entered when required in the dial sequence by pressing the "#" key, which provides access pauses for future redial. Any number of access pauses may be entered as long as the total entries do not exceed twenty.

Auto Dialing

The last number dialed is retained in the memory and therefore can be redialed out by going off hook and pressing the "#" key. Dial pulsing will start when the key is depressed and finish after the entire number is dialed out unless an access pause is detected. In such a case, the dial pulsing will stop and will resume again only after the user pushes the "#" key.

Table 1. S2560A/S2560B Pin/Function Descriptions

Pin	Number	Function
Keyboard (R_1, R_2, R_3, R_4, C_1, C_2, C_3)	2, 3, 4, 1, 16, 17, 18	These are 4 row and 3 column inputs from the keyboard contacts. These inputs are open when the keyboard is inactive. When a key is pushed, an appropriate row and column input must go to V_{DD} or connect with each other. A logic interface is also possible as shown in Figure 2. Active pull up and pull down networks are present on these inputs when the device begins keyboard scan. The keyboard scan begins when a key is pressed and starts the oscillator. Debouncing is provided to avoid false entry (typ. 20ms).
Inter-Digit Pause Select (IDP)	15	One programmable line is available that allows selection of the pause duration that exists between dialed digits. It is programmed according to the truth table shown in Table 3. Note that preceding the first dialed pulse is an inter-digit time equal to the selected IDP. Two pauses either 400ms or 800ms are available for dialing rates of 10 and 20 pps. IDP's corresponding to other dialing rates can be determined from Tables 2 and 3.
Dial Rate Select (DRS)	14	A programmable line allows selection of two different output rates such as 7 or 14 pps, 10 or 20 pps, etc. See Tables 2 and 3.
Mark/Space (M/S)	12	This input allows selection of the mark/space ratio, as per Table 3.
Mute Out ($\overline{MUTE}$)	11	A pulse is available that can provide a drive to turn on an external transistor to mute the receiver during the dial pulsing.
Dial Pulse Out ($\overline{DP}$)	9	Output drive is provided to turn on a transistor at the dial pulse rate. The normal output will be "low" during "space" and "high" otherwise.
Dial Rate Oscillator (R_E, C_D, R_D)	6, 7, 8	These pins are provided to connect external resistors R_D, R_E and capacitor C_D to form an R-C oscillator that generates the time base for the Key Pulser. The output dialing rate and IDP are derived from this time base.
Hook Switch ($\overline{HS}$)	5	This input detects the state of the hook switch contact; "off hook" corresponds to V_{SS} condition.
Power (V_{DD}, V_{SS})	13, 10	These are the power supply inputs. The device is designed to operate from 1.5V–3.5V.

Figure 1. Standard Telephone Pushbutton Keyboard

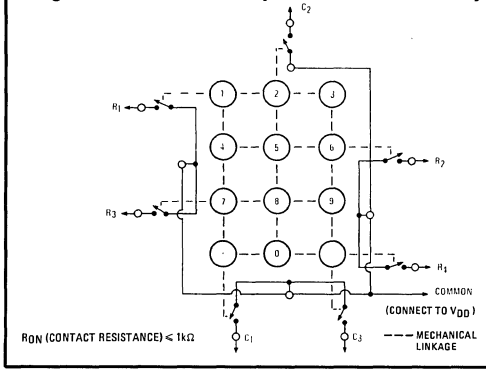


Figure 2. Logic Interface for the S2560

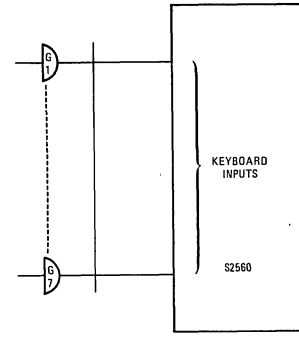


Figure 3. Timing

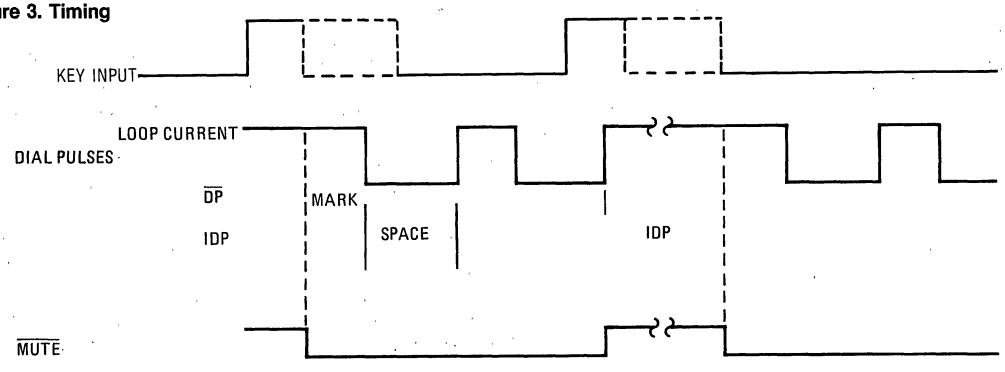


Table 2. Table for Selecting Oscillator Component Values for Desired Dialing Rates and Inter-Digit Pauses

Dial Rate Desired	Osc. Freq. (Hz)	R_D (kΩ)	R_E (kΩ)	C_D (pF)	Dial Rate (pps)		IDP (ms)	
					DRS = V_{SS}	DRS = V_{DD}	IPS = V_{SS}	IPS = V_{DD}
5.5/11	1320				5.5	11	1454	727
6/12	1440				6	12	1334	667
6.5/13	1560				6.5	13	1230	615
7/14	1680	Select components in the ranges indicated in table of electrical specifications			7	14	1142	571
7.5/15	1800				7.5	15	1066	533
8/16	1920				8	16	1000	500
8.5/17	2040				8.5	17	942	471
9/18	2160				9	18	888	444
9.5/19	2280				9.5	19	842	421
10/20	2400	750	750	270	10	20	800	400
$(f_d/240)/(f_d/120)$	f_d				$(f_d/240)$	$(f_d/120)$	$\frac{1920}{f_i} \times 10^3$	$\frac{960}{f_i} \times 10^3$

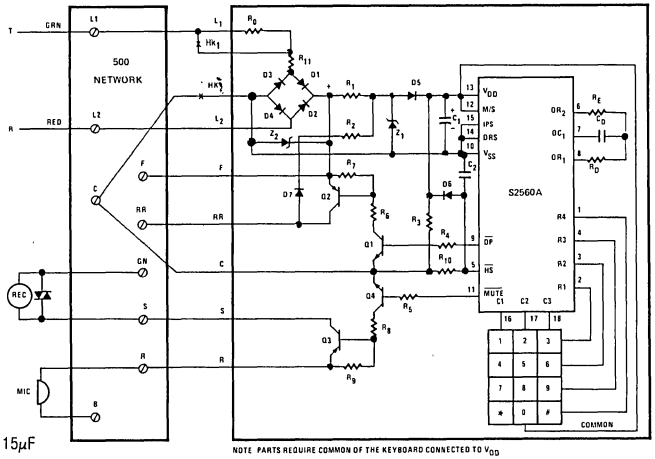
NOTE: IDP is dependent on the dialing rate selected. For example, for a dialing rate of 10pps, an IDP of either 800ms or 400ms can be selected. For a dialing rate of 14pps, and IDP of either 1142ms or 571ms can be selected.

Table 3.

Function	Pin Designation	Input Logic Level	Selection
Dial Pulse Rate Selection	DRS (14)	V_{SS} V_{DD}	(f/240)pps (f/120)pps
Inter-Digit Pause Selection	IDP (15)	V_{DD} V_{SS}	$\frac{960}{f}$ s $\frac{1920}{f}$ s
Mark/Space Ratio	M/S (12)	V_{SS} V_{DD}	33⅓/66⅔ 40/60
On Hook/Off Hook	$\overline{HS}$ (5)	V_{DD} V_{SS}	On Hook Off Hook

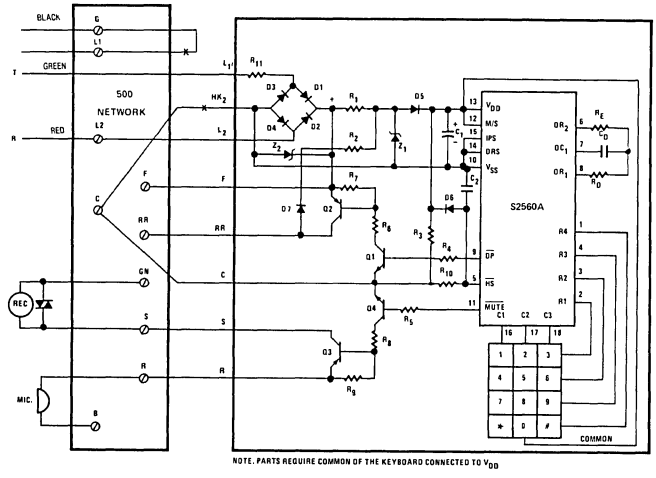
NOTE: f is the oscillator frequency and is detemined as shown in Figure 5.

Figure 4. Pulse Dialer Circuit with Redial



$R_0 = 10\text{-}20M\Omega$, $R_1 = 150k\Omega$, $R_2 = 2k\Omega$
$R_3 = 470k\Omega$, R_4, $R_5 = 10k\Omega$, $R_{10} = 47k\Omega$
R_6, $R_8 = 2k\Omega$, R_7, $R_9 = 30k\Omega$, $R_{11} = 20\Omega$, 2W
$Z_1 = 3.9V$, D_1—D_4 = IN4004, D_5, D_6, D_7 = IN914, $C_1 = 15\mu F$
$R_E = R_D = 750k\Omega$, $C_D = 270pF$, $C_2 = 0.01\mu F$
Q_1, Q_4 = 2N5550 TYPE Q_2, Q_3 = 2N5401 TYPE
Z_2 = IN5379 110V ZENER OR 2XIN4758

Figure 5. Pulse Dialer Circuit with Redial (Single Hook Switch Contact Application for PABX)



$R_1 = 10\text{-}20M\Omega$, $R_2 = 2k\Omega$
$R_3 = 470k\Omega$, R_4, $R_5 = 10k\Omega$
R_6, $R_8 = 2k\Omega$, R_7, $R_9 = 30k\Omega$
$R_{10} = 47k\Omega$, $R_{11} = 20\Omega$, 2W
$Z_1 = 3.9V$, D_1—D_4 = IN4004
D_5, D_6, D_7 = IN914, $C_1 = 15\mu F$
R_E, $R_D = 750k\Omega$, $C_D = 270pF$
$C_2 = 0.01\mu F$, Q_1, Q_4 = 2N5550
Q_2, Q_3 = 2N5401
Z_2 = 150V ZENER OR VARISTOR TYPE GE MOV150

Figure 6. Circuit for Applying Momentary "ON Hook" Condition During Power Up

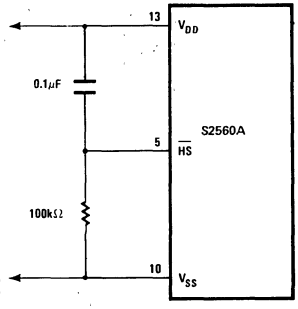
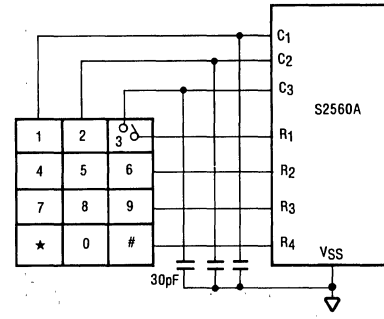


Figure 7. SPST Switch Matrix Interface



Pulse Dialer

S2560G/S2560G1

General Description

The S2560G is a modified version of the S2560A Pulse Dialer with complete pin/function compatibility. It is recommended to be used in all new and existing designs. Most electrical specifications for both devices are identical. Please refer to S2560A data sheet for details. S2560G1 is low voltage version of S2560G.

Differences between the two devices are summarized below:

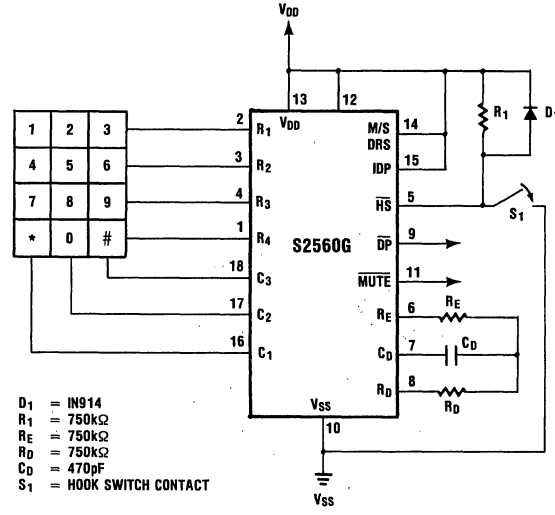
	2560G	2560G1	2560A
Operating Voltage, Dialing:	2.0V to 3.5V	1.5V to 3.5V	1.5V to 3.5V
Operating Voltage, Voice Mode:	1.5V to 3.5V	1.5V to 3.5V	1.5V to 3.5V
Data Retention Voltage (Minimum):	1.0V	1.0V	1.0V
I_{DD} Operating Current:	200μA@2.0V 1000μA@3.5V	100μA@1.5V 500μA@3.5V	100μA@1.5V 500μA@3.5V
I_{DD} Standby Current:	2μA@1V	750nA @ 1V	750nA@1V
Keyboard Debounce Time:	10msec		16msec
X-Y Keyboard Interface:	Does not need capacitors		Capacitors required between column inputs and V_{SS}
Redial Buffer:	22 digits		20 digits
Dialing Characteristics:	Can dial more than 22 digits. Redial disabled if more than 22 digits are entered.		Accepts a maximum of 20 digits. Will not dial additional digits.
Inter-digit pause timing	Follows dial pulses.		Precedes dial pulses

Application Suggestions

1) In most existing designs, the S2560G will work in place of S2560A without any modifications. Problems may arise however, if the keyboard bounce time exceeds 10ms. In such a case, the device may interpret a single key entry as a double key. To avoid this false detection, the keyboard debounce time can be easily increased from 10ms to 20ms by changing the Oscillator Frequency from 2400Hz down to 1200Hz. This is done by changing the value of the capacitor connected to pin 7 from 270pF to 470pF. To preserve the dialing rate at 10pps and IDP at 800ms the DRS and IDP pins now must be connected to V_{DD} instead of V_{SS}. Figure 1 shows the implementation details. Note, that interfacing with X-Y keyboard no longer requires capacitors to V_{SS} from column pins.

2) The hookswitch input pin (pin 5) must be protected from spikes that can occur when the phone goes from off-hook condition to on-hook. Voltage exceeding V_{DD} on this pin can cause the device to draw excessive current. This will discharge the capacitor across V_{DD} and V_{SS} causing the supply voltage to drop. If the voltage drops below 1 volt (data retention voltage) the device could lose redial memory. To prevent the voltage on the hookswitch pin from exceeding V_{DD}, an external diode must be added on the hookswitch pin as shown in Figure 1.

Figure 1. Transient Protection Technique Using Diode Between V_{DD} and $\overline{HS}$



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AMI Semiconductors

Tone Ringer

S2561/S2561A

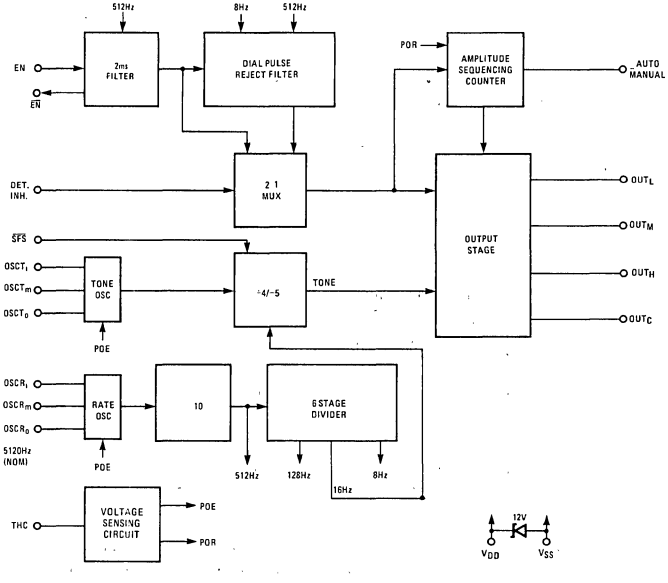
Features

- ☐ CMOS Process for Low Power Operation
- ☐ Operates Directly from Telephone Lines with Simple Interface
- ☐ Provides a Tone Signal that Shifts Between Two Predetermined Frequencies at Approximately 16Hz to Closely Simulate the Effects of the Telephone Bell
- ☐ Push-Pull Output Stage Allows Direct Drive, Eliminating Capacitive Coupling and Provides Increased Power Output
- ☐ 50mW Output Drive Capability at 10V Operating Voltage
- ☐ Auto Mode Allows Amplitude Sequencing such that the Tone Amplitude Increases in Each of the First Three Rings and Thereafter Continues at the Maximum Level
- ☐ Single Frequency Tone Capability

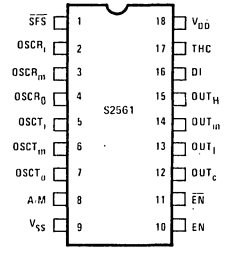
General Description

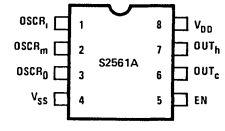
The S2561 Tone Ringer is a CMOS integrated circuit that is intended as a replacement for the mechanical telephone bell. It can be powered directly from the telephone lines with minimum interface and can drive a speaker to produce sound effects closely simulating the telephone bell.

Block Diagram



Pin Configuration





S2561/S2561A

Absolute Maximum Ratings:

Supply Voltage	+12.0V*
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−40°C to +125°C
Voltage at any Pin	V_{SS} −0.3V to V_{DD} +0.3V
Lead Temperature (Soldering, 10sec)	300°C

*This device incorporates a 12V internal zener diode across the VDD to VSS pins. Do NOT connect a low impedance power supply directly across the device unless the supply voltage can be maintained below 12V or current limited to <25mA.

Electrical Characteristics:

Specifications apply over the operating temperature and $3.5V \leqslant V_{DD}$ to $V_{SS} < 12.0V$ unless otherwise specified.

Symbol	Parameter	Min.	Max.	Units	Conditions
V_{DS}	Operating Voltage (V_{DD} to V_{SS})	8.0	12.0	V	Ringing, THC pin open
V_{DS}	Operating Voltage	4.2		V	"Auto" mode, non-ringing
I_{DS}	Operating Current		500	μA	Non-ringing, V_{DD} = 10V, THC pin open, DI pin open or V_{SS}
I_{OHC}	Output Drive Output Source Current (OUT_H, OUT_C outputs)	5		mA	V_{DD} = 10V, V_{OUT} = 8.75V
I_{OLC}	Output Sink Current (OUT_H, OUT_C outputs)	5		mA	V_{DD} = 10V, V_{OUT} = 0.75V
I_{OHM}	Output Source Current (Out_M output)	2		mA	V_{DD} = 10V, V_{OUT} = 8.75V
I_{OLM}	Output Sink Current (OUT_M output)	2		mA	V_{DD} = 10V, V_{OUT} = 0.75V
I_{OHL}	Output Source Current (OUT_L output)	1		mA	V_{DD} = 10V, V_{OUT} = 8.75V
I_{OLL}	Output Sink Current (OUT_L output)	1		mA	V_{DD} = 10V, V_{OUT} = 0.75V
	CMOS to CMOS				
V_{IH}	Input Logic "1" Level	0.7 V_{DD}	V_{DD} + 0.3	V	All inputs
V_{IL}	Input Logic "0" Level	V_{SS} − 0.3	0.3 V_{DD}	V	All inputs
V_{OHR}	Output Logic "1" Level (Rate output)	0.9 V_{DD}		V	I_O = 10μA (Source)
V_{OLR}	Output Logic "0" Level (Rate output)		0.5	V	I_O = 10μA (Sink)
V_{OZ}	Output Leakage Current (OUT_H, OUT_M outputs in high impedance state)		1 1	μA μA	V_{DD} = 10V, V_{OUT} = 0V V_{DD} = 10V, V_{OUT} = 10V
C_{IN}	Input Capacitance		7.5	pF	Any pin
Δfo/fo	Oscillator Frequency Deviation	−5	+5	%	Fixed RC component values $1M\Omega \leqslant R_{ri}$, $R_{ti} \leqslant 5M\Omega$; $100k\Omega \leqslant R_{rm}$, $R_{tm} \leqslant 750k\Omega$; $150pF \leqslant C_{ro}$, $C_{to} \leqslant 3000pF$; 330pF recommended value of C_{ro} and C_{to}, supply voltage varied from 9V ± 2V (over temperature and unit-unit variations)
R_{LOAD}	Output Load Impedance Connected Across OUT_H and OUT_C	600		Ω	Tone Frequency Range = 300Hz to 3400Hz
I_{IH}, I_L	Leakage Current, $V_{IN} = V_{DD}$ or V_{SS}		100	nA	Any input, except DI pin V_{DD} = 10V
V_{TH}	POE Threshold Voltage	6.5	8	V	
V_Z	Internal Zener Voltage	11	13	V	I_Z = 5mA

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leqslant V_I \leqslant V_{DD}$ as a maximum limit). This rule will prevent over-dissipation and possible damage of the input-protection diode when the device power supply is grounded.

Functional Description

The S2561 is a CMOS device capable of simulating the effects of the telephone bell. This is achieved by producing a tone that shifts between two predetermined frequencies (512 and 640Hz) with a frequency ratio of 5:4 at a 16Hz rate.

Tone Generation: The output tone is derived from a tone oscillator that uses a 3 pin R-C oscillator design consisting of one capacitor and two resistors. The oscillator frequency is divided alternately by 4 or 5 at the shift rate. Thus, with the oscillator adjusted for 5120Hz, a tone signal is produced that alternates between 512Hz and 640Hz at the shift rate. The shift rate is derived from another 3 pin R-C oscillator which is adjusted for a nominal frequency of 5120Hz. It is divided down to 16Hz which is used to produce the shift in the tone frequency. It should be noted that in the special case where both oscillators are adjusted for 5120Hz, it is only necessary to have one external R-C network for one oscillator with the other oscillator driven from it. The oscillators are designed such that for fixed R-C component values an accuracy of ±5% can be obtained over the operating supply voltage, temperature and unit-unit variations. See Table 2 for component and frequency selections. In the single frequency mode, activated by connecting the $\overline{SFS}$ input to V_{SS} only the higher frequency continuous tone is produced by using a fixed divider ratio of 4 and by disabling the shift operation.

Ring Signal Detection: In the following description it is assumed that both the tone and rate oscillators are adjusted for a frequency of 5120Hz. Ringing signal (nominally 42 to 105 VAC, 20Hz, 2 sec on/4 sec off duty cycle) applied by the central office between the telephone line pair is capacitively coupled to the tone ringer circuitry as shown in Figure 2. Power for the device is derived from the ringing signal itself by rectification (diodes D1 thru D4) and zener diode clamping (Z_2). The signal is also applied to the EN input after limiting and clamping by a resistor (R_2) and internal diodes to V_{DD} and V_{SS} supplies. Internally the signal is first squared up and then processed thru a 2ms filter followed by a dial pulse reject filter. The 2ns filter is a two-stage register clocked by a 512Hz signal derived from the rate oscillator by a divide by 10 circuit. The squared ring signal (typically a square wave) is applied to the D input of the first stage and also to reset inputs of both stages. This provides for rejection of spurious noise spikes. Signals exceeding a duration of 2ms only can pass through the filter.

The dial pulse reject filter is clocked at 8Hz derived from the rate oscillator by divide by 640 circuit. This circuit is designed to pass any signal that has at least two transitions in a given 125ms time period. This insures that signals below 8Hz will be rejected with certainty. Signals over 16Hz will be passed with certainty and between 8Hz and 16Hz there is a region of uncertainty. By adjusting the rate oscillator to a different frequency the break points of 10Hz and 20Hz the rate oscillator can be adjusted to 6400Hz. Of course this also increases the tone shift rate to 20Hz. The action of the dial pulse reject filter minimizes the dial pulse interference during dialing although it does not completely eliminate it due to the rather large region of uncertainty associated with this type of discrimination circuitry. The dial pulse filter also has the characteristic that an input signal is not detected unless its duration exceeds 125ms. This insures that the tone ringer will not respond to momentary bursts of ringing less than 125 milliseconds in duration (Ref. 1).

In logic interface applications, the 2ms filter and the dial pulse reject filter can be inhibited by wiring the Det. INHIBIT pin to V_{DD}. This allows the tone ringer to be enabled by a logic '1' level applied at the "ENABLE" input without the necessity of a 20Hz ring signal.

Voltage Sensing: The S2561 contains a voltage sensing circuit that enables the output stage and the rate and tone oscillators, only when the supply voltage exceeds a predetermined value. Typical value of this threshold is 7.3 volts. This prduces two benefits. First, it insures that the audible intensity of the output tone is fairly constant throughout the ringing period; and secondly, it insures proper circuit operation during the "auto" mode operation by reducing the power consumption to a minimum when the supply voltage drops below 7.3 volts. This extends the supply voltage decay time beyond 4 seconds (off period of the ring signal) with an adequate filter capacitor and insures the proper functioning of the "amplitude sequencing" counter. It is important to note that the operating supply voltage should be well above the threshold value during the ringing period and that the filter capacitor should be large enough so that the ripple on the supply voltage does not fall below the threshold value. A supply voltage of 10 to 12 volts is recommended.

In applications where the tone ringer is continuously powered and below the threshold level, the internal threshold can be bypassed by connecting the THC pin to V_{DD}. The internal threshold can also be reduced by

connecting an external zener diode between the THC and V_{DD} pins.

Auto Mode: In the "auto" mode, activated by wiring the "auto/manual" input to V_{SS}, an amplitude sequencing of the output tone can be achieved. Resistors R_L and R_M are inserted in series with the Out_L and Out_M outputs, respectively, and paralleled with the Out_H output (Figure 1). Load is connected across Out_H and Out_C pins. R_L is chosen to be higher than R_M. In this manner the first ring is of the lowest amplitude, second ring is of medium amplitude and the third and consecutive rings thereafter are at maximum amplitude. For the proper functioning of the "amplitude sequencing" counter the device must have at least 4.2 volts across it throughout the ring sequence. The filter capacitor is so chosen that the supply voltage will not drop below 4.0 volts during the off period. At the end of a ring sequence when the off period substantially exceeds the 4 second duration, the counter will be reset. This will insure that the amplitude sequencing will start correctly beginning a new ring sequence. The counter is held in reset during the "manual" mode operation. This produces a maximum ring amplitude at all times.

Figure 1-A. Output Stage Connected for Auto Mode Operation

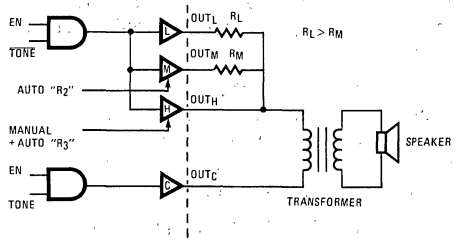


Figure 1-B. Output Stage Connected for Manual Mode Operation

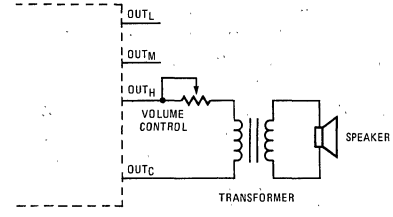
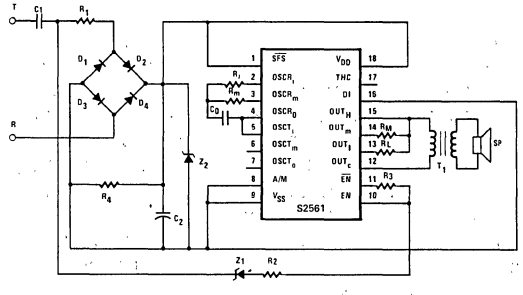
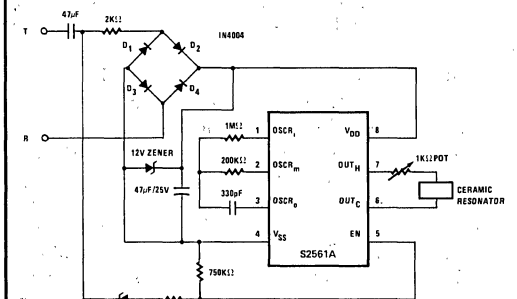


Figure 2-A. Typical Telephone Application of the S2561



C_1	.47μF/200V	R_1	2KΩ	R_l	1MΩ	R_L	18KΩ	SP	8ΩSPEAKER
C_2	47μF/25V	R_2	51KΩ	R_m	200KΩ	R_M	3.3KΩ	T_1	2000Ω/8ΩXFMR
D_1–D_4	IN4004	R_3	10MΩ	C_0	300pF	R_4	100KΩ	Z_1	9 TO 27V ZENER
Z_2	IN4742 12V ZENER								

Figure 2-B. Typical Telephone Application of the S2561A



Output Stage: The output stage is of push-pull type consisting of buffers L, M, H and C. The load is connected across pins Out_H and Out_C (Figure 2). During ringing, the Out_H and Out_C outputs are out of phase with each other and pulse at the tone rate. During a non-ringing state, all outputs are forced to a known level such as ground which insures that there is no DC component in the load. Thus, direct coupling can be used for driving the load. The major benefit of the push-pull arrangement is increased power output. Four times as much power can be delivered to the load for the same operating voltage. Buffers M and H are three-state. In the "auto" mode buffer M is active only during the second ring and in the "high impedance" state at all other times. Buffer H is active beginning the third ring. In the "manual" mode buffers H, L and C are active at all times while buffer M is in a high impedance state. The output buffers are so designed that they can source or sink 5mA at a V_{DD} of 10 volts without appreciable voltage drop. Care has been taken to make them symmetrical in both source and sink configurations. Diode clamping is provided on all outputs to limit the voltage spikes associated with transformer drive in both directions V_{DD} and V_{SS}.

Normal protection circuits are present on all inputs.

Table 1. S2561 (S2561A) Pin/Function Descriptions

Pin	Number	Function
Power (V_{DD}*, V_{SS}*)	18, 9 (8, 4)	These are the power supply pins. The device is designed to operate over the range of 3.5 to 12.0 volts. A range of 10 to 12 volts is recommended for the telephone application.
Ring Enable (EN*, $\overline{EN}$)	10, 11, (5)	These pins are for the 20Hz ring enable input. They can also be used for DC level enabling by wiring the DI pin to V_{DD}. $\overline{EN}$ is available for the S2561 only.
Auto/Manual (A/M)	8	"Auto" mode for amplitude sequencing is implemented by wiring this pin to V_{SS}. "Manual" mode results when connected to V_{DD}. The amplitude sequencing counter is held in reset during the "manual" mode.
Outputs (Out_L, Out_M, Out_H^*, Out_C^*)	13, 14, 15, (7, 6)	These are the push-pull outputs. Load is directly connected across Out_H and Out_C outputs. In the "auto" mode, resistors R_L and R_M can be inserted in series with the Out_L and Out_M outputs for amplitude sequencing (see Figure 1).
Oscillators Rate Oscillator ($OSCR_i^*$, $OSCR_m^*$ $OSCR_o^*$)	2, 3, 4, (1, 2, 3)	These pins are provided to connect external resistors RR_i, RR_m and capacitor CR_o to form an R-C oscillator with a nominal frequency of 5120Hz. See Table 2 for components selection.
Tone Oscillator ($OSCT_i$, $OSCT_m$, $OSCT_o$)	5, 6, 7	These pins are provided to connect external resistors RT_i, RT_m and capacitor CT_o to form an R-C oscillator from which the tone signal is derived. With the oscillator adjusted to 512Hz and 640Hz results. See Table 2 for components selection.
Threshold Control (THC)	17	The internal threshold voltage is brought out to this pin for modification in non-telephone applications. It should be left open for telephone applications. For power supplies less than 9V connect to V_{DD}.

Table 1. (Continued)

Pin	Number	Function
Detector Inhibit (DI)	16	When this pin is connected to V_{DD}, the dial pulse reject filter is disabled to allow DC level enabling of the tone ringer. This pin should be hardwired to V_{SS} in normal telephone-type applications.
Single Frequency Select (SFS)	1	When this pin is connected to V_{SS}, only a single frequency continuous tone is produced as long as the tone ringer is enabled. In normal applications this pin should be hardwired to V_{DD}.

*Pinouts of 8 pin S2561A package.

Table 2. Selection Chart for Oscillator Components and Output Frequencies

Tone/Rate Oscillator Frequency (Hz)	Oscillator Components R_I (kΩ)	R_M (kΩ)	C_O (pF)	Rate (Hz)	Tone (Hz)
5120	1000	200	330	16	512/640
6400	Select components in the ranges indicated in the table of electrical characteristics			20	640/800
3200				10	320/400
8000				25	800/1000
fo				fo/320	fo/10 fo/8

Applications

Typical Telephone Application: Figure 2 shows the schematic diagram of a typical telephone application for the S2561 tone ringer. Circuit power is derived from the telephone lines by the network formed by capacitor C_1, resistor R_1, diode bridge D_1 through D_4, and filter capacitor C_2. C_2 is chosen to be large enough so as to insure that the power supply ripple during ringing does not fall below the internal threshold level (typ. 7.3 volts) and to provide large enough decay time during the off period. A typical value of C_2 may be .47μF. C_1 and R_1 are chosen to satisfy the Ringer Equivalence Number (REN) specification (Ref. 1). For REN = 1 the resistor should be a minimum of 8.2kΩ. It must be noted that the amount of power that can be delivered to the load depends upon the selection of C_1 and R_1.

The device is enabled by limiting the incoming ring signal through resistors R_2, R_3 and diodes d_5 and d_6. Zener diode Z_1 (typ. 9-27 volts) may be required in certain applications where large voltage transients may occur on the line during dial pulsing. The internal 2ms filter and the dial pulse reject filter will suppress any undesirable components of the signal and will only respond to the normal 20Hz ring signal. Ring signals with frequencies above 16Hz will be detected.

The configuration shown will produce a tone with frequency components of 512Hz and 540 Hz with a shift rate of approximately 16 Hz and deliver at least 25mW to an 8Ω speaker through a 2000Ω:8Ω transformer. If "manual" mode is used, a potentiometer may be inserted in series with the transformer primary to provide volume control. If "automatic" mode is used, resistors R_L and R_M can be chosen to provide desired amplitude sequencing. Typically, signal power

will be down 20 log $\frac{R_{LOAD}}{R_L + R_{LOAD}}$ dB during the

first ring, and down 20 log $\frac{R_{LOAD}}{R_M + R_{LOAD}}$ dB during the

second ring with maximum power delivered to the load beginning the third and consecutive rings.

In applications where dial pulse rejection is not necessary, such as in DTMF telephone systems, the ENABLE pin may be connected directly to V_{DD}. Det. Inh pin must be connected to V_{DD} to allow DC level enabling of the ringer.

Reference 1. Bell system communications technical reference: PUB 47001 of August 1976. "Electrical Characteristics of Bell System Network Facilities at the Interface with Voiceband Ancilliary and Data Equipment"—2.6.1. and 2.6.3

GOULD

AMI Semiconductors

DTMF Tone Generator With Redial

S2569/S2569A

COMMUNICATION PRODUCTS

Features

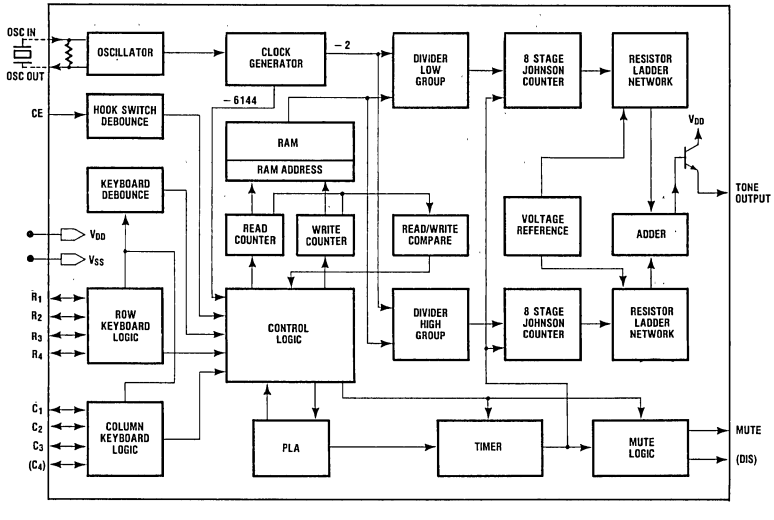
- ☐ Wide Operating Supply Voltage Range (2.50–10V)
- ☐ Low Power CMOS Circuitry Allows Device Power to be Derived Directly from the Telephone Lines
- ☐ 21 Digit Memory for Redial
- ☐ Uses Standard 3x4 (S2569A) or 4x4 (S2569) SPST or X-Y Matrix Keyboard
- ☐ The Total Harmonic Distortion is Below Industry Specification (Max. 7% Over Typical Loop Current Range)
- ☐ Separate Control Keys (S2569) for Disconnect, Pause, Redial and Flash in Column Four
- ☐ Allows Dialing of * and # Keys on S2569. For S2569A Redial Initiated by * or # Key as First Key Offhook, * or # can be Dialed After First Key Offhook.

General Description

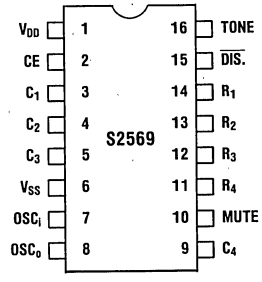
The S2569/S2569A are members of the S2559 Tone Generator family with the added features of Redial, Disconnect, Pause and Flash. They produce the 12 dual tones corresponding to the 12 keys located on the conventional Touch-Tone® telephone keypad. The S2569 has separate keys, located in column four, which initiate the Disconnect(D), Pause(P), Redial(R), and Flash(F) functions. (Note: column four keys do not generate tones.) Only the redial feature is available on the S2569A. Redial on the S2569A is initiated by pressing * or # as the first key offhook.

A voltage reference generated on the chip regulates the signal levels of the dual tones to meet the recommended telephone industry specifications.

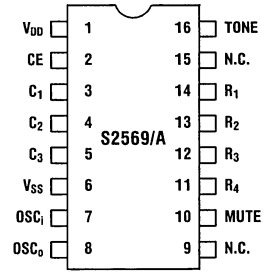
Block Diagram



S2569 Pin Configuration



S2569/A Pin Configuration



Touch-Tone is a registered trademark of AT&T

S2569/S2569A

Absolute Maximum Rating:

DC Supply Voltage (V_{DD}-V_{SS})	+13.5V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +140°C
Power Dissipation at 25°C	500mW
Input Voltage	$V_{SS} - 0.6 < V_{IN} < V_{DD} + 0.6V$

S2569A Electrical Characteristics: Specifications apply over the operating temperature range of 0°C to +70°C unless otherwise noted. Absolute values of measured parameters are specified.

Symbol	Parameter/Conditions	($V_{DD} - V_{SS}$) Volts	Min.	Max.	Unit
	Supply Voltage				
V_{DD}	Tone Out Mode (Valid Key Depressed)		2.50	10.0	V
	Non Tone Out Mode (No Key Depressed)		1.50	10.0	V
V_{DR}	Data Retention Voltage		1.0		V
	Supply Current				
I_{DD}	STANDBY (NO Key Depressed, Tone, Mute and Flash Outputs Unloaded, CE = low	2.00 5.00		1 20	μA μA
	Operating (One Key Selected, Tone, Mute and Flash Outputs Unloaded).	3.00		2.5	mA
	Operating During Flash	3.0		300	μA
	Tone Output				
V_{OR}	Low Group Frequency Voltage ($R_L = 390\Omega$)	5.0	330	690	mVrms
dBcr	Ratio Of Column To Row Tone	2.5–5.0	1.0	3.0	dB
% DIS	Distortion*	2.5–10.0		7	%
	Mute and Flash Outputs				
I_{OH}	Output Source Current $V_{OH} = 2.7V$	3.0	1.0		mA
I_{OL}	Output Sink Current $V_{OL} = 0.3V$	3.0	1.0		mA

* Distortion measured in accordance with the specifications described as "ratio of total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".

NOTE: R_L = load resistor connected from output to V_{SS}.

Basic Chip Operation

The dual tone signal consists of linear addition of two voice frequency signals. One of four signals is selected from a group of frequencies called "low group" and the other is selected from a group of frequencies called "high group". The low group consists of four frequencies; 697, 770, 852 and 941 Hz. The high group consists of three frequencies; 1209, 1336 and 1477 Hz.

When a push button corresponding to a digit (0 thru 9, *, #) is pushed, one appropriate row (R_1 thru R_4) and one appropriate column (C_1 thru C_3) is selected. The active row input selects one of the low group frequencies and active column input selects one of the high group frequencies.

Tone Generation

When a valid key closure is detected, the keyboard logic programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divide-by-16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function. This is done by connecting a weighted resistor ladder network between the outputs of the Johnson counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude V_P ($V_{DD}-V_{REF}$) of the stairstep function is fairly constant. V_{REF} is chosen so that V_P falls within the allowed range of the high group and low group tones.

Normal Dialing

Tone dialing starts as soon as the first digit is entered and debounced. The entered digits are stored sequentially in the internal memory. Pauses may be entered when required in the dial sequence by pressing the "P" key, which provides access pause for future redial. Any number of access pauses may be entered as long as the total entries do not exceed the total number of available digits. Numbers up to 21 digits can be redialed. Numbers exceeding 21 digits will clear redial buffer. Note that only the S2569 has "Pause" capability and the access pause is included in the 21 digit maximum number.

Redial

The last number dialed is retained in the memory and therefore can be redialed by going off hook and pressing the "R" key on the S2569 (located at column 4 and row 3). The S2569A does not use column four and Redial is initiated by "#" or "*" key as the first key off-hook. Tone dialing will start when the key is depressed and finish after the entire number is dialed out unless an access pause is detected. In such a case, the tone dialing output will stop and will resume only after the user pushes any key except Flash and Disconnect keys. During redial all keys are ignored until 70ms after the last digit is dialed (except Disconnect). (Note that the "Pause" function is not available on the S2569A.)

Disconnect/Flash Functions

The S2569 has a push-pull buffer for Disconnect output. With no keys depressed the Disconnect output is high. When the Disconnect key is depressed the Disconnect output goes low until the key is released. Disconnect output can also be used to implement a "Flash" function. When the Flash key is depressed the Disconnect output goes low for 608ms.

Figure 1

1	2	3	D
4	5	6	P
7	8	9	R
*	0	#	F

S2569 Keypad

1	2	3
4	5	6
7	8	9
*	0	#

S2569A Keypad

Keyboard Interface

The S2569/A employs a scanning circuitry to determine key closures. When no key is depressed active pull down resistors are on on the row inputs and active pull up resistors are on on the column inputs. When a key is pushed a high level is seen on one of the row inputs, the oscillator starts and the keyboard scan logic turns on. The active pull up or pull down resistors are selectively switched on and off as the keyboard scan logic determines the row and the column inputs that are selected. The value of pull down and pull up resistors will vary with supply voltage. Typical values of pull up and pull down resistors are shown in Table 1.

Table 1. Typical Resistance Values

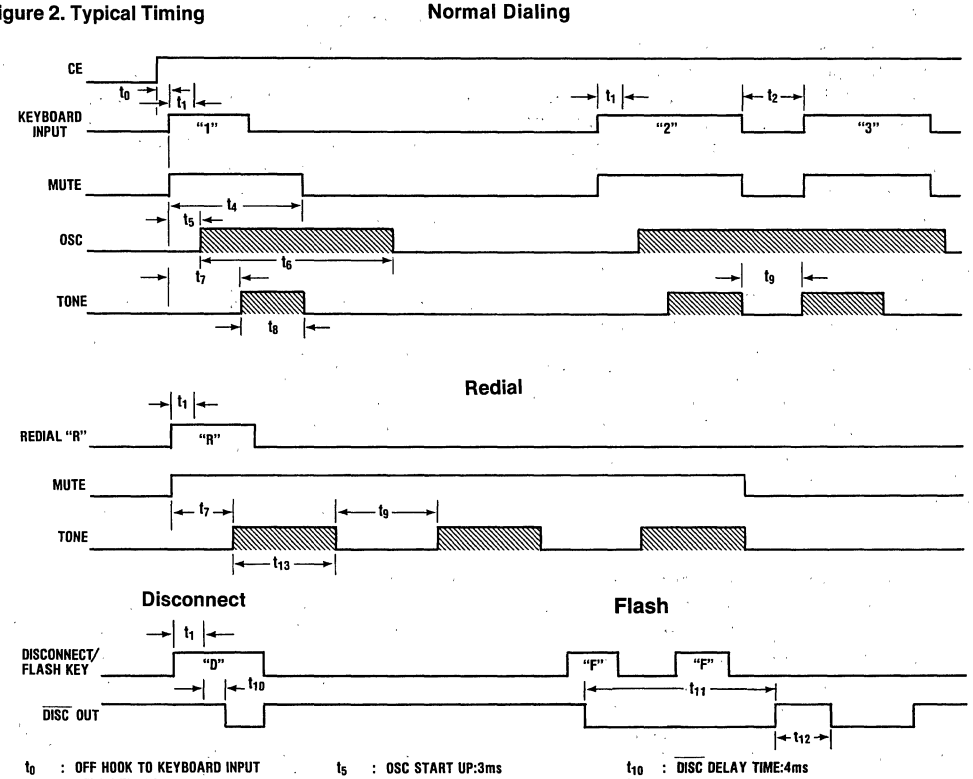
V_{DD}	PULL UP RESISTANCE (TYP.)
2.0V	3.3 K ohm
5.0V	1.5 K ohm
10.0V	1.3 K ohm
V_{DD}	**PULL DOWN RESISTANCE (TYP.)**
2.0V	340 K ohm
5.0V	36.6 K ohm
10.0V	16.6 K ohm

Table 2. Comparisons of Specified Vs. Actual Tone Frequencies Generated by S2569/A

ACTIVE INPUT	OUTPUT FREQUENCY HZ SPECIFIED	ACTUAL	% ERROR
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.9	+0.57
C2	1339	1331.7	−0.32
C3	1477	1471.9	−0.35

NOTE: % error does not include oscillator drift.

Figure 2. Typical Timing



t_0 : OFF HOOK TO KEYBOARD INPUT DELAY TIME:0ms
t_1 : DEBOUNCE TIME:18ms
t_2 : KEY RELEASE TIME:6ms
t_4 : MIN. MUTE PULSE WIDTH:73ms
t_5 : OSC START UP:3ms
t_6 : OSC MIN. ON TIME:142ms
t_7 : TONE OUTPUT DELAY TIME:21ms
t_8 : MIN. TONE OUT TIME:70ms
t_9 : MIN. OFF TIME:70ms
t_{10} : $\overline{\text{DISC}}$ DELAY TIME:4ms
t_{11} : OUTPUT PULSE:608ms
t_{12} : MIN. DISC OFF TIME:50ms
t_{13} : TONE ON TIME:70ms

Logic Interface

The S2569/A can also interface with CMOS logic outputs directly. The S2569/A requires active high logic levels. Since the pull up resistors present in the S2569/A are fairly low values, diodes can be used to eliminate excessive sink current flowing into the logic outputs in their low logic state.

Figure 3a. Typical Application Circuit for Line Powered DTMF Dialer With Redial S2569

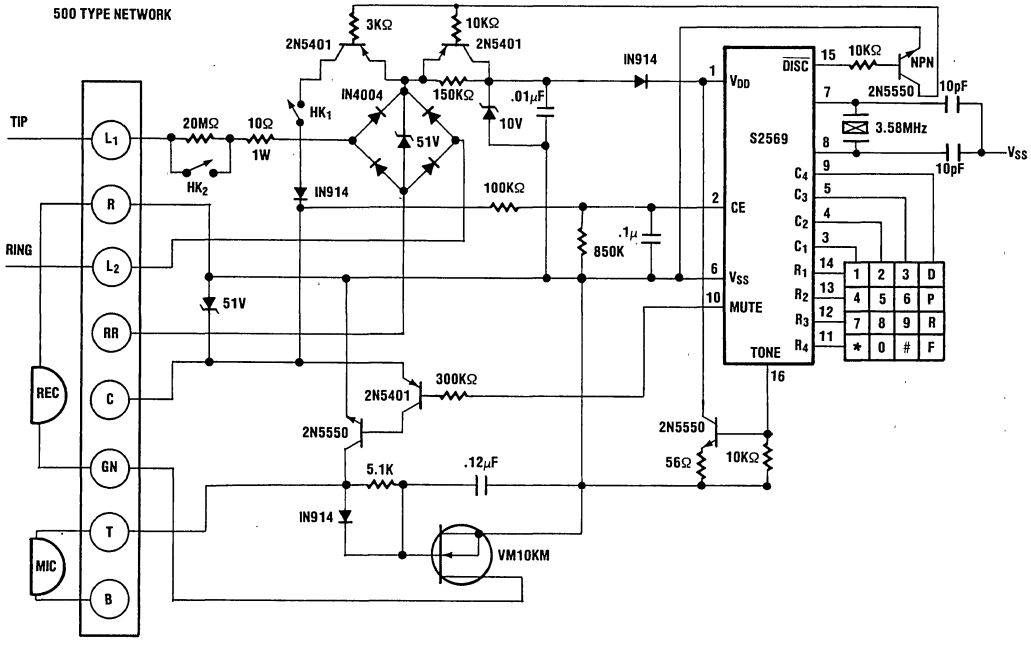
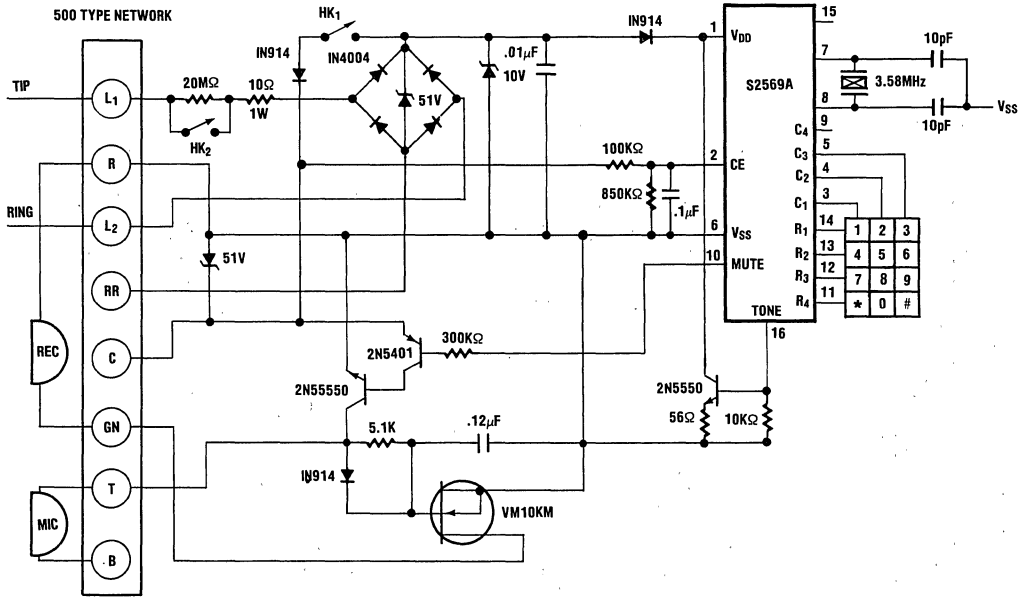


Figure 3b. Typical Application Circuit for Line Powered DTMF Dialer With Redial S2569A



Chip Enable

The S2569/A has a Chip Enable input at pin 2. The Chip Enable for the S2569/A is an active "high". When the Chip Enable is "low", the Tone output goes to V_{SS}, the oscillator is inhibited and the Mute and Disconnect outputs will go into a low state.

Mute Output

The S2569/A has a push-pull buffer for Mute output. With no keys depressed the Mute output is low, when a key is depressed the Mute output goes high until the key is released. Note that minimum mute pulse width is 70ms.

Oscillator

The device contains an oscillator circuit with the necessary parasitic capacitances and feedback resistor (1MΩ) on chip so that it is only necessary to connect a standard 3.58MHz TV crystal across the OSC_i and OSC_o terminals to implement the oscillator function.

Oscillator Crystal Specifications

Quartz Crystal Specification (25°C ±2°C)	
Operating Temperature Range	0°C to +70°C
Frequency	3.579545MHz
Frequency Calibration Tolerance	.02± %
Load Capacitance	18pF
Effective Series Resistance	180 Ohms, max.
Drive Level-Correlation/Operating	2mW
Shunt Capacitance	7pF, max.
Oscillation Mode	Fundamental

Test Mode

The S2569/A will enter the test mode if all rows are pulled high momentarily. 16 times the low group frequency will appear at mute output depending on which row is selected. Also, 16 times the high group frequency will appear at disconnect output depending upon which column is selected.

GOULD

AMI Semiconductors

DTMF Tone Generator

S25089

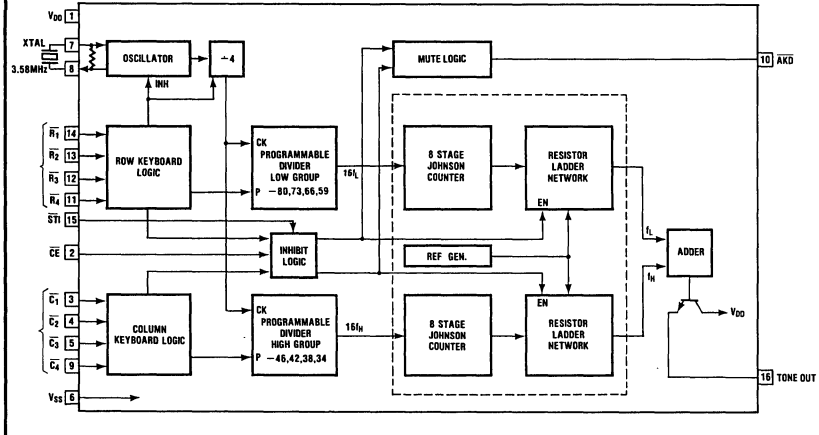
Features

- ☐ Wide Operating Voltage Range: 2.5 to 10 Volts
- ☐ Optimized for Constant Operating Supply Voltages, Typically 3.5V
- ☐ Tone Amplitude Stability is Within ±1.5dB of Nominal Over Operating Temperature Range
- ☐ Low Power CMOS Circuitry Allows Device Power to be Derived Directly From the Telephone Lines or From Small Batteries
- ☐ Now Available in 16 pin Small Outline IC Package for Space Savings
- ☐ Uses TV Crystal Standard (3.58MHz) to Derive All Frequencies Thus Providing Very High Accuracy and Stability
- ☐ Specifically Designed for Electronic Telephone Applications
- ☐ Interfaces Directly to a Standard Telephone Push-Button Keyboard With Common Terminal
- ☐ Low Total Harmonic Distortion
- ☐ Single Tone as Well as Dual Tone Capability
- ☐ Direct Replacement for Mostek MK5089 Tone Generator in most Applications

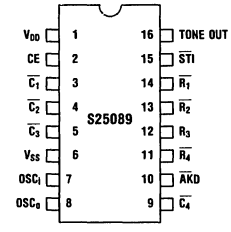
General Description

The S25089 DTMF Generator is specifically designed to implement a dual tone telephone dialing system in applications requiring fixed supply operation and high stability tone output level, making it well suited for electronic telephone applications. The device can interface directly to a standard pushbutton telephone keyboard with common terminal connected to V_{SS} and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinusoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. A voltage reference is generated on the chip which is very stable over the operating temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications.

Block Diagram



Pin Configuration



ALSO AVAILABLE IN 16 PIN SOIC PACKAGE WITH SAME PINOUT.

S25089

Absolute Maximum Ratings:

DC Supply Voltage (V_{DD}-V_{SS})	+10.5V
Operating Temperature:	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation at 25°C	500mW
Input Voltage	$V_{SS} - 0.6 \leq V_{IN} \leq V_{DD} + 0.6$
Input/Output Current (except tone output)	15mA
Tone Output Current	50mA

Electrical Characteristics: (Specifications apply over the operating temperature range of 0°C to +70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions		(V_{DD}-V_{SS}) Volts	Min.	Typ.	Max.	Units
	Supply Voltage						
V_{DD}	Tone Out Mode (Valid Key Depressed)			2.5	—	10.0	V
	Non Tone Out Mode ($\overline{AKD}$ Outputs toggle with key depressed)			1.6	—	10.0	V
	Supply Current						
I_{DD}	Standby (No Key Selected,		3.0	—	1	20	μA
	Tone and $\overline{AKD}$ Outputs Unloaded)		10.0	—	5	100	μA
	Operating (One Key Selected,		3.0	—	.9	1.25	mA
	Tone and $\overline{AKD}$ Outputs Unloaded)		10.0	—	4.5	10.0	mA
	Tone Output						
V_{OR}	Dual Tone Row Tone	$R_L = 10k\Omega$	3.0	−11.0		−8.0	dBm
	Mode Output Amplitude	$R_L = 100k\Omega$	3.5	−10.0		−7.0	dB
dB_{CR}	Ratio of Column to Row Tone**		2.5-10.0	2.4	2.7	3.0	dB
%DIS	Distortion*		2.5-10.0	–	–	10	%
NKD	Tone Output—No Key Down					−80	dBm
	$\overline{AKD}$ Output						
I_{OL}	Output On Sink Current	$V_{OL} = 0.5V$	3.0	0.5	1.0	—	mA
I_{OH}	Output Off Leakage Current		10.00		1	10	μA
	Oscillator Input/Output						
t_{START}	Oscillator Startup Time with Crystal as Specified		3.0-10.0	—	2	5	ms
$C_{I/O}$	Input/Output		3.0	—	12	16	pF
	Capacitance		10.00	—	10	14	pF

*Distortion measured in accordance with the specifications described in REF. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".

**S25089-2 available with range of 1.0dB to 3.0dB.
S25088 available with 0dB ratio (column and row amplitude equal).

Electrical Characteristics: (Continued)

Symbol	Parameter/Conditions		(V_{DD}-V_{SS}) Volts	Min.	Typ.	Max.	Units
	Row, Column and Chip Enable Inputs						
V_{IL}	Input Voltage, Low		—	V_{SS}		.2(V_{DD} − V_{SS})	V
V_{IH}	Input Voltage, High		—	.8(V_{DD} − V_{SS}	—	V_{DD}	V
I_{IH}	Input Current	V_{IH} = 0.0V	3.0	30	90	150	μA
	(Pull up)	V_{IH} = 0.0V	10.0	100	300	500	μA

Oscillator

The S25089 contains an oscillator circuit with the necessary parasitic capacitances and feedback resistor on chip so that it is only necessary to connect a standard 3.58MHz TV crystal across the OSC_I and OSC_O terminals to implement the oscillator function. The oscillator functions whenever a row input is activated. The reference frequency is divided by 4 and then drives two sets of programmable dividers, the high group and the low group.

Crystal Specification

A standard television color burst crystal is specified to have much tighter tolerance than necessary for tone generation application. By relaxing the tolerance specification the cost of the crystal can be reduced. The recommended crystal specification is as follows:

Frequency: 3.579545MHz ±0.02%

R_S <100Ω, L_M = 96mH

C_M = 0.02pF C_H = 5pF C_L = 12pF

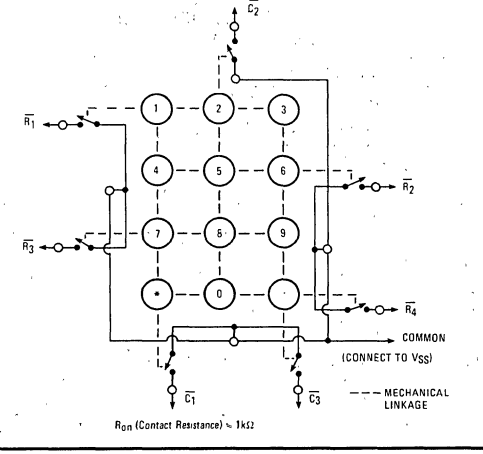
Keyboard Interface

The S25089 can interface with the standard telephone pushbutton keyboard (see Figure 1) with common. The common of the keyboard must be connected to V_{SS}.

Logic Interface

The S25089 can also interface with CMOS logic outputs directly (see Figure 2). The S25089 requires active "Low" logic levels. Low levels on a row and a column input corresponds to a key closure. The pull-up resistors present on the row and column inputs are in the range of 20kΩ–100kΩ.

Figure 1. Standard Telephone Push Button Keyboard



Tone Generation

When a valid key closure is detected, the keyboard logic programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divided by 16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function (see Figure 3). This is done by connecting a weighted resistor ladder network between the outputs of the Johnson

counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude VP (V_{DD}-V_{REF}) of the stair-step function is fairly constant. V_{REF} is so chosen that VP falls within the allowed range of the high group and low group tones.

The individual tones generated by the sinewave synthesizer are then linearly added and drive an NPN transistor connected as an emitter follower to allow proper impedance transformation at the same time preserving signal level. This allows the device to drive varying resistive loads without significant variation in tone amplitude. For example, a load resistor change from 10kΩ to 1kΩ causes a decrease in tone amplitude of less than 1dB.

Dual Tone Mode

When one row and one column is selected, dual tone output consisting of an appropriate low group and high group tone is generated. If two digit keys that are not either in the same row or in the same column are depressed, the dual tone mode is disabled and no output is provided.

Single Tone Mode

Single tones either in the low group or the high group can be generated as follows. A low group tone can be generated by depressing two digit keys in the appropriate row. A high group tone can be generated by depressing two digit keys in the appropriate column, i.e., selecting the appropriate column input and two row inputs in that column. This is slightly different from the MK5089 which requires a low to a single column pin to get a column tone.

Inhibiting Single Tones

The $\overline{STI}$ input (pin 15) is used to inhibit the generation of other than dual tones. It has an internal pull down to V_{SS} supply. When this input is left unconnected or connected to V_{SS}, single tone generation as described in the preceding paragraph (Single Tone Mode) is suppressed with all other functions operating normally. When this input is connected to V_{DD} supply, single or dual tones may be generated as previously described (Single Tone Mode, Dual Tone Mode).

Chip Enable Input (CE, Pin 2)

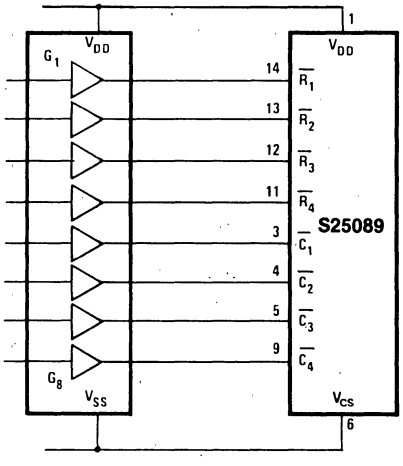
The chip enable input has an internal pull-up to V_{DD} supply. When this pin is left unconnected or connected to V_{DD} supply the chip operates normally. When connected to V_{SS} supply, tone generation is inhibited. All other chip functions operate normally.

Table 1. Comparison of Specified Vs. Actual Tone Frequencies Generated by S25089

ACTIVE INPUT	OUTPUT FREQUENCY Hz		%ERROR
	SPECIFIED	ACTUAL	SEE NOTE
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.9	+0.57
C2	1336	1331.7	−0.32
C3	1477	1471.9	−0.35
C4	1633	1645.0	+0.73

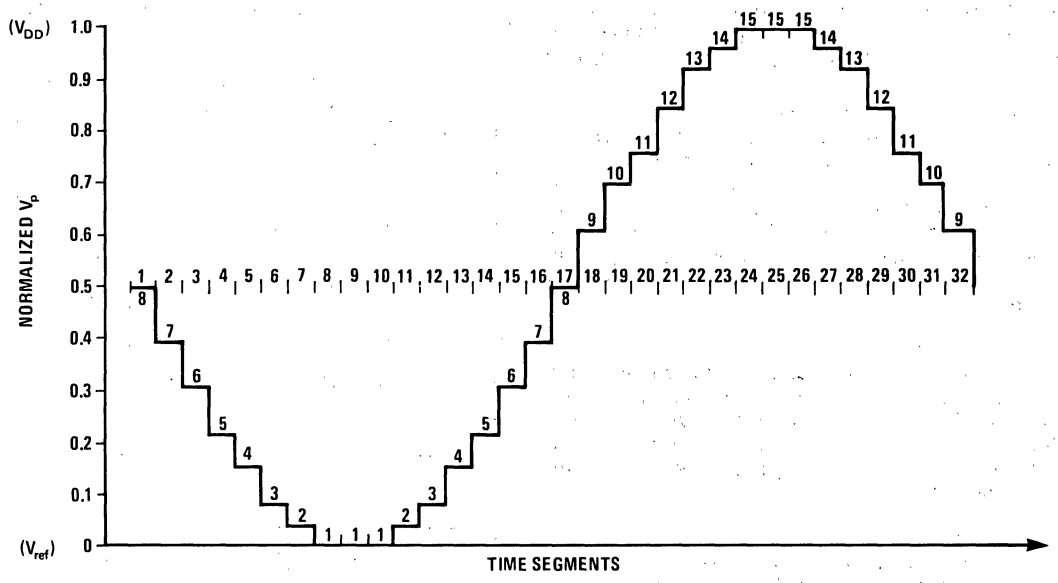
NOTE: %ERROR DOES NOT INCLUDE OSCILLATOR DRIFT

Figure 2. Logic Interface for Keyboard Inputs of the S25089



G1 THRU G8 ANY TYPE CMOS GATE

Figure 3. Stairstep Waveform of the Digitally Synthesized Sinewave



Reference Voltage

The structure of the reference voltage employed in the S25089 is shown in Figure 4. It has the following characteristics:

a) V_{REF} is proportional to the supply voltage. Output tone amplitude, which is a function of (V_{DD} - V_{REF}), increases with supply voltage (Figure 5).
b) The temperature coefficient of V_{REF} is low due to a single V_{BE} drop. Use of a resistive divider also provides an accuracy of better than 1%. As a result, tone amplitude variations over temperature and unit to unit are held to less than ± 1.0dB over nominal.
c) Resistor values in the divider network are so chosen that V_{REF} is above the V_{BE} drop of the tone output transistor even at the low end of the supply voltage range. The tone output clipping at low supply voltages is thus eliminated, which improves distortion performance.

$\overline{AKD}$ (Any Key Down or Mute) Output

The $\overline{AKD}$ output (pin 10) consists of an open drain N channel device (see Figure 6.) When no key is depressed the $\overline{AKD}$ output is open. When a key is depressed the $\overline{AKD}$ output goes to V_{SS}. The device is large enough to sink a minimum of 500μA with voltage drop of 0.2V at a supply voltage of 3.5V.

Figure 4. Structure of the Reference Voltage

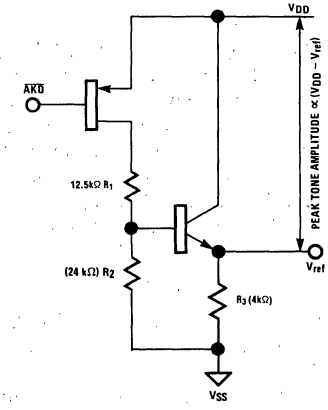


Figure 5. Typical Single Tone Output Amplitude Vs Supply Voltage (R_L = 10k)

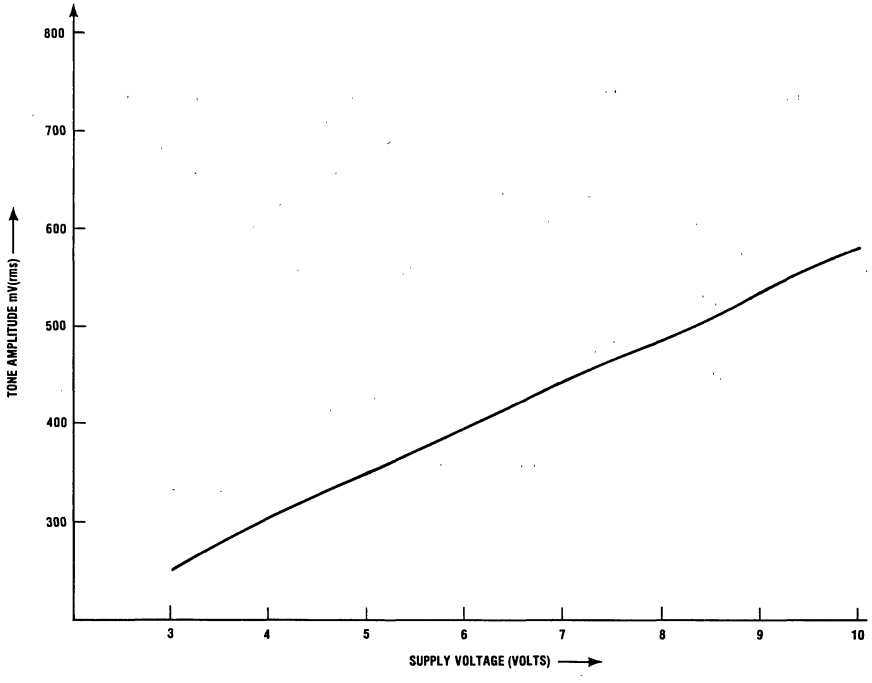
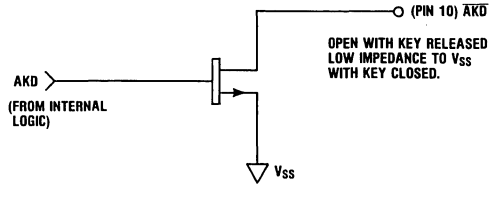


Figure 6. AKD output Structure



GOULD

AMI Semiconductors

DTMF Tone Generator With Binary Input

S2579

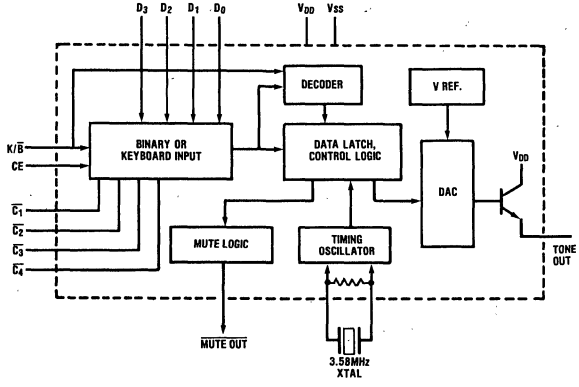
Features

- ☐ Available in 16 pin Small Outline IC Package for Space Savings
- ☐ Wide Operating Supply Voltage Range 3.0 to 10.0 Volts
- ☐ Direct Interface to TTL 4-Bit Logic for Binary Inputs or Standard X-Y Keyboard with Common Terminal
- ☐ Uses Low Cost 3.58MHz TV Crystal to Derive 16 Standard Dual Tone Frequencies
- ☐ Reference Voltage Generated On-Chip Eliminates External Circuitry
- ☐ Dual Tone and Single Tone Capabilities
- ☐ Low Power CMOS Circuitry Allows Telephone Line Power Operation

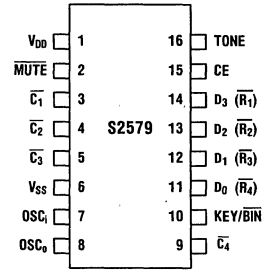
General Description

The S2579 binary input DTMF generator is a CMOS integrated circuit specially designed to accept external logic or microprocessor inputs. The S2579 can also be programmed to interface to 3x4 or 4x4 keyboard with common. The 16 standard dual tone frequencies are derived from a 3.58MHz crystal providing high accuracy and stability. A voltage reference is generated on the chip which is stable over the operating voltage and temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specification. Other applications for the S2579 include radio and mobile telephones, remote control, point-of-sale, and credit card verification terminals and process control.

Block Diagram



Pin Configuration



ALSO AVAILABLE IN 16 PIN SOIC

Absolute Maximum Ratings:

DC Supply Voltage ($V_{DD} - V_{SS}$)	+ 10.5V
Operating Temperature	0°C to + 70°C
Storage Temperature	− 55°C to + 125°C
Power Dissipation at 25°C	500mW
Input Voltage	$V_{SS} - 0.6 \leq V_{IN} \leq V_{DD} + 0.6$
Input/Output Current (except tone output)	15mA
Tone Output Current	50mA

Electrical Characteristics:
Specifications apply over the operating temperature range of 0°C to + 70°C unless otherwise noted. Absolute values of measured parameters are specified.

Symbol	Parameter/Conditions	(V_{DD}-V_{SS}) Volts	Min.	Typ.	Max.	Units
	Supply Voltage					
V_{DD}	Tone Output Mode (With Valid Data)		3.0	5.0	10.0	V
	Supply Current					
I_{DD}	Standby (No Key Selected, No Data, Tone and $\overline{Mute}$ Unloaded)	5.0 10.0		1.6 2.8	2.0 3.2	mA mA
	Operating (Tone and $\overline{Mute}$, Unloaded)	5.0 10.0		4.0 9.0	5.0 18.0	mA mA
R_p	Pullup Resistor (Column, Row and CE Inputs)	5.0 10.0	13 13	25 25		KΩ KΩ
	Key/$\overline{BIN}$ Select Unloaded)	5.0 10.0	13 13	25 25		KΩ KΩ
OSC	Operating Frequency	5.0- 10.0		3.58		MHz
	Tone Output					
V_{OR}	Low Band Alone $R_L = 150\Omega$	5.0	393	481	598	mVrms
dB_{CR}	Ratio of Column to Row Tone	5.0 10.0	1.0	2.0	3.0	dB
%DIS	Distortion*	5.0- 10.0		7	10	%
I_{OL}	Output Sink Current (Pin_2, $\overline{MUTE}$)	5.0	1.6	4.8		mA
D_{ST}	Data Setup Time	5.0	100			ns
D_{HT}	Data Hold Time	5.0	50			ns
	Logic Inputs					
V_{IL}	Input Voltage, Low	5.0			0.8	V
V_{IH}	Input Voltage, High	5.0	2.0			V

*Distortion measured in accordance with the specifications described in Ref. 1 as the "ratio of the total power of all extraneous frequencies in the voice-band above 500Hz accompanying the signal to the total power of the frequency pair".

Pin/Function Descriptions

Pin #	Name	Function
1	V_{DD}	The positive supply voltage pin.
2	$\overline{MUTE}$	This is an open drain output that turns on, to mute the microphone and speaker when a key is pressed.
3	$\overline{C1}$	When pin 10 is high these are the 4 column inputs and must be pulled low true. When pin 10 is low, a low on $\overline{C1}$ provides a single low group tone when CE is valid. If $\overline{C2}$ is low a single high group tone will be generated. Pull-up resistors are present on each pin in the 30KΩ range. These are not latching inputs like the row inputs. These pins ($\overline{C_1}$ $\overline{C_2}$) must be held low for the duration of the single tone.
4	$\overline{C2}$	
5	$\overline{C3}$	
9	$\overline{C4}$	
6	V_{SS}	The negative supply voltage pin.
7	OSC_i	A standard 3.58 MHz TV crystal is connected across these pins. There is an internal resistor.
8	OSC_o	
10	KEY/$\overline{BIN}$	Keyboard/$\overline{Binary}$: This pin selects whether the S2579 will be interfaced with a X-Y keyboard or 4 bit data bus from a microprocessor.
11	D_0 ($\overline{R_4}$)	When pin 10 is high these are the 4 row inputs and must be pulled low true. When pin 10 is low these are the binary data inputs for the 16 DTMF tones (See table 1). Pull-up resistors are on each pin in the 30KΩ range. The data is latched into the S2579 on the rising edge of CE.
12	D_1 ($\overline{R_3}$)	
13	D_2 ($\overline{R_2}$)	
14	D_3 ($\overline{R_1}$)	
15	CE	CHIP ENABLE: When this pin is low, all outputs are disabled. When CE and KEY/$\overline{BIN}$ are high, any single key depression will output a valid DTMF tone. If KEY/$\overline{BIN}$ is low, each time CE is brought high a tone will be output, the value will depend on the levels present at the D_0, D_1, D_2, D_3, $\overline{C_1}$, and $\overline{C_2}$ input pins during the positive transition of CE. The tone will continue until CE is brought low. (In the case of single tones $\overline{C_1}$ or $\overline{C_2}$ must be kept low for the duration of the tone).
16	TONE	TONE OUT. This output is an emitter follower DC coupled for impedance transformation. Typically drives a 100Ω or 150Ω resistor.

Functional Description

Basic Chip Operation

The dual tone multifrequency (DTMF) signal consists of linear addition of two voice frequency signals. One of four signals is selected from a group of frequencies called "low group" and the other is selected from a group of frequencies called "high group". The low group consists of four frequencies; 697, 770, 852 and 941Hz. The high group consists of four frequencies; 1209, 1336, 1477 and 1633Hz.

Tone Generation

When a valid address is detected, the S2579 programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divide by 16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function (see Figure 2). This is done by connecting a weighted resistor ladder network between the outputs of the Johnson counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude V_P ($V_{DD} - V_{REF}$) of the stair-step function is fairly constant. V_{REF} is so chosen that V_P falls within the allowed range of the high group and low group tones (see Table 3).

The individual tones generated by the sinewave synthesizer are then linearly added and drive an emitter follower to allow proper impedance transformation while preserving signal level.

Logic Interface

The S2579 will directly interface with TTL and CMOS logic outputs. When programmed for logic inputs, the S2579 requires active "high" logic levels. Pull-up resistors are present on the row and column inputs in the 30KΩ range.

Keyboard Interface

The S2579 can interface with either the standard telephone pushbutton keyboard (see Figure 1) or an X-Y keyboard with common. The common of the keyboard must be connected to V_{SS}.

When programmed for keyboard interface, the S2579 requires active "low inputs".

Single Tone Mode

Single tones in either the low group frequencies or the high group frequencies can be generated using the S2579. With pin 10 low, (Binary input) and valid data on the row inputs, a low input on the $\overline{C_1}$ or $\overline{C_2}$ pin will generate the appropriate single row or column frequency tone (Table 3). When pin 10 is high, a low group tone can be generated by depressing two digit keys in the appropriate column, i.e., selecting the appropriate column input and two row inputs in that column.

Key/$\overline{BIN}$

This input is used for programming the S2579 to accept either logic or keyboard inputs. If the Key/$\overline{BIN}$ pin is tied "low", the S2579 will be programmed to accept logic or binary input levels. Left floating or tied "high" the S2579 will accept keyboard inputs.

$\overline{MUTE}$ Output

The S2579 has a N-Channel transistor for the $\overline{MUTE}$ output. With no keys depressed, the $\overline{MUTE}$ output is open. When a valid address is enabled, the $\overline{MUTE}$ output goes low.

Oscillator

The device contains an oscillator circuit with the required parasitic capacitances and feedback resistance on chip so that it is only necessary to connect a standard 3.58MHzz TV crystal across the OSC_i and OSC_o terminals to implement the oscillator function.

Figure 1. Standard Telephone Push Button Keyboard

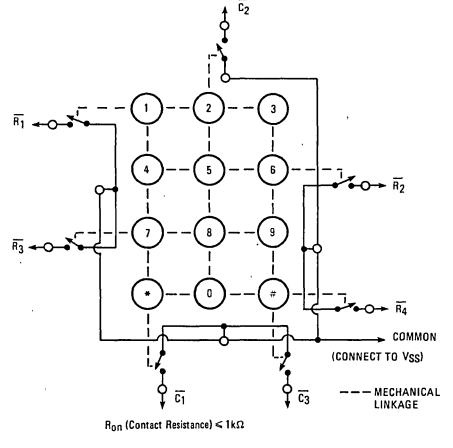


Table 1. Functional Truth Table for Logic Interface

Keyboard Inputs	$\overline{C1}$	$\overline{C2}$	Binary Inputs D3	D2	D1	D0	Frequencies Generated F_L	F_H
1	*	*	0	0	0	1	697	1209
2	*	*	0	0	1	0	697	1336
3	*	*	0	0	1	1	697	1477
4	*	*	0	1	0	0	770	1209
5	*	*	0	1	0	1	770	1336
6	*	*	0	1	1	0	770	1477
7	*	*	0	1	1	1	852	1209
8	*	*	1	0	0	0	852	1336
9	*	*	1	0	0	1	852	1477
0	*	*	1	0	1	0	941	1336
*	*	*	1	0	1	1	941	1209
#	*	*	1	1	0	0	941	1477
A	*	*	1	1	0	1	697	1633
B	*	*	1	1	1	0	770	1633
C	*	*	1	1	1	1	852	1633
D	*	*	0	0	0	0	941	1633
SINGLE TONE	0	*	VALID DATA					F_H
SINGLE TONE	*	0	VALID DATA				F_L	

* Indicates Normally Open, Internal Pullups Make This a "1" State.

Table 2. Functional Truth Table for Keyboard Interface

Inputs					Output
Keys Depressed	Number of Columns Low	Number of Rows Low	Chip Enable	Tone	$\overline{MUTE}$
X	X	X	0	0	1(OPEN)
None	0	0	1	0	1(OPEN)
One	1	1	1	$F_L + F_H$	0
Two or more keys in column	1	2 or 3 or 4	1	F_H	0
Two or more keys in row	2 or 3 or 4	1	1	F_L	0

Table 3. Comparisons of Specified Vs. Actual Tone Frequencies Generated by S2579

ACTIVE INPUT	OUTPUT FREQUENCY Hz SPECIFIED	ACTUAL	%ERROR SEE NOTE
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.9	+0.57
C2	1336	1331.7	−0.32
C3	1477	1471.9	−0.35
C4	1633	1645.0	+0.73

NOTE: %ERROR DOES NOT INCLUDE OSCILLATOR DRIFT

The oscillator functions whenever a row input is activated. The reference frequency is divided by 2 and then drives two sets of programmable dividers, the high group and the low group.

Chip Enable

The S2579 has a chip enable input at pin 15. The chip enable for the S2579 is active "High". When the chip enable is "Low", the tone output goes to V_{SS}, the oscillator is inhibited and the $\overline{MUTE}$ output goes open.

Quartz Crystal Specification (25° C ± 2°C)

Operating Temperature Range: 0°C to +70°C	
Frequency	3.579545MHz
Frequency Calibration Tolerance	02 ± %
Load Capacitance	18pF
Effective Series Resistance	180 Ohms, max.
Drive Level-Correlation/Operating	2mW
Shunt Capacitance	7pF, max.
Oscillation Mode	Fundamental

Figure 2. Stairstep Waveform of the Digitally Synthesized Sinewave

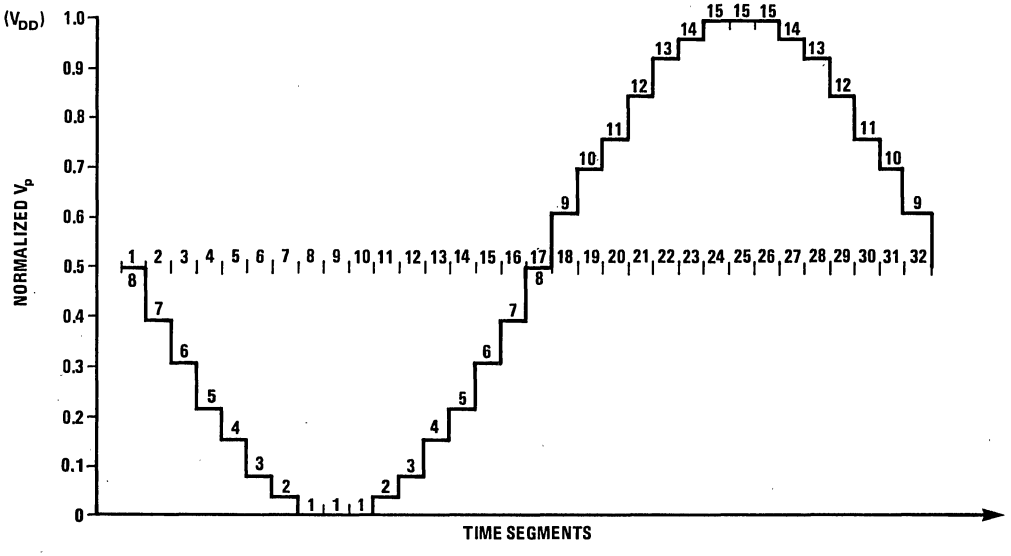
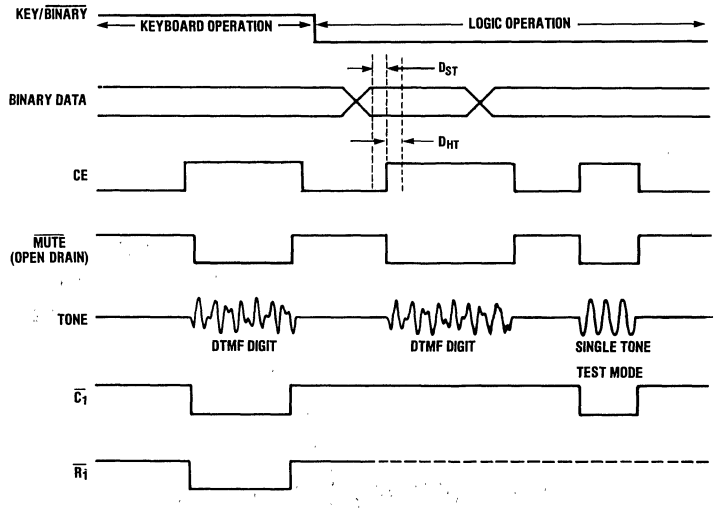


FIGURE 6. STAIRSTEP WAVEFORM OF THE DIGITALLY SYNTHESIZED SINEWAVE

Figure 3. S2579 Timing Diagram



Amplitude/Distortion Measurements

Amplitude and distortion are two important parameters in all applications of the digital tone generator. Amplitude depends upon the operating supply voltage as well as the load resistance connected on the tone output pin. The on-chip reference circuit is fully operational when the supply voltage equals or exceeds 4 volts and as a consequence the tone amplitude is regulated in the supply voltage range above 4 volts. The load resistor value also controls the amplitude. If R_L is low, the reflected impedance into the base of the output transistor is low and the tone output amplitude is lower. For R_L greater than 1KΩ the reflected impedance is sufficiently large and highest amplitude is produced. Individual tone amplitudes can be measured by applying the dual tone signal to a wave analyzer (H-P type 3580A) and amplitudes at the selected frequencies can be noted. This measurement also permits verification of the pre-emphasis between the individual frequency tones.

Distortion is defined as "the ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the power of the frequency pair". This ratio must be less than 10% or when expressed in dB must be lower than −20dB. (Ref. 1.) Voiceband is conventionally the frequency band of 300Hz to 3400Hz. Mathematically distortion can be expressed as:

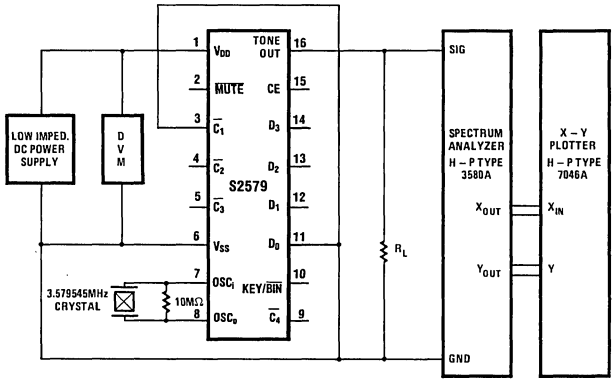
$$\text{Dist.} = \frac{\sqrt{(V_1)^2 + (V_2)^2 + \ldots + (V_N)^2}}{\sqrt{(V_L)^2 + (V_H)^2}}$$

where $(V_1) \ldots (V_N)$ are extraneous frequency (i.e., intermodulation and harmonic) components in the 500 Hz to 3400Hz band and V_L and V_H are the individual frequency components of the DTMF signal. The expression can be expressed in dB as:

$$\text{DIST}_{dB} = 20 \log \frac{\sqrt{(V_1)^2 + (V_2)^2 + \ldots + (V_N)^2}}{\sqrt{(V_L)^2 + (V_H)^2}}$$

$$= 10\{\log [(V_1{}^2 + \ldots (V_N)^2] - \log [(V_L)^2 + (V_H)^2]\} \ldots (1)$$

Figure 4. Test Circuit for Distortion Measurement



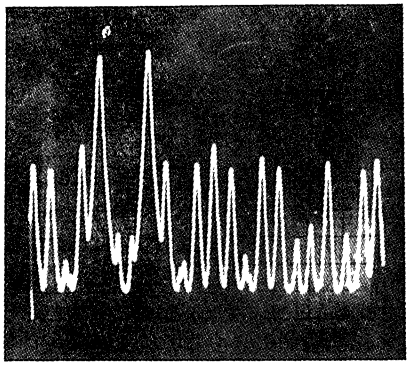
An accurate way of measuring distortion is to plot a spectrum of the signal by using a spectrum analyzer (H-P type 3580A) and an X-Y plotter (H-P type 7046A). Individual extraneous and signal frequency components are then noted and distortion is calculated by using the expression (1) above. Figure 5 shows a spectrum plot of a typical signal obtained from S2579 device operating from a fixed supply of $5V_{DC}$ and $R_L = 390\Omega$ in the test circuit of Figure 4. Mathematical analysis of the spectrum shows distortion to be -30dB (3.2%). For quick estimate of distortion, a rule of thumb as outlined below can be used.

"As a first approximation distortion in dB equals the difference between the amplitude (dB) of the extraneous component that has the highest amplitude and the amplitude (dB) of the low frequency signal." This rule of thumb would give an estimate of -28dB as distortion for the spectrum plot of Figure 5 which is close to the computed result of -30dB.

In a telephone application amplitude and distortion are affected by several factors that are interdependent. For detailed discussion of the telephone application and other applications of the S2579 Tone Generator, refer to the applications note "Applications of Digital Tone Generator."

Ref. 1: Bell System Communications Technical Reference, PUB 47001, **"Electrical Characteristics of Bell System Network Facilities at the Interface with Voiceband Ancillary and Data Equipment,"** August 1976.

Figure 5. A Typical Spectrum Plot



DEVICE: S2579 $R_L = 390\Omega$
TEMP: ROOM TEST CKT: FIGURE 4
$(V_{DD} - V_{SS})$: 5V DC FIXED DUAL TONE: R_4, C_1
HORIZONTAL SCALE = 0.5KHz/DIV
VERTICAL SCALE = 10dB/DIV

GOULD

AMI Semiconductors

Digital Time/Space Crosspoint Switch

Advanced Product Description

S8980

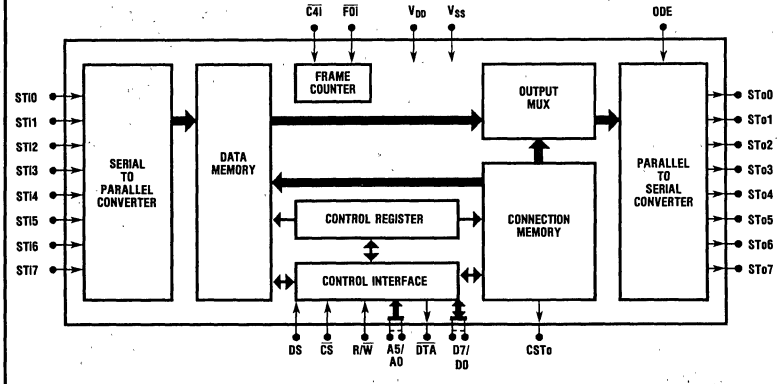
Features

- ST-BUS™ (Serial Telecom Bus) Compatible
- 8-Line x 32-Channel Inputs
- 8-Line x 32-Channel Outputs
- 256 Ports Non-Blocking Switch
- Single Power (+5 V)
- Low Power Consumption: 150 mW Typ
- Microprocessor-Control Interface
- Three-state Serial Outputs

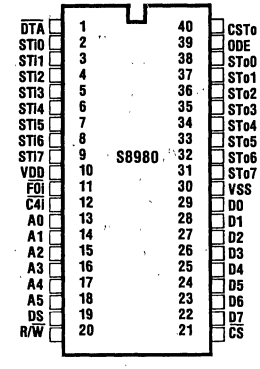
General Description

This VLSI ISO-CMOS device is designed for switching PCM-encoded voice or data, under microprocessor control, in a modern digital exchange, PBX or Central Office. It provides simultaneous connections for up to 256 64 kbit/sec channels. Each of the eight serial inputs and outputs consist of 32 64 kbits/sec channels multiplexed to form a 2048 kbit/sec Serial Data Stream.

Functional Block Diagram



Pin Configuration



Absolute Maximum Ratings†

Supply Voltage $V_{DD} - V_{SS}$	+7V
Voltage on Digital Inputs (V_I)	+0.3V
Current at Digital Inputs	40mA
Voltage on Digital Outputs (V_O)	V_{DD} +0.3V
Current at Digital Outputs	40mA
Storage Temperature	−55°C to +150°C
Power Dissipation	2W

†Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions: Voltages are with respect to ground (V_{SS}), unless otherwise stated.

Symbol	Parameter	Min.	Typ.‡	Max.	Units
T_{OP}	Operating Temperature	0		70	°C
V_{DD}	Positive Supply	4.75	5.0	5.25	V
V_I	Input Voltage	0		V_{DD}	V

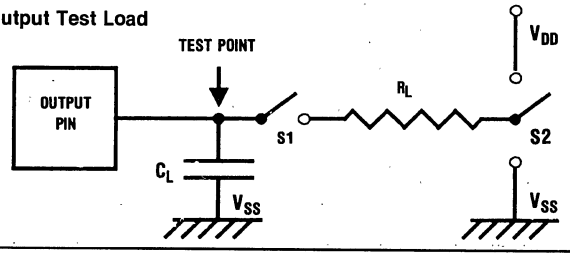
‡Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

DC Electrical Characteristics: Clocked operation over recommended temperature and voltage ranges.

Symbol	Parameter	Conditions	Min.	Typ.‡	Max.	Units
I_{DD}	Supply Current	Outputs Unloaded		30	50	mA
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage			0.8	V	
I_{IL}	Input Leakage	V_I between V_{SS} and V_{DD}			10	μA
V_{OH}	Output High Voltage	I_{OH}=10 mA	2.4			V
I_{OH}	Output High Current	Source Current V_{OH}=2.4 V	10	15		mA
		Source Current V_{OH}=3.0 V	8	12		mA
V_{OL}	Output Low Voltage	I_{OL}=5 mA			0.4	V
I_{OL}	Output Low Current	Sink Current V_{OL}=0.4 V	5	7.5		mA
		Sink Current V_{OL}=2.0 V	20	30		mA
I_{OZ}	High Impedance Leakage	V_{OS} between V_{SS} and V_{DD}			10	μA

‡Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Figure 2. Output Test Load



S1 is open circuit except when testing output levels or high impedance states.

S2 is switched to V_{DD} or V_{SS} when testing output levels or high impedance states.

AC Electrical Characteristics:

Capacitances

Symbol	Parameter	Min.	Typ.‡	Max.	Units
C_I	Input Pin Capacitance		8		pF
C_O	Output Pin Capacitance		8		pF

Clock Timing (Figures 3 and 4)

Symbol	Parameters	Min.	Typ.‡	Max.	Units
t_{CLK}	Clock Period*	200	244	300	ns
t_{CHL}	Clock Width High or Low	100	122	150	ns
t_{CTT}	Clock Transition Time		20		ns
t_{FPS}	Frame Pulse Set up Time	50			ns
t_{FPH}	Frame Pulse Hold Time	50			ns
t_{FPW}	Frame Pulse Width		244		ns

*Contents of Connection Memory are not lost if the clock stops.
NOTE: Frame pulse is repeated every 125 μs in synchronization with the clock.
†Timing is over recommended temperature and voltage ranges.
‡Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Figure 3. Frame Alignment

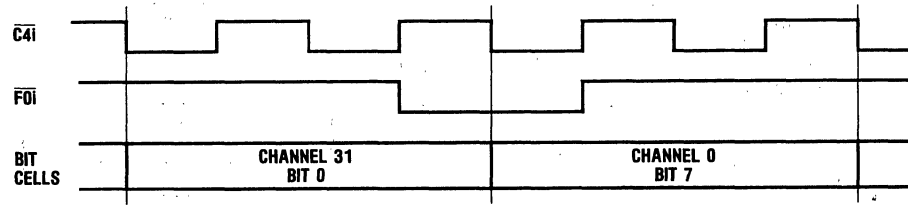
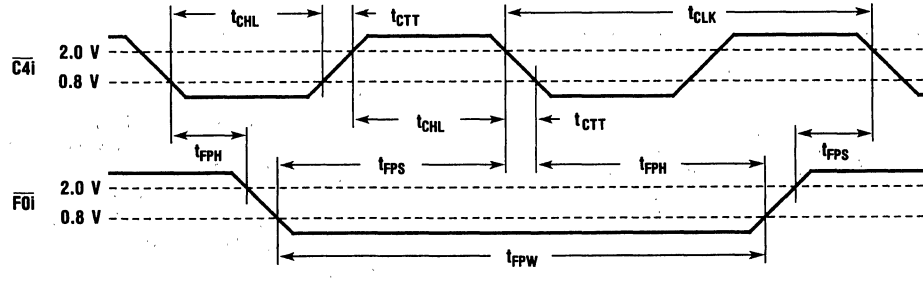


Figure 4. Clock Timing



Serial Streams (Figures 2, 5, 6, and 7)

Symbol	Parameter	Conditions	Min.	Typ.‡	Max.	Units
t_{SAZ}	STo0/7 Delay - Active to High Z	$R_L = 1\ k\Omega^*$, $C_L = 40$ pF			80	ns
t_{SZA}	STo0/7 Delay - High Z to active	$R_L = 1\ k\Omega^*$, $C_L = 40$ pF			100	ns
		$R_L = 1\ k\Omega^*$, $C_L = 200$ pF			125	ns
t_{SAA}	STo0/7 Delay - Active to Active	$C_L = 40$ pF			100	ns
		$C_L = 200$ pF			125	ns
t_{SOH}	STo0/7 Hold Time	$C_L = 40$ pF	0			
		$C_L = 200$ pF	0			
t_{OED}	Output Driver Enable Delay	$R_L = 1\ k\Omega^*$, $C_L = 40$ pF			100	ns
		$R_L = 1\ k\Omega^*$, $C_L = 200$ pF			125	ns
t_{SID}	Serial Input Delay				20	ns
t_{SIH}	Serial Input Hold Time		90			ns
t_{XCH}	External Control Hold Time	$C_L = 50$ pF	0			ns
t_{XCD}	External Control Delay	$C_L = 50$ pF			75	ns

†Timing is over recommended temperature and voltage ranges.
‡Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
*High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

Figure 5. Serial Outputs and External Control

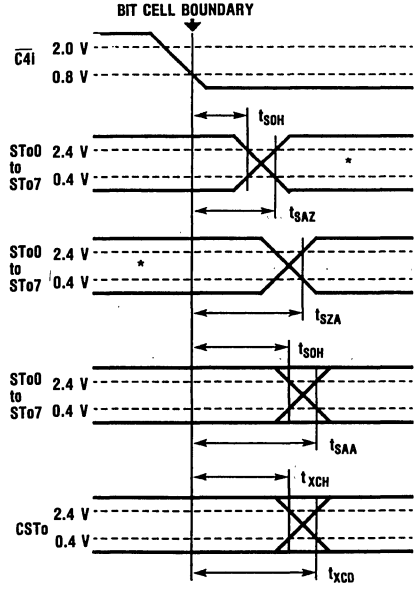


Figure 6. Output Driver Enable

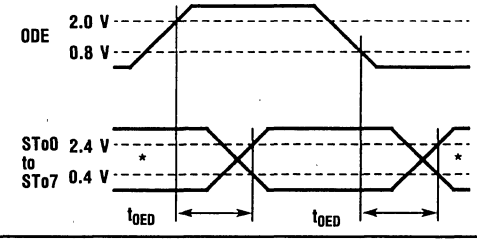
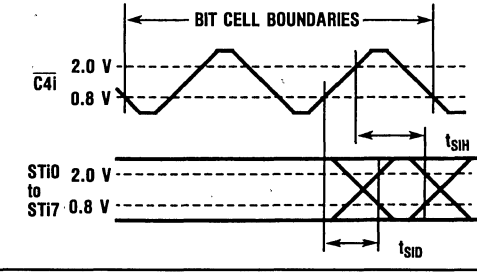


Figure 7. Serial Inputs

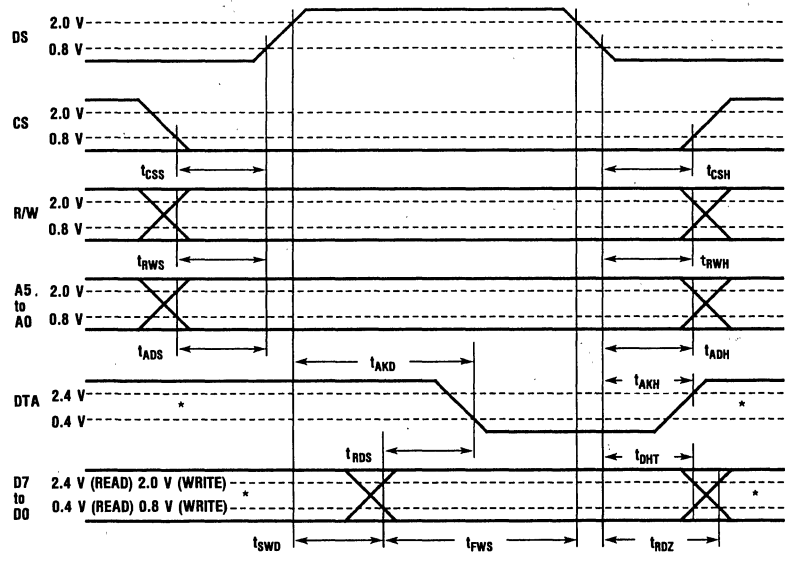


Processor Bus (Figures 2, and 8)

Symbol	Parameter		Conditions	Min.	Typ.‡	Max.	Units
t_{CSS}	Chip Select Set-up Time			20			ns
t_{RWS}	Read/Write Set-up Time			40			ns
t_{ADS}	Address Set-up Time			40			ns
t_{AKD}	Acknowledgement Delay	Fast	$R_L = 1\ k\Omega^*$, $C_L = 130$ pF		60	100	ns
		Slow	$R_L = 1\ k\Omega^*$, $C_L = 130$ pF		1.2	1.8	μs
t_{FWS}	Fast Write Data Set-up Time			30			ns
t_{SWD}	Slow Write Data Delay				250	ns	
t_{RDS}	Read Data Set-up Time		$R_L = 1\ k\Omega^*$, $C_L = 130$ pF	0			ns
t_{DHT}	Data Hold Time	Read	$R_L = 1\ k\Omega^*$, $C_L = 130$ pF	20			ns
		Write		20			ns
t_{RDZ}	Read Data to High Impedance		$R_L = 1\ k\Omega^*$, $C_L = 130$ pF		40	90	ns
t_{CSH}	Chip Select Hold Time			20			ns
t_{RWH}	Read/Write Hold Time			15			ns
tf_{ADH}	Address Hold Time			15			ns
t_{AKH}	Acknowledgement Hold Time		$R_L = 1\ k\Omega^*$, $C_L = 130$ pF	0	60	100	ns

†Timing is over recommended temperature and voltage ranges.
‡Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
*High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

Figure 8. Processor Bus



Pin Function Description

Pin Name	Number	Function
DTA	1	Data Acknowledgement (Open Drain Pulldown Output). This is the data acknowledgement on the microprocessor interface. This pin is pulled low to signal that the chip has processed the data.
STi0-STi7	2-9	ST-BUS™ Input 0 to 7 (Inputs). These are the inputs for the 2048 kbit/sec ST-BUS™ input streams.
V_{DD}	10	Power Input. Positive Supply.
F0i	11	Framing 0-Type (Input). This is the input for the frame synchronization pulse for the 2048 kbit/sec ST-BUS™ streams. A low on this input causes the internal counter to reset on the next negative transition of C4i.
C4i	12	4.096 MHz Clock (Input). ST-BUS™ bit cell boundaries lie on the alternate falling edges of this clock.
A0-A5	13-18	Address 0 to 5 (Inputs). These are the inputs for the address lines on the microprocessor interface.
DS	19	Data Strobe (Input). This is the input for the active high data strobe on the microprocessor interface.
R/W	20	Read or Write (Input). This is the input for the read/write signal on the microprocessor interface — high for read, low for write.
CS	21	Chip Select (Input). This is the input for the active low chip select on the microprocessor interface.
D7-D0	22-29	Data 7 to 0 (Three-state I/O Pins). These are the bidirectional data pins on the microprocessor interface.
V_{SS}	30	Power Input. Negative Supply (Ground).
STo7-STo0	31-38	ST-BUS™ Output 7 to 0 (Three-state Outputs). These are the pins for the eight 2048 kbit/sec ST-BUS™ output streams.
ODE	39	Output Drive Enable (Input). If this input is held high, the STo0-STo7 output drivers function normally. If this input is low, the STo0-STo7 output drivers go into their high impedance state. **NOTE:** Even when ODE is high, channels on the STo0-STo7 outputs can go high impedance under software control.
CSTo	40	Control ST-BUS™ Output (Complementary Output). Each frame of 256 bits on this ST-BUS™ output contains the values of bit 1 in the 256 locations of the Connection Memory High.

Figure 9. Address Memory Map

A5	A4	A3	A2	A1	A0	Hex Address	Location
0	X	X	X	X	X	00-1F	Control Register*
1	0	0	0	0	0	20	Channel 0†
1	0	0	0	0	1	21	Channel 1†
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
1	1	1	1	1	1	3F	Channel 31†

*Writing to the Control Register is the only fast transaction.
†Memory and stream are specified by the contents of the Control Register.

Functional Description

In recent years, there has been a trend in telephony towards digital switching, particularly in association with software control. Simultaneously, there has been a trend in system architectures towards distributed processing or multi-processor systems.

In accordance with these trends, Mitel has devised the ST-BUS™ (Serial Telecom Bus). This bus architecture can be used both in software-controlled digital voice and data switching, and for interprocessor communications. The uses in switching and in interprocessor communications are completely integrated to allow for a simple general purpose architecture appropriate for the systems of the future.

The serial streams of the ST-BUS™ operate continuously at 2048 kbit/sec and are arranged in 125 μs wide frames which contain 32 8-bit channels. Gould AMI manufactures a number of devices which interface to the ST-BUS™; a key device being the S8980 chip.

The S8980 can switch data from channels on ST-BUS™ inputs to channels on ST-BUS™ outputs, and simultaneously allows its controlling microprocessor to read channels on ST-BUS™ inputs or write to channels on ST-BUS™ outputs (Message Mode). To the microprocessor, the S8980 looks like a memory peripheral. The microprocessor can write to the S8980 to establish switched connections between input ST-BUS™ channels and output ST-BUS™ channels, or to transmit messages on the output ST-BUS™ channels. By reading from the S8980, the microprocessor can receive messages from ST-BUS™ input channels or check which switched connections have already been established.

By integrating both switching and interprocessor communications, the S8980 allows systems to use distributed processing and to switch voice or data in an ST-BUS™ architecture.

Hardware Description

Serial data at 2048 kbit/sec is received at the eight ST-BUS™ inputs (STi0 to STi7), and serial data is transmitted at the eight ST-BUS™ outputs (STo0 to STo7). Each serial input accepts 32 channels of digital data, each channel containing an 8-bit word which may represent a PCM-encoded analog/voice sample as provided by a codec (e.g. Gould AMI's S3507, S3507A, S3506, S44231-8).

This serial input word is converted into parallel data and stored in the 256x8 Data Memory. Locations in the Data Memory are associated with particular channels on particular ST-BUS™ input streams. These locations can be read by the microprocessor which controls the chip.

Locations in the Connection Memory, which is split into high and low parts, are associated with particular ST-BUS™ output streams. When a channel is due to be transmitted on an ST-BUS™ output, the data for the channel can either be switched from an ST-BUS™ input or it can originate from the microprocessor. If the data is switched from an input, then the contents of the Connection Memory Low location associated with the output channel is used to address the Data Memory. This Data Memory address corresponds to the channel on the input ST-BUS™ stream on which the data for switching arrived. If the data for the output channel originates from the microprocessor (Message Mode), then the contents of the Connection Memory Low location associated with the output channel are output directly, and this data is output repetitively on the channel once every frame until the microprocessor intervenes.

The Connection Memory data is received, via the Control Interface, at D7 to D0. The Control Interface also receives address information at A5 to A0 and handles the microprocesor control signals $\overline{CS}$, $\overline{DTA}$, R/$\overline{W}$ and DS. There are two parts to any address in the Data Memory or Connection Memory. The higher order bits come from the Control Register, which may be written to or read from via the Control Interface. The lower order bits come from th address lines directly.

The Control Register also allows the chip to broadcast messages on all ST-BUS™ outputs (i.e., to put every channel into Message Mode), or to split the memory so that reads are from the Data Memory and writes are to the Connection Memory Low. The Connection Memory High determines whether individual output channels are in Message Mode, and allows individual output channels to go into a high-impedance state, which enables arrays of S8980s to be constructed. It also controls the CSTo pin. All ST-BUS™ timing is derived from the two signals $\overline{C4i}$ and $\overline{F0i}$.

Software Control

The address lines on the Control Interface give access to the Control Register directly or, depending on the contents of the Control Register, to the High or Low sections of the Connection Memory or to the Data Memory.

If address line A5 is low, then the Control Register is addressed regardless of the other address lines (See Figure 9). If A5 is high, then the address lines A4-A0

select the memory location corresponding to channel 0-31 for the memory and stream selected in the Control Register.

The data in the Control Register consists of mode control bits, memory select bits, and stream address bits (see Figure 10). The memory select bits allow the Connection Memory High or Low or the Data Memory to be chosen, and the stream address bits define one of the ST-BUS™ input or output streams.

Figures 11a and 11b show the effect of the control register on subsequent operations.

Bit 7 of the Control Register allows split memory operation — reads are from the Data Memory and writes are to the Connection Memory Low.

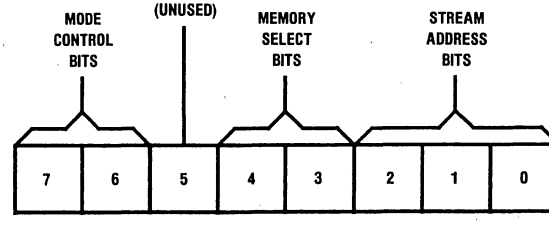
The other mode control bit, bit 6, puts every output channel on every output stream into active Message Mode, i.e., the contents of the Connection Memory Low are output on the ST-BUS™ output streams once every frame unless the ODE pin is low. In this mode the chip behaves as if bits 2 and 0 of every Connection Memory High location were 1, regardless of the actual values.

If bit 7 of the Control Register is 0, then bits 2 and 0 of each Connection Memory High location function normally (see Figure 12). If bit 2 is 1, the associated ST-BUS™ output channel is in Message Mode; i.e., the byte in the corresponding Connection Memory Low location is transmitted on the stream at that channel. Otherwise, one of the bytes received on the serial inputs is transmitted and the contents of the Connection Memory Low define the ST-BUS™ input stream and channel where the byte is to be found (see Figure 13.).

If the ODE pin is low, then all serial outputs are high-impedance. If it is high and bit 6 in the Control Register is 1, then all outputs are active. If the ODE pin is high and bit 6 in the Control Register is 0, then the bit 0 in the Connection Memory High location enables the output drivers for the corresponding individual ST-BUS™ output stream and channel — bit 0 = 1 enables the driver and bit 0 = 0 disables it (see Figure 12).

Bit 1 of each Connection Memory High location (see Figure 12) is output on the CSTo pin once every frame. To allow for delay in any external control circuitry the bit is output one channel before the corresponding channel on the ST-BUS™ streams, and the bit for stream 0 is output first in the channel; e.g., bit 1s for channel 9 of streams 0-7 are output synchronously with ST-BUS™ channel 8 bits 7-0.

Figure 10. Control Register Bits



Bit Name	Number	Function
Split Memory	7	When 1, on subsequent operations all reads are from the Data Memory and all writes are to the Connection Memory, except when the Control Register is accessed. When 0, the Memory Select Bits specify the memory for subsequent operations. In either case, the Stream Address Bits select the subsection of the memory which is made available.
Message Mode	6	When 1, the contents of the Connection Memory Low are output on the Serial Output streams except when the ODE pin is low. When 0, the Connection Memory bits for each channel determine what is output.
(unused)	5	
Memory Select Bits	4-3	0-0 — Reserved for testing 0-1 — Data Memory 1-0 — Connection Memory Low 1-1 — Connection Memory High
Stream Address Bits	2-0	The number expressed in binary notation on these bits refers to the input or output BUS™ stream which corresponds to the subsection of memory made accessible for subsequent operations.

Figure 11a Control Register: Memory and Mode to Contents

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2*	Bit 1*	Bit 0*	Hex Value*	Memory	Mode
0	0	X	0	1	X	X	X	08-0F & 28-2F	Data	Normal
0	1	0	1	X	X	X	X	48-4F & 68-6F		Message
0	0	X	1	0	X	X	X	10-17 & 30-37	Connection Low	Normal
0	1	X	1	0	X	X	X	50-57 & 70-77		Message
0	0	X	1	1	X	X	X	18-1F & 38-3F	Connection High	Normal
0	1	X	1	1	X	X	X	58-5F & 78-7F		
1	0	X	0 1 1	1 0 1	X	X	X	88-8F, A8-AF, 90-97, B0-B7, 98-9F & B8-BF	Split	Normal
1	1	X	0 1 1	1 0 1	X	X	X	C8-CF, E8-EF, D0-D7, F0-F7, D8-DF & F8-FF		Message

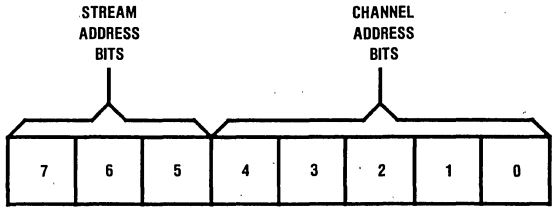
Figure 11b. Control Register: Contents to Memory and Mode

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit2*	Bit 1*	Bit 0*	Hex Value*	Memory	Mode
0	0	0	0	1	X	X	X	08-0F	Data	Normal
0	0	0	1	0	X	X	X	10-17	Connection Low	Normal
0	0	0	1	1	X	X	X	18-1F	Connection High	Normal
0	0	1	0	1	X	X	X	28-2F	Data	Normal
0	0	1	1	0	X	X	X	30-37	Connection Low	Normal
0	0	1	1	1	X	X	X	38-3F	Connection High	Normal
0	1	0	0	1	X	X	X	48-4F	Data	Message
0	1	0	1	0	X	X	X	50-57	Connection Low	Message
0	1	0	1	1	X	X	X	58-5F	Connection High	Message
0	1	1	0	1	X	X	X	68-6F	Data	Message
0	1	1	1	0	X	X	X	70-77	Connection Low	Message
0	1	1	1	1	X	X	X	78-7F	Connection High	Message
1	0	0	0	1	X	X	X	88-8F	Split	Normal
1	0	0	1	0	X	X	X	90-97	Split	Normal
1	0	0	1	1	X	X	X	98-9F	Split	Normal
1	0	1	0	1	X	X	X	A8-AF	Split	Normal
1	0	1	1	0	X	X	X	B0-B7	Split	Normal
1	0	1	1	1	X	X	X	B8-BF	Split	Normal
1	1	0	0	1	X	X	X	C8-CF	Split	Message
1	1	0	1	0	X	X	X	D0-D7	Split	Message
1	1	0	1	1	X	X	X	D8-DF	Split	Message
1	1	1	0	1	X	X	X	E8-EF	Split	Message
1	1	1	1	0	X	X	X	F0-F7	Split	Message
1	1	1	1	1	X	X	X	F8-FF	Split	Message

*The range of values for bits 0 to 2 corresponds to the ST-BUS™ streams 0 to 7.

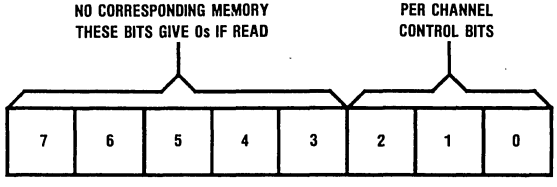
NOTE: All other combinations of values for the 8 bits are reserved for testing.

Figure 12. Connection Memory High Bits



Bit Name	Number	Function
Message Channel	2	When 1, the contents of the corresponding location in Connection Memory Low are output on the location's channel and stream. When 0, the contenst of the corresponding location in Connection Memory Low act as an address for the Data Memory and so determine the source of the connection to the location's channel and stream.
CSTo Bit	1	This bit is output on the CSTo pin one channel early. The CSTo bit for stream 0 is output first.
Output Enable	0	If the ODE pin is high and bit 6 of the Control Register is 0, then this bit enables the output driver for the location's channel and stream. This allows individual channels on individual streams to be made high-impedance, allowing switching matrices to be constructed. A 1 enables the driver and a 0 disables it.

Figure 13. Connection Memory Low Bits



Bit Name	Number	Function
Stream Address Bits*	7-5*	The number expressed in binary notation on these 3 bits is the number of the BUS™ stream for the source of the connection. Bit 7 is the most significant bit. E.G., if bit 7 is 1, bit 6 is 0 and bit 5 is 0, then the source of the connection is a channel on STi4.
Channel Address Bits*	4-0*	The number expressed in binary notation on these 5 bits is the number of the channel which is the source of the connection. (The BUS™ stream where the channel lies is defined by bits 6 and 5.) Bit 4 is the most significant bit. E.g., if bit 4 is 1, bit 3 is 0, bit 2 is 0, bit 1 is 1 and bit 0 is 1, then the source of the connection is channel 19.

*If bit 2 of the corresponding Connection High location is 1 or if bit 6 of the Control Register is 1, then these entire 8 bits are output on the channel and stream associated with this location. Otherwise the bits are used as indicated to define the source of the connection which is output on the channel and stream associated with this location.

Applications

Use in a Simple Digital Switching System

Figures 14 and 15 show how S8980s can be used with S8970 and S3507A to form a simple digital switching system. Figure 14 shows the interface between the S8980s and the filter/codecs. Figure 15 shows the position of these components in an example architecture.

The S3507A filter/codec and S8970 line interface in Figure 14 receives and transmits digitized voice signals on the ST-BUS™ input D_R, and the ST-BUS™ output D_X, respectively. These signals are routed to the ST-BUS™ inputs and outputs on the top S8980, which is used as a digital speech switch.

The S8970 and S3507A are controlled by the ST-BUS™ input D_C originating from the bottom S8980, which generates the appropriate signals from an output channel in Message Mode. This architecture optimizes the messaging capability of the line circuit by building signaling logic, e.g., for on-off hook detection, which communicates on an ST-BUS™ output. This signaling ST-BUS™ output is monitored by a microprocessor (not shown) through an ST-BUS™ input on the bottom S8980.

Figure 15 shows how a simple digital switching system may be designed using the ST-BUS™ architecture. This is a private telephone network with 256 extensions which uses a single S8980 as a speech switch and a second S8980 for communication with the line interface circuits.

Figure 14. Example of Typical Interface between S8980s, S8970, and S3507A for Simple Digital Switching System

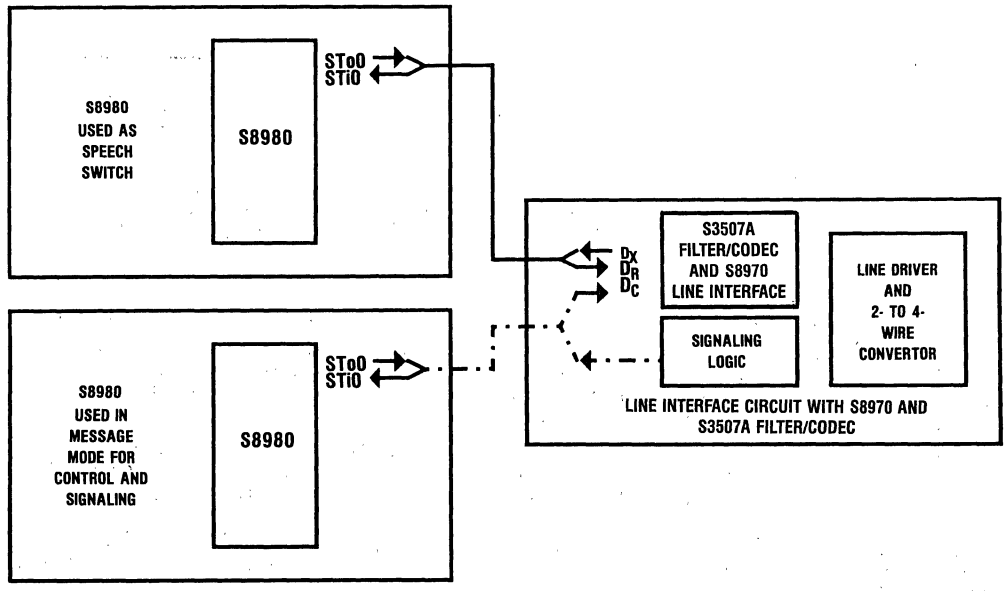
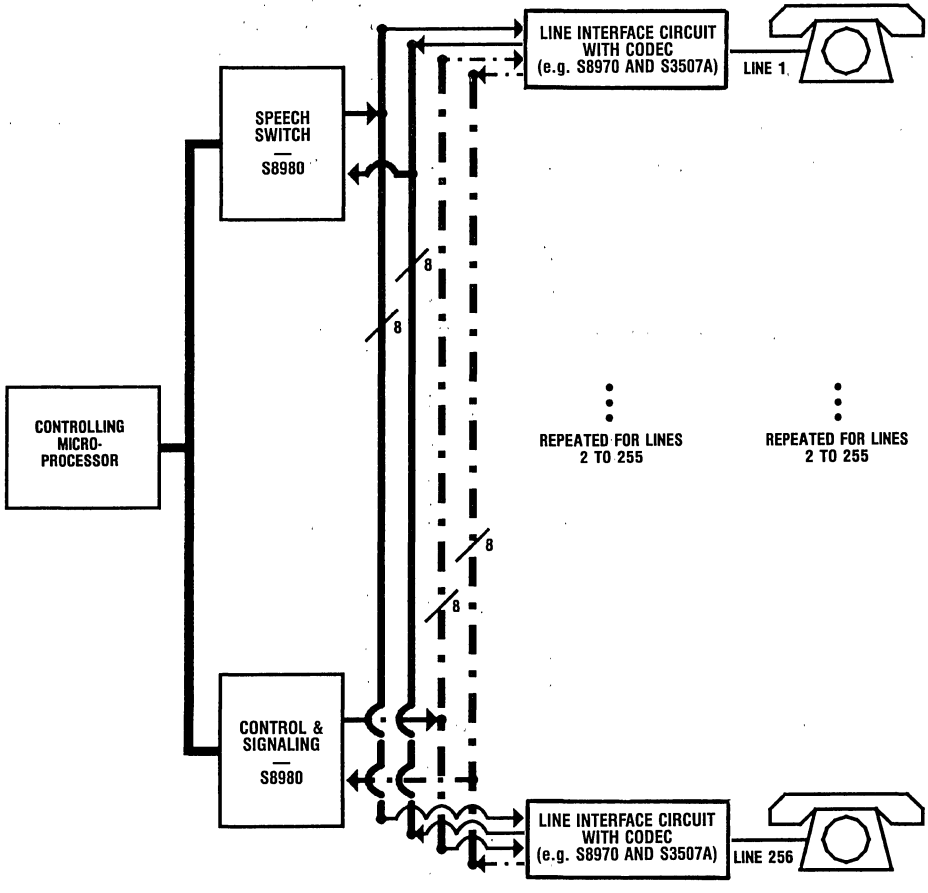


Figure 15. Example Architecture of a Simple Digital Switching System



A larger digital switching system may be designed by cascading a number of S8980s. Figure 16 shows how four S8980s may be arranged in a non-blocking configuration which can switch any channel on any of the ST-BUS™ inputs to any channel on the ST-BUS™ outputs.

Application Circuit with 6802 Processor

Figure 17 shows an example of a complete circuit which may be used to evaluate the chip.

For convenience, a 4 MHz crystal oscillator has been used rather than a 4.096 MHz clock, as both are within the limits of the chip's specifications. The RC delay used with the 393 counters ensures a sufficient hold time for the FP signal, but the values used may have to be changed if faster 393 counters become available.

The chip is shown as memory mapped into the S6802 system. Chip addresses 00-3F correspond to processor addresses 2000-203F. Delay through the address decoder requires the VMA signal to be used twice to remove glitches. The S6802 board uses a 10KΩ pullup on the MR pin, which would have to be incorporated into the circuit if the board was replaced by a processor.

Figure 16. Four S8980s Arranged in a Non-Blocking 16 × 16 Configuration

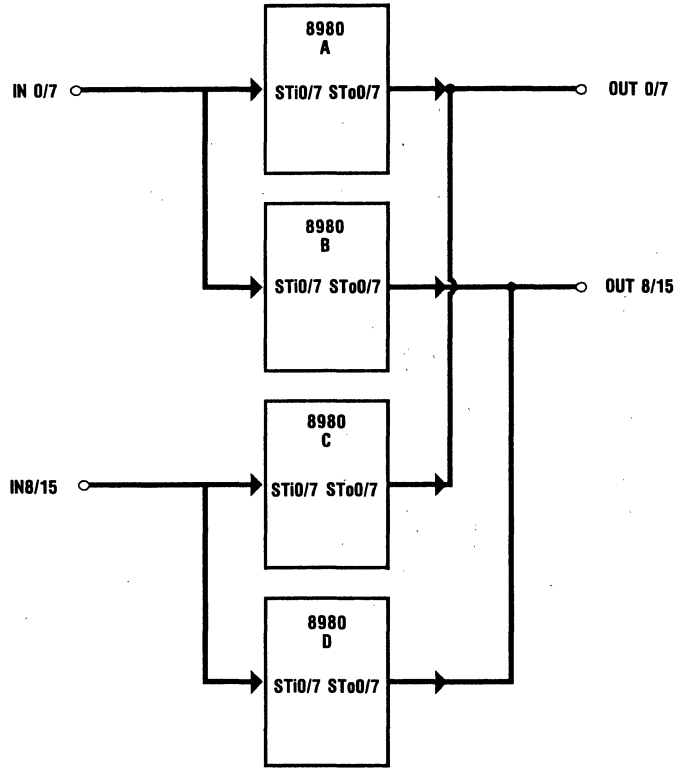
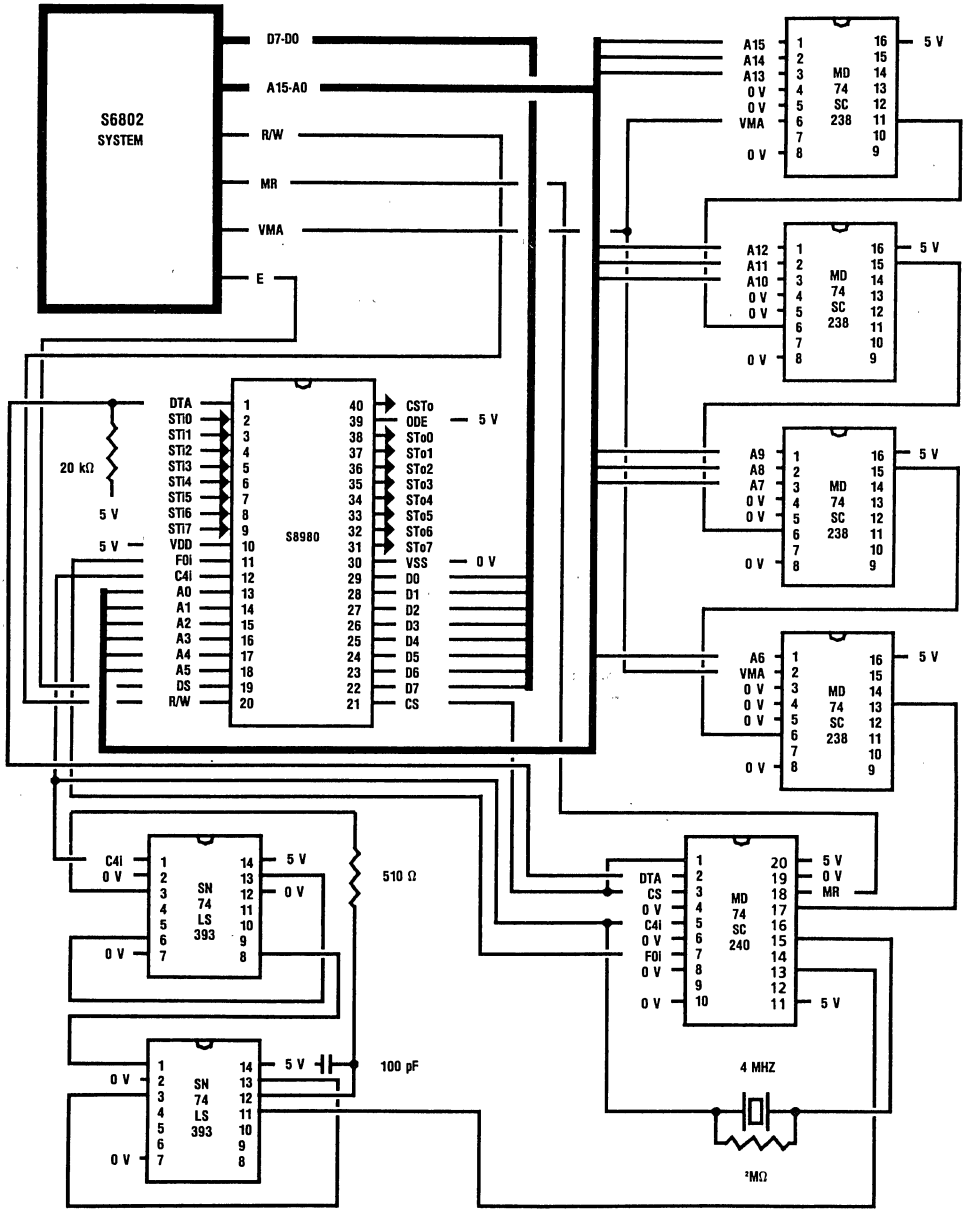


Figure 17. Application Circuit with 6802



GOULD

AMI Semiconductors

Digital Time/Space Crosspoint Switch

Preliminary Data Sheet

S8981

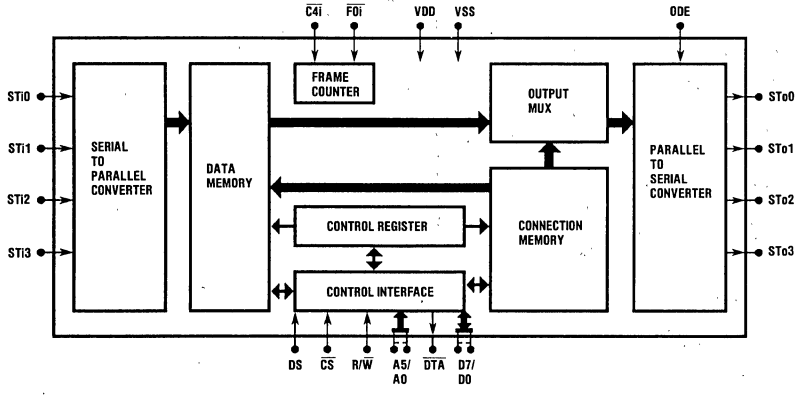
Features

- ☐ ST-BUS™ compatible
- ☐ 4-Line x 32-Channel Inputs
- ☐ 4-Line x 32-Channel Outputs
- ☐ 128 Ports Non-Blocking Switch
- ☐ Single Power Supply (+5V)
- ☐ Low Power Consumption: 150 mW Typ
- ☐ Microprocessor-Control Interface
- ☐ Three-state Serial Outputs

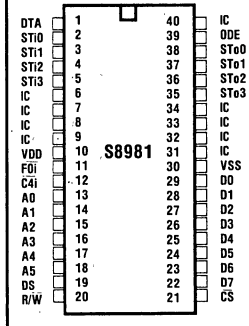
General Description

This VLSI ISO-CMOS device is designed for switching PCM-encoded voice or data, under microprocessor control, in a modern digital exchange, PBX or Central Office. It provides simultaneous connections for up to 128 64 kbit/s channels. Each of the four serial inputs and outputs consist of 32 64 kbit/s channels multiplexed to form a 2048 kbit/s ST-BUS™ stream.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply Voltage	−0.3	7	V
V_I	Voltage at Digital Inputs	V_{SS} −0.3	V_{DD} + 0.3	V
I_I	Current at Digital Inputs		40	mA
V_O	Voltage on Digital Outputs	V_{SS} −0.3	V_{DD} + 0.3	V
I_O	Current at Digital Outputs		40	mA
T_{ST}	Storage Temperature	−65	150	°C
P	Power Dissipation		2	W

Note: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions—Voltages are with respect to ground (V_{SS}) unless otherwise stated.

Symbol	Characteristics	Min.	Typ.	Max.	Units	Test Conditions
T_{OP}	Operating Temperature	0		70	°C	
V_{DD}	Positive Supply	4.75	5.0	5.25	V	
V_I	Input Voltage	0		V_{DD}	V	

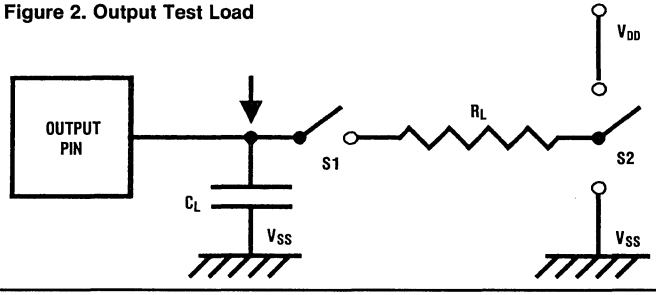
Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

DC Electrical Characteristics—Clocked operation over recommended temperature and voltage ranges.

Symbol	Characteristics	Min.	Typ.	Max.	Units	Test Conditions
I_{DD}	Supply Current		30	50	mA	Outputs unloaded
V_{IH}	Input High Voltage	2.0			V	
V_{IL}	Input Low Voltage			0.8	V	
I_{IL}	Input Leakage			10	μA	V_I between V_{SS} and V_{DD}
V_{OH}	Output High Voltage	2.4			V	I_{OH} = mA
I_{OH}	Output High Current	10	15		mA	Source Current. V_{OH} = 2.4V
		8	12		mA	Source Current. V_{OH} = 3.0V
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 5mA
I_{OL}	Output Low Current	5	7.5		mA	Sink current. V_{OL} = 0.4V
		20	30		mA	Sink Current. V_{OL} = 2.0V
I_{OZ}	High Impedance Leakage			10	μA	V_O between V_{SS} and V_{DD}

Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Figure 2. Output Test Load



S1 is open circuit except when testing output levels or high impedance states.
S2 is switched to V_{DD} or V_{SS} when testing output levels or high impedance states.

AC Electrical Characteristics—Capacitances

Symbol	Characteristics	Min.	Typ.	Max.	Units	Test Conditions
C_I	Input Pin Capacitance		8		pF	
C_O	Output Pin Capacitance		8		pF	

AC Electrical Characteristics—Clock timing (Figure 3 and 4).

Symbol	Characteristics	Min.	Typ-	Max.	Units	Test Conditions
t_{CLK}	Clock Period*	200	244	300	ns	
t_{CHL}	Clock Width High or Low	100	122	150	ns	
t_{CTT}	Clock Transition Time		20		ns	
t_{FPS}	Frame Pulse Set Up Time	50			ns	
t_{FPH}	Frame Pulse Set Up Time	50			ns	
t_{FPW}	Frame Pulse Width		244	ns		

Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
* Contents of Connection Memory are not lost if the clock stops.
Frame pulse is repeated every 125 ms in synchronisation with the clock.
Timing is over recommended temperature and voltage ranges.

Figure 3. Frame Alignment

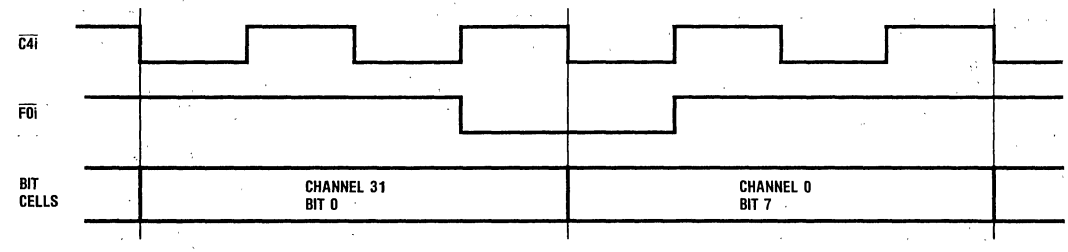
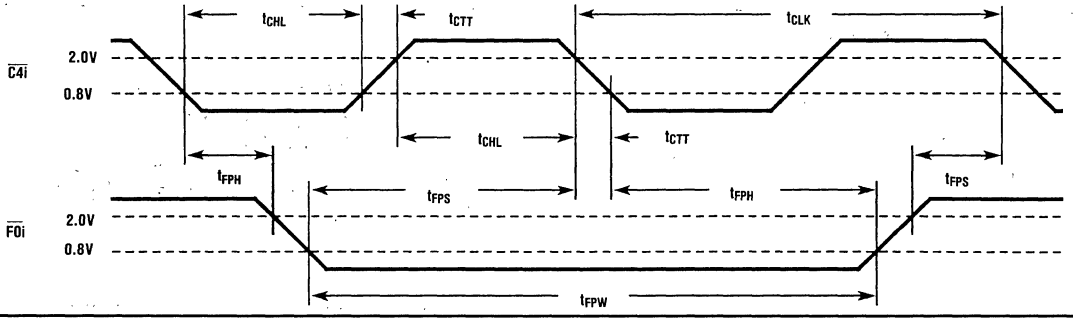


Figure 4. Clock Timing



AC Electrical Characteristics—Serial streams (Figure 2, 5, 6 and 7).

Symbol	Characteristics	Min.	Typ.	Max.	Units	Test Conditions
t_{SAZ}	STo0/3 Delay—Active to High Z			80	ns	$R_L = 1k\Omega^*$, $C_L = 40$ pF
t_{SZA}	STo0/3 Delay—High Z to Active			100	ns	$R_L = 1k\Omega^*$, $C_L = 40$pF
				125	ns	$R_L = 1k\Omega^*$, $C_L = 200$ pF
t_{SAA}	STo0/3 Delay—Active to Active			100	ns	$C_L = 40$ pF
				125	ns	$C_L = 200$ pF
t_{SOH}	STo0/3 Hold Time	0				$C_L = 40$ pF
		0				$C_{LD} = 200$ pF
t_{OED}	Output Driver Enable Delay			100	ns	$R_L = 1k\Omega^*$, $C_L = 40$pF
				125	ns	$R_L = 1k\Omega^*$, $C_L = 200$ pF
t_{SID}	Serial Input Delay			20	ns	
t_{SIH}	Serial Input Hold Time	90			ns	

Note: Timing is over recommended temperature and voltage ranges.
Note 2: Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
*High impedance is measured by pulling to the appropriate rail with C_L, with timing corrected to cancel time taken to discharge C_L.

Figure 5. Serial Outputs

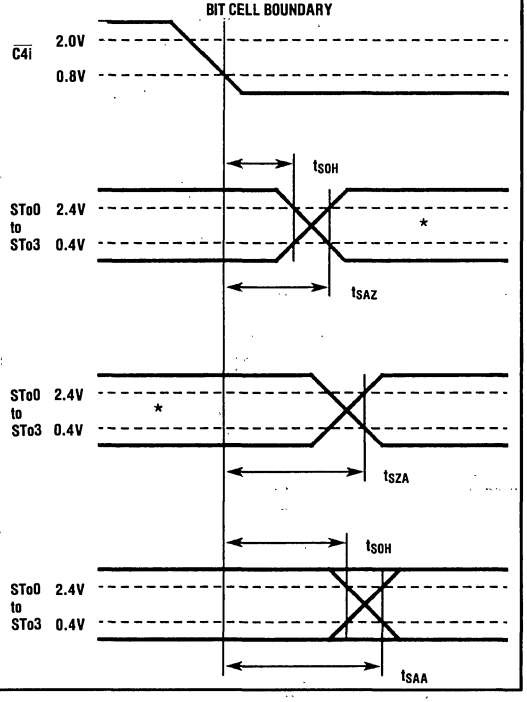
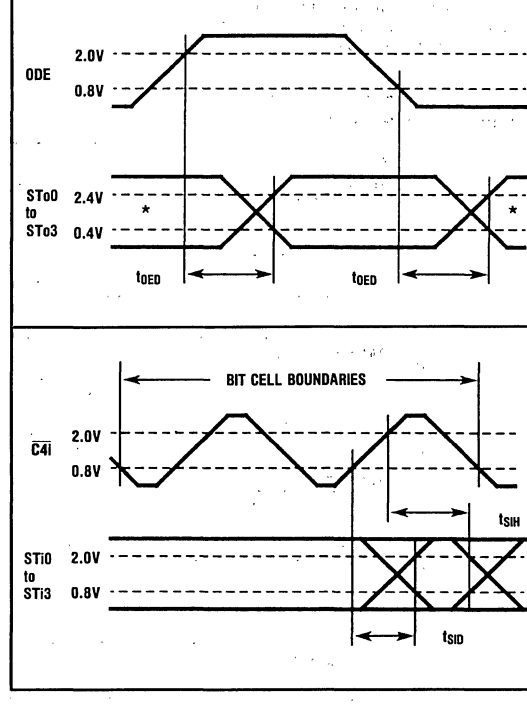


Figure 6. Output Driver Enable

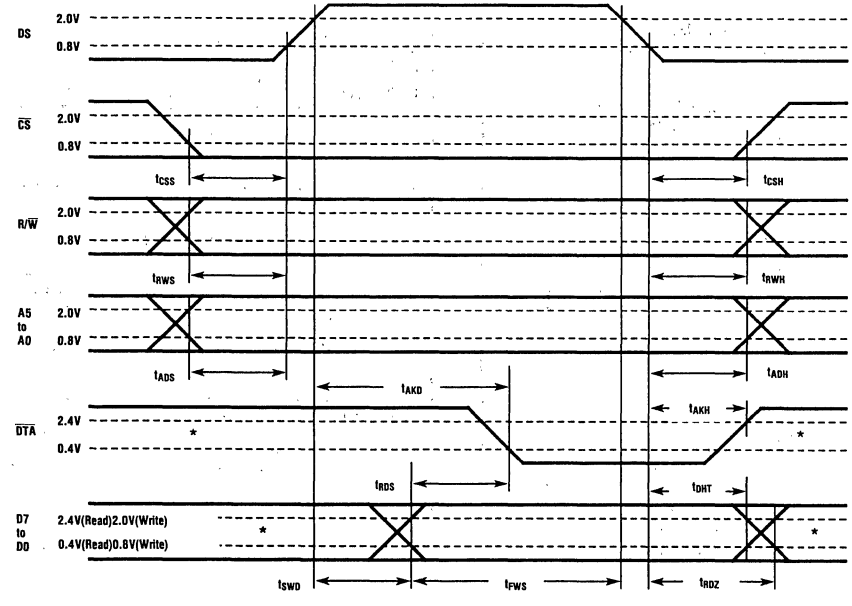


AC Electrical Characteristics[1]—Processor Bus (Figure 2 and 8)

Symbol	Characteristics		Min.	Typ.	Max.	Units	Test Conditions
t_{CSS}	Chip Select Set-Up Time		20			ns	
t_{RWS}	Read/Write Set-Up time		40			ns	
t_{ADS}	Address Set Up Time		40			ns	
t_{AKD}	Acknowledgement Delay	Fast		60	100	ns	$R_L = 1k\Omega^*, C_L = 130$ pF
		Slow		1.2	1.8	µs	$R_L = 1k\Omega^*, C_L = 130$ pF
t_{FWS}	Fast Write Data Set-Up Time		30			ns	
t_{SWD}	Slow Write Data Delay				250	ns	
t_{RDS}	Read Data Set Up Time		0			ns	$R_L = 1k\Omega^*$, $C_L = 130$ pF
t_{DHT}	Data Hold Time	Read	20			ns	$R_L = 1k\Omega^*, C_L = 130$ pF
		Write	20			ns	
t_{RDZ}	Read Data to High Impedance			40	90	ns	$R_L = 1k\Omega^*$, $C_L = 130$ pF
t_{CSH}	Chip Select Hold Time		20			ns	
t_{RWH}	Read/Write Hold Time		15			ns	
t_{ADH}	Address Hold Time		15			ns	
t_{AKH}	Acknowledgement Hold Time		0	60	100	ns	$R_L = 1k\Omega^*$, $C_L = 130$ pF

Note 1: Timing is over recommended temperature and voltage ranges.
Note 2: Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* High impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

Figure 8. Processor Bus



Pin Description

Pin	Label	Description
1	$\overline{DTA}$	**Data Acknowledgement (Open Drain Pulldown Output)**—This is the data acknowledgement on the microprocessor interface. This pin is pulled low to signal that the chip has processed the data.
2-5	STi0-STi3	**ST-BUS Input 0 to 3 (Inputs)**—These are the inputs for the 2048 kbit/s ST-BUS™ input streams.
6-9	IC	**Internal Connections**—Must be connected to V_{DD}.
10	VDD	**Power Input**—Positive Supply.
11	$\overline{F0i}$	**Framing 0-Type (Input)**—This is the input for the frame synchronization pulse for the 2048 kbit/s ST-BUS™ streams. A low on this input causes the internal counter to reset on the next negative transistion of $\overline{C4i}$.
12	$\overline{C4i}$	**4.096 MHz Clock (Input)**—ST-BUS™ bit cell boundaries lie on the alternate falling edges of this clock.
13-18	A0-A5	**Address 0 to 5 (Inputs)**—These are the inputs for the address lines on the microprocessor interface.
19	DS	**Data Strobe (Input)**—This is the input for the active high data strobe on the microprocessor interface.
20	R/$\overline{W}$	**Read or Write (Input)**—This is the input for the read/write signal on the microprocessor interface—high for read, low for write.
21	$\overline{CS}$	**Chip Select (Input)**—This is the input for the active low chip select on the microprocessor interface.
22-29	D7-D0	**Data 7 to 0 (Three-state I/O Pins)**—These are the bidirectional data pins on the microprocessor interface.
30	VSS	**Power Input**—Negative Supply (Ground).
31-34	IC	**Internal Connections**—Leave pins disconnected.
35-38	STo3-STo0	**ST-BUS™ Output 3 to 0 (Three-state Outputs)**—These are the pins for the four 2048 kbit/s ST-BUS™ output streams.
39	ODE	**Output Drive Enable (Input)**—If this input is held high, the STo0-STo3 output drivers function normally. If this input is low, the STo0-STo3 output drivers go into their high impedance state. **NB:** Even when ODE is high, channels on the STo0-STo3 outputs can go high impedance under software control.
40	IC	**Internal Connection**—Leave pin disconnected.

Functional Description

In recent years, there has been a trend in telephony towards digital switching, particularly in association with software control. Simultaneously, there has been a trend in system architectures towards distributed processing or multi-processor systems.

In accordance with these trends, MITEL has devised the ST-BUS™ (Serial Telecom Bus). This bus architecture can be used both in software-controlled digital voice and data switching, and for interprocessor communications. The uses in switching and in interprocessor communications are completely integrated to allow for a simple general purpose architecture appropriate for the systems of the future.

The serial streams of the ST-BUS™ operate continuously at 2048 kbit/s and are arranged in 125μs wide frames which contain 32 8-bit channels. Gould AMI manufactures a number of devices which interface to the ST-BUS™; a key device being the S8981 chip.

The S8981 can switch data from channels on ST-BUS™ inputs to channels on ST-BUS™ outputs, and simultaneously allows its controlling microprocessor to read channels on ST-BUS™

inputs or write to channels on ST-BUS™ outputs (Message Mode.) To the microprocessor, the S8981 looks like a memory peripheral. The microprocessor can write to the S8981 to establish switched connections between input ST-BUS™ channels and output ST-BUS™ channels, or to transmit message on output ST-BUS™ channels. By reading from the S8981, the microprocessor can receive messages from ST-BUS™ input channels or check which switched connections have already been established.

By integrating both switching and interprocessor communications, the S8981 allows systems to use distributed processing and to switch voice or data in an ST-BUS™ architecture.

Hardware Description

Serial data at 2048 kbit/s is received at the four ST-BUS™ inputs (STi0 to STi3), and serial data is transmitted at the four ST-BUS™ outputs (STo0 to STo3). Each serial input accepts 32 channels of digital data, each channel containing an 8-bit word which may represent a PCM-encoded analog/voice sample as provided by a codec (such as the S3507).

This serial input word is converted into parallel data and stored in the 128x8 static Data Memory. Locations in the Data Memory are associated with particular channels on particular ST-BUS™ input streams. These locations can be read by the microprocessor which controls the chip.

Locations in the Connection Memory, which is split into high and low parts, are associated with particular ST-BUS™ output streams. When a channel is due to be transmitted on an ST-BUS™ output, the data for the channel can either be switched from an ST-BUS™ input or it can originate from the microprocessor. If the data is switched from an input, then the contents of the Connection Memory Low location associated with the output channel is used to address the Data Memory. This Data Memory address corresponds to the channel on the input ST-BUS™ stream on which the data for switching arrived. If the data for the output channel originates from the microprocessor (Message Mode), then the contents of the Connection Memory Low location associated with the output channel are output directly, and this data is output repetitively on the channel once every frame until the microprocessor intervenes.

The Connection Memory data is received, via the Control Interface, at D7 to D0. The Control Interface also receives address information at A5 to A0 and handles the microprocessor control signals $\overline{CS}$, $\overline{DTA}$, R/$\overline{W}$ and DS. There are two parts to any address in the Data Memory or Connection Memory. The higher order bits come from the Control Register, which may be written to or read from via the Control Interface. The lower order bits come from the address lines directly.

The Control Register also allows the chip to broadcast message on all ST-BUS™ outputs (i.e., to put every channel into Message Mode), or to split the memory so that reads are from the Data Memory and writes are to the Connection Memory Low. The Connection Memory High determines whether individual output channels are in Message Mode, and allows individual output channels to go into a high-impedance state which enables arrays of S8981s to be constructed.

All ST-BUS™ timing is derived from the two signals $\overline{C4i}$ and $\overline{F0i}$.

Software Control

The Address Lines on the Control Interface give access to the Control Register directly or, depending on the contents of the Control Register to the High or

A5	A4	A3	A2	A1	A0	HEX ADDRESS	LOCATION
0	X	X	X	X	X	00-1F	Control Register*
1	0	0	0	0	0	20	Channel 0†
1	0	0	0	0	1	21	Channel 1†
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
1	1	1	1	1	1	3F	Channel 31†

*Writing to the Control Register is the only fast transaction.

†Memory and stream are specified by the contents of the Control Register.

Low sections of the Connection Memory or to the Data Memory.

If address line A5 is low, then the Control Register is addressed regardless of the other address lines (see Figure 9). If A5 is high, then the address lines A4-A0 select the memory location corresponding to channel 0-31 for the memory and stream selected in the Control Register.

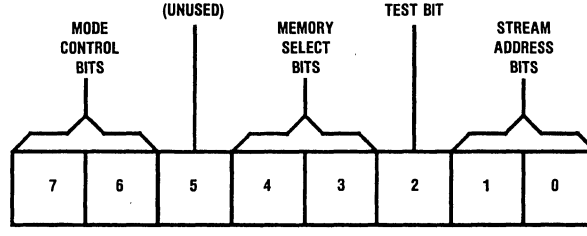
The data in the Control Register consists of mode control bits, memory select bits, stream address bits, and a test bit which should be kept at 0 for normal operation (see Figure 10). The memory select bits allow the Connection Memory High or Low or the Data Memory to be chosen, and the stream address bits define one of the ST-BUS™ input or output streams

Figure 11a and 11b show the effect of the control register on subsequent operations.

Bit 7 of the Control Register allows split memory operation—reads are from the Data Memory and writes are to the Connection Memory Low.

The other mode control bit, bit 6, puts every output channel on every output stream into active Message Mode; i.e., the contents of the Connection Memory Low are output on the ST-BUS™ output streams once every frame unless the ODE pin is low. In this mode the chip behaves as if bits 2 and 0 of every Connection Memory High location were 1, regardless of the actual values.

Figure 10. Control Register Bits



Pin	Label	Function
7	Split Memory	When 1, on subsequent operations all reads are from the Data Memory and all writes are to the Connection Memory, except when the Control Register is accessed. When 0, the Memory Select Bits specify the memory for subsequent operations. In either case, the Stream Address Bits select the subsection of the memory which is made available.
6	Message Mode	When 1, the contents of the Connection Memory Low are output on the Serial Output streams except when the ODE pin is low. When 0, the Connection Memory bits for each channel determine what is output.
5	(unused)	
4-3	Memory Select Bits	0-0 - Reserved for testing. 0-1 - Data Memory. 1-0 - Connection Memory Low. 1-1 - Connection Memory High.
2	Test Bit	This bit is used during probe testing. It should be kept at 0 for normal operations.
1-0	Stream Address Bits	The number expressed in binary notation on these bits refers to the input or output ST-BUS™ stream which corresponds to the subsection of memory made accessible for subsequent operations

Figure 11A. Control Register: Memory and Mode to Contents

MEMORY	MODE	HEX VALUE*	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1*	BIT 0*
DATA	NORMAL	08-0B & 28-2B	0	0	X	0	1	0	X	X
	MESSAGE	48-4B & 68-6B	0	1	X	0	1	0	X	X
CONNECTION LOW	NORMAL	10-13 & 30-33	0	0	X	1	0	0	X	X
	MESSAGE	50-53 & 70-73	0	1	X	1	0	0	X	X
CONNECTION HIGH	NORMAL	18-1B & 38-3B	0	0	X	1	1	0	X	X
	MESSAGE	58-5B & 78-7B	0	1	X	1	1	0	X	X
SPLIT	NORMAL	88-8B, A8-AB, 90-93, B0-B3, 98-9B & B8-BB	1	0	X	0 1 1	1 0 1	0	X	X
	MESSAGE	C8-CB, E8-EB, D0-D3, F0-F3 D8-DB & F8-FB	1	1	X	0 1 1	1 0 1	0	X	X

*The range of values for bits 0 and 1 corresponds to the TDM streams 0 to 3.

Figure 11B. Control Register: Contents to Memory and Mode.

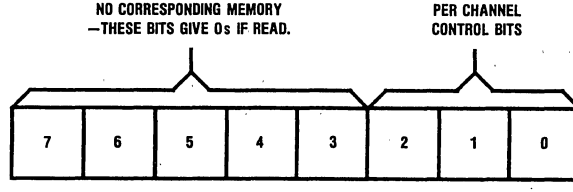
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1*	BIT 0*	HEX VALUE*	MEMORY	MODE
0	0	0	0	1	0	X	X	08-0B	DATA	NORMAL
0	0	0	1	0	0	X	X	10-13	CONNECTION LOW	NORMAL
0	0	0	1	1	0	X	X	18-1B	CONNECTION HIGH	NORMAL
0	0	1	0	1	0	X	X	28-2B	DATA	NORMAL
0	0	1	1	0	0	X	X	30-33	CONNECTION LOW	NORMAL
0	0	1	1	1	0	X	X	38-3B	CONNECTION HIGH	NORMAL
0	1	0	0	1	0	X	X	48-4B	DATA	MESSAGE
0	1	0	1	0	0	X	X	50-53	CONNECTION LOW	MESSAGE
0	1	0	1	1	0	X	X	58-5B	CONNECTION HIGH	MESSAGE
0	1	1	0	1	0	X	X	68-6B	DATA	MESSAGE
0	1	1	1	0	0	X	X	70-73	CONNECTION LOW	MESSAGE
0	1	1	1	1	0	X	X	78-7B	CONNECTION HIGH	MESSAGE
1	0	0	0	1	0	X	X	88-8B	SPLIT	NORMAL
1	0	0	1	0	0	X	X	90-93	SPLIT	NORMAL
1	0	0	1	1	0	X	X	98-9B	SPLIT	NORMAL
1	0	1	0	1	0	X	X	A8-AB	SPLIT	NORMAL
1	0	1	1	0	0	X	X	B0-B3	SPLIT	NORMAL
1	0	1	1	1	0	X	X	B8-BB	SPLIT	NORMAL
1	1	0	0	1	0	X	X	C8-CB	SPLIT	MESSAGE
1	1	0	1	0	0	X	X	D0-D3	SPLIT	MESSAGE
1	1	0	1	1	0	X	X	D8-DB	SPLIT	MESSAGE
1	1	1	0	1	0	X	X	E8-EB	SPLIT	MESSAGE
1	1	1	1	0	0	X	X	F0-F3	SPLIT	MESSAGE
1	1	1	1	1	0	X	X	F8-FB	SPLIT	MESSAGE

*The range of values for bits 0 and 1 corresponds to the TDM streams 0 to 3.
All other combinations of values for the 8 bits are reserved for testing.

If bit 7 of the Control Register is 0, then bits 2 and 0 of each Connection Memory High location function normally. If bit 2 is 1, the associated ST-BUS™ output channel is in Message Mode; i.e., the byte in the corresponding Connection Memory Low location is transmitted on the stream at that channel. Otherwise, one of the bytes received on the serial inputs is transmitted and the contents of the Connection Memory Low define the ST-BUS™ input stream and channel where the byte is to be found (see Figure 13).

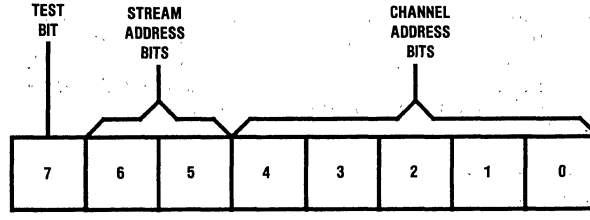
If the ODE pin is low, then all serial outputs are high-impedance. If it is high and bit 6 in the Control Register is 1, then all outputs are active. If the ODE pin is high and bit 6 in the Control Register is 0, then the bit 0 in the Connection Memory High location enables the output drivers for the corresponding individual ST-BUS™ output stream and channel—bit 0 = 1 enables the driver and bit 0 = 0 disables it (see Figure 12).

Figure 12. Connection Memory High Bits



Pin	Label	Description
2	Message Channel	When 1, the contents of the corresponding location in Connection Memory Low are output on the location's channel and stream. When 0, the contents of the corresponding location in Connection Memory Low act as an address for the Data Memory and so determine the source of the connection to the location's channel and stream.
1	(unused)	
0	Output Enable	If the ODE pin is high and bit 6 of the Control Register is 0, then this bit enables the output driver for the location's channel and stream. This allows individual channels on individual streams to be made high-impedance, allowing switching matrices to be constructed. A 1 enables the driver and a 0 disables it.

Figure 13. Connection Memory Low Bits



Pin	Label	Description
7*	Test Bit*	Used during probe test. Keep at 0 unless channel is in the message mode (bit 2 of the corresponding Connection Memory High location or bit 6 of the Control Register).
6-5*	Stream Address Bits*	The number expressed in binary notation on these 2 bits is the number of the ST-BUS™ stream for the source of the connection. Bit 6 is the most significant bit. E.g., if bit 6 is 1 and bit 5 is 0, then the source of the connection is a channel on STi2.
4-0*	Channel Address Bits*	The number expressed in binary notation on these 5 bits is the number of the channel which is the source of the connection (the ST-BUS™ stream where the channel lies is defined by bits 6 and 5). Bit 4 is the most significant bit. E.g., if bit 4 is 1, bit 3 is 0, bit 2 is 0, bit 1 is 1 and bit 0 is 1, then the source of the connection is channel 19.

*If bit 2 of the corresponding Connection High location is 1 or if bit 6 of the Control Register is 1, then these entire 8 bits are output on the channel and stream associated with this location. Otherwide the bits are used as indicated to define the source of the connection which is output on the channel and stream associated with this location.

Applications

Use in a Simple Digital Switching System

Figures 14 and 15 show how S8981s can be used with S8970 and S3507A to form a simple digital switching system. Figure 14 shows the interface between the S8981s and the filter/codecs. Figure 15 shows the position of these components in an example architecture.

The S3507A filter/codec and S8970 line interface in Figure 14 receives and transmits digitized voice signals on the ST-BUS™ input D_R, and ST-BUS™ output D_{XD}, respectively. These signals are routed to the ST-BUS™ inputs and outputs on the top S8981, which is used as a digital speech switch.

The S8970 and S3507A are controlled by the ST-BUS™ input D_C originates the appropriate signals from an output channel in Message Mode. This architecture optimizes the messaging capability of the line circuit by building signalling logic, e.g., for on-off hook detection, which communicates on an ST-BUS™ output. This signalling ST-BUS™ output is monitored by a microprocessor (not shown) through an ST-BUS™ input on the bottom S8981.

Figure 15 shows how a simple digital switching system may be designed using the ST-BUS™ architecture. This is a private telephone network with 128 extensions which uses a single S8981 as a speech switch and a second S8981 for communication with the line interface circuits.

Figure 14. Example of Typical Interface between S8981s, S8970, and S3507A for Simple Digital Switching System

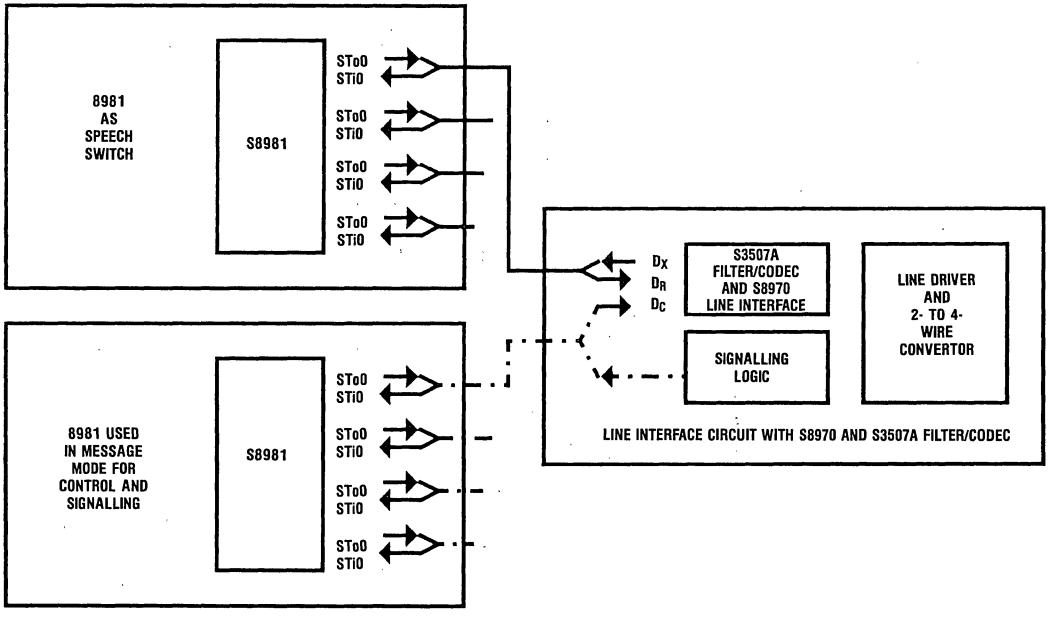
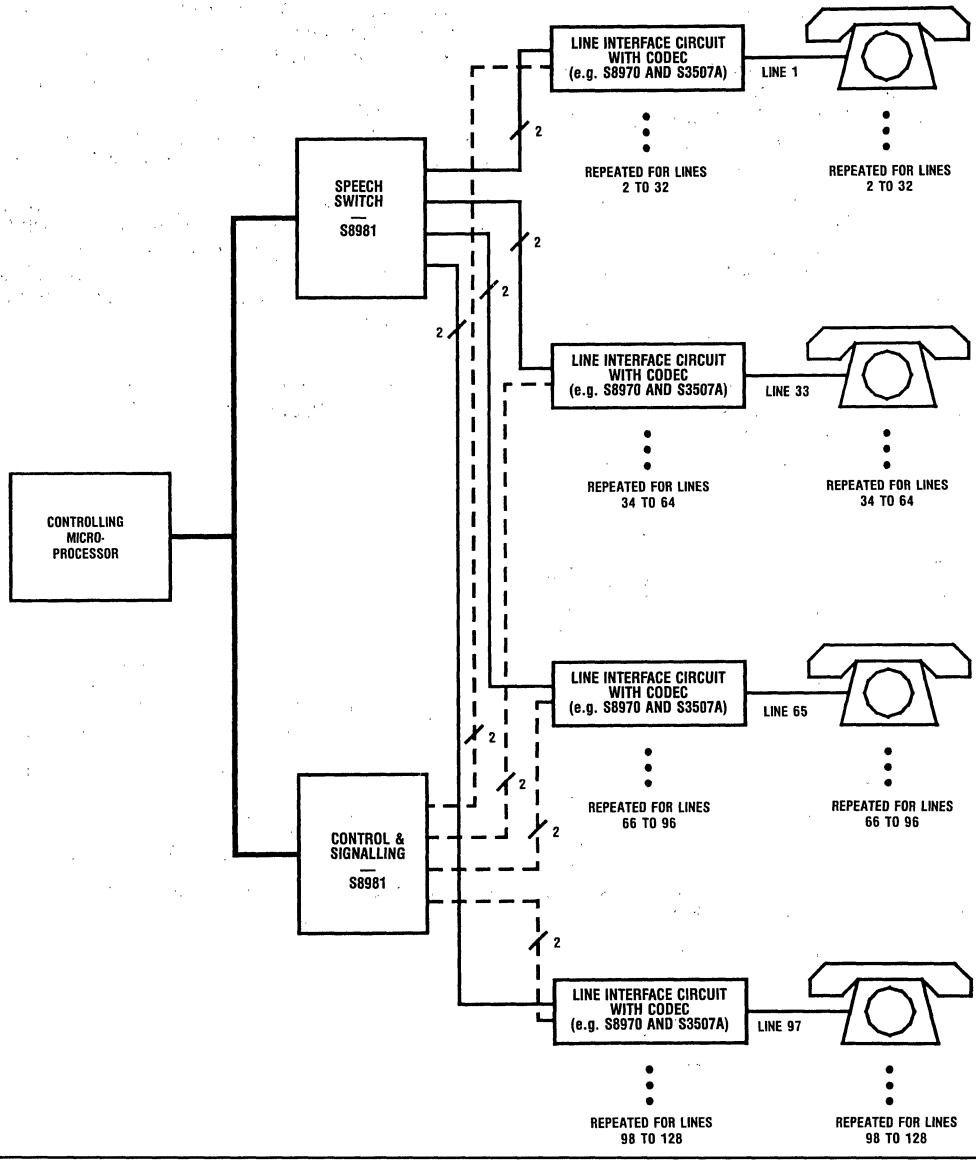
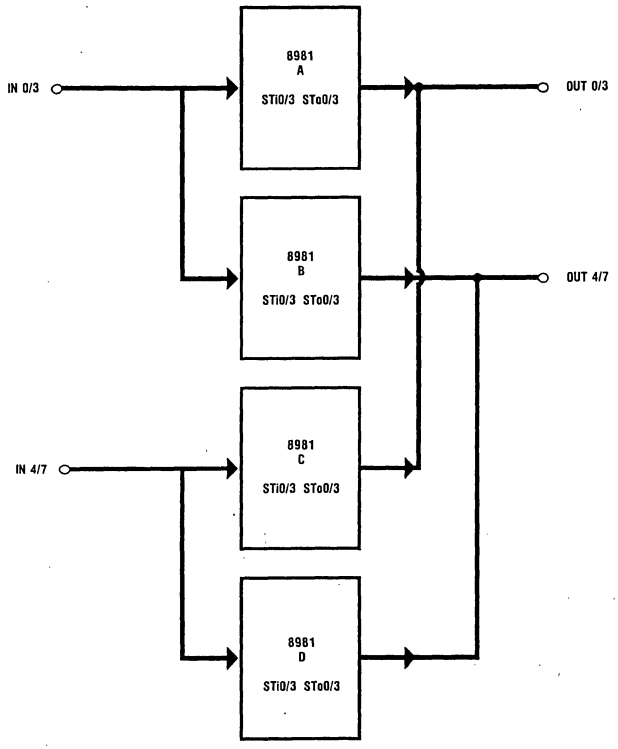


Figure 15. Example Architecture of a Simple Digital Switching System



A larger digital switching system may be designed by cascading a number of S8981s. Figure 16 shows how four S8981s may be arranged in a non-blocking configuration which can switch any channel on any of the ST-BUS™ inputs to any channel on the ST-BUS™ outputs.

Figure 16. Four S8981s Arranged in a Non-Blocking 8 x 8 Configuration



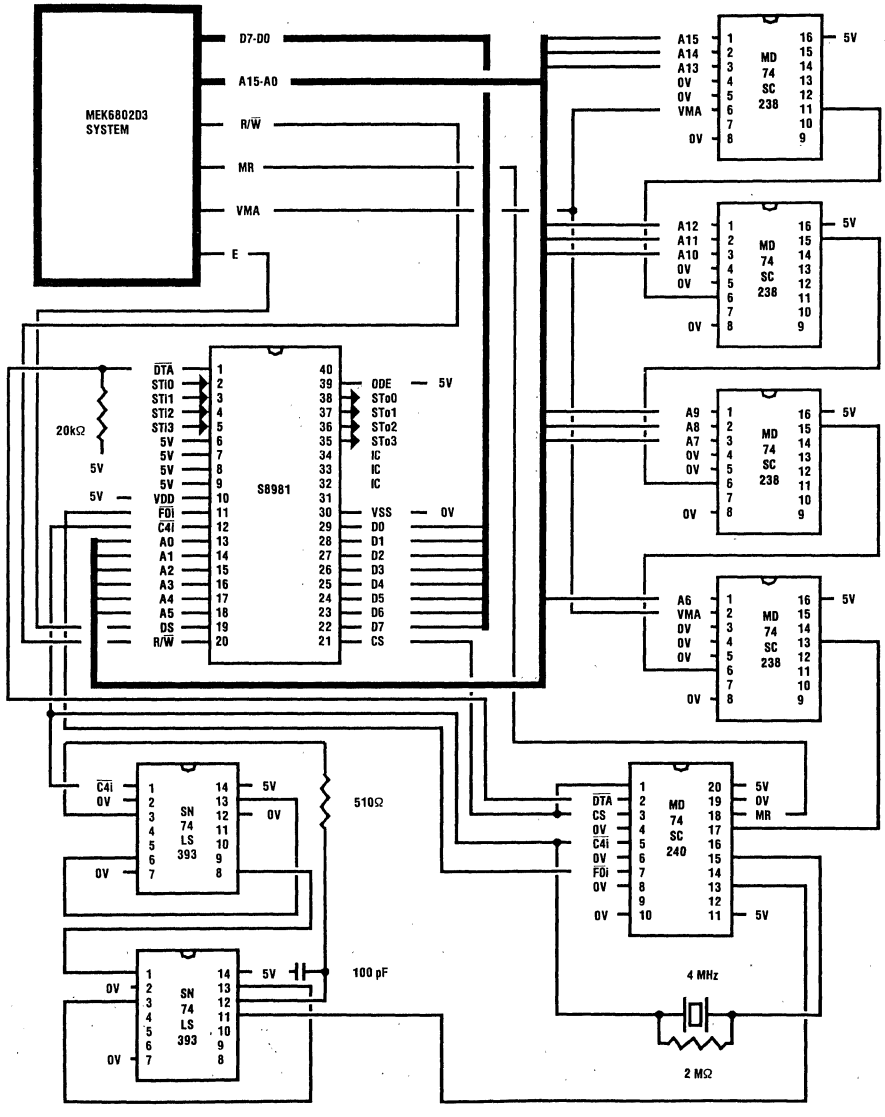
Application Circuit with S6802 Processor

Figure 17 shows an example of a complete circuit which may be used to evaluate the chip.

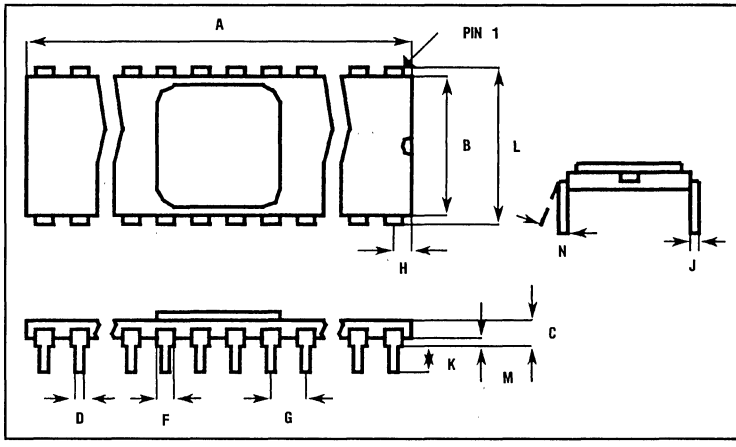
For convenience, a 4 MHz crystal oscillator has been used rather than a 4.096 MHz clock, as both are within the limits of the chips specifications. The RC delay used with the 393 counters ensures a sufficient hold time for the FP signal, but the values used may have to be changed if faster 393 counters become available.

The chip is shown as memory mapped into the MEK6802D3 system. Chip addresses 00-3F correspond to processor addresses 2000-203F. Delay through the address decoder requires the VMA signal to be used twice to remove glitches. The MEK6802D3 board uses a 10KΩ pullup on the MR pin, which would have to be incorporated into the circuit if the board was replaced by a processor.

Figure 17. Application Circuit with S6802



S8981



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.73	15.24	0.580	0.600
C	2.92	3.94	0.115	0.155
D	0.41	0.51	0.016	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.14	1.40	0.045	0.055
J	0.23	0.30	0.009	0.012
K	2.54	3.81	0.100	0.150
L	15.24 BSC		0.600 BSC	
M	1.02	1.52	0.040	0.060
N	—	10°	—	10°

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212A/V.22 Modem Filter With Equalizers & Analog Loopback

S35212A

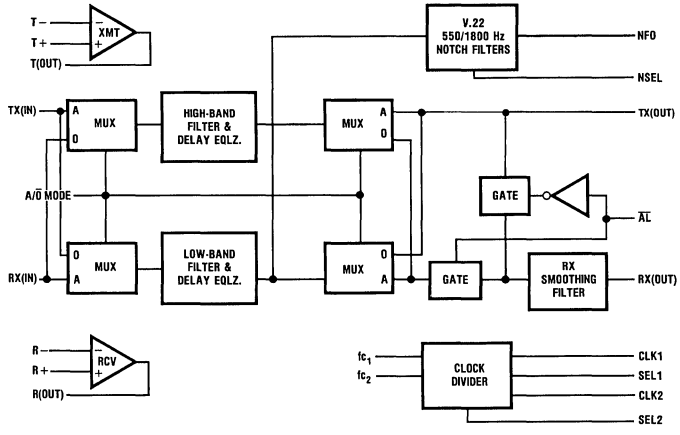
Features

- Bell 212A/V.22/V.22BIS Compatible
- Usable for Bell 103/113 Applications
- High and Low Band Filters With Compromise Group Delay Equalizers and Smoothing Filters
- Guard Tone Notch Filters for CCITT V.22/V.22BIS Applications
- Originate/Answer Operating Modes
- Low Power CMOS: 75 mW Typ.
- Two Uncommitted Operational Amps
- Choice of Clocking Frequencies: 2.4576 MHz, 1.2288 MHz, or 153.6 kHz
- Call Progress Tone Filter Capability
- Analog Loopback Test Capability

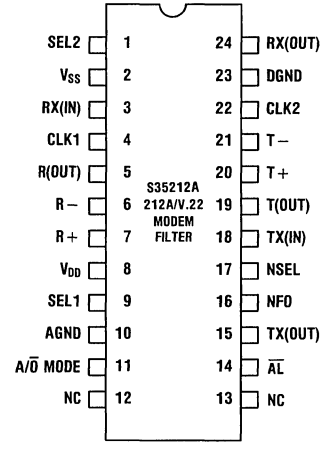
General Description

The S35212A Modem Filter is a monolithic CMOS integrated circuit. It does the filter/equalizing functions of Bell 212A and CCITT V.22 (or V.22BIS) modems. The S35212A includes high band and low band filters. It features on-chip originate/answer mode selection. Included are compromise amplitude and group delay equalizers for full compromise equalization. There is a CCITT notch filter included. It provides rejection at 1800 Hz or 550 Hz. Two uncommitted operational amplifiers are available to use for gain control or anti-aliasing filters. A continuous low pass filter is also included on the RX(OUT) pin to act as a smoothing filter. SEL2 switches the S35212A between the normal data mode

Block Diagram



Pin Configuration



and the call progress monitoring mode. For maximum flexibility the S35212A will operate from a 2.4576 MHz, 1.2228 MHz or 153.6 kHz clock. The S35212A has Analog Loopback capability to switch the transmit carrier output back through the receive output for testing.

Pin Functional Description

Pin Name	Pin Number	Function
SEL2	1	Logic '0' for normal operation. Logic '1' scales down the frequency response by a factor of 6 for Call Progress Tone Detection through the high-band filter.
V_{SS}	2	Negative Supply Voltage (−5 Volts).
RX(IN)	3	Receive Signal Input.
CLK1	4	2.4576 MHz or 1.2288 MHz Clock Input. This input is TTL and CMOS compatible. Leave open when using CLK2.
R(OUT)	5	Receive Uncommitted Op Amp Output (10 kΩ load maximum).
R−	6	Receive Uncommitted Op Amp Negative Input.
R+	7	Receive Uncommitted Op Amp Positive Input.
V_{DD}	8	Positive Supply Voltage (+5 Volts).
SEL1	9	Logic '0' selects 1.2288 MHz. Logic '1' selects 2.4576 MHz clock into Pin 4.
AGND	10	Analog Ground.
MODE (A/$\overline{O}$)	11	Originate/Answer Mode Control Input. A logic '0' sets the device in Originate Mode with the transmit signal in the low-band and receive signal in the high-band. A logic '1' reverses the connections.
N/C	12	Do not connect to this pin.
N/C	13	Do not connect to this pin.
$\overline{AL}$	14	Analog Loopback Control Input. A logic '0' sets the device in Loopback Mode. A logic '1' sets the device in Normal Mode.
TX(OUT)	15	Transmit Signal Output. This output will drive a 20k load.
NFO	16	Notch Filter Output. This output will drive a 20k load.
NSEL	17	A logic '0' on this input programs the notch filter to reject 500 Hz. A logic '1' programs it to reject 1800 Hz.
TX(IN)	18	Transmit Signal Input.
T(OUT)	19	Transmit Uncommitted Op Amp Output (10 kΩ load maximum).
T+	20	Transmit Uncommitted Op Amp Positive Input.
T−	21	Transmit Uncommitted Op Amp Negative Input.
CLK2	22	153.6 kHz Clock Input. This input is TTL and CMOS compatible. Leave open when using CLK1.
DGND	23	Digital Ground.
RX(OUT)	24	Receive Signal Output. This output will drive a 20k load.

Absolute Maximum Ratings

DC Supply Voltage ($V_{DD} - V_{SS}$) ..... + 13.5V
Operating Temperature ..... 0°C to + 70°C
Storage Temperature ..... − 55°C to + 125°C
Analog Input ..... $V_{SS} - 0.3V \leq V_{IN} \leq V_{DD} + 0.3V$

D.C. Electrical Operating Characteristics: $T_A = 0°C$ to $+70°C$; $V_{DD} = +5V \pm 10\%$; $V_{SS} = -5V \pm 10\%$ unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{IH}	High Level Logic Input (Pins 1, 9, 11, 17, 14) SEL2, SEL1, MODE, NSEL, $\overline{AL}$	4		V_{DD}	V
V_{IH}	High Level Logic Input (Pins 4 and 22) CLK1, CLK2	2.0		V_{DD}	V
V_{IL}	Low Level Logic Input (Pins 1, 4, 9, 11, 17, 22, 14)	V_{SS}		0.8	V
R_{IN}	Input Resistance (Pins 3 and 18) RX(IN), TX(IN)		5		MΩ
C_{IN}	Input Capacitance (Pins 3 and 18) RX(IN), TX(IN)		10		pF
P_D	Power Dissipation @ ± 5.25V		75	150	mW

A.C. System Specifications: $T_A = 25°C$; $V_{DD} = +5V \pm 10\%$; $V_{SS} = -5V \pm 10\%$ unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_O	Reference Signal Level Input		1		VRMS
V_{MAX}	Maximum Signal Level Input		1.4		VRMS
BW	Bandwidth (both bands; − 3dB)		960		Hz
A_{FO}	Gain at Center Frequencies	−1	0	+1	dB
ICN_L	Idle Channel Noise-Low Band Filter		22	33	dBrnC0
ICN_H	Idle Channel Noise-High Band Filter		23	33	dBrnC0
N_{FT}	Clock Feedthrough with Respect to Signal Level	TX RX	− 23 − 60		dB dB

Frequency vs. Amplitude Performance of Low- and High- Band Filters

Frequency (Hz) Low-Band Filter	Relative Gain (dB) Min.	Relative Gain (dB) Max.
400		−35
800	−1	+1
1200	0	
1600	−1.5	+1
1800		−18
2000		−48
2400		−55
2800		−50

Frequency (Hz) High-Band Filter	Relative Gain (dB) Min.	Relative Gain (dB) Max.
800		−50
1200		−53
1600		−50
2000	−2.5	+0.5
2400	0	
2800	0	+2.5
3200		−10
3500		−20

Notch Filter Response

Frequency (Hz)	Relative Gain (dB) Min.	Relative Gain (dB) Max.
Low-Band Filter + 1800 Hz Notch Filter		
1200 Hz	−1	+1
1800 Hz		−32
Low-Band Filter + 550 Hz Notch Filter		
1200 Hz	−1	+1
550 Hz		−32

Frequency Response Characteristics
The curves on this page illustrate typical filter responses of the S35212A. Figure 1 shows the basic band split function. This allows full duplex operation within a voice channel. Figures 2 and 3 show the frequency response of the two filters. These curves include the compromise equalizers. Figures 4 and 5 show the typical group delay response of the filters and equalizers.

Figure 1. Typical Amplitude vs. Frequency Plot

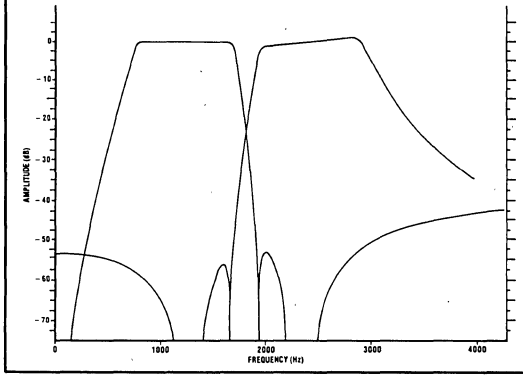


Figure 2. Typical Low-Band Amplitude vs. Frequency Plot

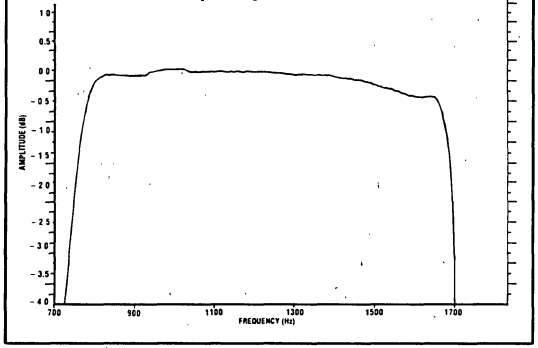


Figure 3. Typical High-Band Amplitude vs. Frequency Plot

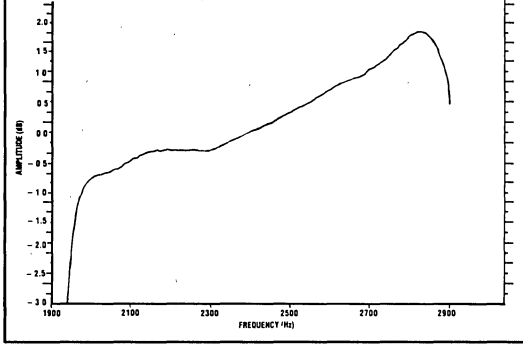


Figure 4. Typical Low-Band Group Delay vs. Frequency Plot

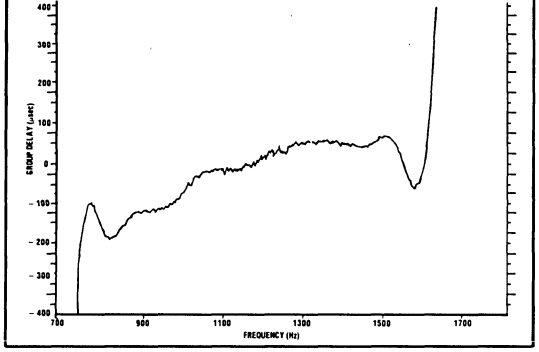
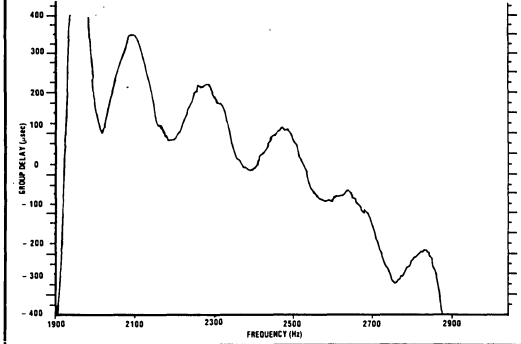


Figure 5. Typical High-Band Group Delay vs. Frequency Plot



Call Progress Monitoring (Pin 1)
The center frequencies of the two filters shift down to one-sixth of their original values when pin 1 goes high. The high-band 2400 Hz filter centers around 400 Hz. Its passband is approximately 300 to 480 Hz. Precision dial tone (350/440 Hz) will pass. Ringback (440/480 Hz) and half of busy/reorder (480/620 Hz) will also pass.

The modem's energy detector software can determine the cadence or timing of the information to identify the proper status of the call.

V.22 Notch Filter (Pins 16, 17)
The S35212A includes a notch filter for CCITT V.22 modem operation. This filter notches out the guard tone required in V.22 operation. When a V.22 modem answers, it sends the 2100 Hz answer tone, and then the 2400 Hz data carrier. It is also required to send along with the data carrier a guard tone of 1800 Hz. (Some administrations require 550 Hz.) The purpose of this tone is to prevent the network from disconnecting. It provides energy at another point in the spectrum other than 2400 Hz. This simulates speech and will not trigger signaling receivers. The tone is only 3 dB below the data carrier. It is 600 Hz closer to the desired receive frequency of 1200 Hz, requiring additional filtering to maintain performance.

Pin 17, NSEL, when high, provides 1800 Hz notching. When low, it provides 550 Hz notching.

The output of the low-band filter, through the notch filter, is always available at pin 16, Notch Filter Out.

Analog Loopback (ALB) (Pin 14)
When pin 14, $\overline{AL}$, is low, the signal at pin 18, TX(IN), passes through the filter selected by pin 11, A/$\overline{O}$, and out through pin 5, RX(OUT).

Analog Loopback tests the local modem and terminal/computer hardware and software. Any character sent from the keyboard echoes back to the screen after being sent to the modem. It is modulated by the modem and sent out to the filter. If pin 14 is low, the analog signal passes back through the RX(OUT) pin to the modem. It is demodulated and returned to the terminal/computer as received data.

Call Progress Tones

Frequencies	Timing/Cadence	Condition Indicated
350 + 440 Hz	Constant Tone	Dial Tone
440 + 480 Hz	2sec on, 4sec off	Audible Ringing
480 + 620 Hz	0.5sec on, 0.5sec off (60 ppm)	Line Busy (Station Busy)
480 + 620 Hz	0.25sec on, 0.25sec off (120 ppm)	Trunk Busy (Reorder)

Clock Input Selection (Pins 4, 9, 22)
The filter uses one of three possible clock frequencies. Either 2.4576 MHz or 1.2288 MHz can be applied to pin 4, CLK1. Pin 9, SEL1, when high, selects the divider for 2.4576 MHz. When low, it selects the divider for 1.2288 MHz. When using the S35212A with the S35213 modem chip, or if a 153.6 kHz clock is available, the clock is applied to pin 22, CLK2. Leave pins 4 and 9 open.

Compatibility with Previous Filters (Pins 12, 13, 14)
The S35212A plugs directly into any socket that previously held an S35212. It functions exactly as the S35212 as long as pin 14 is high. Pins 12 and 13 should be left open.

Answer/Originate Mode Selection (Pin 11)
Pin 11 selects the filters for the particular mode of operation. When it is low for the originate mode, the transmit path is through the low-band filter. Receive is through the high-band filter. When this pin is high for the answer mode, the transmit path is through the high-band filter. Receive is through the low-band filter. An internal pull-down resistor keeps the chip in the originate mode when this pin is not connected.

Uncommitted Operational Amplifiers

The two operational amplifiers are available to use as gain stages or anti-aliasing filters for the complete modem circuit. These are CMOS op amps. They do not have low impedance drive capability. Do not load by less than 10 kΩ. The open loop voltage gain is typically about 86 dB and the unity gain frequency is about 1.5 MHz with < 5 pF loading. Input offset voltages will be 10 mV or less.

Using one of the op amps for anti-aliasing is a good idea. The receive input to the filters must be band limited to avoid aliasing. The telephone network band limits the incoming signals from distant modems. Nevertheless, local noise or noise on the modem board itself can create problems. Figure 6 shows a second-order low-pass filter constructed around the receive op amp. It is a critically-damped, unity-gain, Sallen-Key filter with a cutoff frequency of 6 kHz.

Figure 6. Anti-Aliasing Low-Pass Filter for S35212A

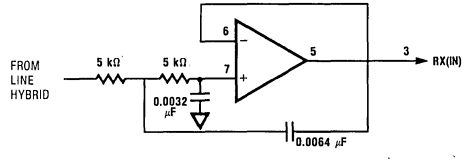
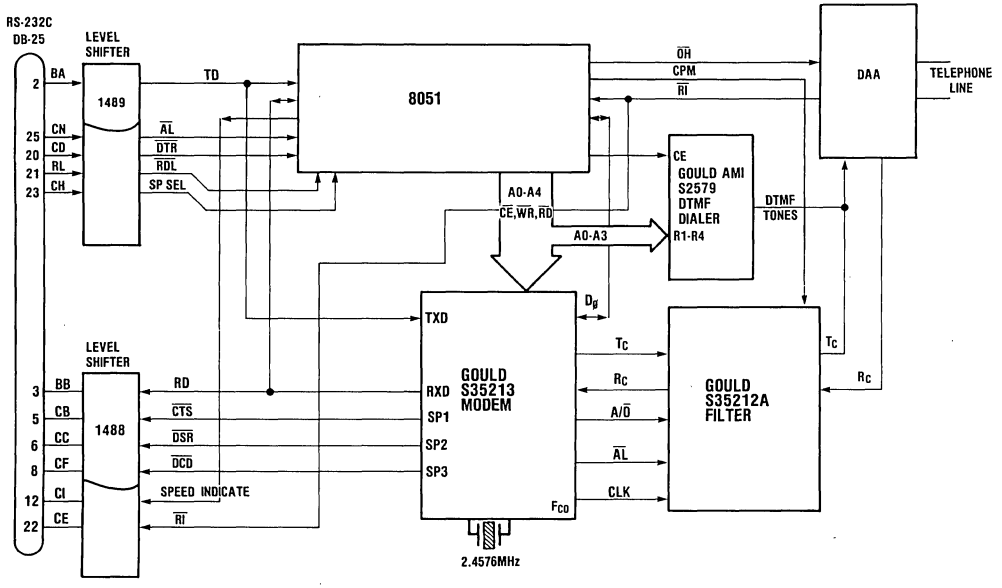


Figure 7. RS-232 Serial Modem for 1200/300bps Asynchronous Operation/Auto-Answer/Auto-Dial Capability



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AMI Semiconductors

212A/V.22 Modem Filter With Equalizers

Advanced Product Description

S35212B

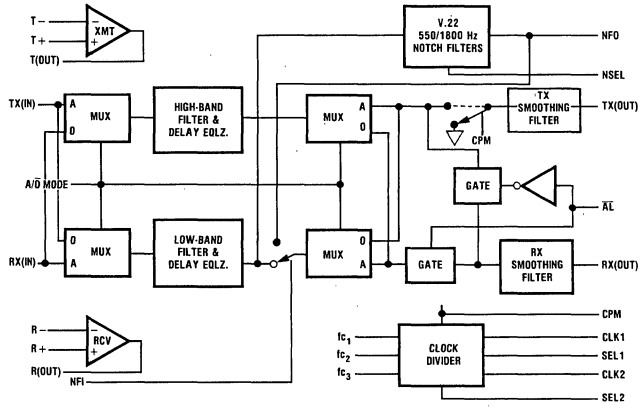
Features

- ☐ Bell 212A/V.22/V.22BIS Compatible
- ☐ Usable for Bell 103/113 Applications
- ☐ High and Low Band Filters With Compromise Group Delay Equalizers and Smoothing Filters
- ☐ Guard Tone Notch Filters for CCITT V.22/V.22BIS Applications
- ☐ Originate/Answer Operating Modes
- ☐ Low Power CMOS: 75 mW Typ.
- ☐ Two Uncommitted Operational Amps
- ☐ Choice of Clocking Frequencies: 2.4576 MHz, 1.2288 MHz, or 153.6 kHz
- ☐ Call Progress Tone Filter Capabilities
- ☐ Analog Loopback Test Capability

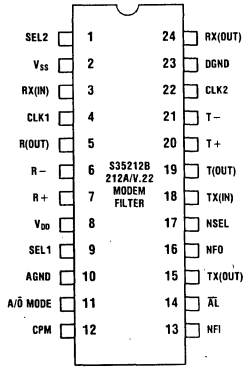
General Description

The S35212B Modem Filter is a monolithic CMOS integrated circuit. It does the filter/equalizing functions of Bell 212A and CCITT V.22 (or V.22BIS) modems. The S35212B includes high band and low band filters. It features on-chip originate/answer mode selection. Included are compromise amplitude and group delay equalizers for full compromise equalization. There is a CCITT notch filter included. It provides rejection at 1800 Hz or 550 Hz. The NFI pin switches the notch filter in or out of the low band filter path. It is in for V.22 and out for 212A operation. Two uncommitted operational amplifiers are available to use for gain control or anti-aliasing filters. A con-

Block Diagram



Pin Configuration



tinuous low pass filter is also included on the RX(OUT) pin to act as a smoothing filter. SEL2 switches the S35212B between the normal data mode and the call progress monitoring mode. The CPM pin switches on a second call progress mode. For maximum flexibility the S35212B will operate from a 2.4576 MHz, 1.2228 MHz or 153.6 kHz clock. The S35212B has Analog Loopback capability to switch the transmit carrier output back through the receive output for testing.

Pin Name	Pin Number	Function
SEL2 *	1	Logic '0' for normal operation. Logic '1' scales down the frequency response by a factor of 6 for Call Progress Tone Detection through the high-band filter.
V_{SS}	2	Negative Supply Voltage (−5 Volts).
RX(IN)	3	Receive Signal Input.
CLK1 *	4	2.4576 MHz or 1.2288 MHz Clock Input. This input is TTL and CMOS compatible. Leave open when using CLK2.
R(OUT)	5	Receive Uncommitted Op Amp Output (10 kΩ load maximum).
R−	6	Receive Uncommitted Op Amp Negative Input.
R+	7	Receive Uncommitted Op Amp Positive Input.
V_{DD}	8	Positive Supply Voltage (+5 Volts).
SEL1	9	Logic '0' selects 1.2288 MHz. Logic '1' selects 2.4576 MHz clock into Pin 4.
AGND	10	Analog Ground.
MODE (A/$\overline{O}$) *	11	Orginate/Answer Mode Control Input. A logic '0' sets the device in Originate Mode with the transmit signal in the low-band and receive signal in the high-band. A logic '1' reverses the connections.
CPM *	12	This pin scales down the frequency response of the low-band filter by 2.5 for Call Progress Detection, leaving the high-band filter to receive incoming carriers.
NFI *	13	Notch Filter Insert. A logic '1' inserts the notch filter in the path from the low-band filter.
$\overline{AL}$ ‡	14	Analog Loopback Control Input. A logic '0' sets the device in Loopback Mode. A logic '1' sets the device in Normal Mode.
TX(OUT)	15	Transmit Signal Output. This output will drive a 20k load.
NFO	16	Notch Filter Output. This output will drive a 20k load.
NSEL *	17	A logic '0' on this input programs the notch filter to reject 500 Hz. A logic '1' programs it to reject 1800 Hz.
TX(IN)	18	Transmit Signal Input.
T(OUT)	19	Transmit Uncommitted Op Amp Output (10 kΩ load maximum).
T+	20	Transmit Uncommitted Op Amp Positive Input.
T−	21	Transmit Uncommitted Op Amp Negative Input.
CLK2 *	22	153.6 kHz Clock Input. This input is TTL and CMOS compatible. Leave open when using CLK1.
DGND	23	Digital Ground.
RX(OUT)	24	Receive Signal Output. This output will drive a 20k load.

*Internal Pull-downs. ‡Internal Pull-up.

Absolute Maximum Ratings

DC Supply Voltage ($V_{DD} - V_{SS}$) ..... +13.5V
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −55°C to +125°C
Analog Input ..... $V_{SS} - 0.3V \leq V_{IN} \leq V_{DD} + 0.3V$

D.C. Electrical Operating Characteristics: $T_A = 0°C$ to $+70°C$; $V_{DD} = +5V \pm 10\%$; $V_{SS} = -5V \pm 10\%$ unless otherwise specified.

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{IN}	High Level Logic Input (Pins 1, 4, 9, 11, 12, 13, 14, 17, 22)	2.0		V_{DD}	V
V_{IL}	Low Level Logic Input (Pins 1, 4, 9, 11, 12, 13, 14, 17, 22)	V_{SS}		0.8	V
R_{IN}	Input Resistance (Pins 3 and 18) RX(IN), TX(IN)		5		MΩ
C_{IN}	Input Capacitance (Pins 3 and 18) RX(IN), TX(IN)		10		pF
P_D	Power Dissipation @ ±5.5V		75	150	mW

A.C. System Specifications: $T_A = 25°C$; $V_{DD} = +5V \pm 10\%$; $V_{SS} = 5V \pm 10\%$ unless otherwise specified.

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_0	Reference Signal Level Input		1		VRMS
V_{MAX}	Maximum Signal Level Input		1.4		VRMS
BW	Bandwidth (both bands; −3 dB)		960		Hz
A_{F0}	Gain at Center Frequencies	−1	0	+1	dB
ICN_L	Idle Channel Noise — Low-Band Filter		22	33	dBrnC0
ICN_H	Idle Channel Noise — High-Band Filter		23	33	dBrnC0
N_{FT}	Clock Feedthrough with Respect to Reference Signal Level TX RX		−40 −60		dB dB
THD_{RX}					
THD_{TX}					

Frequency vs. Amplitude Performance of Low- and High- Band Filters

Frequency (Hz) Low-Band Filter	Relative Gain (dB) Min.	Max.
400		−35
800	−1	+1
1200	0	
1600	−1.5	+1
1800		−18
2000		−48
2400		−55
2800		−50

Frequency (Hz) High-Band Filter	Relative Gain (dB) Min.	Max.
800		−50
1200		−53
1600		−50
2000	−2.5	+0.5
2400	0	
2800	0	+2.5
3200		−10
3500		−20

Notch Filter Response

Frequency (Hz)	Relative Gain (dB) Min.	Max.
Low-Band Filter + 1800 Hz Notch Filter		
1200 Hz	−1	+1
1800 Hz		−45
Low-Band Filter + 550 Hz Notch Filter		
1200 Hz	−1	+1
550 Hz		−35

Frequency Response Characteristics

The curves on this page illustrate typical filter responses of the S35212B. Figure 1 shows the basic band split function. This allows full duplex operation within a voice channel. Figures 2 and 3 show the frequency response of the two filters. These curves include the compromise equalizers. Figures 4 and 5 show the typical group delay response of the filters and equalizers.

Call Progress Monitoring (Pins 1, 12)

The S35212B has two methods of doing call progress monitoring. The first method, in common with the S35212A, uses pin 1, SEL2, for activation. The second method, uses pin 12, CPM, for activation.

Figure 1. Typical Amplitude vs. Frequency Plot

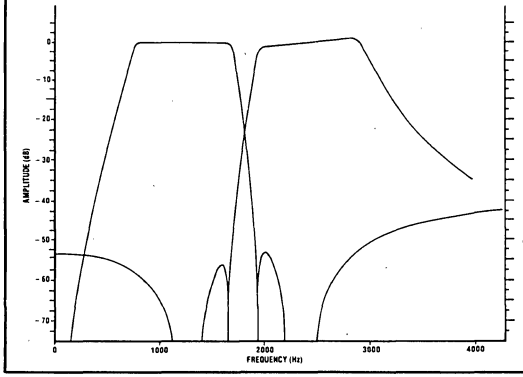


Figure 2. Typical Low-Band Amplitude vs. Frequency Plot

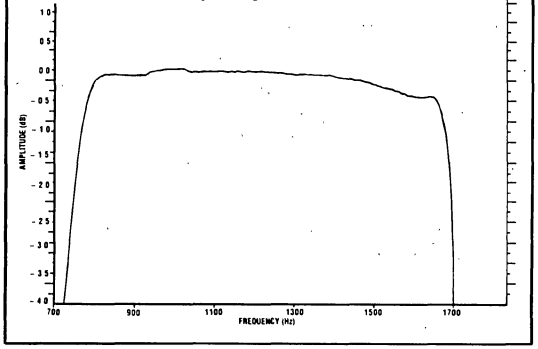


Figure 3. Typical High-Band Amplitude vs. Frequency Plot

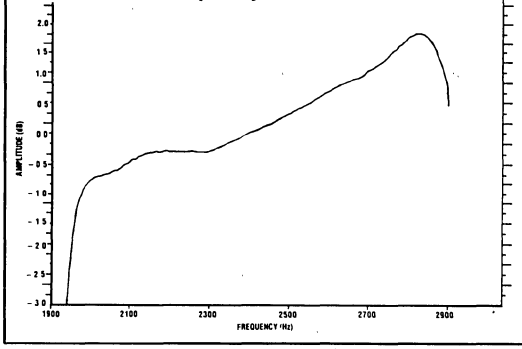


Figure 4. Typical Low-Band Group Delay vs. Frequency Plot

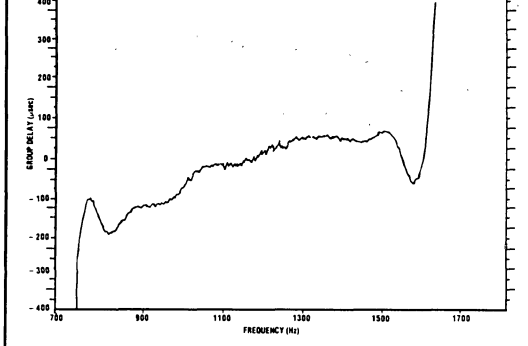
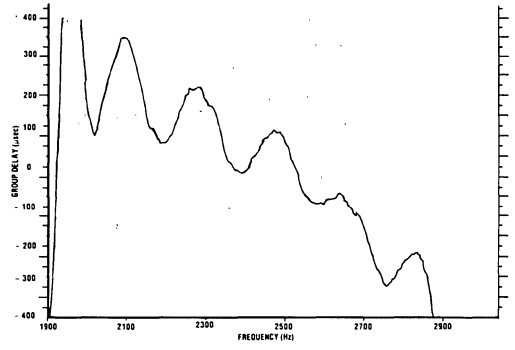


Figure 5. Typical High-Band Group Delay vs. Frequency Plot



The center frequencies of the two filters shift down to one-sixth of their original values when pin 1 goes high. The high-band 2400 Hz filter centers around 400 Hz. Its passband is approximately 300 to 480 Hz. Precision dial tone (350/440 Hz) will pass. Ringback (440/480 Hz) and half of busy/reorder (480/620 Hz) will also pass.

The second method, using pin 12, leaves the high-band filter at 2400 Hz. It shifts the low-band filter down by a factor of 2.5 for a center frequency of 480 Hz. The 620 Hz frequency passes through along with the others. Because the high-band filter remains at 2400 Hz, it takes fewer instructions to switch between call progress tones and data carrier. The receive input goes to both filters under this condition. Either the received carrier or the CPM tones are available at the receive output pin.

The modem's energy detector software can determine the cadence or timing of the information to identify the proper status of the call.

The second mode also squelches the transmit output to the line. No tones will come from the originating modem until answering carrier detection. This is not necessary with the S35213 modem chip, as it already has a squelch command for this purpose.

V.22 Notch Filter (Pins 13, 16, 17)

The S35212B includes a notch filter for CCITT V.22 modem operation. This filter notches out the guard tone required in V.22 operation. When a V.22 modem answers, it sends the 2100 Hz answer tone, and then the 2400 Hz data carrier. It is also required to send along with the data carrier a guard tone of 1800 Hz. (Some adminstrations require 550 Hz.) The purpose of this tone is to prevent the network from disconnecting. It provides energy at another point in the spectrum other than 2400 Hz. This simulates speech and will not trigger signaling receivers. The tone is only 3 dB below the data carrier. It is 600 Hz closer to the desired receive frequency of 1200 Hz, requiring additional filtering to maintain performance.

Pin 13, NFI, when made high, switches in the notch filter. It goes between the output of the low-band filter and the receive smoothing filter. Pin 17, NSEL, when high, provides 1800 Hz notching. When low, it provides 550 Hz notching.

The output of the low-band filter, through the notch filter, is always available at pin 16, Notch Filter Out. This is the same as the S35212A.

Call Progress Tones

Frequencies	Timing/Cadence	Condition Indicated
350+440 Hz	Constant Tone	Dial Tone
440+480 Hz	2sec on, 4sec off	Audible Ringing
480+620 Hz	0.5sec on, 0.5sec off (60 ppm)	Line Busy (Station Busy)
480+620 Hz	0.25sec on, 0.25sec off (120 ppm)	Trunk Busy (Reorder)

Analog Loopback (ALB) (Pin 14)

When pin 14, $\overline{AL}$, is low, the signal at pin 18, TX(IN), passes through the filter selected by pin 11, A/$\overline{O}$, and out through pin 5, RX(OUT). An internal pull-up resistor holds this pin high when not used. The S35212B will directly replace the S35212A without any circuit changes.

Analog Loopback tests the local modem and terminal/computer hardware and software. Any character sent from the keyboard echoes back to the screen after being sent to the modem. It is modulated by the modem and sent out to the filter. If pin 14 is low, the analog signal passes back through the RX(OUT) pin to the modem. It is demodulated and returned to the terminal/computer as received data.

Clock Input Selection (Pins 4, 9, 22)

The filter uses one of three possible clock frequencies. Either 2.4576 MHz or 1.2288 MHz can be applied to pin 4, CLK1. Pin 9, SEL1, when high, selects the divider for 2.4576 MHz. When low, it selects the divider for 1.2288 MHz. When using the S35212B with the S35213 modem chip, or if a 153.6 kHz clock is available, the clock is applied to pin 22, CLK2. Leave pins 4 and 9 open.

Compatibility with Previous Filters (Pins 12, 13, 14)

The S35212B plugs directly into any socket that previously held an S35212 or S35212A. It functions exactly as the S35212 as long as pins 12, 13, and 14 are open. Pins 12 and 13 may be low and pin 14 high for the same results. The S35212B directly replaces the S35212A when pins 12 and 13 are open or low.

Answer/Originate Mode Selection (Pin 11)

Pin 11 selects the filters for the particular mode of operation. When it is low for the originate mode, the transmit path is through the low-band filter. Receive is through the high-band filter. When this pin is high for the answer mode, the transmit path is through the high-band filter. Receive is through the low-band filter. An internal pull-down resistor keeps the chip in the originate mode when this pin is not connected.

Operation Mode Selection

The four control pins, 12 (CPM), 1 (SEL2), 14 ($\overline{AL}$), and 11 (A/$\overline{O}$) put the S35212B into 12 different operating modes. The first eight modes are the same as the S35212A. The additional four modes of the S35212B provide additional call progress monitoring using pin 12. Only five of the 12 modes are normally used. Analog Loopback testing uses another two modes. See Table 1 below.

Uncommitted Operational Amplifiers

The two operational amplifiers are available to use as gain stages or anti-aliasing filters for the complete modem circuit. These are CMOS op amps. They do not have low impedance drive capability. Do not load by less than 10 kΩ. The open loop voltage gain is typically about 86 dB and the unity gain frequency is about 1.5 MHz with < 5 pF loading. Input offset voltages will be 10 mV or less.

Using one of the op amps for anti-aliasing is a good idea. The receive input to the filters must be band limited to avoid aliasing. The telephone network band limits the incoming signals from distant modems.

Nevertheless, local noise or noise on the modem board itself can create problems. Figure 6 shows a

Table 1. Operating Modes

Function	Mode	12 CPM	1 SEL2	14 $\overline{AL}$	11 A/$\overline{O}$	18 TX(IN)	15 TX(OUT)	3 RX(IN)	24 RX(OUT)
Normal Orig.	0	0	0	1	0	L	L	H	H
Normal Ans.	1	0	0	1	1	H	H	L	L
ALB - Orig.	2	0	0	0	0	L	L	H	L
ALB - Ans.	3	0	0	0	1	H	H	L	H
CPM1 - Orig.	4	0	1	1	0	L/6	L/6	H/6	H/6
Test - N/U	5	0	1	1	1	H/6	H/6	L/6	L/6
Test - N/U	6	0	1	0	0	L/6	L/6	H/6	H/6
Test - N/U	7	0	1	0	1	H/6	H/6	L/6	L/6
Det Ans Tone	8	1	X	1	0	—	SQT	L/2.5+H	H
Test - N/U	9	1	X	1	1	H	SQT	L/2.5	L/2.5
Det CPM Tone	10	1	X	0	0	—	SQT	L/2.5+H	L/2.5
Test - N/U	11	1	X	0	1	H	SQT	L/2.5	H

Notes: SQT indicates that the transmit output is squelched.
L indicates the filter with a center frequency of 1200 Hz.
H indicates the filter with a center frequency of 2400 Hz.
+ indicates connection to both filters.
– indicates no filter connection.
X indicates a "don't care" condition.
L/6 indicates the low-band filter scaled down by 6.
L/25 indicates the low-band filter scaled down by 2.5.

Normal operation uses modes 0 and 1 for originate and answer.
Call progress capability uses modes 4, 8, or 10.
Analog Loopback testing uses modes 2 and 3.
Modes 5, 6, 7, 9, and 11 are additional test modes, not normally used.

second-order low-pass filter constructed around the receive op amp. It is a critically-damped, unity-gain, Sallen-Key filter with a cutoff frequency of 6 kHz.

Figures 7 and 8 illustrate the signal path during CPM2 modes 8 and 10. The A/$\overline{O}$, pin 14, is used to select between Call Progress Tones through the low-band filter or data/voice through the high-band filter.

Figure 6. Anti-Aliasing Low-Pass Filter for S35212B

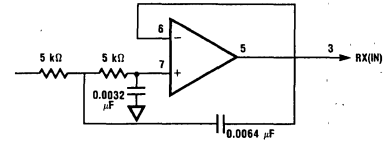


Figure 7. Call Progress Monitor Mode 8: Monitoring Answer Tone/Voice

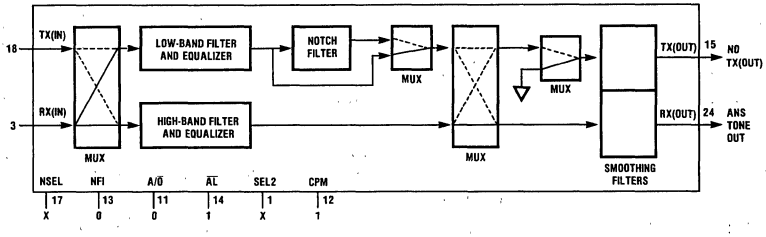
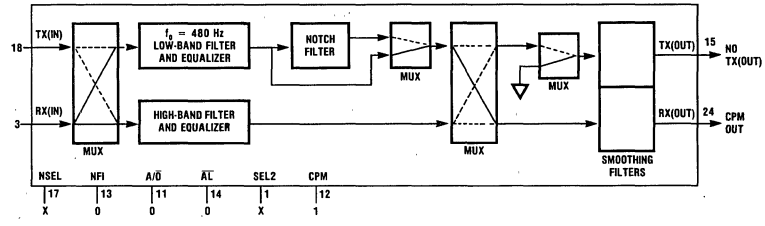


Figure 8. Call Progress Monitor Mode 10: Monitoring Call Progress Tones



GOULD

AMI Semiconductors

Bell 212A Single Chip 1200/300 BPS Modem

S35213

COMMUNICATION PRODUCTS

Features

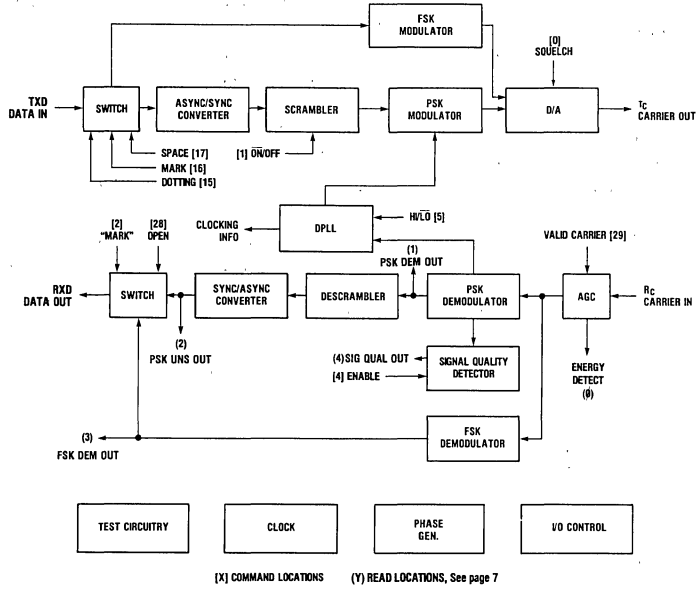
- ☐ Bell 212A compatible
- ☐ Single-chip 1200 bps Full Duplex PSK Modem with 300 bps FSK Fallback Mode
- ☐ On-Chip Scrambler-Descrambler
- ☐ On-Chip Async/Sync and Sync/Async Conversion
- ☐ Full Analog and Digital Loopback Test Capability
- ☐ Carrier Detect and Automatic Gain Control
- ☐ 1200Hz Clock Output for Receive and Transmit Data
- ☐ Selectable for Operation with Internal or External Clock
- ☐ 2.4576MHz Crystal Controlled with Filter Clock (153.6kHz) Output Available
- ☐ 48dB (0 to −48dBm) Dynamic Input Range
- ☐ Selectable Character Length (8, 9, 10 or 11 Bits)
- ☐ Microprocessor Bus Interface
- ☐ CMOS with TTL Compatible Input/Outputs
- ☐ 28-Pin Package

General Description

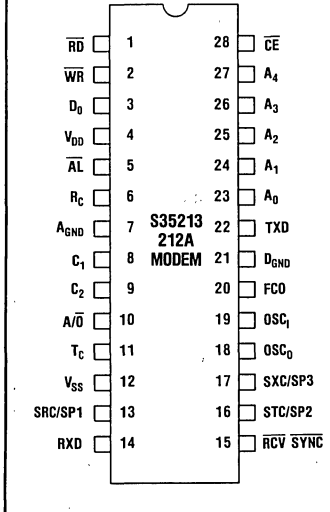
The S35213 is a single-chip Modulator/Demodulator circuit fully compatible with the Bell 212A standard. It contains a 1200 bps PSK Mod/Demod and a fallback 300 bps FSK Mod/Demod. When used with the S35212A modem filter, all the modulation-demodulation and filtering functions to realize a Bell 212A modem are in place.

The S35213 has on-chip Scrambler and Descrambler, asynchronous-to-synchronous and synchronous-to-asynchronous conversion circuitry. It can accept internally generated clock or external clock. It features a 1200Hz output to optionally clock receive or transmit digital data to or from the data terminal. Digital and analog loopback test capability are also provided.

Block Diagram



Pin Configuration



S35213

General Description (Continued)

The S35212A/S35213 chip set is designed for stand-alone as well as integrated modem applications. Both chips are implemented using Gould's proprietary double-poly CMOS technology which guarantees low power operation. This makes the chip set ideal for portable or battery operated systems. It runs from ±5 volt supplies with inputs and outputs being TTL level compatible.

Applications

- ☐ Stand-Alone RS-232C Interface Modems
- ☐ Modem in a Telephone Set with RS-232C Jack
- ☐ Board Level μP bus Interface Modems
- ☐ "Smart Modems"
- ☐ Data Telemetry Systems

Pin Functions

Pin #	Description	I/O	Levels	Function
1	$\overline{RD}$	I	TTL	Read Enable
2	$\overline{WR}$	I	TTL	Write Enable
3	D_ϕ	I/O	TTL	Data I/O — Is high impedance when not selected.
4	V_{DD}	Supply	+5V	+5V supply pin
5	$\overline{AL}$	O	CMOS	Analog loopback signal to filter chip S35212A.
6	R_C	I	Analog	Receive carrier input signal
7	A_{GND}	—	—	Analog ground pin.
8	C_1			External .1μF capacitor for offset compensation connected across these pins.
9	C_2			
10	$A/\overline{O}$	O	CMOS	Answer or originate mode signal to filter chip S35212A.
11	T_C	O	Analog	Transmit carrier output signal drives 20kΩ load at −7dBm (346mVRMS)
12	V_{SS}	Supply	−5V	−5V supply pin.
13	SRC/SP1	O	TTL	Synchronous Receive Clock. Received 1200Hz clock (recovered)—The data bit transitions are synchronous with positive edge of SRC. Alternatively, under asynchronous mode, this pin can be used as a spare line, SP1 (addresses 18, 19).
14	RXD	O	TTL	Received digital data to terminal—will be synchronous with SRC in the sync. mode.
15	$\overline{RCV\ SYNC}$	O	TTL	Provides a negative pulse 3μsec or 6μsec wide on the leading edge of each received data bit.
16	STC/SP2	O	TTL	Synchronous Transmit Clock. Transmitted 1200Hz clock. It's rising edge indicates time to change T_D data. Alternatively, SP2 (addresses 20, 21).
17	SXC/SP3	I/O	TTL	Synchronous External Clock. External transmit clock from data terminal for sync. in the external synchronous mode. Alternatively, SP3 output (addresses 22, 23)
18	OSC_O	O	CMOS	Crystal oscillator output pin-capacitor to V_{SS}. Uses 2.4576 MHz crystal across these pins. The capacitors should be 20pF each.
19	OSC_I	I	CMOS	Crystal oscillator input pin-capacitor to V_{SS}.
20	FCO	O	TTL	153.6kHz clock signal to S35212A filter chip.
21	D_{GND}	—	—	Digital ground pin.
22	TXD	I	TTL	Digital data input from terminal must be synchronized to STC or SXC when in sync. mode.
23	A_0	I	TTL	Address Line.
24	A_1	I	TTL	Address Line.
25	A_2	I	TTL	Address Line
26	A_3	I	TTL	Address Line
27	A_4	I	TTL	Address Line
28	$\overline{CE}$	I	TTL	Chip Enable

Absolute Maximum Ratings

DC Supply Voltage ($V_{DD} - V_{SS}$) ..... +13.5V
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −55°C to +125°C
Analog Input/Digital Input ..... $V_{SS} - 0.3V \leq V_{IN} \leq V_{DD} + 0.3V$

D.C. Electrical Operating Characteristics: $T_A = 0°C$ to $+70°C$; $V_{DD} = +5V$ (±10%); $V_{SS} = -5V$ (±10%) unless otherwise specified

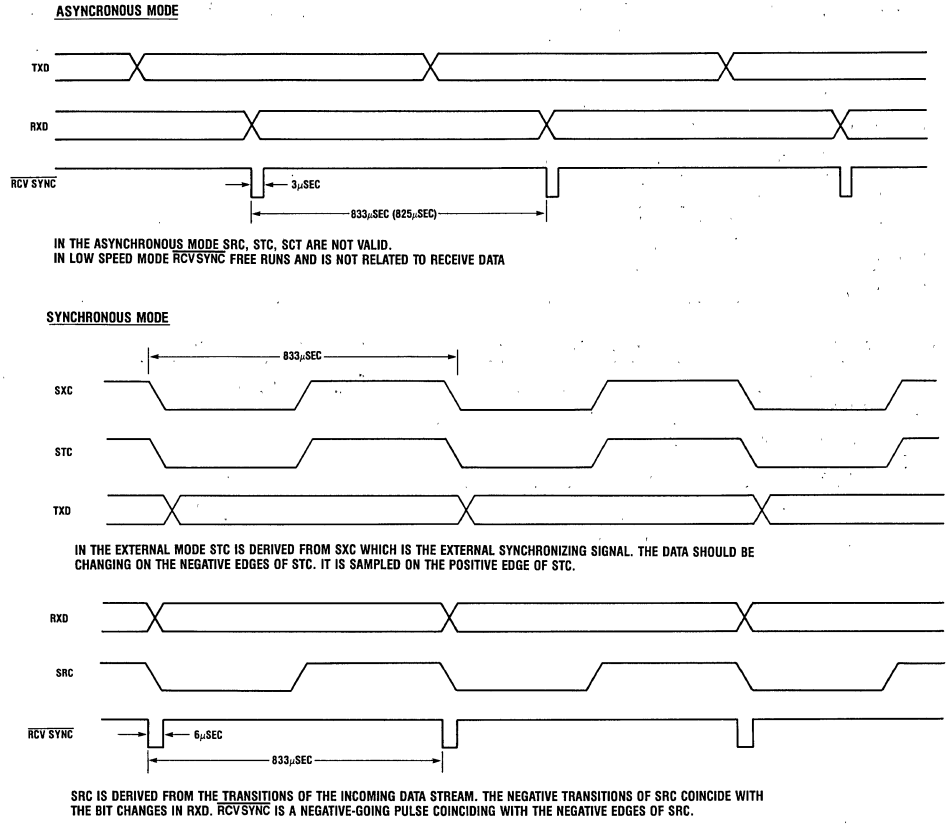
Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{IH}	High Level Logic Input (Pins 1-3, 17, 22-28)	2.0		V_{DD}	V
V_{IL}	Low Level Logic Input (Pins 1-3, 17, 22-28)	V_{SS}		+0.8	V
V_{OH}	High Level Logic Outputs (Pins 3, 13-17, 20) $I_{OH} = 100\mu A$	2.4		V_{DD}	V
V_{OL}	Low Level Logic Outputs (Pins 3, 13-17, 20) $I_{OL} = 1.6mA$	0		+0.4	V
V_{OH}	High Level Logic Outputs (Pins 5, 10)	$V_{DD} - .3(V_{DD} - V_{SS})$		V_{DD}	V
V_{OL}	Low Level Logic Outputs (Pins 5, 10)	V_{SS}		$V_{SS} + .3(V_{DD} - V_{SS})$	V
P_D	Power Dissipation @±5.5V ‡		90	170	mW

A.C. System Specifications: $T_A = 25°C$; $V_{DD} = +5V$; $V_{SS} = -5V$ unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
f_{OSC}	Oscillator Frequency		2.4576		MHz
f_{CO}	Clock Signal Output to Drive S35212A Filter		153.6		KHz
T_{OUT}	Transmit Carrier Output Level into 20KΩ Load (−7.0±1.5dBm)	291	346	411	mVRMS
R_{SENS}	Receive Carrier Input Level	3.0		775	mVRMS

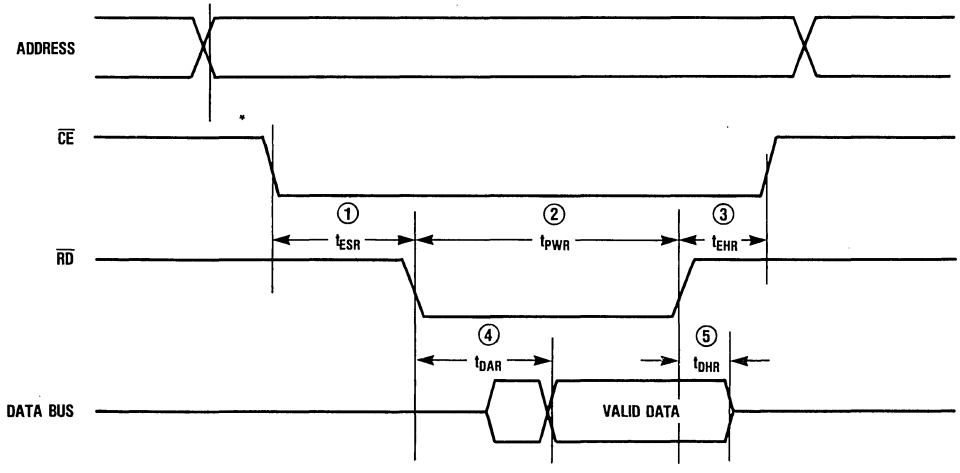
‡ The power consumption is approximately 60% from the positive supply and 40% from the negative supply.

Figure 1. Preliminary Signal Relationships, Serial Data Path, High Speed Mode



μP or μC Interface Timing

Figure 2. Read Timing Characteristics



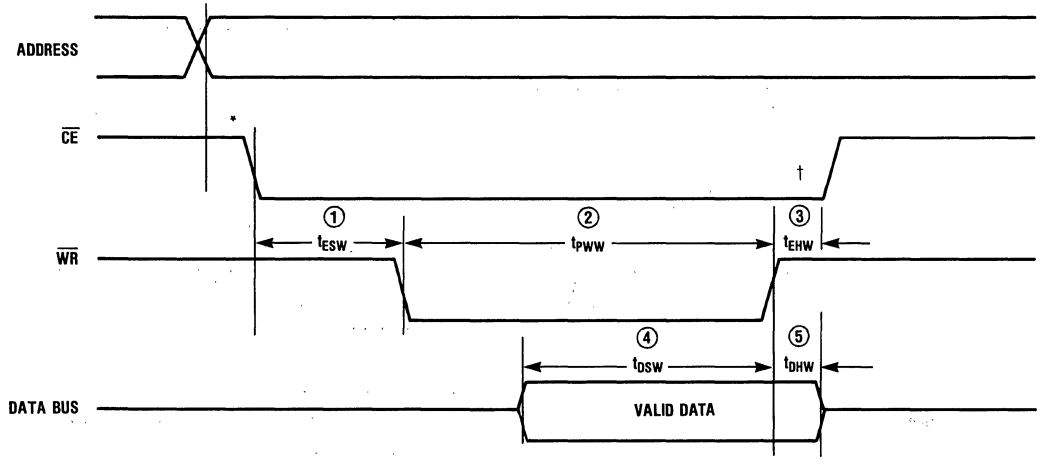
*ADDRESS MAY BE COINCIDENT OR PRIOR TO $\overline{CE}$ GOING LOW.

Read Cycle

Symbol	Parameter	Min.	Max.	Unit
① t_{ESR}	Enable Setup - Read	70		ns
② t_{PWR}	Pulse Width - Read	250		ns
③ t_{EHR}	Enable Hold- Read	0		ns
④ t_{DAR}	Data Access - Read		200	ns
⑤ t_{DHR}	Data Hold - Read	20		ns

μP or μC Interface Timing (Continued)

Figure 3. Write Timing Characteristics



*ADDRESS MAY BE COINCIDENT OR PRIOR TO $\overline{CE}$ GOING LOW.
†DATA WILL LATCH ON THE RISING EDGE OF $\overline{CE}$ OR $\overline{WR}$, WHICHEVER COMES FIRST.

Write Cycle

Symbol	Parameter	Min.	Max.	Unit
① t_{ESW}	Enable Setup - Write	70		ns
② t_{PWW}	Pulse Width - Write	250		ns
③ t_{EHW}	Enable Hold- Write	0		ns
④ t_{DSW}	Data Setup - Write	60		ns
⑤ t_{DHW}	Data Hold - Write	20		ns

S35213 Command Locations [X] Summary Table

Location	Address					Write Commands (All positive true unless otherwise stated)
	A_4	A_3	A_2	A_1	A_0	
0	0	0	0	0	0	Transmit Squelch Control (1 squelches output, 0 allows audio out)
1	0	0	0	0	1	Scrambler Disable (for Remote Digital Loopback)
2	0	0	0	1	0	Force RXD to a Mark
3	0	0	0	1	1	Receive Sync Disable (sets pin 15 to a 1)
4	0	0	1	0	0	Signal Quality Detector Enable (Not characterized)
5	0	0	1	0	1	PLL Lockup Control; Fast/$\overline{\text{Slow}}$
6	0	0	1	1	0	WL1 Data Word Length Control 1
7	0	0	1	1	1	WL0 Data Word Length Control 0
8	0	1	0	0	0	Async Mode/$\overline{\text{Sync Mode}}$
9	0	1	0	0	1	High Speed/$\overline{\text{Low Speed}}$
10	0	1	0	1	0	Slave Mode/$\overline{\text{External Mode}}$ (DTE Clock)[Sync Mode Only]
11	0	1	0	1	1	Local Clock/External Timing (Local if Async)
12	0	1	1	0	0	Answer/$\overline{\text{Originate}}$
13	0	1	1	0	1	Analog Loopback/$\overline{\text{Normal}}$
14	0	1	1	1	0	Digital Loopback/$\overline{\text{Normal}}$
15	0	1	1	1	1	Connect Modulator to Dotting Pattern Generator
16	1	0	0	0	0	Connect Modulator to Mark Generator
17	1	0	0	0	1	Connect Modulator to Space Generator
18	1	0	0	1	0	SRC/$\overline{\text{SP1}}$ Selection of Pin 13 Function
19	1	0	0	1	1	SP1 High/$\overline{\text{Low}}$
20	1	0	1	0	0	STC/$\overline{\text{SP2}}$ Selection of Pin 16 Function
21	1	0	1	0	1	SP2 High/$\overline{\text{Low}}$
22	1	0	1	1	0	SXC/$\overline{\text{SP3}}$ Selection of Pin 17 Function
23	1	0	1	1	1	SP3 High/$\overline{\text{Low}}$
24	1	1	0	0	0	Enter Test Mode 0
25	1	1	0	0	1	Enter Test Mode 1
26	1	1	0	1	0	Enter Test Mode 2
27	1	1	0	1	1	Enter Test Mode 3
28	1	1	1	0	0	Force RXD Open (This is higher priority than location 2 command to force a mark out)
29	1	1	1	0	1	Carrier Valid — Sets Energy Detect Threshold from −43dBm to −48dBm
30	1	1	1	1	0	Reserved
31	1	1	1	1	1	Reserved

Bits Per Word	8	9	10	11
WL 1	0	0	1	1
WL 0	0	1	0	1

Note 1: There is no power-on reset. The controller must perform an initialization routine, particularly to write 0's to the test registers.

S35213 Read Locations (Y)

Location	Address					Read Information
	A_4	A_3	A_2	A_1	A_0	
0	0	0	0	0	0	Energy Detect (1=True, 0=False) 5mSec Time Constant
1	0	0	0	0	1	PSK Demodulator Output
2	0	0	0	1	0	PSK Unscrambled Output
3	0	0	0	1	1	FSK Demodulator Output
4	0	0	1	0	0	Signal Quality Indicator (1=Good, 0=Bad; Is not characterized)

Operation of S35213

The S35213 modem chip was designed to use the S35212A filter, a controller chip, and a dialer chip to serve as either an RS-232 standalone modem or a bus-interfaced modem card for direct plug-in to personal computers.

The chip will do 1200bps asynchronous or synchronous data transmission in a duplex mode over the switched telephone network by using differential phase-shift keying (DPSK) signal. Each phase shift represents two bits of data (called "di-bit" encoding). For a 1200bps data stream this results in a 600 baud symbol rate. In order to provide a relatively uniform energy level and to maintain synchronization the data signals are scrambled before modulation and descrambled after demodulation.

The S35213 contains the PSK modulator/demodulators, the scrambler/descrambler and the synchronous/asynchronous converters mentioned above. Included is a "fallback" mode in case a slow modem or a bad telephone line is encountered. The S35213 can indicate reception of FSK signals and can be operated in the 0 to 300bps FSK mode as a Bell 103 type modem.

Private line protocols as well as the common Bell 212A protocol are available through a flexible command structure. Timing and procedures can be programmed and tailored for specific applications in the controller.

An example of that would be the intitialization routine performed each time the modem is powered on. When the reset command initiated the controller, the controller had to write into locations 0,2,6,7,8,9, 10,etc. to set all the proper functions.

When the $\overline{RI}$ line indicated ringing the DTE would decide whether to answer immediately or after so many rings. After causing $\overline{OH}$ to go low the controller had to turn on the answer tone (a high band FSK mark) by changing locations 0, 9, 12, 16, and others to accomplish the goal of answering. Then location 0 is polled to see if there is carrier detect. As soon as carrier detect is determined the controller will sample locations 2 and 3 to see if the incoming signal is FSK or PSK.

Capability for comprehensive diagnostic functions include Analog Loopback (AL), Digital Loopback (DL) and Remote Digital Loopback (RDL) is incorporated.

Frequency Assignment Table

Standard conventions such as Bell 212A are established to guarantee compatible communications. For Full Duplex operation, modems must be able to transmit and receive simultaneously in the voice frequency channel. For both 300 and 1200bps operation the voice band was separated into high and low band segments. The answering modem transmits in the high band and the originating modem transmits in the low band. The use of high performance filters, such as the Gould S35212A, allows the receive signals to be separated from the transmit signals and demodulated accurately.

Mode		Transmit Frequency (Hz)		Receive Frequency (Hz)	
		Mark	Space	Mark	Space
Bell 103 Originate	0-300bps	1270	1070	2225	2025
Bell 103 Answer	0-300bps	2225	2025	1270	1070
Bell 212 Originate	1200bps	1200		2400	
Bell 212 Answer	1200bps	2400		1200	

Applications Information

With any off-the-shelf 8-bit μC, such as the S6805, a compact and cost-effective 212A modem can be realized. Figure 4 shows how such a modem might be arranged to provide 1200/300bps asynchronous operations with auto-answer and auto-dialing (DTMF & Pulse) with a minimum number of chips. Note that this modem would be able to communicate over the RS-232C link to the DTE (computer) for control functions such as dialing, on-hook/off-hook, speed control (perhaps eliminating CH and CI in the cable) and ring indicate (eliminating CE). Since the functions are all available it becomes an exercise in software to implement the desired features for a particular application.

Figure 4. RS-232 Serial Modem for 1200/300bps Asynchronous Operation/Auto-Answer/Auto-Dial Capability

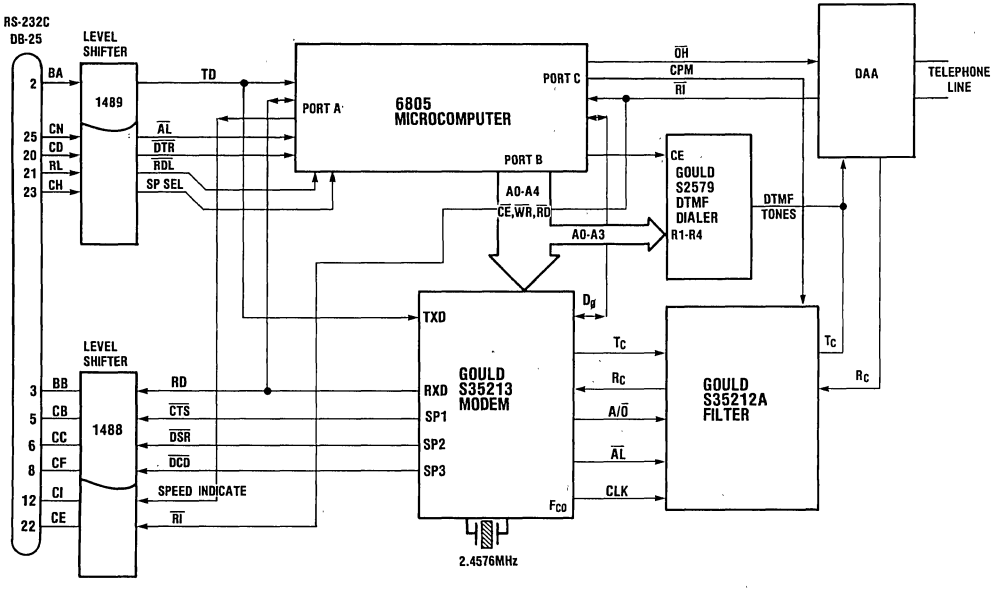


Figure 5 shows an implementation of an intelligent 212A modem with auto-dial, auto-answer, and call progress tone detection capability. The S2579 does the tone dialing function. The controller does the pulse dialing by switching the $\overline{OH}$ (Off Hook) relay line. When $\overline{RI}$ is received from the ring detector circuit in the DAA (Data Access Arrangement) the logic signals the controller to initiate the auto-answer sequence.

During auto-dial or origination sequence the call progress tones (dial tone, busy, ringing, etc.) can be monitored. The S35212A filter will change center frequencies when SEL2 is switched. The high group filter will shift from 2400Hz to 400Hz center frequency, thus passing the 350, 440 and 480Hz tones. By using the energy detector in the S35213, the microcontroller can examine the cadence of the tones to determine status and progress of the call.

The microcomputer (controller) is programmed to handle the modem protocol, perform loopback testing and monitor call progress. It can convert specific terminal controls to appropriate control signals.

This figure illustrates how a parallel interface modem, designed to plug directly into an option slot in a personal computer, might be arranged.

To convert serial data to parallel data for μP bus interface the controller must be able to perform the UART/USRT functions as well as control dual port register files for bus I/O. A variety of controllers such as the MC68121 are available to perform these functions.

Figure 5. 212A Modem System Diagram Auto-Answer/Auto-Dial with μP Bus Interface

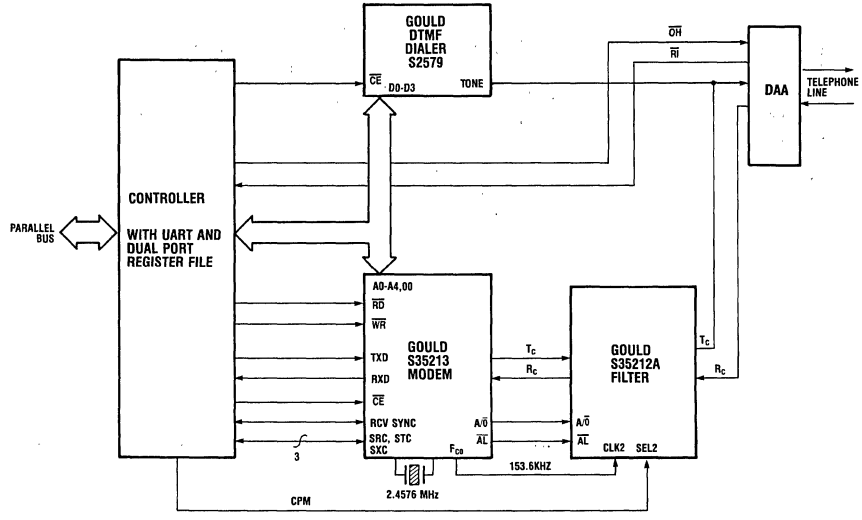
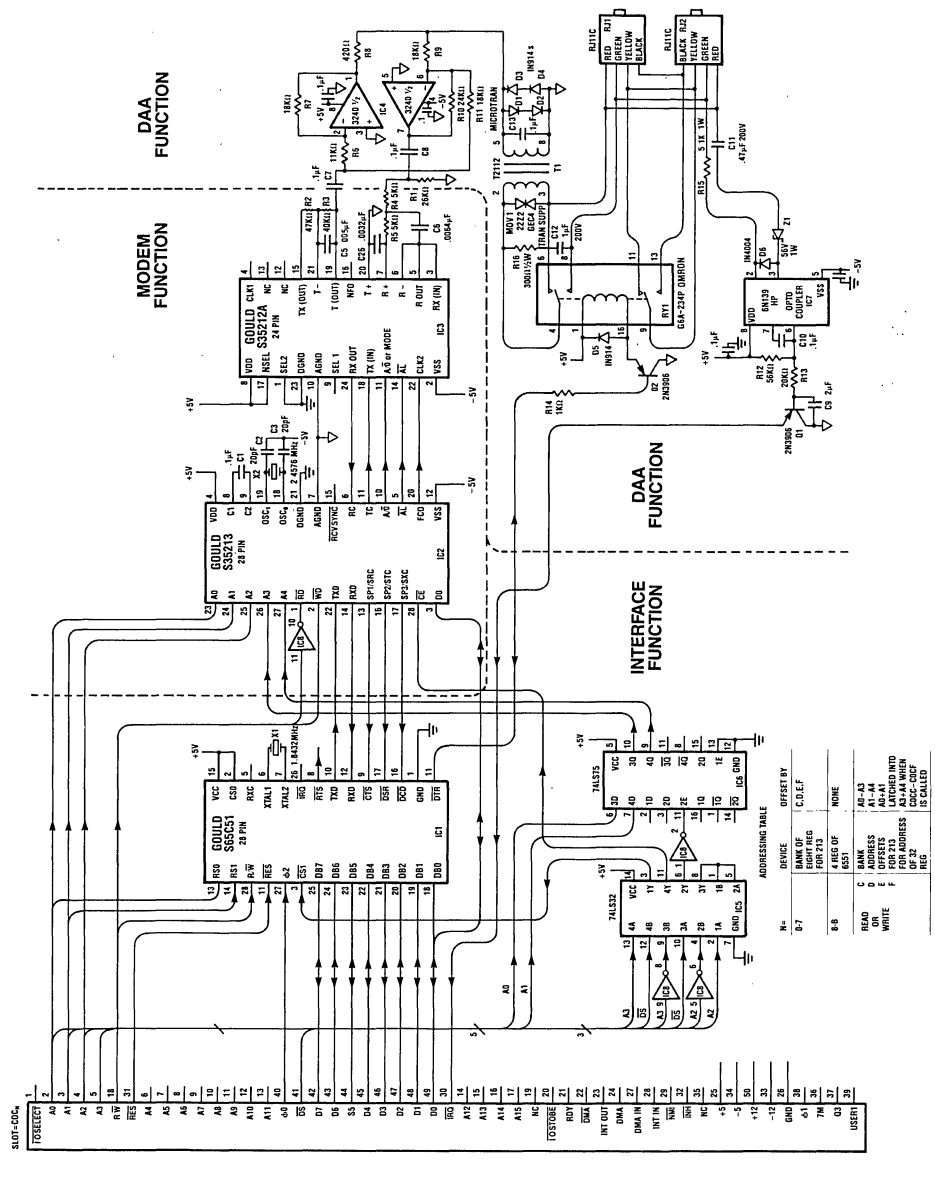


Figure 6. Apple IIE Parallel Interface Example for 1200/300 BPS Asynchronous Operation



Various Reference Documents for MODEM Specifications

Bell System Technical References		
Publication 41101	Feb. 1967	Data Set 103A Interface Specification
Publication 41106	Apr. 1977	Data Sets 103J, 113C, 113D-Type Interface Specification
Publication 41214	Jan. 1978	Data Set 212A Interface Specification
Publication 41008	July 1974	Transmission Parameters Affecting Voiceband Data Transmission — Description of Parameters
Publication 41009	May 1975	Transmission Parameters Affecting Voiceband Data Transmission — Measuring Techniques
Publication 61100		Description of the Analog Voiceband Interface between Bell System Local Exchange Lines and Terminal Equipment.

U.S. Government Printing Office
Title 47 of the Code of Federal Regulations (Telecommunications) Parts 0-19, and Parts 20-69. Part 15 covers EMI/RFI of digital equipment and Part 68 covers telephone interconnect.

Government Printing Office
Washington, D.C. 20402
(202) 783-3238

Bell System Publications: Publishers Data Center
Box C-738
Pratt Street Station
Brooklyn, New York 11205
(212) 834-0170

GOULD

AMI Semiconductors

Bell 103/V.21 Single Chip Modem

Preliminary Data Sheet

S3531

COMMUNI-CATION PRODUCTS

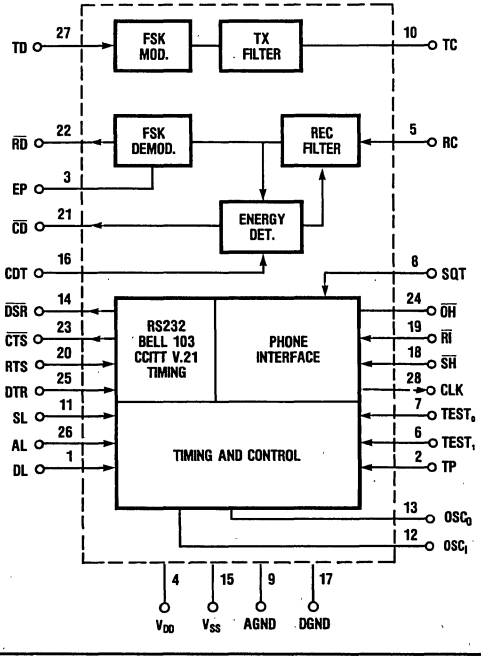
Features

- ☐ Single-Chip 300 bps, Full Duplex, FSK Modem
- ☐ Bell 103/113 and CCITT V.21 Operation (Pin Selectable)
- ☐ Auto Answer/Originate Operating Modes
- ☐ Manual Answer/Originate Modes
- ☐ No External Filtering Required
- ☐ Phase Continuous Transmit Carrier Frequency Switching
- ☐ RS-232 Control Interface
- ☐ Passthrough Mode for Protocol Independence
- ☐ Low Cost 3.58MHz (TV Crystal) Time Base
- ☐ Digital and Analog Loopback Modes
- ☐ UART Clock Output (4.8KHz)
- ☐ V.25 Tone Generation

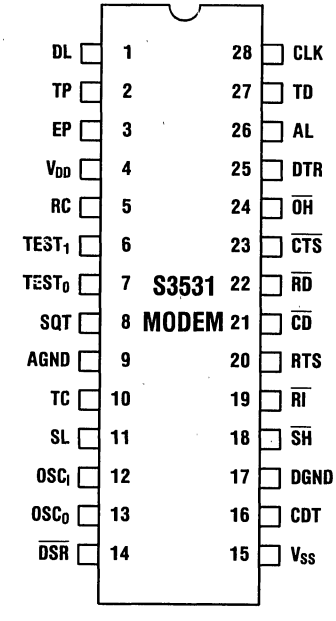
Typical Applications

- ☐ Board Modems for Office Automation Equipment
- ☐ Portable Lap Computers
- ☐ Encrypted Data Stream Modem
- ☐ Password Secure Modem
- ☐ Test Instrument Communications
- ☐ Phone and Modem Combination
- ☐ Smart Vending Machines
- ☐ Alarm Systems

Functional Block Diagram



Pin Configuration



S3531

General Description

The S3531 is a Full Duplex FSK Modem integrated circuit which may be operated in Bell 103/113 or CCITT V.21 applications. The S3531 features transmit and receive filtering; answer/originate mode selections; RS-232 control interface; digital and analog loopback test modes; and generation of both the 4.8KHz UART clock and V.25 Answer Tone. The S3531 is designed for use in stand-alone modem applications and in applications in which the modem function is designed directly into the DTE.

Pin/Function Descriptions

Pin #	Name	Function
1	DL (Digital Loopback)	A high level on this input causes the device to enter the digital loopback mode. In this mode the received data from the remote end is internally looped back to TD and $\overline{DSR}$ is forced high to signal to the DTE that the modem is not ready for transmission. The received data is not available on $\overline{RD}$ during the DL mode.
2	TP (Test Point)	Test Pin. Must be connected to either V_{SS} or V_{DD} for normal operations.
3	EP (Eye Pattern)	Output (analog) of the demodulator prior to slicing. Do not load.
4, 1	V_{DD}, V_{SS}	Positive and negative Power Pins, respectively ($\pm$5V).
5	RC (Receive Carrier)	This analog input is the data carrier received by the data access arrangement from the line. The modem demodulates this signal to generate the receive data bits. A .1μf series capacitor and a 30K pull down resistor is REQUIRED at this input.
6 7	Test 1 Test 0	These are test inputs and must be tied to V_{SS} for normal applications. See table under Passthru Mode.
8	SQT (Squelch Transmitter)	A low level on this input enables (turns on) TC (pin 10). A high level disables (turns off) TC. This pin can be left floating in order to enable TC.
9	AGND	Analog ground (0 Volts).
10	TC (Transmit Carrier)	This analog output is the modulated transmit data carrier. Its frequency depends upon whether the modem is in the answer or originate mode and if a mark or space condition is being sent (Table 1). Typically the output level is at $-$9dBm. (275mVRMS into 10KΩ.)
11	SL (Select)	A high level on this input selects the CCITT V.21 data transmission format. Applying a low level selects the Bell 103 data transmission format.
12 13	OSC_I OSC_O	These are terminals for connecting an external 3.579545MHz TV crystal. All internal clock signals are derived from this time base. Feedback resistor and capacitors are integrated on the chip but additional 20pF caps to V_{SS} from each pin are required.
14	$\overline{DSR}$ (Data Set Ready)	This output, when low, indicates to the data terminal that the modem is ready to transmit data.
16	CDT (Carrier Detect Threshold)	Applying a variable voltage level between 0 and $-$5V at this pin allows control of the recieve carrier detection threshold. This will override the internally determined threshold. If CDT is set to a voltage between +1.5 and +2.0V the AGC will be disabled during the test modes of pins 6 & 7.
17	DGND	Digital ground (0 Volts).
18	$\overline{SH}$ (Switch Hook)	This input is used to manually place the device in the originate mode. The device will make the $\overline{OH}$ output low and start the originate sequence if $\overline{SH}$ input is low ($-$5V) and DTR is on. This can be a level or a momentary low-going pulse input (min. 54msec). A pulse duration of less than 27 msec will not be detected. $\overline{RI}$ should be high if $\overline{SH}$ is to be exercised. Once $\overline{RI}$ has been activated RTS has no effect.

Pin/Function Descriptions (Continued)

Pin #	Name	Function
19	$\overline{RI}$ (Ring Indicator)	This input, when high, permits auto answer capability. The data access arrangements should apply a low level (−5V) to $\overline{RI}$ when a ringing signal is detected. The level should be low for at least 107msec. The input may remain low during data transmission, but must be reset before DTR. Similarly, in manual mode, the answer mode is entered by applying a low level to this input (unless RTS is high).
20	RTS (Request to Send)	A high level on this input with the DTR input in the on condition causes the device to enter the originate mode. $\overline{OH}$ will go low to seize the phone line. Auto dialing can be performed by turning the RTS input on and off to effect dial pulsing. This input must remain high for the duration of data transmission. (Auto answer will **not** function if RTS is high). RTS should follow DTR by no less than 1msec.
21	$\overline{CD}$ (Carrier Detect)	This output goes to a low level to indicate that the receive data carrier has been received at a level of −43dBm. It turns off if the received data carrier falls below the carrier detection threshold of −48dBm [Both values are ±2dB].
22	$\overline{RD}$ (Received Data)	The device presents data bits demodulated from the received data carrier at this output. This output is forced high if the DTR input or the carrier detect output is off.
23	$\overline{CTS}$ (Clear to Send)	This output goes to a low level at the completion of the handshaking sequence and turns off when the modem disconnects. It is always turned off if the device is in the digital loopback mode. Data to be transmitted should not be applied at the TD input until this output turns on.
24	$\overline{OH}$ (Off Hook)	This output goes to a low level when either the $\overline{SH}$ or the RTS input is on in the originate mode and when a valid ring signal is detected on the $\overline{RI}$ input in the answer mode. This output is off if DTR is off or if the disconnect sequence has been completed.
25	DTR (Data Terminal Ready)	A high level on this input enables all the other inputs and outputs and must be present before the device will enter the data mode either manually or automatically. The device will enter an irreversible disconnect sequence if the input is turned off (low level) for more than 14msec during a data call. A pulse duration of less than 6msec will not be detected. To reset the chip before each call, this pin should be held low for greater than 14msec.
26	AL (Analog Loopback)	This input allows the data terminal to make the telephone line busy (off hook) and implement the analog loopback mode. A high level on this input while DTR is high causes the device to make the $\overline{OH}$ output low and to enter the analog loopback mode. The receive filter center frequency is switched to correspond to the transmit filter center frequency and the transmit data carrier output is internally connected to the receive data carrier input as well as being available at TC.
27	TD (Transmit Data)	Data bits to be transmitted are presented to this input serially by the data terminal. A high level is considered a binary '1' or MARK and a low level is considered a binary '0' or SPACE. The data terminal should hold this input in the MARK state when data is not being transmitted. During handshaking this input is ignored.
28	CLK (Clock)	A 4.8KHz LSTTL compatible square wave output is provided for supplying the 16X clock signal required by a UART for 300 bits/sec. data rate. This output facilitates the integration of the modem function in the data terminal.

S3531

Absolute Maximum Ratings

Supply Voltage ($V_{DD} - V_{SS}$) ..... +12.0V
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Power Dissipation ..... $V_{SS} - 0.3V \leq V_{IN} \leq V_{DD} + 0.3V$

D.C. Electrical Operating Characteristics: T_A = 0°C to +70°C; (V_{DD}−V_{SS}) = 10V; ±5% (±5.0V)

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{DD}	Positive Supply Voltage (ref. to DGND, AGND; both at 0V)	+4.75	+5.0	+5.25	VDC
V_{SS}	Negative Supply Voltage (ref. to DGND, AGND)	−4.75	−5.0	−5.25	VDC
P_D	Power Dissipation, Operating (@±5V)		110	200	mW
R_{IN}	Input Resistance	8			MΩ
C_{IN}	Input Capacitance			15	pF

Analog Signal Parameters: T_A = 0°C to 70°C; ±5 VDC. f_{osc} = 3.58MHz

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
f_{osc}	Oscillator Frequency		3.579545 ±0.02%		MHz
f_t	Transmit Frequency Tolerance		±1.2		Hz
t_D	Transmit 2nd Harmonic Attenuation with respect to Carrier Level		50		dB
T_{OUT}	Transmit Output Level into 10KΩ min., 25pF max.	245	275 (−9dBm)	308	mVRMS
	Carrier Input Range (CDT open)	−48 ±2		−6	dBm
DNR	Dynamic Range (CDT open)		42		dB
	Bit Jitter (Input = −30dBm) Bit Bias Bias Distortion		100 1 3		μSec % %
Carrier Detect Trip Points	Off to On On to Off		−43 −48		dBM dBM
Hysteresis			3		dBM

Signal Input and Output Compatibility Table

Pin Name	No.	Input	Output	Voltage Level Low (Max.)	Voltage Level High (Min.)	Logic Family Compatibility	I_{OL} Milliamps	I_{OH} Milliamps
$\overline{SH}$	18	X		−3	+3	CMOS		
$\overline{RI}$	19	X		−3	+3	CMOS		
$TEST_0$	7	X		−3	+3	CMOS		
$TEST_1$	6	X		−3	+3	CMOS		
SQT	8	X		+1	+4	CMOS		
$\overline{OH}$	24		X	+0.4	+2.4	LSTTL	0.4	0.02
CLK	28		X	+0.4	+2.4	LSTTL	0.4	0.02
$\overline{CD}$	21		X	+0.4	+2.4	LSTTL	0.4	0.02
$\overline{RD}$	22		X	+0.4	+2.4	TTL	1.6	0.4
$\overline{CTS}$	23		X	+0.4	+2.4	TTL	1.6	0.4

Signal Input and Output Compatibility Table (Continued)

Pin Name	No.	Input	Output	Voltage Level Low (Max.)	Voltage Level High (Min.)	Logic Family Compatibility	I_{OL} Milliamps	I_{OH} Milliamps
$\overline{DSR}$	14		X	+0.4	+2.4	LSTTL	0.4	0.02
RTS	20	X		+0.8	+2.0	TTL*		
TD	27	X		+0.8	+2.0	TTL*		
DTR	25	X		+0.8	+2.0	TTL*		
AL	26	X		+0.8	+2.0	TTL*		
DL	1	X		+0.8	+2.0	TTL*		
SL	11	X		+0.8	+2.0	TTL*		

*These inputs are high impedance CMOS inputs that respond to TTL voltage levels.

What is a 300 Baud Modem and What Does It Do?

A modem acts like a translator between a computer and the telephone system. Computers work with data in the form of binary pulses but telephones were designed to transmit analog audio waveforms. The modem converts binary data from the computer into analog signals that the phone lines can carry. In the receive mode the modem demodulates the analog signals from the phone line, converting them back to binary form for the computer.

300 Baud modems are among the most common data communications devices in use today. Modems are used for exchanging information between home computers, personal computers, banks, offices and mainframes to name just a few posible applications. 300 Baud modems are used anywhere that a normal telephone line exists. Modems based on the S3531 have the advantages of full duplex operation using either BELL 103 or CCITT V.21 Protocols, a built-in interface to the industry standard RS232 serial data port, very low system part count, and low power CMOS single chip construction.

Both BELL 103 and CCITT V.21 modems use FSK modulation for data transmission over standard phone lines. FSK modulation simply means Frequency Shift Keying or the transmission of frequency "A" for binary "1" and frequency "B" for binary "0". Full duplex FSK occurs when two-way transmission happens simultaneously between two modems.

A simple protocol exists to prohibit both the originating modem and the answering modem from transmitting simultaneously on the same frequency.

Figure 1. Frequency Modulation (FSK)

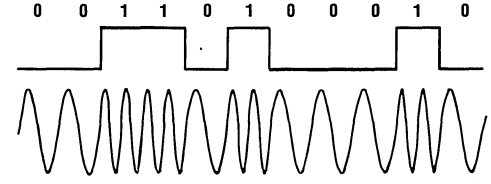
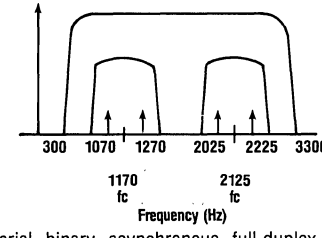
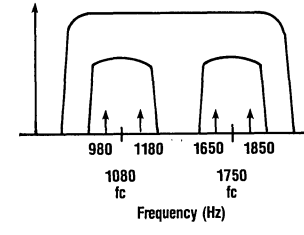


Figure 2. Full Duplex, 300 bps, Bell 103



Data: Serial, binary, asynchronous, full duplex
Data Transfer Rate: 0 to 300 bps
Modulation: Frequency shift-keyed (FSK) FM

Figure 3. Full Duplex, 300 bps, CCITT V.21



The protocol breaks the telephone frequency spectrum into two bands; a high band, and a low band. Each band has its own mark frequency corresponding to a binary 1 and its own space frequency corresponding to a binary 0, for a total of four transmitting frequencies. The protocol states that the originating modem must transmit on the low band and receive on the high band while the answering modem must transmit on the high band and receive on the low band.

Obviously the ability of a modem to separate the high band from the low band is important for correct decoding of the transmitted data. Figures 4, 5, 6, and 7 of the S3531 transmit and receive filters show a sharp 20 db cutoff within just a few hundred Hertz of the edges of the high and low bands.

Block Description

The block diagram of the FSK Modem is shown on page 1. The input to the modulator is the TD (Transmit Data) signal, which is the digital data to be converted to analog form. This input would typically be provided by the RS-232 interface or a UART. The modulator generates a square wave whose frequency is shifted in response to the Transmit Data input.

Figure 4. Transmit Filter Bell 103

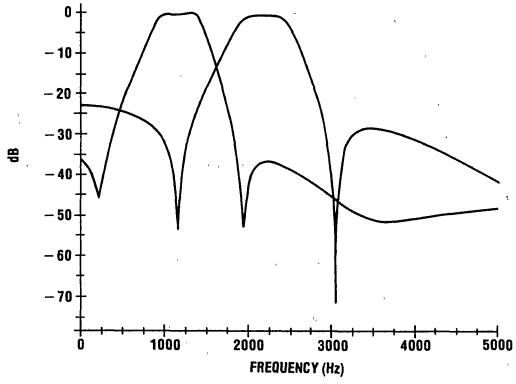


Figure 5. Transmit Filter V.21

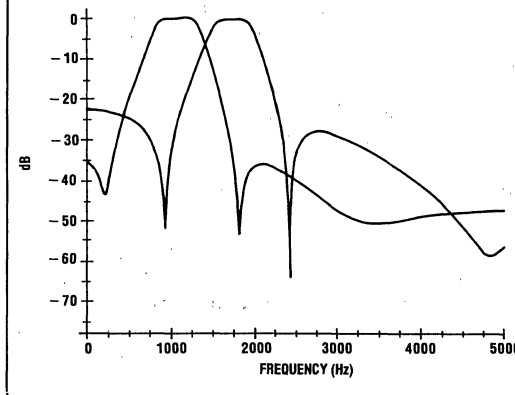


Figure 6. Receive Filter Bell 103

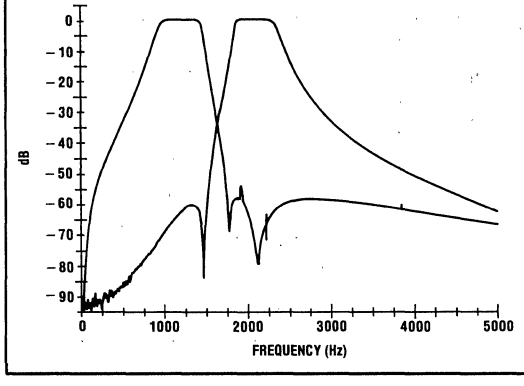
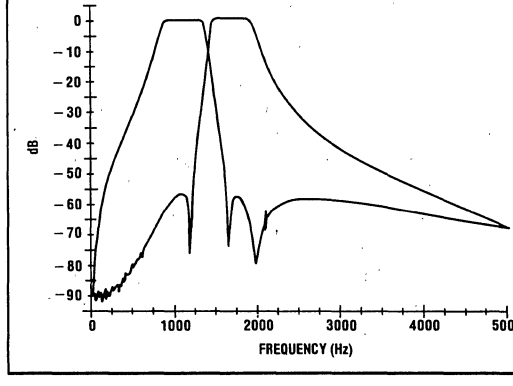


Figure 7. Receive Filter V.21



The transmit filter outputs a Frequency Shift Keying signal at the TC (Transmit Carrier) output. The frequency of the FSK signal corresponds to the fundamental frequency of the square wave at the input of the filter.

The transmit carrier TC can be enabled and disabled by the SQT control input. A low level on this pin enables (turns on) TC, and a high level disables (turns off) TC.

On the receive side, the receive filter whose input is the Receive Carrier, rejects the adjacent channel energy and improves the Signal to Noise Ratio of the received signal.

The output of the receive filter is fed into the demodulator where the data is converted back into digital form.

The next block is the energy detect circuit. It detects energy levels at which reception and demodulation of data is considered reliable, controlling the $\overline{CD}$ signal.

The last block is the timing control and handshake logic, which besides controlling all the other blocks, also implements the RS-232 interface protocol and controls the BELL 103 and CCITT V.21 operations.

Transmit Filter

The function of the transmit filter is to produce an FSK signal from the phase continuous, frequency shifted, square wave input.

The prime objective of the transmit filter is to pass the square wave fundamental component while attenuating its harmonics. These harmonics could be located in the receive band. Unless attenuated by the transmit filter, they would be coupled back through the hybrid, unattenuated by the receive filter, thus causing degradation of bit error rate.

The transmit filter was designed to have a zero at the third harmonic of the square wave, to alleviate the above problem.

The second objective of the transmit filter is to attenuate the out of band energy. This is necessary since the modulation process produces energy over a broad spectrum and not just at the mark/space frequencies. The fundamental component is attenuated by 24 dB to produce a signal at −9 dBm at the TC (Transmit Carrier) output.

Receive Filter

The measured frequency response of the receive filter is shown in Figures 6 and 7. The receive filter rejects out-of-band noise so that the filtered signal can be demodulated with a resultant low bit error rate.

The filter was designed to reject the adjacent channel energy by 60dB. This is essential since that channel is used for carrier transmission which is coupled back, through the hybrid and into the receive section. Unless attenuated by the receive filter, this component would corrupt the demodulated data and result in excessive bit error rate. The filter was also designed to minimize group delay distortion between the mark and space frequencies. The band width of the filter is 500Hz and is centered around the center frequency of the received carrier.

The dynamic range of the receive signal is 42dB due to the automatic gain control circuit employed.

Timing Control

The chip also incorporates a 14 second abort timer. This is necessary for automatic operation. When a call is automatically originated, and the remote device is busy, then the originating device waits for 14 seconds and hangs up. On the other hand, if the modem is called by mistake it will hang up in 14 seconds, unless the appropriate carrier is received.

Clock Crystal

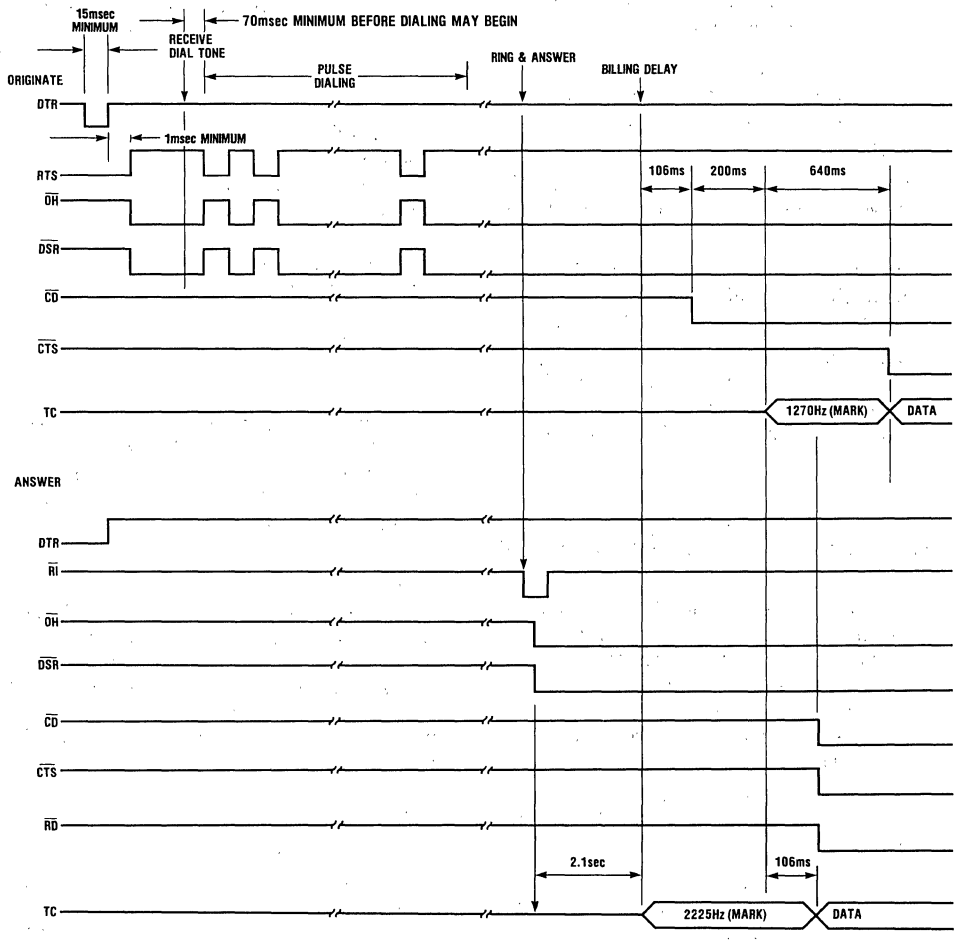
The S3531 uses the popular low-cost 3.58MHz crystal. This crystal is very popular because it is used in all NTSC color TVs and in many low cost personal computers (which require the 3.58MHz to interface with TV monitors). The S3531 can therefore use the same system clock as the display interface to reduce system costs.

Operation

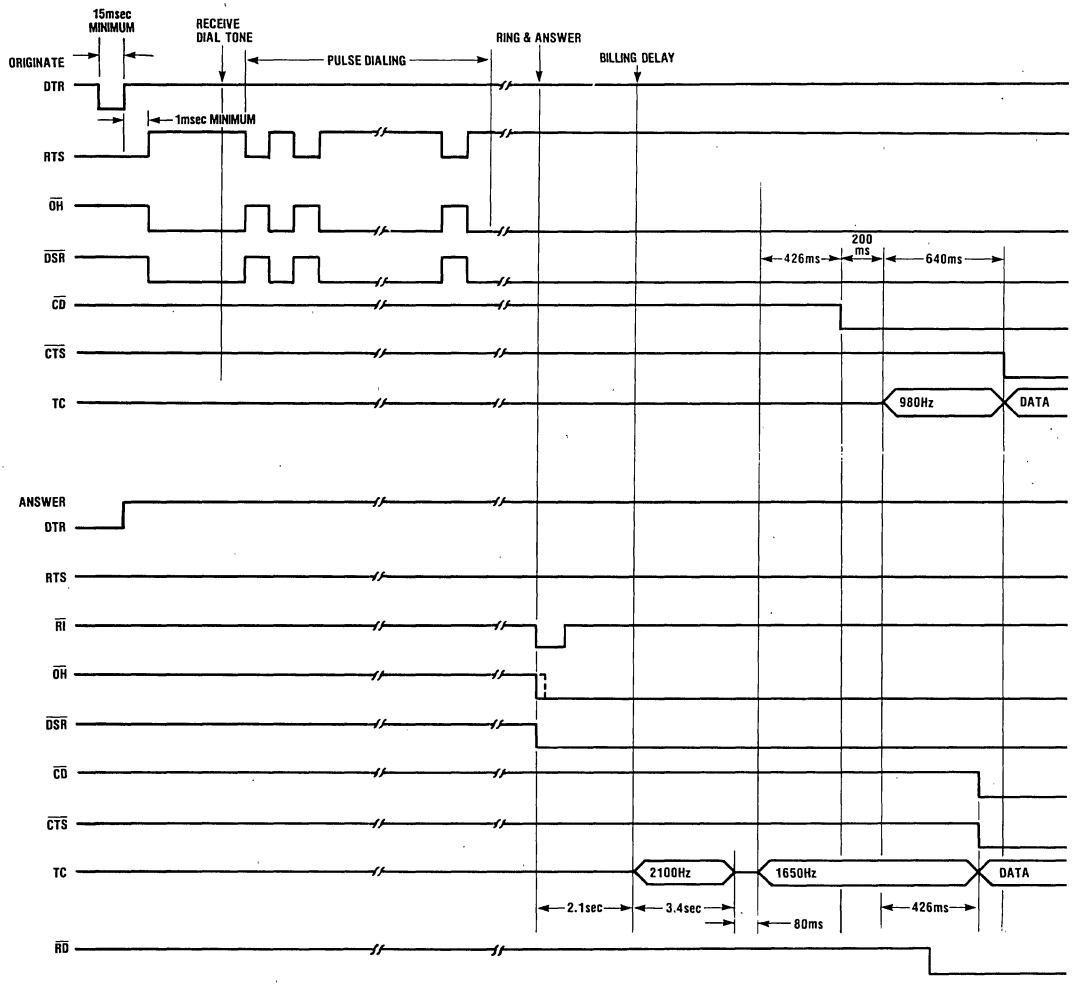
A. Answer Mode

In the answer mode the S3531 stands idle waiting for an incoming call. With DTR high, a low from the ring detector to $\overline{RI}$ causes the S3531 to set $\overline{OH}$ and $\overline{DSR}$ low enabling the hookswitch relay and connecting the modem to the phone line. After 2.1 seconds the S3531 sends a carrier at 2225Hz (mark) to the Originate Modem. If 1270Hz (mark) is returned the S3531 carrier

S3531 Modem Timing Chart for 103 Operating Mode



S3531 Modem Timing Chart for V.21 Operating Mode



detect circuit turns on within 106msec, setting $\overline{CD}$ and $\overline{CTS}$ low indicating completion of the handshaking sequence. Data can then be sent and received.

Originate Mode

In the originate mode with DTR high, a call is initiated by applying a high to the RTS input in auto mode or a negative or low pulse to $\overline{SH}$ in manual mode. This will cause $\overline{OH}$ to go low, enabling the hookswitch relay and connecting the phone line. When dial tone is detected, RTS can be pulsed off to provide dial pulses*. The $\overline{OH}$ will follow the RTS pulses, sending the desired digits over the line. When the answering modem comes on line it will wait 2.1 seconds ("billing delay") and then send the 2225Hz answer tone. 106msec later the $\overline{CD}$ pin will go low indicating carrier received. 190msec later the S3531 will respond with 640msec of 1270Hz. At the end of that time $\overline{CTS}$ will go low indicating to the terminal side that the communications link has been established.

Abort Mode

There is an automatic abort feature in the S3531 to avoid tying up a system when there is difficulty establishing a link. If no carrier is detected within 14 seconds of being put into the answer or originate mode it will abort the call by turning off $\overline{OH}$ and disconnecting the phone line. $\overline{DSR}$ will also go off (high). This abort time can be extended by pulsing RTS low for 1msec before the 14 seconds have elapsed. This will reset the abort timer. If time does run out DTR should be pulsed off to reset the S3531.

Shutdown Mode

Should the received carrier fall below −48 dBm (approx.) during data exchange for more than 213msec the S3531 will terminate the call and go on hook, disconnecting the phone line.

Reset Protocol

By insuring that all control inputs are in their inactive states a minimum of 2msec before the rising edge of DTR, the S3531 will be properly reset.

Manual Operation

The S3531 can be operated manually as well as automatically. With DTR enabled (high) a negative pulse (−5V) of >107msec on $\overline{RI}$ will put the device in the Answer Mode. Similarly (with DTR high) $\overline{SH}$ can be pulled low for >54msec to put the S3531 into the Originate Mode.

Passthru Mode

With the "Test 0" and "Test 1" lines the S3531 can be put into the Passthru Mode disabling the handshake protocol. The transmit and receive functions are enabled but become independent of timing and control. $\overline{CD}$ works as usual and the Answer and Originate Modes are selected manually with $\overline{RI}$ and $\overline{SH}$.

Test 0 PIN 7	Test 1 PIN 6	S3531 STATUS	1 = +5V (V_{DD}) 0 = −5V (V_{SS})
0	0	NORMAL	
1	0	PASSTHRU	

V.21 Mode, CCITT Operation

With the SL pin tied high the S3531 functions in the CCITT V.21 Mode but performs the same operations described above. The basic principle is the same but the frequencies and the timings are switched to V.21 specifications. When in V.21 Mode the V.25 answer tone of 2100Hz will be generated upon answering. See the timing charts and Table 1 for additional details.

Diagnostic Modes

The S3531 has two diagnostic modes for either local or remote testing. By putting the AL pin high while DTR is high, the device enters the Analog Loopback Mode. $\overline{OH}$ goes low to busy out the phone line. The receive filter center frequency is switched to the transmit

Table 1. 103/V.21 Mark and Space Frequencies

Mode	Transmit Frequency (Hz)		Receive Frequency (Hz)	
	Mark	Space	Mark	Space
Bell 103 Originate	1270	1070	2225	2025
Bell 103 Answer	2225	2025	1270	1070
CCITT V.21 Originate	980	1180	1650	1850
CCITT V.21 Answer	1650	1850	980	1180
CCITT V.25 Answer Tone	2100		N/A	

*(Note that OH only follows RTS. The proper timing for dialing must come from the terminal on the RTS line.)

center frequency and the TC signal is internally connected to the RC input. The transmit signal also remains available on the TC pin. Thus any digital data input at TD is coded and sent out via TC, and at the same time back through the analog input, decoded, and out on the $\overline{RD}$ pin.

By putting the DL pin high the S3531 enters the Digital Loopback mode. In this mode any data received from the remote end of the phone line is retransmitted back to its source and $\overline{DSR}$ is forced high. The digital or decoded data is not available at the $\overline{RD}$ output in this mode. See Table 2.

Table 2. Control Logic During Diagnostic Modes

Test Mode			Status Lines			
	DTR	RTS	$\overline{DSR}$	$\overline{OH}$	$\overline{CTS}$	$\overline{CD}$
AL	On	On	On	On	On	On
DL	On	On	Off	On	Off	Off

To establish diagnostic modes in either originate or answer, establish handshaking in the preferred mode (originate or answer), then enter diagnostic modes.

Oscillator Details

Quartz Crystal Specification (25°C ±2°C)	
Operating Temperature Range	0°C to +70°C
Frequency	3.579545MHz
Frequency Calibration Tolerance	.02±%
Load Capacitance	18pF
Effective Series Resistance	180 Ohms, max.
Drive Level-Correlation/Operating	2mW
Shunt Capacitance	7pF, max.
Oscillation Mode	Fundamental

External Drive Requirements

To use an external 3.58MHz clock a TTL level, 50% duty cycle, square wave can be applied to pin 12, OSC_O through a .1μF capacitor. It must have a 2V P-P amplitude and be AC coupled through the .1μF capacitor.

Applications Circuits

Two applications circuits are illustrated. The first circuit is for a stand-alone RS-232 interface modem to be used as a peripheral accessory to a terminal or computer. Plugging into an RS-232 serial port on one side and into a standard modular phone jack on the other side it is a stand-alone direct connect modem for operation at rates up to 300bps.

The second circuit is an add-on modem for building into a computer and connecting to the internal parallel buss structure. The ACIA or UART does the parallel-to-serial and serial-to-parallel conversion required. The edge connector is numbered for an Apple II application but the same interface applies to most μP systems.

Both circuits are intended for direct connection to the phone lines. This requires meeting FCC Part 68 requirements for network protection as well as protection of the modem. No suppression components are illustrated on these examples as the design of the interface will vary depending on the needs of the designer. After a design is completed it must be subjected to Part 68 certification before sale to the public.

If one wants to avoid the protection/certification details a certified DAA (Data Access Arrangement) such as the Cermetek CH1810 can be used instead. The DAA is designed to handle the phone line interface including the 4-wire to 2-wire function and is already registered with the FCC.

Whether using a DAA or not, the S3531 requires very few external components.

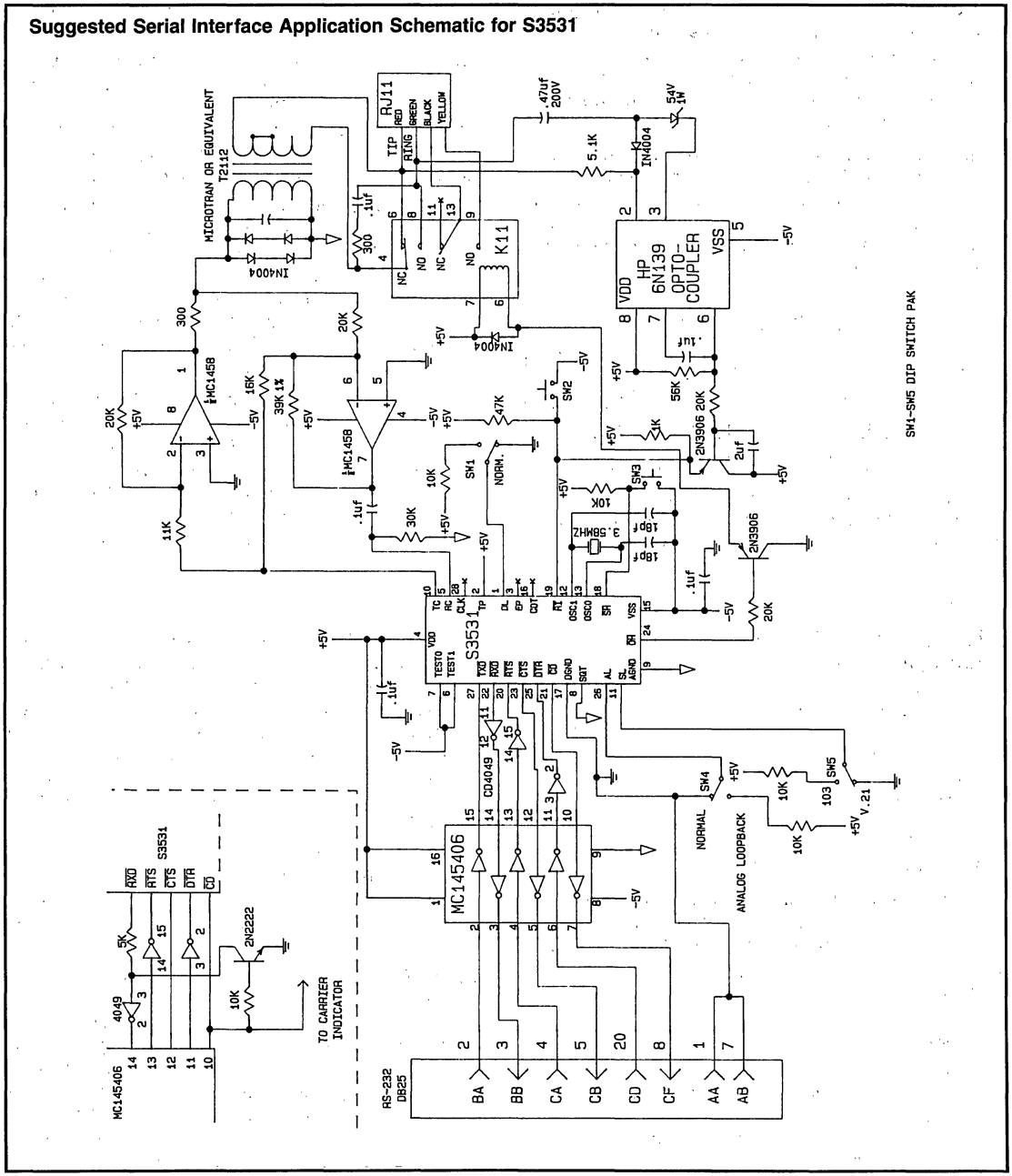
Hybrid Function

In the stand-alone circuit the hybrid 4-wire to 2-wire converter utilizing the dual op amp was configured to provide 1:1 conversion in each direction. A −9dBm voltage level from the Transmit Carrier pin on the S3531 is amplified by the op amp to compensate for the losses in the 300Ω matching resistor and the coupling transformer. The transmit carrier is delivered to the line at −9dBm. (For CCITT applications this should be reduced to −13dBm.)

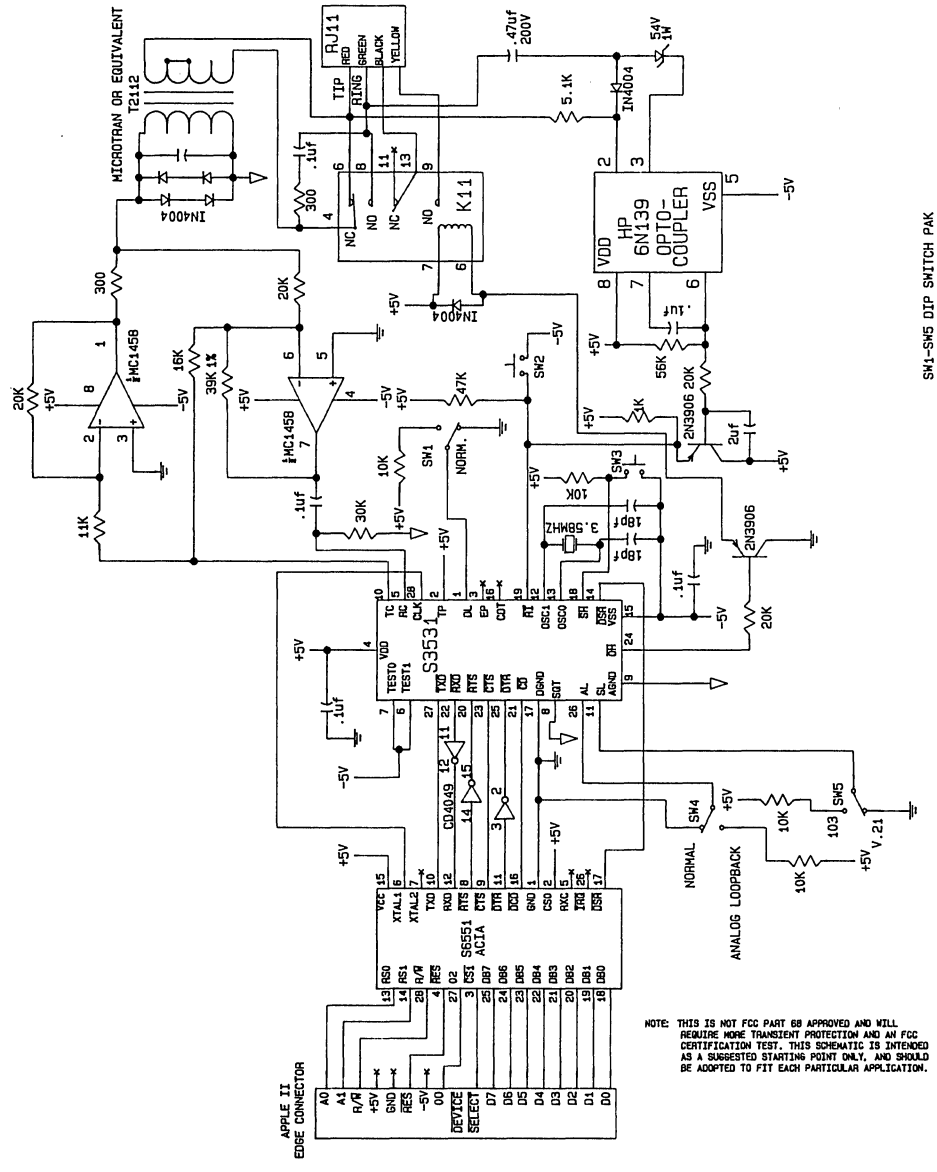
In the receive direction the loss in the coupling transformer is compensated for by the other half of the op amp. If there is a −20dBm signal across Tip and Ring then a −20dBm signal is delivered to the Receive Carrier pin on the S3531.

The 300Ω resistor is to provide the proper termination so that Tip and Ring look like a 600Ω AC impedance to the line. The 16KΩ resistor from the Transmit Carrier pin to the inverting input of the receive op amp is to provide sidetone suppression. The transmit carrier is provided through the 16KΩ resistor 180° out of phase from the transmit carrier presented to the line. Thus, the transmit carrier is cancelled and presented to the Recieve Carrier pin on the S3531 at a reduced level.

Suggested Serial Interface Application Schematic for S3531



Suggested Parallel Interface Application Schematic for S3531 and Apple II



Under ideal conditions 20dB or more of cancellation might be achieved, but because telephone lines vary considerably, a cancellation of around 10dB is a more realistic number.

The transformer listed is rated to 90mA loop current. To go to the maximum loop current the Microtran number would be T5115 for 120mA loop current capability. The DC resistance may be slightly different and various components may need to be adjusted to retain the necessary AC and DC specifications. The T2112 is much smaller and lighter because the low end frequency response is not needed. It is a modem transformer, not a voice transformer.

NOTE once again, that only minimal transient protection is illustrated in these examples, This must be added to meet the needs of the application and the FCC Part 68 requirements.

Modem Glossary

Analog Loopback — A diagnostic test for the entire internal signal path of the modem chip. The transmitted analog output is internally connected to the analog input.

Asynchronous — A scheme for transmitting data on a character-by-character basis without a synchronizing clock signal. In general the asynchronous protocol includes a start bit to identify the beginning of a character, the data bits, and stop bit(s).

Bandwidth — The frequency range of a communications channel. Normal phone lines have a bandwidth of 3000Hz for voice, from 300Hz to 3300Hz.

BPS — The speed at which a modem can transmit or receive data, measured in bits per second. 300 bps is roughly equal to 300 words per minute.

Bias Distortion — Distortion such that the actual mark and space bits are not of equal time duration, thus causing a deviation from the expected 50% duty cycle.

CCITT — International Telegraph and Telephone Consultative Committee. An organization for developing communication system standards. The European equivalent of BELL standards.

Data Distortion — Bit bias distortion occurs when the width of bits received are not equivalent for both a logic one and a logic zero. Bit bias is easily measured as it shows up as a deviation in average voltage. In a normal data stream of alternating ones and zeros the average voltage is zero. However when bit bias destortion is present the duty cycle is not exactly 50% and hence the average voltage is not zero. Excessive bit bias will lead to quality degradation as system UARTs deserialize data correctly only when bit bias distortion is low.

Bit jitter distortion is also important for proper operation of all modems. Bit jitter occurs when the actual center of the data bit drifts around the theoretical center. Again, this is important to the proper operation of a modem because UARTs only deserialize data correctly when bit jitter distortion is low. Jitter distortion is important in all asynchronous serial data systems because the edges of the data bits are used to reconstruct all timing information.

DAA — Data Access Arrangement. An FCC registered device necessary for correctly connecting a device to the switched telephone network. Refer to Part 68 of the FCC's regulations.

DCE — Data Communication Equipment. Modem or any other equipment necessary for the transmission and reception of data between computers and terminals.

Digital Loopback — A diagnostic test for the entire phone line and remote modem. The remote modem's digital output to the DTE is connected to the digital input from the DTE and fed back to the transmitting modem.

Direct Connect Modems — Modems that contain a DAA rather than requiring an acoustic coupler or a tie-in to a phone handset mouthpiece.

DTE — Data Terminal Equipment. The digital equipment that attaches to a modem as the end of the data path. Usually a terminal or a computer.

FSK — Frequency Shift Keying. A modulation method which varies the carrier frequency to correspond with the binary signals to be transmitted.

Full Duplex — Simultaneous two-way communication (transmission and reception) between two computers or modems.

Off-Hook — Connected to the telephone line.

RS232C — A serial communications interface defined by the Electronic Industries Association. Frequently used to connect stand-alone modems to personal computers.

GOULD
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2600Hz Digital Frequency Detector

S3524A

Features

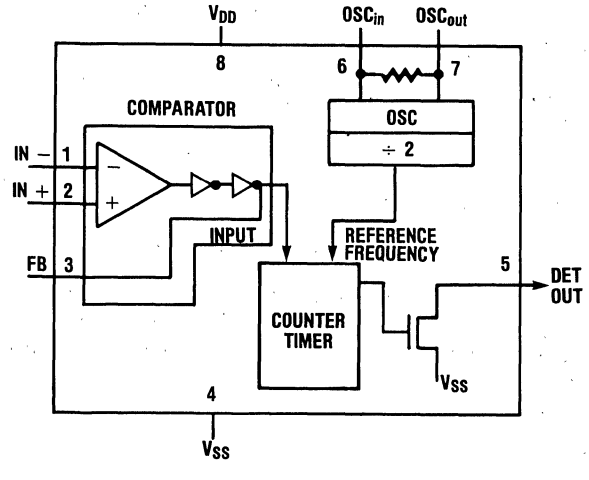
- 2600Hz Center Frequency With 70Hz Bandwidth.
- Small 8-Pin Minidip Package
- Operation From a Low Cost 3.58MHz TV Colorburst Crystal or External Clock
- Input Comparator for Squaring and Sensitivity Adjustment
- Low Power CMOS Technology

Description

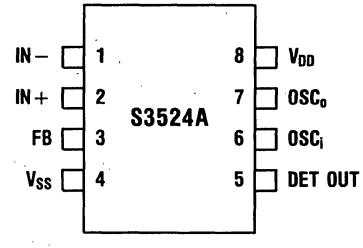
The S3524 is a digital Frequency Detector used to accurately determine if an incoming tone is within a set of predefined limit frequencies. It checks every period of the incoming signal, giving a true output for each period falling within the desired bandwidth.

The S3524A, using a 3.58 MHz clock, will detect a 2600Hz frequency within 70Hz bandwidth. It is primarily designed to follow the S3526B 2600Hz bandpass filter as shown in Figure 4.

Block Diagram



Pin Configuration



S3524A

Absolute Maximum Ratings

Supply Voltage (V_{DD}-V_{SS})	±15V
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +150°C
Analog Input	$V_{SS} - 0.3V \leq V_{IN} \leq V_{DD} + 0.3V$

DC Electrical Operating Characteristics: T_A = 0°C to +70°C

Symbol	Parameter Conditions	Min.	Typ.	Max.	Units
V_{DD}	Positive Supply (Ref. to GND)	4.75	5	5.25	V
V_{SS}	Negative Supply (Ref. to GND)	−4.75	−5	−5.25	V
PD	Power Dissipation			100	mW
V_{IN}	Input Signal Level	43			mV (RMS)
R_O	Load Resistance	6			k Ω

Pin Description

Name	Number	Description
V_{DD}	8	Positive Power Supply. Typically +5V.
V_{SS}	4	Negative Power Supply. Typically −5V.
IN−	1	Input comparator for setting sensitivity and squaring of analog signals. Signal sensitivity is controlled by selecting external resistors,
IN+	2	
FB	3	
DET OUT	5	The detector output. Open drain type output for ease of interface. DET OUT will be high after one full cycle of valid signal is detected, and will remain high until an out of frequency cycle is detected.
OSC IN	6	Oscillator terminals for 3.58MHz reference crystal or clock. Uses standard TV crystal or a rail-to-rail CMOS clock may be used.
OSC OUT	7	

Operation and Applications Information

Figure 1.

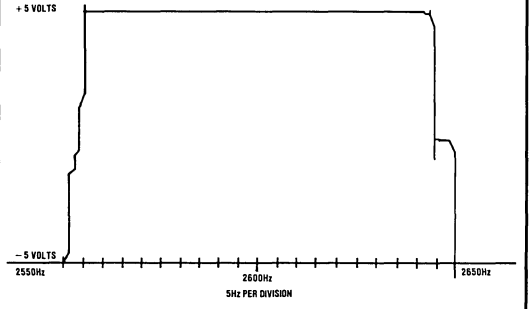


Figure 2. Representative Circuit

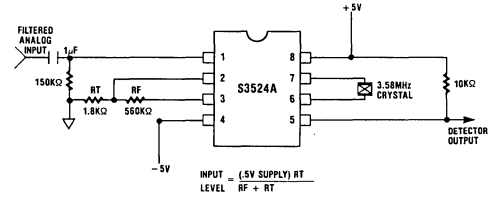
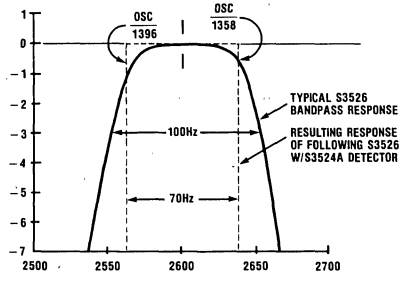


Figure 3. Effective Response of S3526 Bandpass Filter Followed by S3524A Digital Detector



IN SINGLE SUPPLY SITUATION THE GROUND FOR THE SENSITIVITY ADJUSTMENT WOULD BE 1/2 (V_{DD}-V_{SS}) AS DETERMINED BY A REGULATOR OR RESISTIVE VOLTAGE DIVIDER. OFFSET COMPENSATION WOULD BE DONE BY VARYING THE HALF VOLTAGE POINT SLIGHTLY IF DESIRED.

Figure 5. A Typical Detection Bandwidth 2600 for Application Circuit in Figure 4 at 10V

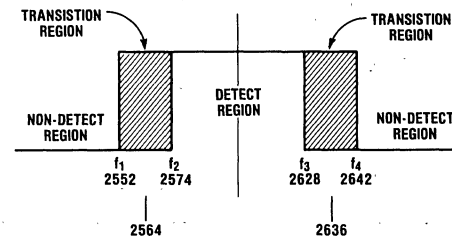
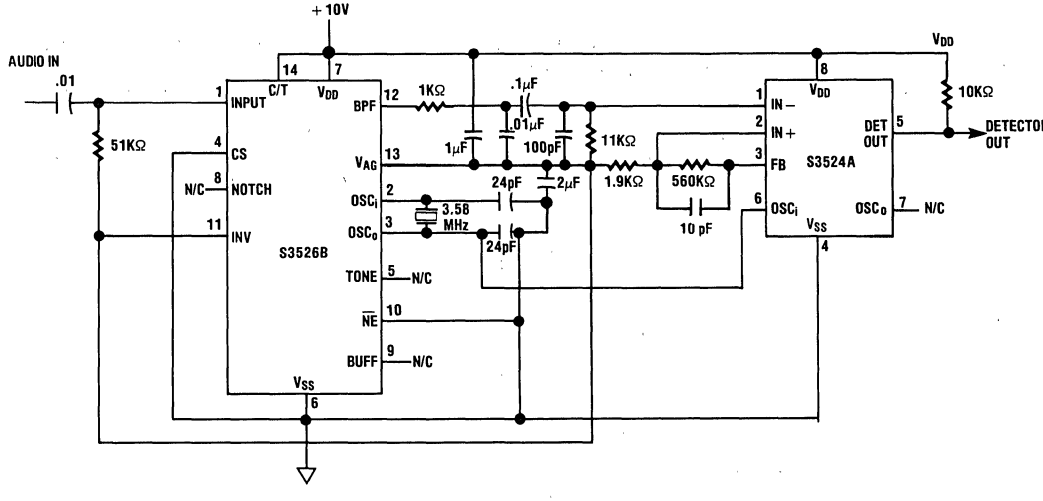


Figure 4. Circuit Example Showing S3526B and S3524A Combined to Provide Narrow Detection Bandwidth



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DTMF Bandsplit Filter

S3525A

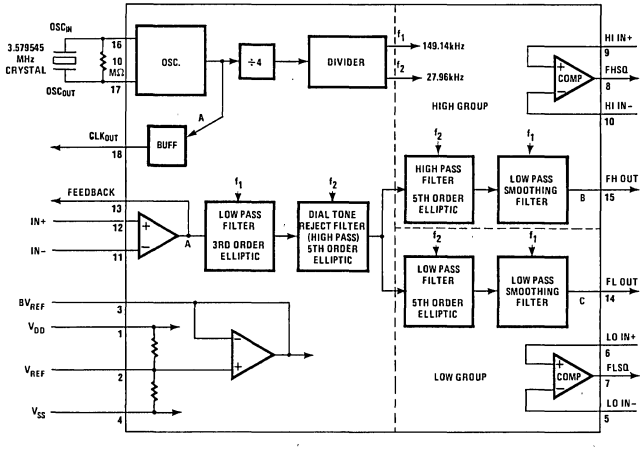
Features

- ☐ CMOS Technology for Wide Operating Single Supply Voltage Range (7.0V to 13.5V). Dual Supplies (±3.5V to ±6.75V) Can Also Be Used.
- ☐ Uses Standard 3.58MHz Crystal as Time Base. Provides Buffered Clock to External Decoder Circuit.
- ☐ Ground Reference Internally Derived and Brought Out.
- ☐ Uncommitted Differential Input Amplifier Stage for Gain Adjustment
- ☐ Filter and Limiter Outputs Separately Available Providing Analog or Digital Outputs of Adjustable Sensitivity.
- ☐ Can be Used with Variety of Available Decoders to Build 2-Chip DTMF Receivers.

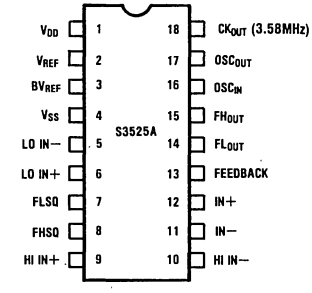
General Description

The S3525 DTMF (Touch Tone®) Bandsplit Filter is an 18-pin monolithic CMOS integrated circuit designed to implement a high quality DTMF tone receiver system when used with a suitable decoder circuit. The device includes a dial tone filter, high group and low group separation filters and limiters for squaring of the filtered signals. An uncommitted input amplifier allows a programmable gain stage or anti-aliasing filter. The dial tone filter is designed to provide a rejection of at least 52dB in the frequency band of 300Hz to 500Hz. The S3525A can be used with digital DTMF decoder chips that need the TV crystal time base allowing use of only one crystal between the filter and decoder chips.

Block Diagram



Pin Configuration



® Registered trademark of AT&T

Absolute Maximum Ratings:

DC Supply Voltage ($V_{DD} - V_{SS}$)	+15.0V
Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +125°C
Analog Input	$V_{SS} - 0.3V \leq V_{IN} \leq V_{DD} + 0.3V$

DC Electrical Operating Characteristics: $T_A = 0°C$ to $+70°C$

Symbol	Parameter/Conditions		Min.	Typ.	Max.	Units
V_{DD}	Positive Supply (Ref to V_{SS})		9.6	12.0	13.5	V
$V_{OL(CKOUT)}$	Logic Output "Low" Voltage $I_{OL} = 160\mu A$			$V_{SS} + 0.4$		V
$V_{OH(CKOUT)}$	Logic Output "High" Voltage $I_{OH} = 4\mu A$			$V_{DD} - 1.0$		V
$V_{OL(FH, FL)}$	Comparator Output Voltage Low	500pF Load			$V_{SS} + 0.5$	V
		10kΩ Load			$V_{SS} + 2.0$	V
$V_{OH(FH, FL)}$	Comparator Output Voltage High	500pF Load	$V_{DD} - 0.5$			V
		10kΩ Load	$V_{DD} - 2.0$			V
$R_{INA(IN-, IN+)}$	Analog Input Resistance		8			MΩ
$C_{INA(INA-, IN+)}$	Analog Input Capacitance				15	pF
V_{REF}	Reference Voltage Out		0.49 ($V_{DD} - V_{SS}$)	0.50 ($V_{DD} - V_{SS}$)	0.51 ($V_{DD} - V_{SS}$)	V
$V_{OR} = [BV_{REF} - V_{REF}]$	Offset Reference Voltage				50	mV
P_D	Power Dissipation	$V_{DD} = 10V$		170		mW
		$V_{DD} = 12.5V$		400		mW
		$V_{DD} = 13.5V$			650	mW

AC System Specifications:

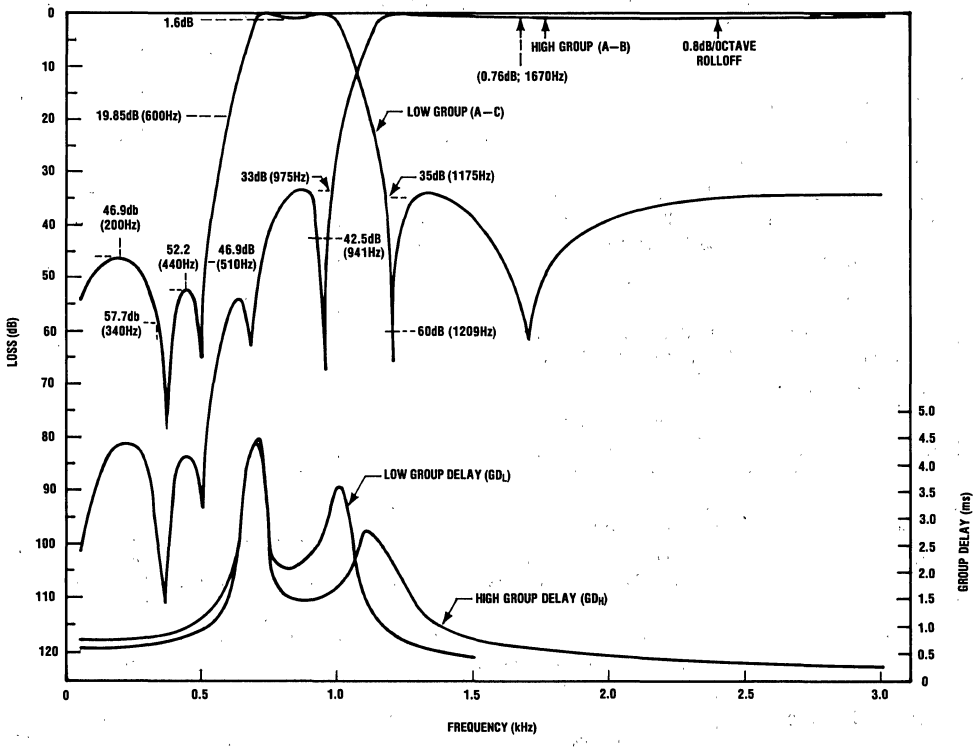
Symbol	Parameter/Conditions		Min.	Typ.	Max.	Units
A_F	Pass Band Gain		5.5	6	6.5	dB
DTR_L	**Dial Tone Rejection** Dial Tone Rejection is measured at the output of each filter with respect to the passband Low Group Rejection	350Hz	55	59		dB wrt 700Hz
		440Hz	50	53		dB wrt 700Hz
DTR_H	High Group Rejection	Either Tone	55	68		dB wrt 1200Hz

AC System Specifications (Continued)

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
	Attenuation Between Groups				
	Attenuation of the nearest frequency of the opposite group is measured at the output of each filter with respect to the passband				
GA_L	Attenuation of 1209Hz	50	>60		dB wrt 700Hz
GA_H	Attenuation of 941Hz	40	42		dB wrt 1200Hz
	Total Harmonic Distortion				
THD	Total Harmonic Distortion (dB). Dual tone of 770Hz and 1336Hz sine-wave applied at the input of the filter at a level of 3dBm each. Distortion measured at the output of each filter over the band of 300 Hz to 10kHz ($V_{DD} = 12V$)			−40	dB
	Idle Channel Noise				
ICN	Idle Channel Noise measured at the output of each filter with C-message weighting. Input of the filter terminated to BV_{REF}			1	mV_{rms}
	Group Delay (Absolute)				
GD_L	Low Group Filter Delay over the band of 50Hz to 3kHz		4.5	6.0	ms
GD_H	High Group Filter Delay over the band of 50Hz to 3kHz		4.5	6.0	ms

Pin #	Function	Descriptions
16,17	OSC_{IN}, OSC_{OUT}	These pins are for connection of a standard 3.579545MHz TV crystal and a 10MΩ ±10% resistor for the oscillator from which all clocking is derived. Necessary capacitances are on-chip, eliminating the need for external capacitors.
18	CKOUT	Oscillator output of 3.58MHz is buffered and brought out at this pin. This output drives the oscillator input of a decoder chip that uses the TV crystal as time base. (Only one crystal between the filter and decoder chips is required.)
11,12,13	IN−, IN+, Feedback	These three pins provide access to the differential input operational amplifier on chip. The feedback pin in conjunction with the IN− and IN+ pins allows a programmable gain stage and implementation of an anti-aliasing filter if required.
15,14	FH OUT, FL OUT	These are outputs from the high group and low group filters. These can be used as inputs to analog receiver circuits or to the on-chip limiters.
9,10,5,6	HI IN−, HI IN+ LO IN−, LO IN+	These are inputs of the high group and low group limiters. These are used for squaring of the respective filter outputs. (See Figure 2.)
8,7	FHSQ, FLSQ	These are respectively the high group and low group square wave outputs from the limiters. These are connected to the respective inputs of digital decoder circuits.
1,4	V_{DD}, V_{SS}	These are the power supply voltage pins. The device can operate over a range of $7V \leq (V_{DD} - V_{SS}) \leq 13.5V$.
2	V_{REF}	An internal ground reference is derived from the V_{DD} and V_{SS} supply pins and brought out to this pin. V_{REF} is $1/2(V_{DD} - V_{SS})$ above V_{SS}.
3	BV_{REF}	Buffered V_{REF} is brought out to this pin for use with the input and limiter stages.

Figure 1. Typical S3525 DTMF Bandsplit Filter Loss/Delay Characteristics



Input Configurations

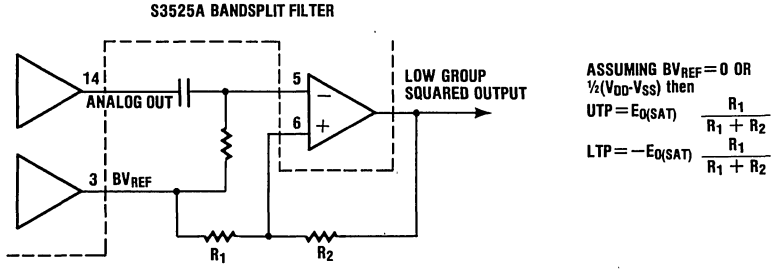
The applications circuits show some of the possible input configurations, including balanced differential and single ended inputs. Transformer coupling can be used if desired. The basic input circuit is a CMOS op amp which can be used for impedance matching, gain adjustment, and even filtering if desired. In the differential mode, the common mode rejection is used to reject power line-induced noise, but layout care must be taken to minimize capacitive feedback from pin 13 to pin 12 to maintain stability.

Since the filters have approximately 6dB gain, the inputs should be kept low to minimize clipping at the analog outputs (FL_{OUT} and FH_{OUT}).

Output Considerations

The S3525 has both analog and digital outputs available. Most integrated decoder circuits require digital inputs so the on-chip comparators are used with hysteresis to square the analog outputs. The sensitivity of the receiver system can be set by the ratio of R1 and R2, shown in Figure 2. The amount of hysteresis will set the basic sensitivity and eliminate noise response below that level.

Figure 2. Typical Squaring Circuit



Crystal Oscillator

The S3525 crystal oscillator circuit requires a 10 Meg ohm resistor in parallel with a standard 3.58MHz television colorburst crystal. For this application, however, crystals with relaxed tolerances can be used. Specifications can be as follows:

Quartz Crystal Specification (25°C ±2°C)	
Operating Temperature Range	0°C to +70°C
Frequency	3.579545MHz
Frequency Calibration Tolerance	.02± %
Load Capacitance	18pF
Effective Series Resistance	180 Ohms, max.
Drive Level-Correlation/Operating	2mW
Shunt Capacitance	7pF, max.
Oscillation Mode	Fundamental

Alternate Clock Configurations

If 3.58MHz is already available in the system it can be applied directly as a logic level to the OSC_{IN} (pin 16). [Max. zero~30% V_{DD}, min. one~70% V_{DD}]. Waveforms not satisfying these logic levels can be capacitively coupled to OSC_{IN} as long as the 10 Meg ohm feedback resistor is installed.

The S3525A provides a buffered 3.58MHz signal from the on-chip oscillator to external decoders or other devices requiring 3.58MHz.

Applications

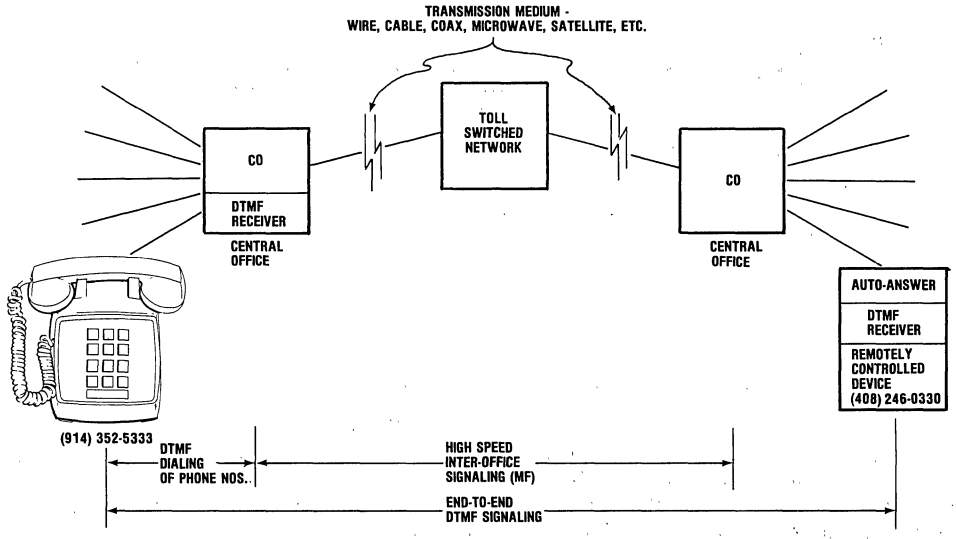
The circuits shown are not necessarily optimal but are intended to be good starting points from which an optimal design can be developed for each individual application.

Companion decoders to be used with the S3525 vary in performance and features. Nitron's NC2030 and MOSTEK's MK5102/03 are available units that can be used with the S3525.

Typical Applications

- ☐ Wireline DTMF Signal Receivers
- ☐ Radio DTMF Signal Receivers
- ☐ Dial Tone Detectors
- ☐ Offsite Data Collectors/Test Instruments
- ☐ Security Alarms
- ☐ Remote Command Receivers
- ☐ Phone Message Playback
- ☐ Camera Controllers
- ☐ Robot Arm Controllers

Figure 6. DTMF End-to-end Signaling Using the Telephone Network



Remote Control

In some systems, a telephone set is used to do remote controlling. A remote device to be signalled is interconnected to the telephone network with its own number (see Figure 6). When that number is dialed, the connection is established. The calling party continues to push the buttons on his telephone, sending command codes.* The DTMF Receiver at the central office is disconnected once the line connection is established, so no problem arises in the telephone network. Now the DTMF Receiver in the answering device is detecting and responding to the dialed digits, performing the control functions.

Dial Tone Detector

Since the frequency response of switched capacitor filters can be varied directly by varying the clock frequency, the S3525A can be used for other Telecommunications applications.

One application is a dial tone detector for telephone accessory equipment to determine the presence or absence of dial tone. Precision dial tone is a combination of 350 and 440Hz. By using a crystal of 1.758MHz the 3dB points of the low group filter output will be 334 to 496Hz. Thus, all the energy from precision dial tone will be available at the low group output.

* Need "Polarity Guard" or non-reversing central office so encoder stays enabled.

Figure 3. DTMF Keyboard

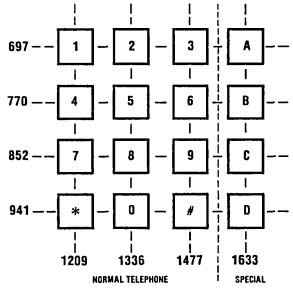
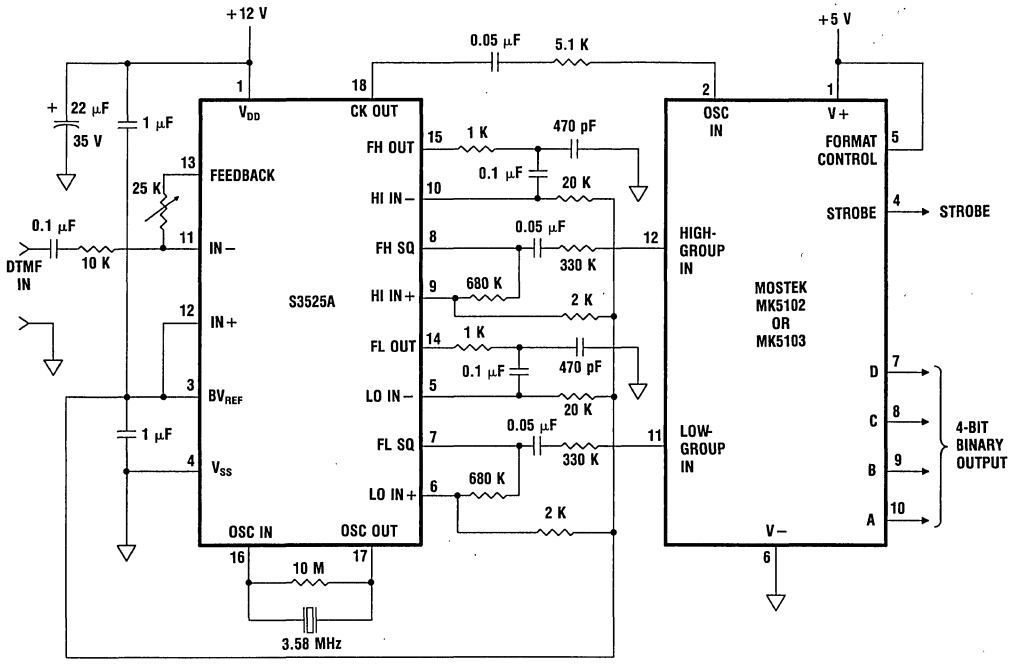


Figure 4. AMI/Mostek 2 Chip DTMF Receiver



An application note on the S3525A is also available. Please contact factory.

GOULD
AMI Semiconductors

Single Frequency Tuneable Bandpass/Notch Filter/Tone Generator

S3526B

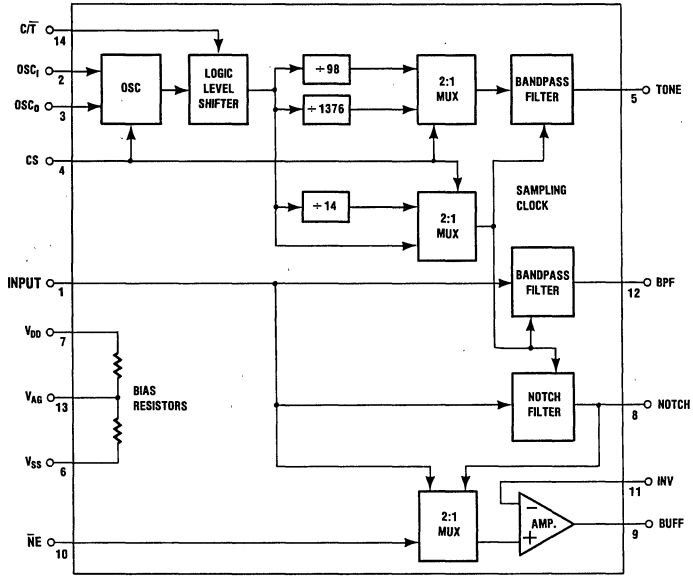
Features

- ☐ Center Frequency of Filters Match and Track Frequency of Generated Tone
- ☐ Tone Frequency Adjustable Over a 100Hz to 5kHz Range
- ☐ Unfiltered Input, Input with Notched Tone, Input Tone and Tone Generator Outputs
- ☐ Operation from a Crystal or External CMOS/TTL Clock
- ☐ Operation at 2600Hz from a Low Cost 3.58MHz TV Color Burst Crystal or 256kHz Ext. Clock
- ☐ Buffered Output Drives 600Ω Loads
- ☐ Single or Split Supply Operation
- ☐ Low Power CMOS Technology

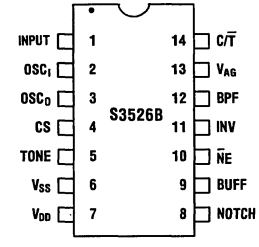
General Description

The S3526B is a low power CMOS Circuit which may be used in a variety of single frequency (SF) communication applications such as SF-Tone Receivers, Tone Remote Control in Mobile systems, Loopback Diagnostics in Modems, control of Echo Cancellers, dialing and privacy functions in Common Carrier Radio Telephone, etc. The main functional blocks of the S3526B include a low distortion tone (sinewave) generator whose frequency may be programmed using a crystal (i.e. 2600Hz using a low cost TV color burst crystal) or external clock time base; a bandpass filter used to extract tone information from the input signal; a band reject filter which is used to "Notch" out tone information from the input signal; and a buffer amplifier with selectable input (unfiltered input signal, or input signal with tone notched) capable of driving a 600Ω load.

S3526B Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage ($V_{DD} - V_{SS}$) ..... + 15.0V
Operating Temperature ..... 0°C to + 70°C
Storage Temperature ..... − 65°C to + 150°C
Input Voltage, All Pins ..... $V_{SS} - 0.3V < V_{IN} < V_{DD} + 0.3V$

D.C. Electrical Operating Characteristics: $T_A = 0°C$ to + 70°C, $(V_{DD} - V_{SS}) = 10V$ unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{DD}	Positive Supply (Ref. to V_{SS})	9.0	10	13.5	V
P_D	Power Dissipation (Maximum @13.5V)		100	275	mW
R_{IN}	Input Resistances (Except Input)	8			MΩ
C_{IN}	Input Capacitances			15.0	pF

General Analog Signal Parameters: $T_A = 0°C$ to + 70°C, $(V_{DD} - V_{SS}) = 10V$

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
A_F	Straight Through Gain (Measured at −10dBm0)	−0.1	0	0.1	dB
Z_{IN}	Input Impedance (Input, Pin 1)		2.5		MΩ
TLP	Transmission Level Point (0dBm0)		1.5		VRMS
V_{FS}	Maximum Input Signal Level (+ 3dBm0)		2.1		VRMS
R_L	Load Resistance (BPF, NOTCH)	10			kΩ
R_L	Load Resistance (BUFF)	600			ohms
V_{OSB}	Buffer Output Offset Voltage		±50	±150	mV
ICN_P	Idle Channel Noise in Pass Condition		2		dBrnC0
V_{OUT}	Output Signal Level into R_L for NOTCH, BPF, BUFF	2.0	2.1		VRMS
V_{OT}	Sine Wave (Tone) Output (Load = 10KΩ)		$0.6(V_{DD} - V_{SS})$ ±0.5dB		Vpk-pk
V_{TD}	Sine Wave Distortion ($f_{OSC} = 3.58MHz$) (See Figure 4)		−35		dB

Filter Performance Specifications
Band Pass Filter Characteristics $T_A = 0°C$ to + 70°C, $(V_{DD} - V_{SS}) = 10V$, $f_{OSC} = 3.58MHz$

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{FS}	Maximum Input Voltage (+ 3dBm0)		2.1		VRMS
A_{BP}	Passband Gain @ − 10dBm0	−0.8	0	+0.8	dB
I_{CN}	Idle Channel Noise		24		dBrnC0
V_{OS}	Output Offset		±50	±150	mV
	* 2600Hz Bandpass Filter Response (referenced from 2600Hz, + 3dBm0) (See Figures 1 and 2)				
	DC to 1600Hz		−80		dB
	2100Hz		−63	−50	dB
	2400Hz		−37	−30	dB
	2540Hz		−7.0	−3	dB
	2560Hz	−3	−1.8		dB
	2640Hz	−3	−1.0		dB
	2660Hz		−5.4	−3	dB
	2800Hz		−35	−30	dB
	3100Hz		−58	−50	dB
	3600Hz		−74		dB
DR	Dynamic Range (V_{FS} to ICN)		70		dB

*Delay from input to output is approximately 8mseconds.

Notch Filter Characteristics $T_A = 0°C$ to $+70°C$, $(V_{DD} - V_{SS}) = 10V$ (Symmetrical Supplies), $f_{OSC} = 3.58MHz$

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{FS}	Maximum Input Voltage (+3dBm0)		2.1		VRMS
A_{BR}	Passband Gain @ −10dBm0)	−0.5	0	+0.5	dB
ICN	Idle Channel Noise		18		dBrnC0
V_{OS}	Output Offset		±100	±225	mV
DR	Dynamic Range (V_{FS} to ICN)		75		dB
	2600Hz Notch Filter Response (referenced from 1000Hz, (+3dBm0) (See Figures 1 and 3)				
	250Hz to 2200Hz	−0.5	±0.1	0.5	dB
	2200Hz to 2400Hz	−5.0		0.5	dB
	2585Hz to 2615Hz		−70	−53	dB
	2800Hz to 3000Hz	−5.0		0.5	dB
	3000Hz to 3400Hz	−0.5	±0.1	0.5	dB

Digital Electrical Parameters $T_A = 0°C$ to $+70°C$, $(V_{DD} - V_{SS}) = 10V$

Symbol	Mode Control Logic Levels	Min.	Typ.	Max.	Units
V_{IH}	C/T CMOS Operation (Pin 14)	$V_{DD} - 0.5$		V_{DD}	V
V_{IL}	C/T TTL Operation (Pin 14)	V_{SS}		$V_{DD} - 4$	V
V_{IH}	CS for Low Speed Clock Input	$V_{DD} - 0.5$		V_{DD}	V
V_{IL}	CS for Crystal or High Speed Clock	V_{SS}		V_{AG}	V
	CMOS Logic Levels				
V_{IH}	Input Voltage "1" Level	$V_{AG} + 2$		V_{DD}	V
V_{IL}	Input Voltage "0" Level	V_{SS}		$V_{AG} - 2$	V

Control Pin Definitions

Pin#	Name	Connection	Operation	Note
14	C/T	V_{DD} to $(V_{DD} - 0.5V)$	CMOS Logic Levels	1
		$(V_{DD} - 4V)$ to V_{SS}	TTL Logic Levels	
4	CS	V_{DD}	Ext. Low Speed Sq. Wave Clock @ Pin 3	2
		V_{SS} or V_{AG}	Crystal Connected Between Pins 2 and 3 or High Speed Clock to Pin 2	
10	$\overline{NE}$	V_{DD} to .7 $(V_{DD} - V_{SS})$ 70%	Buffer Out = Input Signal	
		V_{SS} to .3 $(V_{DD} - V_{SS})$ 30%	Buffer Out = Notch Filter Out	

NOTES: 1) CMOS logic levels are same as V_{DD} and V_{SS} supply voltage levels. For TTL interface ground of TTL logic must be connected to V_{SS} supply pin.
2) For ext. low speed clock operation pin 2 is open. For ext. high speed clock, drive pin 2, leave pin 3 open.
3) The performance specifications are guaranteed with ±5% power supplies for normal operation.

Pin Function Description

Pin	No.	Function
Input	1	This pin is the analog input to the filters and the buffer. It is a high impedance input (Z≅2.5MΩ).
OSC_I OSC_O	2 3	These pins are the timing control for the entire chip. A crystal may be connected across these two pins in parallel with a 10MΩ resistor. Another option is to provide an ext clock at pin 3 and leave pin 2 to open. TTL or CMOS may be used. As a third choice, a CMOS level external clock may be applied to pin 2 directly leaving pin 3 open.
CS	4	Clock Select-This pin when tied to V_{DD} configures the chip to operate from a low speed clock. When tied to V_{AG} or V_{SS} the chip operates from external crystal or high speed clock.
TONE	5	This is an output pin providing a sine wave with a frequency of fosc ÷ 1376 if CS is low or fosc ÷ 98 if CS is high.
V_{SS}	6	Negative supply voltage pin. Typically $-5V \pm 5\%$
V_{DD}	7	Positive supply voltage pin. Typically $+5V \pm 5\%$.
NOTCH	8	Band Reject (Notch) Filter-This is the output of the filter that notches the tone information from the input signal. It is capable of driving a load ⩾10kΩ.
BUFF	9	Buffer Output-The buffer is capable of driving a 600Ω load and provides from its output either the signal input without filtering, or the signal input with the tone frequency notched out.
NE	10	Notch Enable-This pin controls which signal is presented to the buffer input. A logic high (V_{DD}) connects the input signal. A logic low (V_{SS}) connects the output of the band reject (notch)filter.
INV	11	Inverting-This is the inverting input of the buffer.
BPF	12	Band Pass Filter-This is the output of the band pass filter which will pass any energy at the tone frequency present in the input signal. It is capable of driving a load ⩾10kΩ.
V_{AG}	13	Analog Ground-This is the analog ground pin. When used with a single supply, this pin is ½ ($V_{DD} - V_{SS}$) ±100mV. When used with ±5V supplies, this point is at ground. The S3526 has internal voltage divider resistors to V_{DD} and V_{SS} of ≅20kΩ.
C/T	14	CMOS/TTL-This pin determines whether CMOS or TTL levels will be accepted at pin 3 for a clock input. When tied to V_{DD}, the chip accepts CMOS logic levels. When tied to a point ⩽($V_{DD} - 4V$), the chip accepts TTL levels referenced to V_{SS}. For crystal operation pin 14 should be at V_{DD}.

Application Information

The S3526B device is a very versatile filter chip. Although it was designed for the telephone market SF signaling application when used with the commonly available TV colorburst crystal, it will work over a wide range of frequencies. Typically, it will cover from 100Hz to 5kHz providing coverage of the entire voice band for in-band signaling.

Because it is a very high Q filter the transient response time must be considered when determining the maximum data rate for a particular frequency. This response is illustrated in Figure 5 and shows that it is quite adequate for 10 pulse-per-second (50% duty cycle) data rate at 2600Hz. But the same data rate could not be used at 500Hz, for example, as a detector could not differentiate between tone on and tone off conditions.

Figure 1. Typical Filter Performance Curves at 2600Hz

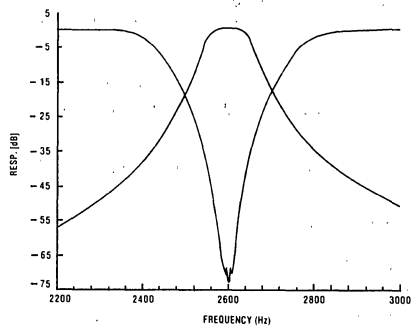


Figure 2. Typical Bandpass Response

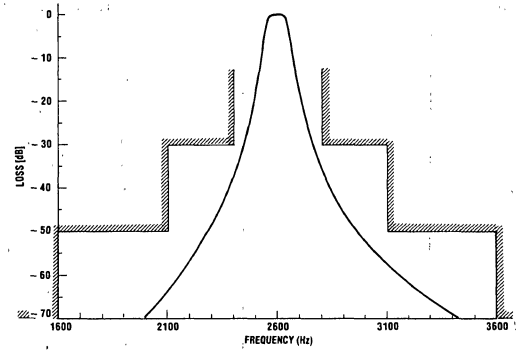


Figure 3. Typical Notch Response

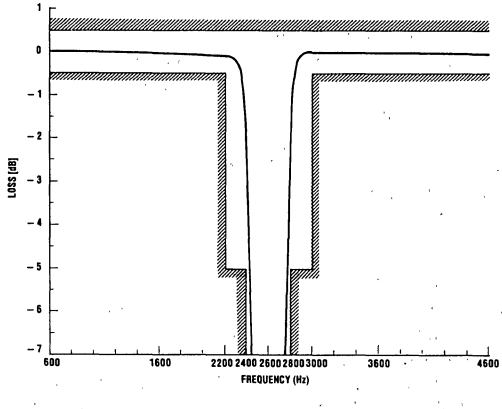


Figure 4. Typical Sine Wave Output Spectrum from Pin 5

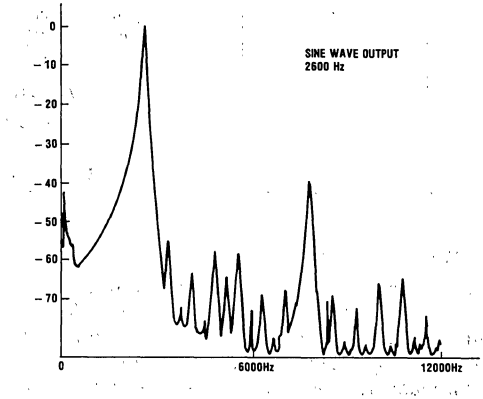


Figure 5. Typical Delay Characteristics at + 3dBmO with 2600Hz Pulsed at 10pps with 50% Duty Cycle

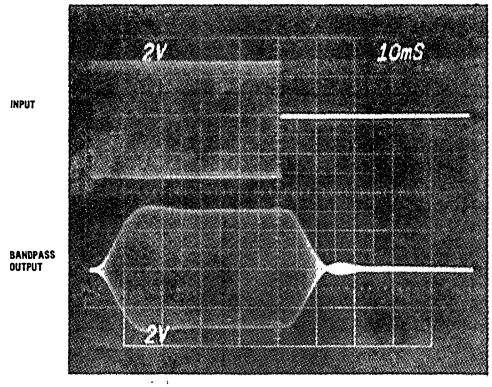
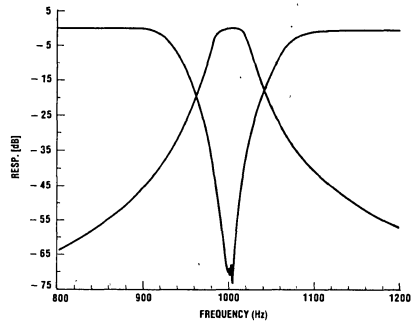


Figure 6. Typical Filter Performance Curves at 1000Hz



The combination of tone generator, notch filter, and bandpass filter allows one to generate a signaling tone at the sending end and notch it out at the receiving end, as well as detect it through the bandpass filter. For reliable detection the output of the bandpass filter can be compared with the output of the bandreject filter. If the output of the BR filter is within a fixed ratio of the BP filter (such as 10dB) then the signal present may be considered voice rather than signaling and ignored.

In situations where the entire voice band is desired except during signaling the buffer output can be switched straight through to the input. When the output of the filters indicates that a signaling tone is present, the NE pin can be switched low, switching the notch filter into the signal path to prevent the tone from reaching the listener or from being passed further down the system to another signaling receiver.

By using the notch filter with telephone accessories it can be guaranteed that the accessory will not violate the telephone company specifications about transmitting 2600Hz into the lines, causing disconnected calls.

Power Supplies

The S3526B will work with either single or dual power supplies. When used with dual power supplies (± 5V) the analog inputs and outputs will be referenced to ground. If an external clock signal is provided, rather than using a crystal, it must be swinging from V_{SS} to V_{AG} for TTL swings or from V_{SS} to V_{DD} for CMOS swings. If this is not convenient the signal can be capacitively coupled into pin 3 as illustrated in Figure 7. In the dual supply mode, the power supplies should track or maintain close tolerances for maximum accuracy. If the supplies should skew, the filter characteristics will change very slightly and in most applications, will have no effect at all but can be seen if the curves are plotted on high accuracy equipment.

When using the S3526B on a single power supply the analog inputs and outputs will be referenced to V_{AG} which is ½ ($V_{DD} - V_{SS}$). This means that the analog signals may need to be capacitively coupled in and out if they are normally ground referenced. For example, the input may appear as in Figure 8. But when an external clock is used in the single supply situation it can be direct coupled TTL levels referenced to ground.

Selecting Clocking Sources

The switched capacitor filter design allows the S3526B to be easily tuned by varying the clock frequency. This makes it useful for many applications in telephone signaling, data communications, medical telemetry, test equipment, automatic slide projectors, etc. The necessary clock frequency can be determined by multiplying the desired center frequency by 1376. This frequency

can then be provided from a crystal, an external clock, or a rate multiplier chip. With Clock Select (CS), pin 4 tied low the TONE, pin 5, will provide the desired frequency and the filters will be centered around that frequency. There are many common, low cost microprocessor frequency crystals available that might be very close to a desired frequency. Table 1 illustrates some possible application frequencies. For example, by using a standard 3.00MHz crystal the 2175Hz tone would be 2180Hz or .23% high.

If it is desired to use a lower frequency clock and precision tone generation is not required the external clock can be determined by multiplying the center frequency by 98.4, and tying Clock Select (CS) pin 4 high. Note that the TONE, pin, 5, is not accurate in this situation, being .41% higher than the filter center frequency, although it will fall well within the passband of both filters and be perfectly usable.

Figure 7. External Clock Drive

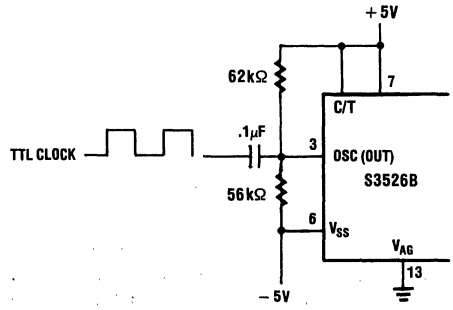


Figure 8.

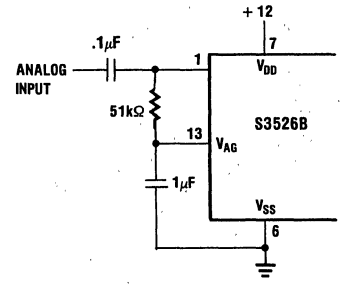


Table 1. Tone and Clock Frequencies for Various Applications

Tone In Hertz	Application	CS=0 XTAL or HIGH Freq. Clock (MHz)	CS=1 Ext. Clock Input (Low Freq.) (Hz)
550	Guard Tone-Data Comm	.756800	54,120
1000	Test Tone	1.376000	98,400
1020	Test Tone	1.403520	100,368
1400	Medical Telemetry	1.926400	137,760
1600	SF Signaling—Military	2.201600	157,440
1800	Guard Tone-Data Comm	2.476800	177,120
1850	Pilot Tone-Radio	2.545600	182,040
1950	Pilot Tone-Radio	2.683200	191,880
2125	Echo Suppressor Disable	2.924000	209,100
2150	Echo Suppressor Disable	2.958400	211,560
2175	Guard Tone-Radio	2.992800	214,020
2280	SF Signaling-Telephone	3.137280	224,352
2400	SF Signaling-Telephone	3.302400	236,160
2600	SF Signaling-Telephone	3.579545	256,000
2713	Loopback Tone-Datacom	3.733088	266,959
2800	SF Signaling-Telephone	3.852800	275,520
2805	Signaling Tone-Radio	3.859680	276,012
3825	SF Signaling-European	5.263200	376,380

GOULD
AMI Semiconductors

Programmable Low Pass Filter

S3528B

COMMUNICATION PRODUCTS

Features

- ☐ Cutoff Frequency Selectable in 64 Steps Via Six Bit Control Word
- ☐ Continuously Tuneable Cutoff Frequency Variable Via External Clock (Crystal, Resonator, or TTL/CMOS Clock)
- ☐ Cutoff Frequency (f_C) Range of 10Hz to 20kHz, 40Hz to 20kHz Via Popular 3.58MHz TV Crystal
- ☐ Seventh Order Ellipitical Ladder Filter with Cosine Prefiltering Stage
- ☐ Passband Ripple: <0.1dB
- ☐ Stopband Attenuation: >51dB for $f>1.3f_C$
- ☐ Uncommitted Input and Output Op Amps for Anti-Aliasing and Smoothing Functions
- ☐ Steps May Be Custom Programmed from a Set of 2,048 Discrete Points Via Internal ROM
- ☐ Low Power CMOS Technology

Typical Applications for the S3528B and S3529B Programmable Filters

Telecommunications

- ☐ PBX and Trunk Line Status Monitoring
- ☐ Automatic Answering/Forwarding/Billing Systems
- ☐ Anti-Alias Filtering
- ☐ Adaptive Filtering

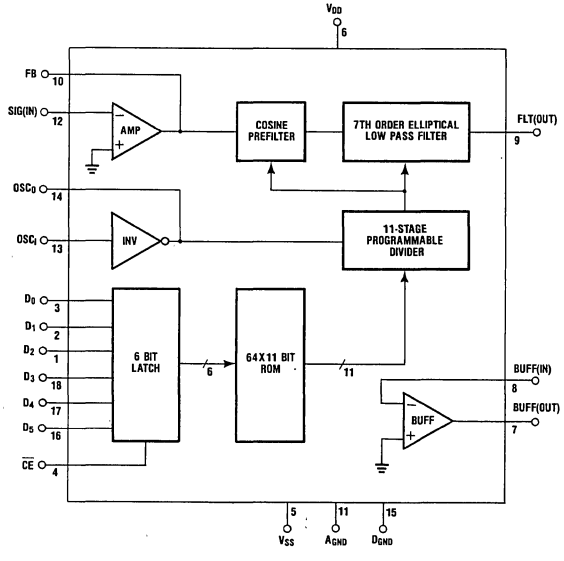
Remote Control

- ☐ Alarm Systems
- ☐ Heating Systems
- ☐ Acoustic Controllers

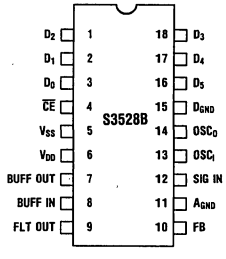
Test Equipment/Instrumentation

- ☐ Spectrum Analyzers
- ☐ Computer Controlled Analog Circuit Testers
- ☐ Medical Telemetry/Filtering
- ☐ ECG Signal Filtering
- ☐ Automotive Command Selection and Filtering

S3528B Block Diagram



Pin Configuration



S3528B

Typical Applications for the S3528B and S3529B Programmable Filters (continued)

Audio

- ☐ Electronic Organs
- ☐ Speech Analysis and Synthesis
- ☐ Speaker Crossovers
- ☐ Sonabuoys
- ☐ Spectrum Selection
- ☐ Low Distortion Digitally Tuned Audio Oscillators

General Description

The S3528B's CMOS design using switched-capacitor techniques allows easy programming of the filter's cutoff frequency (f_C) in 64 steps via a six-bit control word. For dynamic control of cutoff frequencies, the S3528B can operate as a peripheral to a microprocessor system with the code for the cutoff frequency being latched in from the data bus. When used with the companion high pass filter, the S3529B, a bandpass or a bandreject filter with a variable center frequency is obtained. For special applications the S3528B's internal ROM can be customized to accommodate a specific set of cutoff frequencies from a choice of 2,048 possibilities.

Absolute Maximum Ratings

Supply Voltage ($V_{DD} - V_{SS}$)	+ 15.0V
Operating Temperature	0°C to + 70°C
Storage Temperature	− 65°C to + 150°C
Input Voltage, All Pins	$V_{SS} - 0.3V \leq V_{IN} \leq V_{DD} + 0.3V$

D.C. Electrical Operating Characteristics: $T_A = 0°C$ to $+70°C$, $(V_{DD} - V_{SS}) = 10V$ unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{DD}	Positive Supply (Ref. to V_{SS})	9.0	10	13.5	V
P_D	Power Dissipation @10V @13.5V		60 135	110 225	mW mW
R_{IN}	Input Resistance (Pins 1-4, 8, 12, 13, 16-18)	8			MΩ
C_{IN}	Input Capacitance (Pins 1-4, 8, 12, 13, 16-18)			15.0	pF

General Analog Signal Parameters: $(V_{DD} - V_{SS}) = 10V \pm 10\%$, $T_A = 0°C$ to $+ 70°C$, $f_{clock} = 3.58MHz$

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
A_F	Pass Band Gain at 0.6 f_c	− 0.5	0	0.5	dB
V_0	Reference Level Point (0dBm0)		1.5		VRMS
V_{FS}	Maximum Input Signal Level (+ 3dBm0)		2.1		VRMS
R_L	Load Resistance FLT OUT, Pin 9	10			kΩ
R_L	Load Resistance BUFF OUT, Pin 7	600			ohms
V_{OUT}	Output Signal Level into R_L for FLT OUT, BUFF OUT, $V_{IN} = 2.1V$	2.0	2.1		VRMS
THD	Total Harmonic Distortion at .3f_c		.3		%
WBN	Wideband Noise (to 30kHz) $f_c = 3.2kHz$		.15		mVRMS
WBN	Wideband Noise (to 80kHz) $f_c = 15kHz$		.13		mvRMS
ICN	Idle Channel Noise $f_c = 3200Hz$		8	23	dBrnC0
V_{OS}	Buffer Output (Pin 7) Offset Voltage		± 10	± 30	mV
V_{OFS}	Filter Output (Pin 9) Offset Voltage		± 80	± 200	mV

Filter Performance Specifications

Low Pass Filter Characteristics: $f_{clock} = 3.58MHz$, $(V_{DD} - V_{SS}) = 10V$, $T_A = 0°C$ to $+70°C$

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
	Pass Band Ripple (Ref. 0.6 f_c)	−0.5	±0.05	0.5	dB
Filter Response(1): F_c = 3200Hz (Pin 9)					
	(See Figure 5) (fc) 3200Hz	−0.5	±0.1	0.5	dB
	(1.06fc) 3372Hz	−5.5	−3.0	−0.5	dB
	(1.27fc) 4060		−42		dB
	(1.3fc) 4155		−51	−48	dB
	(1.32fc) 4235		−65	−48	dB
	(1.62fc) 5175		−75	−48	dB
	(1.3fc Upward) 4155 to 100,000Hz		< −51		dB
DR	Dynamic Range (V_{FS} to ICN) [+3.0 to −82 dBm]		85		dB

Digital Electrical Parameters: $V_{DD} = +5V$, $V_{SS} = -5V$, $T_A = 0°C$ to $+70°C$ unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	2.0		V_{DD}	Volts
V_{IL}	Input Low Voltage	V_{SS}		0.8	Volts
I_N	Input Leakage Current ($V_{IN} = 0$ to 4VDC)			10	μADC
C_{IN}	Input Capacitance			15	pF
Digital Timing Characteristics					
t_{CE}	Chip Enable Pulse Width	200	300		nsec
t_{AS}	Address Setup Time		300		nsec
t_{AH}	Address Hold Time		20		nsec
f_{osc}	Crystal Oscillator Frequency(2)		3.58		MHz
t_{SET}	Settling Time from $\overline{CE}$ to Stable f_c ($f_c = 3200$)(3)		6		msec

1.) Filter Response Referenced to f = 1,920Hz

2.) The tables are based on common TV crystal. See paragraph on "Clock Frequencies" for more detail.

3.) $t_{SET} = \frac{10}{f_c} + 3msec$

Pin Function Description

Pin Name	Number	Function
V_{DD}	6	Positive supply voltage pin. Normally +5V ±10%.
V_{SS}	5	Negative supply voltage pin. Normally −5V ±10%.
A_{GND}	11	Analog ground reference point for analog input and output signals. Normally connected to ground.
D_{GND}	15	Digital ground reference point for digital input signals. Normally connected to ground.
D_0	3	Control word Inputs: The set of six bits allows selection of one of sixty-four cutoff frequencies. The 6 bit control word is latched on the rising edge of $\overline{CE}$. The high-impedance inputs may be bridged directly across a microprocessor data bus. These inputs are TTL or CMOS compatible. A "1" is 2.0V to V_{DD}, and a "0" is 0.8V to V_{SS}.
D_1	2	
D_2	1	
D_3	18	
D_4	17	
D_5	16	
$\overline{CE}$	4	Chip Enable: This pin has 3 states. When $\overline{CE}$ is at V_{DD} the data in the latch is presented to the ROM and the inputs have no effect. When $\overline{CE}$ is at ground the data presented on the inputs is read into the latch but the previous data is still in the ROM. Returning $\overline{CE}$ to V_{DD} presents the new data to the ROM and f_c changes. When $\overline{CE}$ is at V_{SS} the inputs go directly to the ROM, changing f_c immediately. This is the configuration for a fixed filter; $\overline{CE}$ is at V_{SS} and the D_0 through D_5 are tied to V_{DD} or V_{SS}/D_{GRND} depending on the desired f_c.

Pin Function Description (continued)

Pin Name	Number	Function
OSC_I OSC_O	13 14	Oscillator In and Oscillator Out: Placing a crystal and a 10MΩ resistor across these pins creates the time base oscillator. An inexpensive choice is to use the 3.58MHz TV colorburst crystal.
SIG IN	12	Signal Input: This is the inverting input of the input op amp. The non-inverting input is internally connected to Analog Ground.
FB	10	Feedback: This is the feedback point for the input op amp. The feedback resistor should be ⩾10kΩ for proper operation.
FLT OUT	9	Filter Out: This is the high impedance output of the programmable low pass filter. Loads must be ⩾10kΩ.
BUFF IN	8	Buffer Input: The inverting input of the buffer amplifier.
BUFF OUT	7	Buffer Out: The buffer amplifier output to drive low impedance loads. This pin may drive as low as 600Ω loads.

Example of Circuit Connection for S3528B
Figure 1. Stand Alone Operation

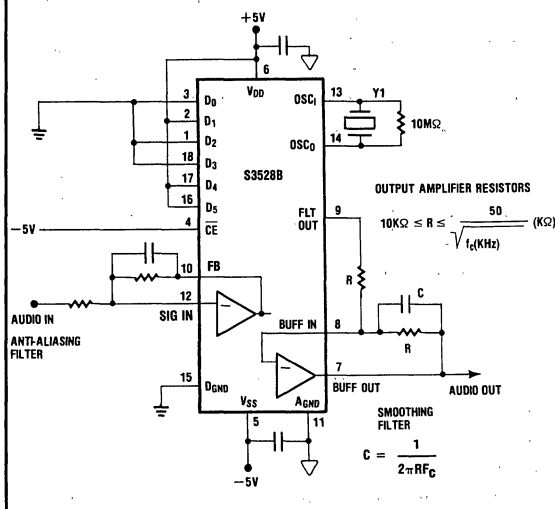
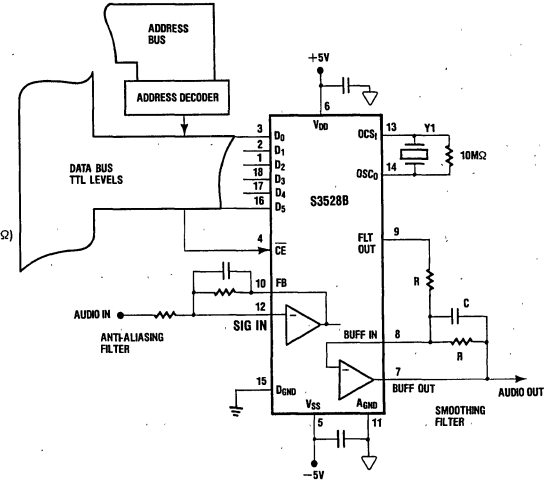


Figure 2. Microprocessor Interface



Operation

S3528B Filter is a CMOS Switched Capacitor Filter device designed to provide a very accurate, very flat, programmable filter that can be used in fixed applications where only one cutoff frequency is used, or in dynamic applications where logic or a microprocessor can select any one of 64 different cutoff frequencies. It is normally clocked by an inexpensive TV color burst crystal and provides the cutoff frequencies seen in Table 1 when the Data Bus pins are programmed.

All that is required for fixed operation is a 10MΩ resistor, the 3.58MHz TV crystal, and some resistors and capacitors around the input and output amplifiers to set the gain, anti-aliasing, and smoothing. The Data Bus pins are programmed from the table to either a "1" (+5V) or a "0" (ground or −5V) for the desired cutoff frequency. The $\overline{CE}$ pin is tied low, to V_{SS}.

Operation (continued)

The ROM is addressed by the contents of the latch and presents an 11-bit word to the programmable divider which divides f_{CLK}.

The FILTER OUT pin is capable of driving a 10kΩ load directly or, for smoothing and driving a 600Ω load, the output buffer amplifier can be used for impedance matching.

As illustrated in the curves of Figures 3, and 5 through 7, the passband ripple (for fc<18kHz) is less than ±0.1dB and the stop band rejection is better than 50dB, as measured on a network analyzer.

For microprocessor controlled operation, the Data Bus can be bridged across a regular TTL bus and when $\overline{CE}$ is strobed, the data present will be latched in and the filter will settle down to its new cutoff frequency. In CMOS systems, the Data Bus and $\overline{CE}$ can be swung rail-to-rail. A_{GND} and D_{GND} must be at ½ the supply voltage.

The following table illustrates the available cutoff frequencies based on using a 3.58MHz TV crystal for a time base, by approximately 100Hz steps through the voice band from 100Hz to 3900Hz. Note that the hex input code for each frequency in the voice band is one-hundredth of the cutoff frequency. For 3200Hz, the hex code is 32, for 900Hz it is 09. Additional frequencies are listed with their codes on the right side of the Table 1.0.

Table 1.0—Standard Frequency Table: Programmable Filter S3528B. f_{CLOCK} = 3.58MHz

Voice Band

Input Code (HEX) D_5–D_0	Divider Ratio	f_c Actual (Hz)
00	2048	44
01	895	100
02	447	200
03	298	300
04	224	399
05	179	500
06	149	601
07	128	699
08	112	799
09	99	904
10	89	1005
11	81	1105
12	74	1209
13	69	1297
14	64	1398
15	60	1491
16	56	1598
17	53	1688
18	50	1790
19	47	1904
20	45	1989
21	43	2081
22	41	2183
23	39	2295
24	37	2418
25	36	2486
26	34	2632
27	33	2711
28	32	2797
29	31	2887
30	30	2983
31	29	3086
32	28	3196
33	27	3314
34	26	3442
36	25	3579
37	24	3728
39	23	3891

Additional Points Available

Input Code (HEX) D_5–D_0	Divider Ratio	f_c Actual (Hz)
0A	188	476
0B	358	250
0C	90	994
0D	87	1028
0E	85	1053
0F	78	1147
1A	61	1467
1B	58	1542
1C	52	1721
1D	46	1945
1E	44	2034
1F	40	2237
2A	38	2350
2B	35	2557
2C	22	4067
2D	20	4474
2E	18	4971
2F	16	5593
35	15	5965
38	14	6392
3A	12	7457
3B	10	8949
3C	9	9943
3D	6	14915
3E	5	17897
3F	4	22372

$$f_{cutoff} = \frac{f_{CLOCK}}{40 \text{ (Divider Ratio)}}$$

$$f_{sampling} = \frac{f_{CLOCK}}{\text{Divider Ratio}}$$

Figure 3. Family of Loss Curves for 4 Different Control Codes

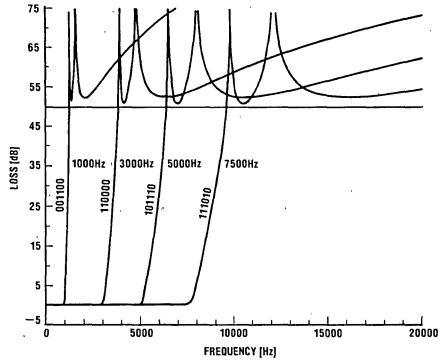


Figure 4. Address and Chip Enable Timing

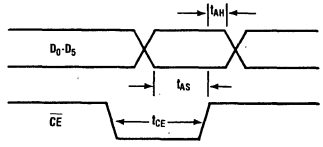


Figure 5. Loss Curve, Control = 110010, f_C = 3200Hz

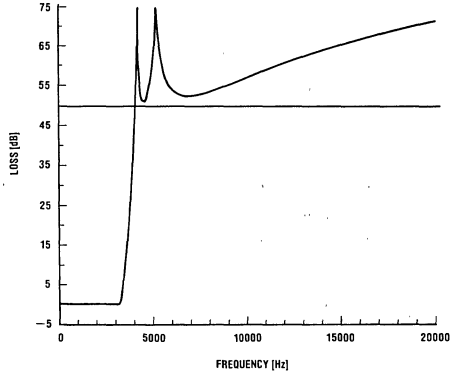


Figure 6. Passband Control Detail, Control = 110010, f_C = 3200Hz

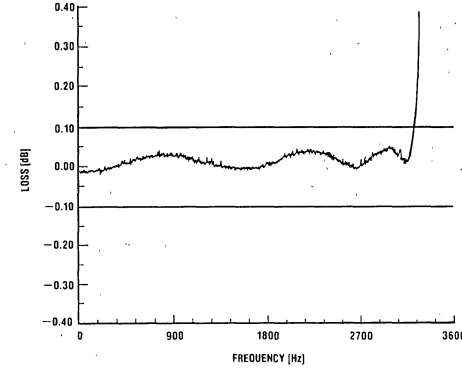


Figure 7. Family of Loss Curves for 4 Different Control Codes

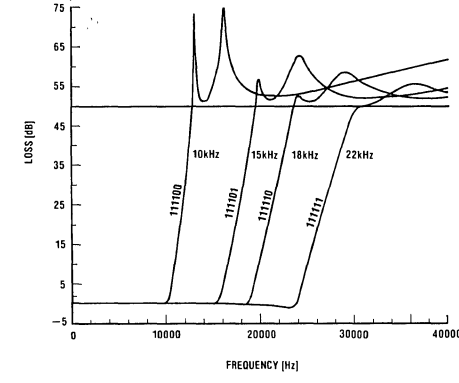


Figure 8. Loss and Group Delay, Fc = 3200Hz

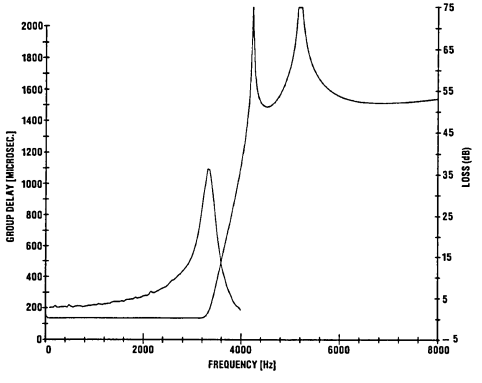
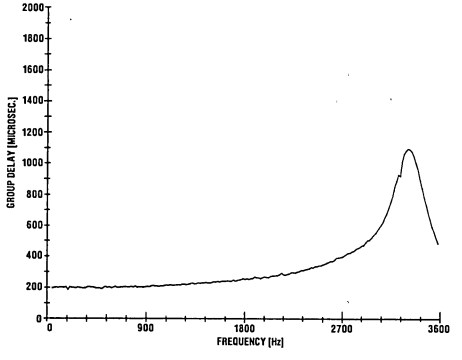


Figure 9. Group Delay, Control = 110010, FC = 3.2kHz

$GDf_{C=X} \doteq GDf_{C=3.2kHz} \left(\frac{3.2kHz}{X\ kHz}\right)$



Applications Information

Many filter applications can benefit from the S3528B, particularly if extremely flat passband response with precise, repeatable cutoff frequencies are required. Or, if the same performance is required at different frequencies it can be switched or microprocessor controlled. The circuits (Figures 1 and 2) illustrate how the S3528B might be connected for two different uses. The "stand alone" drawing (Figure 1) shows how it would be programmed as a fixed, 3200Hz low pass filter. The other drawing (Figure 2) shows a microprocessor driven application that lets the cutoff frequency be varied on command.

Some fields that can use such a filter are speech analysis and scrambling, geo-physical instrumentation, under water accoustical instrumentation, two-way radio, telecommunications, electronic music, remotely programmable test equipment, tracking filter, etc.

Anti-Aliasing

In planning an application the basic fundamentals of sampling devices must be considered. For example, aliasing must be taken into consideration. If a frequency close to the sampling frequency is presented to the input it can be aliased or folded back into the passband. Because the S3528B has an input cosine filter the effective sample frequency is twice the filter clock frequency of 40 times the cutoff frequency. If f_C = 1000Hz and a signal of 79,200Hz is put into the filter, it will alias the 80kHz effective sampling frequency of the input cosine filter and appear as an 800Hz signal at the output. This means that for some applications the input op amp must be used to construct a simple one or two pole RC anti-aliasing filter to insure performance. In many situations, however, this will not be necessary since the input signal will already be band-limited.

Smoothing

In addition, all sampling devices will have aliased components near the clock frequency in the output. For example, there will be small components at $f_{clk} \pm f_{in}$ in the output waveform. This can be reduced by constructing a simple smoothing filter around the output buffer amplifier. Because of the sinx/x characteristics of a sample and hold stage the aliasing components are already better than 30dB down. The clock feed through is approximately −50dBV. This means that a simple one pole filter can provide another 20dB of rejection to keep the aliasing below 50dB down. In the case of a 3kHz f_{CUTOFF} and the smoothing filter designed for a 3dB point at $4f_{CUTOFF}$ the smoothing filter will affect

Smoothing (continued)

the 3kHz point by .25dB. If this is not desirable then the smoothing filter might be constructed as a second order filter.

For a fixed application, anti-aliasing and smoothing are straight forward. For a dynamic operation, the desired operating range of frequencies must be considered carefully. It may be necessary to switch in or out additional components in the RC filters to move cutoff frequencies. The S3528B has a ratio of cutoff frequencies of 550:1 and to use the full range would require some switching.

Notch Rejection

The filter is designed to have 51dB of rejection at $1.3f_{CUTOFF}$ and greater. If greater rejection of a specific tone or signal frequency is desired, the cutoff frequency can be selected to position the undesired tone at $1.325f_{CUTOFF}$ or $1.62f_{CUTOFF}$. This will place it in a notch as illustrated in Figure 5.

The S3529B (High Pass Filter) and the S3528B (Low Pass Filter) can be used together to make either Band Pass or Band Reject/Notch filters. The control code selection determines the bandwidth of the resulting filter.

It should be noted that with the S3528B and S3529B data pins connected in parallel and their analog inputs and outputs in series a bandpass filter of approximately 10% bandwidth is created.

Figure 10. S3528B and S3529B in Parallel Notch Configuration—Narrow Bandwidth

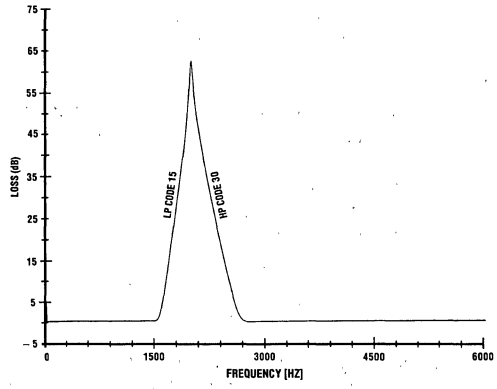


Figure 11. Cascaded S3528B and S3529B Control = 100001 Bandpass Configuration—10% Bandwidth

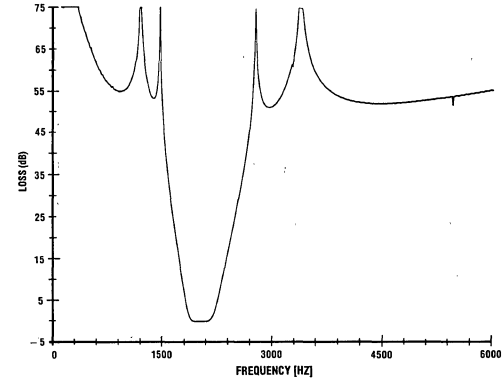
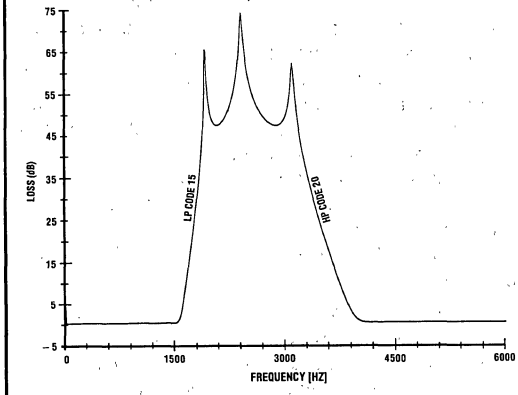


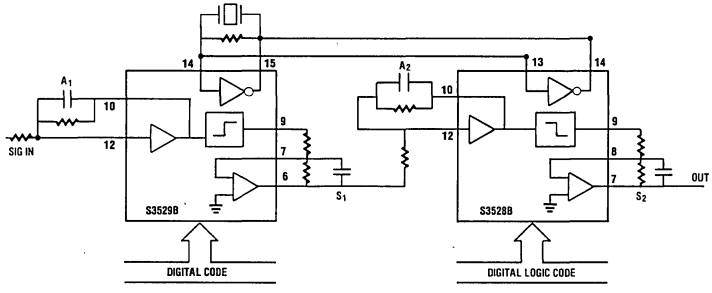
Figure 12. S3528B and S3529B in Parallel Notch Configuration—Wide Bandwidth



Crystal Oscillator

The S3528B crystal oscillator circuit requires a 10 Meg ohm resistor in parallel with a standard 3.58MHz television colorburst crystal. For this application, however, crystals with relaxed tolerances can be used. Specifications can be as follows:

Figure 13. Bandpass Application: General Case Configuration



Note:

— Anti-aliasing and smoothing filters on both chips A1, A2, S1, S2

— Lowpass after highpass to remove higher harmonics, unless cosine input filter of lowpass needed to clean noisy input signal

— For wider band width two different oscillators can be used.

- For same digital logic code
  N = multiple of clock#1 to clock#2

$$f_{cL} = \frac{.9 f_{cu}}{N}$$

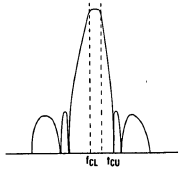


Figure 14. Notch Applications: General Case Configuration

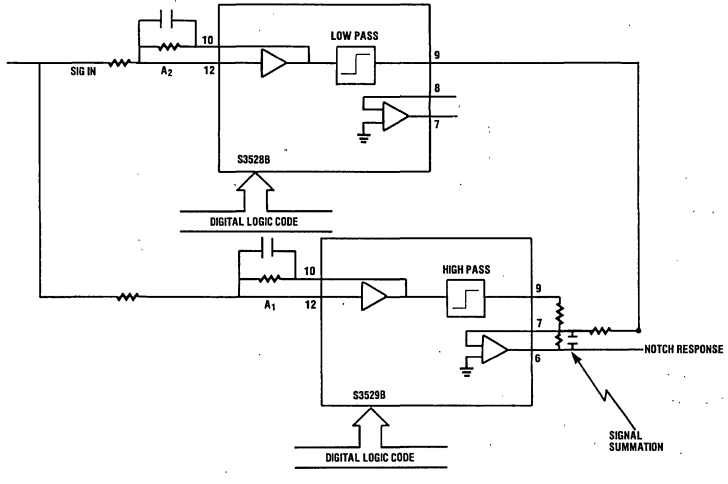
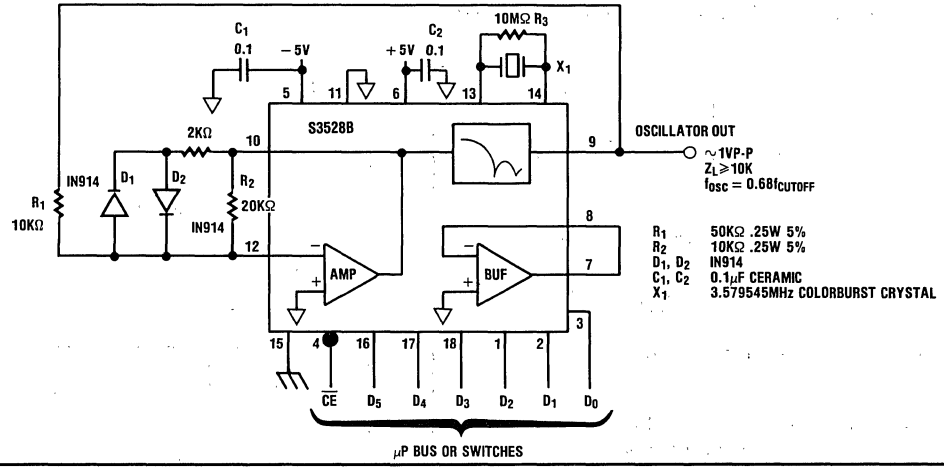


Figure 15. Low Distortion Digitally Tuned Audio Oscillator Application Circuit



Frequency 3.579545 ±.02%
RS≤180Ω L_M~96MH
C_L = 18pF C_h = 7pF

Figure 16. S3528B Driving Additional S3528B or S3529B Devices

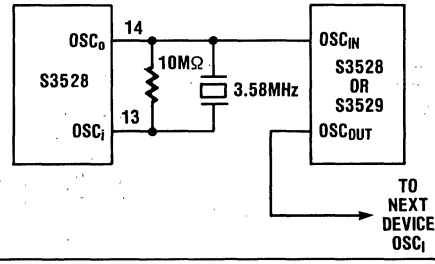
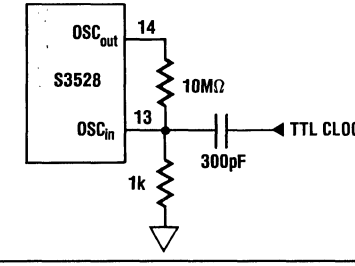


Figure 17. External Driving S3528B Pin OSC_i



Alternate Clock Configurations

If 3.58MHz is already available in the system it can be applied directly as a logic level to the OSC_{IN} (pin 13). [Max. zero~30% (V_{DD}-V_{SS}), min. one~70% (V_{DD}-V_{SS})]. Waveforms not satisfying these logic levels can be capacitively coupled to OSC_{IN} as long as the 10 Meg ohm feedback resistor is installed as shown in Figure 16.

Although the tables are constructed around the TV colorburst crystal, other clock frequencies can be used from crystals or external clocks to achieve any cutoff frequency in the operating range. For example, by using a rate multiplier and duty-cycle restorer circuit between the system clock and the S3528B, and switching the inputs to the S3528B, almost any cutoff frequency between 40Hz and 35kHz can be selected. The clock input frequency can be anywhere between 500kHz and 5MHz.

In addition to crystals or external clocks the S3528B can be used with ceramic resonators such as the Murata CSA series "Ceralock" devices. All that is required is the resonator and 2 capacitors to V_{SS}. Although the resonators are not quite as accurate as crystals they can be less expensive.

GOULD
AMI Semiconductors

Programmable Highpass Filter

S3529B

COMMUNICATION PRODUCTS

Features

- ☐ Cutoff Frequency Selectable in 64 Steps Via Six-Bit Control Word
- ☐ Cutoff Frequency (f_C) Range of 10Hz to 20kHz, 40Hz to 20kHz Via 3.58MHz TV Crystal
- ☐ Seventh Order Elliptical Filter
- ☐ Passband Ripple: 0.1dB
- ☐ Stopband Attenuation: 51dB for f<.77 f_C
- ☐ Clock Tunable Cutoff Frequency Continuously Variable Via External Clock (Crystal, Resonator, or TTL/CMOS Clock)
- ☐ Uncommitted Input and Output Op Amps for Anti-Aliasing and Smoothing Functions
- ☐ Low Power CMOS Technology

Typical Applications for the S3528B and S3529B Programmable Filters

Telecommunications

- ☐ PBX & Trunk Line Status Monitoring
- ☐ Automatic Answering/Forwarding/Billing Systems
- ☐ Adaptive Filtering

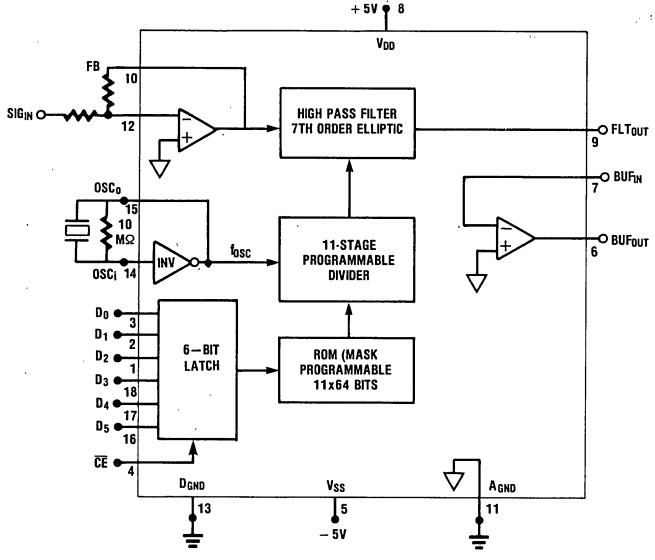
Remote Control

- ☐ Alarm Systems
- ☐ Heating Systems
- ☐ Acoustic Controllers

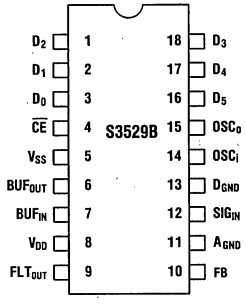
Test Equipment/Instrumentation

- ☐ Spectrum Analyzers
- ☐ Computer Controlled Analog Circuit Testers
- ☐ Medical Telemetry Filtering
- ☐ ECG Signal Filtering
- ☐ Automotive Command Selection and Filtering

Block Diagram



Pin Configuration



S3529B

General Description

The S3529B's CMOS design using switched-capacitor techniques allows easy programming of the filter's cutoff frequency (f_C) in 64 steps via a six-bit control word. For dynamic control of cutoff frequencies, the S3529B can operate as a peripheral to a microprocessor system with the code for the cutoff frequency being latched in from the data bus. When used with the companion low pass filter, the S3528B, a bandpass filter with a variable center frequency is obtained. For special applications the S3529B's internal ROM can be customized to accommodate a specific set of cutoff frequencies from a choice of 2,048 possibilities.

Absolute Maximum Ratings

Supply Voltage ($V_{DD} - V_{SS}$) ..... + 15.0V
Operating Temperature ..... 0°C to + 70°C
Storage Temperature ..... − 65°C to + 150°C
Input Voltage, All Pins ..... $V_{SS} - 0.3V \leq V_{IN} \leq + 0.3V$

D.C. Electrical Operating Characteristics: $T_A = 0°C$ to + 70°C, ($V_{DD} - V_{SS}$) = 10V unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{DD}	Positive Supply (Ref. to V_{SS})	9.0	10	13.5	V
P_D	Power Dissipation @10V		60	110	mW
	@13.5V		135	225	mW
R_{IN}	Input Resistance (Pins 1-4, 7, 12, 14, 16-18)	8			MΩ
C_{IN}	Input Capacitance (Pins 1-4, 7, 12, 14, 16-18)			15.0	pF

Digital Electrical Parameters: V_{DD} = + 5V ±10%, V_{SS} = − 5V ±10%, T_A = 0°C to + 70°C unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	2.0		V_{DD}	V
V_{IL}	Input Low Voltage	V_{SS}		0.8	V
I_N	Input Leakage Current (V_{IN} = 0 to 4VDC)			10	μADC
C_{IN}	Input Capacitance			15	pF

Digital Timing Characteristics

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
t_{CE}	Chip Enable Pulse Width	200	300		ns
t_{AS}	Address Setup Time		300		ns
t_{AH}	Address Hold Time		20		ns
f_{OSC}	Crystal Oscillator Frequency(1)		3.58		MHz
t_{SET}	Settling Time From CE to Stable f_C (f_C = 3200)(2)		6		ms

Notes:

1. The tables are based on the common 3.58MHz color burst TV crystal.
2. $t_{SET} = \frac{10}{f_C} + 3msec$

General Analog Signal Parameters: ($V_{DD} - V_{SS}$) = 10V, T_A = 0°C to +70°C, f_{OSC} = 3.58MHz

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
A_F	Pass Band Gain at 2.2 f_C	−0.5	0	0.5	dB
V_{MAX}	Reference Level Point (0dBm0)		1.5		VRMS
V_{FS}	Maximum Input Signal Level (+3dBm0)		2.1		VRMS
R_L	Load Resistance (FLT_{OUT}, Pin 9)	10			kΩ
R_L	Load Resistance (BUF_{OUT}, Pin 6)	600			Ω
V_{OUT}	Output Signal Level into R_L for FLT_{OUT}, BUF_{OUT}	2.0	2.1		VRMS
T_{HD}	Total Harmonic Distortion: Input code 22, Frequency = 2kHz; Bandlimited to $f_{clk/2}$		.15		%
WBN	Wideband Noise: Input code 22, Bandlimited to 15kHz		.25		mVRMS
V_{OS}	Buffer Output (Pin 6) Offset Voltage		±10		mV
V_{OES}	Filter Output (Pin 9) Offset Voltage		±80		mV

Filter Performance Specifications: High Pass Filter Characteristics (f_{OSC} = 3.58MHz) ($V_{DD} - V_{SS}$) = 10V, T_A = 0°C to +70°C

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
	Passband ripple (Ref. 2.2 f_C) $f_C \leq f < 7f_C$	−0.5	±0.05	0.5	dB
Filter Response: f_C = 1005Hz					
	(f_C) 1005Hz	−0.5	±0.1	0.5	dB
	(0.96 f_C) 960	−5	−3.0	−1	db
	(0.768 f_C) 772		−53	−43	db
	(.754 f_C) 758		−85	−43	db
	(.614 f_C) 617		−70	−43	db
	Stopband $f < .768\ f_C$		< −53		db
DR	Dynamic Range (V_{FS} to WBN)		78		dB

Pin Description

Pin Name	Pin#	Function
V_{DD}	8	Positive supply voltage pin. Normally +5 volts ±10%.
V_{SS}	5	Negative supply voltage pin. Normally −5 volts ±10%.
A_{GND}	11	Analog ground reference point for analog input signals. Normally connected to ground.
D_{GND}	13	Digital ground reference point for digital input signals. Normally connected to ground.
D_0	3	The input bus to allow selection of the desired cutoff frequency. The value of the word presented to these pins selects the cutoff frequency. It is latched in on the rising edge of $\overline{CE}$. These are high impedance CMOS inputs and can be bridged directly across a microprocessor data bus.
D_1	2	
D_2	1	
D_3	18	
D_4	17	
D_5	16	

Pin Description (Continued)

Pin Name	Pin#	Function
$\overline{CE}$	4	Chip Enable: This pin has 3 states. When $\overline{CE}$ is at V_{DD} the data in the latch is presented to the ROM and the inputs have no effect. When $\overline{CE}$ is at ground the data presented on the inputs is read into the latch but the previous data is still in the ROM. Returning $\overline{CE}$ to V_{DD} presents the new data to the ROM and f_{cutoff} changes. When $\overline{CE}$ is at V_{SS} the inputs go directly to the ROM, changing f_{cutoff} immediately. The configuration for a fixed filter is: $\overline{CE}$ at V_{SS} and the D_0 through D_5 are tied to V_{DD} or V_{SS}/D_{GND} depending on the desired f_{cutoff}.
OSC_i	14	Oscillator In and Oscillator Out. Placing a crystal and a 10MΩ resistor across these pins creates the time base
OSC_o	15	oscillator. An inexpensive choice is to use the 3.58MHz TV crystal.
SIG_{IN}	12	Signal Input. This is the inverting input of the input op amp. The non-inverting input is internally connected to Analog Ground.
FB	10	Feedback. This is the feedback point for the input op amp. The feedback resistor should be ⩾10kΩ for proper operation.
FLT_{OUT}	9	The high impedance output of the high pass filter. Load should be 10KΩ.
BUF_{IN}	7	The inverting input of the buffer amplifier.
BUF_{OUT}	6	The buffer amplifier output to drive low impedance loads. Load should be ⩾600Ω.

Example of Circuit Connection for S3529B

Figure 1. Stand Alone Operation

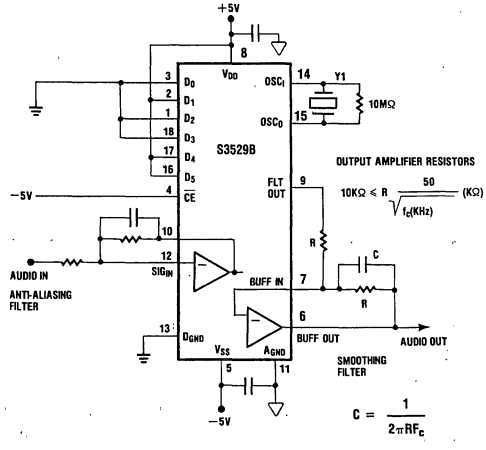


Figure 2. Microprocessor Interface

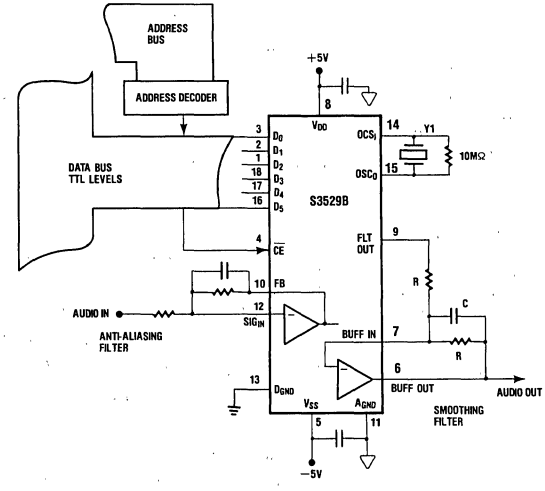


Table 1. Standard Frequency Table: Programmable Filter S3529B, f_{clock} = 3.58MHz

Voice Band Input D_5-D_0 (HEX)	Divider Ratio	f_c Actual (Hz)	Additional Points Input Code D_5-D_0 (HEX)	Divider Ratio	f_c Actual (Hz)
00	2048	40	0A	188	433
01	895	91	0B	358	227
02	447	182	0C	90	904
03	298	273	0D	87	935
04	224	363	0E	85	957
05	179	455	0F	78	1043
06	149	546	1A	61	1334
07	128	635	1B	58	1402
08	112	726	1C	52	1565
09	99	822	1D	46	1768
10	89	914	1E	44	1849
11	81	1005	1F	40	2034
12	74	1099	2A	38	2136
13	69	1179	2B	35	2325
14	64	1271	2C	22	3697
15	60	1355	2D	20	4067
16	56	1453	2E	18	4519
17	53	1535	2F	16	5085
18	50	1627	35	15	5423
19	47	1731	38	14	5811
20	45	1808	3A	12	6779
21	43	1892	3B	10	8135
22	41	1985	3C	9	9039
23	39	2086	3D	6	13559
24	37	2198	3E	5	16270
25	36	2260	3F	4	20338
26	34	2392			
27	33	2465			
28	32	2543			
29	31	2625			
30	30	2712			
31	29	2805			
32	28	2905			
33	27	3013			
34	26	3129			
36	25	3254			
37	24	3389			
39	23	3537			

$$f_{CUTOFF} = \frac{f_{clock}}{44\ (\text{Divider Ratio})}$$

Alternate Clock Configurations

If 3.58MHz is already available in the system it can be applied directly as a logic level to the OSC_{IN} (pin 14). (Max. zero~30% V_{DD}, min. one~70% V_{SS}). Waveforms not satisfying these logic levels can be capacitively coupled to OSC_{IN} as long as the 10MΩ feedback resistor is installed as shown in Figure 3.

Figure 3. External Driving S3529B Pin OSC_I

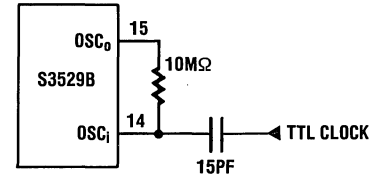


Figure 4. Passband Detail, Control = 110010, f_c = 1005Hz

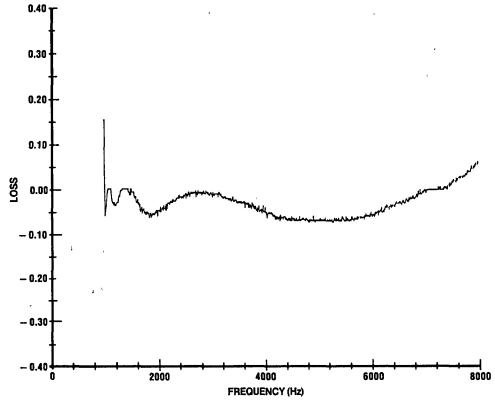


Figure 5. Loss Curve, Control = 110010, f_c = 1005Hz

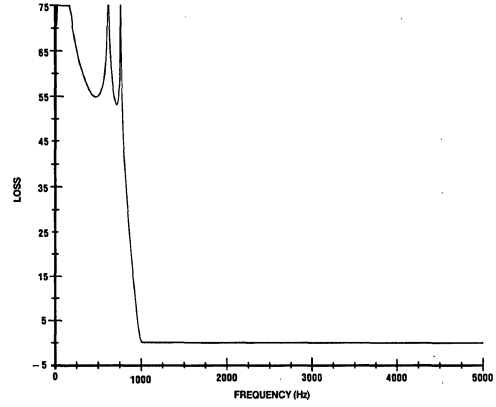


Figure 6. Loss Response, DC to Clock Detail, Control = 110010, f_c = 1005Hz

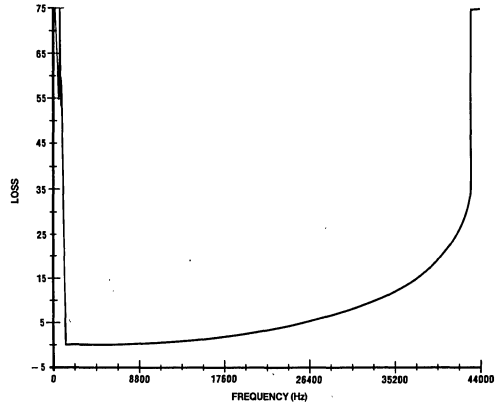


Figure 7. Cascaded S3528B and S3529B, Control = 100001 Bandpass Configuration—10% Bandwidth

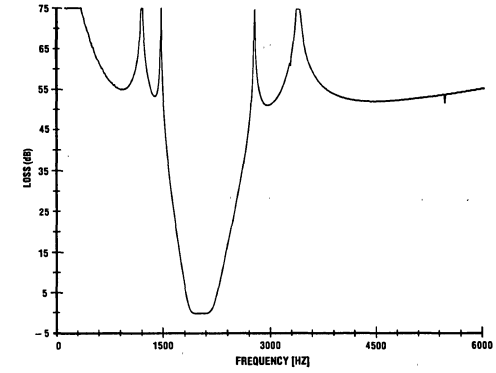


Figure 8. S3528B and S3529B in Parallel, Notch Configuration—Narrow Bandwidth

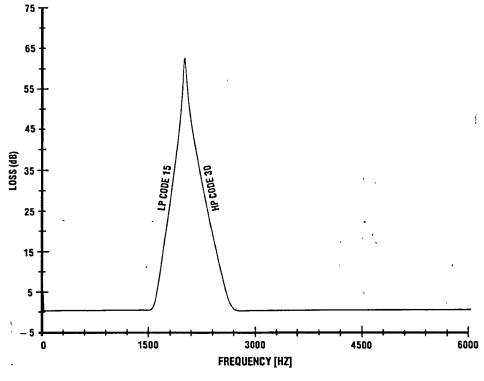
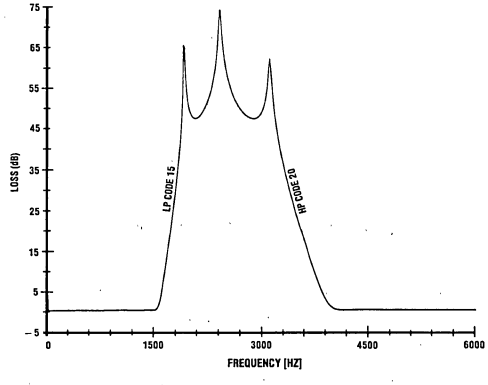


Figure 9. S3528B and S3529B in Parallel, Notch Configuration—Wide Bandwidth

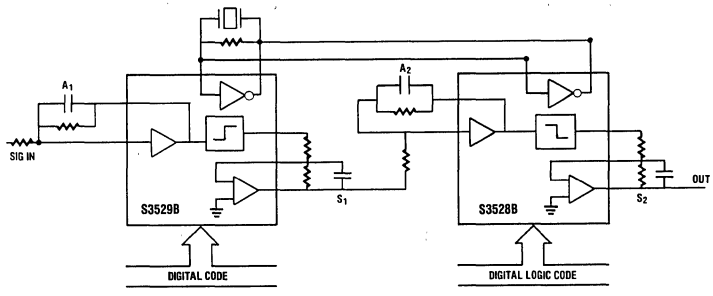


Applications Information

The S3529B High Pass Filter has a very sharp 50dB drop off at f_C. The Passband Ripple is less than 0.5dB. Note that unlike passive element filter, attenuation increases for sampled-data filters at the higher frequencies due to the sample and hold effect. ($f_{CLOCK} = 44xf_{CUTOFF}$).

The S3529B High Pass Filter and the S3528B Low Pass Filter can be used together to make either Band Pass or Band Reject filters. The control code selection determines the bandwidth of the resulting filter.

Figure 10. Bandpass Application: General Case Configuration



Note:

— Anti-aliasing and smoothing filters on both chips A1, A2, S1, S2

— Lowpass after highpass to remove higher harmonics, unless cosine input filter of lowpass needed to clean noisy input signal

— For wider band width two different oscillators can be used.

— If filter clock (f_{clock}) for lowpass is an integer multiple of the f_{clock} for highpass, then S1 and A2 may be removed without causing beat frequencies.

- For same digital logic code
  N = multiple of clock#1 to clock#2

$$f_{cL} = \frac{.9 f_{cu}}{N}$$

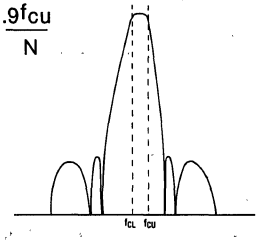


Figure 11. Notch Applications: General Case Configuration

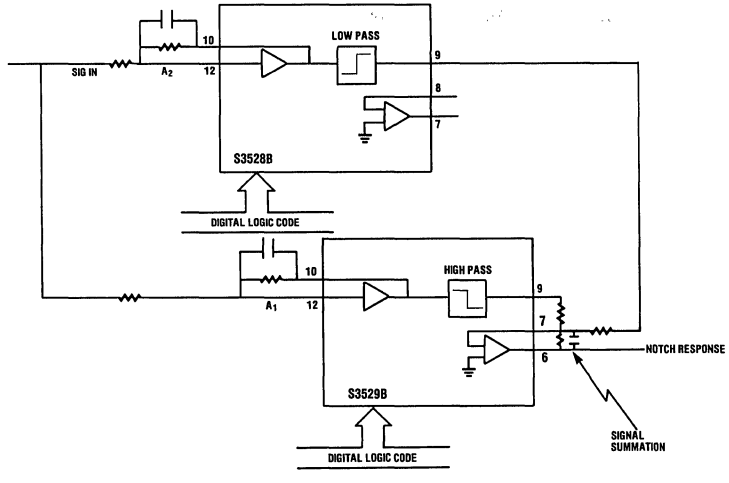


Figure 12. Sampling Theory

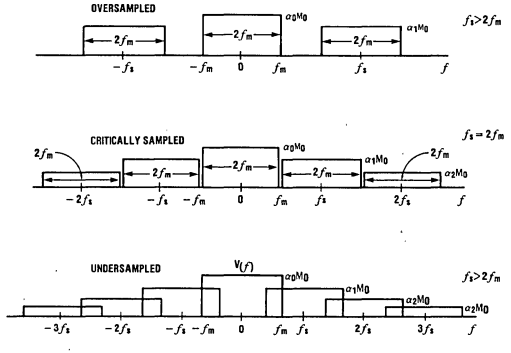
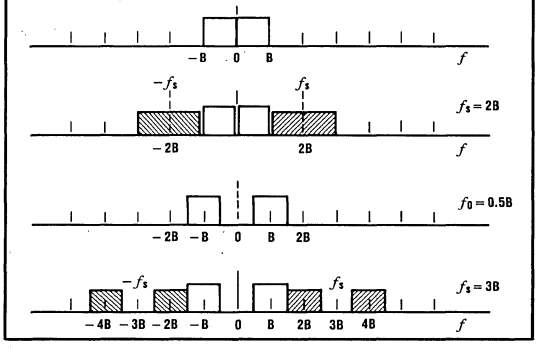
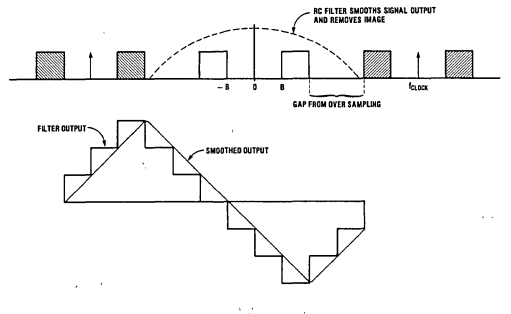


Figure 13. Avoiding Aliasing



Note that critical sampling avoids aliasing, but in the above example no real life filter can separate the message from the image. One must oversample in real life.

Figure 14. Implementation



Applications Information

Anti-Aliasing

fs = sampling frequency
fm = frequency bandwidth of message

In planning an application the fundamentals of sampling devices must be considered.

☐ Make certain the harmonic image does not fold into the desired pass band. i.e, Oversample.

☐ Bandlimit the input so that the input frequencies, noise, and tails will not come too close to the clock and be folded back into the pass band.

☐ Bandlimit the output so that the image is sufficiently attenuated and the switched capacitor output is smoothed. i.e., kill the higher order terms in the Fourier Series.

☐ For dynamic operation check for aliasing at each cutoff frequency.

GOULD

AMI Semiconductors

Industrial Temperature CMOS Single Chip μ-Law/A-Law Synchronous Combo Codecs With Filters

S3506I/S3507I/S3507AI

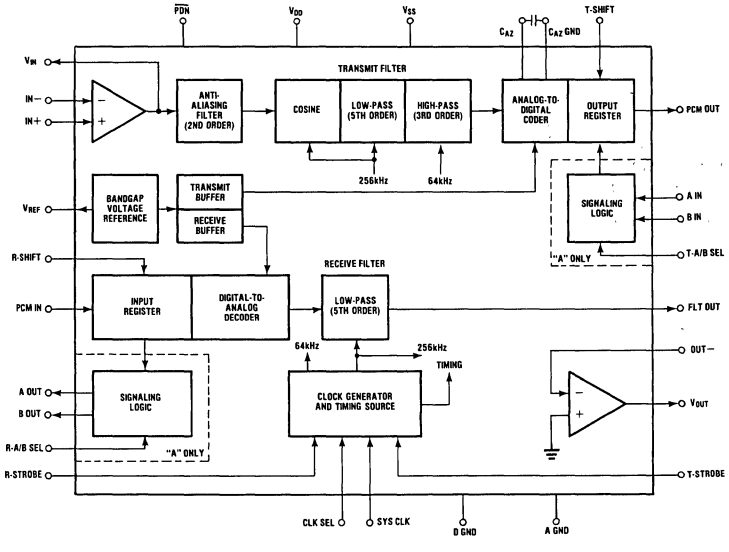
Features

- ☐ Independent Transmit and Receive Sections With 75dB Isolation
- ☐ Low Power CMOS 80mW (Operating) 10mW (Standby)
- ☐ Stable Voltage Reference On-Chip
- ☐ Meets or Exceeds AT&T D3, and CCITT G.711, G.712 and G.733 Specifications
- ☐ Input Analog Filter Eliminates Need for External Anti-Aliasing Prefilter
- ☐ Input/Output Op Amps for Programming Gain
- ☐ Output Op Amp Provides ±3.1V into a 600Ω Load or Can Be Switched Off for Reduced Power(70mW)
- ☐ Special Idle Channel Noise Reduction Circuitry for Crosstalk Suppression
- ☐ Encoder has Dual-Speed Auto-Zero Loop for Fast Acquisition on Power-up
- ☐ Low Absolute Group Delay = 450μsec @ 1kHz

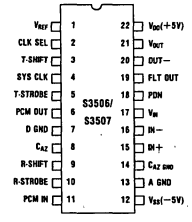
General Description

The S3506 and S3507 are monolithic silicon gate CMOS Companding Encoder/Decoder chips designed to implement the per channel voice frequency Codecs used in PCM systems. The chips contain the band-limiting filters and the analog↔digital conversion circuits that conform to the desired transfer characteristic. The S3506 provides the European A-Law companding and the S3507 provides the North American μ-Law companding characteristic.

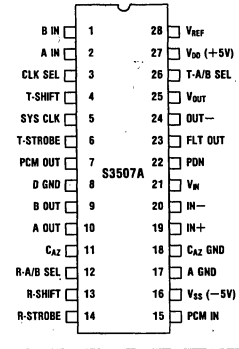
Block Diagram



Pin Configuration (22 Pin)



Pin Configuration (28 Pin)



S3506I/S3507I/S3507AI

General Description (Continued)

These circuits provide the interface between the analog signals of the subscriber loop and the digital signals of the PCM highway in a digital telephone switching system. The devices operate from dual power supplies of ±5V.

For a sampling rate of 8kHz, PCM input/output data rate can vary from 64kb/s to 2.1Mb/s. Separate transmit/receive timing allows synchronous or time-slot asynchronous operation.

In 22-pin cerdip or ceramic packages (.400" centers) the S3506/S3507 are ideally suited for PCM applications: Exchange, PABX, or Digital Telephone as well as fiber optic and other non-telephone uses. A 28-pin version, the S3507A, provides standard μ-Law A/B signaling capability. These devices are also available in a 28-pin chip carrier.

Absolute Maximum Ratings

DC Supply Voltage V_{DD}	+6.0V
DC Supply Voltage V_{SS}	−6.0V
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Power Dissipation at 25°C	1000mW
Digital Input	$V_{SS} - 0.3 \leq V_{IN} \leq V_{DD} + 0.3$
Analog Input	$V_{SS} - 0.3 \leq V_{IN} \leq V_{DD} + 0.3$

Electrical Operating Characteristics ($T_A = -46°$ to 90°C)

Power Supply Requirements

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{DD}	Positive Supply	4.75	5.0	5.25	V	
V_{SS}	Negative Supply	−4.75	−5.0	−5.25	V	
P_{OPR}	Power Dissipation (Operating)		80	140	mW	
P_{OPR}	Power Dissipation (Operating w/o Output Op Amp		70		mW	V_{DD} = 5.0V
P_{STBY}	Power Dissipation (Standby)		10	25	mW	V_{DD} = −5.0V

AC Characteristics (Refer to Figures 3A and 4A)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
D_{SYS}	System Clock Duty Cycle	40	50	60	%	
f_{SC}	Shift Clock Frequency	0.064		2.048	MHz	
D_{SC}	Shift Clock Duty Cycle	40	50	60	%	
t_{rc}	Shift Clock Rise Time			100	ns	
t_{fc}	Shift Clock Fall Time			100	ns	
t_{rs}	Strobe Rise Time			100	ns	
t_{fs}	Strobe Fall Time			100	ns	
t_{sc}	Shift Clock to Strobe (On) Delay	−100	0	200	ns	
t_{sw}	Strobe Width	600ns		124.3μs	@2.048 MHz	700ns min @1.544MHz

AC Characteristics (continued) (Refer to Figures 3A and 4A)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{cd}	T-Shift Clock to PCM OUT Delay		100	150	ns	100pF, 510Ω Load
t_{dc}	R-Shift Clock to PCM IN Set-Up Time	60			ns	
t_{rd}	PCM Output Rise Time $C_L = 100pF$		50	100	ns	to 3V; 510Ω to V_{DD}
t_{fd}	PCM Output Fall Time $C_L = 100pF$		50	100	ns	to .4V; 510Ω to V_{DD}
t_{dss}	A/B Select to Strobe Trailing Edge Set-up Time	100			ns	

DC Characteristics ($V_{DD} = +5V, V_{SS} = -5V$)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
R_{INA}	Analog Input Resistance IN+, IN−	100			KΩ	
C_{IN}	Input Capacitance to Ground		7	15	pF	All Logic and Analog Inputs
	R-Shift Clock, T-Shift Clock, PCM IN, System Clock, Strobe, $\overline{PDN}$					
I_{INL}	Logic Input Low Current			1	μA	$V_{IL} = 0.8V$
I_{INH}	Logic Input High Current			1	μA	$V_{IH} = 2.0V$
	T-A/B SEL, A IN, B IN, R-A/B SEL					
I_{INL}	Logic Input Low Current			600	μA	$V_{IL} = 0.8V$
I_{INH}	Logic Input High Current			600	μA	$V_{IH} = 2.0V$
V_{IL}	Logic Input "Low" Voltage			0.8	V	
V_{IH}	Logic Input "High" Voltage	2.0			V	
V_{OL}	Logic Output "Low" Voltage (PCM Out)			0.4	V	510Ω Pull-up to V_{DD} + 2 LSTTL
V_{OL}	Logic Output "Low" Voltage (A/B OUT)			0.4	V	$I_{OL} = 1.6mA$
V_{OH}	Logic Output "High" Voltage	2.4			V	$I_{OH} = 40\mu A$
R_L	Output Load Resistance V_{OUT}	600			Ω	

Transmission Delays

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
	Encoder		125		μs	From T_{STROBE} to the Start of Digital Transmitting
	Decoder	30	8T + 25		μs	T = Period in μs of R_{SHIFT} CLOCK
	Transmit Section Filter			182	μs	@1kHz
	Receive Section Filter			110	μs	@1kHz

S3506 Single-Chip A-Law Filter/Codec Performance

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
ICN_W	Idle Channel Noise (Weighted Noise)			−85	−66.5	dBm0p	CCITT G.712 4.1
ICN_{SF}	Idle Channel Noise (Single Frequency Noise)				−60	dBm0	CCITT G.712 4.2
ICN_R	Idle Channel Noise (Receive Section)				−74	dBm0p	CCITT G.712 4.3
	Spurious Out-of-Band Signals at Channel Output				−28	dBm0	CCITT G.712 6.1
IMD_{2F}	Intermodulation (2 Tone method)				−35	dBm	CCITT G.712 7.1
IMD_{PF}	Intermodulation (1 Tone + Power Frequency)				−49	dBm	CCITT G.712 7.2
	Spurious In-Band Signals at the Channel Output Port				−40	dBm0	CCITT G.712 9
	Interchannel Crosstalk $V_{IN} - V_{OUT}$		75	80		dB	CCITT G.712 11
$V_{IN(Max)}$	Max Coding Analog Input Level			±3.1		V_{0pk}	
V_{OUT} (Max)	Max Coding Analog Output Level			±3.1		V_{0pk}	$R_L = 600\Omega$
AD	Absolute Delay End-to-End @ 1KHz			450	500	μsec	@ 0dBm0
ED	Envelope Delay Distortion	500 to 600Hz		200	750	μsec	Relative to Minimum Delay Frequency
		600 to 1000Hz		120	375	μsec	
		1000Hz to 2600Hz		110	125	μsec	
		2600Hz to 2800Hz		160	750	μsec	
SD	Signal to Total Distortion	0 to −30dBm0	33.5	39		dB	Method 2 - Sine-wave Signal Used
		−40dBm0	27.5	31		dB	
		−45dBm0	22.5	26		dB	
FR	Frequency Response 300Hz to 3000Hz				±.25	dB	
GT	Gain Tracking with Input Level Variations (End-to-End. Each half channel is one half this value.)			±0.2 ±0.4 ±1.0	±0.5 ±1.0 ±3.0	dB	+3 to −40 dBm0 −45 to −50 dBm0 −55dBm0
ΔG	Gain Variation with Temperature and Power Supply Variation			±0.25		dB	
	Transmit Gain Repeatability			±0.1	±0.2	dB	
	Receive Gain Repeatability			±0.1	±0.2	dB	
$OTLP_R$	Zero Transmission Level Point (Decoder See Figure 1)			1.51		VRMS	V_{OUT} Digital Milliwatt Response
$OTLP_T$	Zero Transmission Level Point (Encoder See Figure 1)			1.51		VRMS	V_{IN} to Yield Same as Digital Milliwatt Response at Decoder

S3507/S3507A Single-Chip μ-Law Filter/Codec Performance

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
ICN_W	Idle Channel Noise (Weighted Noise)			5	−66.5	dBm0	
ICN_{SF}	Idle Channel Noise (Single Frequency Noise)				−60	dBm0	
ICN_R	Idle Channel Noise (Receive Section)				−74	dBm0	
	Spurious Out-of-Band Signals at the Channel Output				−28	dBm0	
$OTLP_T$	Zero Transmission Level Point (Encoder See Figure 1)			1.51		VRMS	V_{IN} to Yield Same as Digital Milliwatt Response at Decoder
$OTLP_R$	Zero Transmission Level Point (Decoder See Figure 1)			1.44		VRMS	V_{OUT} Digital Milliwatt Response
AD	Absolute Delay End-to-End @ 1KHz			450	500	μsec	@ 0dBm0
ED	Envelope Delay	500 to 600Hz		200	750	μsec	Relative to
		600 to 1000Hz		120	375	μsec	Minimum
	Distortion	1000Hz to 2600Hz		110	125	μsec	Delay
		2600Hz to 2800Hz		160	750	μsec	Frequency
SD	Signal to	0 to −30dBm0	33.5	39		dB	
	Total	−40dBm0	27.5	31		dB	
	Distortion	−45dBm0	22.5	26		dB	
FR	Frequency Response 300Hz to 3000Hz				±.25	dB	
IMD_{2F}	Intermodulation (2 Tone method)				−35	dBm	
IMD_{PF}	Intermodulation (1 Tone + Power Frequency)				−49	dBm	
	Spurious In-Band Signals at the Channel Output Port				−40	dBm0	
	Interchannel Crosstalk $V_{IN}-V_{OUT}$		75	80		dB	
$V_{IN(Max)}$	Max Coding Analog Input Level			±3.1		V_{0pk}	
$V_{OUT(Max)}$	Max Coding Analog Output Level			±3.1		V_{0pk}	$R_L=600\Omega$
GT	Gain Tracking with Input Level Variations (End-to-End. Each Half Channel is One Half of this Value.)			±0.2	±0.5	dB	+3 to −40 dBm0
				±0.4	±1.0	dB	−45 to −50 dBm0
				±1.0	±3.0	dB	−55 dBm0
△G	Gain Variation with Temperature and Power Supply Variation			±0.25		dB	
	Transmit Gain Repeatability			±0.1	±0.2	dB	
	Receive Gain Repeatability			±0.1	±0.2	dB	

Pin/Function Descriptions

Pin	S3506/S3507	S3507A	Description
SYS CLK	4	5	**System Clock**—This pin is a TTL compatible input for a 256kHz, 1.544MHz, 2048MHz, or 1.536MHz clock that is divided down to provide the filter clocks. The status of CLK SEL pin must correspond to the provided clock frequency.
T-SHIFT	3	4	**Transmit Shift Clock**—This TTL compatible input shifts PCM data out of the coder on the positive going edges after receiving a positive edge on the T-STROBE input. The clocking rate can vary from 64kHz to 2.048MHz.
R-SHIFT	9	13	**Receive Shift Clock**—This TTL compatible input shifts PCM data into the decoder on the negative going edges after receiving a positive edge on the R-STROBE input. The clocking rate can vary from 64kHz to 2.048MHz.
T-STROBE	5	6	**Transmit Strobe**—This TTL compatible pulse input (8kHz) is used for analog sampling and for initiating the PCM output from the coder. It must be synchronized with the T-SHIFT clock with its positive going edges occurring with the positive edge of the shift clock. The width of this signal is not critical. An internal bit counter generates the necessary timing for PCM output.
R-STROBE	10	14	**Receive Strobe**—This TTL compatible pulse input (8kHz) initiates clocking of PCM input data into the decoder. It must be synchronized with the R-SHIFT clock with its positive going edges occurring with the positive edge of the shift clock. The width of the signal is not critical. An internal bit counter generates necessary timing for PCM input.
CLK SEL	2	3	**Clock Select**—This pin selects the proper divide ratios to utilize either 256kHz, 1.544MHz, 2.048MHz, or 1.536MHz as the system clock. The pin is tied to V_{DD} (+5V) for 2.048MHz, to V_{SS} (−5V) for 1.544MHz or 1.536MHz operation, or to D GND for 256kHz operation.
PCM OUT	6	7	**PCM Output**—This is a LS-TTL compatible open-drain output. It is active only during transmission of PCM output for 8 bit periods of T-SHIFT clock signal following a positive edge of the T-STROBE input. Data is clocked out by the positive edge of the T-SHIFT clock into one 510Ω pull-up per system plus 2 LS-TTL inputs.
PCM IN	11	15	**PCM Input**—This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of T-SHIFT clock.
C_{AZ} C_{AZ} GND	8 14	11 18	**Auto Zero**—A capacitor of 0.1μF ±20% should be connected between these pins for coder auto zero operation. Sign bit of the PCM data is integrated and fed back to the comparator for DC offset cancellation.
V_{REF}	1	28	**Voltage Reference**—Output of the internal band-gap reference voltage (≈−3.075V) generator is brought out to V_{REF} pin. Do not load this pin.
IN+ IN− V_{IN}	15 16 17	19 20 21	These pins are for analog input signals in the range of $-V_{REF}$ to $+V_{REF}$. IN− and IN+ are the inputs of a high input impedance op amp and V_{IN} is the output of this op amp. These three pins allow the user complete control over the input stage so that it can be connected as a unity gain amplifier, amplifier with gain, amplifier with adjustable gain or as a differential input amplifier. The adjustable gain configuration will facilitate calibration of the transmit channel. V_{IN} should not be loaded by less than 47K ohms.
FLT OUT	19	23	**Filter Out**—This is the output of the low pass filter which represents the recreated analog signal from the received PCM data words. The filter sample frequency of 256kHz is down 37dB at this point. This is a high impedance output which can be used by itself or connected to the output amplifier stage which has a low output impedance. It should not be loaded by less than 47K ohms, or the Digital MilliWatt response will fall off slightly.

Pin/Function Descriptions (Continued)

Pin	S3506/S3507	S3507A	Description
OUT− V_{OUT}	20 21	24 25	These two pins are the output and input of the uncommitted output amplifier stage. Signal at the FLT OUT pin can be connected to this amplifier to realize a low output impedance with unity gain, increased gain or reduced gain. This allows easier calibration of the receive channel. The V_{OUT} pin has the capability of driving 0dBm into a 600Ω load. (See Figure 1). If OUT− is connected directly to V_{SS} the op amp will be powered down, reducing power consumption by 10mW, typically.
V_{DD} V_{SS}	22 12	27 16	These are power supply pins. V_{DD} and V_{SS} are positive and negative supply pins, repectively (typ. +5V, −5V). V_{DD} should be applied first.
A GND D GND	13 7	17 8	Analog and digital ground pins are separate for minimizing crosstalk.
$\overline{PDN}$	18	22	**Power Down**—This TTL compatible input when held low puts the chip into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high or low, but as long as they are static, the powered down mode is in effect. Should be tied to +5 when not used.
A IN B IN T-A/B SEL		2 1 26	The transmit A/B select input selects the A signal input on a positive transition and the B signal input on the negative transition. These inputs are TTL compatible. The A/B signaling bits are sent in bit 8 of the PCM word in the frame following the frame in which T-A/B SEL input makes a transition. A common A/B select input can be used for all channels in a multiplex operation, since it is synchronized to the T-STROBE input in each device.
A OUT B OUT R-A/B SEL		10 9 12	In the decoder the A/B signaling bits received in the PCM input word are latched to the respective outputs in the same frame in which the R-AB SEL input makes a transition. A bit is latched on a positive transition and B bit is latched on a negative transition. A common A/B select input can be used for all channels in a multiplex operation.

Functional Description

The simplified block diagram of the S3506/S3507 appears on page one. The device contains independent circuitry for processing transmit and receive signals. Switched capacitor filters provide the necessary bandwidth limiting of voice signals in both directions. Circuitry for coding and decoding operates on the principle of successive approximation, using charge redistribution in a binary weighted capacitor array to define segments and a resistor chain to define steps. A bandgap voltage generator supplies the reference level for the conversion process.

Transmit Section

Input analog signals first enter the chip at the uncommitted op amp terminals. This op amp allows gain trim to be used to set 0TLP in the system. From the V_{IN} pin the signal enters the 2nd order analog antialiasing filter. This filter eliminates the need for any offchip filtering as it provides attenuation of 34dB (typ.) at 256kHz and 46dB (typ.) at 512Hz. From the Cosine Filter the signal enters a 5th Order Low-Pass Filter clocked at 256kHz, followed by a 3rd Order High-Pass Filter clocked at 64kHz. The resulting band-pass characteristics meet the CCITT G.711, G.712 and G.733 specifications. Some representative attenuations are >26dB (typ) from 0 to 60Hz and >35dB (typ) from 4.6kHz to 100kHz. The output of the high pass filter is sampled by a capacitor array at the sampling rate of 8kHz. The polarity of the incoming signal selects the appropriate polarity of the reference voltage. The successive approximation analog-to-digital conversion process requires 9½ clock cycles, or about 72μs. A switched capacitor dual-speed, auto-zero loop using a small non-critical external capacitor (0.1μF) provides DC offset cancellation by integrating the sign bit of the PCM data and feeding it back to the non-inverting input of the comparator.

The PCM data word is formatted according to the μ-law companding curve for the S3507 with the sign bit and the ones complement of the 7 magnitude bits according to the AT&T D3 specification. In the S3506 the PCM data word is formatted according to the A-Law companding curve with alternate mark inversion (AMI), meaning that the even bits are inverted per CCITT specifications.

Included in the circuitry of the S3507/S3507A is "All Zero" code suppression so that negative input signal values between decision value numbers 127 and 128 are encoded as 00000010. This prevents loss of repeater synchronization by T1 line clock recovery circuitry as there are never more than 15 consecutive zeros. The 8-bit PCM data is clocked out by the transmit shift clock which can vary from 64kHz to 2.048MHz.

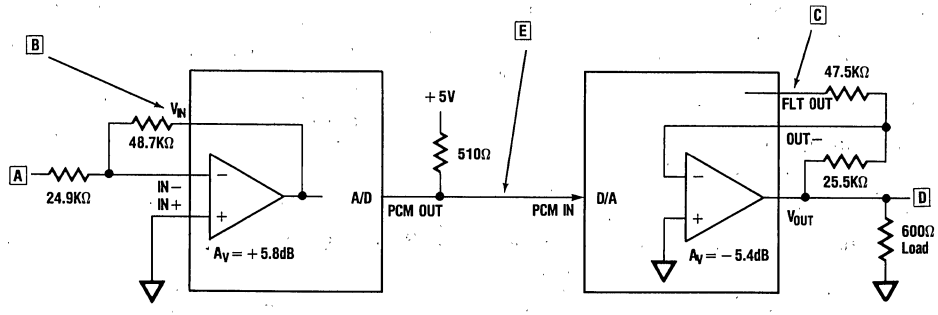
Idle Channel Noise Suppression

An additional feature of the CODEC is a special circuit to eliminate any transmitted idle channel noise during quiet periods. When the input of the chip is such that for 250msec. the only code words generated were +0, −0, +1, or −1, the output word will be a +0. The steady +0 state prevents alternating sign bits or LSB from toggling and thus results in a quieter signal at the decoder. Upon detection of a different value, the output resumes normal operation, resetting the 250msec. timer. This feature is a form of Idle Channel Noise or Crosstalk Suppression. It is of particular importance in the S3506 A-Law version because the A-Law transfer characteristic has "mid-riser" bias which enhances low level signals from crosstalk.

Receive Section

A receive shift clock, variable between the frequencies of 64kHz to 2.048MHz, clocks the PCM data into the input buffer register once every sampling period. A charge proportional to the received PCM data word appears on the decoder capacitor array. A sample and hold initialized to zero by a narrow pulse at the beginning of each sampling period integrates the charge and holds for the rest of the sampling period. A switched-capacitor 5th Order Low-Pass Filter clocked at 256kHz smooths the sampled and held signal. It also performs the loss equalization to compensate for the sin x/x distortion due to the sample and hold operation. The filter output is available for driving electronic hybrids directly as long as the impedance is greater than 47kΩ. When used in this fashion the low impedance output amp can be switched off for a savings in power consumption. When it is required to drive a 600Ω load the output is configured as shown in Figure 1 allowing gain trimming as well as impedance matching. With this configuration a transmission level of 0dBm can be delivered into the load with the +3.14dB or +3.17dB overload level being the maximum expected level.

Figure 1. S3507 Input/Output Reference Signal Levels



The resistors are illustrated for a 0dBm IN/0dBm OUT system. Point [A] bridges a 600Ω termination and Point [D] drives a 600Ω load (illustrated). The 0dBm level produces the equivalent digital milliwatt code at Point [E] as defined in the AT&T and CCITT specifications for PCM. This is called the zero transmission level point or OTLP and 3.17dB of overload capability remains before saturation occurs.

	[A]	[B]	[C]	[D]	[E]
Voltage for OTLP	.775VRMS 1.10Vpk	1.51VRMS 2.13Vpk	1.44VRMS 2.04Vpk	.775VRMS 1.10Vpk	Digital Milliwatt Code per AT&T/CCITT
Voltage for Saturation	1.12VRMS 1.58Vpk	2.17VRMS 3.075Vpk	2.07VRMS 2.93Vpk	1.12VRMS 1.58Vpk	Saturation Codes

Power Down Logic

Powering down the CODEC can be done in several ways. The most direct is to drive the PDN pin to a low level. Stopping both the transmit strobe and the receive strobe will also put the chip into the stand-by mode. The strobes can be held high or low.

Voltage Reference Circuitry

A temperature compensated band-gap voltage generator (−3.075V) provides a stable reference for the coder and decoder. Two amplifiers buffer the reference and supply the coder and decoder independently to minimize crosstalk. This reference voltage is trimmed during assembly to ensure a minimum gain error of ±0.2dB due to all causes. The V_{REF} pin should not be connected to any load.

Power Supply and Clock Application

For proper operation V_{DD} and V_{SS} should be applied simultaneously. If not possible, then V_{SS} should be applied first. To avoid forward-biasing the device the clock voltages should not be applied before the power supply voltages are stable. When cards must be plugged into a "hot" system it may be necessary to install 1000Ω current-limiting resistors in series with the clock lines to prevent latch-up.

Timing Requirements

The internal design of the Single-Chip CODEC paid careful attention to the timing requirements of various systems. In North America, central office and channelbank designs follow the American Telephone and Telegraph Company's T1 Carrier PCM format to multiplex 24 voice channels at a data rate of 1.544Mb/s. PABX designs, on the other hand, may use their own multiplexing formats with different data rates. Yet, in digital telephone designs, CODEC's may be used in a non-multiplexed form with a data rate as low as 64kb/s. The S3507 and S3507A fill these requirements.

In Europe, telephone exchange and channelbank designs follow the CCITT carrier PCM format to multiplex 30 voice channels at a data rate of 2.048Mb/s. The S3506 is designed for this market and will also handle PABX and digital telephone applications requiring the A-Law transfer characteristics.

The timing format chosen for the AMI Codec allows operation in both multiplexed or non-multiplexed form with data rates variable from 64kb/s to 2.048Mb/s. Use of separate internal clocks for filters and for shifting of PCM input/output data allows the variable data rate capability. Additionally, the S3506/S3507 does not require that the 8kHz transmit and receive sampling strobes be exactly 8 bit periods wide. The device has an internal bit counter that counts the number of data bits shifted. It is reset on the leading (+) edges of the strobe, forcing the PCM output in a high impedance state after the 8th bit is shifted out. This allows the strobe signal to have any duty cycle as long as its repetition rate is 8kHz and transmit/receive shift clocks are synchronized to it. Figure 2 shows the waveforms in typical multiplexed uses of the CODEC.

System Clock

The basic timing of the Codec is provided by the system clock. This 2.048MHz, 1.544MHz, or 256kHz clock is divided down internally to provide the various filter clocks and the timing for the conversions. In most systems this clock will also be used as the shift clock to clock in and out the data. However, the shift clock can actually be between 64kHz and 2.048MHz as long as one of the system clock frequencies is provided. Independent strobes and shift clocks allow asynchronous time slot operation of transmit and receive. The 3507 will also operate with a 1.536MHz system clock, as used in some PABX systems, with the CLK SEL pin in the 1.544MHz Mode.

Signaling in μ-Law Systems

The S3506 and S3507 are compact 22-pin devices to meet the two worldwide PCM standards. In μ-Law systems there can be a requirement for signaling information to be carried in the bit stream with the coded analog data. This coding scheme is sometimes called 7-5/6 bit rather than 8 bit because the LSB of every 6th frame is replaced by a signaling bit. This is referred to as A/B Signaling and if a signaling frame carries the "A" bit, then 6 frames later the LSB will carry the "B" bit. To meet this requirement, the S3507A is available in a 28-pin dip package, or in a 28-pin chip carrier, as 6 more pins are required for the inputs and outputs of the A/B signaling.

Pin Configuration—S3507A 28-Lead Chip Carrier

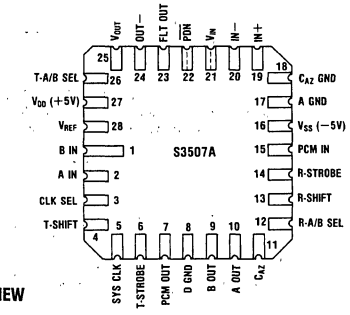
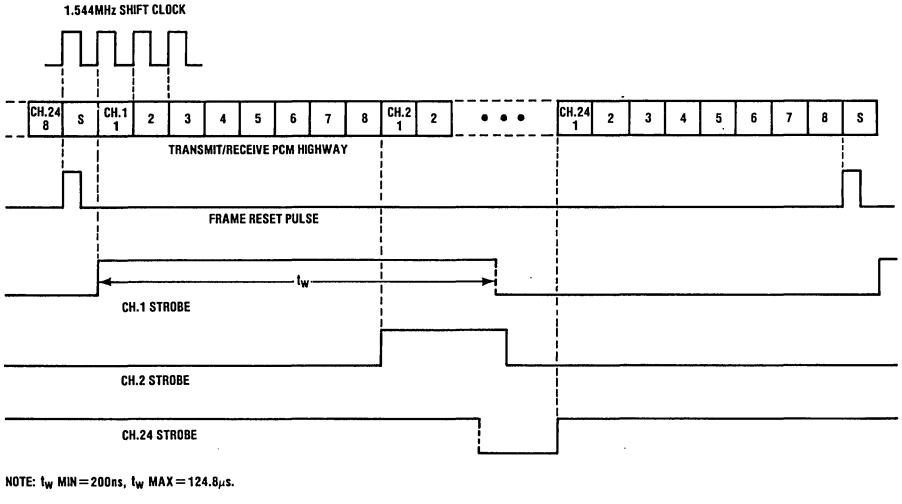
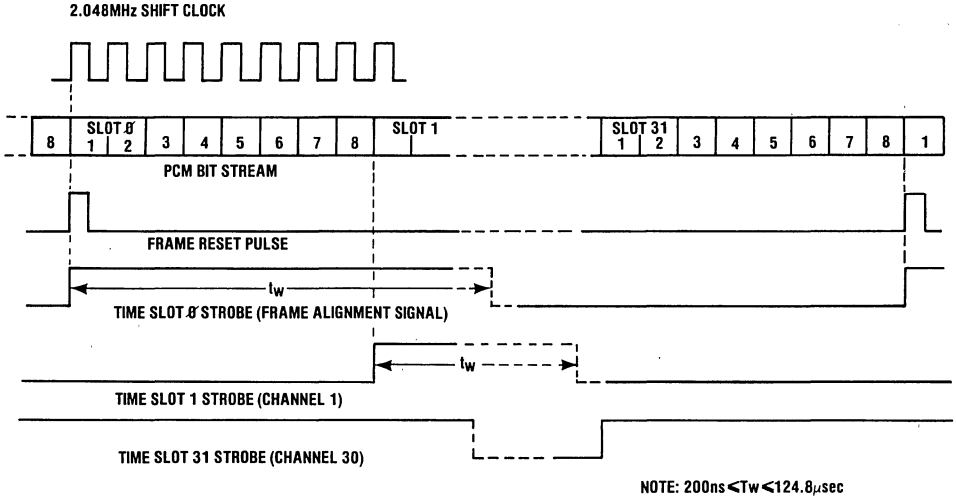


Figure 2A. Waveforms in a 24 Channel PCM System



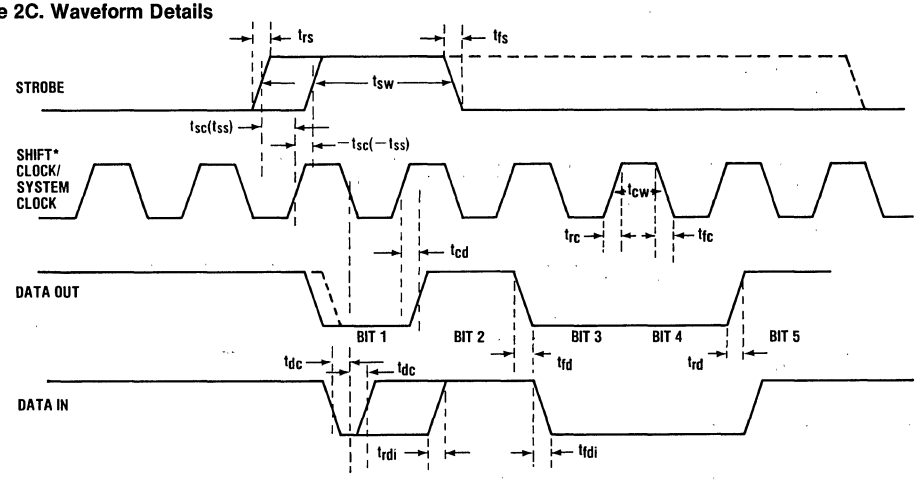
NOTE: t_W MIN = 200ns, t_W MAX = 124.8μs.

Figure 2B. Waveforms in 30 Channel PCM System



NOTE: 200ns $\leq$ Tw $\leq$ 124.8μsec

Figure 2C. Waveform Details



*In this example, the shift clock is the system clock (1.544 or 2.048MHz). In systems where the data shift rate is not the same, the relationship of each to the strobe remains the same. The system clock and shift clock must relate to the strobe within the t_{sc}, t_{ss} timing requirements.

The effect of the strobe occurring after the shift clock is to shorten the first (sign) bit at the data output.

The length of the strobe is not critical. It must be at a logic state longer than one system clock cycle. Therefore, the minimum would be >488ns at 2.048 and the maximum <124.3μsec at 1.544MHz.

	MIN	MAX
t_{cw}	195nsec.	9.38μsec.
t_{rs}		100ns
t_{fs}		100ns
$t_{sc}(t_{ss})$	−100nsec.	200ns
t_{rc}		100ns
t_{fc}		100ns
t_{sw}	600ns*	124.3μsec.
t_{cd}	100nsec.	150ns
t_{dc}(setup time, hold time)	60nsec.	
t_{rdi}		100ns
t_{fdi}		100ns

‡That is, the strobe can precede the shift clock by 200nsec, or follow it by as much as 100nsec.
*@2.048MHz 700ns @1.544MHz

Signaling Interface

In the AT&T T1 carrier PCM format an A/B signaling method conveys channel information. It might include the on-or-off hook status of the channel, dial pulsing (10 or 20 pulses per second), loop closure, ring ground, etc., depending on the application. Two signaling conditions (A and B) per channel, giving four possible signaling states per channel are repeated every 12 frames (1.5 milliseconds). The A signaling condition is sent in bit 8 of all 24 channels in frame 6. The B signaling conditions is sent in frame 12. In each frame, bit 193 (the S bit) performs the terminal framing function and serves to identify frames 6 and 12.

The S3507A in a 28-pin package is designed to simplify the signaling interface. For example, the A/B select input pins are transition sensitive. The transmit A/B select pin selects the A signal input on a positive transition and the B signal input on the negative transition. Internally, the device synchronizes the A/B select input with the strobe signal. As a result, a common A/B select signal can be used for all 24 transmit channels in the channelbank. The A and B signaling bits are sent in the frame following the frame in which the A/B select input makes the transition. Therefore, A/B select input must go positive in the beginning of frame 5 and the negative in the beginning of frame 11 (see Figure 3).

Figure 3. Signaling Waveforms in a T1 Carrier System

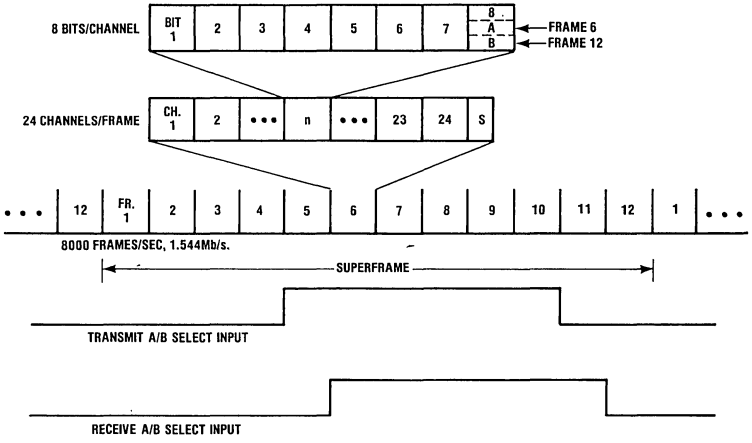
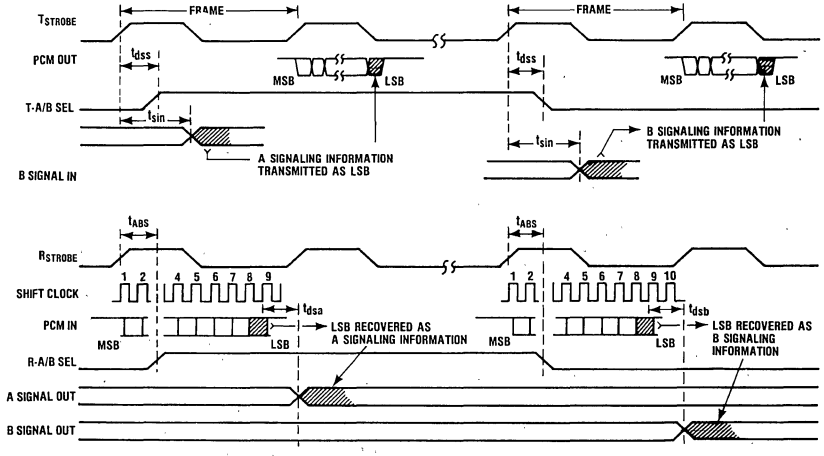
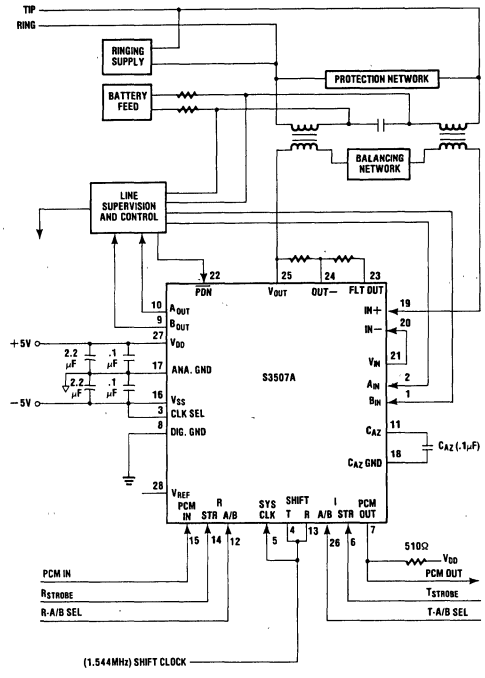


Figure 3A. Signaling Waveform Details



	t_{dss}	t_{sin}	t_{ABS}	t_{dsa}	t_{dsb}
max	1.4μs	80μs	3μs	300ns	300ns

Figure 4. A Subscriber Line Interface Circuit



The decoder uses a similar scheme for receiving the A and B signaling bits, with one difference. They are latched to the respective outputs in the same frame in which the A/B select input makes a transition. Therefore, the receive A/B select input must go high at the beginning of frame 6 and go low at the beginning of frame 12.

Applications Examples

There are two major categories of Codec applications. Central office, channel bank and PABX applications using a multiplex scheme, and digital telephone type dedicated applications. Minor applications are various A/D or D/A needs where the 8 bit word size is desirable for μP interface and fiber optic multiplex systems where non-standard data rates may be used.

A Subscriber Line Interface Circuit

Figure 4 shows a typical diagram of a subscriber line interface circuit using the S3507A. The major elements of such a circuit used in the central office or PABX are a two-to-four wire converter, PCM Codec with filters (S3507A) and circuitry for line supervision and control. The two-to-four wire converter—generally implemented by a transformer-resistor hybrid—provides the interface between the two-wire analog subscriber loop and the digital signals of the time-division-multiplexed PCM highways. It also supplies battery feed to the subscriber telephone. The line supervision and control circuitry provides off-hook and disconnect supervision, generates ringing and decodes rotary dial pulses. It supplies the A/B signaling bits to the coder for transmission within the PCM voice words. It receives A/B signaling outputs from the decoder and operates the A/B signaling relays.

In the T1 carrier system, 24 voice channels are multiplexed to form the transmit and receive highways, 8 data bits from each channel plus a framing bit called the S bit form a 193 bit frame. Since each channel is sampled 8000 times per second, the resultant data rate is 1.544Mb/s.

Within the channelbank the transmit and receive channels of a Codec can occupy the same time slot for a synchronous operation or they can be independent of each other for time slot asynchronous operation. Asynchronous operation helps minimize switching delays through the system. Since the strobe or sync pulse for the coder and decoder sections is independent of each other in the S3507A, it can be operated in either manner.

In the CCITT carrier system, 30 voice channels and 2 framing and signaling channels are multiplexed to form the transmit and receive PCM highways, 8 data bits from each channel. Since each channel is sampled 8000 times per second, the resultant data rate is 2.048Mb/s.

The line supervision and control circuitry within each subscriber line interface can generate all the timing signals for the associated Codec under control of a central processor. Alternatively, a common circuitry within the channelbank can generate the timing signals for all channels. Generation of the timing signals for the S3506 and S3507 is straightforward because of the simplified timing requirements (see Timing Requirements for details). Figures 5 and 5A show design schemes for generating these timing signals in a common circuitry. Note that only three signals: a shift clock, a frame reset pulse (coincident with the S bit) and a superframe reset pulse (coincident with the S bit in Frame 1) are needed. These signals are generated by clock recovery circuitry in the channelbank. Since the Gould Codec does not need channel strobes to be exactly 8-bit periods wide, extra decoding circuitry is not needed.

Figure 5. Generating Timing Signals in a T1 Carrier System

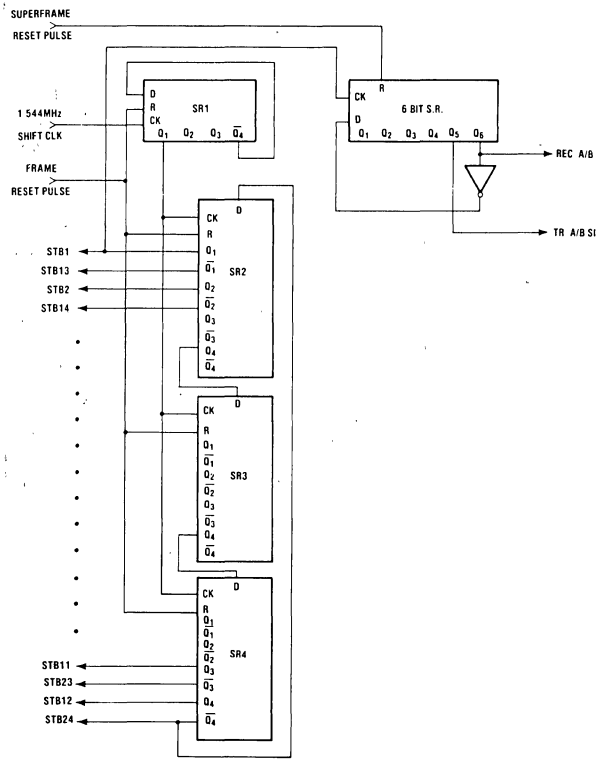
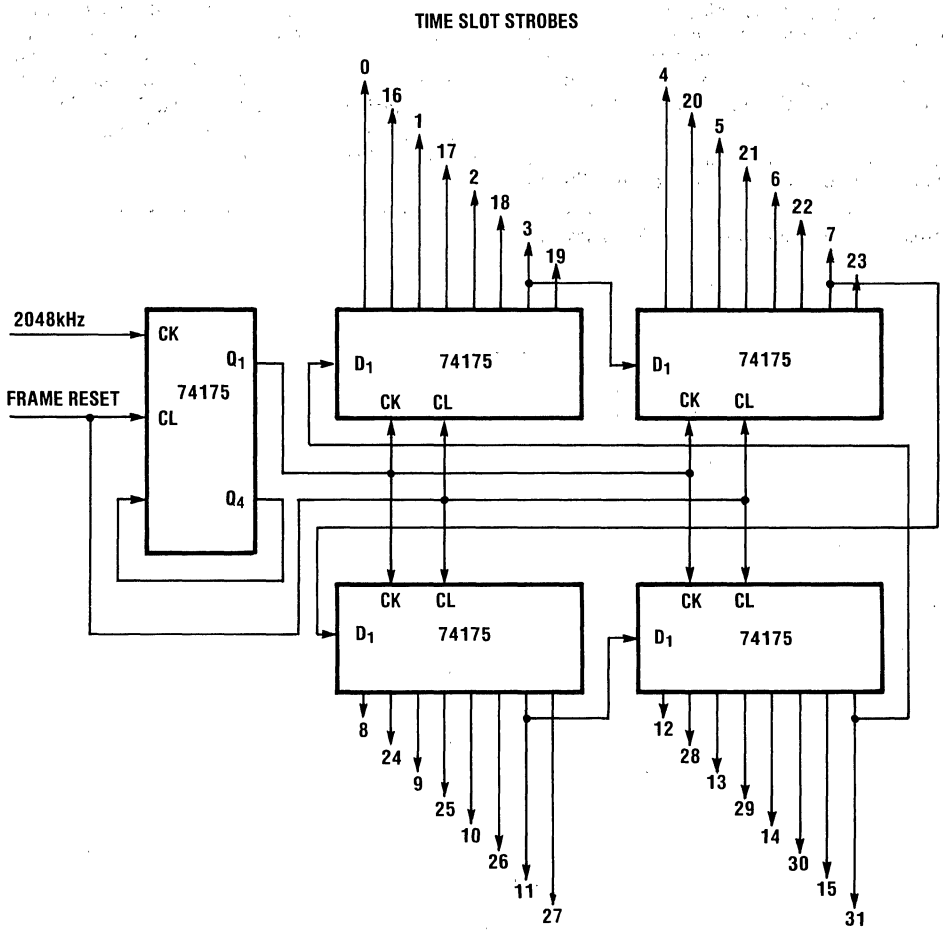


Figure 5A. Generating Timing Signals in a CCITT Carrier System (30 + 2 Channels)

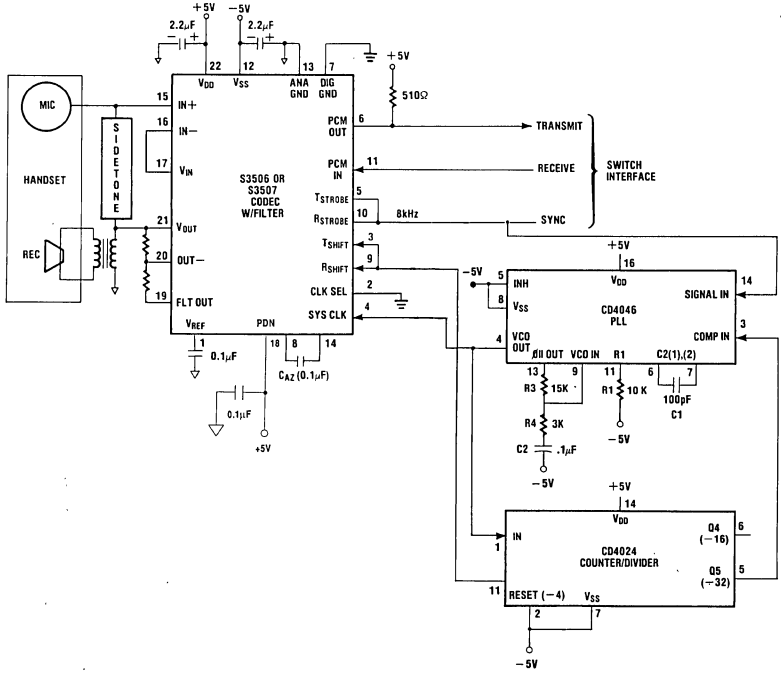


A Digital Telephone Application

Most new PABX designs are using PCM techniques for voice switching with an increasing trend toward applying them at the telephone level. The simplest form of a digital telephone design uses four wire pairs to interface to the switch. Two pairs carry transmit and receive PCM voice data. One pair supplies an 8kHz synchronizing clock signal and the remaining pair supplies power to the telephone. More sophisticated designs reduce costs by time-division-multiplexing and superimposition techniques which minimize the number of wire pairs. The Gould Single-Chip Codec is ideally suited for this application because of the low component count and its simplified timing requirements. Figure 6 shows a schematic for a typical digital telephone design.

Since asynchronous operation is not necessary, transmit and receive timing signals are common. A phase-lock-loop derives the 256kHz system clock and 64kHz shift clock from the 8kHz synchronizing signal received from the switch. The synchronizing signal also serves as the transmit/receive strobe signal since its duty cycle is not important for Codec operation. Microphone output feeds directly into the coder input while the decoder output drives the receiver through an impedance transformer to complete the design.

Figure 6. A Digital Telephone Application



GOULD
AMI Semiconductors

S3541 Digital C Message Weighted and 1 KHz Notch Filter

S3541

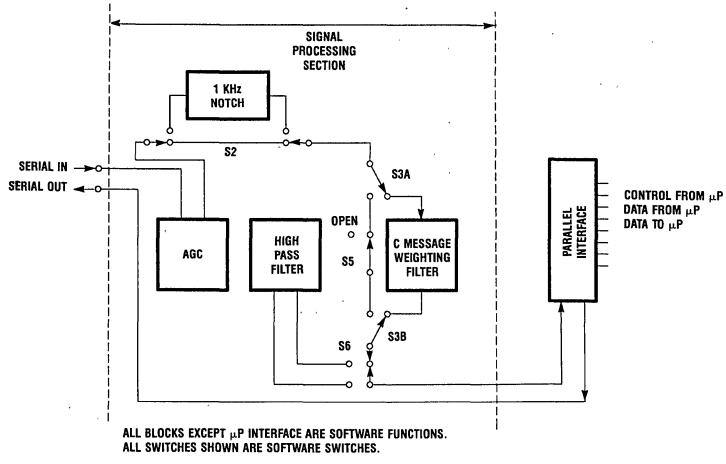
Features

- All Digital Operation for compatibility with all digital telephone systems and for higher reliability.
- Serial Port for Direct connection.
- Parallel Port for Direct connection to host microcontrollers.
- C Message Weighted Filter for line noise measurement to Bell and IEEE specifications.
- High Pass filter for removal of DC offsets and/or measurement.
- Notch filter for line noise measurements under 1 KHz load conditions to Bell and IEEE specifications. Notch filter has more than 50 dB of rejection.
- Single +5 volt power supply operation for reduced system cost.
- Space saving 28-pin plastic DIP package.

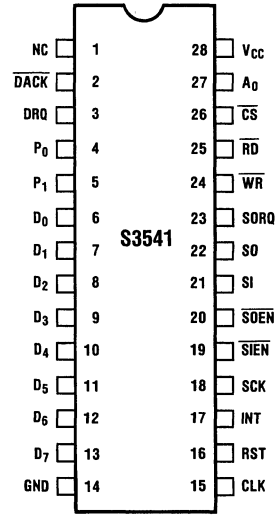
General Description

The S3541 is a monolithic, integrated circuit based upon Digital Signal Processing (DSP) techniques and represents a human ear response to noise during telephone line noise measurements. The primary application for the S3541 is line noise measurement within U.S. telephony system channels. Other applications include diagnostic functions within a PABX system, and voice energy detect systems. The device contains three filters: A C Message Weighted filter, a 1 KHz Notch filter, and a High Pass filter. These filters meet specifications defined by Bell Systems Technical Reference Publication #41009, May 1975 and IEEE Std 743-1984.

Block Diagram



Pin Configuration



GOULD

AMI Semiconductors

Single Chip Conference Trunk

Preliminary Data Sheet

S3547

COMMUNICATION PRODUCTS

Features

- 6 telephones/persons maximum conference with AGC
- 2 groups of 3 telephones/persons conferences
- +3 dB gain pad function
- PCM highway (1.544/2.048 Mbps) serial interface
- Parallel microprocessor bus interface
- 500 Hz tone generator
- Small 28 pin plastic DIP package
- +5 V single power supply

General Description

S3547 is the single chip conference trunk for 6 telephones/persons. S3547 uses the N-1 addition method to realize a natural conversation. The output level is automatically controlled by using the peak value to avoid the over range error. 2 separate conferences of 3 persons each can also be realized concurrently with this chip.

S3547 has a serial interface for PCM highway to realize the conference trunk without any CODEC or Op-Amp in the digital exchange system. It has a 500 Hz tone generator that can be used, for example, as the signal for speakers to indicate that an additional speaker is joining the conference.

S3547 is easily controlled by various microprocessors because it has a bus interface which is compatible with 8080, 8085, 8086, Z80, etc.

Figure 1. S3547 Conference Trunk

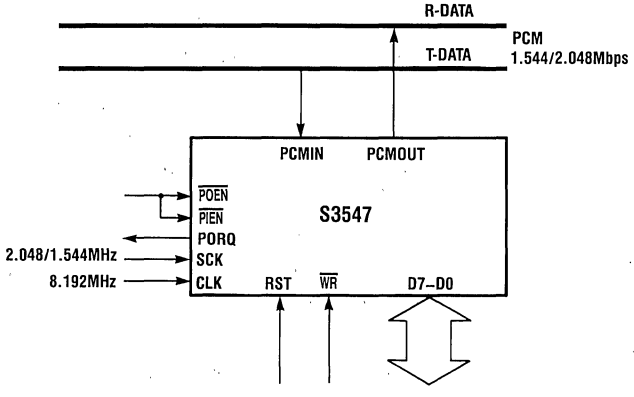


Figure 2. Pin Configuration

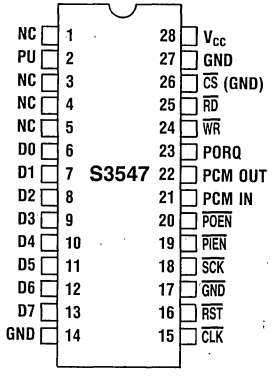
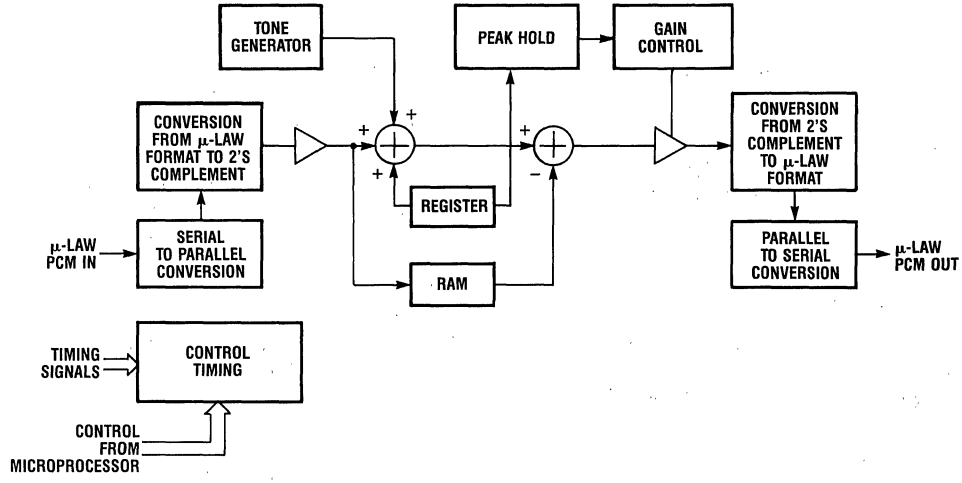


Figure 3. S3547 Block Diagram



1. Functional Description

The Block Diagram of S3547 is shown in Fig. 3. S3547 has the DSP architecture.

Compressed μ-law PCM data is expanded to the linear 2's complement data for internal arithmetic operation. After the arithmetic operation, the output data for each channel is converted to μ-law PCM data again.

The output data for each channel is the data that is generated by subtracting its own channel data from the sum of all channel data in a conference. This is called the N-1 addition method.

As the simple addition operation of 6 channel data may cause the over-range error, the input data from each channel is attenuated to non-over range level. The output signal level is automatically controlled to provide sufficient audio level to hear. The peak value of sum of all channel data is held for about 100 ms, which provides a natural conversation. This peak value is used for the output level control.

The automatic gain control is not executed in the 2 groups of 3 persons conference mode.

S3547 is easily controlled by 2 types of 8-bit command. These commands are defined as "command 1" and "command 2" according to the MSB value. The MSB of command 1 is high and that of command 2 is low.

The level of the 500 Hz tone is also selectable by the command 1.

1.1 6 persons/phones conference mode

When D6 bit of the command 1 is high, 6 persons/phones conference mode is set. 6 consecutive time slots are assigned for this mode. It is possible to use 2 to 6 channels arbitrarily. The channel assignment for a conference is done by command 2.

1.2 2 groups of 3 persons/phones conference mode

When D6 bit of the command 1 is low, 2 groups of 3 persons/phones conference mode is set. First 3 chan-

Table 1. Pin Description

Pin No.	Name	Type	Function
1	NC	I	No Connection
2	PU	I	Must be pulled up to Vcc
3,4,5	NC	I	Must be open.
6–13	D0–D7	I/O 3 state	Port for 8 bit data of command1 and command2.
14	GND		Connect to GND
15	CLK	I	Single phase master clock 8MHz/8.192MHz
16	RST	I	Reset and initialize the S3547 internal logic. Set the first command waiting state.
17	GND	I	Connect to GND
18	SCK	I	PCM data input/output clock. A serial data bit is transferred when this pin is high.
19	$\overline{PIEN}$	I	PCM input enable pin. This pin enables the shift clock to serial input register.
20	$\overline{POEN}$	O	PCM output enable pin. This pin enables the shift clock to serial output register.
21	PCMIN	I	PCM data input. Serial data is latched at the rising edge of SCK.
22	PCMOUT	O	PCM data output. Serial data is clocked out at the falling edge of SCK.
23	PORQ	O	PCM output request. It generates an output signal for an external device indicating that the serial data register has been loaded and is ready for output. PORQ is reset when the entire 8-bit word has been transferred.
24	$\overline{WR}$	I	Write control signal. Write the contents of data bus into the data register.
25	$\overline{RD}$	I	Read control signal. It is possible to read out the previous command. This pin should be pulled up to Vcc in normal case.
26	$\overline{CS}$	I	Chip select. This pin enables data transfer with data or status port with RD or WR signal.
27	GND	I	Connect to GND
28	Vcc		+5 V Power.

Table 2.1 Command 1 (D7=0)

Bit	Status	Function
D6	0 1	6 persons/phones conference mode 2 groups of 3 persons/phones conference mode.
D5	0 1	500 Hz tone disable 500 Hz tone out for 0.2 seconds
D4	 0 1	For 3 phones conference mode 500 Hz tone out for group 1 500 Hz tone out for group 2
D3	 0 1	Tone level control bit Hold the previous data 500 Hz tone level is selectable by D2 and D1 data.
D2, D1	 11 10 01 00	500 Hz tone level data when D3 is high. Large Medium Small Disable a 500 Hz tone
D0	0 1	Command 1 enable Program reset

Table 2.2 Command 2 (D7=1)

Bit	Status	Functions
D6	0 1	Enable channel position select Optional gain position select
D5–D0		The allocation of channels. D5→Ch6, D4→Ch5, D3→Ch4 D2→Ch3, D1→Ch2, D0→Ch1

nels of a series of 6 channels are the Group 1, and the others are the Group 2. Selection of the channels for each group is done by command 2.

1.3 500 Hz tone

When D5 bit of the command 1 is high, 500 Hz single tone signal is added to each channel for about 0.2 seconds. In the 3 persons/phones conference mode, the selection of groups is done by D4 bit of command 1.

D2 and D1 command bits are used for tone level data when D3 bit of command 1 is high.

1.4 Selection of channels for conference

When D6 bit of command 2 is low, D0–D5 of command 2 are correspond to channel assignment of channel 1–6. By setting these bits high, channels for the conference are selected. The output of the channel which is not selected is "11111111". The selection of channels for each group in 2 groups of 3 phones mode is the same as 6 phones conference mode.

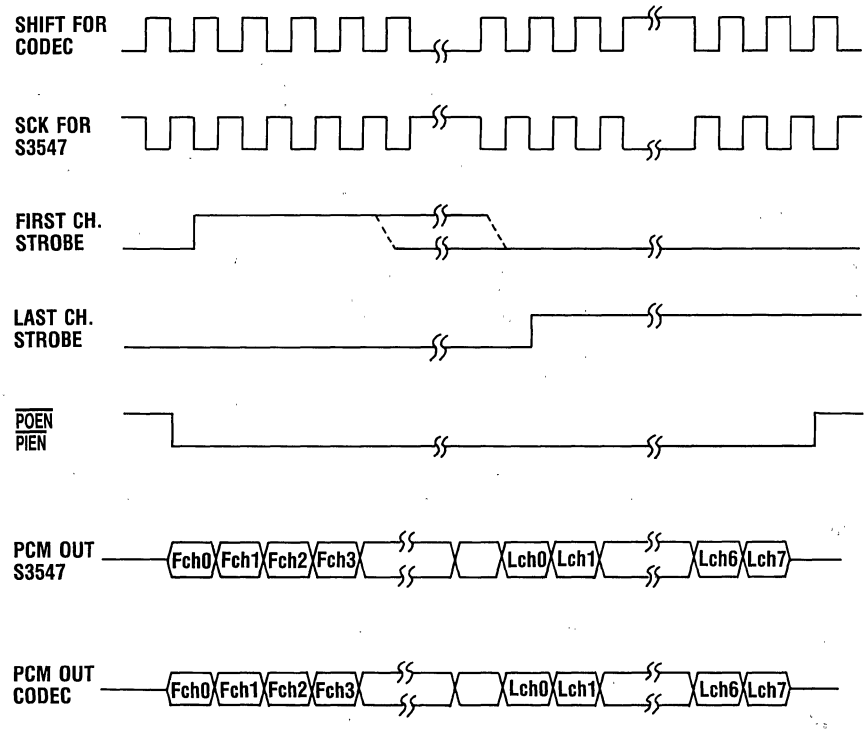
1.5 Optional input gain

S3547 has the optional gain function for input data of each channel to compensate the outside line loss. When D6 bit of the command 2 is high, the selected channels have +3 dB optional gain for incoming signal. In the 6 phones conference mode, it is possible to set the optional gain up to two channels.

1.6 Program reset

When D0 bit of command 1 is high, internal program is reset. Once program reset is complete, S3547 ter-

Figure 4. Serial I/O Timing



minates the conference function and waits for the command 1 for the next conference.

2. Timing for serial data

The serial input and output data of S3547 is the 8-bit μ-law PCM data.

S3547 treats a series of 6 PCM data. The timing for the PCM highway is shown in Fig. 4. Example of the PCM highway interface circuit is shown in Fig. 5.

3. Timing for command input

The first control command input timing is shown in Fig. 6. The first input command after the reset pulse or program reset is to set conference mode and to select 500 Hz tone level, using command 1. After this initial sequence, the command for S3547 can be controlled dynamically until S3547 is reset by software or hardware.

Figure 5. Example of PCM Interface Circuit

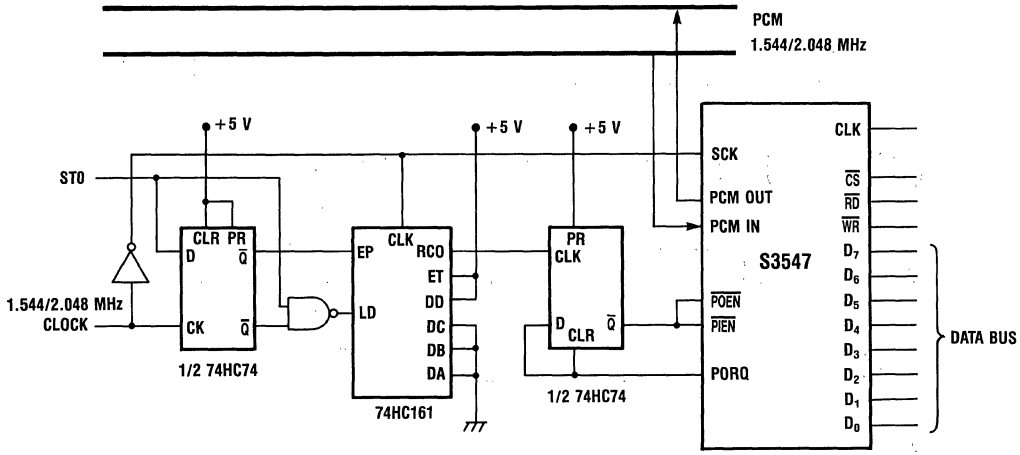
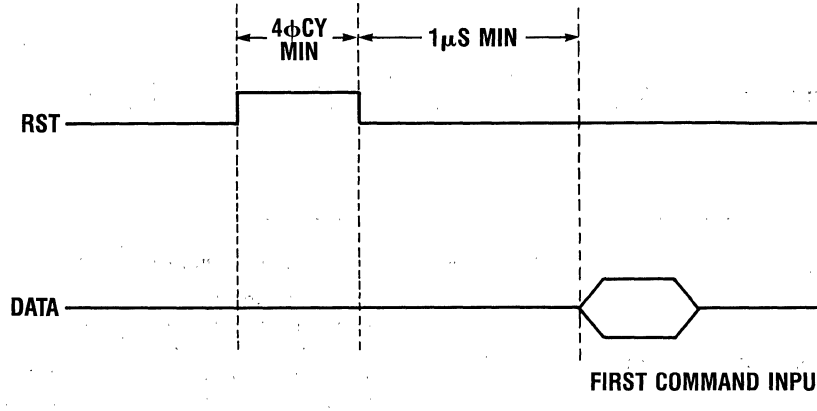


Figure 6. Timing For Command Input



Absolute Maximum Rating

Voltage (VCC)	−0.5 to +7.0 Volts[1]
Voltage, Any Input (VI)	−0.5 to +7.0 Volts[1]
Voltage, Any Output (VO)	−0.5 to +7.0 Volts[1]
Operating Temperature (TOPT)	0°C to +70°C
Storage Temperature (TSTG)	−65°C to +150°C

Note 1: With respect to GND

D.C. Characteristics: (TA=0°C to +70°C, VCC=+5V±5%)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
VIL	Input Low Voltage	−0.5		0.8	V	
VIH	Input High Voltage	2.0		VCC+0.5	V	
VϕL	CLK Low Voltage	−0.5		0.45	V	
VϕH	CLK High Voltage	3.5		VCC+0.5	V	
VOL	Output Low Voltage			0.45	V	IOL=2.0mA
VOH	Output High Voltage	2.4			V	IOH=400μA
ILIL	Input Load Current			−10	μA	VIN=0V
ILIH	Input Load Current			10	μA	VIN=VCC
ILOL	Output Float Leakage			−10	μA	VOUT=0.47V
ILOH	Output Float Leakage			10	μA	VOUT=VCC
ICC	Power Supply Current (0 to 70°C)		180	280	mA	

Capacitance

Cϕ	CLK, SCK Input Capacitance			20*	pF	fc = 1MHz
CIN	Input Pin Capacitance			10*	pF	fc = 1MHz
COUT	Output Pin Capacitance			20*	pF	fc = 1MHz

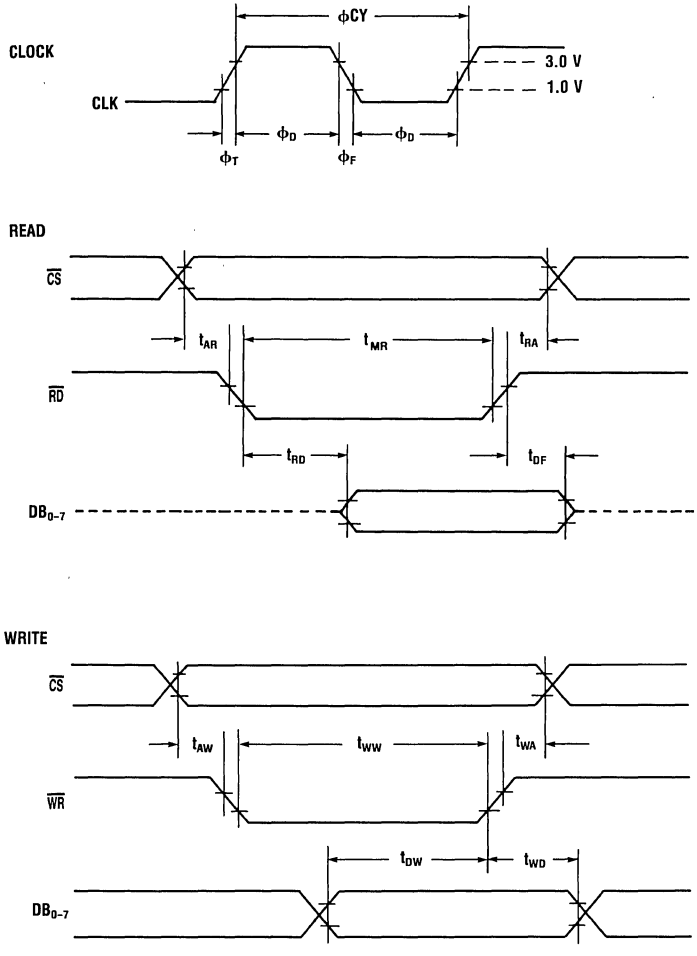
*These values are not 100% tested in production.

A.C. Characteristics: (TA=0°C to +70°C, VCC=+5V±5%)

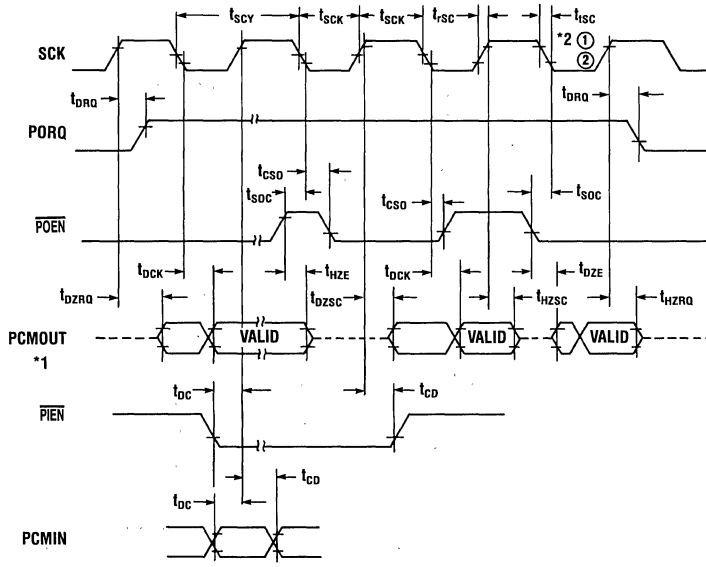
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
ϕCY	CLK Cycle Time	122		2000	ns	See Note 1
ϕD	CLK Pulse Width	60			ns	
ϕR	CLK Rise Time			10	ns	See Note 1
ϕF	CLK Fall Time			10	ns	See Note 1
tAR	Address Setup Time for $\overline{RD}$	0			ns	
tRA	Address Hold Time for $\overline{RD}$	0			ns	
tRR	$\overline{RD}$ Pulse Width	250			ns	
tRD	Data Delay from $\overline{RD}$			150	ns	CL=100pF
tDF	Read to Data Floating	10		100	ns	CL=100pF
tAW	Address Setup Time for $\overline{WR}$	0			ns	
tWA	Address Hold Time for $\overline{WR}$	0			ns	
tWW	$\overline{WR}$ Pulse Width	250			ns	
tDW	Data Setup Time for $\overline{WR}$	150			ns	
tWD	Data Hold Time for $\overline{WR}$	0			ns	
tRV	$\overline{RD}$, $\overline{WR}$, Recovery Time	250			ns	See Note 2
tSCY	SCK Cycle Time	480		DC	ns	
tSCK	SCK Pulse Width	230			ns	
tRSC	SCK Rise Time			20	ns	See Note 1
tFSC	SCK Fall Time			20	ns	See Note 1
tDRQ	PORQ Delay	30		150	ns	CL=100pF
tSOC	$\overline{POEN}$ Setup Time for SCK	50			ns	
tCSO	$\overline{POEN}$ Hold Time for SCK	30			ns	
tDCK	PCMOUT Delay from SCK=LOW			150	ns	
tDZRQ	PCMOUT Delay from SCK with PORQ↑	20		300	ns	See Note 2
tDZSC	PCMOUT Delay from SCK	20		300	ns	See Note 2
tDZE	PCMOUT Delay from $\overline{POEN}$	20		180	ns	See Note 2
tHZE	$\overline{POEN}$ to PCMOUT Floating	20		200	ns	See Note 2
tHZSC	SCK to PCMOUT Floating	20		300	ns	See Note 2
tHZRQ	PCMOUT Delay from SCK with PORQ↓	70*		300	ns	See Note 2
tDC	$\overline{PIEN}$, PCMIN Setup Time for SCK	55*			ns	See Note 2
tCD	$\overline{PIEN}$, PCMIN Hold Time from SCK	30*			ns	
tRST	RST Pulse Width	4*			ϕCY	

* These values are guaranteed by design and not by 100% testing.
Note 1: Voltage at measuring point of timing 1.0V and 3.0V
Note 2: Voltage at measuring point of AC Timing: VIL=VOL=0.8V, VIH=VOH=2.0V
Input Waveform of AC Test (expected CLK, SCK)

Timing Waveforms



Timing Waveforms

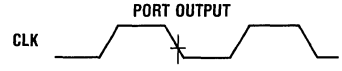


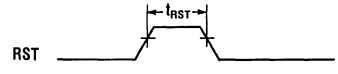
*1: For PCMOUT timing, the data at rising edge of SCK is valid and the other data is invalid. In setup hold time of data for SCK, the most strict specifications are the following.

SETUP = tSCK — tDCK
HOLD = tHZRQ

*2: Voltage at measuring point of tRSC and tFSC for SCK timing

① 3.0V, ② 1.0V





GOULD

AMI Semiconductors

Digital Signal Processor

S7720

COMMUNICATION PRODUCTS

Features

- ☐ Fast Instruction Execution — 250 ns
- ☐ 16-Bit Data Word
- ☐ Multi-Operation Instructions for Optimizing Program Execution
- ☐ Large Memory Capacities
  - — Program ROM 512 × 23 Bits
  - — Coefficient ROM 510 × 13 Bits
  - — Data RAM 128 × 16 Bits
- ☐ Fast (250 ns) 16 × 16-31 Bit Multiplier
- ☐ Dual Accumulators
- ☐ Four Level Subroutine Stack for Program Efficiency
- ☐ Multiple I/O Capabilities: Serial, Parallel, DMA
- ☐ Compatible with Most Microprocessors, Including: 8080, 8085, 8086, Z80™*
- ☐ Power Supply +5V
- ☐ NMOS
- ☐ Package — 28 Pin Dip

General Description

The S7720 Digital Signal Processor (DSP) is an advanced architecture microcomputer optimized for signal processing algorithms. Its speed and flexibility allow the DSP to efficiently implement signal processing functions in a wide range of environments and applications.

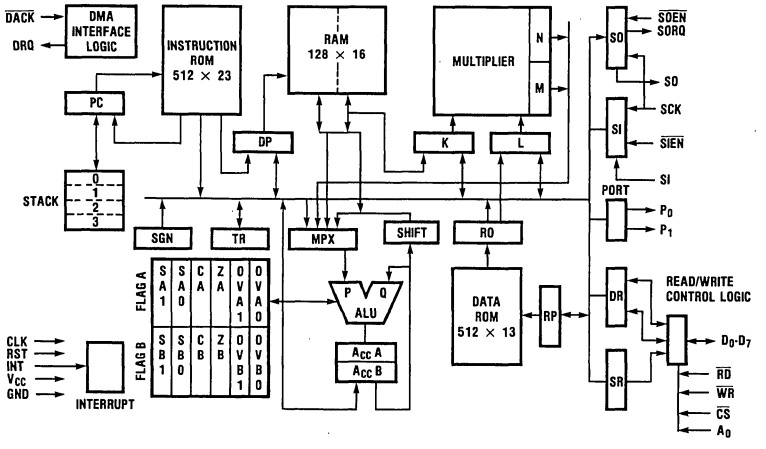
The DSP is the state of the art in signal processing today, and for the future.

Performance Benchmarks

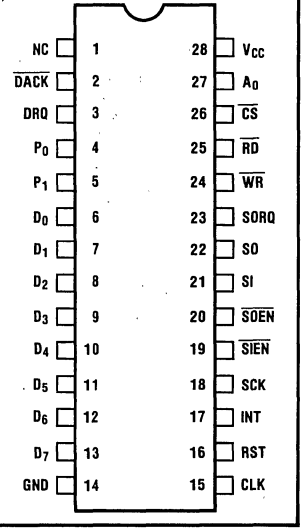
- ☐ Second Order Digital Filter (BiQuad) 2.25 μs
- ☐ SINE/COS of Angles 5.25 μs
- ☐ μ/A LAW to Linear Conversion 0.50 μs
- ☐ FFT: 32 Point Complex 0.7 ms
  - 64 Point Complex 1.6 ms

*Trademark of Zilog Corp.

Functional Block Diagram



Pin Configuration



S7720

Functional Description

Fabricated in high speed NMOS, the S7720 DSP is a complete 16-bit microcomputer on a single chip. ROM space is provided for coefficient storage, while the on-chip RAM may be used for temporary data, coefficients and results. Computational power is provided by a 16-bit Arithmetic/Logic Unit (ALU) and a separate 16 × 16-bit fully parallel multiplier. This combination allows the implementation of a "sum of products" operation in a single 250 nsec instruction cycle. In addition, each arithmetic instruction provides for a number of data movement operations to further increase throughout. Two serial I/O ports are provided for interfacing to codecs and other serially-oriented devices while a parallel port provides both data and status information to conventional μP for more sophisticated applications. Handshaking signals, including DMA controls, allow the DSP to act as a sophisticated programmable peripheral as well as a stand alone microcomputer.

Absolute Maximum Ratings*

Voltage (V_{CC} Pin)	−0.5 to +7.0 Volts[1]
Voltage, Any Input (V_I)	−0.5 to +7.0 Volts[1]
Voltage, Any Output (V_O)	−0.5 to +7.0 Volts[1]
Operating Temperature (T_{OPT})	−40°C to +85°C
Storage Temperature (T_{STG})	−65°C to +150°C

NOTE 1: With respect to GND.

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
C_ϕ	CLK, SCK Input Capacitance			20*	pF	f_C=1MHz
C_{IN}	Input Pin Capacitance			10*	pF	f_C=1MHz
C_{OUT}	Output Pin Capacitance			20*	pF	f_C=1MHz

*These values are not 100% tested in production.

Electrical Specifications: (T_A=0° ~ +70°C, V_{CC}= +5V ± 5%)

D.C. Characteristics

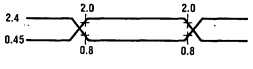
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} +0.5	V	
$V_{\phi L}$	CLK Low Voltage	−0.5		0.45	V	
$V_{\phi H}$	CLK High Voltage	3.5		V_{CC} +0.5	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL}=2.0mA
V_{OH}	Output High Voltage	2.4			V	I_{OH}−400μA
I_{LIL}	Input Load Current			−10	μA	V_{IN}=0V
I_{LIH}	Input Load Current			10	μA	V_{IN}=V_{CC}
I_{LOL}	Output Float Leakage			−10	μA	V_{OUT}=0.47V
I_{LOH}	Output Float Leakage			10	μA	V_{OUT}=V_{CC}
I_{CC}	Power Supply Current (0 to 70°C)		180	280	mA	
I_{CC}	Power Supply Current (−40 to 85°C)			330	mA	

A.C. Characteristics: ($T_A = -10° \sim +70°C$, $V_{CC} = +5V \pm 5\%$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
ϕCY	CLK Cycle Time	122		2000	ns	See Note 1
ϕD	CLK Pulse Width	60			ns	
ϕR	CLK Rise Time			10	ns	See Note 1
ϕF	CLK Fall Time			10	ns	See Note 1
t_{AR}	Address Setup Time for $\overline{RD}$	0			ns	
t_{RA}	Address Hold Time for $\overline{RD}$	0			ns	
t_{RR}	$\overline{RD}$ Pulse Width	250			ns	
t_{RD}	Data Delay from $\overline{RD}$			150	ns	$C_L = 100pF$
t_{DF}	Read to Data Floating	10		100	ns	$C_L = 100pF$
t_{AW}	Address Setup Time for $\overline{WR}$	0			ns	
t_{WA}	Address Hold Time for $\overline{WR}$	0			ns	
t_{WW}	$\overline{WR}$ Pulse Width	250			ns	
t_{DW}	Data Setup Time for $\overline{WR}$	150			ns	
t_{WD}	Data Hold Time for $\overline{WR}$	0			ns	
t_{RV}	$\overline{RD}$, $\overline{WR}$, Recovery Time	250			ns	See Note 2
t_{AM}	DRQ Delay			150	ns	
t_{DACK}	$\overline{DACK}$ Delay Time	1*			ϕD	See Note 2
t_{SCY}	SCK Cycle Time	480		DC	ns	
t_{SCK}	SCK Pulse Width	230			ns	
t_{RSC}	SCK Rise/Fall Time			20	ns	See Note 1
t_{DRQ}	SORQ Delay	30		150	ns	$C_L = 100pF$
t_{SOC}	$\overline{SOEN}$ Setup Time	50			ns	
t_{CSO}	$\overline{SOEN}$ Hold Time	30			ns	
t_{DCK}	SO Delay from SCK = LOW			150	ns	
t_{DZRQ}	SO Delay from SCK with SORQ↑	20		300	ns	See Note 2
t_{DZSC}	SO Delay from SCK	20		300	ns	See Note 2
t_{DZE}	SO Delay from $\overline{SOEN}$	20		180	ns	See Note 2
t_{HZE}	$\overline{SOEN}$ to SO Floating	20		200	ns	See Note 2
t_{HZSC}	SCK TO SO Floating	20		300	ns	See Note 2
t_{HZRQ}	SO Delay from SCK with SORQ↓	70*		300	ns	See Note 2
t_{DC}	$\overline{SIEN}$, SI Setup Time	80			ns	See Note 2
t_{CD}	$\overline{SIEN}$, SI Hold Time	160			ns	
t_{DP}	P_0, P_1 Delay			$\phi CY + 150$*	ns	
t_{RST}	RST Pulse Width	4*			ϕCY	
t_{INT}	INT Pulse Width	8*			ϕCY	

*These values are guaranteed by design and not by 100% testing.
NOTE 1: Voltage at measuring point of timing 1.0V and 3.0V
NOTE 2: Voltage at measuring point of AC Timing: $V_{IL} = V_{OL} = 0.8V$, $V_{IH} = V_{OH} = 2.0V$

Input Waveform of AC Test (except CLK, SCK)



Clock

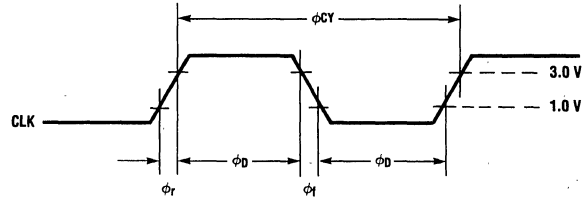


Figure 1. Clock

Read

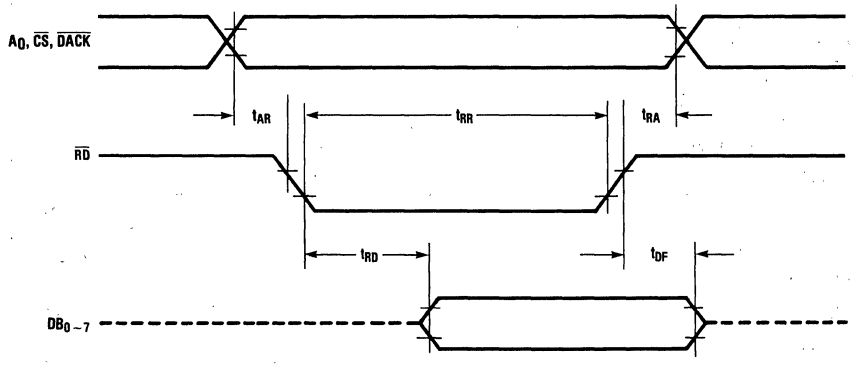


Figure 2. Read Operation

Write

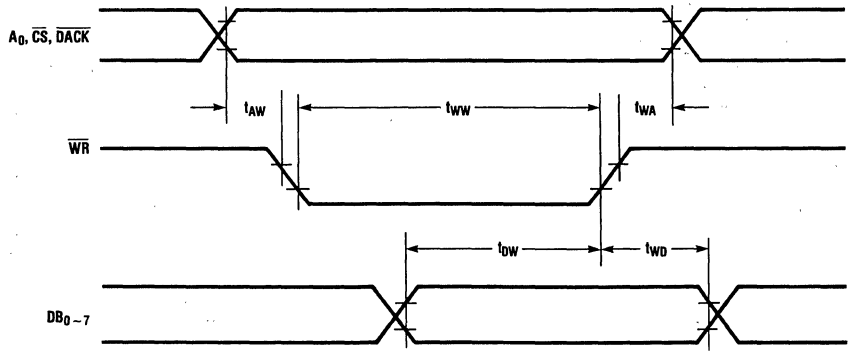
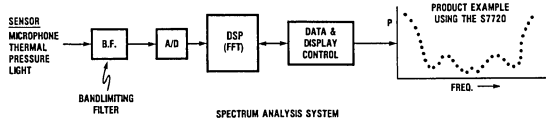
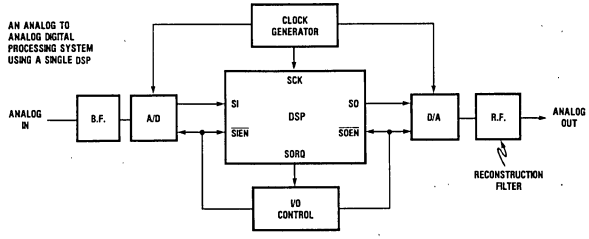


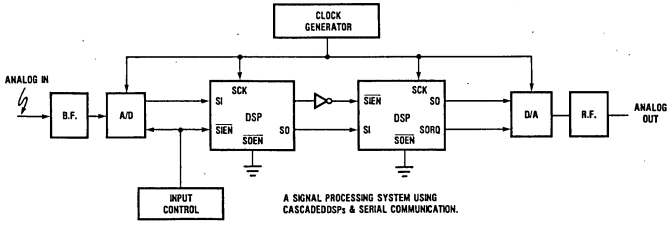
Figure 3. Write Operation

S7720

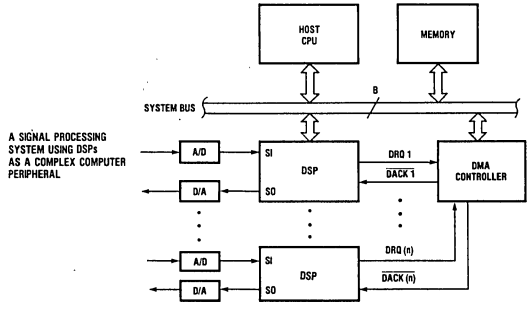


SPECTRUM ANALYSIS SYSTEM





A SIGNAL PROCESSING SYSTEM USING CASCADEDDSPs & SERIAL COMMUNICATION.



GOULD

AMI Semiconductors

Digital Signal Processor

Advanced Product Description

S77C20

Features

- ☐ Fast Instruction Execution — 250 ns
- ☐ 16-Bit Data Word
- ☐ Multi-Operation Instructions for Optimizing Program Execution
- ☐ Large Memory Capacities
  - — Program ROM 512 × 23 Bits
  - — Coefficient ROM 510 × 13 Bits
  - — Data RAM 128 × 16 Bits
- ☐ Fast (250 ns) 16 × 16-31 Bit Multiplier
- ☐ Dual Accumulators
- ☐ Four Level Subroutine Stack for Program Efficiency
- ☐ Multiple I/O Capabilities: Serial, Parallel, DMA
- ☐ Compatible with Most Microprocessors, Including: 8080, 8085, 8086, Z80™*
- ☐ Power Supply +5V
- ☐ CMOS
- ☐ Package — 28 Pin Dip
- ☐ Package — 28 Pin PLCC

General Description

The S77C20 Digital Signal Processor (DSP) is an advanced architecture microcomputer optimized for signal processing algorithms. Its speed and flexibility allow the DSP to efficiently implement signal processing functions in a wide range of environments and applications.

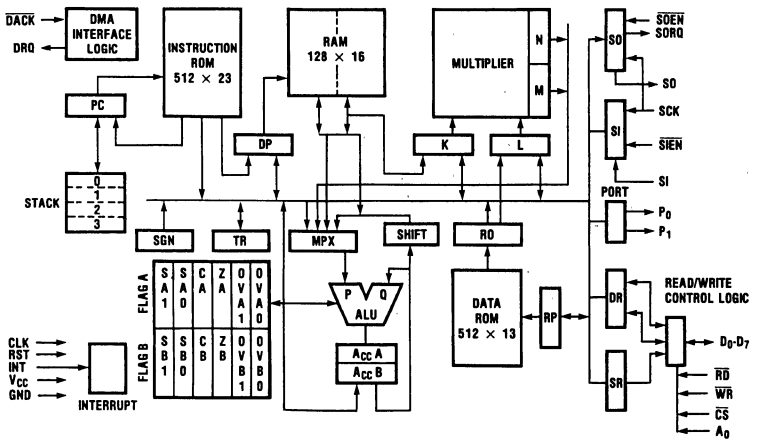
The DSP is the state of the art in signal processing today, and for the future.

Performance Benchmarks

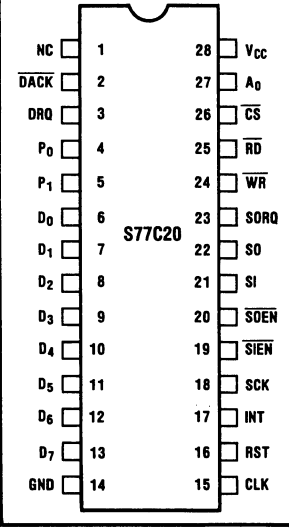
☐ Second Order Digital Filter (BiQuad)	2.25 μs
☐ SINE/COS of Angles	5.25 μs
☐ μ/A LAW to Linear Conversion	0.50 μs
☐ FFT: 32 Point Complex	0.7 ms
64 Point Complex	1.6 ms

*Trademark of Zilog Corp.

Functional Block Diagram



Pin Configuration



Functional Description

Fabricated in high speed CMOS, the S77C20 DSP is a complete 16-bit microcomputer on a single chip. ROM space is provided for coefficient storage, while the on-chip RAM may be used for temporary data, coefficients and results. Computational power is provided by a 16-bit Arithmetic/Logic Unit (ALU) and a separate 16 × 16-bit fully parallel multiplier. This combination allows the implementation of a "sum of products" operation in a single 250 nsec instruction cycle. In addition, each arithmetic instruction provides for a number of data movement operations to further increase throughout. Two serial I/O ports are provided for interfacing to codecs and other serially-oriented devices while a parallel port provides both data and status information to conventional μP for more sophisticated applications. Handshaking signals, including DMA controls, allow the DSP to act as a sophisticated programmable peripheral as well as a stand alone microcomputer.

Absolute Maximum Ratings*

Voltage (V_{CC} Pin)	−0.5 to +7.0 Volts[1]
Voltage, Any Input (V_I)	−0.5 to +7.0 Volts[1]
Voltage, Any Output (V_O)	−0.5 to +7.0 Volts[1]
Operating Temperature (T_{OPT})	−0°C to +70°C
Storage Temperature (T_{STG})	−65°C to +150°C

NOTE 1: With respect to GND.

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
C_ϕ	CLK, SCK Input Capacitance			20*	pF	f_C=1MHz
C_{IN}	Input Pin Capacitance			10*	pF	f_C=1MHz
C_{OUT}	Output Pin Capacitance			20*	pF	f_C=1MHz

*These values are not 100% tested in production.

Electrical Specifications: (T_A=0° ~ +70°C, V_{CC}= +5V ±5%)
D.C. Characteristics

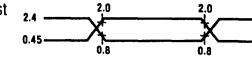
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} +0.5	V	
$V_{\phi L}$	CLK Low Voltage	−0.5		0.45	V	
$V_{\phi H}$	CLK High Voltage	3.5		V_{CC} +0.5	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL}=2.0mA
V_{OH}	Output High Voltage	2.4			V	I_{OH}−400μA
I_{LIL}	Input Load Current			−10	μA	V_{IN}=0V
I_{LIH}	Input Load Current			10	μA	V_{IN}=V_{CC}
I_{LOL}	Output Float Leakage			−10	μA	V_{OUT}=0.47V
I_{LOH}	Output Float Leakage			10	μA	V_{OUT}=V_{CC}
I_{CC}	Power Supply Current (0 to 70°C)		18	24	mA	

A.C. Characteristics: ($T_A = -0°C \sim +70°C$, $V_{CC} = +5V \pm 5\%$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
ϕCY	CLK Cycle Time	122		2000	ns	See Note 1
ϕD	CLK Pulse Width	60			ns	
ϕR	CLK Rise Time			10	ns	See Note 1
ϕF	CLK Fall Time			10	ns	See Note 1
t_{AR}	Address Setup Time for $\overline{RD}$	0			ns	
t_{RA}	Address Hold Time for $\overline{RD}$	0			ns	
t_{RR}	$\overline{RD}$ Pulse Width	250			ns	
t_{RD}	Data Delay from $\overline{RD}$			150	ns	$C_L = 100pF$
t_{DF}	Read to Data Floating	10		100	ns	$C_L = 100pF$
t_{AW}	Address Setup Time for $\overline{WR}$	0			ns	
t_{WA}	Address Hold Time for $\overline{WR}$	0			ns	
t_{WW}	$\overline{WR}$ Pulse Width	250			ns	
t_{DW}	Data Setup Time for $\overline{WR}$	150			ns	
t_{WD}	Data Hold Time for $\overline{WR}$	0			ns	
t_{RV}	$\overline{RD}$, $\overline{WR}$, Recovery Time	250			ns	See Note 2
t_{AM}	DRQ Delay			150	ns	
t_{DACK}	$\overline{DACK}$ Delay Time	1*			ϕD	See Note 2
t_{SCY}	SCK Cycle Time	480		DC	ns	
t_{SCK}	SCK Pulse Width	230			ns	
t_{RSC}	SCK Rise/Fall Time			20	ns	See Note 1
t_{DRQ}	SORQ Delay	30		150	ns	$C_L = 100pF$
t_{SOC}	$\overline{SOEN}$ Setup Time	50			ns	
t_{CSO}	$\overline{SOEN}$ Hold Time	30			ns	
t_{DCK}	SO Delay from SCK = LOW			150	ns	
t_{DZRQ}	SO Delay from SCK with SORQ↑	20		300	ns	See Note 2
t_{DZSC}	SO Delay from SCK	20		300	ns	See Note 2
t_{DZE}	SO Delay from $\overline{SOEN}$	20		180	ns	See Note 2
t_{HZE}	$\overline{SOEN}$ to SO Floating	20		200	ns	See Note 2
t_{HZSC}	SCK TO SO Floating	20		300	ns	See Note 2
t_{HZRQ}	SO Delay from SCK with SORQ↓	70*		300	ns	See Note 2
t_{DC}	$\overline{SIEN}$, SI Setup Time	55*			ns	See Note 2
t_{CD}	$\overline{SIEN}$, SI Hold Time	30*			ns	
t_{DP}	P_0, P_1 Delay			$\phi CY + 150$*	ns	
t_{RST}	RST Pulse Width	4*			ϕCY	
t_{INT}	INT Pulse Width	8*			ϕCY	

*These values are guaranteed by design and not by 100% testing.
NOTE 1: Voltage at measuring point of timing 1.0V and 3.0V
NOTE 2: Voltage at measuring point of AC Timing: $V_{IL} = V_{OL} = 0.8V$, $V_{IH} = V_{OH} = 2.0V$

Input Waveform of AC Test (except CLK, SCK)



Clock

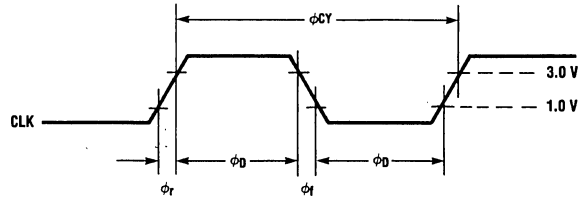


Figure 1. Clock

Read

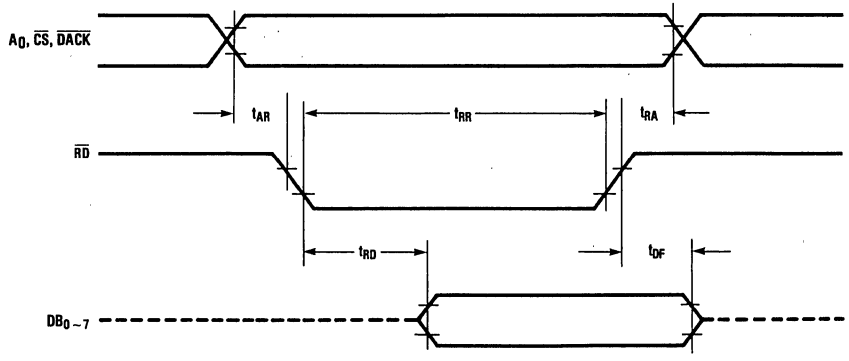


Figure 2. Read Operation

Write

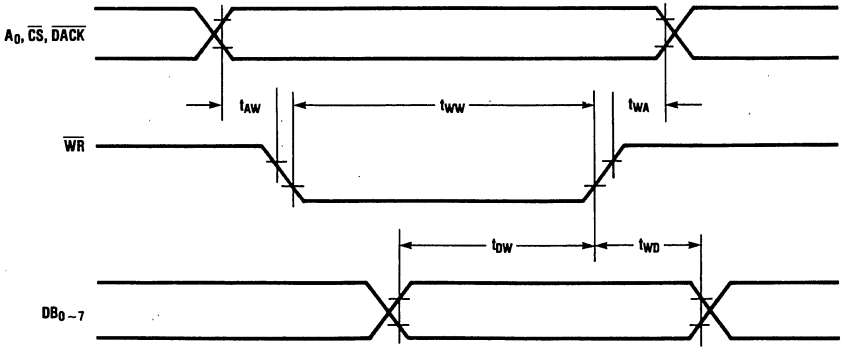


Figure 3. Write Operation

Arithmetic Capabilities

General

One of the unique features of the SPI's architecture is its arithmetic facilities. With a separate multiplier, ALU, and multiple internal data paths, the SPI is capable of carrying out a multiply, an add, or other arithmetic operation, and a data move between internal registers in a single instruction cycle.

ALU

The ALU is a 16-bit 2's complement unit capable of executing 16 distinct operations on virtually any of the SPI's internal registers, thus giving the SPI both speed and versatility for efficient data management.

Accumulators (ACCA/ACCB)

Associated with the ALU are a pair of 16-bit accumulators, each with its own set of flags, which are updated at the end of each arithmetic instruction (except NOP). In addition to Zero Result, Sign Carry, and Overflow Flags, the SPI incorporates auxiliary Overflow and Sign Flags (SA1, SB1, OVA1, OVB1). These flags enable the detection of an overflow condition and maintain the correct sign after as many as three successive additions or subtractions.

Table 2. ACC A/B Flag Registers

FLAG A	SA1	SA0	CA	ZA	OVA1	OVA0
FLAG B	SB1	SB0	CB	ZB	OVB1	OVB0

Sign Register (SGN)

When OVA1 (or OVB1) is set, the SA1 (or SB1) bit will hold the corrected sign of the overflow. The SGN Register will use SA1 (SB1) to automatically generate saturation constants 7FFFH(+) or 8000H(−) to permit efficient limiting of a calculated value.

Multiplier

Thirty-one bit results are developed by a 16 × 16-bit 2's complement multiplier in 250 ns. The result is automatically latched to two 16-bit registers M&N (sign and 15 higher bits in M, 15 lower bits in N; LSB in N is zero) at the end of each instruction cycle. A new product is available for use after every instruction cycle, providing significant advantages in maximizing processing speed for real time signal processing.

Stack

The SPI contains a 4-level program stack for efficient program usage and interrupt handling.

Interrupt

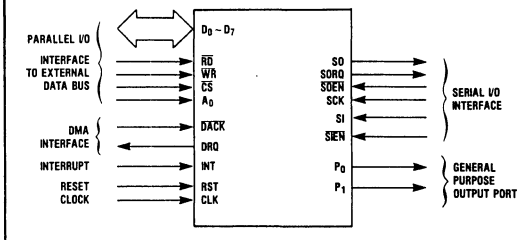
A single level interrupt is supported by the SPI. Upon sensing a high level on the INT terminal, a subroutine call to location 100H is executed. The EI bit of the status register is automatically reset to 0, thus disabling the interrupt facilities until reenabled under program control.

Input/Output

General

The SPI has three communication ports; two serial and one 8-bit parallel, each with its own control lines for interface handshaking. The parallel port also includes DMA control lines (DRQ and DACK) for high speed data transfer and reduced processor overhead. A general purpose 2-line output port rounds out a full complement of interface capability.

Figure 1.



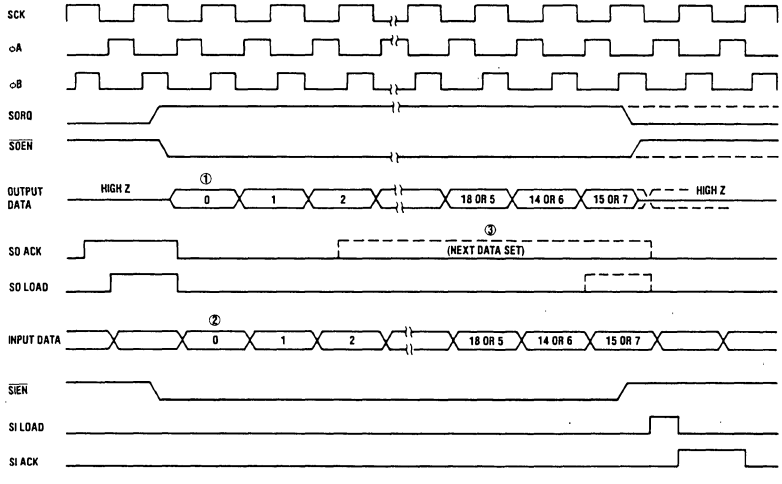
Serial I/O

The two shift registers (SI, SO) are software-configurable to single or double byte transfers. The shift registers are externally clocked (SCK) to provide a simple interface between the SPI and serial peripherals such as A/D and D/A converters, codecs, or other SPIs.

Parallel I/O

The 8-bit parallel I/O port may be used for transferring data or reading the SPI's status. Data transfer is handled through a 16-bit Data Register (DR) that is software-configurable for double or single byte data transfers. The port is ideally suited for operating with 8080, 8085, and 8086 processor buses and may be used with other processors and computer systems.

Figure 2. Serial I/O Timing



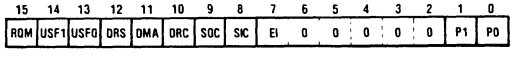
NOTES: ① DATA CLOCKED OUT ON FALLING EDGE OF SCK
② DATA CLOCKED IN ON RISING EDGE OF SCK
③ BROKEN LINE DENOTES CONSECUTIVE SENDING OF NEXT DATA

Table 3. Parallel R/W Operation

$\overline{CS}$	A_0	$\overline{WR}$	$\overline{RD}$	OPERATION
1	X	X	X	Internal operation is not affected: D_0-D_7 are kept under a high impedance
X	X	1	1	
0	0	0	1	Data of D_0-D_7 are latched to DR register[1]
0	0	1	0	Contents of DR register are output to D_0-D_7[1]
0	1	0	1	Inhibited
0	1	1	0	8 higher bits of SR register are output to D_0-D_7
0	X	0	0	Inhibited

NOTE 1: Eight MSBs or 8 LSBs of data register (DR) are used depending on DR status bit (DRS). The condition of $\overline{DACK}=0$ is equivalent to $A_0=\overline{CS}=0$.

Figure 3. Status Register



The status register is a 16-bit register in which the 8 most significant bits may be read by the system's MPU for the latest I/O and processing status.

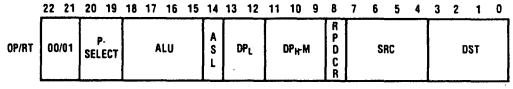
Table 4. Status Register Flags

FLAG	OPERATION
RQM (Request for Master)	A read or write from DR to IDB sets RQM = 1. An external read (write) resets RQM = 0.
USF1 and USF0 (User Flags 1 and 0	General purpose flags which may be read by an external processor for user defined signaling
DRS (DR Status)	For 16-bit DR transfers (DRC = 0). DRS = 1 after first 8 bits have been transferred. DRS = 0 after all 16 bits transferred.
DMA (DMA Enable)	DMA = 0 (Non-DMA transfer mode) DMA = 1 (DMA transfer mode).
DRC (DR Control)	DRC = 0 (16-bit mode) DRC = 1 (8-bit mode).
SOC (SO Control)	SOC = 0 (16-bit mode) SOC = 1 (8-bit mode).
SIC (SI Control)	SIC = 0 (16-bit mode) SIC = 1 (8-bit mode).
EI (Enable Interupt)	EI = 0 (interrupts disabled) EI = 1 (interrupts enabled).
P1, P0 (Ports 0 and 1)	P0 and P1 directly control the state of output pins P0 and P1.

Instructions

The SPI has 3 types of instructions, all of which are one 23-bit word and execute in 250 ns.

Figure 4. Arithmetic/Move-Return (OP = 00/RT = 01)



OP/RT Instruction Field Specification

There are two instructions of this type, both of which are capable of executing all ALU functions listed in Table 6. The ALU functions operate on the value specified by the P-select field. (See Table 5.)

Besides the arithmetic functions these instructions can also modify (1) the RAM Data Pointer DP, (2) the Data ROM Pointer RP, and (3) move data along the on-chip data bus from a source register to a destination register (the possible source and destination registers are listed in Tables 11 and 12 respectively). The difference in the two instructions of this type is that RT executes a subroutine or interrupt return at the end of the instruction cycle while the OP does not.

Table 5. P-Select Field

P-SELECT FIELD			
MNEMONIC	**D_{20}**	**D_{19}**	**INPUT**
RAM	0	0	RAM
IDB	0	1	Internal Data Bus[1]
M	1	0	M Register
N	1	1	N Register

NOTE 1: Any value on the on-chip data bus. Value may be selected from any of the registers listed in Table 11 source register selections.

Table 6. ALU Field

	ALU FIELD					FLAGS AFFECTED*						
						FLAG A	SA1	SA0	CA	ZA	OVA1	OVA0
MNEMONIC	**D_{18}**	**D_{17}**	**D_{16}**	**D_{15}**	**ALU FUNCTION**	FLAG B	SB1	SB0	CB	ZB	OVB1	OVB0
NOP	0	0	0	0	No Operation		—	—	—	—	—	—
OR	0	0	0	1	OR		X	↕	0	↕	0	0
AND	0	0	1	0	AND		X	↕	0	↕	0	0
XOR	0	0	1	1	Exclusive OR		X	↕	0	↕	0	0
SUB	0	1	0	0	Subtract		↕	↕	↕	↕	↕	↕
ADD	0	1	0	1	ADD		↕	↕	↕	↕	↕	↕
SBB	0	1	1	0	Subtract with Borrow		↕	↕	↕	↕	↕	↕
ADC	0	1	1	1	Add with Carry		↕	↕	↕	↕	↕	↕
DEC	1	0	0	0	Decrement Acc		↕	↕	↕	↕	↕	↕
INC	1	0	0	1	Increment Acc		↕	↕	↕	↕	↕	↕
CMP	1	0	1	0	Complement Acc (1's Complement)		X	↕	0	↕	0	0
SHR1	1	0	1	1	1-bit R-Shift		X	↕	↕	↕	0	0
SHL1	1	1	0	0	1-bit L-Shift		X	↕	↕	↕	0	0
SHL2	1	1	0	1	2-bit L-Shift		X	↕	0	↕	0	0
SHL4	1	1	1	0	4-bit L-Shift		X	↕	0	↕	0	0
XCHG	1	1	1	1	8-bit Exchange		X	↕	0	↕	0	0

NOTES: ↕ May be affected, depending on the results — Previous status can be held 0 Reset X Indefinite

Table 7. ASL Field

MNEMONIC	ASL FIELD D_{14}	ACC SELECTION
ACCA	0	ACCA
ACCB	1	ACCB

Table 8. DP_L Field

MNEMONIC	D_{13}	D_{12}	LOW DP MODIFY (DP_3-DP_0)
DPNOP	0	0	No Operation
DPINC	0	1	Increment DP_L
DPDEC	1	0	Decrement DP_L
DPCLR	1	1	Clear DP_L

Table 9. RPDCR Field

MNEMONIC	RPDCR D_8	OPERATION
RPNOP	0	No Operation
RPDEC	1	Decrement RP

Table 10. SRC Field

MNEMONIC	SCR FIELD D_7	D_6	D_5	D_4	SPECIFIED REGISTER
NON	0	0	0	0	NO Register
A	0	0	0	1	AccA (Accumulator A)
B	0	0	1	0	AccB (Accumulator B)
TR	0	0	1	1	TR Temporary Register
DP	0	1	0	0	DP Data Pointer
RP	0	1	0	1	RP ROM Pointer
RO	0	1	1	0	RO ROM Output Data
SGN	0	1	1	1	SGN Sign Register
DR	1	0	0	0	DR Data Register
DRNF	1	0	0	1	DR Data No Flag[1]
SR	1	0	1	0	SR Status
SIM	1	0	1	1	SI Serial in MSB[2]
SIL	1	1	0	0	SI Serial in LSB[3]
K	1	1	0	1	K Register
L	1	1	1	0	L Register
MEM	1	1	1	1	RAM

NOTE 1: DR to IDB RQM not set. IN DMA DRQ not set.
NOTE 2: First bit in goes to MSB, last bit to LSB.
NOTE 3: First bit in goes to LSB, last bit to MSB (bit reversed).

Table 11. DP_H-M Field

MNEMONIC	D_{11}	D_{10}	D_9	HIGH DP MODIFY
M0*	0	0	0	Exclusive OR or DP_H (DP_6-DP_4) with the Mask defined by the three bits (D_{11}-D_9) of the DP_H-M field
M1	0	0	1	
M2	0	1	0	
M3	0	1	1	
M4	1	0	0	
M5	1	0	1	
M6	1	1	0	
M7	1	1	1	

*No change

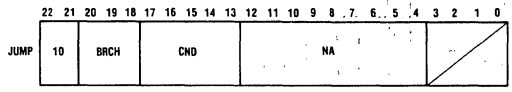
Table 12. Destination Field Specifications

MNEMONIC	DST FIELD D_3	D_2	D_1	D_0	SPECIFIED REGISTER
@NON	0	0	0	0	NO Register
@A	0	0	0	1	A_{CC} A (Accumulator A)
@B	0	0	1	0	A_{CC} B (Accumulator B)
@TR	0	0	1	1	TR Temporary Register
@DP	0	1	0	0	DP Data Pointer
@RP	0	1	0	1	RP ROM Pointer
@DR	0	1	1	0	DR Data Register
@SR	0	1	1	1	SR Status Register
@SOL	1	0	0	0	SO Serial Out LSB[1]
@SOM	1	0	0	1	SO Serial Out MSB[2]
@K	1	0	1	0	K (Mult)
@KLR	1	0	1	1	IDB→K ROM→L[3]
@KLM	1	1	0	0	Hi RAM→K IDB→L[4]
@L	1	1	0	1	L (Mult)
@NON	1	1	1	0	NO Register
@MEM	1	1	1	1	RAM

NOTE 1: LSB is first bit out.
NOTE 2: MSB is first bit out.
NOTE 3: Internal data bus to K and ROM to L register.
NOTE 4: Contents of RAM address specified by DP_6=1 (i.e., 1, DP_5, DP_4, DP_0) is placed In K register. IDB is placed in L.

Jump/Call/Branch

Figure 5. JP Instruction Field Specification



Three types of program counter modifications are accommodated by the processor and are listed in Table 13. All the instructions, if unconditional or if the specified condition is true, take their next program execution address from the Next Address field (NA); otherwise PC = PC + 1.

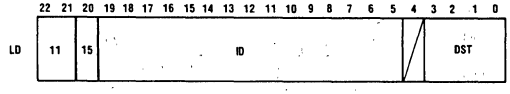
Table 13. BRCH Field

MNEMONIC	BRCH FIELD D_{20}	D_{19}	D_{18}	FUNCTION
JMP	1	0	0	Unconditional Jump
CALL	1	0	1	Subroutine Call
JNCA	0	1	0	Conditional Jump

For the conditional jump instruction, the condition field specifies the jump condition. Table 14 lists all the instruction mnemonics of the Jump/Call/Branch codes.

Load Data (LDI)

Figure 6. LD Instruction Field Specification



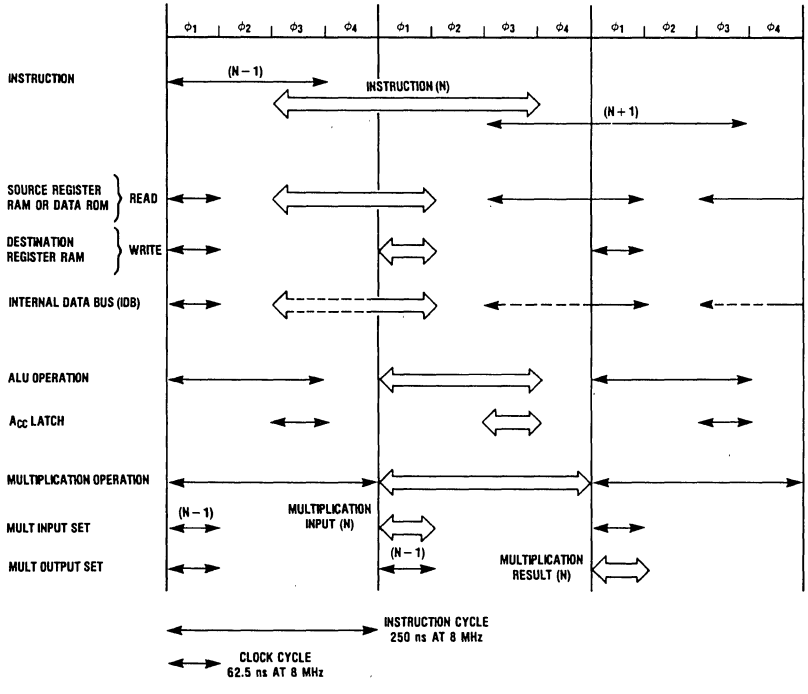
The Load Data instruction will take the 16-bit value contained in the Immediate Data field (ID) and place it in the location specified by the Destination field (DST) (see Table 12).

Table 14. BRCH/CND Fields

MNEMONIC	CND FIELD D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	CONDITION[1]
JNCA	0	0	0	0	0	CA=0
JCA	0	0	0	0	1	CA=1
JNCB	0	0	0	1	0	CB=0
JCB	0	0	0	1	1	CB=1
JNZA	0	0	1	0	0	ZA=0
JZA	0	0	1	0	1	ZA=1
JNZB	0	0	1	1	0	ZB=0
JZB	0	0	1	1	1	ZB=1
JNOVA0	0	1	0	0	0	OVA0=0
JOVA0	0	1	0	0	1	OVA0=1
JNOVB0	0	1	0	1	0	OVB0=0
JOVB0	0	1	0	1	1	OVB0=1
JNOVA1	0	1	1	0	0	OVA1=0
JOVA1	0	1	1	0	1	OVA1=1
JNOVB1	0	1	1	1	0	OVB1=0
JOVB1	0	1	1	1	1	OVB1=1
JNSA0	1	0	0	0	0	SA0=0
JSA0	1	0	0	0	1	SA0=1
JNSB0	1	0	0	1	0	SB0=0
JSB0	1	0	0	1	1	SB0=1
JNSA1	1	0	1	0	0	SA1=0
JSA1	1	0	1	0	1	SA1=1
JNSB1	1	0	1	1	0	SB1=0
JSB1	1	0	1	1	1	SB1=1
JDPL0	1	1	0	0	0	DP_L=0
JDPLF	1	1	0	0	1	DP_L=F(HEX)
JNSIAK	1	1	0	1	0	SIACK=0
JSIAK	1	1	0	1	1	SIACK=1
JNSOAK	1	1	1	0	0	SOACK=0
JSOAK	1	1	1	0	1	SOACK=1
JNRQM	1	1	1	1	0	RQM=0
JRQM	1	1	1	1	1	RQM=1

NOTE 1: BRCH or CND values not in this table are prohibited.

Figure 7. Instruction Timing (Four Phase-Internal Clock)



Instruction Timing

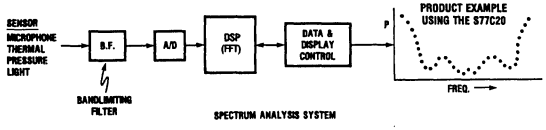
To control the execution of instructions, the external 8-MHz clock is divided into a four-phase, nonoverlapping clock. Execution begins at the rising edge of $\phi 3$ and ends at the falling edge of $\phi 2$. The ALU commences operation at the rise of $\phi 1$, and completes all operations at the fall of $\phi 3$.

Once an instruction-ROM address is available at the rise of $\phi 3$, the instruction is latched, and the source register and RAM address are determined so that data may be put on the internal bus by the fall of $\phi 4$. The ALU input is latched at the rise of $\phi 1$, and the output is available for accumulator latch at the rise of $\phi 3$. The cycle then repeats.

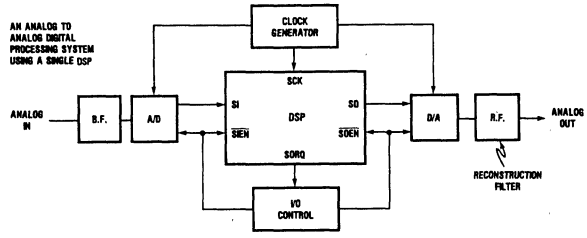
The multiplier takes its input at the rise of $\phi 1$, and its results are available in 250 ns, at the rise of the next $\phi 1$.

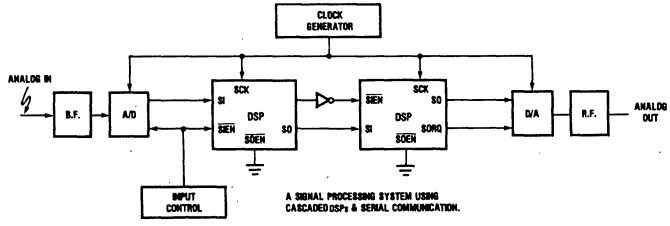
S77C20

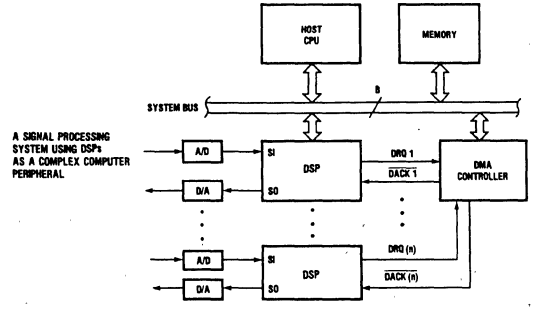
S7720



SPECTRUM ANALYSIS SYSTEM







Technical manual also available describing the use of the S77C20 Signal Processing Interface chip including functional description, instructions, and several system examples. Please contact factory.

GOULD

AMI Semiconductors

16-Bit Cascadable CMOS ALU

Preliminary Data Sheet

S614381

COMMUNICATION PRODUCTS

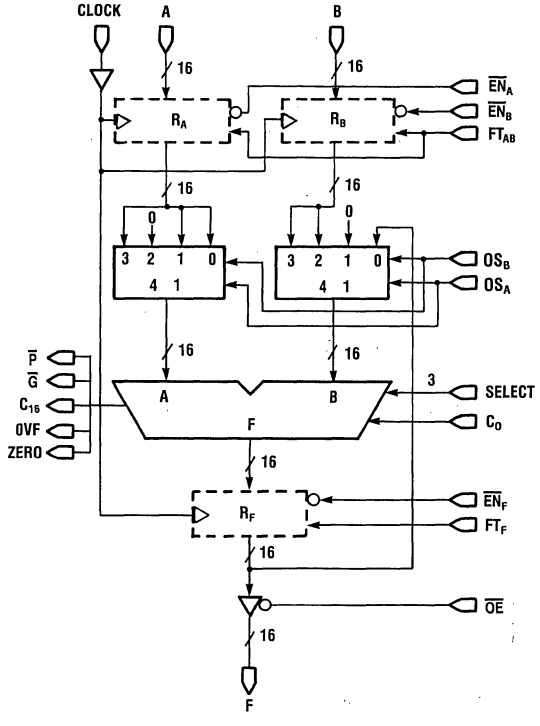
Features

- Hi-Speed HCMOS 16-Bit Cascadable ALU.
- Extension Architecture of 74S381.
- Input/Output Registers with Transparent Mode.
- Cascadable, With or Without Carry Lookahead.
- Force A or B = O Allows two's complement, also Pass A, Pass B.
- Internal Feedback Path for Accumulator Operation.
- Status & Carry Outputs Available.
- CMOS Technology with 5v and TTL I/O Operation.

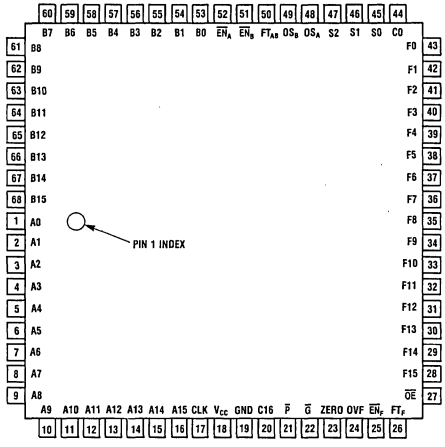
General Description

The S614381 is a flexible 16-bit hi-speed Arithmetic Logic Unit Slice. It combines four 74S381 type 4-bit ALU's with a 74S182 carry lookahead generator, along with input and output registers for pipeline operation. It also contains a multiplexed input operand to the ALU for added ALU functions. It retains full functional compatibility to the 74S381 type devices in a single 68-pin J-Lead PLCC package.

Block Diagram



Pin Configuration



S614381

Pin Definitions

A_{0-15}	A Input
B_{0-15}	B Input
F_{0-15}	Result Output
C_0	Carry Input
C_{16}	Carry Output
$\overline{P}$	Carry Propagate Output
$\overline{G}$	Carry Generate Output
OVF	ALU Overflow Flag
ZERO	ALU Result Zero Flag
$\overline{EN}_A$	A Register Enable
$\overline{EN}_B$	B Register Enable
FT_{AB}	A, B, Register Feedthrough Control
$\overline{EN}_F$	F Register Enable
FT_F	F Register Feedthrough Control
OS_B	B Operand Select
OS_A	A Operand Select
S_{0-2}	Instruction Select
$\overline{OE}$	Output Enable
CLK	Clock
V_{CC}, GND	Power Supply

Architecture and Operation

The S614381 operates on 16 bit operands denoted A and B, and produces a 16 bit result F. The ALU provides three arithmetic, three logical and two initialization functions, selectable from three select lines. Full ALU status is provided, allowing the S614381 to be cascaded for longer words. Input/output registers are provided for pipeline operation with a bypass feature under user control. An internal multiplexer allows multiple source operand selection into the ALU. This allows extended ALU functions; such as PASS A, PASS B, two's complementation and a feedback path of the output of the ALU back to its input for accumulator operation. Furthermore, the mux can force A or B input to zero, allowing unary functions to be performed on either operand.

ALU Operation

The ALU is controlled by three select lines S_2–S_0. The ALU functions and associated control signals are given in Figure 1.

The functions B minus A, and A minus B, (two's complement subtraction) can be achieved by setting C_O = 1 of the least significant S614381 slice and selecting the function codes 001 and 010 respectively.

ALU Status

Two status bits are provided from the ALU. They are overflow and zero. Three cascading functions are also provided which are Carry, Propogate, and Generate. These outputs are defined for the three arithmetic functions only. The Generate, Propogate, C_{16}, and OVF flags for the A + B operation are defined in Figure 2. The status flags produced for NOT(A) + B and A + NOT(B) can be found by complementing A_i and B_i in Figure 2 respectively. The ALU sets the Zero output when all sixteen output bits are zero.

Figure 1. ALU Function Definition

S_2	S_1	S_0	Function
0	0	0	CLEAR (F = 00 . . . . 0)
0	0	1	NOT(A) + B (B MINUS A)
0	1	0	A + NOT(B) (A MINUS B)
0	1	1	A + B (A PLUS B)
1	0	0	A XOR B
1	0	1	A OR B
1	1	0	A AND B
1	1	1	PRESET (F = 11 . . . . 1)

Figure 2. ALU Status Flags

BIT CARRY GENERATE=$g_i=A_iB_i$, FOR i=0,1, . . . ,15

BIT CARRY PROPAGATE=$p_i=A_i+B_i$, FOR i=0,1, . . . ,15

$P_0=p_0$

$P_i=p_i(P_{i-1})$ FOR i=1,2, . . . ,15

and

$G_0=g_0$

$G_i=g_i+p_i(G_{i-1})$ FOR i=1,2, . . . ,15

$C_i=G_{i-1}+P_{i-1}(C_{i-1})$ FOR i=1,2, . . . ,15

then

$\overline{G}=NOT(G_{15})$

$\overline{P}=NOT(P_{15})$

$C_{16}=G_{15}+P_{15}C_{15}$

$OVF=C_{15}$ XOR C_{16}

Operand Registers

There are two 16-bit wide input registers for operands A and B. These registers have a common clock triggered on the rising edge, and separate register enable control signals $\overline{EN}_A$ and $\overline{EN}_B$. This architecture allows the S614381 to accept arguments from a single 16-bit data bus. In the case where it is not desired to have registered inputs for A and B, a control line FT_{AB} allows the registers to become transparent.

When FT_{AB} is asserted, the operand registers A, B are bypassed; however, they continue to function normally via the $\overline{EN}_A$ and $\overline{EN}_B$ controls. The contents of the input registers will again be available to the ALU by releasing the control line FT_{AB}.

Output Register

The output of the ALU, drives the input of a 16-bit register. This register is clocked by the same rising edge clock as the input registers. By disabling the output register, intermediate results can be held while loading new input operands. The output buffer of the output register is three-state controlled by $\overline{OE}$ input to allow the S614381 to be used in a single bi-directional bus system. The output register can also be made transparent by asserting the FT_F control signal. As with the input registers, when FT_F is asserted, the output register is bypassed, but the register continues to function normally via the $\overline{EN}_F$ control. The contents of the output register will again be made available on the output pins if FT_F is released. With both control signals FT_{AB} and FT_F asserted (High), the S614381 is functionally identical to four cascaded 74S381 type devices.

Operand Selection

There are two operand select lines OS_A and OS_B that control the 4 to 1 multiplexers immediately preceding the ALU inputs. These multiplexers allow several options as to ALU source inputs. Figure 3 shows the inputs to the ALU as a function of the operand select inputs. Either A or B operand may be forced to zero.

Figure 3. Operand Selection Control

OS_B	OS_A	OPERAND B	OPERAND A
0	0	F	A
0	1	0	A
1	0	B	0
1	1	B	A

The S614381 can be configured as a chain calculation by having both select lines released (low). The registered ALU output is passed back to the B input of the ALU. In this way, accumulation operations can be performed by providing new operands via the A input port. The accumulator can be pre-loaded from the A input by setting OS_A true. By forcing the function select lines to the clear state 000, the accumulator may be cleared. Note that this feedback operation is not affected by the state of the FT_F control. That is, the F outputs of the S614381 may be driven directly by the ALU (FT_F = high). The output register continues to function, however, and provides the ALU B operand source.

Absolute Maximum Ratings

DC Supply Voltage (V_{DD}–V_{SS})	+7V
Operating Temperature	0°C to 70°C
Storage Temperature	−55°C to +150°C
Digital Input	V_{SS} − 0.3V ≤ V_{IN} ≤ V_{DD} +.3V

DC Electrical Operating Characteristics: T_A = 0°C to +70°C; V_{DD} = +5V (±10%); V_{SS} = 0V unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Low Level Input Voltage		V_{SS}		0.8	V
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{OL}	Low Level Output Voltage	I_{OL}=4mA	0		0.4	V
V_{OH}	High Level Output Voltage	I_{OH}=.8mA	2.4		V_{DD}	V

AC Electrical Characteristics: $T_A = 70°C$; $V_{DD} = +4.75V$; $V_{SS} = 0V$

Input	To Output				
$FT_{AB} = 0$, $FT_F = 0$	**F_{0-15}**	**$\overline{P}$, $\overline{G}$**	**OVF, ZERO**	**C_{16}**	**Units**
Clock	25	43	43	39	ns
C_0	—	—	50	38	ns
S_0–S_2, OS_A, OS_B	—	42	42	49	ns
$FT_{AB} = 0$, $FT_F = 1$	**F_{0-15}**	**$\overline{P}$, $\overline{G}$**	**OVF, ZERO**	**C_{16}**	**Units**
Clock	60	45	50	48	ns
C_0	45	—	50	38	ns
S_0–S_2, OS_A, OS_B	44	49	38	49	ns
$FT_{AB} = 1$, $FT_F = 0$	**F_{0-15}**	**$\overline{P}$, $\overline{G}$**	**OVF, ZERO**	**C_{16}**	**Units**
A_{0-15}, B_{0-15}	—	35	50	38	ns
Clock	25	—	—	—	ns
C_0	—	—	50	38	ns
S_0–S_2, OS_A, OS_B	—	47	38	47	ns
$FT_{AB} = 1$, $FT_F = 1$	**F_{0-15}**	**$\overline{P}$, $\overline{G}$**	**OVF, ZERO**	**C_{16}**	**Units**
A_{0-15}, B_{0-15}	57	35	50	37	ns
Clock	—	—	—	—	
C_0	45	—	50	38	ns
S_0–S_2, OS_A, OS_B	44	47	38	49	ns

NOTE:
1. Values are of average times based on the given: test truth table (inputs/outputs)
2. Actual values depend on the specific input patterns of A_0–A_{15}, B_0–B_{15}, C_0, S_{0-2}.
3. All outputs are loaded with 50pf, during AC testing.

Clock Cycle Time and Pulse Width

High Pulse	15	ns
Low Pulse	15	ns
Minimum Cycle Time	50	ns

Setup and Hold Time With Respect to Clock Rising Edge

Input	Setup		Hold	Units
	$FT_{AB} = 0$	$FT_{AB} = 1$	$FT_{AB} = 0/1$	
A_0–A_{15}, B_0–B_{15}	6	31	2	ns
$\overline{EN_A}$, $\overline{EN_B}$, $\overline{EN_F}$,	5	5	0	ns

Three State Enable/Disable Times

t_{en}	15	ns
t_{DS}	10	ns

Test Truth Table (Inputs/Outputs)

	Inputs						Outputs							
Function	S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	$\overline{G}$	$\overline{P}$	OVF	C_{16}
Clear	0	0	0	X	X	X	0	0	0	0	0	0	1	1
B Minus A	1	0	0	0	0	0	1	1	1	1	1	0	0	0
				0	0	1	0	1	1	1	0	0	0	1
				0	1	0	0	0	0	0	1	1	0	0
				0	1	1	1	1	1	1	1	0	0	0
				1	0	0	0	0	0	0	1	0	0	1
				1	0	1	1	1	1	1	0	0	0	1
				1	1	0	1	0	0	0	1	1	0	0
				1	1	1	0	0	0	0	1	0	0	1
A Minus B	0	1	0	0	0	0	1	1	1	1	1	0	0	0
				0	0	1	0	0	0	0	1	1	0	0
				0	1	0	0	1	1	1	0	0	0	1
				0	1	1	1	1	1	1	1	0	0	0
				1	0	0	0	0	0	0	1	0	0	1
				1	0	1	1	0	0	0	1	1	0	0
				1	1	0	1	1	1	1	0	0	0	1
				1	1	1	0	0	0	0	1	0	0	1
A Plus B	1	1	0	0	0	0	0	0	0	0	1	1	0	0
				0	0	1	1	1	1	1	1	0	0	0
				0	1	0	1	1	1	1	1	0	0	0
				0	1	1	0	1	1	1	0	0	0	1
				1	0	0	1	0	0	0	1	1	0	0
				1	0	1	0	0	0	0	1	0	0	1
				1	1	0	0	0	0	0	1	0	0	1
				1	1	1	1	1	1	1	0	0	0	1
A⊕B	0	0	1	0/1	0	0	0	0	0	0	1	1	0	0
				0/1	0	1	1	1	1	1	1	1	0	0
				0/1	1	0	1	1	1	1	1	0	0/1	0/1
				0/1	1	1	0	0	0	0	0	0	1	1
A + B	1	0	1	0/1	0	0	0	0	0	0	1	1	0	0
				0/1	0	1	1	1	1	1	1	1	0	0
				0/1	1	0	1	1	1	1	1	1	0	0
				0/1	1	1	1	1	1	1	1	0	0/1	0/1
AB	0	1	1	0/1	0	0	0	0	0	0	0	0	1	1
				0/1	0	1	0	0	0	0	1	1	0	0
				0/1	1	0	0	0	0	0	0	0	1	1
				0/1	1	1	1	1	1	1	1	0	0/1	0/1
Preset	1	1	1	0/1	0	0	1	1	1	1	1	1	0	0
				0/1	0	1	1	1	1	1	1	1	0	0
				0/1	1	0	1	1	1	1	1	1	0	0
				0/1	1	1	1	1	1	1	1	0	0/1	0/1

1 = HIGH Voltage Level
0 = LOW Voltage Level

GOULD

AMI Semiconductors

Dual Port Memory Controller (D.P.M.C.)

Preliminary Data Sheet

S61C35

Features

- Full asynchronous arbitration between two Ports for access to user selected memory (SRAM, DRAM, EPROM, etc.)
- Easy 8/16 (32) bit microprocessor interface
- Allows building Dual Port Memory of any depth, width, from standard (SRAM, DRAM, EPROM)
- Fast control signal passing of winning port to user selected RAM
- Upper/lower Data Strobes for 8/16 (32) bit applications
- $\overline{BUSY}$ output function for loosing Port (open drain for or-tied operation)
- Four separately selected registers per Port for:
  —message passing between Ports
  —locking capability for either Port
  —interrupt mechanism for above features
- $\overline{INT}$ output function for both Ports (open drain for or-tied operation)
- Both Ports operate independently
- Master/slave mode for controller ganging
- 5V supply, 48 pin DIP
- Full TTL compatibility

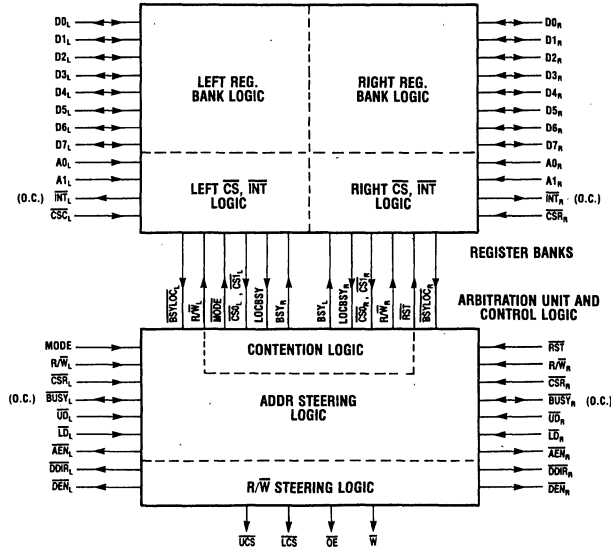
Applications

- Multiprocessor shared memory
- Asynchronous interprocessor communication
- Data buffering between asynchronous processes
- Software FIFO buffers

General Description

The S61C35 is a fast access Dual Port Memory Controller (D.P.M.C.). It allows fully asynchronous fast arbitration between two (2) different Ports (Microprocessor type interfaces). The winning Port is allowed

Functional Block Diagram



Pin Function

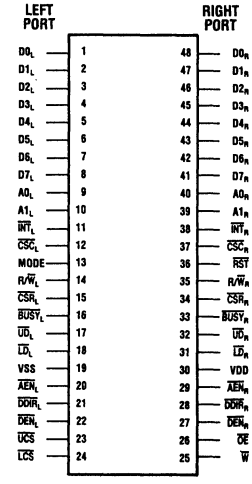
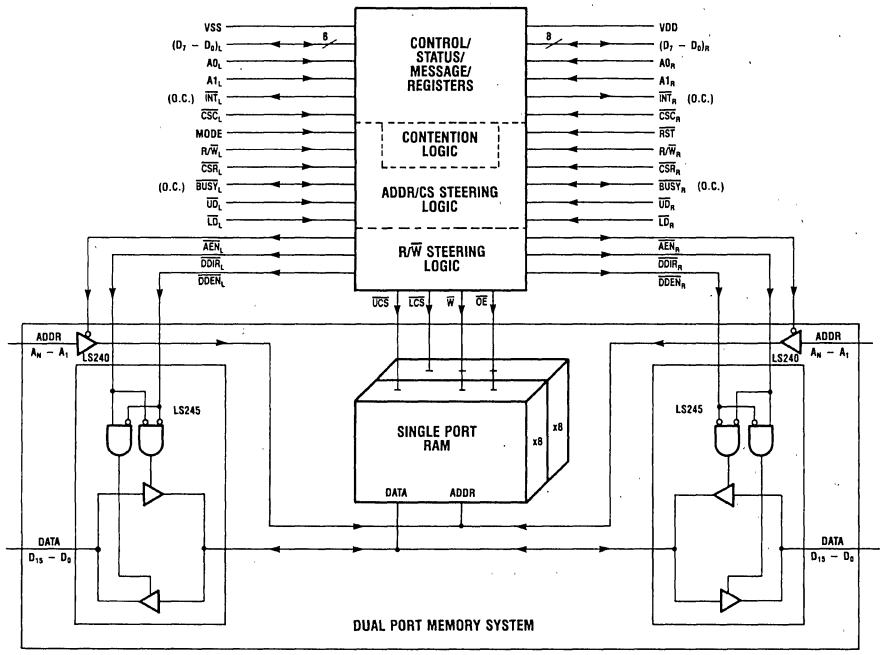
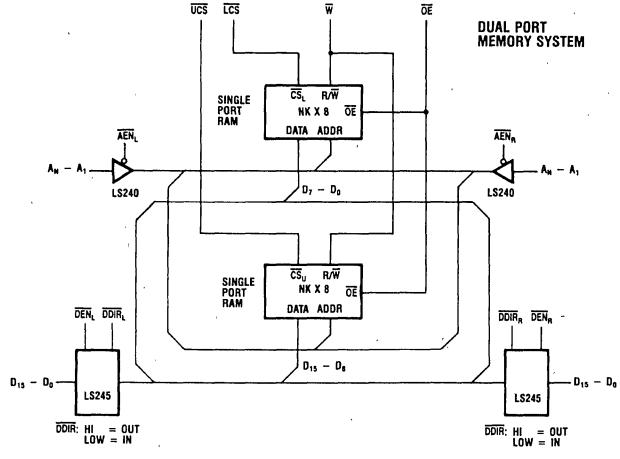


Figure 1. Example Configuration of S61C35 for NK x 16 Dual Port Memory





control signal access to a bank of user selected and designed dual ported memory (SRAM, DRAM, EPROM, etc.). (See fig. 1 for example). The loosing Port is sent a busy signal to indicate it should wait for access. The S61C35 allows the system designer to create fast inexpensive dual ported memory out of existing single port RAM chips of any variety and type (SRAM, DRAM, EPROM, etc.). He also has the freedom to create any desired depth or width to his dual port memory.

In addition to fast, arbitrated, dual ported user designed memory, each port can access its own on chip register bank, composed of four (4) independent registers per port for added control features. These registers are control, status, message-in, and message-out. They allow the system designer the ability under program control to lock out the opposite port to access of the dual ported memory. There is also the ability for the locked out port to override this condition and select whether he will receive a busy condition in hardware when he is locked out. Furthermore, there is a complete facility for message passing between ports via status register handshake flags. Both the locking and message passing facility cause appropriate status bits to be set or cleared. The control register allows selected masking of these status bits to form a master interrupt to the user. Finally, the S61C35 can be used in a slave mode through use of a hardware mode pin. This allows selected options for ganging of controllers.

Detailed Description

The Dual Port Memory Controller (S61C35) is a high speed dual ported arbitration unit between two (2) fully asynchronous ports to allow multiplexed access to a user defined dual ported memory, built from off the shelf single ported RAM devices. In this way, a user can define and build his own dual port memory system in accordance to his own specified depth, width, speed, type (i.e., SRAM, DRAM, EPROM, etc.) or other considerations.

I Arbitration Unit and Control Logic

The Dual Port Memory Controller (D.P.M.C.) uses the input signals of $\overline{CSR}_L$ and $\overline{CSR}_R$ to asynchronously arbitrate as to who will gain access to the user defined dual port memory system. Once arbitration is complete, the loosing port receives its $\overline{BUSY}$ signal low, as long as its $\overline{CSR}$ is low. The D.P.M.C. will then use the status signals of R/$\overline{W}$, $\overline{UDS}$, $\overline{LDS}$ of the winning port to create

Dip Pin Description

Pin	Name	Pin	Name
1	$D0_L$	48	$D0_R$
2	$D1_L$	47	$D1_R$
3	$D2_L$	46	$D2_R$
4	$D3_L$	45	$D3_R$
5	$D4_L$	44	$D4_R$
6	$D5_L$	43	$D5_R$
7	$D6_L$	42	$D6_R$
8	$D7_L$	41	$D7_R$
9	$A0_L$	40	$A0_R$
10	$A1_L$	39	$A1_R$
11	$\overline{INT}_L$	38	$\overline{INT}_R$
12	$\overline{CSC}_L$	37	$\overline{CSC}_R$
13	MODE	36	$\overline{RST}$
14	R/$\overline{W}_L$	35	R/$\overline{W}_R$
15	$\overline{CSR}_L$	34	$\overline{CSR}_R$
16	$\overline{BUSY}_L$	33	$\overline{BUSY}_R$
17	$\overline{UD}_L$	32	$\overline{UD}_R$
18	$\overline{LD}_L$	31	$\overline{LD}_R$
19	VSS	30	VDD
20	$\overline{AEN}_L$	29	$\overline{AEN}_R$
21	$\overline{DDIR}_L$	28	$\overline{DDIR}_R$
22	$\overline{DEN}_L$	27	$\overline{DEN}_R$
23	$\overline{UCS}$	26	$\overline{OE}$
24	$\overline{LCS}$	25	$\overline{W}$

the necessary dual port memory system control signals. They are broken down into two (2) classes:

1) RAM enable signals for the winning ports data and address lines ($\overline{DDIR}$, $\overline{DEN}$, $\overline{AEN}$). And
2) RAM Control signals for the winning port to control the single port RAM of the user's own specification ($\overline{UCS}$, $\overline{LCS}$, $\overline{W}$, $\overline{OE}$).

The RAM enable signals are used in conjunction with user defined external data and address drivers (e.g., 74xx245, 74xx240 or similar type). The RAM control signals are used to form an upper and/or lower chip select for the user specified single port RAM. These are directly generated from $\overline{UD}$ and $\overline{LD}$ of the winning port. Furthermore, the R/$\overline{W}$ of the winning port generates the

Pin Description

Pin Name	I/O	Pin Function
$D7_{L/R}$–$D0_{L/R}$	I/O	8 bit bi-directional data bus, for access to the left/right port register bank.
$A1_{L/R}$–$A0_{L/R}$	I	Address lines for left/right port register bank register selection.
$\overline{CSC}_{L/R}$	I	System chip select for left/right port register bank.
$\overline{INT}_{L/R}$	O(O.C.)	Interrupt output for left/right port. (Open collector output)
Mode	I	Allows selection of controller mode for either: Hi = Master Mode Lo = Slave Mode
$\overline{RST}$	I	Reset input for the controller.
$R/\overline{W}_{L/R}$	I	Read/write input for the left/right port register bank, as well as dual port memory control logic.
$\overline{CSR}_{L/R}$	I	System chip select for left/right port dual port memory system access.
$\overline{BUSY}_{L/R}$	O(O.C.)	Left/right port busy flag to indicate port has lost dual port memory access or control/status register bank access rights. (Open collector output)
$\overline{UD}_{L/R}$	I	System left/right port upper data strobe.
$\overline{LD}_{L/R}$	I	System left/right port lower data strobe.
$\overline{DDIR}_{L/R}$	O	System left/right port data direction output control line.
$\overline{DEN}_{L/R}$	O	System left/right port data enable output control line.
$\overline{UCS}$	O	Single port RAM. Upper (byte, word, etc.) chip select line.
$\overline{LCS}$	O	Single port RAM. Lower (byte, word, etc.) chip select line.
$\overline{OE}$	O	Single port RAM output enable line option.
$\overline{W}$	O	Single port memory write control line.

Note: Both left and right ports are designated together for clarity. (i.e. $\overline{CSC}_L$, $\overline{CSC}_R$ = $\overline{CSC}_{L/R}$)

appropriate $\overline{W}$ or $\overline{OE}$ for the single port RAM. Table 1 shows the port's status signals and resulting winning ports RAM enable and RAM control signal generation. It must be kept in mind that it is the user's responsibility to alleviate any possible common I/O contention problems in his dual port memory system from use of common I/O single port RAM.

II Register Bank

A) General Overview

The Dual Port Memory Controller (D.P.M.C.) has two separate independent register banks, one for each port. Each register bank has its own separate chip select pins ($\overline{CSC}_L$, $\overline{CSC}_R$) for access to that port's register bank. There are four registers within each register bank, which are separately addressed by each port through their respective A1–A0 address lines. This allows for four (4) internal registers per register bank and are designated in Table 2. Each register bank uses its appropriate $R/\overline{W}$ signal to read and write to its registers. It is important to note that except for Control Register (CR0) and Status Register (CR1) each port can simultaneously read or write to its own register bank independent of the other port. The register banks are also separately selected ($\overline{CSC}_{L/R}$), apart from the dual port memory chip selects ($\overline{CSR}_{L/R}$) and are on-board the chip. The register banks contain four (4) separate registers each, and their access is outlined in Table 3.

They are: 1) Control Register (CR0)
2) Status Register (CR1)
3) Message-In Register (CR2)
4) Message-Out Register (CR3)

Figures 3–5 show the Left/Right port register bit definitions of (CR0–CR3) respectively.

Table 1. Control Signals Generated For Winning Port

A.

$\overline{UD}_{L/R}$	$\overline{LD}_{L/R}$	$\overline{CSR}_{L/R}$		$\overline{UCS}$	$\overline{LCS}$
0	0	0		0	0
0	1	0		0	1
1	0	0	GENERATES	1	0
1	1	0		1	1

Port That Loses Has Its $\overline{UD}$, $\overline{LD}$ Ignored

B.

$\overline{CSR}_{L/R}$	$R/\overline{W}_{L/R}$		$\overline{DEN}_{L/R}$	$\overline{DDIR}^{*}_{L/R}$	$\overline{W}$	$\overline{OE}$
0	1		0	1	1	0
0	0	GENERATES	0	0	0	1

Port That Loses Has Its $\overline{DEN}$ = 1
$\overline{DDIR}$ = 0

*$\overline{DDIR}$ Is Defined as 0 = Data Direction Is Into Single Port RAM
1 = Data Direction Is Out of Single Port RAM

Table 2. Register Banks

LEFT PORT REGISTER BANK	RIGHT PORT REGISTER BANK
CONTROL REG. STATUS REG. MESSAGE IN REG. MESSAGE OUT REG.	CONTROL REG. STATUS REG. MESSAGE IN REG. MESSAGE OUT REG.

The left port's message out register becomes the right port's message in register.

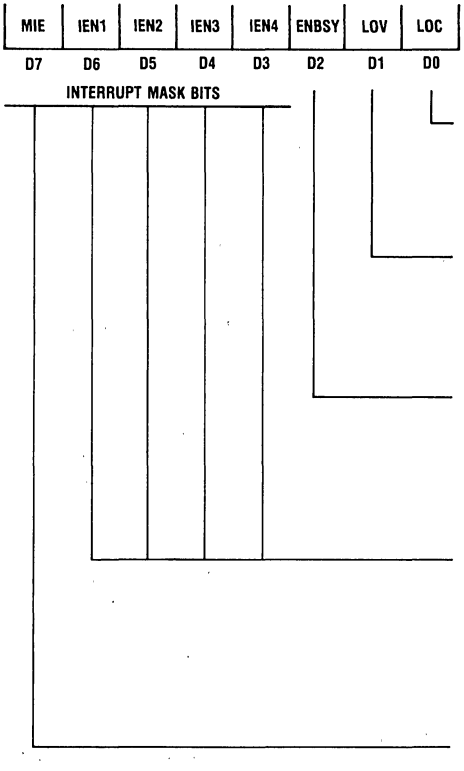
The right port's message out register becomes the left port's message in register.

Table 3. Left/Right Port Register Bank (Access)

CONTROL SIGNALS				REGISTER NAME	ABBREVIATED NAME
A1	A0	$\overline{CSC}$	$R/\overline{W}$	D_7–D_0	
0	0	0	I/O	CONTROL REGISTER	CR0
0	1	0	I/O*	STATUS REGISTER	CR1
1	0	0	I	MESSAGE IN REGISTER	CR2
1	1	0	I/O	MESSAGE OUT REGISTER	CR3

*ONLY BITS D_2–D_0 CAN BE WRITTEN TO.

Figure 2. Left/Right Port Control Register (CR0)
(If Current Port = Left/Right, Then Opposite Port = Right/Left)



LOCK OUT
1 = CURRENT PORT TO LOCK OUT OPPOSITE PORT FROM DUAL PORT MEMORY ACCESS
0 = DON'T LOCK OUT OPPOSITE PORT

LOCK OVERRIDE
1 = RELEASE LOCK OUT OF CURRENT PORT IF IT IS LOCKED OUT BY OPPOSITE PORT
0 = DON'T OVERRIDE LOCK

ENABLE BUSY PIN
1 = ENABLE $\overline{BUSY}$ PIN ON $\overline{CSR}$ OF CURRENT PORT, IF IT IS LOCKED OUT
0 = DISABLE $\overline{BUSY}$ ON $\overline{CSR}$ OF CURRENT PORT IF IT IS LOCKED OUT

INTERRUPT ENABLE BITS

1 = ENABLE CORRESPONDING INTERRUPT STATUS BIT
0 = DISABLE CORRESPONDING INTERRUPT STATUS BIT

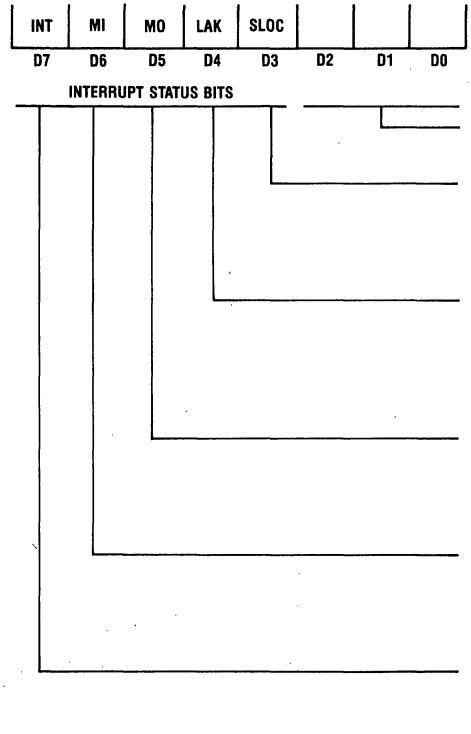
IEN1–IEN4—ENABLE BITS FOR CORRESPONDING INTERRUPT STATUS BITS (MO, MI, LAK, SLOC) OF STATUS REGISTER.

MASTER INTERRUPT ENABLE

1 = ENABLE MASTER INTERRUPT
0 = DISABLE MASTER INTERRUPT

MIE—ENABLE BIT FOR MASTER INTERRUPT (INT) OF STATUS REGISTER.

Figure 3. Left/Right Port Status Register (CR1)
(If Current Port = Left/Right, Then Opposite Port = Right/Left)



GENERAL BITS FOR USER (READ AND WRITE)

SOFTWARE LOCK
1 = CURRENT PORT HAS BEEN LOCKED OUT BY OPPOSITE PORT
0 = CURRENT PORT IS NO LONGER LOCKED OUT BY OPPOSITE PORT

LOCK ACKNOWLEDGE*
1 = OPPOSITE PORT HAS BEEN LOCKED OUT BY CURRENT PORT SETTING LOC(D0)(CR0) BIT
0 = OPPOSITE PORT HAS NOT BEEN LOCKED OUT BY CURRENT PORT SETTING LOC(D0)(CR0) BIT

MESSAGE OUT
1 = CURRENT PORTS MESSAGE OUT REGISTER HAS BEEN READ BY OPPOSITE PORT
0 = CURRENT PORTS MESSAGE OUT REGISTER HAS NOT BEEN READ BY OPPOSITE PORT

MESSAGE IN
1 = OPPOSITE PORT HAS WRITTEN INTO CURRENT PORTS MESSAGE-IN REGISTER
0 = CURRENT PORT HAS READ ITS MESSAGE IN REGISTER.

MASTER INTERRUPT**
1 = $\overline{INT}$ PIN GOES LOW
0 = $\overline{INT}$ PIN GOES HI

*LAK (LOCK ACKNOWLEDGE) (D4)(CR1) OF THE CURRENT PORT IS SET, ONLY AFTER THE *LOC(D0)(CR0) OF THE CURRENT PORT IS SET AND LOC(D0)(CR0) OF THE OPPOSITE PORT HAS NOT BEEN SET.

**INT(D7)(CR1) IS THE CURRENT PORT'S MASTER INTERRUPT.

$\overline{INT}$(PIN) = INT • MIE

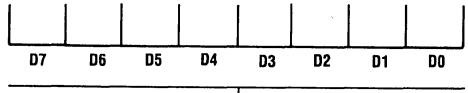
WERE INT = (MI • IEN1) + (MO • IEN2) + (LAK • IEN3) + (SLOC • IEN4)

INT IS GENERATED ON THE ↓ OF ANY OF THE INTERRUPT SOURCES IF THEY ARE ENABLED.

THE MASTER INTERRUPT (INT), IS CLEARED BY READING THE STATUS REGISTER, WHILE EACH INTERRUPT STATUS BIT (MI, MO, LAK, SLOC) IS CLEARED BY THE APPROPRIATE ACTION. THE INTERRUPT STATUS BITS (MI, MO, LAK AND SLOC) CAN ALWAYS BE READ AS TO THEIR STATUS.

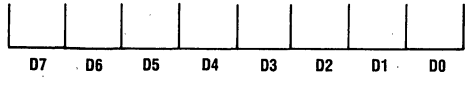
NOTE: THE CONTROL REGISTER (CR0) LEFT AND (CR0) RIGHT ARE ARBITRATED AGAINST EACH OTHER TO PREVENT MUTUAL SIMULTANEOUS LOCK-OUT. THEIR ACCESS IS MUTUALLY EXCLUSIVE. THE STATUS REGISTER (CR1) LEFT AND (CR1) RIGHT ARE ALSO ARBITRATED TO ENSURE NO LOOSE OF INTERRUPT SETTING.

Figure 4. Left/Right Port Message In Register (CR2)
(If Current Port = Left/Right, Then Opposite Port = Right/Left)



MESSAGE-IN REGISTER
ANY 8 BIT BYTE WRITTEN TO THE OPPOSITE PORTS MESSAGE-OUT REGISTER WILL GO TO THE CURRENT PORTS MESSAGE-IN REGISTER.

Figure 5. Left/Right Port Message Out Register (CR3)
(If Current Port = Left/Right, Then Opposite Port = Right/Left)



MESSAGE-OUT REGISTER
ANY 8 BIT BYTE WRITTEN TO THE CURRENT PORT'S MESSAGE-OUT REGISTER WILL GO TO THE OPPOSITE PORT'S MESSAGE-IN REGISTER.

B) Control and Status Register Detailed Description
The following is a detailed description of the control and status registers. This description applies to the left or right port (see figures 3–5 as references). This description is for a control/status register of the same port.

Control Register Bit Description (D7–D0) of (CR0)

(If current port = left/right, then opposite port = right/left)

MIE(D7)(CR0) = Master INT Enable
When set to 1, this enables the master interrupt INT(D7)(CR1) of the status register. If INT(D7)(CR1) goes to 1, then $\overline{INT}$ pin will go low. When set to 0, this will disable the master interrupt INT(D7)(CR1) of the status register. If INT(D7)(CR1) goes to 1, the $\overline{INT}$ pin will not go low.

IEN1–4(D6–D3)(CR0) = Interrupt Enable Bits 1–4
Each bit is an interrupt enable bit for the corresponding interrupt status bit in the status register. When set to 1, they enable the corresponding bit in the status register to form the master interrupt.

$\overline{INT}$ PIN = (INT • MIE)
were INT = (MI • IEN1) + (MO • IEN2) +
(LAK • IEN3) + (SLOC • IEN4)
were INT, MI, MO, LAK, SLOC = D7–D3 (CR1) of the status register.
and MIE, IEN1, IEN2, IEN3, IEN4, = D7–D3 (CR0) of the control register.

ENBSY(D2)(CR0) = Enable Busy
When set to 1 on the current port, this enables the $\overline{BUSY}$ pin for the current port, to be activated by the current ports $\overline{CSR}$ pin, if that port has been locked out by the opposite port. This allows the locked out port to have a hardware $\overline{BUSY}$ pin status for the locked condition, if it trys to access the Dual Port Memory with its $\overline{CSR}$ pin. When ENBSY bit of the current port is set, $\overline{BUSY}$ pin of the current port will follow the current ports $\overline{CSR}$ pin in logic sense if the current port has been locked out by the opposite port.

LOV(D1)(CR0) = Lock Override
This bit is enabled to be set on the current port only when the current port has been locked out by the opposite port and the current ports SLOC bit has gone to 1. Only at that time, can the user set the LOV(D1)(CR0) bit. When set, this bit will unlock the current port and then the current ports SLOC bit will go low. When this happens LOV(D1)(CR0) will automatically be cleared and disabled. In this way, neither port can permanently unlock his port.

The user should always check his SLOC(D3)(CR1) bit to make sure that he is unlocked before trying to access the dual port memory again.

LOC(D0)(CR0) = Lock Out
When set to 1 on the current port, the opposite port will be locked out from dual port memory accesses if the current port's SLOC(D3)(CR1) bit was not previously set. If the current port's SLOC(D3)(CR1) bit was set, this would mean the current port was already locked out. In this case, the LOC bit of the current port will be set, but will not take effect until either the current port clears its locked out condition by using its LOV(D1)(CR0) bit or the opposite port clears its LOC(D0)(CR0) bit. It is important to note that the control register, as well as status register of both register banks, are arbitrated against each other, to prevent simultaneous access. This guarantees that there is never a case of mutual lock out by both ports simultaneously setting their respective LOC(D0)(CR0) bits.

Status Register Bit Description (D7–D0) of (CR1)

(If current port = left/right, then opposite port = right/left).

INT(D7)(CR1) = Master Interrupt
This bit is set by the leading edge of any of the status bit flags (IM, MO, LAK, SLOC) of the same port. As explained before, these bits are enabled by IEN1–4 of the same ports control register (see IEN1–4(D6–D3)(CR0) of control register).

MI(D6)(CR1) = Message-In
When set to one, this flag indicates that the opposite port has written a message into its message-out register and is ready to be read on the current port's message-in register. When the current port reads its message in register, this flag bit is cleared.

MO(D5)(CR1) = Message Out
When set to 1, this flag indicates that the opposite port has read its message-in register and the current port is clear to write new data into its message-out register. When the current port writes new data to its message-out register, then this flag bit is cleared.

LAK(D4)(CR1) = Lock Acknowledge
This is an acknowledgment flag bit that tells the current port that it has successfully locked out the opposite port from dual port memory access. This occurs when the current port sets its LOC(D0)(CR) bit. If the opposite port has not already set its own LOC bit, then the current port will lock out the opposite port and then the current ports LAK flag bit will be set.

SLOC(D3)(CR1) = Software Lock
This is a software status flag that indicates that the current port has been locked out of dual port memory access by the opposite port. When set to 1, in the current port, the opposite port has set its LOC(D0)(CR0) bit and the opposite ports LAK(D4)(CR1) flag bit has in turn been set, indicating the opposite port has locked out the current port. It is cleared when either the opposite port clears its LOC(D0)(CR0) bit, or the current port sets its lock override bit LOV(D1)(CR0) to override the lock.

Setting/Clearing Status Flags
The master interrupt (INT) bit is a combination of MO, MI, LAK, or SLOC bits of the status register, depending on which of these bits is enabled by their corresponding interrupt enable bits of the control register (IEN 1–4 respectively).

The master interrupt (INT) bit is cleared on any subsequent reading of the status register. The individual interrupt status bits (MO, MI, LAK, SLOC) are cleared in the following way:

1) MO, MI —are cleared in the status register by subsequent reads or writes to the same ports message in and message out registers.

2) LAK —is cleared by the opposite port overriding its lockout, or the current port clearing its LOC bit.

3) SLOC —is cleared by the current port overriding its lockout by using the lock override bit LOV, or by the opposite port clearing its LOC bit.

C. Reset
On reset, the following bits are set in the Left/Right Port Register Bank:

(D7–D0)(CR0)—Control register	=	0000000
(D7–D0)(CR1)—Status register	=	0010000
(D7–D0)(CR2)—Message-in register	=	0000000
(D7–D0)(CR3)—Message-out register	=	0000000

D. Mode
The mode pin is a special pin that is used to switch the S61C35 from a master device to a slave device. When set to one, the S61C35 is a master device and operates as previously described in the datasheet. In certain cases where the user needs more than one controller, he can combine several S61C35s together. In this case, one controller can be the master mode in that all contention arbitration and register banks will be in the master and only the master will output the $\overline{\text{BUSY}}$ pin. The other S61C35s can be in a slave mode in which their $\overline{\text{BUSY}}$ pins become inputs which would be tied to the master's $\overline{\text{BUSY}}$ output. This makes the slave control signals dependent on the $\overline{\text{BUSY}}$ of the master. When an S61C35 is in the slave mode, its contention arbitration and register banks are turned off to allow only one master device. It should be noted that using the S61C35 in a slave mode will effectively double the overall access time of the system due to the added propagation delay from the master BUSY output to the slave $\overline{\text{BUSY}}$ input and subsequent enabling and generation of control signals. This can be reduced however with careful system design considerations.

Design Precautions
The user has the flexibility of reading his own status register by a polling method or interrupt method. If the user uses the polled method for an indication of lockout, he should be aware that if he does not have his ENBSY(D2)(CR0) bit on, and is not locked out, he could begin to write to the Dual Port Memory System, and if at that exact same time, he does become locked out, he could complete his write cycle with no $\overline{\text{BUSY}}$ to him. As a result, he would perform a write to the dual port memory and never know that it never was accomplished. This can never happen if his lock was interrupt driven.

Other such potential problems could exist and it is the designer's responsibility to realize these and understand how he wants to program the device.

Absolute Maximum Ratings

DC Supply Voltage (V_{DD} – V_{SS})	+7V
Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
Digital Input	V_{SS} – 0.3V ≤ V_{IN} ≤ V_{DD} + 0.3V

D.C. Electrical Operating Characteristics: T_A = 0°C to +70°C; V_{DD} = +5V (±10%); V_{SS} = 0V unless otherwise specified

Symbol	Parameter/Conditions	Minimum	Typical	Maximum	Units
V_{IH}	High Level Logic Input	2.0		V_{DD}	V
V_{IL}	Low Level Logic Input	V_{SS}		+0.8	V
V_{OH}	High Level Logic Outputs I_{OH} = .8mA	2.4		V_{DD}	V
V_{OL}	Low Level Logic Outputs I_{OL} = 4.0mA	0		+0.4	V
P_D	Power Dissipation @ ±5.5V		150		mW

AC Electrical Characteristics (V_{CC} = 5V ±10%, all temperature ranges)

No	Parameter Symbol	Parameter Description	Test Condition (Note)	S61C35			Units
				Min	Typ	Max	
BUSY Timing							
①	t_{CS}	Chip select RAM (CSR) cycle time			100		ns
②	t_{BAC}	$\overline{BUSY}$ access time from chip select RAM	(7,6)	15	25	55	ns
③	t_{BR}	$\overline{BUSY}$, control signals release time	(7,6)	5	10	20	ns
④	t_{APS}	Arbitration priority set-up time			5	10	ns
⑤	t_{BFAC}	Buffer controls access time from chip select RAM	(7,6)	10	25	55	ns
⑥	t_{RAC}	RAM controls access time from chip select RAM	(7,6)	10	25	55	ns
⑦	t_{SBFAC}	Buffer controls access time from $\overline{BUSY}$ (slave mode)	(8,6)	5	15	25	ns
⑧	t_{SRAC}	RAM controls access time from $\overline{BUSY}$ (slave mode)	(8,6)	5	15	25	ns
Read Cycle							
⑨	t_{RC}	Read cycle time			100		ns
⑩	t_{AA}	Address access time		20	45	80	ns
⑪	t_{RS}	Read set up time		0	0		ns
⑫	t_{RAC}	Read access	(12)	5	10		ns
⑬	t_{CSAC}	Chip select access time		20	45	80	ns
⑭	t_{HZ}	Output low z time		8	15	30	ns

AC Electrical Characteristics (Continued)

No	Parameter Symbol	Parameter Description	Test Condition (Note)	S61C35 Min	S61C35 Typ	S61C35 Max	Units
Write Cycle							
⑮	t_{WC}	Write access time			100		ns
⑯	t_{CW}	Chip select to end of write			100		ns
⑰	t_{AS}	Address setup time		0	0		ns
⑱	t_{WP}	Write pulse width		50			ns
⑲	t_{WR}	Write recovery time		0	0		ns
⑳	t_{DS}	Data setup to write		10			ns
㉑	t_{DH}	Data hold after write		10			ns
㉒	t_{WZ}	Write enable to data output z		10			ns
㉓	t_{OW}	Output active from end of write		10			ns
Interrupt Timing							
㉔	t_{WINS}	Write to int set		15	30	60	ns
㉕	t_{CSINS}	CS to int set		15	30	60	ns
㉖	t_{CSINR}	CS to int reset		5	10	20	ns

Notes
(1) Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient
(2) Below min. time, $\overline{CSR}_L$ is guaranteed to win arbitration at typical limits(1). For V_{DD} and temperature limits at max. or min., $\overline{CSR}_L$ is not guaranteed to win, but proper arbitration will occur with either $\overline{CSR}_L$ or $\overline{CSR}_R$ winning.
(3) Address valid prior or coincident with $\overline{CSC}_{L/R}$ transition.
(4) $R/\overline{W}_{L/R}$ is Hi for read cycle.
(5) $\overline{CSC}_{L/R}$ is Low for read cycle.
(6) Assumes $\overline{UD}_{L/R}$, $\overline{LD}_{L/R}$, $R/\overline{W}_{L/R}$ are valid prior to or coincident to $\overline{CSR}_{L/R}$. If this is not the case, add extra delay time to control signal delay from $\overline{CSR}_{L/R}$.
(7) Mode = Hi
(8) Mode = Low
(9) Register bank access of control, message-in or message-out.
(10) Register bank access of status register to clear $\overline{INT}_{L/R}$.
(11) Transition from Low to Hi of $\overline{CSC}_{L/R}$ or $R/\overline{W}_{L/R}$ causes $\overline{INT}_{L/R}$.
(12) When accessing non-arbitrated, message-in/out registers, t_{RAC} is taken from $R/\overline{W}$. When accessing arbitrated registers, control and status, if t_{RS} is > 35ns (typical) then t_{RAC} is as given. If t_{RS} < 35ns, then t_{RAC} is not valid as given but will follow t_{CSAC}, timing.

Figure 6. $\overline{CSR}_{L/R}$ to $\overline{BUSY}_{R/L}$ (Left/Right Port—Not Locked Out)

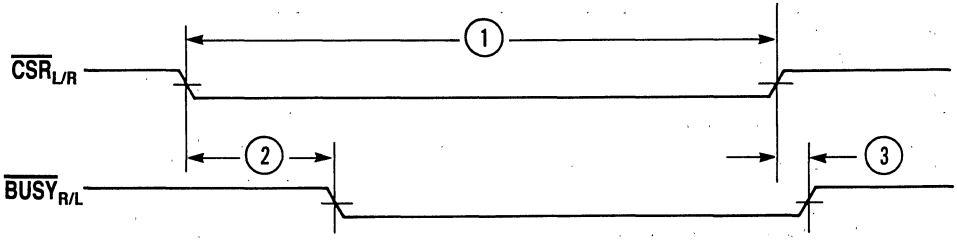


Figure 7. $\overline{CSR}_{L/R}$ to $\overline{BUSY}_{R/L}$ (Left/Right Port—Locked Out)

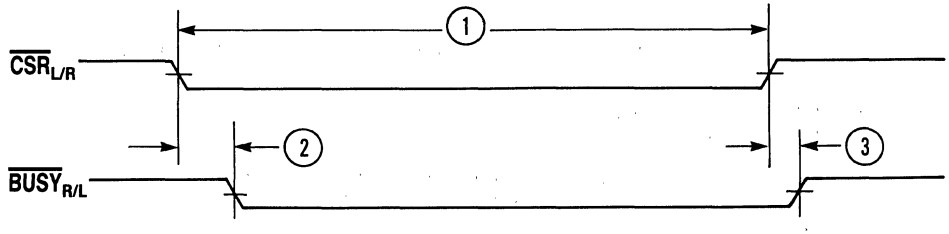


Figure 8. $\overline{CSR}_{L/R}$ Contention Arbitration ($\overline{CSR}_L$ Valid First)

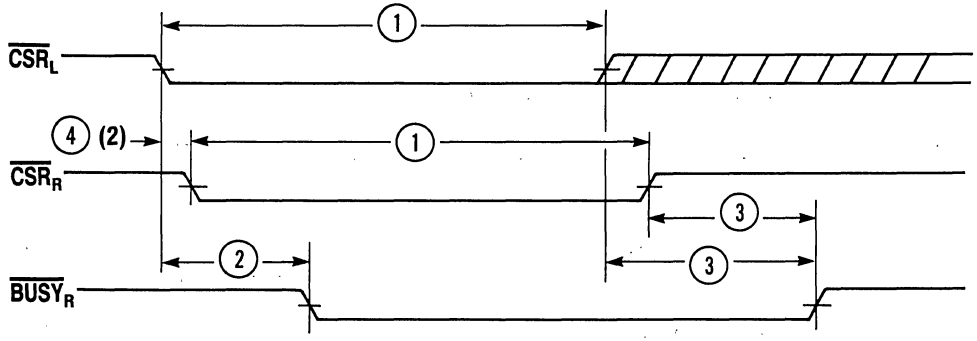


Figure 9. $\overline{CSR}_{L/R}$ Contention Arbitration ($\overline{CSR}_R$ Valid First)

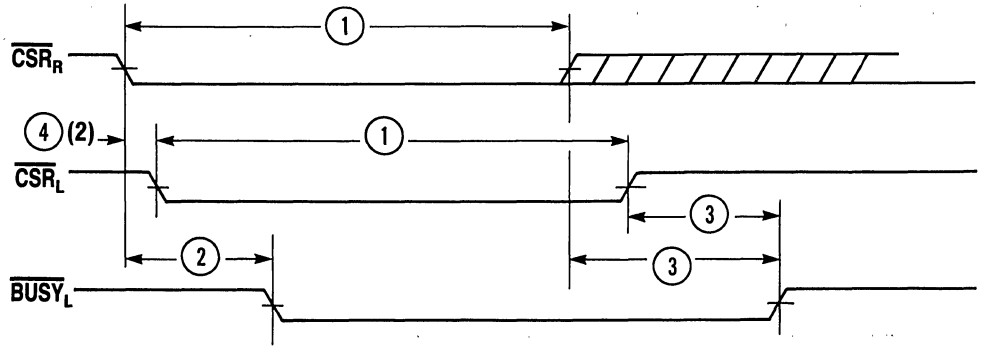


Figure 10. $BUSY_{L/R}$ to Control Signals Valid (Left/Right Port) of Winning Port from Contention Arbitration (Master Mode)(7)

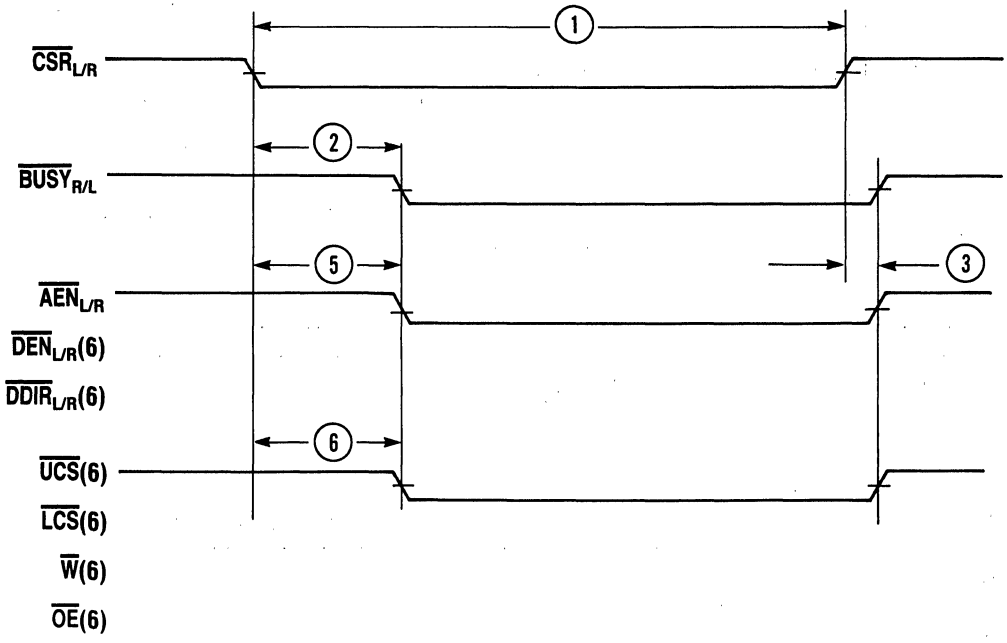


Figure 11. $\overline{BUSY}_{L/R}$ to Control Signals Valid (Left/Right Port) of Winning Port from Contention Arbitration (Slave Mode)(8)

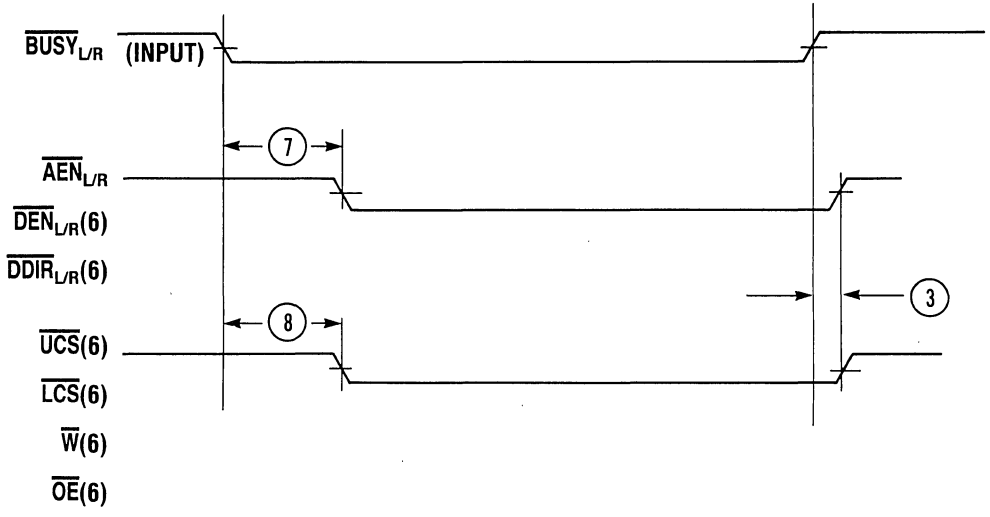


Figure 12. Register Bank (Left/Right Port) (Read Cycle)(4,5)

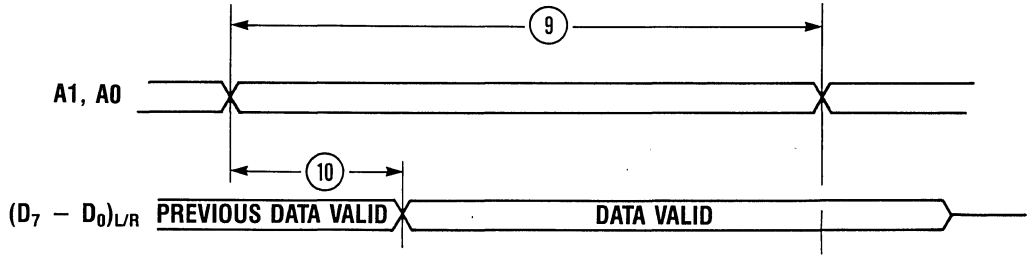


Figure 13. Register Bank (Left/Right Port) (Read Cycle)(3,4)

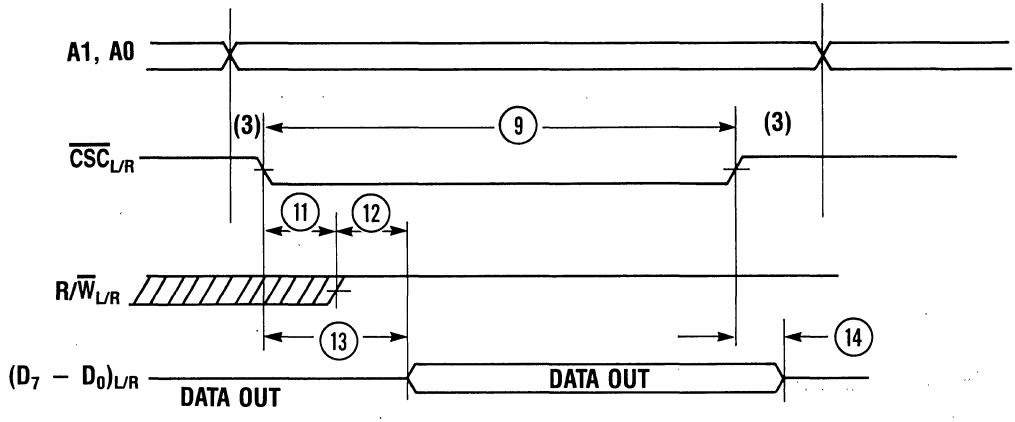


Figure 14. Register Bank (Left/Right Port) (Write Cycle)(3) ($\overline{W}$ Controlled)

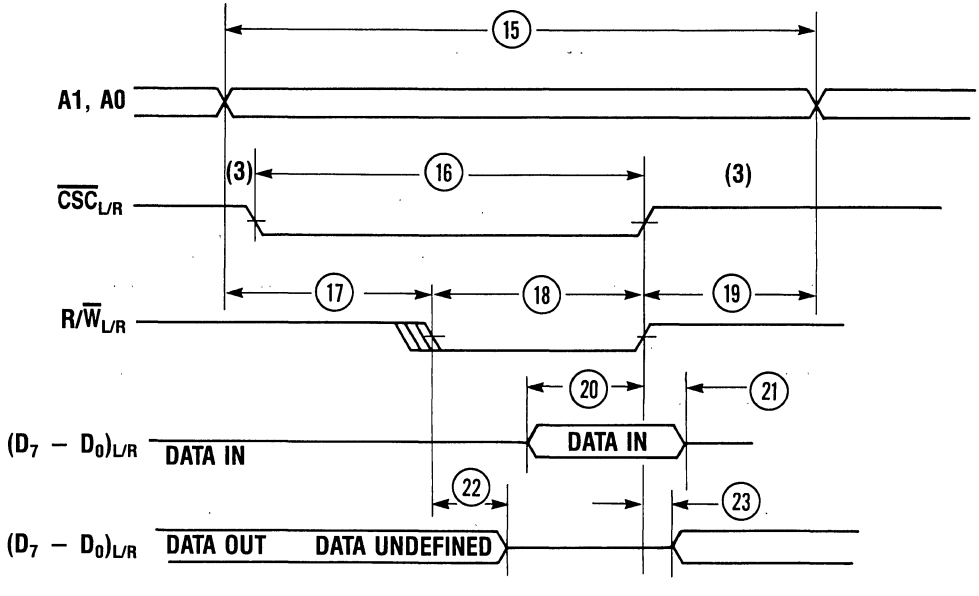


Figure 15. Register Bank (Left/Right Port) (Write Cycle)(3) ($\overline{CSC}_{L/R}$ Controlled)

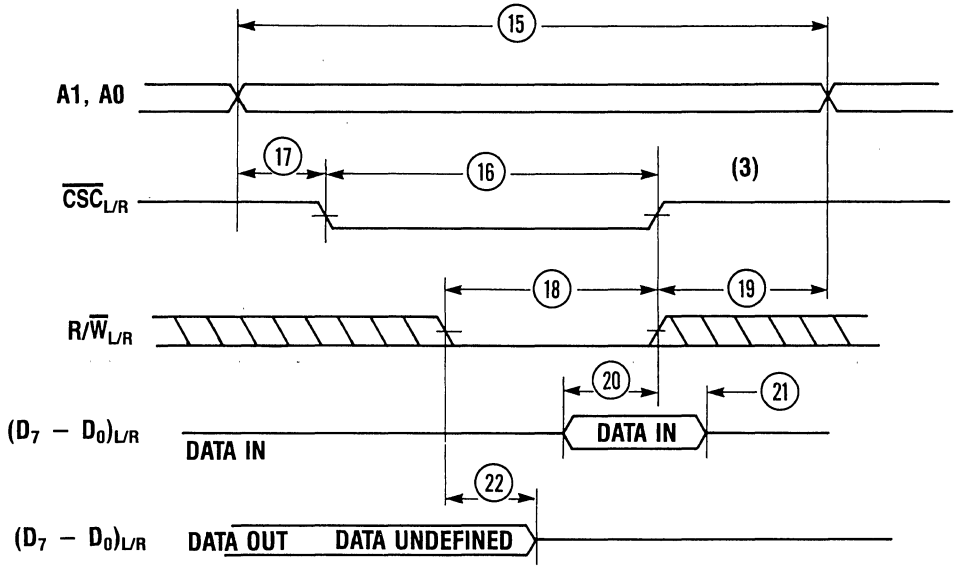


Figure 16. Interrupt Timing (Interrupt Setting)(9)(11)

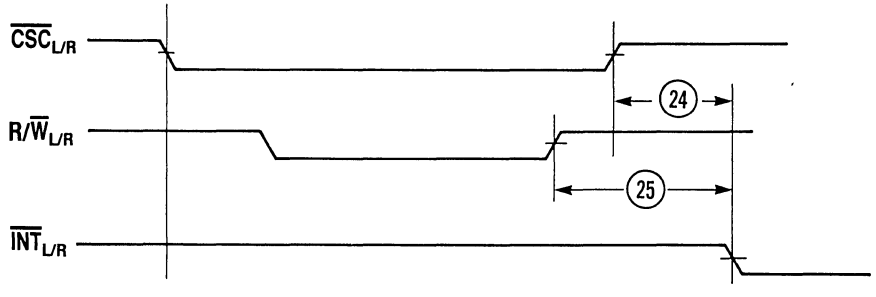
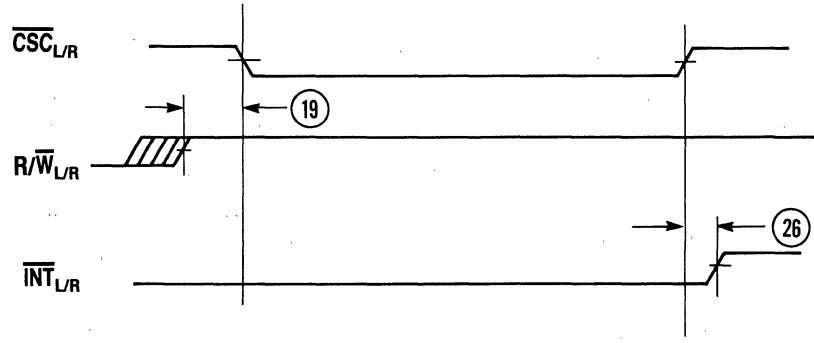


Figure 17. Interrupt Timing (Interrupt Clearing)(10)



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16-Bit Bounds Checker

Preliminary Data Sheet

S61C337

COMMUNI-CATION PRODUCTS

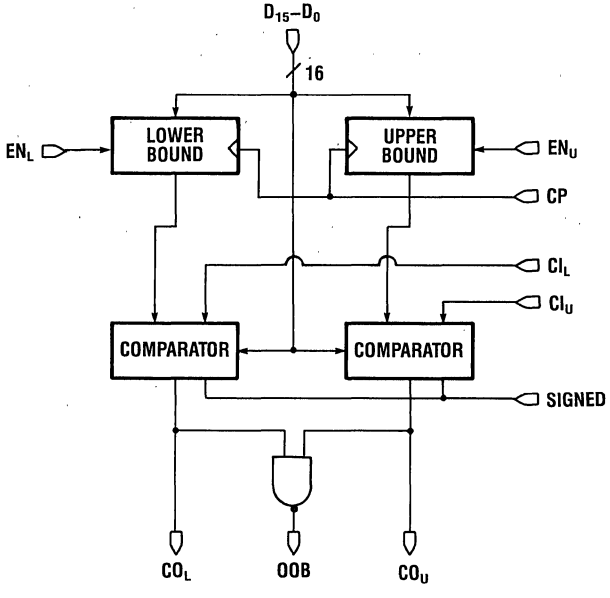
Features

- Applications include;
  - —Arithmetic underflow/overflow checking
  - —Virtual memory to real memory address boundary comparisons
- Double Comparator
  - —Compares a 16-bit input number with a lower limit and an upper limit
- Cascadable
  - —16-bit cascadable to longer words
- Out-of-Bounds Flag
  - —Flags values that are outside the bounds of a lower and an upper limit
- Compares Signed or Unsigned Numbers
- 28-Pin Plastic Dip Package
- CMOS

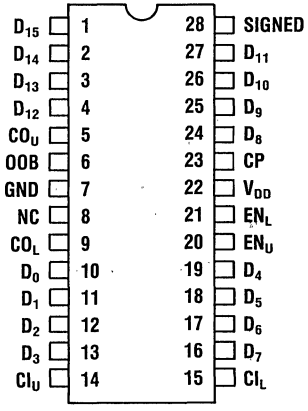
General Description

The S61C337 is a 16-bit bounds checker, which can compare a 16-bit signed or unsigned number with a lower and an upper bound limit stored in registers. The device can flag values that are out of bounds, as well as inbounds. The device is also cascadable up to 32-bits or greater.

Block Diagram



Pin Configuration



S61C337

Pin Name	I/O	Pin Function
D_{15}–D_0	I	Input to limit registers and comparators.
EN_L, EN_U	I	Load enable signals for the limit registers.
CP	I	Clock pulse to load limit registers when enabled. (Low-to-High transition)
CI_L, CI_U	I	Carry input signals for cascading.
CO_L, CO_U	O	Carry output signals from results of comparisons.
OOB	O	Out-of-bounds signal to flag values that are out of *bounds*. Defined as $(\overline{CO_L \cdot CO_U})$.
SIGNED	I	Hi—selects signed comparisons. Low—selects unsigned comparisons.
NC	—	No connect
GND	—	Ground
V_{DD}	—	Power, +5V

Detailed Description

The S61C337 is a high speed CMOS bounds checker that can determine if a signed or unsigned 16-bit number lies within a lower and upper limit. The device can easily be cascaded for larger words.

Limit Registers and Comparators

The S61C333 has an upper limit and lower limit registers. These registers are loaded from the D_{15}–D_0 bus with the load enable inputs EN_U, EN_L and clock pulse CP, rising edge. The values then presented to the D_{15}–D_0 data bus are compared with the values stored in the limit registers through comparators. The comparators can operate on either signed or unsigned numbers depending on the SIGNED signal input (Hi = signed, Low = unsigned). The results of the comparison are given in the outputs CO_U C_L, and OOB. The definitions of carry inputs CI_U and CI_L are given in Table-1 and the combination of the different regions Table-2. If data being compared is out of the region, the out-of-bounds flag OOB, is set which is defined as $(CO_U \cdot CO_L)$.

Cascading

Comparison of numbers longer than 16-bits requires cascading of two or more bounds—checker slices. (See Fig.-1) The comparison starts from the least significant slice (LSS) with CI_U, CI_L of the LSS acting as inputs to the overall bounds checker. The CO_U, CO_L of the LSS slice act as inputs to the most significant slice (MSS) inputs CI_U, CI_L. The MSS outputs CO_U, CO_I and OOB, act as the outputs of the overall bounds checker. The SIGNED input of the MSS identifies the value when being compared with either signed or unsigned numbers when the SIGNED input of the LSS is tied low.

The comparison can also start from the MSS. In this case, CO_U, CO_L, OOB of the LSS act as outputs of the overall bounds checker, while CO_U, CO_L of the MSS are connected to CI_U, CI_L of the LSS.

Table 1. Definition of CO_L and CO_U

Inputs		Outputs	
CI_L	CI_U	CO_L	CO_U
0	0	$L < D$	$D < U$
0	1	$L < D$	$D \leq U$
1	0	$L \leq D$	$D < U$
1	1	$L \leq D$	$D \leq U$

Note:
D = Data Input
L = Lower Unit
U = Upper Unit

Table 2. Different Combinations of Regions

Inputs		Outputs			Description
CI_L	CI_U	CO_L	CO_U	OOB	
0	0	0	0	1	Impossible Combination
		0	1	1	$D \leq L$
		1	0	1	$U \leq D$
		1	1	0	$L < D < U$
0	1	0	0	1	Impossible Combination
		0	1	1	$D \leq L$
		1	0	1	$U < D$
		1	1	0	$L < D \leq U$
1	0	0	0	1	Impossible Combination
		0	1	1	$D < L$
		1	0	1	$U \leq D$
		1	1	0	$L \leq D < U$
1	1	0	0	1	Impossible Combination
		0	1	1	$D < L$
		1	0	1	$U < D$
		1	1	0	$L \leq D \leq U$

Note:
D = Data Input
L = Lower Unit
U = Upper Unit

Logic Symbol

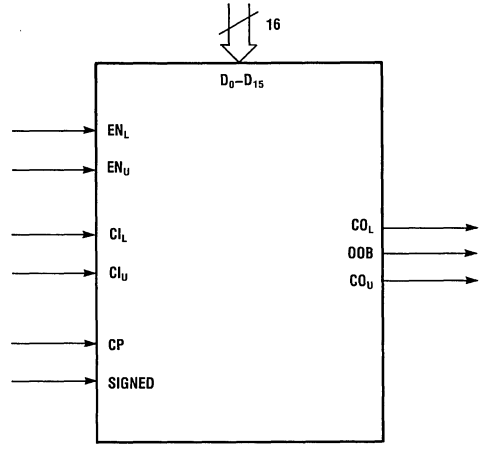
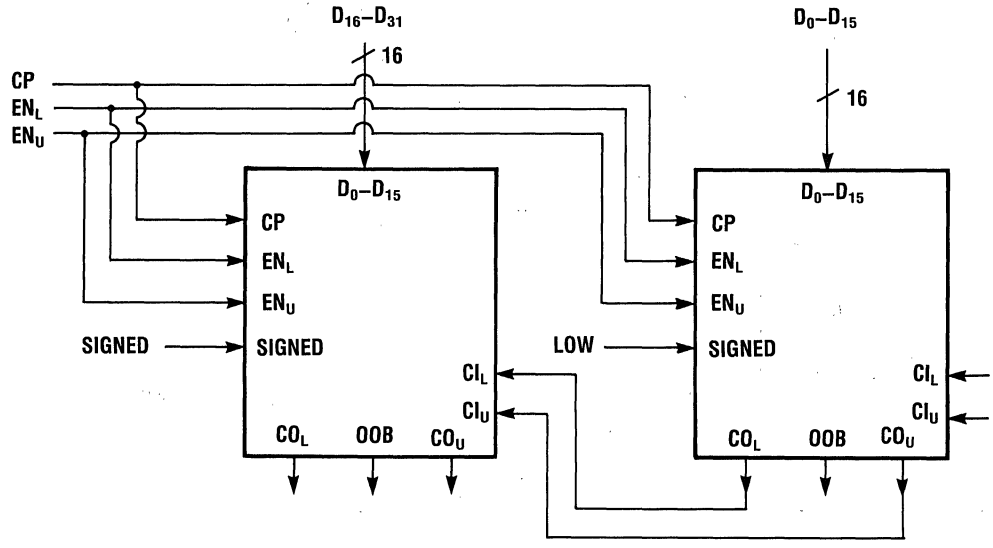


Figure 1. 32-Bit Bounds Checker



Absolute Maximum Ratings

DC Supply Voltage (V_{DD} – V_{SS}) ..... +7V
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −55°C to +150°C
Digital Input ..... V_{SS} – 0.3V ≤ V_{IN} ≤ V_{DD} + 0.3V

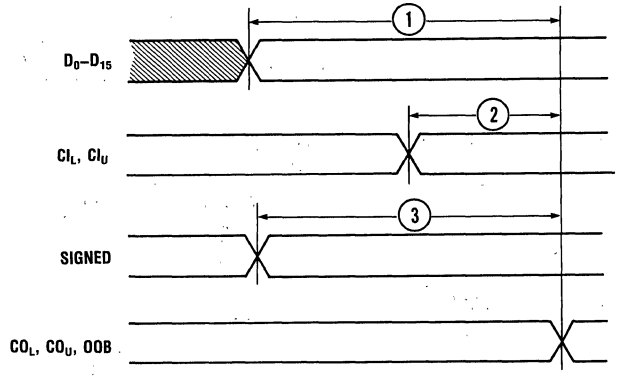
D.C. Electrical Operating Characteristics: T_A = 0°C to +70°C; V_{DD} = +5V (±10%); V_{SS} = 0V unless otherwise specified

Symbol	Parameter/Conditions	Minimum	Typical	Maximum	Units
V_{IH}	High Level Logic Input	2.0		V_{DD}	V
V_{IL}	Low Level Logic Input	V_{SS}		+0.8	V
V_{OH}	High Level Logic Outputs I_{OH} = .8mA	2.4		V_{DD}	V
V_{OL}	Low Level Logic Outputs I_{OL} = 4.0mA	0		+0.4	V
P_D	Power Dissipation @ ±5.5V		150		mW

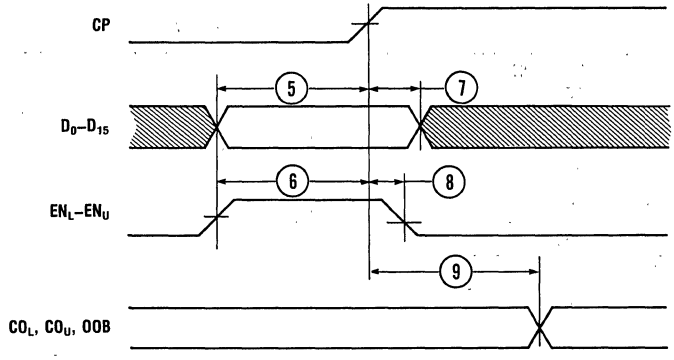
Switching Characteristics T_A = 70°C; V_{DD} = 4.5V; V_{SS} =0V

No.	Parameter Symbol		Test Conditions	Typ.	Max.	Units
1	t_{PD}	D_0–D_{15} to CO_L, CO_U, OOB		19	34	ns
2	t_{PC}	CI_L, CI_U to CO_L, CO_U, OOB		18	35	ns
3	t_{PS}	SIGNED to CO_L, CO_U, OOB		13	24	ns
4	t_{CPO}	CP to CO_L, CO_U, OOB		28	46	ns
5	t_{SD}	D_0–D_{15} Setup Time			10	ns
6	t_{SL}	EN_L, EN_U Setup Time			13	ns
7	t_{HD}	D_0–D_{15} Hold Time			2	ns
8	t_{HL}	EN_L, EN_U Hold Time			2	ns
9	t_{PWL}	Clock Pulse Width LOW		12		ns
10	t_{PWH}	Clock Pulse Width HIGH		12		ns

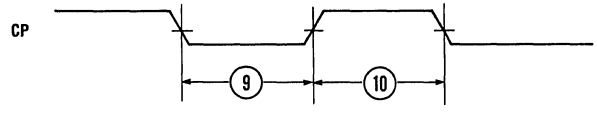
Switching Waveforms



Propagation Delays from Data Input to Output



Loading the Limit Registers



Clock Pulse

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32-Bit Shuffle/Exchange Network

Preliminary Data Sheet

S618839

COMMUNI-CATION PRODUCTS

Features

- High speed, low power HCMOS.
- High speed Data Manipulation.
- Shuffles up to 32-Bit Data Streams.
- Performs shuffle and exchange permutations on entire Data Streams or substrings for implementing algorithms and/or matrix operations.
- 3-state outputs allow 32-Bit or 16-Bit bus interface.
- Available in space saving surface mount 84 PLCC package.
- Functionally Compatible to TI 74AS8839.

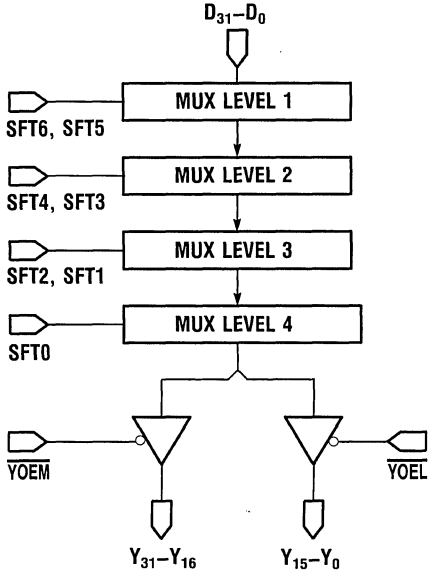
General Description

The S618839 is a 32-bit high-speed shuffle/exchange network. It is packaged in an 84-pin plastic leaded chip carrier (PLCC). The device can perform various shuffle/exchange permutations on 32-bit, 16-bit, 8-bit, or 4-bit data in a single instruction cycle by using four levels of multiplexing.

The types of permutations performed at the four levels is determined by an input decoder at each level. Data permutations are not clock dependent, and thus are dependent only on internal data propagation paths. The delay is the same regardless of the number of positions to be routed, which results in a high-speed shuffle (see Figure 1).

The shuffle/exchange network is designed for use primarily in applications such as Fast Fourier Transforms (FFT), parallel sorting, and matrix multiplication. It can also be used in varous forms of interconnection networks used in Fault-tolerant computer applications, as well as multiple processor applications. This includes single instruction multiple data (SIMD) array processors.

Block Diagram



Pin Configuration

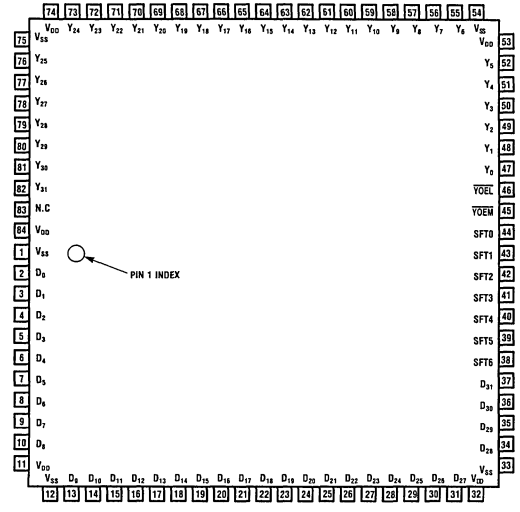
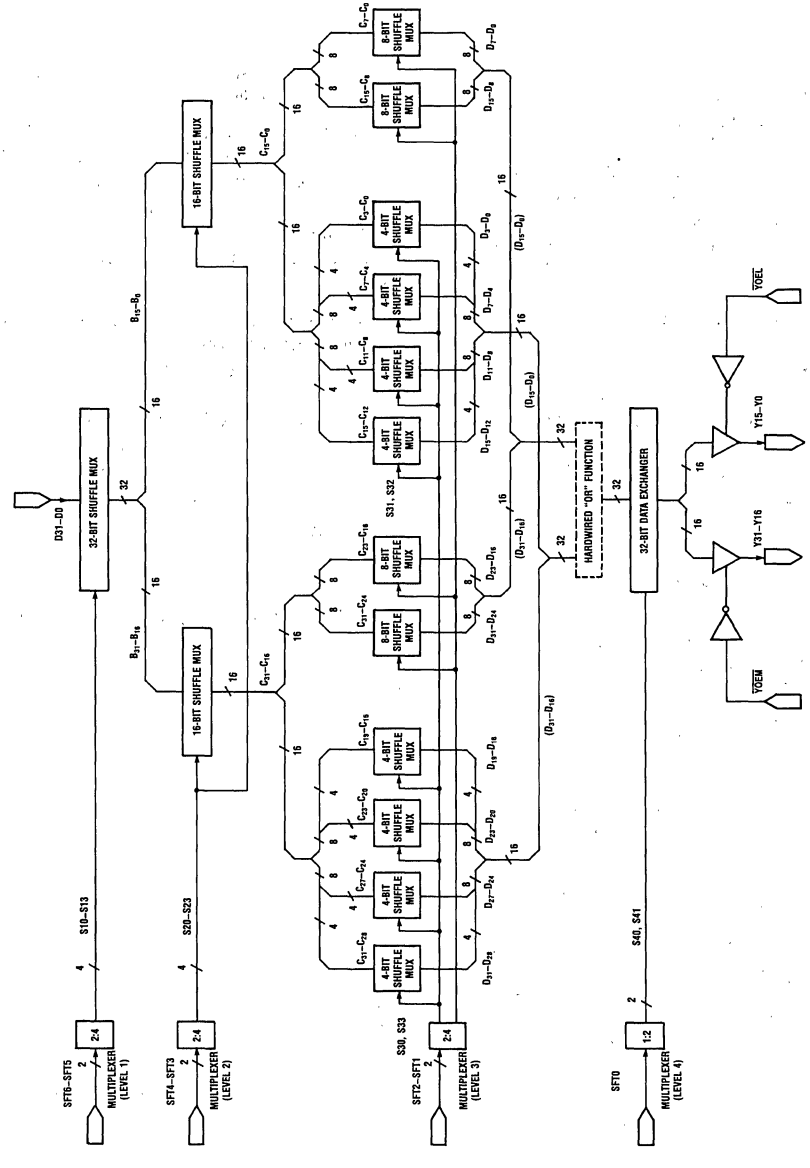


Figure 1. S618839 32-Bit Shuffle/Exchange Network



Data Permutations

The S618839 can perform five types of data permutations. These permutations can occur on one 32-bit, two 16-bit, and four 8-bit or eight 4-bit data words. These five permutations are:

1. Perfect shuffle
2. Inverse shuffle
3. Upper broadcast
4. Lower broadcast
5. Bit exchange

Examples of these permutations are found in Figure 2. Data permutations are performed by a series of multiplexers arranged in four levels:

1. A 32-bit multiplexer;
2. Two 16-bit multiplexers;
3. Four 8-bit multiplexers or eight 4-bit multiplexers;
4. One 32-bit multiplexer

Data can be shuffled in a single pass at each of the above levels or shifted at selected levels and passed through the others without alteration.

Data Flow

Data is input to the chip by the D-Port, which passes data to a 32-bit multiplexer. It is then shuffled or passed unaltered to the next level according to the control inputs SFT6–SFT5 pins. Output of the 32-bit multiplexer is input to two 16-bit multiplexers for permutation or pass operation as controlled by SFT4–SFT3 input pins. Output from this level passes to four 8-bit multiplexers or eight 4-bit multiplexers for parallel permutation operations under control of the SFT2–SFT1 input pins. Output from this level passes to a final 32-bit multiplexer where it is permuted or passed to the output pins under control of the SFT0 input pin. The result is passed out of the chip through the 32-bit Y port (see Tables 1–5).

Instruction Set

Possible modes of operation at the four levels of multiplexers are shown in Tables 1–5. All of the mode selections are controlled by seven SFT inputs, as shown in the tables.

Table 1. 32-Bit Multiplexer Operations

Multiplexer Level 1	Signal		Function	Notes
	SFT6	SFT5		
(One 32-bit word)	0	0	Pass data unaltered	
	0	1	Perfect shuffle	
	1	0	Inverse shuffle	
	1	1	Upper broadcast	
	—	—	Lower broadcast	Can be performed as lower broadcast at 16-bit multiplexer level 2 (see Table 2).

Table 2. 16-Bit Multiplexer Operations

Multiplexer Level 2	Signal		Function	Notes
	SFT4	SFT3		
(Two 16-bit words)	0	0	Pass data unaltered	
	0	1	Perfect shuffle	
	1	0	Inverse shuffle	
	—	—	Upper broadcast	Can be performed as upper broadcast at 32-bit multiplexer level 1 (see Table 1).
	1	1	Lower broadcast	

Table 3. 8-Bit Multiplexer Operations

Multiplexer Level 3	Signal		Function	Notes
	SFT2	SFT1		
	0	0	Pass data unaltered	
	0	1	Perfect shuffle	
	1	0	Inverse shuffle	
(Four 8-bit words)	—	—	Lower broadcast	Can be performed as lower broadcast at 16-bit multiplexer level 2 (see Table 2).
	—	—	Upper broadcast	Can be performed as upper broadcast at 32-bit multiplexer level 1 (see Table 1).

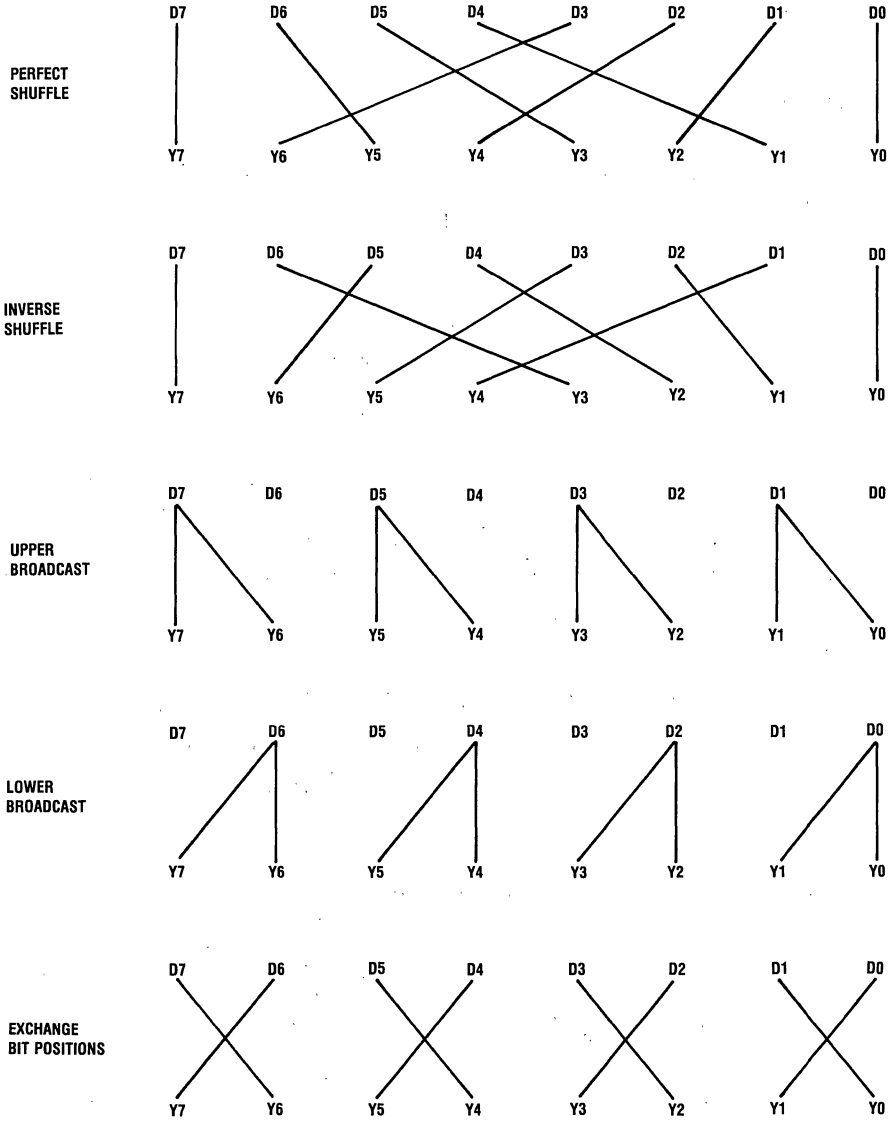
Table 4. 4-Bit Multiplexer Operations

Multiplexer Level 3	Signal		Function	Notes
	SFT2	SFT1		
	0	0	Pass data unaltered	
	1	1	Perfect shuffle	
	1	1	Inverse shuffle	
(Eight 4-bit words)	—	—	Lower broadcast	Can be performed as lower broadcast at 16-bit multiplexer level 2 (see Table 2).
	—	—	Upper broadcast	Can be performed as upper broadcast at 32-bit multiplexer level 1 (see Table 1).

Table 5. Bit Exchange Multiplexer Operations

Multiplexer Level 4	Signal SFT6	Function	Notes
(One 32-bit word)	0	Pass data unaltered	
	1	Exchange bits	

Figure 2. Permutation Types, 8-Bit String Example



Examples
Figures 3–14 exemplify the instruction set for the S618839. Figures 3–13 illustrate the data permutations possible at each multiplexer level, assuming that data is passed unaltered through the other levels. In figure 14, data is permuted at three multiplexer levels during a single pass through the chip.

Multiplexer Level 1 (figures 3–6)

Figure 3. Perform a perfect shuffle on a 32-bit word and pass the result to the Y port.

CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
0	1	0	0	0	0	0

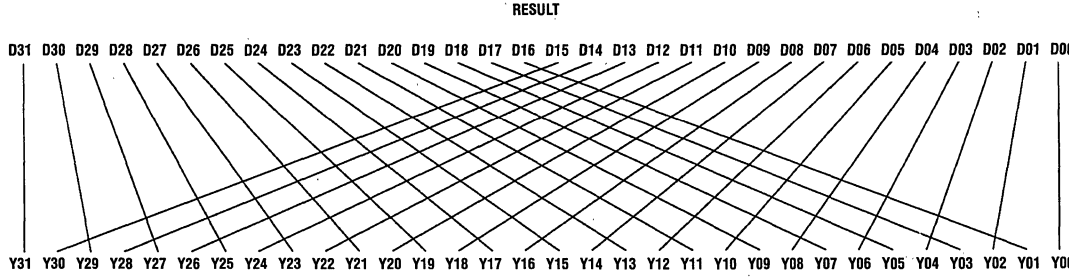


Figure 4. Perform an inverse shuffle on a 32-bit word and pass the result to the Y port.

CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
1	0	0	0	0	0	0

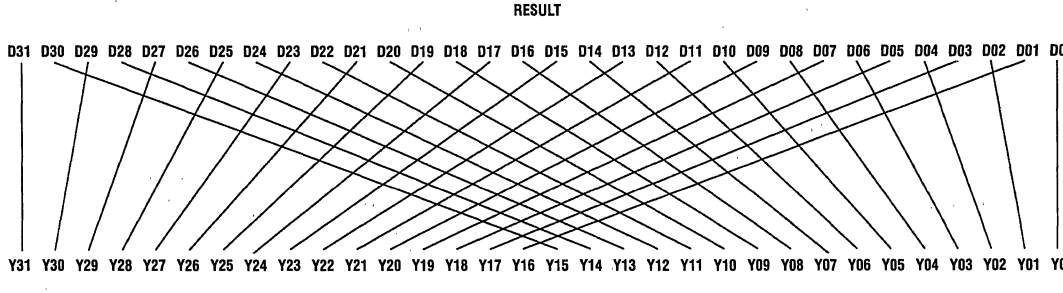


Figure 5. Perform an upper broadcast on a 32-bit word and pass the result to the Y port.

CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
1	1	0	0	0	0	0

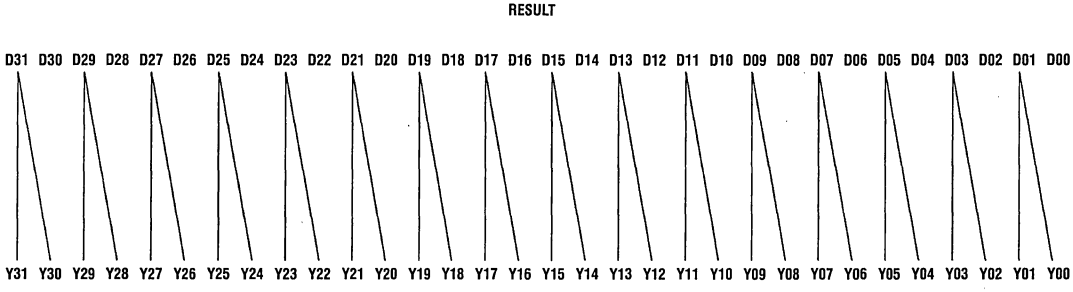
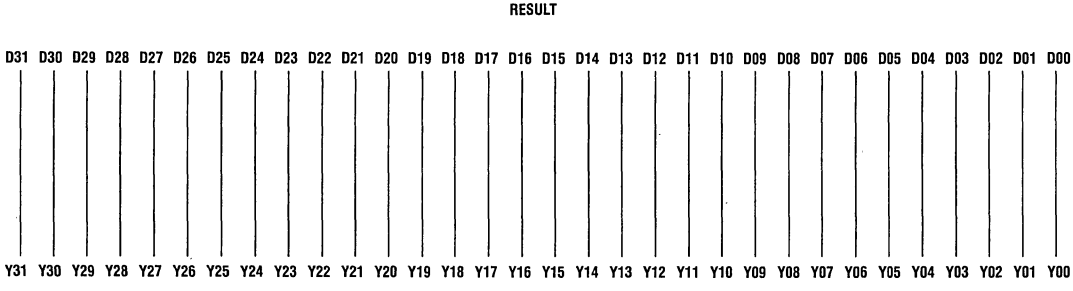


Figure 6. Pass a 32-bit word throught the 8839 without permutation.

CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
0	0	0	0	0	0	0



Multiplexer Level 2 (figures 7–9)

Figure 7. Perform a perfect shuffle on two 16-bit words and pass the result to the Y port.

CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
0	0	0	1	0	0	0

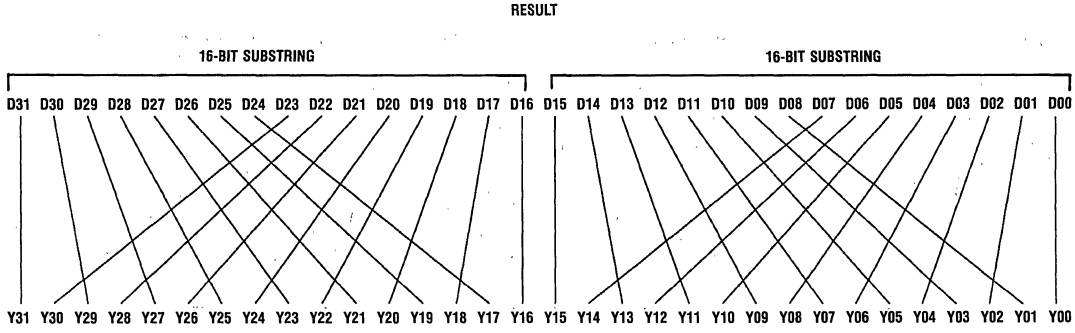


Figure 8. Perform an inverse shuffle on two 16-bit words and pass the result to the Y port.

CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
0	0	1	0	0	0	0

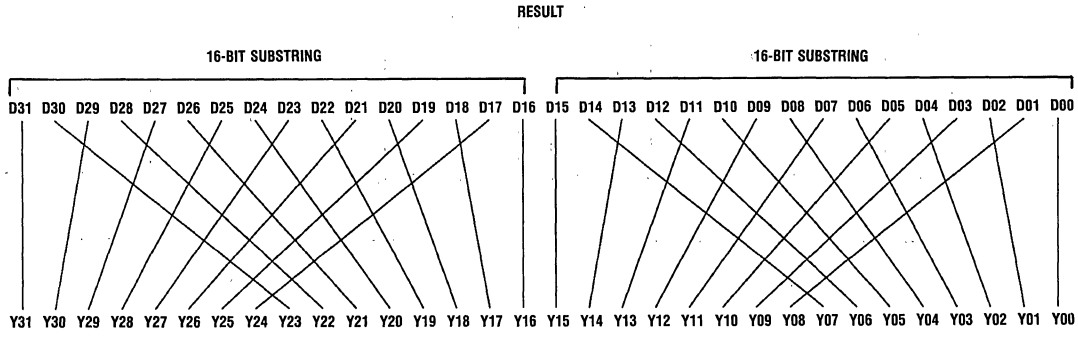
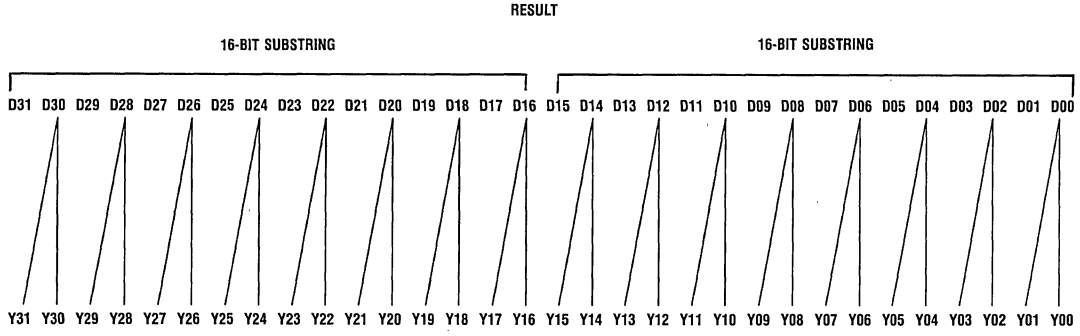


Figure 9. Perform a lower broadcast on two 16-bit words and pass the result to the Y port.

CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
0	0	1	1	0	0	0



Multiplexer Level 3 (figures 10–12)

Figure 10. Perform a perfect shuffle on four 8-bit words and pass the result to the Y port.

CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
0	0	0	0	0	1	0

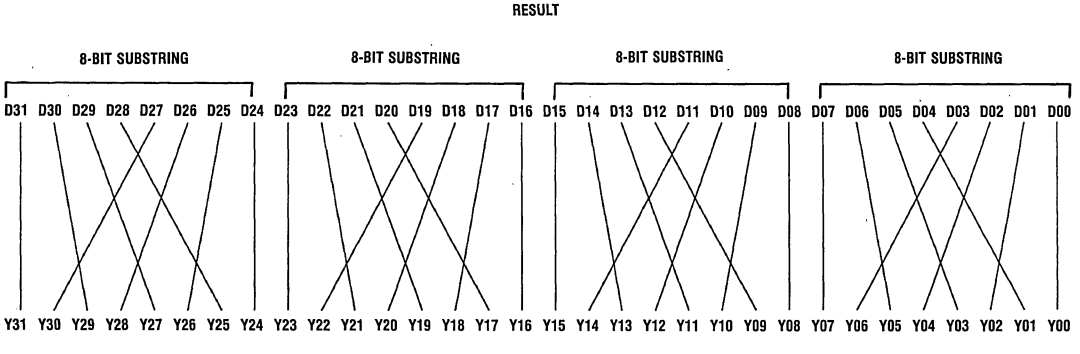


Figure 11. Perform an inverse shuffle on four 8-bit words and pass the result to the Y port.

CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
0	0	0	0	1	0	0

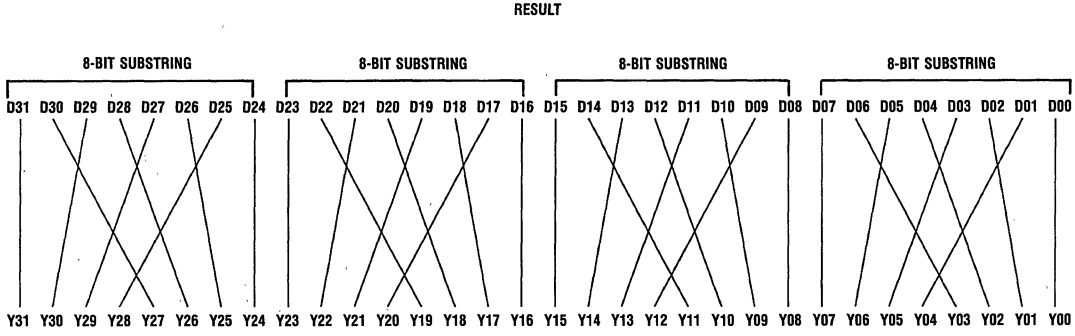
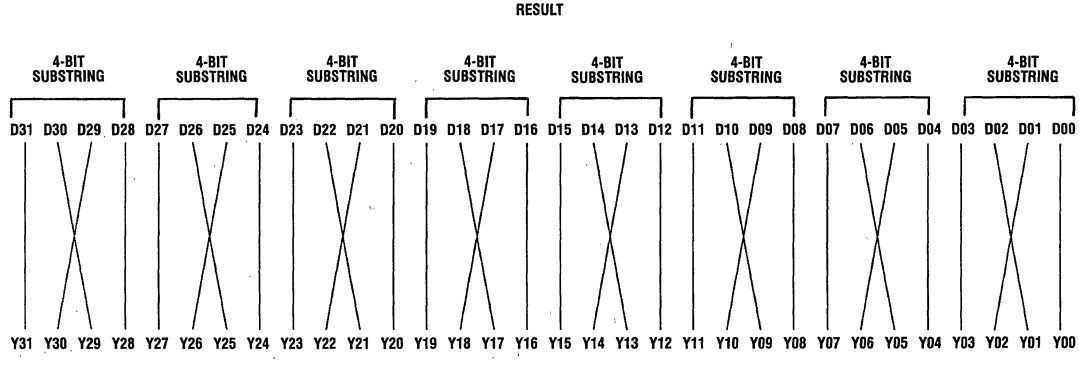


Figure 12. Perform a perfect / inverse shuffle on eight 4-bit words and pass the result to the Y port.

CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
0	0	0	0	1	1	0



Multiplexer Level 4 (figure 13)

Figure 13. Bit-exchange a 32-bit word and pass the result to the Y port.

CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
0	0	0	0	0	0	1

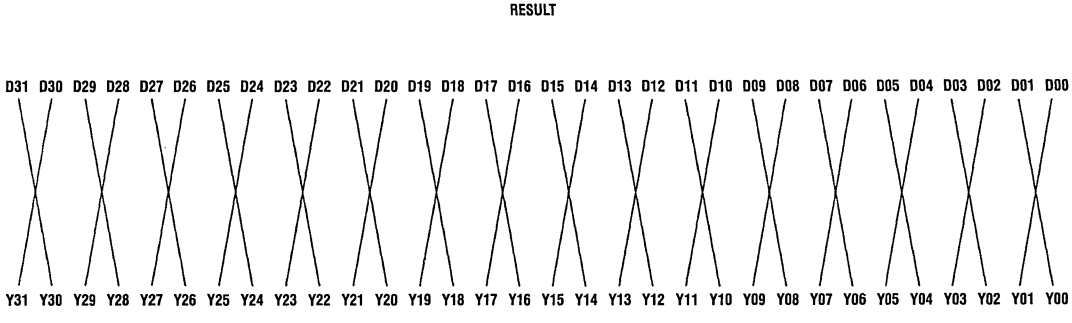


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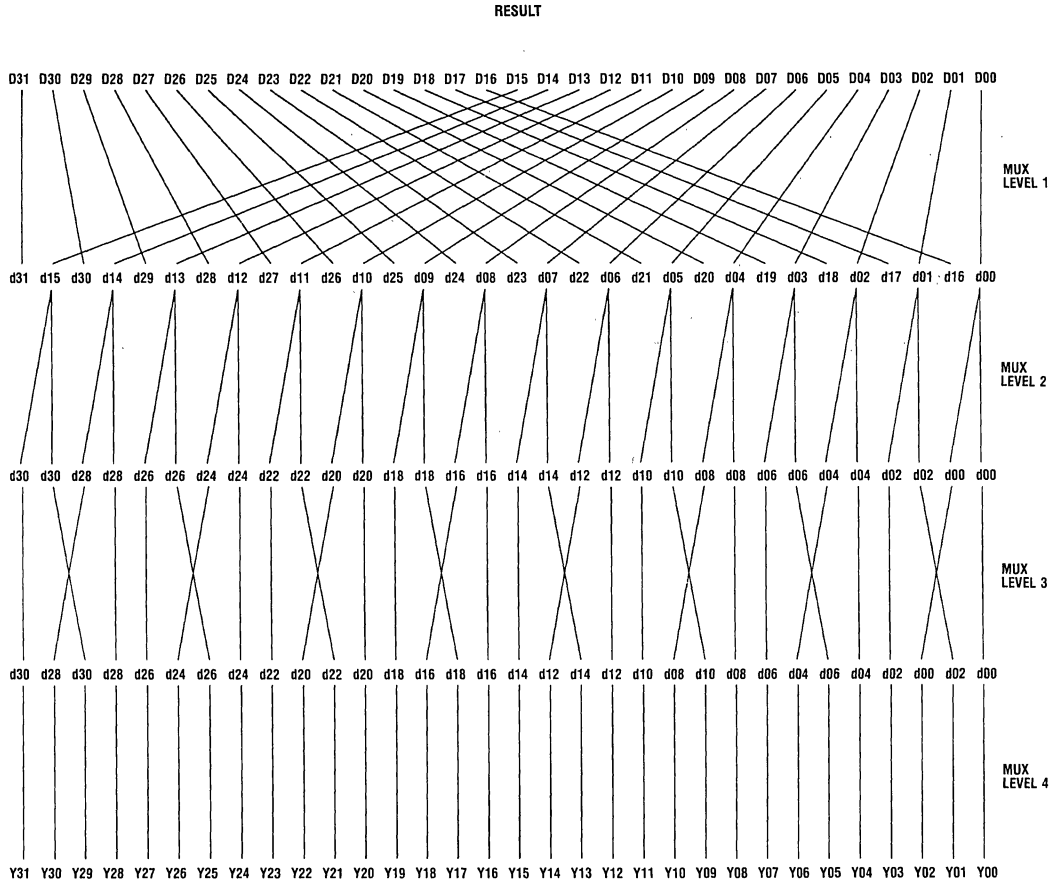
Figure 14. Perform a perfect shuffle on a 32-bit word, followed by a lower broadcast; followed by an 8, 4 bit word shuffles; pass the result to the Y port.

CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
0	1	1	1	1	1	0



Absolute Maximum Ratings

DC Supply Voltage ($V_{DD} - V_{SS}$) ..... +7V
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −55°C to +150°C
Digital Input ..... $V_{SS} - 0.3V \leq V_{IN} \leq V_{DD} + 0.3V$

D.C. Electrical Operating Characteristics: T_A = 0°C to +70°C; V_{DD} = +5V (±10%); V_{SS} = 0V unless otherwise specified

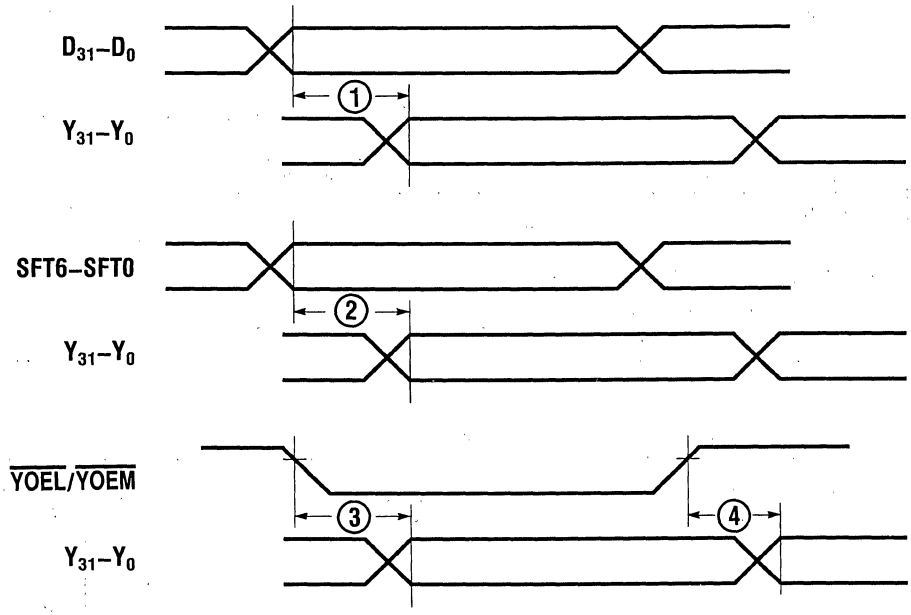
Symbol	Parameter/Conditions	Minimum	Typical	Maximum	Units
V_{IH}	High Level Logic Input	2.0		V_{DD}	V
V_{IL}	Low Level Logic Input	V_{SS}		+0.8	V
V_{OH}	High Level Logic Outputs I_{OH} = .8mA	2.4		V_{DD}	V
V_{OL}	Low Level Logic Outputs I_{OL} = 4.0mA	0		+0.4	V
P_D	Power Dissipation @ ±5.5V		150		mW

Switching Characteristics: (Over Operating Range Unless Otherwise Specified)

No	Parameter Symbol	Test Conditions	S618839			Units
			Min	Typ	Max	
①	t_{DY}			15	30	ns
②	t_{SY}			17	35	ns
③	t_{EN}			6	6	ns
④	t_{DIS}			4	4	ns

Max and Min values may not be 100 percent tested.

Switching Wave Forms



GOULD

AMI Semiconductors

64-Bit Digital Crossbar Switch

Preliminary Data Sheet

S618840

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Features

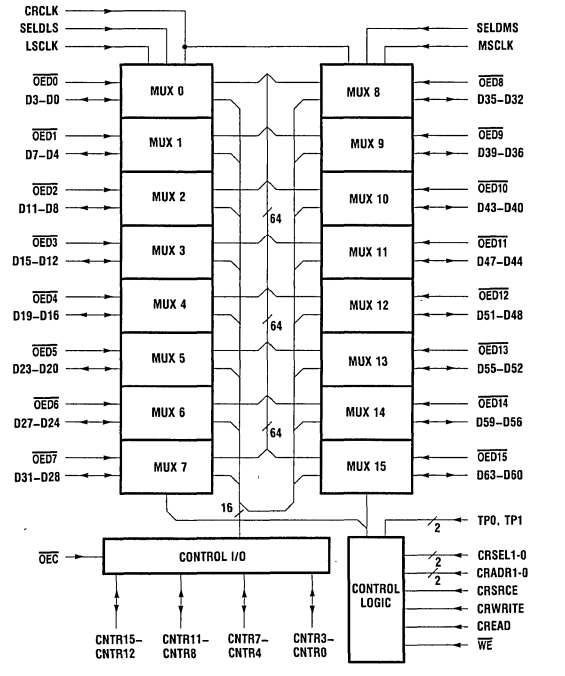
- Hi speed, low power HCMOS digital cross bar switch.
- Programmable switch for parallel processing applications.
- Dynamically reconfigurable for fault-tolerant routing.
- 64-bit bidirectional I/O's in 16-(4 bit) nibbles.
- Data switch source, programmable by nibble.
- Two banks of control flip-flops for storing switch source configurations.
- Two selectable hard-wired switch source configurations.
- CMOS technology with 5V operation and TTL I/O levels.
- Functionally compatible to TI 74AS8840.

General Description

The S618840 is a 64 Bit Digital Crossbar Switch. It has 64 data I/O pins arranged in 16 switchable nibbles (4 bits). There are 16, 4 bit multiplexers, which allows each input nibble to be broadcast (switched) to any other 1 to 15 nibbles, as output, in a single cycle. Multiple input nibbles can be switched to multiple output nibbles, under control of programmable configurations or hard-wired options (See Figure 1).

The control of the multiplexers is selectable from four sources including two banks of programmable control flip-flops (Bank 1, Bank 2) and two hard-wired control circuits.

Block Diagram



Pin Configuration

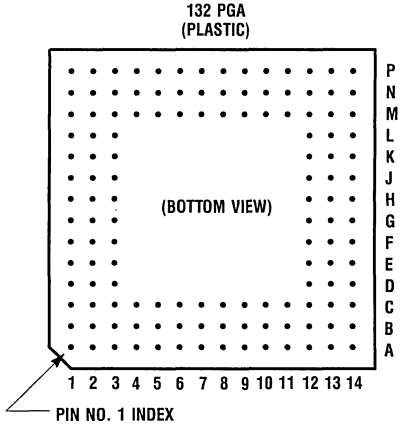
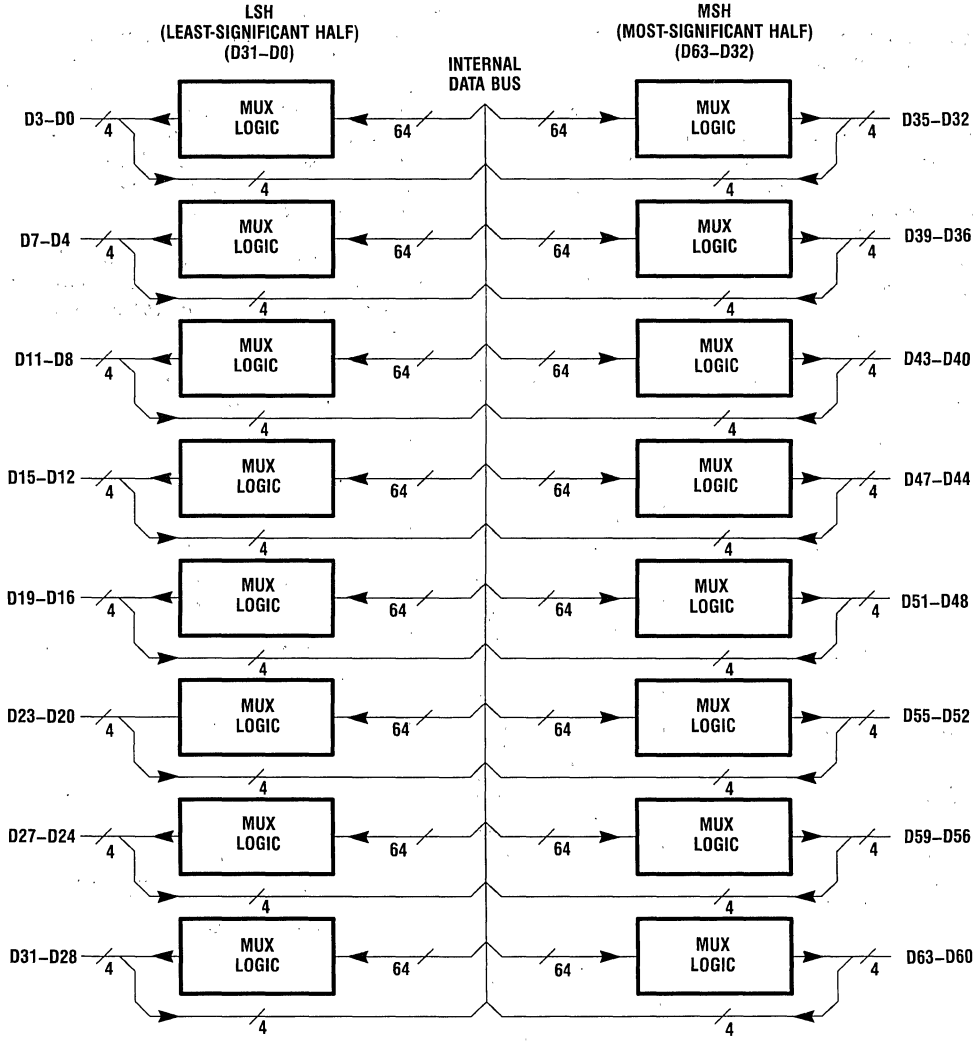


Figure 1. S618840 Digital Crossbar Switch



S618840

The S618840 is primarily intended for multiprocessor interconnection networks and parallel processing applications. In a more general sense, it can be used whenever one needs to transfer data from multiple sources to multiple destinations. Also, since the switching can take place dynamically, this device is also suitable for reconfigurable networks for fault-tolerant routing.

Pin Designation

A1	V_{SS}	C6	$\overline{WE}$	H1	V_{DD}	M10	D5
A2	TP1	C7	CNTR0	H2	V_{SS}	M11	D8
A3	CRSEL0	C8	CNTR3	H3	D53	M12	V_{DD}
A4	V_{SS}	C9	CNTR7	H12	$\overline{D20}$	M13	D12
A5	$\overline{CREAD}$	C10	CNTR11	H13	$\overline{OED5}$	M14	D13
A6	$\overline{OEC}$	C11	CNTR15	H14	D21	N1	$\overline{D44}$
A7	CNTR1	C12	V_{DD}	J1	$\overline{D52}$	N2	$\overline{OED11}$
A8	CNTR2	C13	D29	J2	$\overline{OED13}$	N3	$\overline{D41}$
A9	CNTR5	C14	$\overline{D28}$	J3	D51	N4	$\overline{OED10}$
A10	CNTR8	D1	$\overline{OED15}$	J12	D17	N5	D37
A11	CNTR10	D2	D61	J13	D18	N6	D35
A12	CNTR13	D3	SELDMS	J14	D19	N7	D33
A13	LSCLK	D12	$\overline{D30}$	K1	D50	N8	V_{SS}
A14	V_{SS}	D13	$\overline{OED7}$	K2	D49	N9	$\overline{D1}$
B1	MSCLK	D14	V_{SS}	K3	D48	N10	$\overline{OED1}$
B2	TP0	E1	D59	K12	D15	N11	$\overline{D6}$
B3	CRADR1	E2	V_{SS}	K13	V_{SS}	N12	$\overline{OED2}$
B4	CRSEL1	E3	D60	K14	D16	N13	D10
B5	CWRITE	E12	D27	L1	$\overline{V_{SS}}$	N14	D11
B6	CRCLK	E13	D26	L2	$\overline{OED12}$	P1	V_{SS}
B7	V_{SS}	E14	D25	L3	$\overline{D45}$	P2	D43
B8	CNTR4	F1	D56	L12	$\overline{OED3}$	P3	D40
B9	CNTR6	F2	D57	L13	$\overline{D14}$	P4	D38
B10	CNTR9	F3	D58	L14	$\overline{OED4}$	P5	D36
B11	CNTR12	F12	$\overline{D24}$	M1	D47	P6	$\overline{D34}$
B12	CNTR14	F13	$\overline{OED6}$	M2	D46	P7	$\overline{OED8}$
B13	SELDLS	F14	D23	M3	V_{DD}	P8	V_{DD}
B14	D31	G1	$\overline{D54}$	M4	D42	P9	D0
C1	D62	G2	$\overline{OED14}$	M5	$\overline{D39}$	P10	D3
C2	D63	G3	D55	M6	$\overline{OED9}$	P11	D4
C3	V_{DD}	G12	D22	M7	$\overline{D32}$	P12	D7
C4	CRADR0	G13	V_{SS}	M8	$\overline{OED0}$	P12	D9
C5	CRSRCE	G14	V_{DD}	M9	D2	P14	V_{SS}

Pin Description

Pin Name	No.	I/O	Description
D0	P9		
D1	N9		
D2	M9		
D3	P10		
D4	P11		
D5	M10		
D6	N11		
D7	P12		
D8	M11		
D9	P13		
D10	N13		
D11	N14		
D12	M13		
D13	M14		
D14	L13		
D15	K12	I/O	Bi-directional data I/O pins (D31–D0 are Least-Significant Half) (LSH)
D16	K14		
D17	J12		
D18	J13		
D19	J14		
D20	H12		
D21	H14		
D22	G12		
D23	F14		
D24	F12		
D25	E14		
D26	E13		
D27	E12		
D28	C14		
D29	C13		
D30	D12		
D31	B14		
D32	M7		
D33	N7		
D34	P6		
D35	N6		
D36	P5		
D37	N5		
D38	P4	I/O	Bi-directional data I/O pins (D63–D31 are Most-Significant Half) (MSH)
D39	M5		
D40	P3		
D41	N3		
D42	M4		
D43	P2		
D44	N1		
D45	L3		

Pin Description (cont.)

Pin Name	No.	I/O	Description
D46	M2	I/O	Bi-directional data I/O pins (D63–D31 are Most-Significant Half) (MSH)
D47	M1		
D48	K3		
D49	K2		
D50	K1		
D51	J3		
D52	J1		
D53	H3		
D54	G1		
D55	G3		
D56	F1		
D57	F2		
D58	F3		
D59	E1		
D60	E3		
D61	D2		
D62	C1		
D63	C2		
$\overline{OED0}$	M8	I	Output enable for data I/O pins, nibbles within (D63–D0) i.e. $\overline{OED0}$ — D3–D0, $\overline{OED1}$ — D7–D4, • • • $\overline{OED15}$ — D63–D60
$\overline{OED1}$	N10		
$\overline{OED2}$	N12		
$\overline{OED3}$	L12		
$\overline{OED4}$	L14		
$\overline{OED5}$	H13		
$\overline{OED6}$	F13		
$\overline{OED7}$	D13		
$\overline{OED8}$	P7		
$\overline{OED9}$	M6		
$\overline{OED10}$	N4		
$\overline{OED11}$	N2		
$\overline{OED12}$	L2		
$\overline{OED13}$	J2		
$\overline{OED14}$	G2		
$\overline{OED15}$	D18		
SELDLS	B13	I	Selects either data input registers or real-time data of (LSH) data input to main internal 64-bit bus
SELDMS	D3	I	Selects either data input registers or real-time data of (MSH) data input to main internal 64-bit bus
LSCLK	A13	I	Clock input to clock (LSH) data input into data input registers (⌐)
MSCLK	B1	I	Clock input to clock (MSH) data input into data input registers (⌐)
$\overline{OEC}$	A6	I	Output enable for CNTR15–CNTR0

Pin Description (cont.)

Pin Name	No.	I/O	Description
TP1 TP0	A2 B2	I	Test pins
CRSEL0 CRSEL1	A3 B4	I	Selects one of four control functions to control the multiplexers
CRSRCE	C5	I	Selects source load for control flip flop register banks
CWRITE	B5	I	Control flip flop register bank select (CF(X)–bank1, CF(X)–bank2)
$\overline{WE}$	C6	I	Write enable for control flip flop registers (CF(X))
CRADR1 CRADR0	B3 C4	I	Control flip-flop register address select. Decodes/selects, 1 of 4, 16 bit groups of control flip-flops for I/O on CNTR15–CNTR0
CRCLK	B6	I	Control flip flop register clock (⌐)
CREAD	A5	I	Selects between control flip flop register banks (1) or (2), to read out on CNTR15–CNTR0
CNTR0 CNTR1 CNTR2 CNTR3 CNTR4 CNTR5 CNTR6 CNTR7 CNTR8 CNTR9 CNTR10 CNTR11 CNTR12 CNTR13 CNTR14 CNTR15	C7 A7 A8 C8 B8 A9 B9 C9 A10 B10 A11 C10 B11 A12 B12 C11	I/O	Control I/O. Input/Output pins (four groups of four bits, for data I/O to the control flip flop registers addressed by CRADR1–0)
V_{SS} V_{SS} V_{SS} V_{SS} V_{SS} V_{SS} V_{SS} V_{SS}	A1 E2 H2 L1 P1 N8 P14 K13	—	Ground pins

Pin Description (cont.)

Pin Name	No.	I/O	Description
V_{SS} V_{SS} V_{SS} V_{SS} V_{SS}	G13 D14 A14 B7 A4	—	Ground pins
V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD}	H1 M3 P8 M12 G14 C12 C3	—	5-volt supply pins

Table 1. S618840 Response to Control Inputs

Signal	High	Low
LSCLK	Clocks LSH of data input into input data registers on low-to-high transition	
MSCLK	Clocks MSH of data input into input data registers on low-to-high transition	
SELDLS	Selects real-time LSH data input to main internal data bus	Selects stored LSH data input to main internal data bus
SELDMS	Selects real-time MSH data input to main internal data bus	Selects stored MSH data input to main internal data bus
CNTR15–CNTR0	I/O pins for control flip-flops (see Table 7)	
CRADR1–CRADR0	Selects 16-bit groups of control flip-flops as destination or source for inputs or outputs on CNTR15–CNTR0 (see Table 7)	
CREAD	Selects **second bank** of control flip-flops to read on CNTR15–CNTR0 in 16-bit words addressed by CRADR1–CRADR0	Selects **first bank** of control flip-flops to read on CNTR15–CNTR0 in 16-bit words addressed by CRADR1–CRADR0
CRWRITE	Control flip-flops destination select (see Table 5)	
CRSRCE	Control flip-flops load source select (see Table 5)	
$\overline{WE}$	Inhibits write to control flip-flops	Enables write to control flip-flops
CRCLK	Clocks CNTR15–CNTR0 inputs into control flip-flops	
$\overline{OEC}$	Inhibits output of data from control flip-flops on CNTR15–CNTR0	Enables output of data from control flip-flops on CNTR15–CNTR0
$\overline{OED15}$–$\overline{OED0}$	Inhibits output of data I/O pin nibbles	Enables output of data I/O pin nibbles
CRSEL1–CRSEL0	Selects one of four control functions to control the switch (see Table 2)	
TP1–TP0	Test pins (see Table 8)	

Detailed Description
The 64 data I/O pins of the S618840 are arranged as 16, 4 bit nibble groups. Each of these nibble I/O pins is a bidirectional input/output to 1 of 16 nibble multiplexers (See Figure 1, 2). During a switching cycle, each multiplexer passes four bits of data, either stored in data input registers or as direct real-time data input, to a 64 bit internal data bus. Then, each of the 16 nibble multiplexers independently selects 1 of 16 nibbles from the internal data bus as output on 1 of the 16 data I/O pin nibbles.

The 16 input data nibbles are organized into two groups of 8 nibbles. These are: LSH (Least Significant Half) and MSH (Most Significant Half). Data to the internal 64 bit data bus, is selectable from the data input registers or real-time data input by SELDLS for LSH and SELDMS for MSH. Two clocks, LSCLK and MSCLK are used to clock data into the data input registers for the LSH, MSH respectively.

Each output nibble, is selected from 1 of 16 nibbles of the 64 bit internal data bus. This is done by a 16 X 4 bit multiplexer; one for each output nibble (See Figure 2 & 3). These 16 multiplexers are controlled by a selectable control source input. This control source input can be either one of two banks of programmable control flip-flops, or one of two hand-wired control circuits. Inputs to the programmable control flip-flops can be loaded from either a pre-defined nibble of the 64 bit internal data bus or from the $\overline{\text{CNTRL}}$(15–0) pins. A separate CRCLK is used along with $\overline{\text{WE}}$ to load the banks of the control flip-flops (See Figure 3).

Architecture
The S618840 has its 64 data I/O pins arranged in 16 multiplexer logic groups (See Figure 2 and 3). Each multiplexer group controls four bits of real-time data input and four bits of stored data input register to the internal 64 bit data bus.

Two input controls are provided to select between the stored data input register or real-time data input to go to the 64 bit internal data bus. These are SELDLS for the LSH side (D31–D0) and SELDMS for the MSH side (D63–D32). The data stored in the data input registers is controlled by LSCLK for the LSH side (D31–D0) and MSCLK for the MSH side (D63–D32). The 16 data input nibbles (N(X)) make up the 64 bit internal data bus.

This 64 bit internal data bus supplies 16 data nibbles to 16, 16 X 4 bit output multiplexers (MUX(16X4)). One of the four selectable control sources controls the 16 X 4 bit output multiplexers to multiplex one of the 16 nibbles of the 64 bit internal data bus to one of the 16 nibbles of the data I/O pins, under control of a tri-state output driver $\overline{\text{OED}}$(15–0).

The input to output pattern of the entire crossbar switch is controlled by the input and output multiplexers. Many switching configurations can be selected by programming the control flip-flop banks to control the output selection from the 16 X 4 bit multiplexers (MUX(16X4)).

Multiplexer logic group (MUX(X), X=15–0)
Input data flows into the 64 bit internal data bus and thus each of the 16 multiplexers, on four data I/O pins connected to a data input register and a 2 X 4 bit multiplexer (MUX(2X4)). Data inputs to the 4 bit internal data bus are thus, either clocked into a data input register and input, or passed directly to the internal bus. The 64 bits of internal data bus are presented to each of the 16 X 4 bit multiplexers (MUX(16X4)), which selects the data nibble output.

Each of the 16 multiplexers (MUX(X), (X=15–0) (Figure 3), contains two control flip-flop CF(X) nibbles, Bank 1 and Bank 2. Each CF(X) is composed of four D-type positive edge triggered flip-flops. Table 2 shows the control source selection decoding.

Table 2. 16-to-1 Output Multiplexer Control Source Selects

CRSEL1	CRSEL0	Control Source Selected
0	0	CF(X) Flip-flop Bank 1*
0	1	CF(X) Flip-flop Bank 2*
1	0	MSH/LSH Exchange**
1	1	Read-Back (output echoes input)**

*Programmable
**Hard-wired control function

In addition to the two programmable CF(X) banks, there are two hard-wired, pre-defined control functions which can be selected. The READ-BACK source, allows each multiplexer to output its own input bits. (eg. MUX(5) read back is (N(5), (D23–D20)), of the 64 bit internal data bus). The MSH/LSH EXCHANGE directs all the nibbles of the LSH side and MSH side respectively

Figure 2. Block Diagram—Digital Crossbar Switch S618840

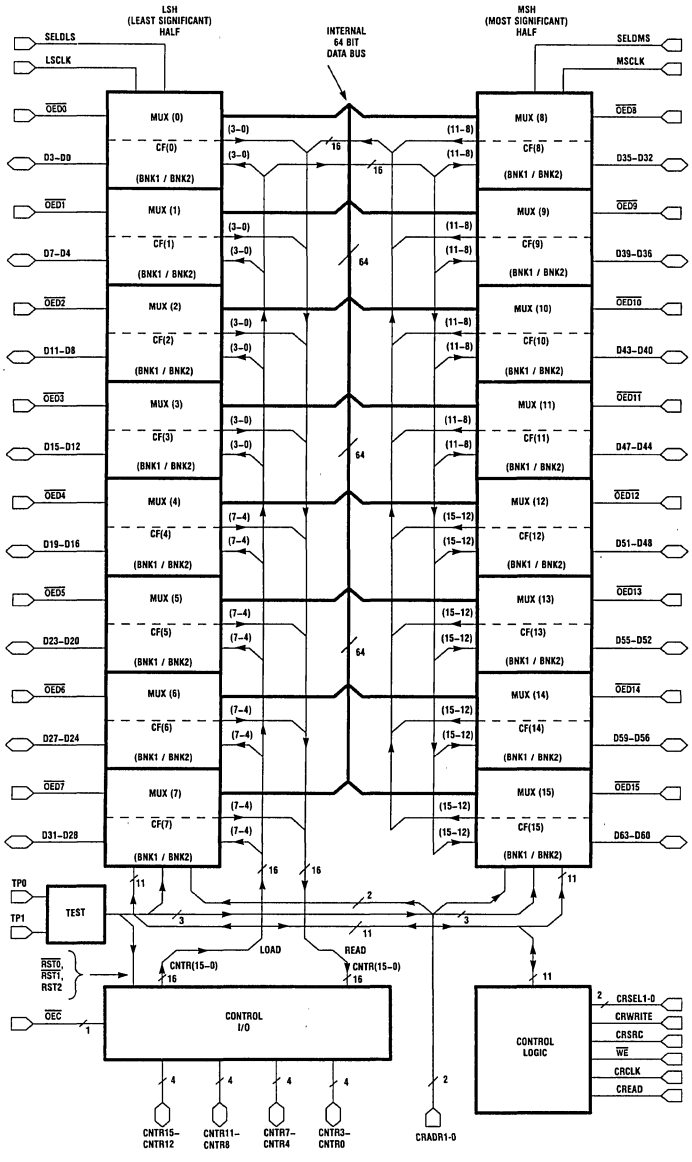
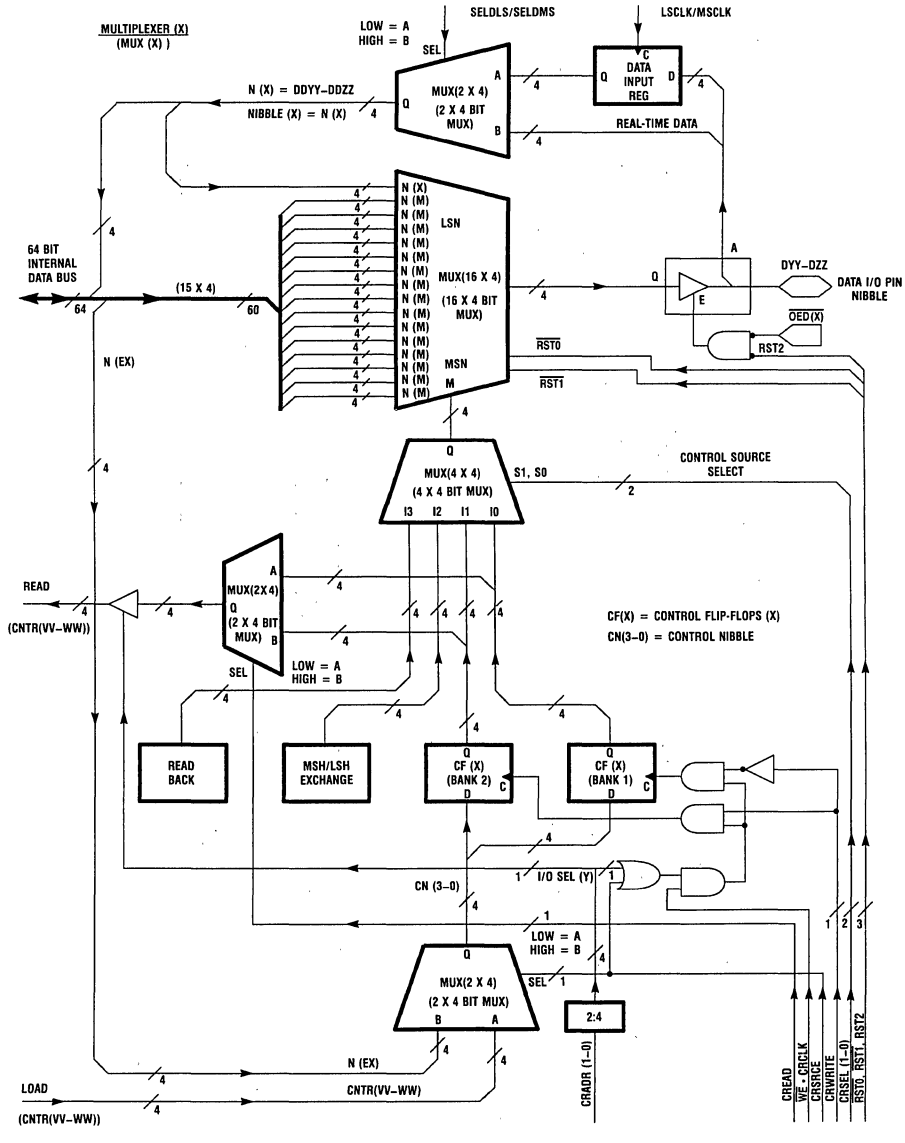


Figure 3. Multiplexer Logic (Mux (X), N (X), X = 15-0)



to be output nibbles to their corresponding opposite side. For example;

D23–D20 ← Exchanges with → D55–D52

NOTE: Neither of the control hard-wire functions affects the contents of the CF(X) banks.

A four bit control nibble CN(3–0) can be stored in each CF(X) to control the 16 X 4 bit MUX (MUX(16X4)), (See Figure 3). One control nibble is loaded in each CF per MUX, a total of 16 control nibbles per flip-flop bank. Table 4 lists the control nibbles CN(3–0) (which are used to control the 16 X 4 bit MUX) and the internal data bus bits selected by CN(3–0) by the 16 X 4 bit MUX (MUX(16X4)). The control nibble CN(3–0) can have a source from a pre-defined nibble from the internal data bus (N(EX)), or from the control I/O lines CNTR(15–0).

Table 3, shows the internal data bus nibble N(EX) and I/O lines CNTR(VV–WW), used as a possible source of input for CN(3–0). It also shows the relationship of each multiplexer block, the nibble it defines and the data lines associated to it.

Each control nibble in Table 4 can be stored in either bank of CF(X) and sent as an internal control signal to the 16 X 4 MUX (MUX(16X4)). As an example, any CF(X) loaded with '1000' from the CN(3–0) can be used to select the (D35–D32) nibble (N(8)) of the internal data bus as output of the 16 X 4 MUX, or all 16, CF(X) of bank 1 can be loaded with the same CN(3–0) and the same outputs will be selected by the entire switch for the 16 X 4 bit MUXs.

Table 3. MUX(X), N(X), N(EX), DYY–DZZ, CNTR VV–CNTR WW

X	MUX(X)	N(X)	DYY–DZZ	N(EX)	CNTR(VV–WW)
0	MUX(0)	N(0)	D3–D0	N(8)	(3–0)
1	MUX(1)	N(1)	D7–D4	N(9)	(3–0)
2	MUX(2)	N(2)	D11–D8	N(10)	(3–0)
3	MUX(3)	N(3)	D15–D12	N(11)	(3–0)
4	MUX(4)	N(4)	D19–D16	N(12)	(7–4)
5	MUX(5)	N(5)	D23–D20	N(13)	(7–4)
6	MUX(6)	N(6)	D27–D24	N(14)	(7–4)
7	MUX(7)	N(7)	D31–D28	N(15)	(7–4)
8	MUX(8)	N(8)	D35–D32	N(0)	(11–8)
9	MUX(9)	N(9)	D39–D36	N(1)	(11–8)
10	MUX(10)	N(10)	D43–D40	N(2)	(11–8)
11	MUX(11)	N(11)	D47–D44	N(3)	(11–8)
12	MUX(12)	N(12)	D51–D48	N(4)	(15–12)
13	MUX(13)	N(13)	D55–D52	N(5)	(15–12)
14	MUX(14)	N(14)	D59–D56	N(6)	(15–12)
15	MUX(15)	N(15)	D63–D60	N(7)	(15–12)

Table 4. 16 X 4 Bit Multiplexer Control Nibbles

Control Nibble Values CN3	CN2	CN1	CN0	CN(3–0) Hex	Nibble from 64 Bit Internal Data Bus Selected as Multiplexer Output	N(X)
0	0	0	0	0	D3–D0	0
0	0	0	1	1	D7–D4	1
0	0	1	0	2	D11–D8	2
0	0	1	1	3	D15–D12	3
0	1	0	0	4	D19–D16	4
0	1	0	1	5	D23–D20	5
0	1	1	0	6	D27–D24	6
0	1	1	1	7	D31–D28	7
1	0	0	0	8	D35–D32	8
1	0	0	1	9	D39–D36	9
1	0	1	0	A	D43–D40	10
1	0	1	1	B	D47–D44	11
1	1	0	0	C	D51–D48	12
1	1	0	1	D	D55–D52	13
1	1	1	0	E	D59–D56	14
1	1	1	1	F	D63–D60	15

The CRSRCE pin controls the source used as input to the CN(3–0) lines from the multiplexer, to then be used as input to the CF(X) control flip-flops. As stated before, this can be from either the internal data bus as nibble N(EX) or from the external control I/O pins CNTR (15–0). The CRWRITE pin selects whether bank 1 or bank 2 of the control flip-flops is to be loaded. In effect, CRWRITE and CRSRCE, together, control the source, destination for loading the control flip-flops. (See Table 5).

Table 5. Control Flip-Flops Load Selects

CRSRCE	CRWRITE	Source and Destination
0	0	CNTR inputs to flip-flop bank 1
0	1	CNTR inputs to flip-flop bank 2
1	0	N(EX) Data inputs to flip-flop bank 1
1	1	N(EX) Data inputs to flip-flop bank 2

When either CF(X), bank 1 or 2 is being loaded from the internal data bus, the four signals; $\overline{WE}$, CRSRCE, CRWRITE, and the control flip-flop clock CRCLK are used in combination, to load *all* 16 control nibbles in a single cycle. Table 3 shows that internal data bus nibbles on the LSH side of the switch are sent to the CN(3–0) control nibbles of the MSH side. Likewise the internal data bus nibbles on the MSH side of the switch are sent to the CN(3–0) control nibbles of the LSH side. For example, the data nibble N(8) for MUX(8) would use the internal data bus nibble N(EX)=N(0), (D3–D0) as input to its CN(3–0) control nibble to be loaded into CF(8) bank 1 or 2. Likewise, the data nibble N(0) for MUX(0) would use the internal data bus nibble N(EX)=N(8), (D35–D32) as inputs to its CN(3–0) control nibble to be loaded into CF(0) bank 1 or 2. Table 6 shows the pattern for MSH/LSH exchange when a bank of CF(X) flip-flops is loaded with CN(3–0) from the internal data bus as its sources.

When either CF(X), bank 1 or 2 is being loaded from the external control I/O pins CNTR(15–0), the four signals; $\overline{WE}$, CRSRCE, CRWRITE, and the control flip-flop clock CRCLK are used. However, the CRADR1 and CRADR0 pins address four control nibbles at a time to be loaded in one clock cycle from the control I/O pins CNTR(15–0). This can be seen in Table 7. Note that the load sequence for each CRADR1–0 address is staggered. The same addresses of CRADR1–0 in combination with CREAD and $\overline{OEC}$ will read out four CF(X) groups at a time on the control I/O pins CNTR(15–0). (See Table 6).

Table 6. Inputs to Control Flip-Flops (CF)

Control Flip-Flop Nibbles	Data Outputs Affected	N(X)	CNTR Inputs to Control Flip-Flops	Data Inputs to Control Flip-Flops	N(EX)
CF0	D3–D0	N(0)	CNTR3–CNTR0	D35–D32	N(8)
CF1	D7–D4	N(1)		D39–D36	N(9)
CF2	D11–D8	N(2)		D43–D40	N(10)
CF3	D15–D12	N(3)		D47–D44	N(11)
CF4	D19–D16	N(4)	CNTR7–CNTR4	D51–D48	N(12)
CF5	D23–D20	N(5)		D55–D52	N(13)
CF6	D27–D24	N(6)		D59–D56	N(14)
CF7	D31–D28	N(7)		D63–D60	N(15)
CF8	D35–D32	N(8)	CNTR11–CNTR8	D3–D0	N(0)
CF9	D39–D36	N(9)		D7–D4	N(1)
CF10	D43–D40	N(10)		D11–D8	N(2)
CF11	D47–D44	N(11)		D15–D12	N(3)
C12	D51–D48	N(12)	CNTR15–CNTR12	D19–D16	N(4)
CF13	D55–D52	N(13)		D23–D20	N(5)
CF14	D59–D56	N(14)		D27–D24	N(6)
CF15	D63–D60	N(15)		D31–D28	N(7)

Table 7. Loading Control Flip-Flops From CNTR I/O's

CRADR1	CRADR0	$\overline{WE}$	CRCLK	Control (CNTR) I/O Numbers				CF(X) Selected
				15–12	11–8	7–4	3–0	
0	0	L	⌐	CF12	CF8	CF4	CF0	12, 8, 4, 0
0	1	L	⌐	CF13	CF9	CF5	CF1	13, 9, 5, 1
1	0	L	⌐	CF14	CF10	CF6	CF2	14, 10, 6, 2
1	1	L	⌐	CF15	CF11	CF7	CF3	15, 11, 7, 3
X	X	H	X	Inhibit write to flip-flops				

Table 8. Test Pin Inputs

TP1	TP0	$\overline{OED15}$–$\overline{OED0}$	$\overline{OEC}$	Result
0	0	0	0	All outputs and I/Os forced low
0	1	0	0	All outputs and I/Os forced high
1	0	X	X	All outputs placed in a high-impedance state
1	1	X	X	Normal operation (default state)

Test Pins

The test pins TP1–TP0 are provided for various system tests. The normal operation as depicted in Table 8, is for the test pins to be in a high state. To force all outputs in a high impedance state (CNTR(15–0) and D63–D0), set TP1 = high and TP0 = low. To force all outputs in a high state, set TP1 = low, TP0 = high. To force all outputs in a low state, set TP1 = low, TP0 = low.

Programming Examples

Programming the S618840 is a straight forward procedure involving few control signals and procedures to set up the switch configurations by loading the control words in the control flip-flop banks. The following examples, help to demonstrate the control signals and procedures for loading and using control words.

MSH/LSH Exchange

This example will show two ways to swap LSH nibbles to MSH nibbles. This can be done by two methods, either using the predefined control source MSH/LSH EXCHANGE selected by the CRSEL(1–0) pins or by separately loading the CF(X) control flip-flops of each multiplexer with the proper control nibble to select the exact opposite nibble for an MSH/LSH exchange.

In the first case, where the pre-defined MSH/LSH EXCHANGE control source is used, Figure 4, line 1, 2 gives a programming example. In line 1, an input data pattern is written into the LSH, MSH halves of the switch and stored in the data input registers. This is done by putting all $\overline{OED}$ lines high and presenting input data to the data I/O pins. This is followed by clocking LSCLK and MSCLK. In line 2, the MSH/LSH exchange is selected by (CRSEL(1–0) = 10) and all $\overline{OED}$ lines are brought low. The result is to read out the MSH/LSH data stored in the data input registers of the MSH/LSH switch halves—in an exchanged order.

The same effect can be done by separately programming each CF(X) control flip-flop of bank 1 of all the multiplexers. The control nibbles for this can be seen in Table 9 which are taken from Table 3, 4, and 6.

With this list of control words, the control I/O pins CNTR(15–0) are used to load the CF(X) (X=15–0) control flip-flops. These are loaded into bank 1, four control flip-flops at a time for a total of four clocks. This is shown in Figure 4, lines 3, 4, 5, and 6. In line 7, once the control flip-flops are set up, the MSH/LSH exchange is made with the control source of the 16 X 4 MUX now coming from bank 1 (CRSEL(1–0) = 00). Line 8 is used to show how by using (CRSEL(1–0) = 11), the read back control source is selected which shows the contents of each data input register read out on its corresponding data I/O pins.

The CF(X) control flip-flops of bank 1 could also have been loaded from the internal 64 bit data bus. In this mode and from Table 3, it can be seen that the MSH data I/O pins (D63–D33) are used as inputs to the

Table 9. Control Words for an MSH/LSH Exchange

Control Flip-Flop Nibbles	CNTR Inputs to Load Flip-Flops	CN (3–0) Binary	CN (3–0) Hex	Results
CF0	CNTR3–CNTR0	1000	8	D35–D32 → D3–D0
CF1		1001	9	D39–D36 → D7–D4
CF2		1010	A	D43–D40 → D11–D8
CF3		1011	B	D47–D44 → D15–D12
CF4	CNTR7–CNTR4	1100	C	D51–D48 → D19–D16
CF5		1101	D	D55–D52 → D23–D20
CF6		1110	E	D59–D56 → D27–D24
CF7		1111	F	D63–D60 → D31–D28
CF8	CNTR11–CNTR8	0000	0	D3–D0 → D35–D32
CF9		0001	1	D7–D4 → D39–D36
CF10		0010	2	D11–D8 → D43–D40
CF11		0011	3	D15–D12 → D47–D44
CF12	CNTR15–CNTR12	0100	4	D19–D16 → D51–D48
CF13		0101	5	D23–D20 → D55–D52
CF14		0110	6	D27–D24 → D59–D56
CF15		0111	7	D31–D28 → D63–D60

corresponding LSH, CN(3–0) control nibble. Likewise the LSH data I/O pins (D32–D0) are used as inputs to the corresponding MSH, CN(3–0) control nibble. These control nibbles are then loaded into either bank 1 or 2 of the CF(X) control flip-flops. The control flip-flops are loaded from the data I/O pins in one CRCLK cycle (all 16 nibbles). This is shown in line 9 of Figure 4. Following this, lines 10–13 read out the contents of CF(X) bank 1 on the CNTR(15–0) lines as addressed by CRADR(1–0). This shows the correct control nibble pattern was loaded into bank 1 from the data I/O pins to program an MSH/LSH exchange mode. The control nibbles loaded from the data I/O pins may be loaded as one 64 bit real-time input or as two 32 bit words stored previously in the data input registers. To use the data stored in the data input registers, the MSCLK, LSCLK are used to load the MSH, LSH data inputs into the data input registers. Then SELDMS, SELDLS are used to select these registers as the data input to the internal data bus and as a source input to load the control flip-flops. Whenever the control flip-flops are loaded from the data inputs, all 64 bits of control data must be present when the CRCLK is used so that all control nibbles in a program are loaded simultaneously.

Figure 4 lines 14 and 15 show the loading of the MSH and LSH data input registers on separate cycles. Line 16 shows the loading of the CF(X) bank 1 control flip-flops in one cycle from the data input registers.

Broadcast a Nibble

In this example, any of the 16 data I/O input nibbles can be broadcast to any of the other 15 data I/O output nibbles. Input nibble (D3–D0) will be used as input in this example, to be broadcast to all the other data I/O pins as output. The CF(X) bank 2 control flip-flops will be used as the control source of the 16 X 4 MUX's. Also, the control flip-flops will be loaded using the CNTR(15–0) control I/O pins. To do this, CRSRCE is set low to select the CNTR pins as input for the CN(3–0) control nibble. Then the CRWRITE pin is set high to select bank 2. Also CREAD is set high so as to select bank 2 for reading CF(X) out on the CNTR pins. Figure 4, lines 17–20 show the loading of CF(X) control flip-flops bank 2 with the control nibbles necessary for broadcasting of data I/O pins (D3–D0) to all other 15 data I/O nibbles. Line 21 shows (D3–D0) set as input to the value "A" which is broadcast to all other pins which are set as outputs. Note that $\overline{OED0}$=1, while $\overline{OED15–2}$=0. Also note that the previously control nibbles set in bank 1 are still valid. The input pins CRSEL(1–0) simply select which bank (or hard-wire function) is to be the control source input to the 16 X 4 MUX input.

Absolute Maximum Ratings

DC Supply Voltage (V_{DD} – V_{SS})	+7V
Operating Temperature	0°C to +70°C
Storage Temperature	–55°C to +150°C
Digital Input	V_{SS} – 0.3V ≤ V_{IN} ≤ V_{DD} + 0.3V

D.C. Electrical Operating Characteristics: T_A = 0°C to +70°C; V_{DD} = +5V (±10%); V_{SS} = 0V unless otherwise specified

Symbol	Parameter/Conditions	Minimum	Typical	Maximum	Units
V_{IH}	High Level Logic Input	2.0		V_{DD}	V
V_{IL}	Low Level Logic Input	V_{SS}		+0.8	V
V_{OH}	High Level Logic Outputs I_{OH} = .8mA	2.4		V_{DD}	V
V_{OL}	Low Level Logic Outputs I_{OL} = 4.0mA	0		+0.4	V
P_D	Power Dissipation @ ±5.5V		150		mW

Figure 4. Programming Examples

Line No.	CRSRCE	CWRITE	WE	CRCLK	CRADR1	CRADR0	CREAD	CNTR(15-12) Pins (Hex)	CNTR(11-8) Pins (Hex)	CNTR(7-4) Pins (Hex)	CNTR(3-0) Pins (Hex)	OEC	CRSEL1	CRSEL0	SELDMS	MSCLK	SELDLS	LSCLK	D63-D60	D59-D56	D55-D52	D51-D48	D47-D44	D43-D40	D39-D36	D35-D32	D31-D28	D27-D24	D23-D20	D19-D16	D15-D12	D11-D8	D7-D4	D3-D0	OED 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	TP1	TP0
1	X	X	1	1	X	X	X	X	X	X	X	1	X	X	X	X	X	⌐	6	6	6	6	A	A	A	A	9	9	9	9	5	5	5	5	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	1
2	X	X	1	1	X	X	X	X	X	X	X	1	X	X	X	X	X	1	9	9	9	9	5	5	5	5	6	6	6	6	A	A	A	A	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	0
3	0	0	0	⌐	0	0	X	4	0	C	8	1	X	X	1	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	1
4	0	0	0	1	0	1	X	5	1	D	9	1	X	X	1	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	0
5	0	0	0	⌐	1	0	X	6	2	E	A	1	X	X	1	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	1
6	0	0	0	⌐	1	1	X	7	3	F	B	1	X	X	1	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	1
7	X	X	1	1	X	X	X	X	X	X	X	1	0	0	1	0	1	9	9	9	9	5	5	5	5	6	6	6	6	A	A	A	A	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	0
8	X	X	1	1	X	X	X	X	X	X	X	1	1	1	0	1	0	1	6	6	6	6	A	A	A	A	9	9	9	9	5	5	5	5	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	1
9	1	0	0	⌐	0	X	X	X	X	X	X	1	X	X	1	X	1	⌐	F	E	D	C	B	A	9	8	X	X	X	X	X	X	X	X	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	1
10	X	X	1	1	1	0	0	4	0	C	8	0	X	X	1	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	0
11	X	X	1	1	1	0	1	5	1	D	9	0	X	X	1	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	1
12	X	X	1	1	1	1	0	6	2	E	A	0	X	X	1	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	1
13	X	X	1	1	1	1	1	7	3	F	B	0	X	X	1	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	1
14	X	X	1	1	X	X	X	X	X	X	X	1	X	X	1	X	1	⌐	F	E	D	C	B	A	9	8	X	X	X	X	X	X	X	X	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	1
15	X	X	1	1	X	X	X	X	X	X	X	1	X	X	1	X	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	1
16	1	0	0	⌐	1	X	X	X	X	X	X	1	X	X	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	1
17	0	1	0	⌐	0	0	1	0	0	0	0	1	X	X	1	X	1	⌐	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	1
18	0	1	0	⌐	0	1	1	0	0	0	0	1	X	X	1	X	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	1
19	0	1	0	⌐	1	0	1	0	0	0	0	1	X	X	1	X	1	⌐	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	1
20	0	1	0	⌐	1	1	0	0	0	0	0	1	X	X	1	X	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1	1
21	X	X	1	1	X	X	X	X	X	X	X	1	1	0	1	1	X	1	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	1	1

X = Don't Care

AC Electrical Characteristics (V_{CC} = 5V ±10%, all temperature ranges, unless otherwise specified)

Parameter		S618840 Min	S618840 Max	Unit
tw Pulse duration	LSCLK, MSCLK, and CRCLK high or low	12(1)		ns
tsu Setup time before CRCLK (⌐)	Data	10		ns
	CNTRn	8		
	SELDMS, SELDLS	12		
	CRADR1, CRADR0	12		
	CRSRCE, CRWRITE	10		
	WE	11		
tsu Setup time, Data before LSCLK(⌐) or MSCLK(⌐)		5		ns
th Hold time after CRCLK(⌐)	Data	5		
	CNTRn	5		
	SELDMS, SELDLS	5		
	CRADR1, CRADR0	5		
	CRSRCE, CRWRITE	5		
	WE	5		
th Hold time, Data after LSCLK(⌐) or MSCLK(⌐)		5		ns

Parameter	From (Input)	To (Output)	S618840 Min	S618840 Typ(1)	S618840 Max(2)	Unit
tpd	Data in	Data out		21	44	ns
	MSCLK, LSCLK			25	50	
	SELDMS, SELDLS			24	48	
	CRCLK			31	61	
	CRSEL1, CRSEL0			27	56	
	CREAD	CNTRn		17	35	
	CRCLK			25	51	
	CRADR1, CRADR0			16	32	
	TP1, TP0	All outputs		22	43	
ten	TP1, TP0	All outputs		22	42	ns
	$\overline{OED}$	Data out		13	27	
	$\overline{OEC}$	CNTRn		30	61	
tdis	TP1, TP0	All outputs		21	43	ns
	$\overline{OED}$	Data out		6	12	
	$\overline{OEC}$	CNTRn		6	12	

(1) Values are at Vcc = 5v, Vdd = Ov, T_A = 25°C
(2) Values are at Vcc = 4.5v, Vdd = Ov, T_A = 80°C
Max and Min values may not be 100% tested

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Asynchronous Communication Interface Adapter

S6551/S6551A

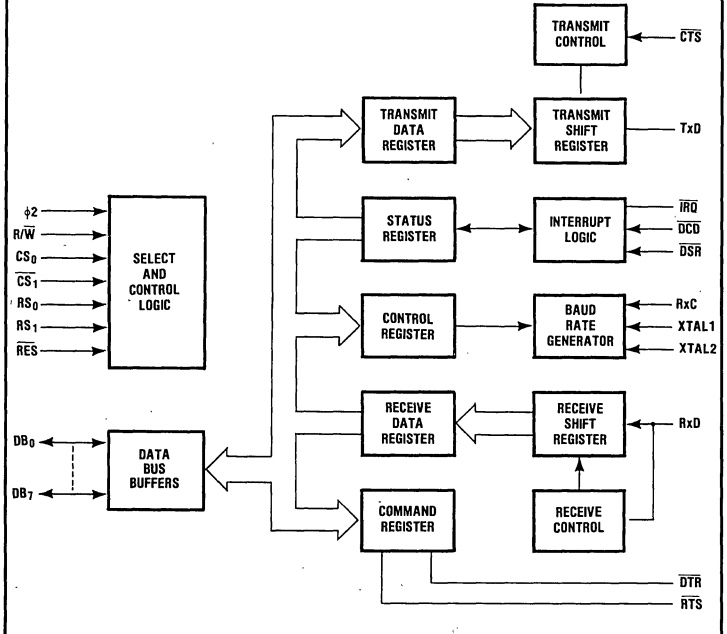
Features

- ☐ On-Chip Baud Rate Generator: 15 Programmable Baud Rates Derived from a Standard 1.8432MHz External Crystal (50 to 19,200 Baud)
- ☐ Programmable Interrupt and Status Register to Simplify Software Design
- ☐ Single + 5 Volt Power Supply
- ☐ Serial Echo Mode
- ☐ False Start Bit Detection
- ☐ 8-Bit Bi-Directional Data Bus for Direct Communication With the Microprocessor
- ☐ External 16X Clock Input for Non-Standard Baud Rates (Up to 125K Baud)
- ☐ Programmable: Word Lengths; Number of Stop Bits; and Parity Bit Generation and Detection
- ☐ Data Set and Modem Control Signals Provided
- ☐ Parity: (Odd, Even, None, Mark, Space)
- ☐ Full-Duplex or Half-Duplex Operation
- ☐ 5, 6, 7, 8 and 9-Bit Transmission

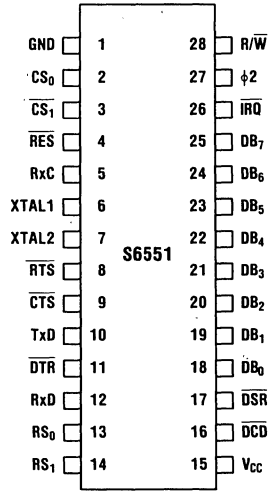
General Description

The S6551/S6551A is an Asynchronous Communication Adapter (ACIA) intended to provide interfacing for the microprocessors to serial communication data sets and modems. A unique feature is the inclusion of an on-chip programmable baud rate generator, with a crystal being the only external component required.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage V_{CC} ..... −0.3V to +7.0V
Input/Output Voltage V_{IN} ..... −0.3V to +7.0V
Operating Temperature Range T_A ..... 0°C to +70°C
Storage Temperature Range T_{stg} ..... −55°C to +150°C

All inputs contain protection circuitry to prevent damage to high static charges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Operating Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C, unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	2.0	—	V_{CC}	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
I_{IN}	Input Leakage Current: V_{IN} = 0 to 5V (ϕ2, R/W, RES, CS_0, CS_1, RS_0, RS_1, CTS, RxD, DCD, DSR)	—	±1.0	±2.5	μA
I_{TSI}	Input Leakage Current for High Impedance State (Three State)	—	±2.0	±10.0	μA
V_{OH}	Output High Voltage: I_{LOAD} = −100μA (DB_0-DB_7, TxD, RxC, RTS, DTR)	2.4	—	—	V
V_{OL}	Output Low Voltage: I_{LOAD} = 1.6mA (DB_0-DB_7, TxD, RxC, RTS, DTR, IRQ)	—	—	0.4	V
I_{OH}	Output High Current (Sourcing): V_{OH} = 2.4V (DB_0-DB_7, TxD, RxC, RTS, DTR)	—	—	−100	μA
I_{OL}	Output Low Current (Sinking): V_{OL} = 0.4V (DB_0-DB_7, TxD, RxC, RTS, DTR, IRQ)	—	—	1.6	mA
I_{OFF}	Output Leakage Current (Off State): V_{OUT} = 5V (IRQ)	—	1.0	10.0	μA
C_{CLK}	Clock Capacitance (ϕ2)	—	—	20	pF
C_{IN}	Input Capacitance (Except XTAL1 and XTAL2)	—	—	10	pF
C_{OUT}	Output Capacitance	—	—	10	pF
P_D	Power Dissipation (See Graph) (T_A = 0°C)	—	170	300	mW

Write Cycle (V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C, unless otherwise noted)

		S6551		S6551A		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
t_{CYC}	Cycle Time	1.0	—	0.5	—	μs
t_C	ϕ2 Pulse Width	400	—	200	—	ns
t_{ACW}	Address Set-Up Time	120	—	70	—	ns
t_{CAH}	Address Hold Time	0	—	0	—	ns
t_{WCW}	R/$\overline{W}$ Set-Up Time	120	—	70	—	ns
t_{CWH}	R/$\overline{W}$ Hold Time	0	—	0	—	ns
t_{DCW}	Data Bus Set-Up Time	150	—	60	—	ns
t_{HW}	Data Bus Hold Time	20	—	20	—	ns

(t_r and t_f = 10 to 30ns)

Figure 1. Power Dissipation vs. Temperature

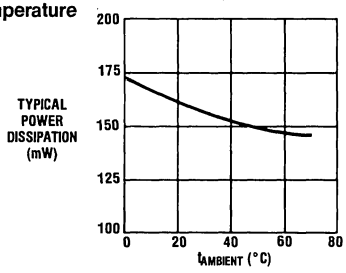
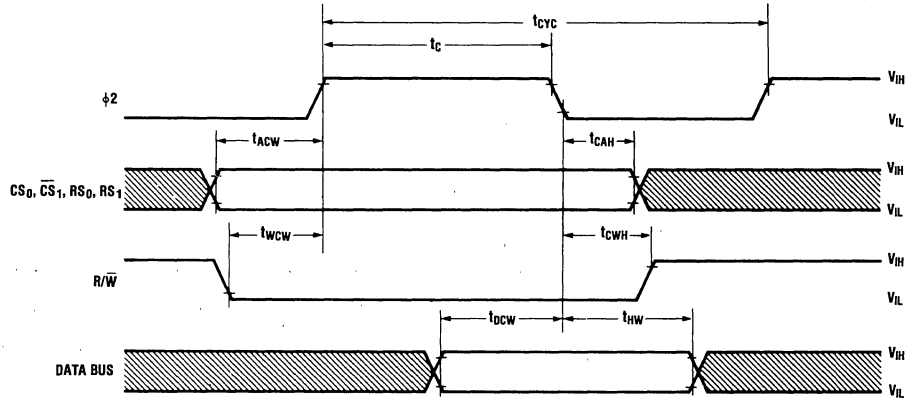


Figure 2. Write Timing Characteristics



Read Cycle (V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C, unless otherwise noted)

Symbol	Parameter	S6551		S6551A		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0.5	—	μs
t_C	$\phi 2$ Pulse Width	400	—	200	—	ns
t_{ACR}	Address Set-Up Time	120	—	70	—	ns
t_{CAR}	Address Hold Time	0	—	0	—	ns
t_{WCR}	R/$\overline{W}$ Set-Up Time	120	—	70	—	ns
t_{CDR}	Read Access Time (Valid Data)	—	200	—	150	ns
t_{HR}	Read Hold Time	20	—	20	—	ns
t_{CDA}	Bus Active Time (Invalid Data)	40	—	40	—	ns

Figure 5. Test Load for Data Bus (DB_0-DB_7), $\overline{TxD}$, $\overline{DTR}$, RTS Outputs

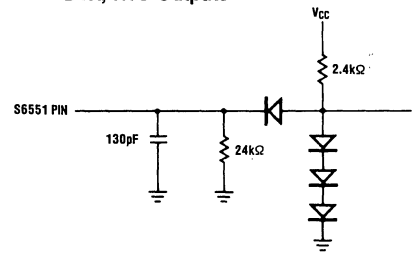


Figure 6a. Interrupt and Output Timing

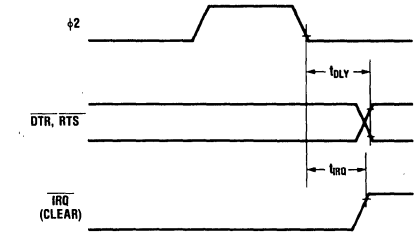


Figure 6b. Transmit Timing with External Clock

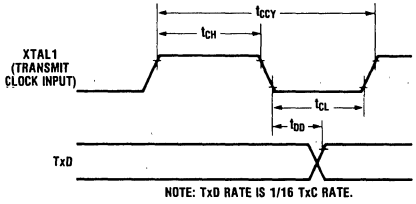
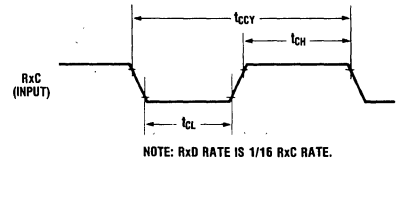


Figure 6c. Receive External Clock Timing



Pin Description

$\overline{RES}$ (Reset). During system initialization a low on the RES input will cause internal registers to be cleared.

ϕ2 Input Clock. The input clock is the system ϕ2 clock and is used to trigger all data transfers between the system microprocessor and the S6551.

R/$\overline{W}$ (Read/Write). The R/$\overline{W}$ is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the S6551. A low on the R/$\overline{W}$ pin allows a write to the S6551.

$\overline{IRQ}$ (Interrupt Request). The $\overline{IRQ}$ pin is an interrupt signal from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

DB_0-DB_7 (Data Bus). The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the S6551. These lines are bi-directional and are normally high-impedance except during Read cycles when selected.

CS_0-$\overline{CS_1}$ (Chip Selects). The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The S6551 is selected when CS_0 is high and $\overline{CS_1}$ is low.

RS_0, RS_1 (Register Selects). The two register select lines are normally connected to the processor address lines to allow the processor to select the various S6551 internal registers. The following table indicates the internal register select coding:

Table 1

RS_1	RS_0	WRITE	READ
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

The table shows that only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear the S6551 registers. The Programmed Reset is slightly different from the Hardware Reset ($\overline{RES}$) and these diferences are described in the individual register definitions.

Figure 3. Clock Generation

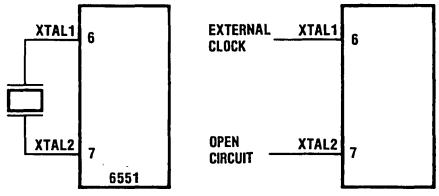
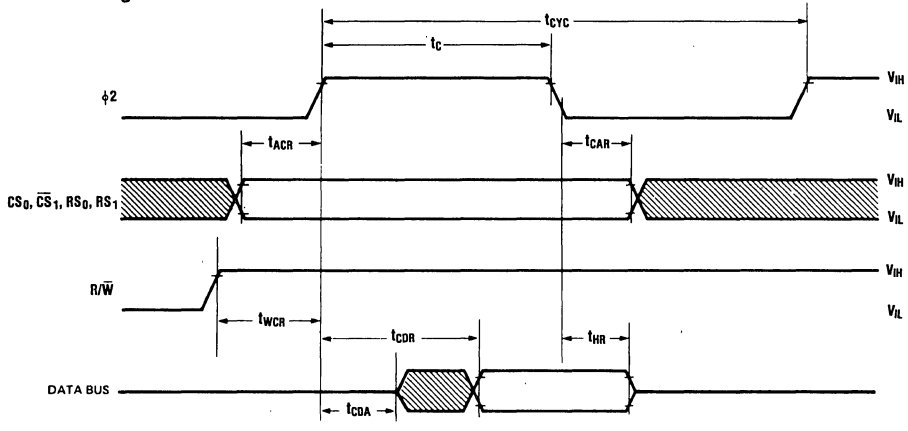


Figure 4. Read Timing Characteristics



Transmit/Receive Characteristics

Symbol	Parameter	S6551		S6551A		Unit
		Min.	Max.	Min.	Max.	
t_{CCY}	Transmit/Receive Clock Rate	400*	—	400*	—	ns
t_{CH}	Transmit/Receive Clock High Time	175	—	175	—	ns
t_{CL}	Transmit/Receive Low Time	175	—	175	—	ns
t_{DD}	EXTAL1 to TxD Propagation Delay	—	500	—	500	ns
t_{DLY}	Propagation Delay ($\overline{RTS}$, DTR)	—	500	—	500	ns
t_{IRQ}	$\overline{IRQ}$ Propagation Delay (Clear)	—	500	—	550	ns

(t_r and t_f = 10 to 30ns)

*The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times t_{CCY}}$

XTAL1, XTAL2 (Crystal Pins). These pins are normally directly connected to the external crystal (1.8432MHz M-Tron MP-2 recommended) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTAL1 pin, in which case the XTAL2 pin must float.

TxD (Transmit Data). The TxD output line is used to transfer serial NRZ (non-return-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected.

RxD (Receive Data). The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock. This selection is made by programming the Control Register.

RxC (Receive Clock). The RxC is a bi-directional pin which serves as either the receiver 16xclock input or the receiver 16xclock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

$\overline{\text{RTS}}$ (Request to Send). The $\overline{\text{RTS}}$ output pin is used to control the modem from the processor. The state of the $\overline{\text{RTS}}$ pin is determined by the contents of the Command Register.

CTS (Clear to Send). The $\overline{\text{CTS}}$ input pin is used to control the transmitter operation. The enable state is with $\overline{\text{CTS}}$ low. The transmitter is automatically disabled if $\overline{\text{CTS}}$ is high.

$\overline{\text{DTR}}$ (Data Terminal Ready). This output pin is used to indicate the status of the S6551 to the modem. A low on $\overline{\text{DTR}}$ indicates the S6551 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

$\overline{\text{DSR}}$ (Data Set Ready). The $\overline{\text{DSR}}$ input pin is used to indicate to the S6551 the status of the modem. A low indicates the "ready" state and a high, "not-ready." $\overline{\text{DSR}}$ is a high-impedance input and must not be a no-connect. If unused, it should be driven high or low, but not switched.

Note: If Command Register Bit 0 = 1 and a change of state on $\overline{\text{DSR}}$ occurs, $\overline{\text{IRQ}}$ will be set, and Status Register Bit 6 will reflect the new level. The state of $\overline{\text{DSR}}$ does not affect either Transmitter or Receiver operation.

$\overline{\text{DCD}}$ (Data Carrier Detect). The $\overline{\text{DCD}}$ input pin is used to indicate to the S6551 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not. $\overline{\text{DCD}}$, like $\overline{\text{DSR}}$, is a high-impedance input and must not be a no-connect.

Note: If Command Register Bit 0 = 1 and a change of state on $\overline{\text{DCD}}$ occurs, $\overline{\text{IRQ}}$ will be set, and Status Register Bit 5 will reflect the new level. The state of $\overline{\text{DCD}}$ does not affect Transmitter operation, but must be low for the Receiver to operate.

Figure 7. Transmitter/Receiver Clock Circuits

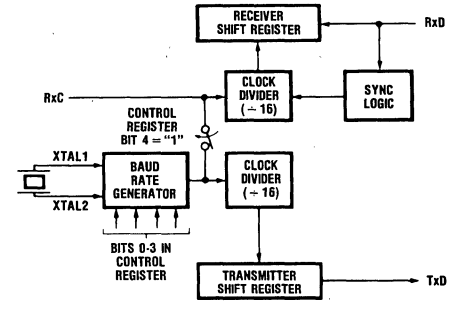


Figure 8. Control Register Format

CONTROL REGISTER

7	6	5	4	3	2	1	0

STOP BITS

0 = 1 STOP BIT
1 = 2 STOP BITS
1 STOP BIT IF WORD LENGTH = 8 BITS AND PARITY *
1½ STOP BITS IF WORD LENGTH = 5 BITS AND NO PARITY

WORD LENGTH

BIT 6	BIT 5	DATA WORD LENGTH
0	0	8
0	1	7
1	0	6
1	1	5

RECEIVER CLOCK SOURCE

0 = EXTERNAL RECEIVER CLOCK
1 = BAUD RATE GENERATOR

BAUD RATE GENERATOR

0	0	0	0	16x EXTERNAL CLOCK
0	0	0	1	50 BAUD
0	0	1	0	75
0	0	1	1	109.92
0	1	0	0	134.58
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	0
PROGRAM RESET	–	–	–	–	–	–	–	–

*THIS ALLOWS FOR 9-BIT TRANSMISSION (8 DATA BITS PLUS PARITY).

Internal Organization

The Transmitter/Receiver sections of the S6551 are depicted by the block diagram in Figure 7.

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then RxC becomes an output pin and can be used to slave other circuits to the S6551.

Control Register

The Control Register is used to select the desired mode for the S6551. The word length, number of stop bits, and clock controls are all determined by the Control Register, which is depicted in Figure 8.

Command Register

The Command Register is used to control Specific Transmit/Receive functions and is shown in Figure 9.

Figure 9. Command Register Format

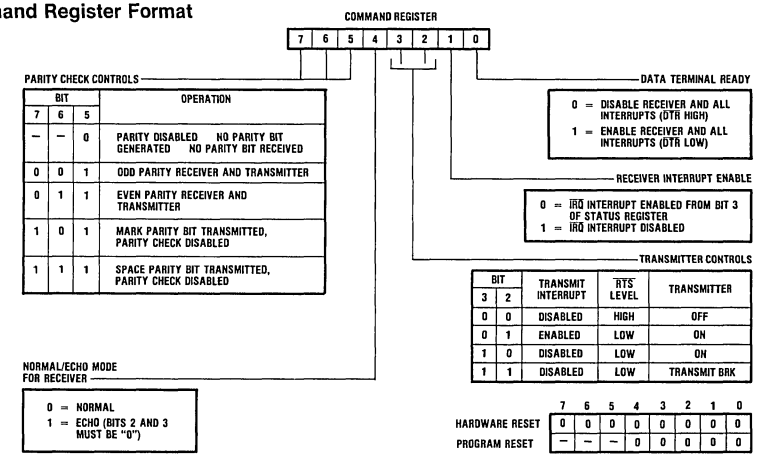
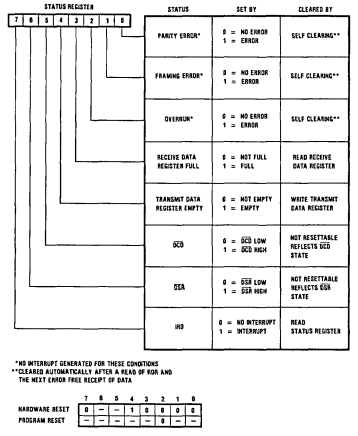


Figure 10. Status Register Format



Status Register

The Status Register is used to indicate to the processor the status of various S6551 functions and is outlined in Figure 10.

Transmit and Receive Data Registers

These registers are used as temporary data storage for the S6551 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

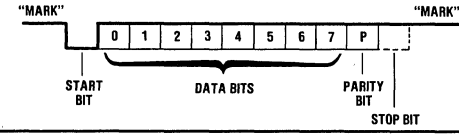
- ☐ Bit 0 is the leading bit to be transmitted.
- ☐ Unused data bits are the high-order bits and are "don't care" for transmission.

The Receive Data Register is characterized in a similar fashion:

- ☐ Bit 0 is the leading bit received.
- ☐ Unused data bits are the high-order bits and are "0" for the receiver.
- ☐ Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0".

Figure 11 illustrates a single transmitted or received data word, for the example of 8 data bits, parity, and 1 stop bit.

Figure 11. Serial Data Stream Example



GOULD
AMI Semiconductors

Asynchronous Communication Interface Adaptor

S65C51

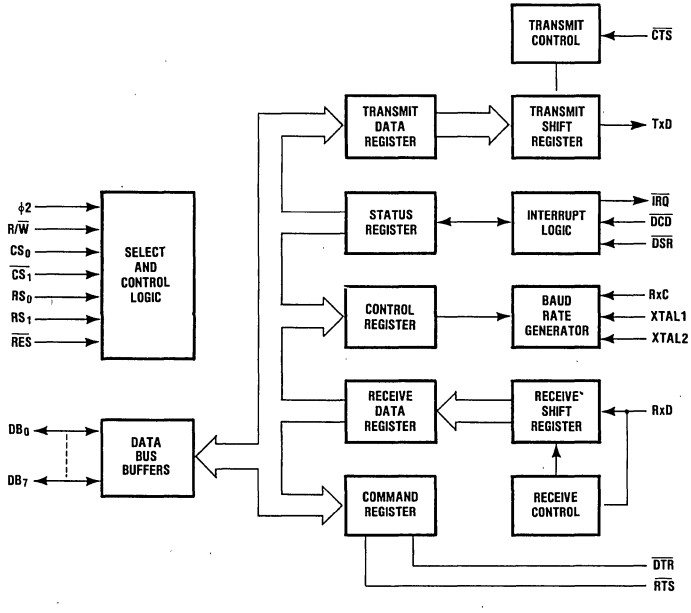
Features

- ☐ On-Chip Baud Rate Generator: 15 Programmable Baud Rates Derived from a Standard 1.8432MHz External Crystal (50 to 19,200 Baud)
- ☐ Programmable Interrupt and Status Register to Simplify Software Design
- ☐ Single +5 Volt Power Supply
- ☐ Serial Echo Mode
- ☐ False Start Bit Detection
- ☐ 8-Bit Bi-Directional Data Bus for Direct Communication With the Microprocessor
- ☐ External 16X Clock Input for Non-Standard Baud Rates (Up to 125K Baud)
- ☐ Programmable: Word Lengths; Number of Stop Bits; and Parity Bit Generation and Detection
- ☐ Data Set and Modem Control Signals Provided
- ☐ Parity: (Odd, Even, None, Mark, Space)
- ☐ Full-Duplex or Half-Duplex Operation
- ☐ 5, 6, 7, 8 and 9-Bit Transmission

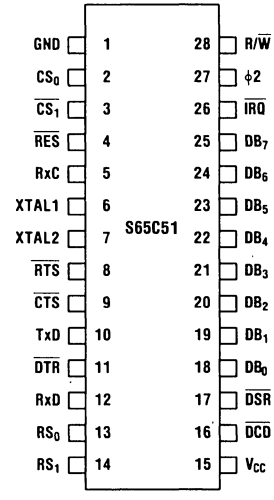
General Description

The S65C51 is a CMOS Asynchronous Communication Adapter (ACIA) intended to provide interfacing for the microprocessors to serial communication data sets and modems. A unique feature is the inclusion of an on-chip programmable baud rate generator, with a crystal being the only external component required.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage V_{CC}-V_{SS}	−0.3V to +7.0V
Voltage on any I/O Pin V_I	V_{SS} − 0.3V to V_{CC} + 0.3V
Current on any I/O Pin I_I	±10mA
Operating Temperature T_A	0°C to +70°C
Storage Temperature T_S	−55°C to +150°C
Power Dissipation Plastic	0.6W
Ceramic	1.0W

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

Electrical Operating Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Comments
V_I	Input Voltage	0		V_{CC}	V	
V_O	Output Voltage	0		V_{CC}	V	
T_A	Operating Temperature	0	25	70	°C	
f	Operating Frequency	0		2.0	MHz	

D.C. Characteristics—V_{CC} = 5.0V ± 5% V_{SS}/GND = 0V (All voltages are referenced to V_{SS}/GND.)

Inputs

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{CC1}	Quiescent Supply Current		2		μA	Outputs Unloaded
I_{CC}	Operating Supply Current		2		mA/MHz	Outputs Unloaded
V_{IH}	Input High Voltage XTL1	3.0		V_{CC}	V	
V_{IH}	OTHER INPUTS	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	0		0.8	V	
I_{IZ}	Input Leakage Current RxC, (D_0-D_7)			10	μA	V_{IN} = 0 to V_{CC}
V_{CC}	Other Inputs (Except XTL1)			2.5	μA	V_{IN} = 0 to V_{CC}
C_{IN}	Input Capacitance (D_0-D_7)		5.0		pF	
C_{IN}	Other Inputs (Except XTL1)		10.0		pF	

Outputs

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OH}	Output High Voltage (D0-7, TxD, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	2.4			V V	I_{OH} = −20μA I_{OH} = −100μA
V_{OL}	Output Leakage Current D0-7, TxD, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$			0.4	V	I_{OH} = 1.6mA
I_{OZ}	Output Leakage Current $\overline{IRQ}$ (OFF state)		10		μA	V_{OH} = V_{SS} to V_{CC}
C_O	Output Capacitance		5.0		pF	

Note: $V_H = V_{CC} - 0.1$ Volts

A.C. Test Conditions: output reference levels .8V and 2.4V, input pulse levels .8V to 2.2V, XTAL input levels .0V to 4.0V.

A.C. Characteristics—V_{CC} = 5.0V ± 5% V_{SS} = 0V (All voltages referenced to V_{SS}/GND. Test load Figures 2 and 3.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{CYC}	ϕ_2 Cycle Period	500			ns	See timing diagram 1, 3
t_C	ϕ_2 HIGH Pulse Width	200			ns	See timing diagram 1, 3
t_{AS}	Address Set-Up Time	70			ns	See timing diagram 1, 3
t_{AH}	Address Hold Time	0			ns	See timing diagram 1, 3
t_{DDR}	ϕ_2 to Valid Data Delay			150	ns	See timing diagram 3
t_{DHR}	Data Hold Time (Read)	10			ns	See timing diagram 3
t_{DSW}	Data Set-Up Time (Write)	60			ns	See timing diagram 1
t_{DHW}	Data Hold Time (Write)	10			ns	See timing diagram 1
t_{RWS}	Read/Write Set-up Time	70			ns	See timing diagram 3
t_{RWH}	Read/Write Hold time	0			ns	See timing diagram 1, 3
t_{ECP}	External TxD Clock Cycle Period	0.4			μs	See timing diagram 5b
t_{ECH}	External TxD Clock High Duration	175			ns	See timing diagram 5b
t_{ECL}	External TxD Clock Low Duration	175			ns	See timing diagram 5b
t_{TXDD}	External Clock to Valid Data Transmitted			500	ns	See timing diagram 5b
t_{DLY}	Propagation Delay from ϕ_2 ($\overline{RTS}$, $\overline{DTR}$)			500	ns	See timing diagram 5a
t_{IRQD}	$\overline{IRQ}$ Propagation Delay from ϕ_2 (CLEAR)			500	ns	See timing diagram 5a
t_{ECP}	External RxD Clock Cycle Period	0.4			μs	See timing diagram 5c
t_{ECH}	External RxD Clock High Duration	175			ns	See timing diagram 5c
t_{ECL}	External RxD Clock Low Duration	175			ns	See timing diagram 5c

Note: Rise and Fall times (t_R & t_F) are 10 to 30 ns

Figure 1. Write Timing Characteristics

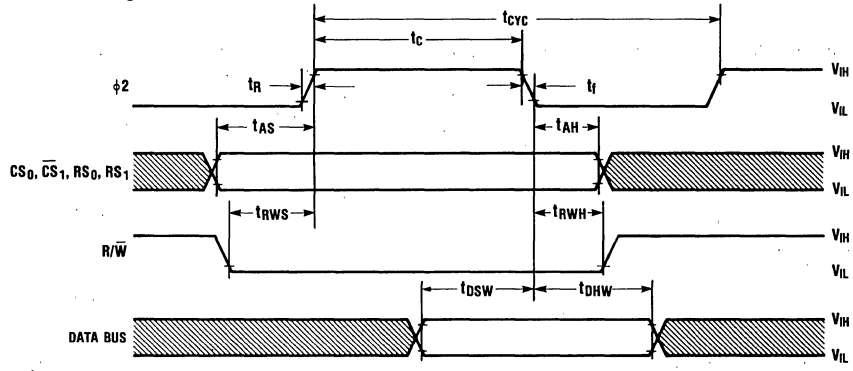


Figure 2. Clock Generation

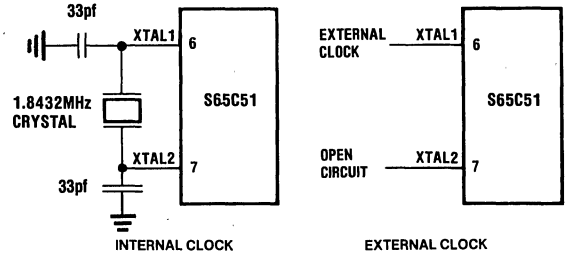


Figure 3. Read Timing Characteristics

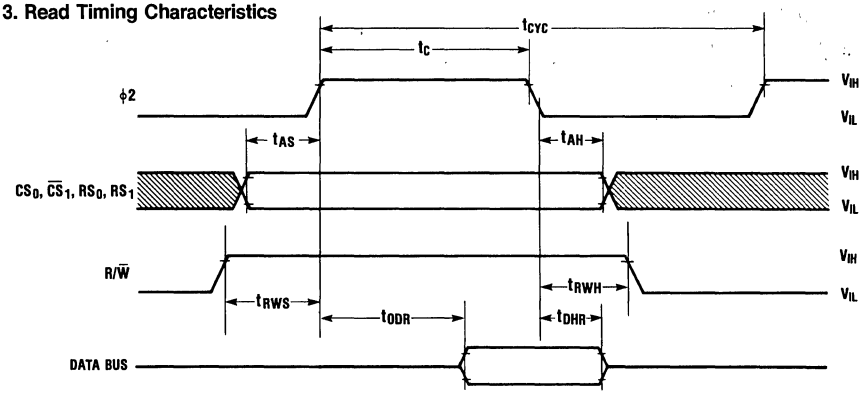


Figure 4a. Test Load for Data Bus (DB_0-DB_7), TxD, DTR, RTS Outputs

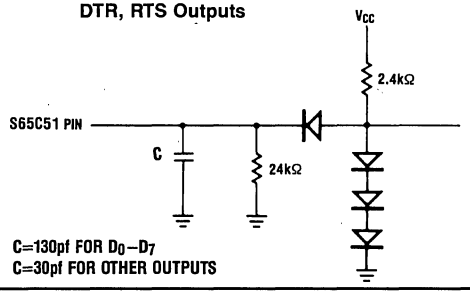


Figure 4b. Test Load for IRQ

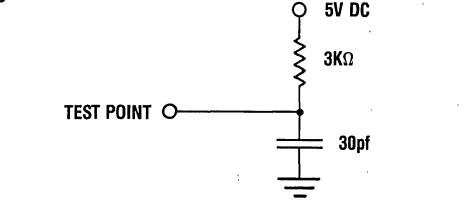


Figure 5a. Interrupt and Output Timing

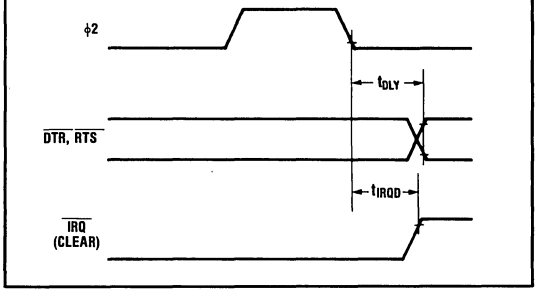


Figure 5b. Transmit Timing with External Clock

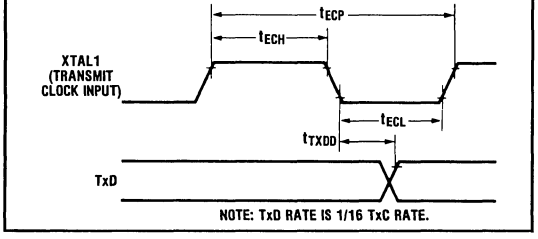
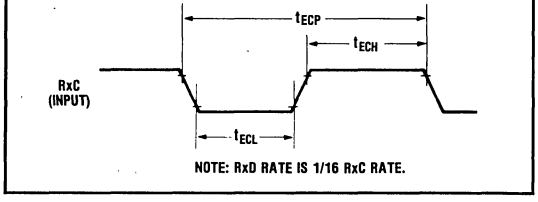


Figure 5c. Receive External Clock Timing



FUNCTIONAL DESCRIPTION

The S65C51 Asynchronous Communications Interface Adapter provides processor (μP) based systems with a full duplex serial interface. The μP port is directly compatible with 6800/6500 style bus architectures. Coupled with the Status Register, a powerful and flexible interrupt facility is included on the S65C51 to allow fast response from the μP to the ACIA.

The serial port provides signals which may be used to control a communication channel compatible to the EIA Standard RS-232 specification. An on-board baud rate generator allows 16 different baud rates, for data transmission and reception timing. All frequencies are derived from an external clock or crystal. The receive frequency may be received separately from the transmit frequency, allowing reception and transmission at independent speeds. Alternatively, the ACIA will produce a signal that is 16 times the baud rate, for use by a remote ACIA (Table 1 - RxC).

The format of the data word is programmable. The word length ranges from 5 to 9 bits (including parity). Parity can be odd, even or deselected altogether. The parity bit may also be forced high or low. Either 1, 1.5, or 2 stop bits may be added to the end of the serial data stream. For maintenance applications, the received data stream may be looped back onto the transmit data stream using echo mode operation.

SERIAL INTERFACE DESCRIPTION

Transmitted and Received Data

Data is transmitted from the ACIA on the TxD pin, and received on the RxD pin. The inactive state of either data channel (RxD or TxD) is a mark condition (logical high).

MICRO-PROCESSOR CIRCUITS

Table 1. Pin Description

Pin	Name	Description
1	V_{SS}	**Ground Input.** 0V.
2,3	CS0, $\overline{CS1}$	**Chip Select.** TTL inputs CS0=1 & CS1=0 select the chip for data transfer on the microprocessor bus. The direction of the transfer is determined by the state of the R/$\overline{W}$ pin.
4	$\overline{RES}$	**Hardware Reset.** $\overline{RES}$=0 to reset the chip. All internal registers will be cleared except bits 4, 5 and 6 in the Status Register (SR_b4, SR_b5 and SR_b6). SR_b4 is set, and SR_b5 and SR_b6 are unaffected.
5	RxC	**Receive Clock.** This is a bidirectional pin which serves as either the receiver 16x clock input or the receiver clock 16x output. The latter mode is selected if the internal baud rate generator is used as the receiver clock source.
6	XTAL1	**Clock Input.** For External Clock or Crystal connection. If clock is stopped, this input must be held high. XTAL1 has CMOS compatible thresholds (See figure 4).
7	XTAL0	**Clock connection.** This pin must be connected to the side of a crystal opposite to XTAL1, or left floating when using an external clock (See figure 4).
8	$\overline{RTS}$	**Request to Sent.** Output signal to the modem from the ACIA to control data transfers (See COMMAND REGISTER table 3).
9	$\overline{CTS}$	**Clear to send.** Input signal from the modem to the ACIA to control data transfers. When this input is held high, the transmitter is disabled.
10	TxD	**Transmit Data.** Serial data output in NRZ (Non Return to Zero) format.
11	$\overline{DTR}$	**Data Terminal Ready.** Output to the modem to indicate the ACIA status. $\overline{DTR}$=1 if ACIA is disabled (See COMMAND REGISTER table 3).
12	RxD	**Receive Data.** Serial data input NRZ (Non Return to Zero) format.
13, 14	RS0, RS1	**Register Select Inputs.** The state of these pins determines which internal register is connected to the data bus when the device is selected (see chip select description and Register Decode Table).
15	V_{DD}	**Positive Supply Input.** +5V.
16	$\overline{DCD}$	**Data Carrier Detect Input.** Status of carrier at the modem. [$\overline{DCD}$=0 if the carrier is detected]. The state of this pin is reflected by bit 5 of the Status Register (SR). If interrupts are enabled (Command Register (CR) bit 0=1) and the logical state $\overline{DCD}$ is changed, an interrupt will occur. When not used, this input should be connected to ground or to a logic high. The input state does not affect transmitter function but a logical low must be present for the receiver to operate.
17	$\overline{DSR}$	**Data Set Ready Input.** $\overline{DSR}$=0 if the modem is ready to perform a data transfer. The state of this pin is reflected by SR_b6. If interrupts are enabled (CR_b0=1), and the logical state of $\overline{DSR}$ is changed, an interrupt will occur. When not used, this input should be connected to ground or to a logic high. The input state does not affect the transmitter or the receiver function.
18-25	D_0-D_7	**Microprocessor Data Bus.** Bidirectional data bus which is TTL compatible. When the device is not selected these pins enter a high impedance state.
26	$\overline{IRQ}$	**Interrupt request to MPU.** (open drain output). When an interrupt occurs, this output is forced low until the interrupt is serviced (by reading the Status Register).
27	θ_2	**System clock input.** This synchronizes data transfer with the microprocessor.
28	R/$\overline{W}$	**Read/Write Input.** Controls the direction of data transfer between the microprocessor and the ACIA.

This type of data code is termed Non-Return to Zero (NRZ). Data transmitted or received by the S65C51 is always preceded by a "start bit." The Transmitter/Receiver sections of the S65C51 are depicted in Fig. 6.

The start bit is a space condition (logical low) which signifies the start of active data on the channel. The receiving ACIA also uses the start bit to optimize its sampling for the middle of the data bits that follow. Between received words, the ACIA samples the channel at 16x Baud rate. When a low is detected, the ACIA waits half a bit period before sampling again. This delay allows subsequent bits (sampled at the same frequency as the baud rate) to be sampled as far from the bit boundaries as possible. Noise or "glitch" immunity is also added by this mechanism. Low going pulses of less than 1/2 a bit period wide will not be mistaken for the start bit (the ACIA resumes the 16x sampling rate).

Data bits following the start bit are in ascending order, with the least significant bit (LSB) first, and the most significant bit (MSB) last. The MSB depends on the number of bits per word selected; the ACIA can be programmed for 5 bit, 6 bit, 7 bit or 8 bit data word transmission/reception. Each bit has a period equal to the reciprocal of the selected baud rate, which in turn is dependent on the clock source frequency (see table 4).

Parity sensing and generation can be chosen for odd parity, even parity or no parity. When parity is selected, the parity bit follows the MSB of the data word. For even parity, the condition of the parity bit will be such that there are an even number of marks when considering the data word

Table 2. Register Address Decoding

RS_1	RS_0	WRITE	READ
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

Figure 6. Transmitter/Receiver Clock Circuits

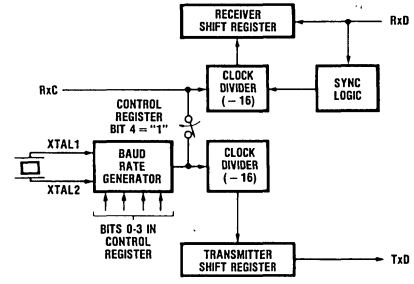


Table 3. Command Register Description

COMMAND REGISTER

7	6	5	4	3	2	1	0

PARITY CHECK CONTROLS

BIT 7	BIT 6	BIT 5	OPERATION
–	–	0	PARITY DISABLED NO PARITY BIT GENERATED NO PARITY BIT RECEIVED
0	0	1	ODD PARITY RECEIVER AND TRANSMITTER
0	1	1	EVEN PARITY RECEIVER AND TRANSMITTER
1	0	1	MARK PARITY BIT TRANSMITTED, PARITY CHECK DISABLED
1	1	1	SPACE PARITY BIT TRANSMITTED, PARITY CHECK DISABLED

DATA TERMINAL READY

0 = DISABLE RECEIVER AND ALL INTERRUPTS (DTR HIGH)
1 = ENABLE RECEIVER AND ALL INTERRUPTS (DTR LOW)

RECEIVER INTERRUPT ENABLE

0 = $\overline{IRQ}$ INTERRUPT ENABLED FROM BIT 3 OF STATUS REGISTER
1 = $\overline{IRQ}$ INTERRUPT DISABLED

TRANSMITTER CONTROLS

BIT 3	BIT 2	TRANSMIT INTERRUPT	$\overline{RTS}$ LEVEL	TRANSMITTER
0	0	DISABLED	HIGH	OFF
0	1	ENABLED	LOW	ON
1	0	DISABLED	LOW	ON
1	1	DISABLED	LOW	TRANSMIT BRK

NORMAL/ECHO MODE FOR RECEIVER

0 = NORMAL
1 = ECHO (BITS 2 AND 3 MUST BE "0")

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	0
PROGRAM RESET	–	–	–	0	0	0	0	0

and the parity bit. With odd parity, the condition of the parity bit will be such that there is an odd number of marks when considering the data word and the parity bit (both cases exclude the start and stop bits).

Transmit and Receive Clocks

The signals used by the ACIA for transmit/receive timing are found on 3 pins: XTAL0, XTAL1 and RxC. XTAL1 and XTAL0 are the input and output, respectively, of a crystal oscillator circuit. The crystal can be connected to these pins as seen in figure 7. This oscillator circuit drives the internal baud rate generator, which divides the square wave output of the oscillator by the divisor selected (see table 4). If a crystal is not used, an external clock may drive the oscillator input while the oscillator output is left floating. If the clock is stopped (device still powered), the oscillator input should be held to a logical high.

The clock for the receiver may be taken from 1 of 2 sources: the output of the internal baud rate generator, or from an external clock input on the RxC pin. In the latter case, the baud rate is 1/16th of the external clock. If the source of receiver timing is the internal baud rate generator, RxC becomes an output and sources a clock 16 times (16x) the baud rate (for driving remote ACIAs).

Control Signals

These signals are compatible with the RS-232C modem control circuits. The signals are the Request To Send ($\overline{RTS}$), Data Terminal Ready ($\overline{DTR}$) outputs and the Clear To Send ($\overline{CTS}$), Data Set Ready ($\overline{DSR}$) and the Data Carrier Detect ($\overline{DCD}$) inputs. Note that the ACIA is viewed as the Data Termination Equipment (DTE) as opposed to the Data Communication Equipment (DCE) when referencing the RS-232C specification.

Request To Send. $\overline{RTS}$ is used to indicate to the DCE that it should assume the data channel transmit mode. The state of this output is controlled by bits 2 and 3 of the Command Register ($COMR_b2$ and $COMR_b3$, see table 3). When it is high (not asserted, or in other words, "negated") the ACIA's transmitter is disabled.

Data Terminal Ready. The $\overline{DTR}$ signal indicates to the DCE that the ACIA is ready for communication. This output is asserted when $COMR_b0$ is set.

Clear To Send. The $\overline{CTS}$ signal from the DCE tells the ACIA that the DCE is prepared to accept data to pass on to the remote end of the communication channel. When this signal is not asserted, the transmitter of the ACIA is disabled. If the ACIA is in the middle of transmitting a data

Table 4. Control Register Description

CONTROL REGISTER

7	6	5	4	3	2	1	0

STOP BITS

0 = 1 STOP BIT
1 = 2 STOP BITS
1 STOP BIT IF WORD LENGTH = 8 BITS AND PARITY *
1½ STOP BITS IF WORD LENGTH = 5 BITS AND NO PARITY

WORD LENGTH

BIT 6	BIT 5	DATA WORD LENGTH
0	0	8
0	1	7
1	0	6
1	1	5

RECEIVER CLOCK SOURCE

0 = EXTERNAL RECEIVER CLOCK
1 = BAUD RATE GENERATOR

BAUD RATE GENERATOR

3	2	1	0	16x EXTERNAL CLOCK	BAUD
0	0	0	0		
0	0	0	1	50	
0	0	1	0	75	
0	0	1	1	109.92	
0	1	0	0	134.58	
0	1	0	1	150	
0	1	1	0	300	
0	1	1	1	600	
1	0	0	0	1200	
1	0	0	1	1800	
1	0	1	0	2400	
1	0	1	1	3600	
1	1	0	0	4800	
1	1	0	1	7200	
1	1	1	0	9600	
1	1	1	1	19,200	

*THIS ALLOWS FOR 9-BIT TRANSMISSION (8 DATA BITS PLUS PARITY).

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	0
PROGRAM RESET	–	–	–	–	–	–	–	–

Table 5. Status Register Description

STATUS REGISTER

7	6	5	4	3	2	1	0

STATUS	SET BY	CLEARED BY
PARITY ERROR*	0 = NO ERROR 1 = ERROR	SELF CLEARING**
FRAMING ERROR*	0 = NO ERROR 1 = ERROR	SELF CLEARING**
OVERRUN*	0 = NO ERROR 1 = ERROR	SELF CLEARING**
RECEIVE DATA REGISTER FULL	0 = NOT FULL 1 = FULL	READ RECEIVE DATA REGISTER
TRANSMIT DATA REGISTER EMPTY	0 = NOT EMPTY 1 = EMPTY	WRITE TRANSMIT DATA REGISTER
$\overline{DCD}$	0 = $\overline{DCD}$ LOW 1 = $\overline{DCD}$ HIGH	NOT RESETTABLE REFLECTS $\overline{DCD}$ STATE
$\overline{DSR}$	0 = $\overline{DSR}$ LOW 1 = $\overline{DSR}$ HIGH	NOT RESETTABLE REFLECTS $\overline{DSR}$ STATE
IRQ	0 = NO INTERRUPT 1 = INTERRUPT	READ STATUS REGISTER

*NO INTERRUPT GENERATED FOR THESE CONDITIONS.
**CLEARED AUTOMATICALLY AFTER A READ OF RDR AND THE NEXT ERROR FREE RECEIPT OF DATA.

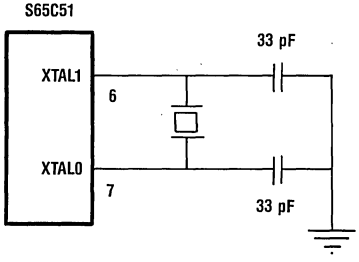
	7	6	5	4	3	2	1	0
HARDWARE RESET	0	–	–	1	0	0	0	0
PROGRAM RESET	–	–	–	–	–	0	–	–

Table 6. Crystal Specification

Characteristics	Spec.
Temperature stability @ −45 to +85°C	±0.01%
Frequency* (MHz)	1.8432
Frequency tolerance* (±%)	0.02
Resonance mode*	parallel
Equivalent resistance* (ohms)	400 max.
Drive level* (mW)	2
Shunt capacitance* (pF)	7 max.
Load capacitance* (pF)	16.5 typ.
Oscillation mode*	

* characteristics at 25°C ±2°C

Figure 7. Suggested Crystal Connection



word when $\overline{CTS}$ is negated, the TxD channel goes immediately to a mark condition. The data word being transmitted at the time is lost, but the character (if any) in the Transmit Data Register (TDR) is not (see register description). As soon as $\overline{CTS}$ is asserted, this data word will be transmitted, if the transmitter is still enabled internally (see figure 11).

Data Set Ready. The $\overline{DSR}$ signal from the DCE tells the ACIA that the DCE is ready to operate. A transition on this pin can cause an interrupt (if interrupts are enabled) and the state of the pin is reflected in the state of SR_b6. Transitions that follow will not affect the status bit until after the μP has serviced the first interrupt (read the SR). At that point the SR will again reflect the current level of the $\overline{DSR}$ input, and an interrupt will occur again if it has changed. Transmitter and receiver operation is not affected by the level of this pin.

Data Carrier Detect. The $\overline{DCD}$ signal from the DCE indicates to the ACIA that the received signal is within specified limits. When $\overline{DCD}$ is not true, the receiver of the ACIA will be disabled and the data being shifted in at that moment is lost. A transition on this pin, like the $\overline{DSR}$ input, causes an interrupt. Subsequent transitions will not affect the status bit until the first interrupt is serviced. If the pin has changed since the first occurred and before it was serviced, another interrupt will occur. An even number of level changes on $\overline{DSR}$ and $\overline{DCD}$, before the first interrupt has been serviced, will not cause another interrupt. This is because the status bits will be at the same logic level that caused the original interrupt.

REGISTER DESCRIPTION

The S65C51 contains 7 registers, 5 that are visible to the μP. These registers are: the Transmit Shift Register (TSR, not available to μP), the Receive Shift Register (RSR, not available to μP), the Transmit Data Register (TDR), the Receive Data Register (RDR), the Status Register (SR), the Command Register (COMR), and the Control Register (CR). One of the 5 latter registers is visible to the μP

the μP when the chip selects (CS0, SC1) are asserted and the E clock is true (high); the register chosen by the state of the register selects (RS0, RS1). The direction of μP bus transfer is determined by the state of the R/$\overline{W}$ signal (a high indicates a read of the contents of the register, a low a write to a register). When the SR is written to (the data written doesn't matter) a software reset will occur. For a comparison between the effect of a hardware reset and a software reset, see table 2.

Transmit Data Register

The Transmit Data Register (TDR), in conjunction with the Transmit Shift Register, is used to place data on the transmit channel (TxD). If no word is being transmitted, a data word written to the TDR is immediately transferred into the TSR to be shifted out. A start bit precedes the data on the TxD channel; parity is added to the end of the word as needed (after the valid MSB is shifted out); and 1, 1.5, or 2 stop bits follow to end the transmitted information. If the ACIA is programmed to send a data word that is less than 8 bits in length (5, 6 or 7 bits), the extra bits in the data word are ignored.

While the TSR is occupied shifting out active data onto TxD (including the bit periods for the transmission of parity bits and stop bits), information written to TDR will be latched and held. When the last stop bit of the previous word is finished, the ACIA will transfer the data word in the TDR into the TSR and transmit it. If the TDR is written to more than once while information is being transmitted on TxD, the data word in TDR will be overwritten and retain the data associated with the last write.

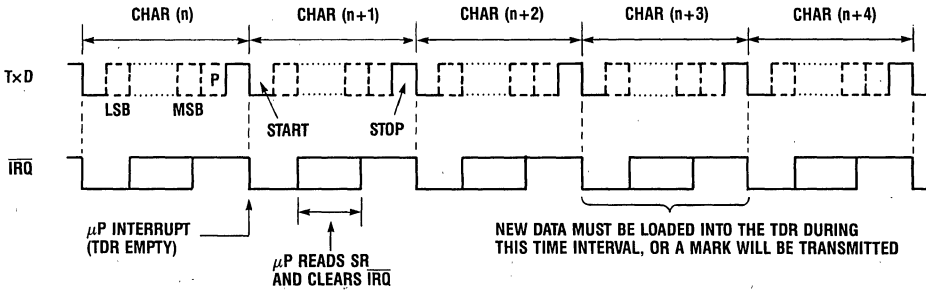
If transmit interrupts are enabled, when the TDR is empty an interrupt will occur and SR_b4 will be set (SR_b4 will be set even if interrupts are disabled). This coincides with the beginning of the start bit for the data just transferred to the TSR. The interrupt must be serviced to be removed (by reading SR), but SR_b4 may only be cleared by a write to the TDR. If the interrupt is serviced but TDR is not written to, another interrupt will occur at the next word boundary (word boundaries are referenced to the start of the last transmitted word, and occur every full word period after the end of the word. This timing is reset by a new transmission because, if TxD is idle the new word is transmitted immediately - see figures 8 & 10).

Receive Data Register

Data on the receive channel (RxD) is stripped of the overhead bits (start, parity and stop) by the ACIA and shifted into the Receive Shift Register (RSR). When a full data word has been received (depending on the programmed length), the contents of the RSR are transferred into the Receive Data Register (RDR). If receive interrupts are enabled, this transfer will cause an interrupt to occur and SR_b3 to be set (SR_b3 is set even when interrupts are disabled). The interrupt actually occurs about 9/16 through the last stop bit. As with the TDR, the interrupt is removed by reading SR and SR_b3 is cleared by reading the RDR.

If $\overline{DCD}$ is not asserted, the RSR is immediately disabled and any word being received at the time is lost. If the receive circuitry is disabled through the Command Register, a data word in the process of being received will be finished before the RSR is disabled.

Figure 8. Contiuous Data Transmit



When a continuous break character is received, the first character period will look like a data word of all zeroes and a framing error. If interrupts are enabled, an interrupt will occur. Thereafter the receiver will be disabled until a stop bit is received, so no more interrupts will occur. It is possible that the μP could interpret a data word made up of zeroes, without a stop bit in the correct position, as a received break condition (see figure 9 and 15).

Command Register

The Command Register (COMR) determines the type of parity used in the transmitted word, and the type of parity checked for in the received word. Parity is controlled by COM_b5 - COM_b7 (see table 3). The bit position normally occupied by a parity bit may be forced to a mark or a space if required.

$COMR_b4$ enables or disables echo mode (for echo to be enabled, COM_b2 and COM_b3 must both be 0). When in echo mode, the ACIA's receive circuitry is still operational, but data written to the TDR will not be transmitted until echo mode is disabled and the transmitter is reenabled. $\overline{RTS}$ is asserted in echo mode, even though it is not programmed to be active by $COMR_b3$ and $COMR_b2$.

When data is received on RxD (the receiver must be enabled internally and $\overline{DCD}$ true) it is transmitted 1/2 bit period after it has been received. Interrupts occur just as they would when initiated by any received data (if interrupts are enabled). If echo mode is disabled during reception of a character, transmission on TxD stops immediately and $\overline{RTS}$ is negated. The word continues to be shifted into the RSR if it is still enabled (see figures 13 and 14).

$COMR_b2$ and $COMR_b3$ control the transmit circuitry, disabling or enabling the transmitter and $\overline{RTS}$, and disabling or enabling transmit interrupts. If continuous break mode is selected during the transmission of a data word, the current word will be transmitted and the break condition will begin immediately after. Transmit interrupts are automatically disabled during the transmit break condition.

The break condition will last for at least one character period, so if the transmitter is enabled immediately after the break condition has been set (assuming the ACIA has begun to transmit the break) the transmitter will not return to normal operation until after one character period of break. When the break mode is removed, one stop bit will be placed on TxD before the transmission of the next word.

$COMR_b1$ enables or disables receiver interrupts and $COMR_b0$ enables or disables the receiver circuitry, all interrupts and the $\overline{DTR}$ signal. See figure 4b.

Control Register

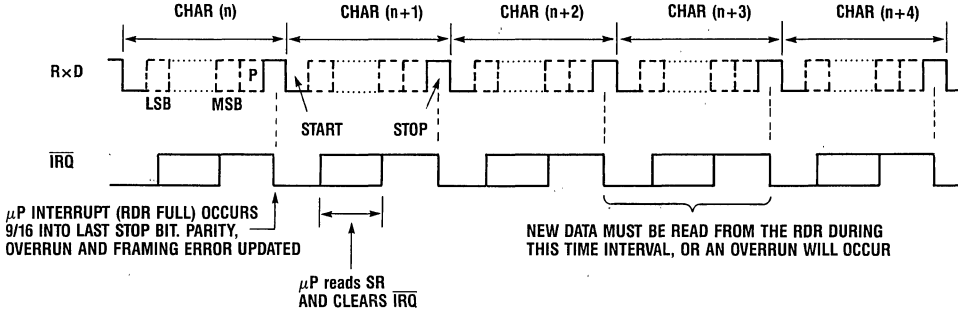
The Control Register (CR) determines the number of stop bits in transmitted and received information; the length of the word; the source of the receive and transmit timing and the divisor used by the baud rate generator.

Note that when the receiver clock source is chosen such that RxC is an input, the setting of the baud rate generator has no effect on the receiver speed. See table 4.

Status Register

The Status Register (SR) performs a "housekeeping" function for the ACIA. The SR contains several error bits,

Figure 9. Contiuous Data Receive



MICRO-PROCESSOR CIRCUITS

2 bits to display the state of the transmit and receive registers, 2 bits used for modem status and 1 bit for displaying interrupt status.

SR_b7 is the inverse of the $\overline{IRQ}$ signal. When an interrupt is active, SR_b7 is set. It is cleared by reading the SR.

SR_b5 and SR_b6 reflect the state of the $\overline{DCD}$ pin and the $\overline{DSR}$ pin respectively. These bits cannot be reset or cleared by the μP.

SR_b3 is the Receive Data Register full bit and SR_b4 is the Transmit Data Register Empty bit. These bits have been described fully in the TDR and RDR sections.

The 3 LSB bits in the SR are error bits, set when a specific error condition occurs. These bits may only be cleared if the RDR is read and a word is received without an error (the error that occurred previously). SR_b0 is the parity error detect bit. When this bit is set, it indicates that parity is enabled and the level of the parity bit received by the ACIA was incorrect. SR_b1 is the Framing error detect bit. If a word is received that does not have a stop bit where expected, the framing error bit will be set.

SR_b2 is the Overrun error bit. This bit is set if a data word is received without the previous word having been read. The word in the RDR is maintained until it is read, so subsequent words in the RSR, that result in an overrun condition, are lost. Interrupts continue to occur with each data word received in the RSR as normal (see figure 12). When an overrun occurs in echo mode, the TxD channel goes to a mark until the first start bit after the RDR is read by the μP.

Suggested sequence for reading SR after interrupt

1 **Read Status Register.**
This operation automatically clears SR_b7 and negates the $\overline{IRQ}$ signal. Subsequent transitions on $\overline{DSR}$ and $\overline{DCD}$ will cause another interrupt.
2 **Check SR_b7**
If not set, source was not the ACIA.
3 **Check SR_b6 and SR_b5**
These must be compared to their previous levels, which must be stored externally by the processor. If they are both a logical low (modem on-line) and they are unchanged then the remaining bits must be checked.
4 **Check SR_b3**
Is RDR full?
5 **Check SRb0, SRb1, SRb2**
Only if RDR is set.
6 **Check SR_b4**
Is TDR empty? Check even if RDR is full when in full duplex operation.
7 If none of the above occurred, $\overline{CTS}$ must have been negated.

Figure 10. TDR not loaded by Processor

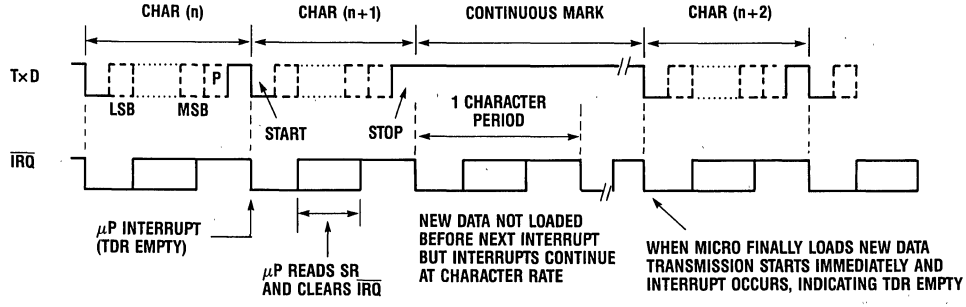


Figure 11. Effect of $\overline{CTS}$ on TxD

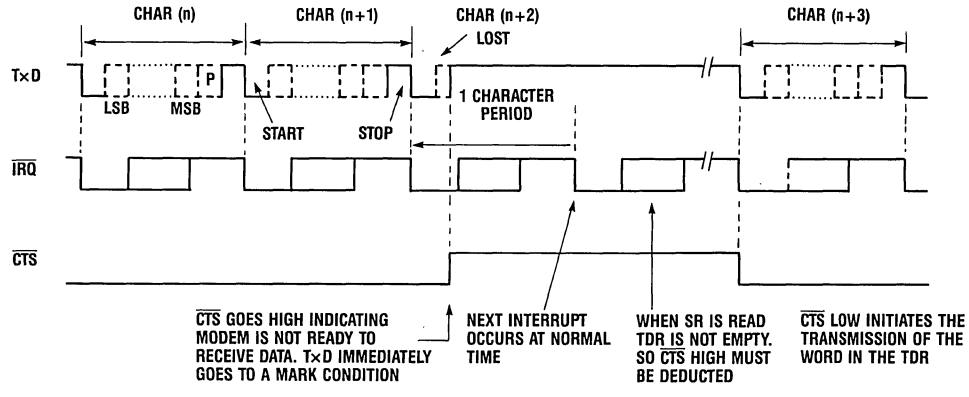


Figure 12. Effect of overrun on receiver

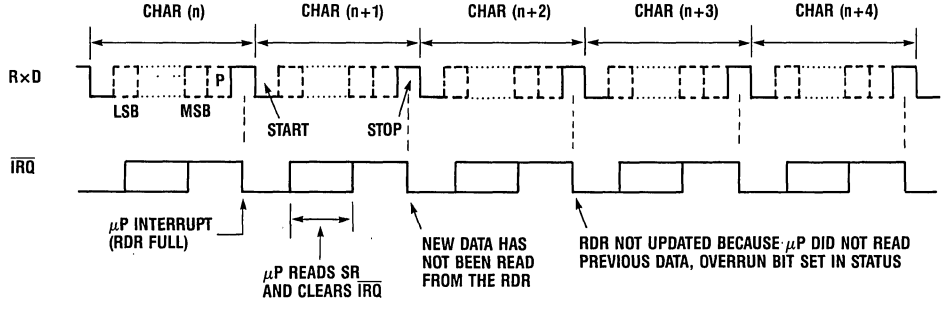


Figure 13. Effect of $\overline{CTS}$ on Echo mode operation

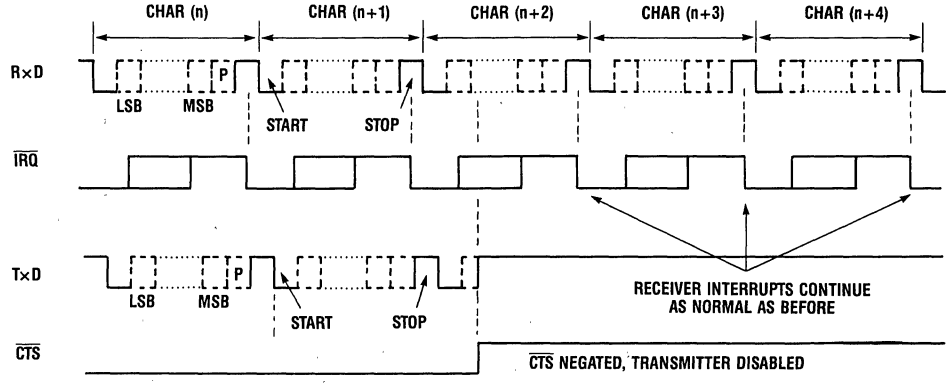


Figure 14. Overrun in Echo mode

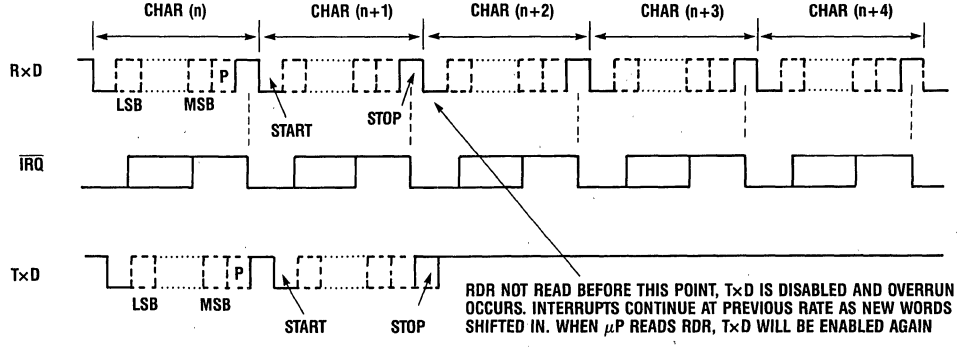
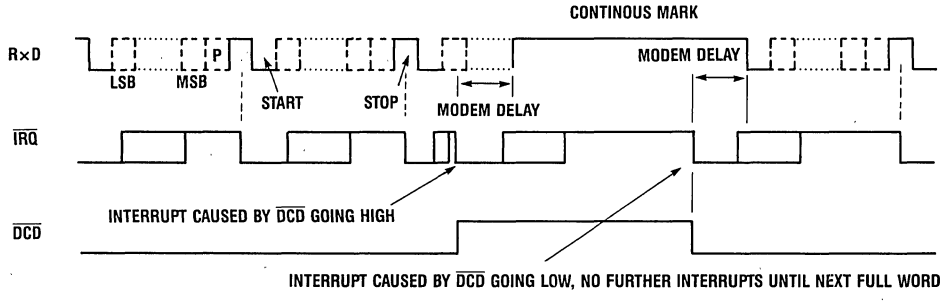
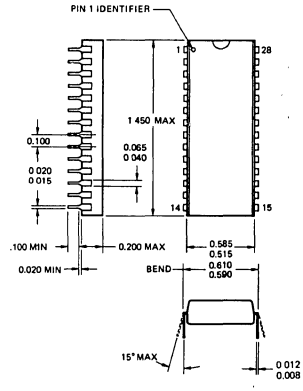


Figure 15. Effect of $\overline{DCD}$ on receiver

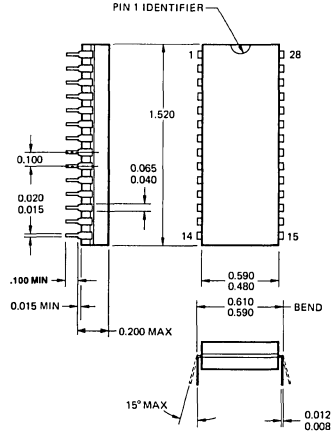


Package Outlines

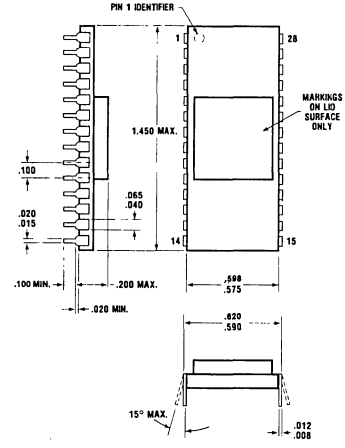
28-Lead Plastic



28-Lead Cerdip



28-Lead Ceramic



GOULD

AMI Semiconductors

CRT Controller

S6845E

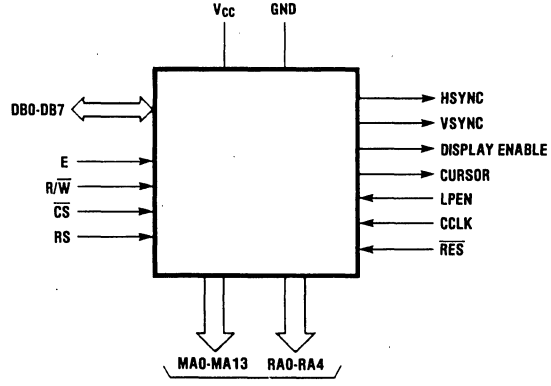
Features

- Single +5 volt (±5%) power supply.
- Alphanumeric and limited graphics capabilities.
- Fully programmable display (rows, columns, blanking, etc.).
- Interlaced or non-interlaced scan.
- 50/60 Hz operation.
- Fully programmable cursor.
- External light pen capability.
- Capable of addressing up to 16K character Video Display RAM.
- No DMA required
- Pin-compatible with MC6845R.
- Row/Column or straight-binary addressing for Video Display RAM.
- Video Display RAM may be configured as part of microprocessor memory field or independently slaved to 6845.
- Internal status register.
- 3.7 MHz Character Clock.
- Transparent Address Mode.

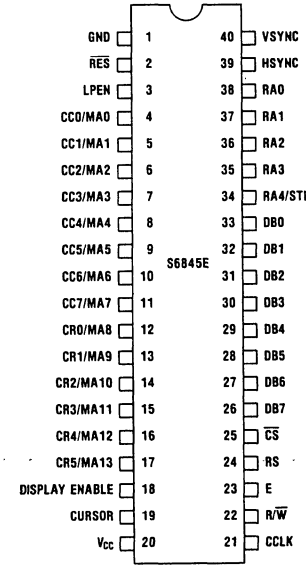
Description

The S6845E is a CRT Controller intended to provide capability for interfacing any 8 or 16 bit microprocessor family to CRT or TV-type raster scan displays. A unique feature is the inclusion of several modes of operation, so that the system designer can configure the system with a wide assortment of techniques.

Interface Diagram



Pin Configuration



Absolute Maximum Ratings*

Supply Voltage, V_{CC}	−0.3V to +7.0V
Input/Output Voltage, V_{IN}	−0.3V to +7.0V
Operating Temperature, T_{OP}	0°C to 70°C
Storage Temperature, T_{STG}	−55°C to 150°C

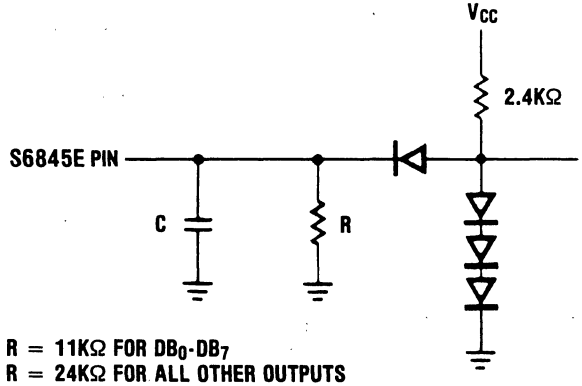
*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics: V_{CC} = +5.0 ± 5%, T_A = 0°C to 70°C, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	−0.3		0.8	V	
I_{IN}	Input Leakage (φ2, R/$\overline{W}$, RES, CS, RS, LPEN, CCLK)			2.5	μA	
I_{TSI}	Three-State Input Leakage (DB0-DB7) V_{IN} = 0.4 to 2.4V			±10.0	μA	
V_{OH}	Output High Voltage I_{LOAD} = −205μA (DB0-DB7) I_{LOAD} = −100μA (all others)	2.4			V	
V_{OL}	Output Low Voltage I_{LOAD} = 1.6mA			0.4	V	
P_D	Power Dissipation		325	650	mW	
C_{IN}	Input Capacitance φ2, R/$\overline{W}$, RES, CS, RS, LPEN, CCLK DB0-DB7			10.0 12.5	pF pF	
C_{OUT}	Output Capacitance			10.0	pF	

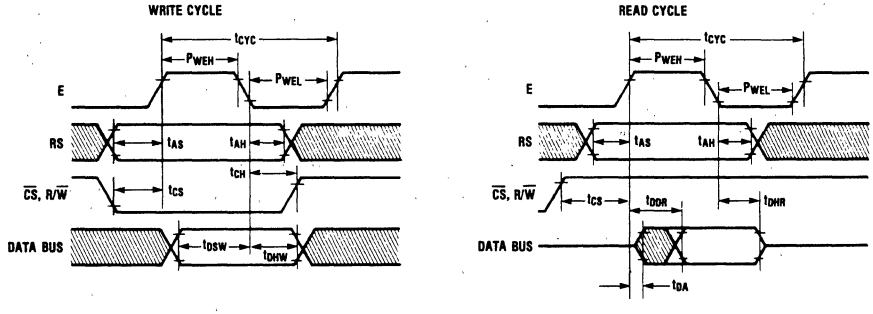
All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

Test Load



R = 11KΩ FOR DB_0-DB_7
R = 24KΩ FOR ALL OTHER OUTPUTS
C = 130 pF TOTAL FOR D_0-D_7
C = 30 pF ALL OTHER OUTPUTS

MPU Bus Interface Characteristics



Write Cycle (V_{CC} = 5.0V ± 5%, T_A = 0°C to + 70°C, unless otherwise noted)

Symbol	Parameter	S6845E Min.	S6845E Max.	S6845EA Min.	S6845EA Max.	Unit
t_{CYC}	Cycle Time	1.0	—	0.5	—	µs
P_{WEH}	E Pulse Width, High	440	—	200	—	ns
P_{WEL}	E Pulse Width, Low	420	—	190	—	ns
t_{AS}	Address Set-Up Time	80	—	40	—	ns
t_{AH}	Address Hold Time	0	—	0	—	ns
t_{CS}	R/$\overline{W}$, $\overline{CS}$ Set-Up Time	80	—	40	—	ns
t_{CH}	R/$\overline{W}$, $\overline{CS}$ Hold Time	0	—	0	—	ns
t_{DSW}	Data Bus Set-Up Time	165	—	60	—	ns
t_{DHW}	Data Bus Hold Time	10	—	10	—	ns

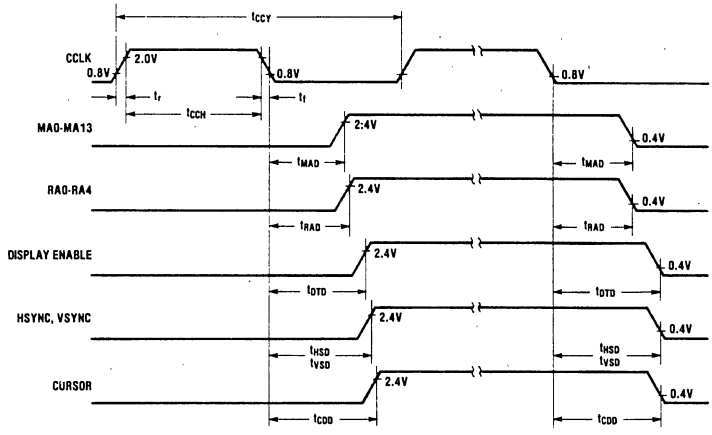
(t_r and t_f = 10 to 30 ns)

Read Cycle (V_{CC} = 5.0V ± 5%, T_A = 0°C to + 70°C, unless otherwise noted)

Symbol	Parameter	S6845E Min.	S6845E Max.	S6845EA Min.	S6845EA Max.	Unit
t_{CYC}	Cycle Time	1.0	—	0.5	—	µs
P_{WEH}	ϕ2 Pulse Width, High	440	—	200	—	ns
P_{WEL}	ϕ Pulse Width, Low	420	—	190	—	ns
t_{AS}	Address Set-Up Time	80	—	40	—	ns
t_{AH}	Address Hold Time	0	—	0	—	ns
t_{CS}	R/W, CS Set-Up Time	80	—	40	—	ns
t_{DDR}	Read Access Time (Valid Data)	—	290	—	150	ns
t_{DHR}	Read Hold Time	10	—	10	—	ns
t_{DA}	Data Bus Active Time (Invalid Data)	20	60	20	60	ns
t_{TAD}	MA0-MA13 Switching Delay (Refer to Figure Trans Addressing) on page 4	100 typ.	160	100 typ.	160	ns

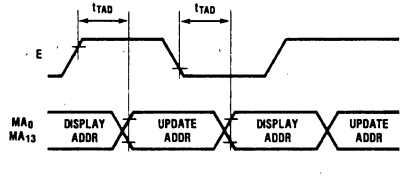
(t_r and t_f = 10 to 30 ns)

Memory and Video Interface Characteristics (V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

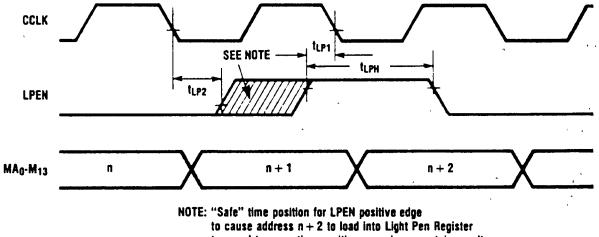


Symbol	Parameter	Min.	Typ.	Max.	Units
t_{CCH}	Minimum Clock Pulse Width, High	130			ns
t_{CCY}	Clock Frequency			3.7	MHz
t_r, t_f	Rise and Fall Time for Clock Input			20	ns
t_{MAD}	Memory Address Delay Time		100	160	ns
t_{RAD}	Raster Address Delay Time		100	160	ns
t_{DTD}	Display Timing Delay Time		160	250	ns
t_{HSD}	Horizontal Sync Delay Time		160	250	ns
t_{VSD}	Vertical Sync Delay Time		160	250	ns
t_{CDD}	Cursor Display Timing Delay Time		160	250	ns

Transparent Addressing (ϕ1/ϕ2 Interleading)



Light Pen Strobe Timing



NOTE: "Safe" time position for LPEN positive edge to cause address n + 2 to load into Light Pen Register. t_{LP2} and t_{LP1} are time positions causing uncertain results.

Symbol	Parameter	S6845E Min.	S6845E Max.	S6845EA Min.	S6845EA Max.	Unit
t_{LPH}	LPEN Strobe Width	100	—	100	—	ns
t_{LP1}	LPEN to CCLK Delay	—	120	—	120	ns
t_{LP2}	CCLK to LPEN Delay		0	—	0	ns

t_r and t_f = 20ns (max.)

MPU Interface Signal Description

E (Enable)

The enable signal is the system input and is used to trigger all data transfers between the system microprocessor and the S6845. Since there is no maximum limit to the allowable E cycle time, it is not necessary for it to be a continuous clock. This capability permits the S6845 to be easily interfaced to non-6500-compatible microprocessors.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the S6845; a low on the R/$\overline{W}$ pin allows a write to the S6845.

$\overline{CS}$ (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The S6845 is selected when $\overline{CS}$ is low.

RS (Register Select)

The Register Select input is used to access internal registers. A low on this pin permits writes into the Address Register and Reads from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

DB_0-DB_7 (Data Bus)

The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the S6845. These lines are bi-directional and are normally high-impedance except during read cycles when the chip is selected.

Video Interfrace Signal Description

HSYNC (Horizontal Sync)

The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC signal is an active-high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC position and width are both fully programmable.

DISPLAY ENABLE

The DISPLAY ENABLE signal is an active-high output and is used to indicate when the S6845 is generating active display information. The number of horizontal displayed characters and the number of vertical displayed characters are both fully programmable and together are used to generate the DISPLAY ENABLE signal. DISPLAY ENABLE may be delayed by one character time by setting bit 4 of R8 to a "1".

CURSOR

The CURSOR signal is an active-high output and is used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The CURSOR position may be delayed by one character time by setting bit 5 of R8 to a "1".

LPEN

The LPEN signal is an edge-sensitive input and is used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time of active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK

The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

$\overline{RES}$

The $\overline{RES}$ signal is an active-low input used to initialize all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing is initiated when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can be used to synchronize display frame timing with line frequency.

Memory Address Signal Description

MA0-MA13 (Video Display RAM Address Lines)

These signals are active-high outputs and are used to address the Video Display RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0-MA13:

- Binary
  Characters are stored in successive memory locations. Thus, the software must be developed so that row and column co-ordinates are translated to sequentially-numbered addresses for video display memory operations.
- Row/Column
  In this mode, MA0-MA7 function as column addresses CC0-CC7, and MA8-MA13, as row addresses CR0-CR5. In this case, the software may handle addresses in terms of row and column locations, but additional address compression circuits are needed to convert CC0-CC7 and CR0-CR5 into a memory-efficient binary scheme.

RA0-RA4 (Raster Address Lines)

These signals are active-high outputs and are used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

The high-order line, RA4, is unique in that it can also function as a strobe output pin when the S6845 is programmed to operate in the "Transparent Address Mode". In this case the strobe is an active-high output and is true at the time the Video display RAM update address is gated on to the address lines, MA0-MA13. In this way, updates and readouts of the Video Display RAM can be made under control of the S6845 with only a small amount of external circuitry.

Description of Internal Registers

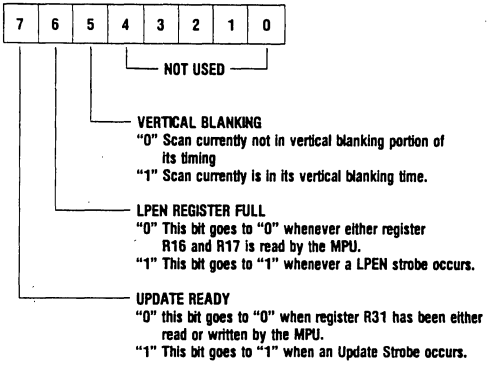
Figure 1 illustrates the format of a typical video display and is necessary to understand the functions of the various S6845 internal registers. Figure 2 illustrates vertical and horizontal timing. Figure 3 summarizes the internal registers and indicates their address selection and read/write capabilities.

Address Register

This is a 5-bit register which is used as a "pointer" to direct S6845 data transfers to and from the system MPU. Its contents is the number of the desired register (0-31). When RS is low, then this register may be loaded; when RS is high, then the register selected is the one whose identity is stored in this register.

Status Register

This 3-bit register is used to monitor the status of the CRTC, as follows:



Horizontal Total (RO)

This 8-bit register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

Horizontal Displayed (R1)

This 8-bit register contains the number of displayed characters per horizontal line.

Horizontal Sync Position (R2)

This 8-bit register contains the position of the HSYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left-to-right location of the displayed text on the video screen. In this way, the side margins are adjusted.

MICRO-PROCESSOR CIRCUITS

Figure 1. Video Display Format

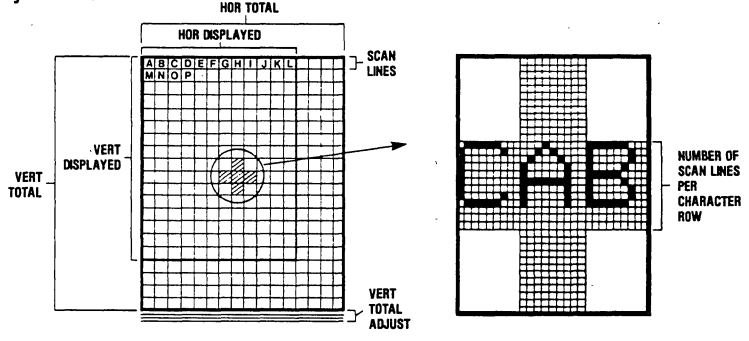
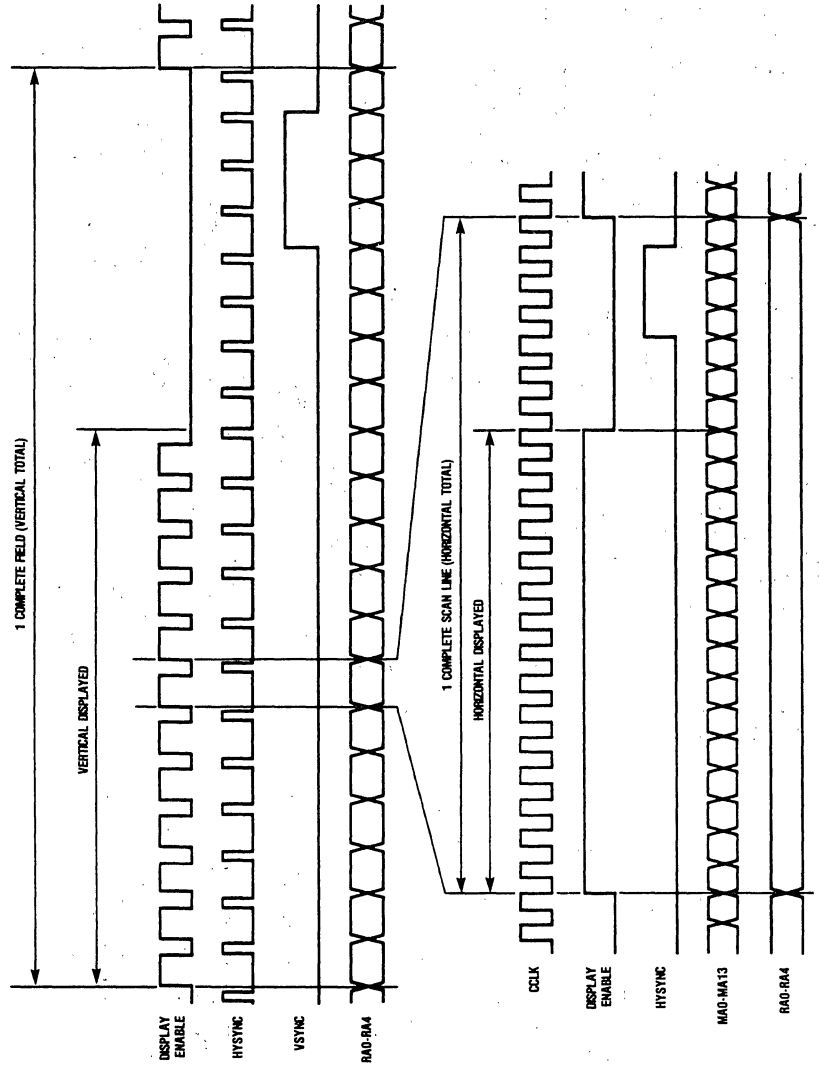
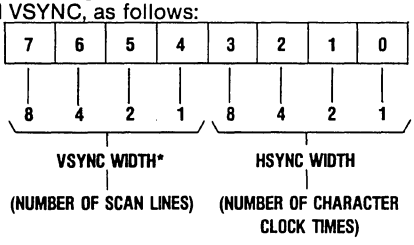


Figure 2. Vertical and Horizontal Timing



Horizontal and Vertical SYNC Widths (R3)

This 8-bit register contains the widths of both HSYNC and VSYNC, as follows:



*IF BITS 4-7 ARE ALL "0", THEN VSYNC WILL BE 16 SCAN LINES WIDE.

Control of these parameters allow the S6845 to be interfaced to a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one-shot timing.

Vertical Total (R4)

The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may be used to provide absolute synchronism.

		Address Reg.					Reg.				Register Bit							
$\overline{CS}$	RS	4	3	2	1	0	No.	Register Name	Stored Info.	RD	WR	7	6	5	4	3	2	1	0
1		—	—	—	—	—	—												
0	0	—	—	—	—	—	—	Address Reg.	Reg. No.		✓				A_4	A_3	A_2	A_1	A_0
0	0	—	—	—	—	—	—	Status Reg.		✓		U	L	V					
0	1	0	0	0	0	0	R0	Horiz. Total	#Charac. −1		✓	●	●	●	●	●	●	●	●
0	1	0	0	0	0	1	R1	Horiz. Displayed	#Charac.		✓	●	●	●	●	●	●	●	●
0	1	0	0	0	1	0	R2	Horiz. Sync Position	#Charac.		✓	●	●	●	●	●	●	●	●
0	1	0	0	0	1	1	R3	VSYNC, HSYNC Widths	#Scan Lines and #Char. Times		✓	V_3	V_2	V_1	V_0	H_3	H_2	H_1	H_0
0	1	0	0	1	0	0	R4	Vert. Total	#Charac. Row −1		✓		●	●	●	●	●	●	●
0	1	0	0	1	0	1	R5	Vert. Total Adjust	#Scan Lines		✓				●	●	●	●	●
0	1	0	0	1	1	0	R6	Vert. Displayed	#Charac. Rows		✓		●	●	●	●	●	●	●
0	1	0	0	1	1	1	R7	Vert. Sync Position	#Charac. Rows		✓		●	●	●	●	●	●	●
0	1	0	1	0	0	0	R8	Mode Control			✓	U_1	U_0	C	D	T	RC	I_1	I_0
0	1	0	1	0	0	1	R9	Scan Line	#Scan Lines −1		✓				●	●	●	●	●
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No.		✓		B_1	B_0	●	●	●	●	●
0	1	0	1	0	1	1	R11	Cursor End	Scan Line No.		✓				●	●	●	●	●
0	1	0	1	1	0	0	R12	Display Start Addr (H)	Row		✓			●	●	●	●	●	●
0	1	0	1	1	0	1	R13	Display Start Addr (L)	Col		✓	●	●	●	●	●	●	●	●
0	1	0	1	1	1	0	R14	Cursor Position (H)	Row	✓	✓			●	●	●	●	●	●
0	1	0	1	1	1	1	R15	Cursor Position (L)	Col	✓	✓	●	●	●	●	●	●	●	●
0	1	1	0	0	0	0	R16	Light Pen Reg (H)		✓				●	●	●	●	●	●
0	1	1	0	0	0	1	R17	Light Pen Reg (L)		✓		●	●	●	●	●	●	●	●
0	1	1	0	0	1	0	R18	Update Location (H)			✓			●	●	●	●	●	●
0	1	1	0	0	1	1	R19	Update Location (L)			✓	●	●	●	●	●	●	●	●
0	1	1	1	1	1	1	R31	Dummy Location											

Notes: ● Designates binary bit

▨ Designates unused bit. Reading this bit is always "0", except for R31, which does not drive the data bus at all, and for $\overline{CS}$ = "1" which operates likewise.

Vertical Total Adjust (R5)

The Vertical Total Adjust Register is a 5-bit write only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

Vertical Displayed (R6)

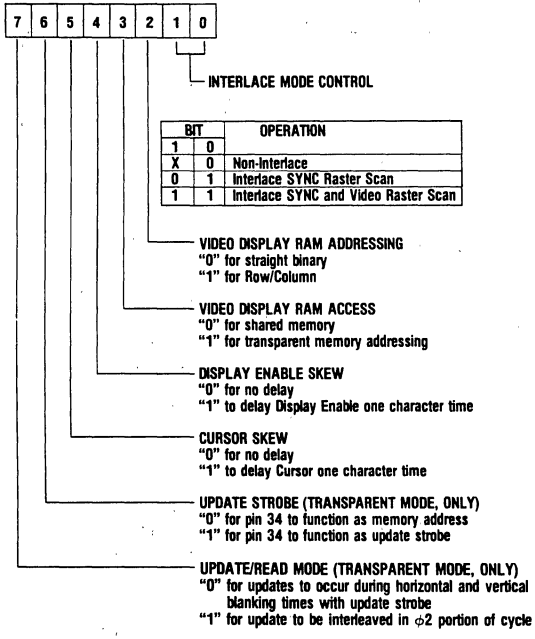
This 7-bit register contains the number of displayed character rows in each frame. In this way, the vertical size of the displayed text is determined.

Vertical Sync Position (R7)

This 7-bit register is used to select the character row time at which the VSYNC pulse is desired to occur and, thus, is used to position the displayed text in the vertical direction.

Mode Control (R8)

This register is used to select the operating modes of the S6845 and is outlined as follows:



Scan Line (R9)

This 5-bit register contains the number of scan lines per character row, including spacing minus one.

Cursor Start (R10) and Cursor End (R11)

These 5-bit registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor mode, as follows:

BIT		CURSOR MODE
6	5	
0	0	No Blinking
0	1	No Cursor
1	0	Blink at 16x field rate (fast)
1	1	Blink at 32x field rate (slow)

Note that the ability to program both the start and end scan line for the cursor enables either block cursor or underline to be accommodated. Registers R14 and R15 are used to control the character position of the cursor over the entire 16K address field.

Display Start Address High (R12) and Low (R13)

These registers together comprise a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the S6845 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

Cursor Position High (R14) and Low (R15)

These registers together comprise a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

LPEN High (R16) and Low (R17)

These registers together comprise a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

Update Address High (R18) and Low (R19)

These registers together comprise a 14-bit register whose contents is the memory address at which the next read or update will occur (for transparent address mode, only). Whenever a read/update occurs, the update location automatically increments to allow for fast updates or readouts of consecutive character locations. This is described elsewhere in this document.

Dummy Location (R31)

This register does not store any data, but is required to detect when transparent addressing updates occur. This is necessary to increment the Update Address Register and to set the Update Ready bit in the status register.

Description of Operation

Register Formats

Register pairs R12/R13, R14/R15, R16/R17, and R18/R19 are formatted in one of two ways:

1. Straight binary if register R8, bit 2 is a "0".
2. Row/column if register R8, bit 2 is a "1". In this case the low byte is the Character Column and the high byte is the Character Row.

Figure 4 illustrates the address sequence for the video display control for each mode.

Note from Figure 4 that the straight-binary mode has the advantage that all display memory addresses are stored in a continuous memory block, starting with address 0 and ending at 1919. The disadvantage with this method is that, if it is desired to change a displayed character location, the row and column identity of the location must be written. The row/column mode, on the other hand, does not need to undergo this conversion. However, memory is not used as efficiently, since the memory addresses are not continuous, but gaps exist. This requires that the system be equipped with more memory than is actually used and this extra memory is wasted. Alternatively, address compression logic may be employed to translate the row/column format into a continuous address block.

In this way, the user may select whichever mode is best for the given application. The trade-offs between the modes are software versus hardware. Straight-binary mode minimizes hardware requirements and row/column requires minimum software.

Figure 4. Display Address Sequences (with Start Address = 0) for 80 × 24 Example

TOTAL = 90 / DISPLAY = 80 / TOTAL = 34 / DISPLAY = 24

	0	1	2	...	...	77	78	79	80	81	...	89
	80	81	82	...	...	157	158	159	160	161	...	169
	160	161	162	...	...	237	238	239	240	241	...	249
	:	:	:			:	:	:	:	:		:
	:	:	:			:	:	:	:	:		:
	:	:	:			:	:	:	:	:		:
	1760	1761	1762	...	...	1837	1838	1839	1840	1841	...	1849
	1840	1841	1842	...	...	1917	1918	1919	1920	1921	...	1929
	1920	1921	1922	...	...	1997	1998	1999	2000	2001	...	2009
	2000	2001	2002	...	...	2077	2078	2079	2080	2081	...	2089
	:	:	:			:	:	:	:	:		:
	2640	2641	2642	...	...	2717	2718	2719	2720	2721	...	2729

STRAIGHT BINARY ADDRESSING SEQUENCE

TOTAL = 90 / DISPLAY = 80 / COLUMN ADDRESS (MA0-MA7) / TOTAL = 34 / DISPLAY = 24 / ROW ADDRESS (MA8-MA13)

	0	1	2	...	...	77	78	79	80	81	...	89
0	0	1	2	...	...	77	78	79	80	81	...	89
1	256	257	258	...	...	333	334	335	336	337	...	345
2	512	513	514	...	...	589	590	591	592	593	...	601
:	:	:	:			:	:	:	:	:		:
:	:	:	:			:	:	:	:	:		:
21	:	:	:			:	:	:	:	:		:
22	5632	5633	5634	...	...	5709	5710	5711	5712	5713	...	5721
23	5888	5889	5890	...	...	5965	5966	5967	5968	5969	...	5977
24	6144	6145	6146	...	...	6221	6222	6223	6224	6225	...	6233
25	6400	6401	6402	...	...	6477	6478	6479	6480	6481	...	6489
:	:	:	:			:	:	:	:	:		:
33	8448	8449	8450	...	...	8525	8526	8527	8528	8529	...	8537

ROW/COLUMN ADDRESSING SEQUENCE

Video Display RAM Addressing

There are two modes of addressing for the video display memory:

1. Shared Memory
   In this mode the memory is shared between the MPU address bus and the S6845 address bus. For this case, memory contention must be resolved by means of external timing and control circuits. Both the MPU and the S6845 must have access to the video display RAM and the contention circuits must resolve this multiple access requirement. Figure 5 illustrates the system configuration.
2. Transparent Memory Addressing
   For this mode, the display RAM is not directly accessible by the MPU, but is controlled entirely by the S6845. All MPU accesses are made via the S6845 and a small amount of external circuits. Figure 6 shows the system configuration for this approach.

Figure 5. Shared Memory System Configuration

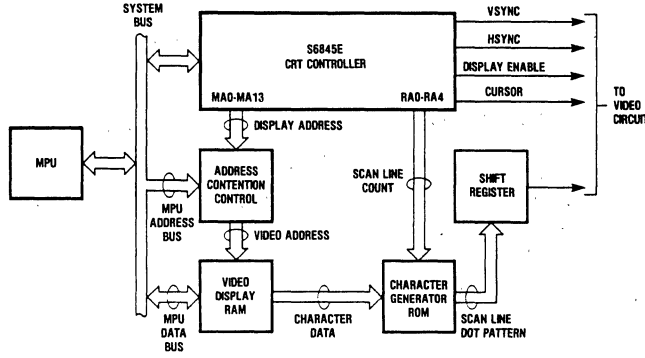
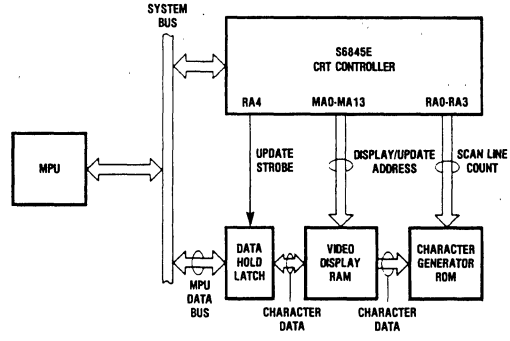


Figure 6. Transparent Memory Addressing System Configuration (Data Hold Latch needed for Horizontal/Vertical Blanking updates, only).



Memory Contention Schemes for Shared Memory Addressing

From the diagram of Figure 4, it is clear that both the S6845 and the system MPU must be capable of addressing the video display memory. The S6845 repetitively fetches character information to generate the video signals in order to keep the screen display active. The MPU occasionally accesses the memory to change the displayed information or to read out current data characters. Three ways of resolving this dual-contention requirement are apparent:

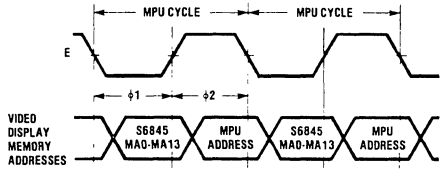
- MPU Priority

  In this technique, the address lines to the video display memory are normally driven by the S6845 unless the MPU needs access, in which case the MPU addresses immediately override those from the S6845 and the MPU has immediate access.

- $\phi 1/\phi 2$ Memory Interleaving

  This method permits both the S6845 and the MPU access to the video display memory by time-sharing via the system $\phi 1$ and $\phi 2$ clocks. During the $\phi 1$ portion of each cycle (the time when E is low), the S6845 address outputs are gated to the video display memory. In the $\phi 2$ time, the MPU address lines are switched in. In this way, both the S6845 and the MPU have unimpeded access to the memory. Figure 7 illustrates the timings.

Figure 7. $\phi 1/\phi 2$ Interleaving



- Vertical Blanking

  With this approach, the address circuitry is identical to the case for MPU Priority updates. The only difference is that the Vertical Retrace status bit (bit 5 of the Status Register) is used by the MPU so that access to the video display memory is only made during vertical blanking time (when bit 5 is a "1"). In this way, no visible screen perturbations result.

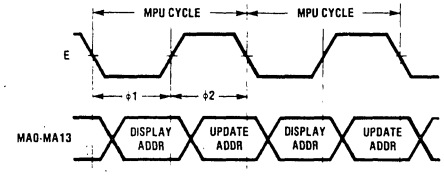
Transparent Memory Addressing

In this mode of operation, the video display memory address lines are not switched by contention circuits, but are generated by the S6845. In effect, the contention is handled by the S6845. As a result, the schemes for accomplishing MPU memory access are different:

- $\phi 1\phi 2$ Interleaving

  This mode is similar to the Interleave mode used with shared memory. In this case, however, the $\phi 2$ address is generated from the Update Address Register (Registers R18 and R19) in the S6845. Thus, the MPU must first load the address to be accessed into R18/R19 and then this address is always gated onto the MA lines during $\phi 2$. Figure 8 shows the timing.

Figure 8. $\phi 1/\phi 2$ Transparent Interleaving

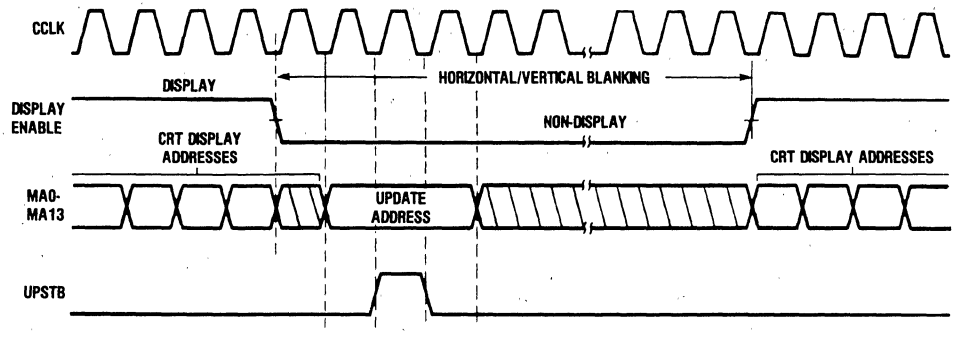


- Horizontal/Vertical Blanking

  In this mode, the Update Address is loaded by the MPU, but is only gated onto the MA lines during horizontal or vertical blank times, so memory accesses do not interfere with the display appearance. To signal when the update address is on the MA Lines, an update strobe (STB) is provided as an alternate function of pin 34. Data hold latches are necessary to temporarily retain the character to be stored until the retrace time occurs. In this way, the system MPU is not halted waiting for the blanking time to arrive. Figure 9 illustrates the address and strobe timing for this mode.

Transparent address modes are quite complex and offer significant advantages in system implementation.

Figure 9. Retrace Update Timings



Interlace Modes

There are three raster-scan display modes (see Figure 10).

a) Non-Interlaced Mode. In this mode each scan line is refreshed at the vertical field rate (50 or 60 Hz).

In the interlaced scan modes, even and odd fields alternate to generate frames. The horizontal and vertical timing relationship causes the scan lines in the odd fields to be displaced from those in the even fields. The two additional raster-scan display modes pertain to interlaced scans.

b) Interlace-Sync Mode. this mode is used when the same information is to be displayed in both odd and even fields. Enhanced readability results because the space between adjacent rows are filled and a higher quality character is displayed. This is achieved with only a slight alteration in the device operation: in alternate fields, the position of the VSYNC signal is delayed by ½ of a scan line time. This is illustrated in Figure 11 and is the only difference in the S6845 operation in this mode.

c) Interlaced Sync and Video Mode. this mode is used to double the character density on the screen by displaying the even lines in even fields and the odd lines in odd fields. As in the Interlace-Sync mode, the VSYNC position is delayed in alnate display fields. In addition, the address generation is altered.

Figure 10. Comparison of Display Modes.

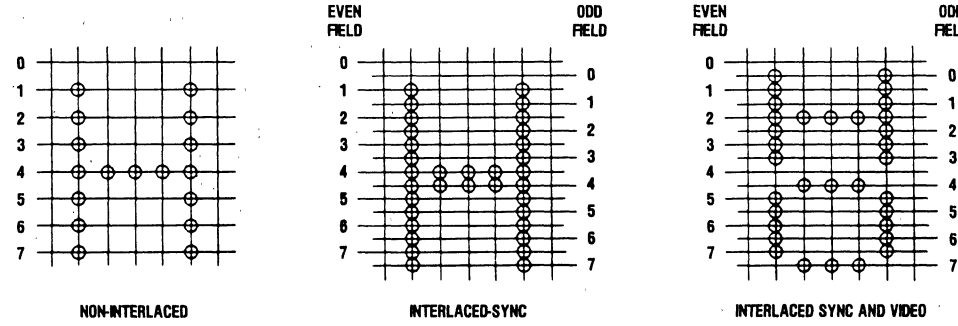


Figure 11. Interlace Sync Mode and Interlace Sync & Video Mode Timing

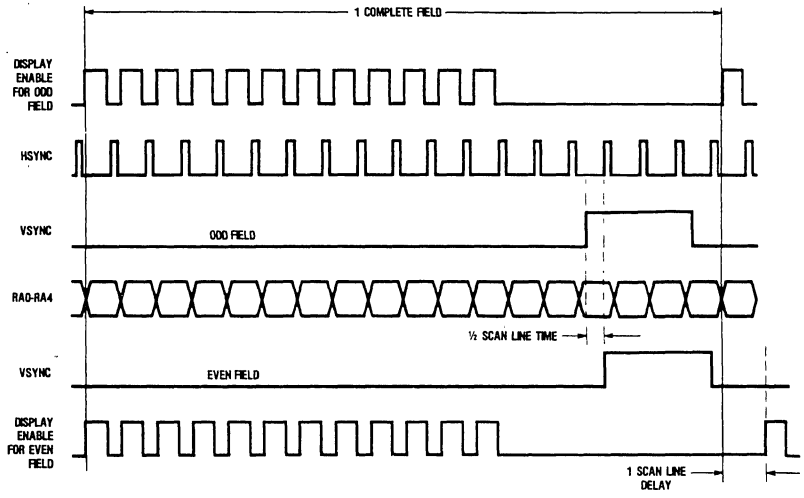
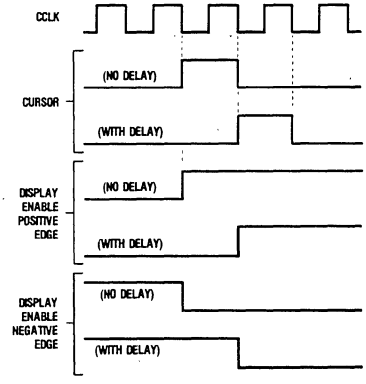


Figure 12. Cursor and Display Enable Skew



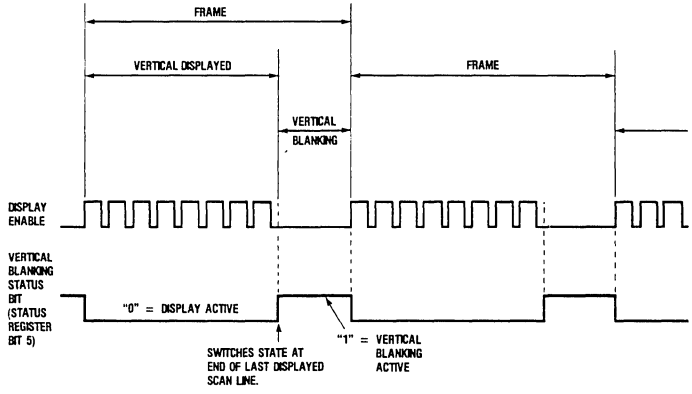
Cursor and Display Enable Skew Control

Bits 4 and 5 of the Mode Control register (R8) are used to delay the Display Enable and Cursor outputs, respectively. Figure 12 illustrates the effect of the delays.

CRTC Register Comparison
NON-INTERLACE

REGISTER	SY6845R	MC6845R HD6845R	HD6845S	SY6545-1	S6845E
R0 HORIZONTAL TOT	TOT-1	TOT-1	TOT-1	TOT-1	TOT-1
R1 HORIZONTAL DISP	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R2 HORIZONTAL SYNC	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R3 HORIZONTAL AND VERT SYNC WIDTH	HORIZONTAL	HORIZONTAL	HORIZONTAL AND VERTICAL	HORIZONTAL AND VERTICAL	HORIZONTAL AND VERTICAL
R4 VERTICAL TOT	TOT-1	TOT-1	TOT-1	TOT-1	TOT-1
R5 VERTICAL TOT ADJ	ANY VALUE	ANY VALUE	ANY VALUE	ANY VALUE EXCEPT R5 = (R9H)•X	ANY VALUE
R6 VERTICAL DISP	ANY VALUE < R4	ANY VALUE < R4	ANY VALUE < R4	ANY VALUE < R4	ANY VALUE < R4
R7 VERTICAL SYNC POS	ACTUAL-1	ACTUAL-1	ACTUAL-1	ACTUAL-1	ACTUAL-1
R8 MODE REG BITS 0 AND 1	INTERLACE MODE SELECT	INTERLACE MODE SELECT	INTERLACE MODE SELECT	INTERLACE MODE SELECT	INTERLACE MODE SELECT
BITS 2	—	—	—	ROW/COLUMN OR STRAIGHT BINARY ADDRESSING	ROW/COLUMN OR STRAIGHT STRAIGHT ADDRESSING
BITS 3	—	—	—	SHARED OR TRANSPARENT ADDR	SHARED OR TRANSPARENT ADDR
BITS 4	—	—	DISPEN SKEW	DISPEN SKEW	DISPEN SKEW
BITS 5	—	—	DISPEN SKEW	CURSOR SKEW	CURSOR SKEW
BITS 6	—	—	CURSOR SKEW	RA4/UPSTB	RA4/UPSTB
BITS 7	—	—	CURSOR SKEW	TRANSPARENT MODE SELECT	TRANSPARENT MODE SELECT
R9 SCAN LINES	TOT-1	TOT-1	TOT-1	TOT-1	TOT-1
R10 CURSOR START	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R11 CURSOR END	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R12/R13 DISP ADDR	WRITE ONLY	WRITE ONLY	READ/WRITE	WRITE ONLY	WRITE ONLY
R14/R5 CUROSR POS	READ/WRITE	WRITE ONLY	READ/WRITE	READ/WRITE	READ/WRITE
R16/R17 LPEN REG	READ ONLY	READ ONLY	READ ONLY	READ ONLY	READ ONLY
R18/R19 UPDATE ADDR REG	N/A	N/A	N/A	TRANSPARENT MODE ONLY	TRANSPARENT MODE ONLY
R31 DUMMY REG	N/A	N/A	N/A	TRANSPARENT MODE ONLY	TRANSPARENT MODE ONLY
STATUS REG	YES	NO	NO	YES	YES
INTERLACE SYNC					
R0	TOT-1 = ODD OR EVEN	TOT-1 = ODD	TOT-1 = ODD	TOT-1 = ODD	TOT-1 = ODD OR EVEN
INTERLACE SYNC AND VIDEO					
R4 VERTICAL	TOT-1	TOT-1	TOT-1	TOT/2-1	TOT-1
R6 VERT DISP	TOT	TOT/2	TOT	TOT/2	TOT
R7 VERT SYNC	ACTUAL-1	ACTUAL-1	ACTUAL-1	ACTUAL/2	ACTUAL-1
R9 SCAN LINES	TOT-1 ODD/EVEN	TOT-1 ONLY EVEN	TOT-2 ODD/EVEN	TOT-1 ODD/EVEN	TOT-1 ODD/EVEN
R10 CURSOR START R11 CURSOR END	ODD/EVEN ODD/EVEN	BOTH ODD OR BOTH EVEN	ODD/EVEN ODD/EVEN	ODD/EVEN ODD/EVEN	ODD/EVEN ODD/EVEN
CCLK	2.5 MHz	2.5 MHz	3.7 MHz	2.5 MHz	3.7 MHz

Figure 13. Operation of Vertical Blanking Status Bit



Package Availability

Ordering Information

Part Number	Package	CPU Clock Rate
S6845E	Molded DIP	1 MHz
S6845EA	Molded DIP	2 MHz

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Display Driver Circuits

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30-Volt Dichroic LCD Driver

S4520

Features

- ☐ High Voltage Outputs Capable of a 32-Volt Swing
- ☐ Drives Up to 38 Devices
- ☐ Cascadable
- ☐ On-Chip Oscillator
- ☐ Requires Only 4 Control Lines
- ☐ CMOS Construction For:
  - Wide Supply Range
  - Low Power Consumption
  - High Noise Immunity
  - Wide Temperature Range
- ☐ **Military Version (screened per Mil. Std. 883 method 5004 and tested per method 5010) will be available upon request.**

Applications

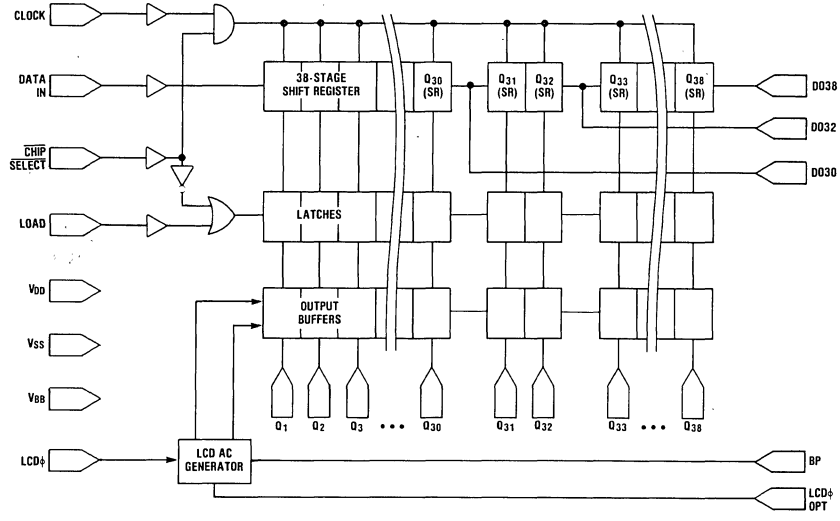
- ☐ Liquid Crystal Displays
- ☐ Flat Panel Displays
- ☐ Print Head Drives

General Description

The S4520 is a CMOS/LSI circuit that drives high-voltage dichroic liquid crystal displays, usually under microprocessor control. The S4520 requires only four control inputs (CLOCK, DATA IN, LOAD and CHIP SELECT) due to its serial input construction. It can latch the data to be output, relieving the microprocessor from the task of generating the required waveforms, or it may be used to bring data directly to the drivers. The A.C. frequency of the backplane output can be generated by the internal oscillator or, the user has the option of supplying this signal from an external source. If the internal oscillator is used to generate the backplane signal, the frequency will be determined by an external resistor and capacitor. One S4520 circuit can drive 38 segments. Other packaging options can provide 32 segment drivers. Note: For 30 segment version contact the factory.

DISPLAY DRIVERS

Block Diagram



Absolute Maximum Ratings

V_{DD}	−0.3V to +17V
V_{BB}	V_{SS} + 0.3V to V_{DD} − 32V
Inputs (CLK, DATA IN, LOAD)	V_{SS} − 0.3V to V_{DD} + 0.3V
Inputs (LCDϕ)	V_{BB} − 0.3V to V_{DD} + 0.3V
Power Dissipation	250mW
Storage Temperature	−65°C to +125°C
Operating Temperature	−55°C to +85°C

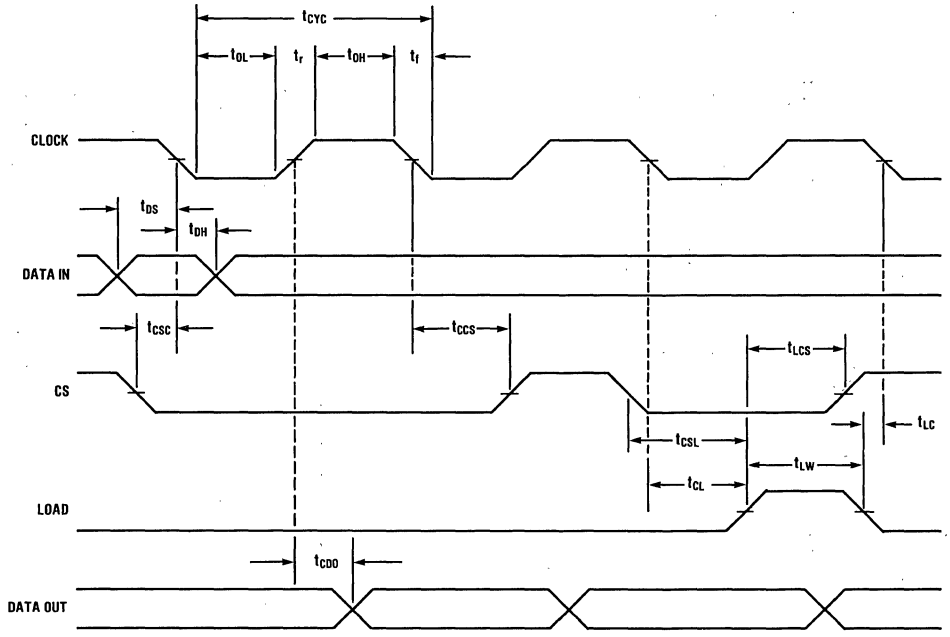
Electrical Characteristics: $3V \leq V_{DD} \leq 16V$, $-55°C \leq T_A \leq +85°C$, unless otherwise noted

Symbol	Parameter	Min.	Max.	Units	Test Condition
	Power Supply				
V_{DD}	Logic Supply Voltage	3	16	V	
V_{BB}	Display Supply Voltage	$V_{DD}-32$	$V_{DD}-15$	V	$V_{BB} \leq V_{SS}$
I_{DD}	Supply Current (external oscillator) Supply Current (internal oscillator)		200 200	μA μA	CMOS input levels. No loads.
I_{BB}	Display Driver Current		−200	μA	f_{BP} = 100Hz. No loads.
	Inputs (CLK, DATA IN, LOAD, $\overline{CS}$)				
V_{IH}	Input High Level	$0.5V_{DD}$	V_{DD}	V	$V_{DD} \geq 5V$
V_{IL}	Input Low Level	V_{SS}	$0.2V_{DD}$	V	
I_L	Input Leakage Current		5	μA	
C_I	Input Capacitance		5	pF	
$V_{O_{AVG}}$	DC Bias (Average) Any Segment Output to Backplane		±25	mV	$f_{BP} \leq 100Hz$
V_{IH}	LCDϕ Input High Level	$0.9V_{DD}$	V_{DD}	V	Externally Driven
V_{IL}	LCDϕ Input Low Level	V_{BB}	$0.1V_{DD}$	V	Externally Driven
	Capacitance Loads (typical)				
$C_{L_{SEG}}$	Segment Output		1000	pF	$f_{BP} \leq 100Hz$
$C_{L_{BP}}$	Backplane Output		40000	pF	$f_{BP} \leq 100Hz$
R_{SEG}	Segment Output Impedance		10	KΩ	I_L = 10 μA
R_{BP}	Backplane Output Impedance		312	Ω	I_L = 10 μA
R_{DO}	Data Out Output Impedance		3	KΩ	I_L = 10 μA

Timing Characteristics:

Symbol	Parameter	Min.	Max.	Units	V_{DD}
t_{CYC}	Cycle time (noncascaded)	1000		ns	3.0V
		500		ns	5.0V
		320		ns	≥7.5V
t_{CYC}	Cycle time (cascaded)	1300		ns	3.0V
		600		ns	5.0V
		350		ns	≥7.5V
t_{OL}, t_{OH}	Clock pulse width low/high	450		ns	3.0V
		220		ns	5.0V
		140		ns	≥7.5V
t_{OH}	Clock pulse width high (cascaded)	750		ns	3.0V
		320		ns	5.0V
		180		ns	≥7.5V
t_r, t_f	Clock rise, fall (Note 12)		1	μs	
t_{DS}	Data In setup	300		ns	3.0V
		150		ns	5.0V
		120		ns	≥7.5V
t_{CSC}	$\overline{CS}$ setup to Clock	200		ns	3.0V
		100		ns	5.0V
		50		ns	≥7.5V
t_{DH}	Data hold	10		ns	
t_{CCS}	$\overline{CS}$ hold	450		ns	3.0V
		220		ns	5.0V
		140		ns	≥7.5V
t_{CL}	Load pulse setup (Note 5)	500		ns	3.0V
		280		ns	5.0V
		180		ns	≥7.5V
t_{LCS}	$\overline{CS}$ hold (rising LOAD to rising $\overline{CS}$)	300		ns	3.0V
		200		ns	5.0V
		150		ns	≥7.5V
t_{LW}	Load pulse width (Note 5)	500		ns	3.0V
		220		ns	5.0V
		140		ns	≥7.5V
t_{LC}	Load pulse delay (Falling load to falling clock)	0		ns	
t_{CDO}	Data Out valid from Clock		550	ns	3.0V
			220	ns	5.0V
			110	ns	≥7.5V
t_{CSL}	$\overline{CS}$ setup to LOAD	0		ns	

Figure 1. Signal Timing Diagram



Logic Truth Table

DATA IN	CLOCK	$\overline{\text{CHIP SELECT}}$	LOAD	Q_1(SR)	Q_N(SR)	BP	Q_N(DRIVER)
X	X	1	0	NC	NC	0	QN(L)
X	X	1	1	NC	NC	1	QN(L)
0	⌐	0	0	NC	NC	1	QN(L)
0	⌐	0	1	NC	NC	1	QN(L)
0	¬	0	0	0	QN—1→QN	1	QN(L)
0	¬	0	1	0	QN—1→QN	1	QN(SR)
1	⌐	0	0	NC	NC	1	QN(L)
1	⌐	0	1	NC	NC	1	QN(L)
1	¬	0	0	1	QN—1→QN	1	QN(L)
1	¬	0	1	1	QN—1→QN	1	QN(SR)

Notes: NC = No Change SR = Shift Register L = Latch

Operating Notes

1. The shift register loads and shifts on the falling edge of CLK. DATA OUT changes on the rising edge of CLK.
2. The buffer number corresponds to how many clock pulses have occurred since its data was present at the input (e.g., the data on Q_{10} was input 10 clock pulses earlier). DATA is shifted into Segment 1 and shifted out from Segments 30, 32 or 38, depending on bonding option used.
3. A logic 1, shifted into the shift register (through DATA IN), causes the corresponding segment's output to be out of phase with the backplane.
4. A logic 1 on LOAD causes a parallel load of the data in the shift register, into the latches that control the output drivers.
5. LOAD may also be held high while clocking. In this case, the latch is transparent and, the falling edge of LOAD will latch the data.
6. To cascade units, (a) connect the DATA OUT of one chip to the DATA IN of the next chip, and (b) either connect the backplane of one chip to LCDϕ of all other chips (thus one RC provides frequency control for all chips) **or** connect LCDϕ of all chips to a common driving signal. If the former is chosen, the backplane that is tied to the LCDϕ of the other chips should **not** also be connected to the backplanes of those chips.
7. The LCDϕ pin can be used in two modes, driven or self-oscillating. If LCDϕ is driven, the circuit will sense this condition. If the LCDϕ pin is allowed to oscillate, its frequency is determined by an external capacitor. The Backplane frequency is a divide by 256 of the LCDϕ frequency, in the self-oscillating mode.
8. If LCDϕ is driven externally, it is in phase with the backplane output.
9. Backplanes can be tied together, if they have the same signal applied to their LDCϕ inputs.
10. In the self-oscillating mode, the backplane frequency is approximately defined by the relationship $f_{BP}(Hz) = 10 \div R(C + .0002)$ at $V_{DD} = 5V$, R in KΩ, C in μF.

    examples: R = 56KΩ, C = .0015μF: $f_{BP} \doteq 100Hz$
    R = 110KΩ, C = .00068μF: $f_{BP} \doteq 100Hz$
11. Minimum value of R for RC oscillator is 50KΩ.
12. Power consumption increases for clock rise or fall times greater than 100ns.

Ordering Information

1. All orders must specify a package type (i.e. S4520C, 48 CLCC)
2. All orders must specify whether an internal oscillator or external oscillator will be used (i.e. S4520D external oscillator).
3. A set-up charge or minimum order quantity may apply for packaging options not shown.
4. Standard products available (refer to pages 1 and 8 for pin out descriptions):

Version	Package	Segments	Oscillator	Data Out
S4520C	48 CLCC	38	Internal	38
S4502D	48 CLCC	38	External	38
S4520G	44 PLCC	32	Int or Ext	32

Contact sales office for other packaging options.

Chip Select Inverse Input

The $\overline{CS}$ input is used to enable clocking of the shift register. When $\overline{CS}$ is low, the chip will be selected and the shift register will be enabled. When $\overline{CS}$ is high, the shift register will be disabled and the output buffers will be driven by the data in the latches.

Clock Input

The CLOCK input is used to clock data serially, into the shift register. A clock signal may be continuously present, because the shift register is enabled only when $\overline{CS}$ is low.

Load Input

The LOAD input controls the operation of the data latches and allows new data to be loaded into the shift register, without changing the appearance of the display. When LOAD is high, the values in the shift register will be loaded into the data latches. If desired, LOAD can be held high and the data latches will be transparent. The LOAD input is disabled when $\overline{CS}$ is high.

LCD Oscillator Input

When used with an external oscillator, the LCD oscillator is driven by the input voltage level. In this configuration, the backplane output will be in phase with the input waveform. In the self-oscillating mode, an external resistor and capacitor are connected to the oscillator input pin, and the backplane frequency will be a divide by 256 of the internal oscillator frequency.

LCD Oscillator Options

Internal Oscillator — The LCD oscillator option (LCDϕ OPT) is internally (or externally) connected to the LCD oscillator input (LCDϕ) and, it provides the oscillator feedback.

External Oscillator — The LCD oscillator option is not connected.

Data Input

Data present at DATA IN will be clocked into the shift register, when $\overline{CS}$ is low. Data is loaded into the shift register on the falling edge of the clock and shifts to the output on the rising clock edge.

Data Output

Depending on the packaging option selected, DO30, DO32 and DO38 are buffered outputs driven by the corresponding element of the shift register. The value of DOxx will be the same as the value of the matching shift register bit (i.e. the value at DO32 will be the same as bit 32 of the shift register). The data output is typically used to drive the data input of another S4520. By cascading S4520 circuits in this manner, additional display elements can be driven.

Backplane Output

The backplane output provides the voltage waveform for the LCD backplane. When used with the internal oscillator, the backplane frequency will be equal to the oscillator frequency divided by 256:

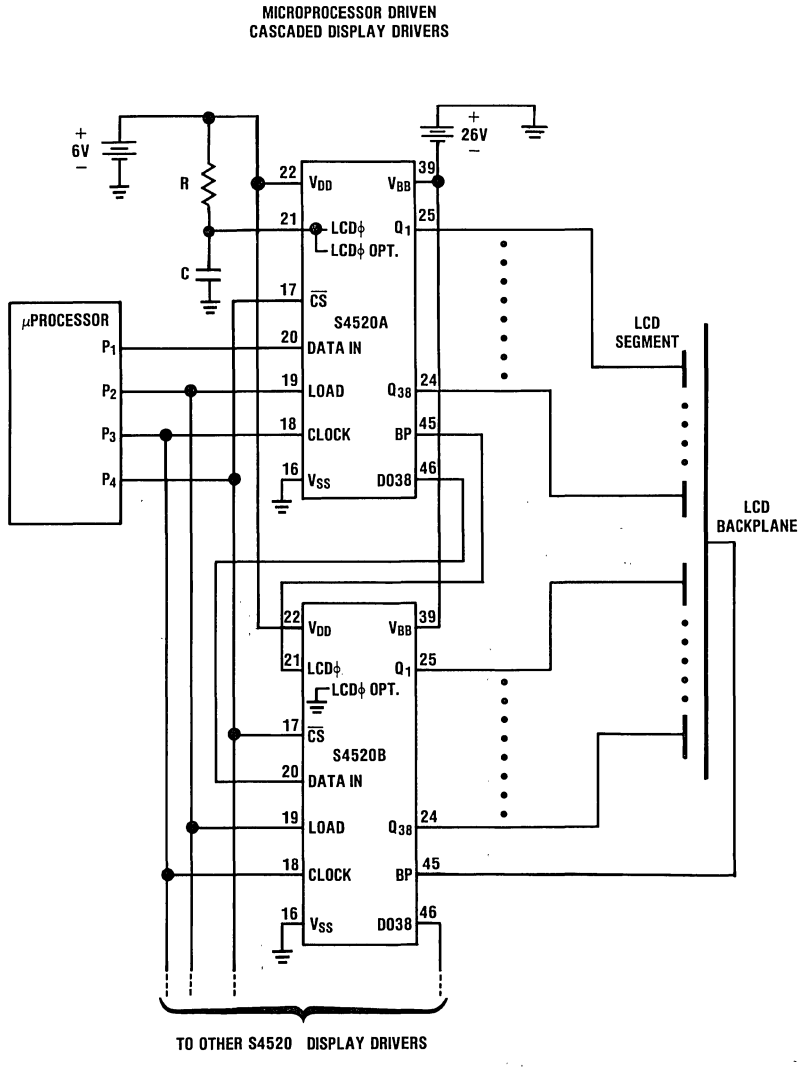
$$f_{BP} = f_{OSC}\,(\text{int}) \div 256.$$

With an external oscillator, the backplane frequency will be in phase with and equal in magnitude to the input signal.

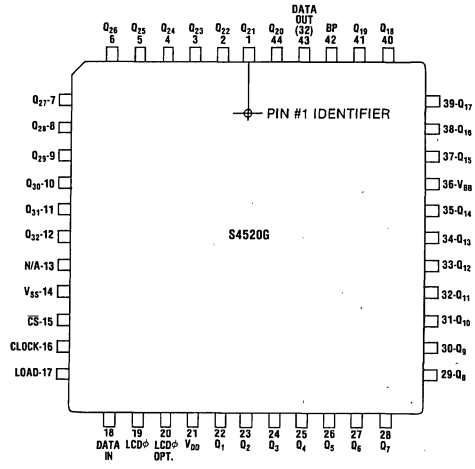
Segment Drive Outputs

The segment drive outputs provide the segment drive voltage to the LCD. With a logic level "1" in the latch associated with the segment drive output, the output voltage will be out of phase with the backplane (i.e the segment will be ON). A logic level "0" will cause the segment drive to be in phase with the backplane output voltage.

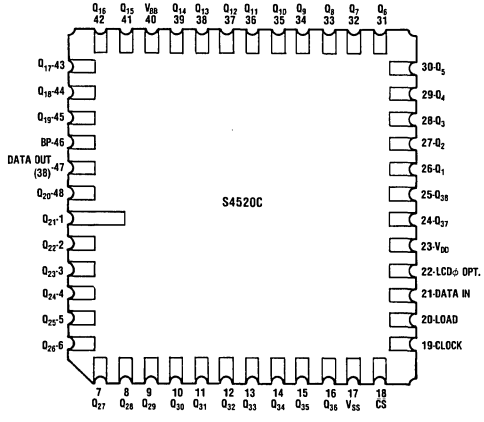
Figure 2. Typical Application

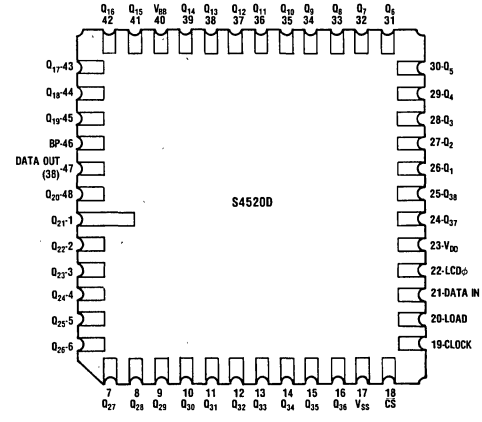


44-Plastic Leaded Chip Carrier (PLCC)



48-Ceramic Leadless Chip Carrier (CLCC)





NOTE: Viewed From Top Side of Package

Contact sales for other possible package options.

GOULD

AMI Semiconductors

32 Bit Driver

S4521

Features

- ☐ Drives Up to 32 Devices
- ☐ Cascadable
- ☐ On Chip Oscillator
- ☐ Requires Only 3 Control Lines
- ☐ CMOS Construction For:
  - Wide Supply Range
  - High Noise Immunity
  - Wide Temperature Range

Applications:

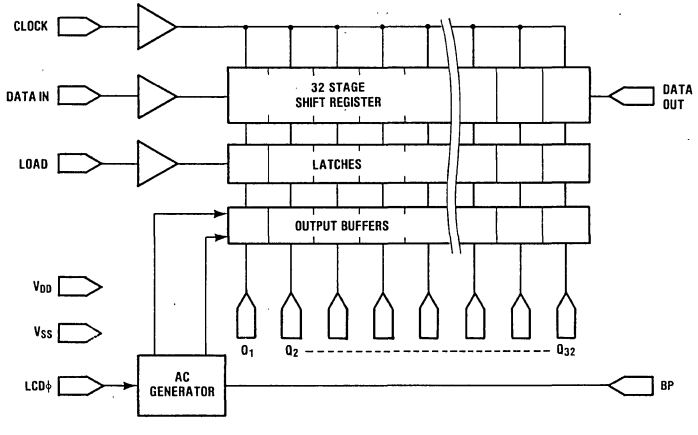
- ☐ Liquid Crystal Displays
- ☐ LED and Incandescent Displays
- ☐ Solenoids
- ☐ Print Head Drives
- ☐ DC and Stepping Motors
- ☐ Relays

General Description

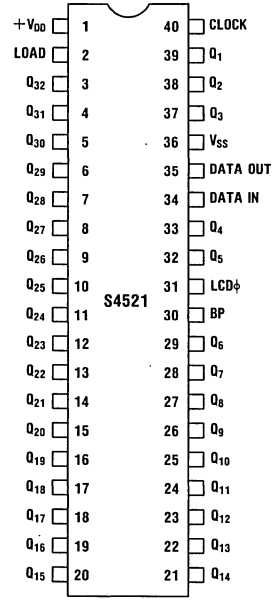
The S4521 is an MOS/LSI circuit that drives a variety of output devices, usually under microprocessor control. This device requires only three control lines due to its serial input construction. It latches the data to be output, relieving the microprocessor from the task of generating the required waveform, or it may be used to bring data directly to the drivers. The part acts as a versatile peripheral to drive displays, motors, relays and solenoids within its output limitations. It is especially well suited to driving liquid crystal displays, with a backplane A.C. signal option that is provided. The A.C. frequency of the backplane output that can be user supplied or generated by attaching a capacitor to the LCD_f input, which controls the frequency of the internal oscillator. One circuit will drive up to 32 devices and more can be driven by cascading several drivers together. The S4521F version is available in a surface-mountable plastic mini-flat pack.

DISPLAY DRIVERS

Functional Block Diagram



Pin Configuration



Absolute Maximum Ratings

V_{DD}	−0.3 to +17V
Inputs (CLK, DATA IN, LOAD, LCDϕ)	V_{SS} − 0.3 to V_{DD} + 0.3V
Power Dissipation	250mW
Storage Temperature	−65°C to +125°C
Operating Temperature	−40°C to +85°C

Electrical Characteristics: $3V \leq V_{DD} \leq 13V$, unless otherwise noted

Symbol	Parameter	Min.	Max.	Units	Test Condition
V_{DD}	Supply Voltage	3	13	V	
	Supply Current				
I_{DD1}	Operating		200	μA	f_{BP} = 120Hz, No Load, V_{DD} = 5V
I_{DD2}	Quiescent		200	μA	LCDϕ High or Low, f_{BP} = 0 Load @ Logic 0, V_{DD} = 5V
	Inputs (CLK, DATA IN, LOAD)				
V_{IH}	High Level	0.6 V_{DD}	V_{DD}	V	$3V \leq V_{DD} < 5V$
		0.5 V_{DD}	V_{DD}	V	$5V \leq V_{DD} \leq 13V$
V_{IL}	Low Level	V_{SS}	0.2 V_{DD}	V	
I_L	Input Current		5	μA	
C_I	Input Capacitance		5	pF	
f_{CLK}	CLK Rate	DC	2	MHz	50% Duty Cycle
t_{DS}	Data Set-Up Time	100		ns	Data Change to CLK Falling Edge
t_{DH}	Data Hold Time	10		ns	Falling CLK Edge to Data Change
t_{PW}	Load Pulse Width	200		ns	
t_{PD}	Data Out Prop. Delay		220	ns	C_L = 30pF, From Rising CLK Edge
t_{LC}	Load Pulse Set-Up	300		ns	Falling CLK Edge to Rising Load Pulse
t_{LCD}	Load Pulse Delay	0		ns	Falling Load Pulse to Falling CLK Edge
$V_{O_{AVG}}$	DC Bias (Average) Any Q Output to Backplane		±25	mV	f_{BP} = 120Hz
V_{IH}	LCDϕ Input High Level	.9 V_{DD}	V_{DD}	V	Externally Driven
V_{IL}	LCDϕ Input Low Level	V_{SS}	.1 V_{DD}	V	Externally Driven
	Capacitance Loads				
C_{LQ}	Q Output		50,000	pF	f_{BP} = 120Hz
C_{LBP}	Backplane		1.5	μF	f_{BP} = 120Hz, See Note 8
R_{ON}	Q Output Impedance		3.0	KΩ	I_L = 10μA, V_{DD} = 5V
R_{ON}	Backplane Output Impedance		100	Ω	I_L = 10μA, V_{DD} = 5V
R_{ON}	Data Out Output Impedance		3.0	KΩ	I_L = 10μA, V_{DD} = 5V

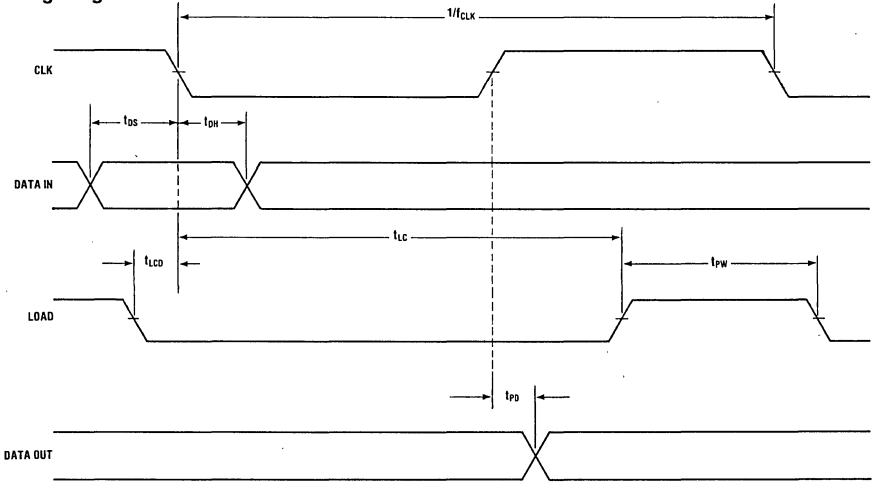
Operating Notes

1. The shift register shifts on the falling edge of CLK. It outputs on the rising edge of the CLK.
2. The buffer number corresponds to how many clock pulses have occurred since its data was present at the input (e.g., the data on Q10 was input 10 clock pulses earlier).
3. A logic 1 on Data In causes a Q output to be out of phase with the Backplane.
4. A logic 1 on Load causes a parallel load of the data in the shift register, into the latches that control the Q output drivers.
5. To cascade units, (a) connect the Data Out of one chip to Data In of next chip, and (b) either connect Backplane of one chip to LCDϕ of all other chips (thus one RC provides frequency control for all chips) or connect LCDϕ of all chips to a common driving signal. If the former is chosen, the Backplane that is tied to the LCDϕ inputs of the other chips should **not** also be connected to the Backplanes of those chips.
6. If LCDϕ is driven, it is in phase with the Backplane output.
7. The LCDϕ pin can be used in two modes, driven or self-oscillating. If LCDϕ is driven, the circuit will sense this condition. If the LCDϕ pin is allowed to oscillate, its frequency is determined by an external capacitor. The Backplane frequency is a divide by 32 of the LCDϕ frequency, in the self-oscillating mode.
8. In the self-oscillating mode, the backplane frequency is approximately defined by the relationship $f_{BP}(Hz) = 0.2 \div C(\text{in } \mu F)$ at $V_{DD} = 5V$.
9. If the total display capacitance is greater than 100,000 pF, a decoupling capacitor of $1\mu F$ is required across the power supply (pins 1 and 36).

Pin Description

Pin #	Name	Description
1	V_{DD}	Logic and Q Output Supply Voltage
2	LOAD	Signal to Latch Data from Registers
30	BP	Backplane Drive Output
31	LCDϕ	Backplane Drive Input
34	DATA IN	Data Input to Shift Register
35	DATA OUT	Data Output from Shift Register-primarily used in cascading
36	V_{SS}	Ground Connection
40	CLOCK	System Clock Input
3-29, 32-33, 37-39	Q_1-Q_{32}	Direct Drive Outputs

Signal Timing Diagrams



GOULD
AMI Semiconductors

10 Bit, High Voltage, High Current Driver

S4534

Features:

- ☐ Outputs Capable of 60 Volt Swings at 25mA
- ☐ Drives Up to 10 Devices
- ☐ Cascadable
- ☐ Requires Only 4 Control Lines

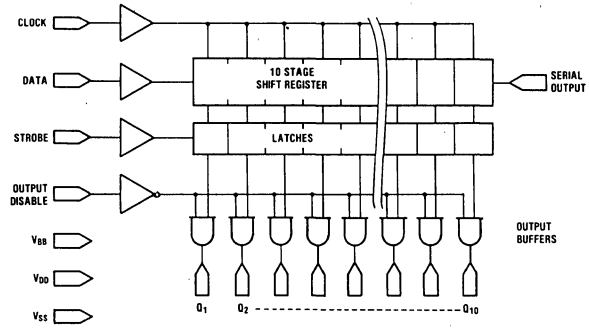
Applications:

- ☐ Vacuum Fluorescent Displays
- ☐ LED and Incandescent Displays
- ☐ Solenoids
- ☐ Print Head Drives
- ☐ DC and Stepping Motors
- ☐ Relays

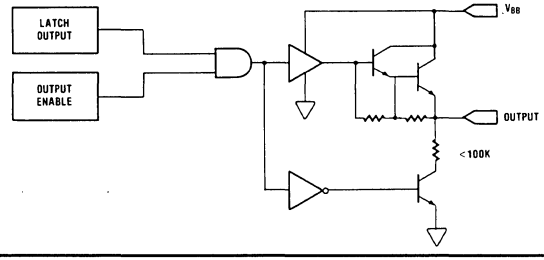
General Description

The AMI S4534 is a high voltage, high current MOS/LSI circuit that drives a variety of output devices, usually under microprocessor control, by converting low level signals such as TTL, and CMOS to high voltage, high current drive signals. This device requires only four control lines due to its serial input construction. It latches the data to be output, or it may be used to bring data directly to the driver. The part acts as a versatile peripheral to drive displays, motors, relays and solenoids within its output limitations of a 60 volt swing and up to 50mA per drive. It is especially well suited to drive vacuum fluorescent displays due to its high voltage output capability. One circuit will drive up to 10 devices and more can be driven by cascading several drivers together.

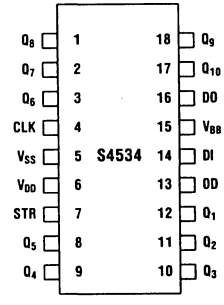
Functional Block Diagram



Output Buffer (Functional Diagram)



Pin Configuration



S4534

Absolute Maximum Ratings at 25°C

V_{BB}	65V
V_{DD}	4.5 to 15V
V_{IN}	V_{SS} – .3V to V_{DD} + .3V
V_{OUT} (Logic)	V_{SS} – .3V to V_{DD} + .3V
V_{OUT} (Display)	V_{SS} – .3V to V_{BB} + .3V
Power Dissipation	1.2W
Operating Temperature	0°C to +70°C*
Storage Temperature	–65°C to +125°C

* S4534H = –40°C to +85°C

Operational Specification: $0°C \leqslant T_A \leqslant 70°C$ (unless otherwise noted)

Symbol	Parameter	Min.	Max.	Units	Test Condition
V_{IL}	Input Zero Level	–0.3	1.1	V	
V_{IH}	Input One Level	3.4 3.6	V_{DD}+0.3 V_{DD}+0.3	V V	4.75V$\leqslant = V_{DD} <$5.25V 5.25V$\leqslant V_{DD} \leqslant$12.0V
I_{IN}	Input Leakage Current		1.0	μA	V_{DD}=5V
V_{SL}	Signal Out Zero Level	V_{SS}	0.7	V	I_{SO}=–20μA
V_{SH}	Signal Out One Level	V_{DD}–.95 4.3	V_{DD} V_{DD}	V V	I_{SO}=20μA, 4.75V$\leqslant V_{DD} <$5.25V I_{SO}=20μA, 5.25V$\leqslant V_{DD} \leqslant$12.0V
V_{DD}	Logic Voltage Supply	4.75	12	V	
V_{BB}	Display Voltage Supply	20	60	V	
I_{DD}	Logic Supply Current		20 30	mA mA	No Loads, V_{DD}=5V No Loads, V_{DD}=10V
I_{BB}	Display Supply Current		6	mA	No Loads, T=25°C
V_{OL}	Output Zero Level	V_{SS}	1.0	V	I_O=–20μA
V_{OH}	Output One Level	V_{BB}–2.5	V_{BB}	V	I_O=25mA
t_{SD}	Serial Out Prop. Delay	60	375	ns	C_L=50pF
t_{PD}	Parallel Out Prop. Delay		5	μs	C_L=50pF
t_W	Input Pulse Width	375		ns	
t_{SU}	Data Set-Up Time	150		ns	
t_H	Data Hold Time	40		ns	

DISPLAY DRIVERS

Functional Description

Serial data present at the input is transferred to the shift register on the Logic "0" to Logic "1" transition of the clock input signal. On succeeding clock pulses, the registers shift data information towards the serial data output. The input serial data must be presented prior to the rising edge of the clock input waveform.

Information present at any register is transferred to its respective latch when the strobe signal is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the strobe signal is held high.

When the output disable input is high, all of the high voltage buffers are disabled without affecting the information stored in the latches or shift register. With the output disable signal low, the high voltage outputs are controlled by the state of the latches.

At low logic supply voltages, it is possible that the serial data output (DO) may be unstable for up to 2μs, after the rising edge of the strobe (STR) or output disable (OD) inputs.

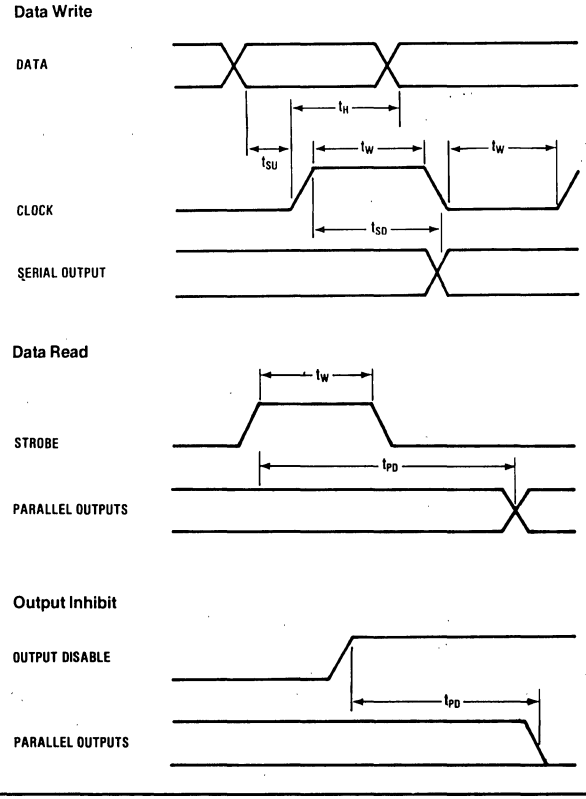
Table 1.

NUMBER OF OUTPUTS ON (I_{OUT} = 25mA)	MAX. ALLOWABLE DUTY CYCLE AT AMBIENT TEMPERATURE OF				
	25°C	40°C	50°C	60°C	70°C
10	100%	97%	85%	73%	62%
9	↑	100%	94%	82%	69%
8	↑	↑	100%	92%	78%
7	↑	↑	↑	100%	89%
6	↑	↑	↑	↑	100%
1	100%	100%	100%	100%	100%

Pin Description

Pin #	Name	Description
5	V_{SS}	Ground Connection
16	DO	Output of Shift Register—primarily used in cascading
13	OD	Output Disable
15	V_{BB}	Q Output Drive Voltage
4	CLK	System Clock Input
6	V_{DD}	Logic Supply Voltage
7	STR	Strobe to Latch Data from Registers
14	DI	Data Input to Shift Register
1-3, 8-12, 17-18	Q_1-Q_{10}	Direct Drive Outputs

Signal Timing Diagrams



GOULD
AMI Semiconductors

32 Bit, High Voltage Driver

S4535

Features

- ☐ High Voltage Outputs Capable of 60 Volt Swing
- ☐ Drives Up to 32 Devices
- ☐ Cascadable
- ☐ Requires Only 4 Control Lines

Applications:

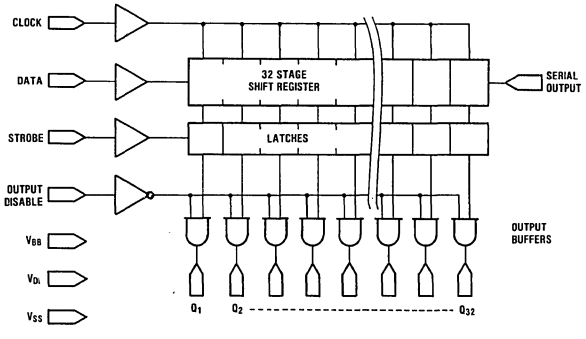
- ☐ Vacuum Fluorescent Displays
- ☐ LED and Incandescent Displays
- ☐ Solenoids
- ☐ Print Head Drives
- ☐ DC and Stepping Motors
- ☐ Relays

General Description

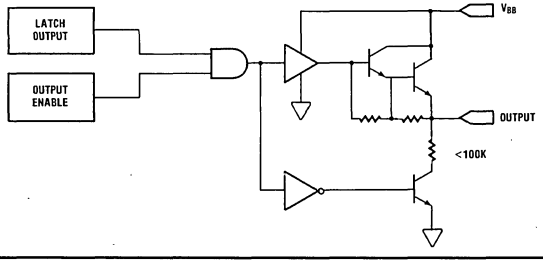
The S4535 is a high voltage MOS/LSI circuit that drives a variety of output devices, usually under microprocessor control, by converting low level signals such as TTL, and CMOS to high voltage, high current drive signals. This device requires only four control lines due to its serial input construction. It latches the data to be output, or it may be used to bring data directly to the driver. The part acts as a versatile peripheral to drive displays, motors, relays and solenoids within its output limitations of a 60 volt swing and up to 25mA per drive. It is especially well suited to drive vacuum fluorescent displays due to its high voltage output capability. One circuit will drive up to 32 devices and more can be driven by cascading several drivers together.

DISPLAY DRIVERS

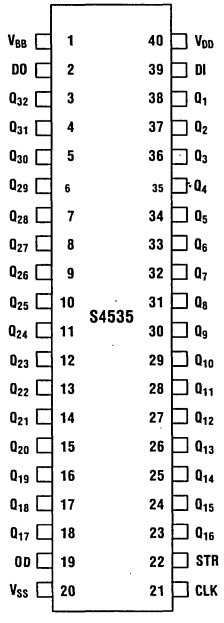
Functional Block Diagram



Output Buffer (Functional Diagram)



Pin Configuration



S4535

Absolute Maximum Ratings at 25°C

V_{BB}	65V
V_{DD}	12V
V_{IN}	V_{SS} – .3V to V_{DD} + .3V
V_{OUT} (Logic)	V_{SS} – .3V to V_{DD} + .3V
V_{OUT} (Display)	V_{SS} – .3V to V_{BB} + .3V
Power Dissipation	1.6W
Operating Temperature	–40°C to +85°C*
Storage Temperature	–65°C to +125°C

* Extended temperature range available. Please contact AMI for price and delivery information.

Operational Specification: $-40°C \leq T_A \leq +85°C$ (unless otherwise noted)

Symbol	Parameter	Min.	Max.	Units	Test Condition
V_{IL}	Input Zero Level	–0.3	0.8	V	
V_{IH}	Input One Level	3.5	$V_{DD}+0.3$	V	
V_{SL}	Signal Out Zero Level	V_{SS}	0.5	V	$I_{SO} = -20\mu A$
V_{SH}	Signal Out One Level	$V_{DD}-0.5$	V_{DD}	V	$I_{SO} = 20\mu A$
V_{DD}	Logic Voltage Supply	4.5	5.5	V	
V_{BB}	Display Voltage Supply	20	60	V	
I_{DD}	Logic Supply Current		35	mA	No Loads, T = 25°C
I_{BB}	Display Supply Current		10	mA	No Loads, T = 25°C
V_{OL}	Output Zero Level	V_{SS}	1.0	V	$I_O = -20\mu A$
V_{OH}	Output One Level	$V_{BB}-2.5$ $V_{BB}-3.2$	V_{BB} V_{BB}	V V	$I_O = 5mA$ $I_O = 25mA$, One Output
t_{SD}	Serial Out Prop. Delay		500	ns	$C_L = 50pF$
t_{PD}	Parallel Out Prop. Delay		5	μs	$C_L = 50pF$
t_W	Input Pulse Width	500		ns	
t_{SU}	Data Set-Up Time	150		ns	
t_H	Data Hold Time	50		ns	

Functional Description

Serial data present at the input is transferred to the shift register on the Logic "0" to Logic "1" transition of the clock input signal. On succeeding clock pulses, the registers shift data information towards the serial data output. The input serial data must be presented prior to the rising edge of the clock input waveform.

Information present at any register is transferred to its respective latch when the strobe signal is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the strobe signal is held high.

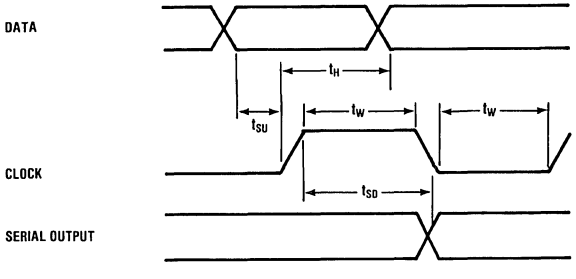
When the output disable input is high, all of the high voltage buffers are disabled without affecting the information stored in the latches or shift register. With the output disable signal low, the high voltage outputs are controlled by the state of the latches.

Pin Description

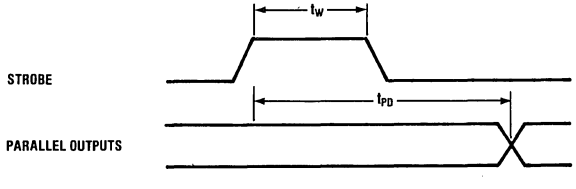
Pin #	Name	Description
20	V_{SS}	Ground Connection
2	DO	Output of Shift Register—primarily used for cascading
19	OD	Output Disable
1	V_{BB}	Q Output Drive Voltage
21	CLK	System Clock Input
40	V_{DD}	Logic Supply Voltage
22	STR	Strobe to Latch Data from Registers
39	DI	Data Input to Shift Register
3-18 and 23-38	Q_1-Q_{32}	Direct Drive Outputs

Signal Timing Diagrams

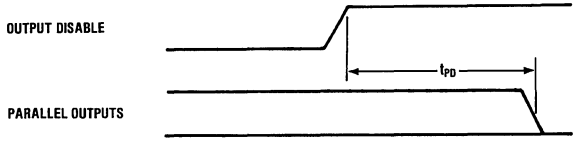
Data Write



Data Read



Output Inhibit



PLDs (PEELs™)

GOULD
AMI Semiconductors

CMOS E²PLD
Electrically Erasable Programmable Logic

PEEL™ 18CV8

Features

Advanced CMOS E²PROM Technology

Low Power Consumption
- TTL: 25mA Standby + 0.7mA/MHz Max

High Performance
- T_{PD} 25nS Max, T_{CO} 15nS Max, T_{SC} 20nS Min

Reprogrammability
- 100% factory tested
- Cost effective "window-less" package
- Erase/Program time in seconds
- Adds convenience, reduces field retrofit and development cost

Design Security
- Prevents unauthorized reading or copying of design

Architectural Flexibility
- 74 Product Term x 36 Input array
- Up to 18 Inputs and 8 I/O pins
- Independently configurable I/O macro cells: polarity, register, combinatorial, bi-directional
- Synchronous preset, asynchronous clear
- Independent output enables

Application Versatility
- Replace SSI/MSI logic
- Emulates bipolar PAL™ devices and the EP300/310
- Simplifies inventory control
- Allows new design possibilities

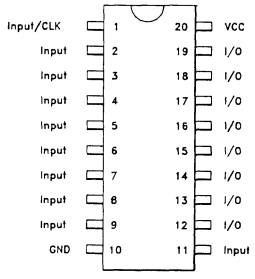
Development/Programmer Support
- Popular PC-based development tools and programmers

General Description

The Gould PEEL™ 18CV8 is a CMOS Programmable Electrically Erasable Logic device that provides a high performance, low power, reprogrammable, and architecturally flexible alternative to conventional programmable logic devices (PLDs). Designed in advanced CMOS E²PROM technology, the performance of the PEEL 18CV8 rivals speed parameters of standard bipolar PLDs with a dramatic improvement in power consumption. The electrically erasable reprogrammable technology of the PEEL

PLDs

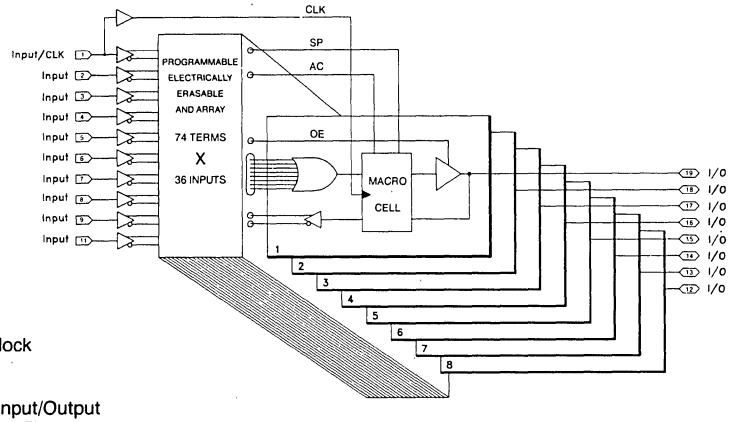
Pin Diagram
(Figure 1)



Pin Names

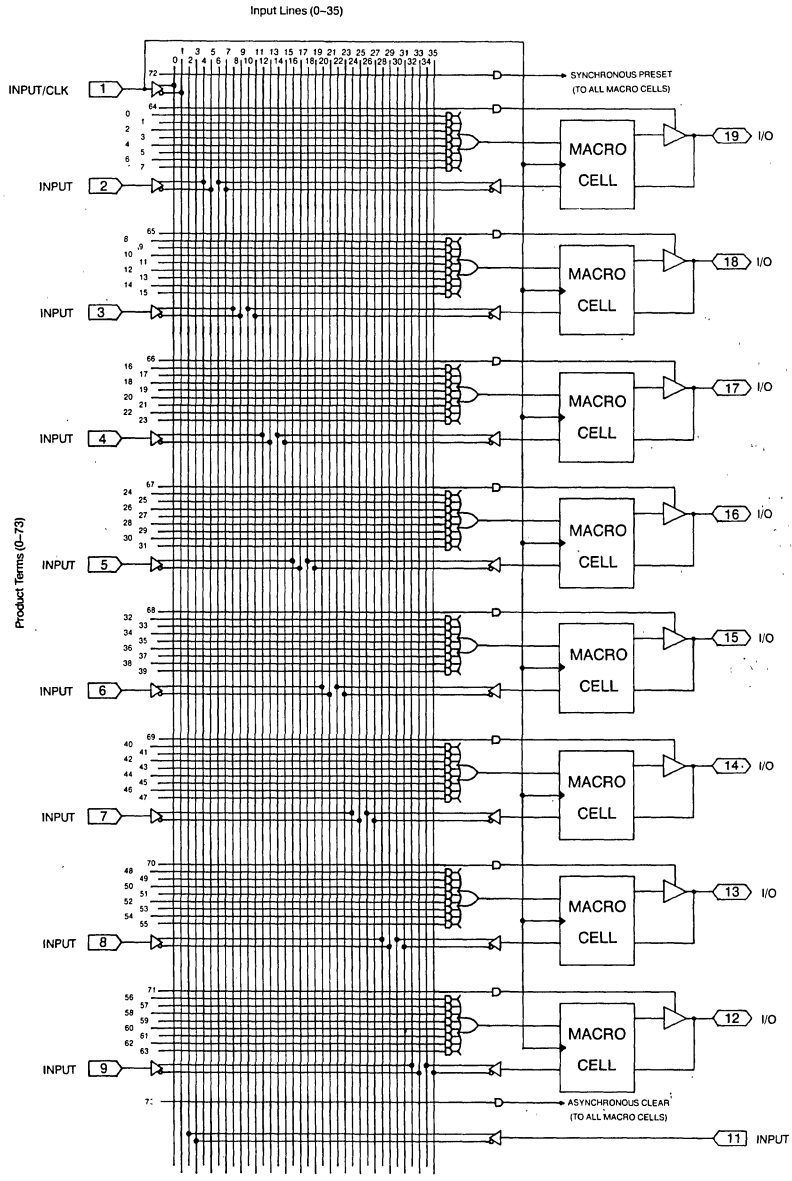
INPUT/CLK	Input and/or Clock
INPUT	Input
GND	Ground
I/O	Bi-Directional Input/Output
V_{CC}	Power Supply (+5V)

Block Diagram
(Figure 2)



SP = Synchronous Preset
AC = Asynchronous Clear
OE = Output Enable

Figure 3. PEEL18CV8 logic array diagram



18CV8 not only reduces development and field retrofit costs but enhances testability enabling Gould to ensure 100% field programmability and function.

Packaged in a cost-effective "window-less" 20 pin DIP, the flexible architecture of the PEEL 18CV8 allows for replacement of standard SSI/MSI logic circuitry or pin-out compatible emulation of 20-pin bipolar PAL devices and the Altera EP300/310. In addition, over a hundred new logic configurations, not possible with earlier generation PLDs, can be implemented. Primary development and programming support of the PEEL 18CV8 is provided by popular third-party PC based development tools and stand-alone programmers. Gould also offers a Development System specifically for the PEEL 18CV8 and other PEEL devices.

Architectural Overview

The basic architecture of the PEEL 18CV8 is similar to that of earlier generation PLDs to the extent that it utilizes a sum-of-products logic array in a programmable AND fixed OR structure. This familiar logic arrangement allows user defined output functions to be created by programming the connection of input signals into the array. What makes the architecture of the PEEL 18CV8 different, however, is the increased capability and flexibility it provides resulting in a higher level of equivalent gate integration and a simplification of design.

The block diagram in figure 2 illustrates the key elements of the PEEL 18CV8 architecture. Externally, the PEEL 18CV8 provides up to 18 inputs and 8 outputs for use. At the core is a programmable electrically erasable "AND array" of 36 input lines by 74 product terms. The 36 input lines are derived from the true and complements of the 18 possible input pins. The 74 product terms are made up of: 1 synchronous preset term, 1 asynchronous clear term, 8 output enable terms and 64 terms divided into groups of 8 each feeding into an OR function.

Each OR function is directly associated with one of eight macro cells and I/O pins. An individual macro cell can be programmed into one of twelve different configurations. Depending on the configuration, the output of the macro cell can be fed back into the array or output via its associated I/O pin. The configurations include various arrangements for bi-directional I/O, registered or combinatorial feedback, registered or combinatorial output and output polarity control. The output enable term of each I/O pin can be used to force a high impedance state for bi-directional I/O operations or for dedicated input usage. The synchronous preset term, asynchronous clear term and clock (pin 1, I/CLK) are globally routed to all macro cells.

Logic Array Operation

A more detailed view of the overall architecture, specifically the logic array, is illustrated by the PEEL 18CV8 Logic Array diagram in figure 3. As referred to previously, the logic array of the PEEL 18CV8 consists of:

- 36 Input Lines:
  - 10 true and complement inputs
  - 8 true and complement inputs/feedbacks
- 74 Product Terms:
  - 64 product terms (8x8 Sum-of-Products form)
  - 8 output enable product terms
  - 1 synchronous preset term
  - 1 asynchronous clear term

Looking at the logic array diagram, the 36 input lines (0–35) run vertically and the 74 product terms (0–73) run horizontally. Each input line and product term intersection in the array has an associated programmable E²PROM memory cell that determines whether the intersection is connected or open. A connection allows an input line to become a logical input of the intersected product term (AND gate). Thus, each product term, although unlikely in a real application, truly equals a 36 input AND gate.

In figure 3, the logic array has 64 product terms that are divided into groups of 8 each feeding into a sum (OR gate). By connecting specific inputs or I/O macro cell feedbacks to the product terms, complex sum-of-products logic functions can be created. Each sum feeds into its associated I/O macro cell where the logic function can be further controlled for output to an I/O pin or feedback into the array.

In addition to the 64 product terms of the 8 sum-of-product groups, there are 8 output enable product terms, 1 synchronous preset product term and 1 asynchronous clear product term. These additional terms are used to directly control specific I/O functions which are covered in the following section.

I/O Macro Cell and Output Enable Operation

A great amount of architectural flexibility is provided by the PEEL 18CV8's reconfigurable I/O macro cells and independently controlled output enables. A closer look at the I/O macro cell, figure 4, shows that it consists of a D-type flip-flop and two signal select multiplexers.

The D-type flip-flop operates similarly to standard TTL D flip-flops to the extent that the D input is latched on the rising edge (LOW to HIGH transition) of the CLK input and Q or $\overline{Q}$ output signals can be used. Two additional inputs are controlled by the asynchronous clear and synchronous preset terms.

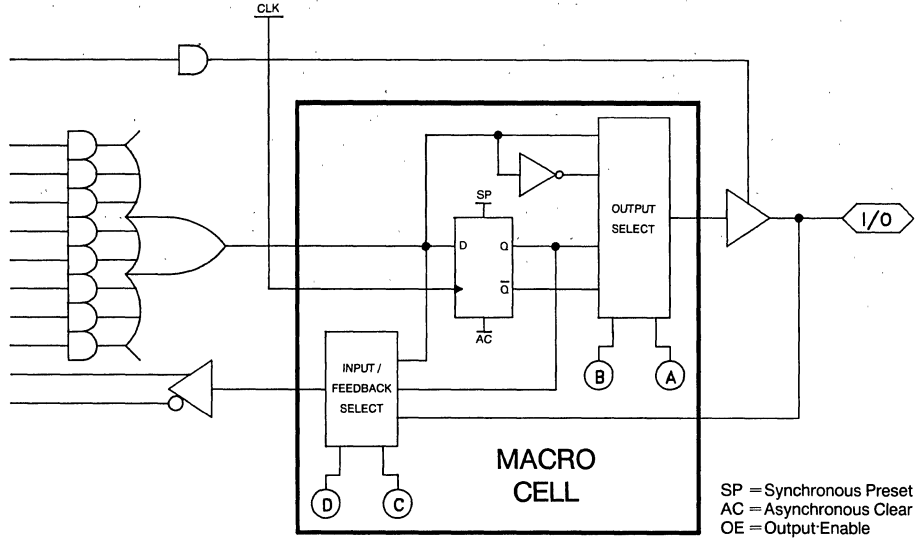
When the asynchronous clear product term is asserted (HIGH) the Q output will immediately be set to a LOW regardless of the clock state. When the synchronous preset term is asserted (HIGH) the Q output will be set to a HIGH on the following rising edge (LOW to HIGH transition) of the CLK input. Priority is given to the asynchronous clear signal if both asynchronous clear and synchronous preset have been asserted. Upon power-up, the asynchronous clear function is automatically performed setting the Q outputs of all macro cell flip-flops to a LOW.

The two signal select multiplexers of each macro cell are controlled by four E²PROM programmable bits (A,B,C and D) that determine which of the twelve possible configurations the macro cell will assume. This independent flexibility allows a single PEEL 18CV8 to implement a combination of configurations among its eight macro cells. The configurations include various arrangements for bi-directional I/O, registered or combinatorial feedback, registered or combinatorial output and output polarity control. The twelve possible I/O macro cell configurations are listed in table 1. Their equivalent circuits are illustrated in figure 5.

Table 1. PEEL18CV8 macro cell configurations

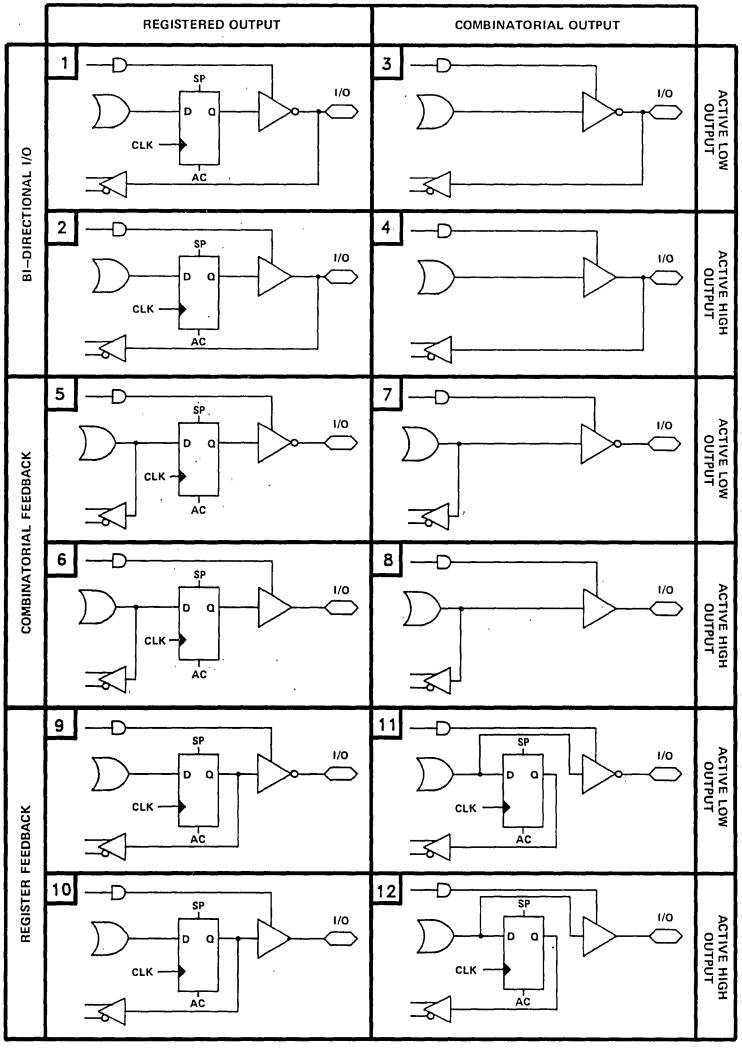
Configuration					Input/Feedback Select	Output Select	
#	A	B	C	D			
1	1	1	1	1	Bi-Directional I/O	Register	Active Low
2	0	1	1	1			Active High
3	1	0	1	1		Combinatorial	Active Low
4	0	0	1	1			Active High
5	1	1	1	0	Combinatorial Feedback	Register	Active Low
6	0	1	1	0			Active High
7	1	0	1	0		Combinatorial	Active Low
8	0	0	1	0			Active High
9	1	1	0	0	Register Feedback	Register	Active Low
10	0	1	0	0			Active High
11	1	0	0	0		Combinatorial	Active Low
12	0	0	0	0			Active High

Figure 4. PEEL 18CV8 macro cell diagram



Each of the 8 output enable terms can enable or disable the output of its associated I/O macro cell. When the output enable product term is a logical true (HIGH) the output signal is enabled to the I/O pin. When it is a logical false (LOW) the I/O pin is in a high impedance state. The output enable product terms allow individual I/O pins to be input only or bi-direction I/O.

Figure 5. PEEL 18CV8 macro cell configuration equivalent circuits



Applications of the PEEL 18CV8

The versatility of the PEEL makes it an effective alternative to conventional methods of logic design over a broad range of applications.

As an SSI/MSI logic replacement, the PEEL enhances the design process with increased flexibility, higher performance, faster development time and design security. Manufacturing benefits are also realized by requiring fewer components and interconnects resulting in more efficient use of space, simplified inventory control and higher reliability.

As a bipolar PAL replacement, the PEEL has comparable speed yet offers several advantages including: enhanced design flexibility, simplified inventory control, reduced power consumption, reprogrammability, and 100% factory testability for function and programming.

Design flexibility is of particular importance since the PEEL 18CV8 not only emulates the majority of the 20 pin PAL devices (see table 2) but also allows functions found among several PAL device types to be combined. In addition, completely new functions, not supported by the standard PAL devices, can be implemented. This flexibility means a designer can focus on the design rather than on the restrictions of a fixed architecture. Reprogrammability is also a key benefit over one time programmable PALs. This feature adds convenience and cost savings in development prototyping and field retrofitting of systems. Converting existing PAL designs to the PEEL 18CV8 for plug-in replacement is easily accomplished using the PEEL evaluation or development tools described later in this data sheet.

As a design alternative to low-density gate arrays, one or more PEEL 18CV8s offer a cost-effective and low-risk option. With its architectural flexibility and equivalent gate density of approximately 300 gates, designs traditionally employing low-density gate arrays can be implemented quickly at no factory development (NRE) cost. Unlike the lead times encountered with gate arrays, the PEEL 18CV8 is off-the-shelf available. Futhermore, if a design error is made or an upgrade is necessary, the changes can simply be reprogrammed.

Similar to SSI/MSI logic, PALs and low density gate arrays, applications of the PEEL 18CV8 cover all the primary areas of system design including, data processing, communications, industrial, consumer, military and transportation. Specific functions implemented using the PEEL 18CV8 range from basic logic and system support circuitry to stand-alone controllers. Some of these applications possibilities include:

- **SSI/MSI Logic Replacement/Customization**
  - Random logic
  - Decoders/encoders
  - Comparators
  - Multiplexers
  - Counters
  - Shift registers
- **Processor System Support**
  - Address decoding
  - Wait-state generation
  - Memory protection
  - Memory refresh
  - DMA control
  - Interrupt control
  - Timer/Counter functions
  - Bus arbitration and interface
  - Error detection and correction
- **I/O Interface and Support**
  - Intelligent I/O port
  - Data Comm interface
  - Display interface
  - Keyboard scanning
  - Disk and tape drive control
  - Front panel interface
- **Stand-Alone Non μP Based Controllers**
  - Motor control
  - Sensor monitoring
  - Security access control
  - Display Control

Table 2. PLD devices that can be emulated by the PEEL 18CV8

20-pin PAL

Output Type	Part Number and I/O Capacity								
Combinatorial-High	10H8	12H6	14H4	16H2			16H8	16HD8	
Combinatorial-Low	10L8	12L6	14L4	16L2			16L8	16LD8	
Combinatorial-Polarity							16P8		18P8
Registered-Low					16R4	16R6	16R8		
Registered-Polarity					16RP4	16RP6	16RP8		

ALTERA

EP 300/310

Absolute Maximum Ratings*8

Symbol	Parameter	Conditions	MIN	MAX	UNIT
V_{CC}	Supply Voltage	relative to GND	−.5	7.0	V
V_I	Voltage applied to Input*10	relative to GND*1,2	−.5	7.0	V
V_O	Voltage applied to Output	relative to GND*1,2	−.5	7.0	V
I_O	Output Current	per pin (I_{OL},I_{OH})		±25	mA
T_{ST}	Storage Temperature		−65	+125	°C
T_{LT}	Lead Temperature	(soldering 10 seconds)		+300	°C

Operating Ranges

Symbol	Parameter	Conditions	MIN	MAX	UNIT
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
T_A	Operating Temperature	Commercial	0	+70	°C
T_R	Clock Rise Time	*5		500	nS
T_F	Clock Fall Time	*5		500	nS
T_{RVCC}	V_{CC} Rise Time	*5		10	mS

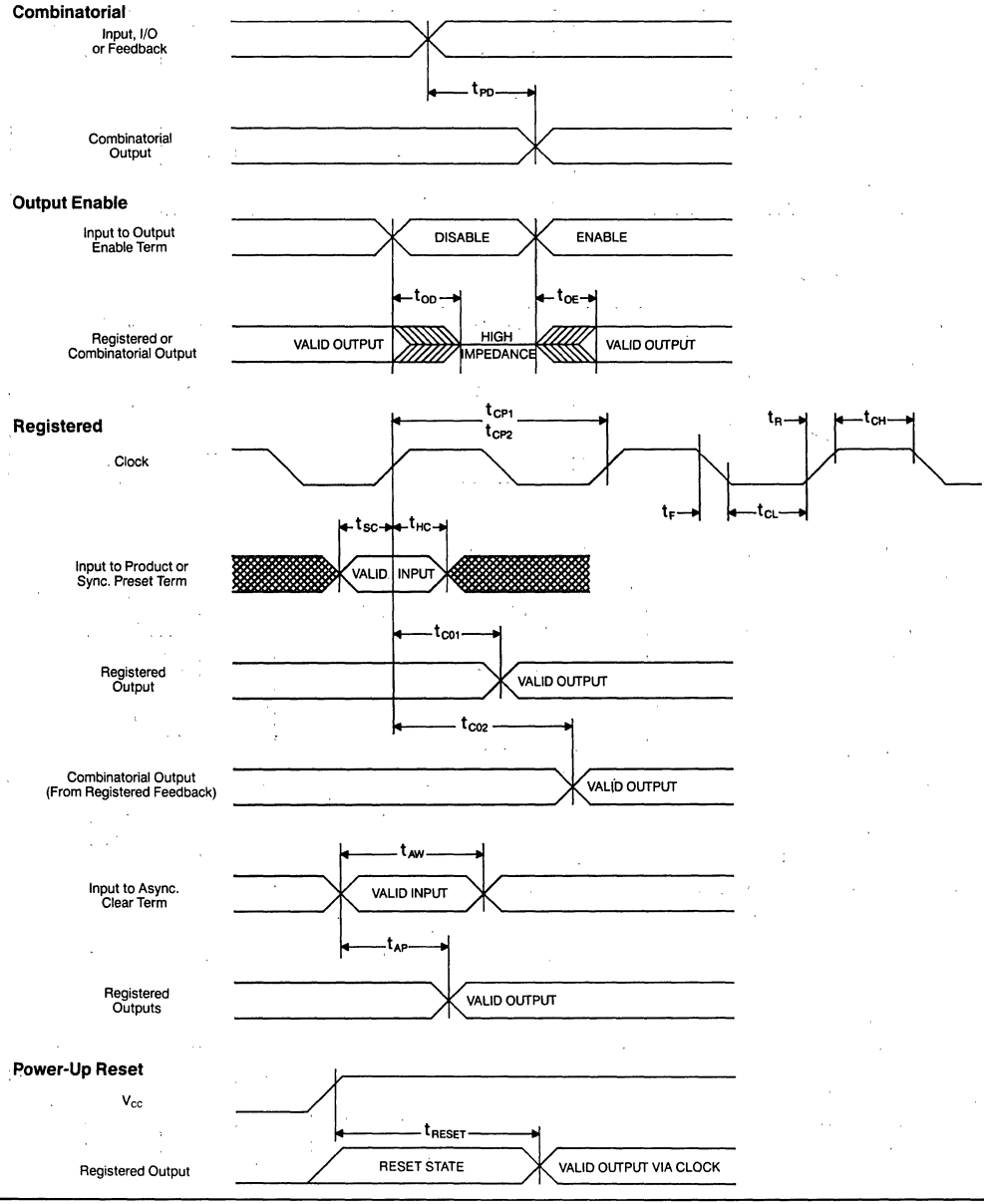
D.C. Characteristics (Over Operating Range Specifications)

Symbol	Parameter	Conditions	MIN	TYP*7	MAX	UNIT
I_{CCS}	V_{CC} Current Standby	$V_{IN}=V_{IL}$ or V_{IH} *9		12	25	mA
I_{CCA}	V_{CC} Current Active	$V_{IN}=V_{IL}$ or V_{IH}, All inputs, feedback and I/O switching. *9			I_{CCS} + .7 mA/MHz	mA
I_{IL}	Input Leakage	V_{IN}=GND to V_{CC}			±10	uA
I_{OZ}	Output Leakage	I/O = High Impedance, V_O=GND to V_{CC}			±10	uA
V_{IL}	Input Low Voltage		−0.3		.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}+0.3	V
V_{OL}	Output Low Voltage	I_{OL}=+8.0mA *12			.45	V
V_{OLC}	Output Low Voltage CMOS	I_{OL}=10μA			0.1V	V
V_{OH}	Output High Voltage TTL	I_{OH}=−4.0mA	2.4			V
V_{OHC}	Output High Voltage CMOS	I_{OH}=−10μA	V_{CC}−0.1V			V

Capacitance*3

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance	f=1MHz		4	6	pf
C_{OUT}	Output Capacitance	f=1MHz		8	12	pf
C_{CLK}	Clock Pin Capacitance	f=1MHz		8	13	pf

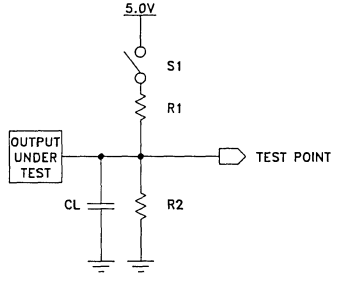
A.C. Switching Waveforms



A.C. Characteristics (Over Operating Range Specifications)

Symbol	Parameter	Conditions	18CV8-25		18CV8-35		18CV8-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PD}	Input*4 to combinatorial output			25		35		50	nS
t_{OD}	Input*4 to output disable	*6		25		35		50	nS
t_{OE}	Input*4 output enable	*6		25		35		50	nS
t_{SC}	Input*4 set-up to clock		20		30		32		nS
t_{HC}	Input*4 hold after clock		0		0		0		nS
t_{CL}	Clock low time	*5	15		15		20		nS
t_{CH}	Clock high time	*5	15		15		20		nS
t_{CO1}	Clock to output			15		20		28	nS
t_{CO2}	Clock to combinatorial output delay via registered feedback			35		50		70	nS
t_{CP1}	Minimum clock period (register feedback to register output via internal path)			30		45		42	nS
f_{MAX1}	Max. frequency ($1/t_{CP1}$)		35.3		22.2		23.8		MHz
t_{CP2}	Minimum clock period ($t_{SC} + t_{CO1}$)			35		50		60	nS
f_{MAX2}	Max. frequency ($1/t_{CP2}$)		28.5		20		16.6		MHz
t_{AW}	Async. clear pulse width	*11	25		35		50		nS
t_{AP}	Input*4 to async. clear			30		40		55	nS
t_{RESET}	Power-on reset time for registers in clear state	*5		5		5		5	uS

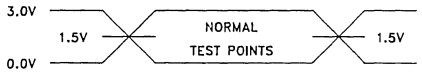
A.C. Equvialent Load Circuit



TTL Levels
R1 = 464Ω
R2 = 250Ω

CMOS Levels
R1 = 480KΩ
R2 = 480KΩ

A.C. Testing Input/Output Waveform



A.C. Test Point/Load Circuit Table

AC TEST	TEST POINT	CL	S1
NORMAL	1.5V	30pf	closed
tOE(Z→1)	VOH	30pf	open
tOE(Z→0)	VOL	30pf	closed
tOD(1→Z)	VOH-.5V	5pf	open
tOD(0→Z)	VOL+.5V	5pf	closed

Z=High Impedance

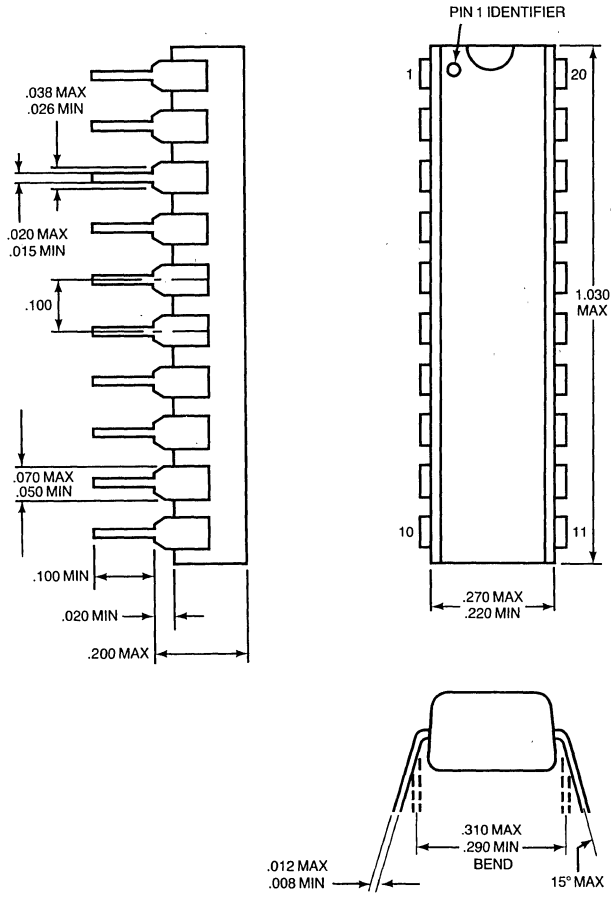
Notes

*1 Minimum DC input is −.5V, however, inputs may undershoot to −2.0V for periods less than 20ns.
*2 Voltage applied to input or output must not exceed V_{CC} + 1.0V.
*3 These measurements are periodically sample tested.
*4 "Input" refers to an Input signal.
*5 Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
*6 See A.C. test point / load circuit table for t_{OE}, and t_{OD} testing.
*7 Typical values and capacitance are measured at V_{CC} = 5.0V and T_A = 25°C.
*8 Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.
*9 I/O pins are open (no load).
*10 V_{IN} specified is not for program/verify operation. Contact Gould for information regarding PEEL 18CV8 program/verify specifications.
*11 Minimum width required to ensure proper asynchronous clear operation and does not imply rejection of signal less than this value.
*12 Contact factory for increased IOL requirements.

PLDs

Packaging

20-Pin Plastic



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CMOS Programmable Electrically Erasable Logic Device

Preliminary Data Sheet

PEEL™ 18CV8-15

Features

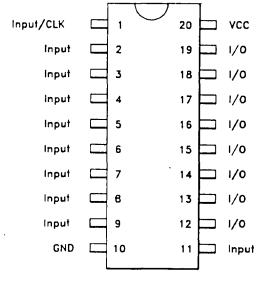
- **Advanced CMOS EEPROM Technology**
- **Low Power Consumption**
  —TTL: 90mA standby +0.7mA/MHz max
- **High Performance**
  —t_{PD} = 15ns max
  —t_{CO} = 12ns max, t_{SC} = 12ns min
- **EE Instant Reprogrammability**
  —100% factory tested
  —Cost-effective windowless package
  —Erases and programs in seconds
  —Adds convenience, reduces field retrofit and development costs
- **Foolproof Design Security**
  —Prevents unauthorized reading or copying of design
- **Architectural Flexibility**
  —74 product term x 36 input array
  —Up to 18 inputs and 8 I/O pins
  —Independently configurable I/O macro cells
  —Synchronous preset, asynchronous clear
  —Independent output enables
- **Application Versatility**
  —Replaces SSI/MSI logic
  —Emulates bipolar PAL* devices and EPLDs
  —Simplifies inventory control
  —Allows new design possibilities
- **Development/Programmer Support**
  —PC-based development tools and programmer support from Gould and third-party manufacturers

General Description

The Gould PEEL18CV8-15 is a CMOS Programmable Electrically Erasable Logic device that provides a high-performance, low-power, reprogrammable, and architecturally flexible alternative to early-generation programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the performance of the PEEL18CV8-15 rivals speed parameters of bipolar PLDs with a dramatic reduction in power consumption.

PLDs

Pin Configuration



Pin Names

INPUT/CLK	Input and/or Clock
INPUT	Input
GND	Ground
I/O	Bi-Directional Input/Output
V_{CC}	Power Supply (+5V)

Figure 1. Pinout for DIP

Block Diagram

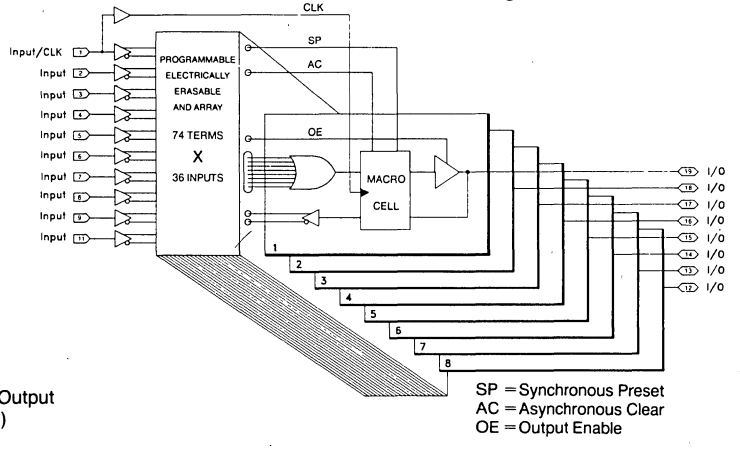


Figure 2. Block diagram of the PEEL18CV8

PEEL™ 18CV8-15

EE reprogrammability simplifies inventory management, reduces development and field retrofit costs, enhances testability to ensure 100% field programmability and function, while allowing for low-cost "windowless" packaging in a 20-pin, 300-mil DIP. The PEEL18CV8-15's flexible architecture allows the device to replace SSI/MSI logic circuitry. Gould's JEDEC file translator allows the PEEL18CV8-15 to replace existing 20-pin PLDs without the need to rework the existing design. Development and programming support for the PEEL18CV8-15 is provided by popular third-party PC-based development tools and programmers from third-party manufacturers. Gould also offers a free design software package and a low-cost development system.

Absolute Maximum Ratings Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	−0.5 to +7.0	V
V_I, V_O	Voltage Applied to Any Pin[6]	Relative to GND [4,5,9]	−0.5 to V_{CC} +0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	±25	mA
T_{ST}	Storage Temperature		−65 to +125	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
T_A	Ambient Temperature	Commercial	0	+70	°C
T_R	Clock Rise Time	See Note 3		250	ns
F_F	Clock Fall Time	See Note 3		250	ns
T_{RVCC}	V_{CC} Rise Time	See Note 3		10	ms

D.C. Electrical Characteristics Over the operating range.

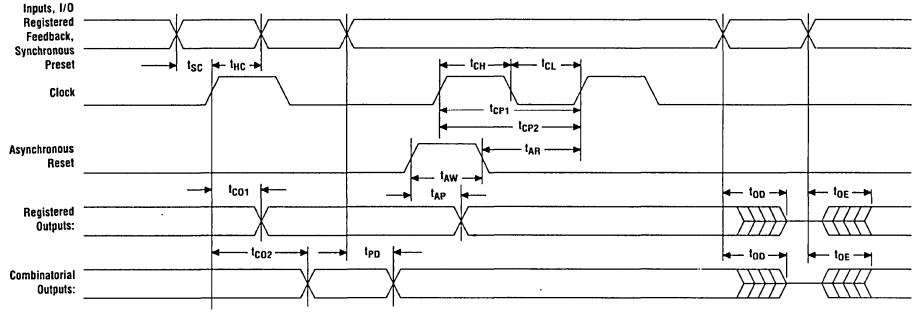
Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage—TTL	V_{CC}=Min, I_{OH}=−4.0mA	2.4		V
V_{OL}	Output HIGH Voltage—CMOS	V_{CC}=Min, I_{OH}=−10μA	V_{cc} −0.1		V
V_{OHC}	Output LOW Voltage—TTL	V_{CC}=Min, I_{OL}=−12mA		0.45	V
V_{OLC}	Output LOW Voltage—CMOS	V_{CC}=Min, I_{OL}=10μA		0.1	V
V_{IH}	Input HIGH Level		2.0	V_{CC}+0.3	V
V_{IL}	Input LOW Level		−0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC}=Max, GND≤V_{IN}≤V_{CC}		±10	μA
I_{OZ}	Output Leakage Current	I/O=High-Z, GND≤V_O≤V_{CC}		±10	μA
I_{SC}	Output Short Circuit Current	V_{CC}=Max, V_O=0.5V[10]	−30	−100	mA
I_{CCST}	V_{CC} Current, Standby, TTL	V_{IN}=V_{IL} or V_{IH}[7]		90	mA
I_{CCAT}	V_{CC} Current, Active, TTL	V_{INI}=V_{IL} or V_{IH}. All outputs open.[7]		I_{CCST}+ 0.7mA/MHz	mA
C_{IN}[8]	Input Capacitance	T_A=25°C, V_{CC}=5.0V @ f=1MHz		6	pF
C_{OUT}[8]	Output Capacitance	T_A=25°C, V_{CC}=5.0V @ f=1MHz		12	pF

PEEL™18CV8-15

A.C. Electrical Characteristics Over the Operating Range[3]

Symbol	Parameter	Min	Max	Unit
t_{PD}	Input[4] or feedback to non-registered output		15	nS
t_{OE}	Input[4] to output enable[6]		15	nS
t_{OD}	Input[4] to output disable[6]		15	nS
t_{CO1}	Clock to output		12	nS
t_{CO2}	Clock to combinational output delay via internal registered feedback		25	nS
t_{SC}	Input[4] or feedback setup to clock	12		nS
t_{HC}	Input[4] hold after clock	0		nS
t_{CL}, t_{CH}	Clock width—clk low time, clk high time[5]	10		nS
t_{CP1}	Minimum clock period (register feedback to registered output via internal path)	20		nS
f_{max1}	Maximum clock frequency ($1/t_{CP1}$)	50		MHz
f_{CP2}	Minimum clock period ($t_{SC}+t_{CO1}$)	24		nS
f_{max2}	Maximum clock frequency ($1/t_{CP2}$)	41.6		MHz
t_{AW}	Asynchronous clear pulse width	15		nS
t_{AP}	Input[4] to asynchronous clear		20	nS
t_{AR}	Asynchronous Reset Recovery Time		10	nS
t_{RESET}	Power-on reset time for registers in clear state		5	μS

Switching Waveforms



Notes:

1. "Input" refers to Input pin signal.
2. See A.C. test-point/load-circuit table for t_{OE} and t_{OD} testing.
3. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
4. Minimum DC input is −0.15V, however, inputs may undershoot to −2.0V for periods of less than 20ns.
5. Voltage applied to an input or output must not exceed V_{CC} +1.0V.
6. V_{IN} specified is not for program/verify operation. Contact Gould for information regarding PEEL18CV8 program/verify specifications.
7. I/O pins are open (no load).
8. These measurements are periodically sample tested.
9. Total output current sourced from device not to exceed I_{SC}.
10. Test one output at a time for a duration less than 1 second.
11. Specification for minimum pulse width that will guarantee asynchronous clear operation. However, it is possible that pulses of shorter duration may trigger asynchronous clear operation.

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CMOS Programmable Electrically Erasable Logic Device

Preliminary Data Sheet

PEEL™20CG10

Features

- **Advanced CMOS EEPROM Technology**
- **High Performance with Low Power Consumption**
  - —t_{PD} =25ns max, t_{CO} =15ns max
  - —t_{CC} =55mA+0.5mA/MHz max
- **EE Reprogrammability**
  - —Superior programming and functional yield
  - —Low cost windowless package
  - —Erases and programs in seconds
- **Development and Programming Support**
  - —Third-party software and programmers
  - —Gould PEEL Development System with APEEL™ Logic Assembler
- **Architectural Flexibility**
  - —92 product term x 44 input AND array
  - —Up to 22 inputs and 10 outputs
  - —Independently programmable 12-configuration I/O macrocells
  - —Synchronous preset, asynchronous clear
  - —Independent programmable output enables
- **Application Versatility**
  - —Replaces random SSI/MSI logic
  - —Emulates 24-pin bipolar PAL devices
  - —Convert 24-pin PAL and EPLD designs with Gould software
  - —Superset compatible with the CMOS PALC20G10

General Description

The Gould PEEL20CG10 is a CMOS Programmable Electrically Erasable Logic Device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to conventional programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PEEL20CG10 rivals speed parameters of comparable bipolar PLDs while dramatically improving power consumption. EE reprogrammability simplifies inventory management, reduces development and field retrofit costs, enhances testability to ensure 100% field programmability and function, while allowing for low-cost "windowless" packaging in a 24-pin, 300-mil DIP.

Pin Configuration

Pin Names

I/CLK = Input Only/Clock
I = Input Only
I/O = Bi-Directional Input/Output
GND = Ground
Vcc = Power Supply (+5V)

Figure 1. DIP pinout

Block Diagram

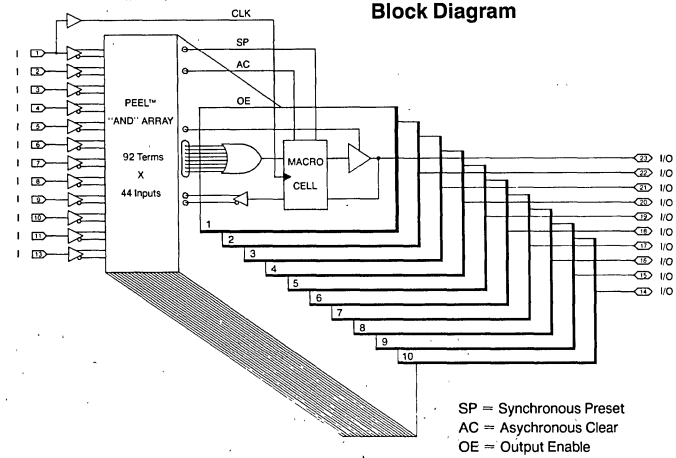
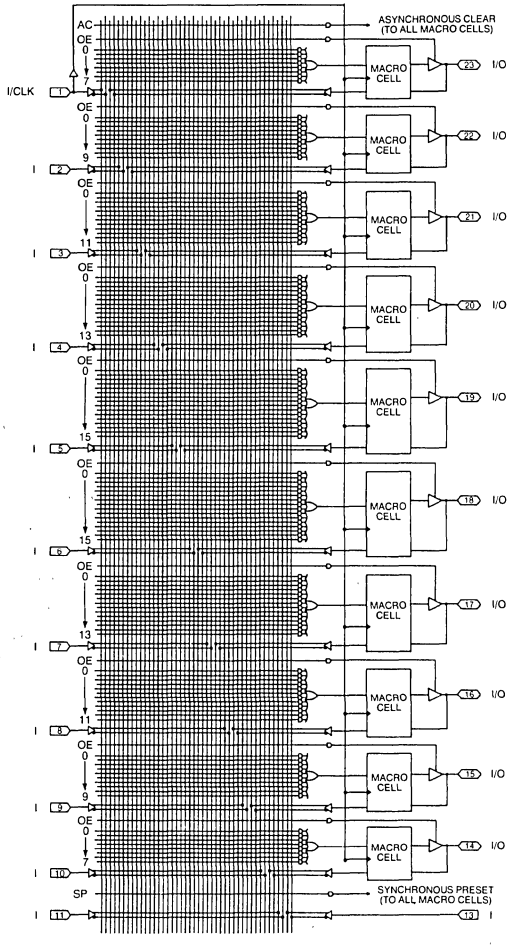


Figure 2. Block diagram of the PEEL20CG10

PEEL™ 20CG10

The PEEL20CG10's flexible architecture and Gould's JEDEC file translator allows the PEEL20CG10 to replace bipolar 24-pin PAL devices without the need to rework the existing design. Applications for the PEEL20CG10 include: replacement of random SSI/MSI logic circuitry; emulation of 24-pin bipolar PAL devices; and user customized sequential and combinational functions such as counters, shift registers, state machines, address decoders, multiplexers, etc. Development and programming support for the PEEL20CG10 is provided by Gould and third-party manufacturers.

Figure 3. PEEL20CG10 Logic Array Diagram



Function Description

The PEEL20CG10 implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview

The PEEL20CG10 architecture is illustrated in the block diagram of figure 2. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure the PEEL20CG10 can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is an I/O macrocell which can be independently programmed to one of 12 different configurations. The programmable macrocells allow each I/O to create sequential or combinational logic functions of active-high or active-low polarity, while providing three different feedback paths into the AND array.

AND/OR Logic Array

The programmable AND array of the PEEL20CG10 (shown in figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 Input Lines:

- 24 input lines carry the true and compliment of the signals applied to the 12 input pins
- 20 additional lines carry the true and compliment values of feedback or input signals from the ten I/Os

92 product terms:

- 80 product terms (8 per I/O) used to form logical sums
- 10 output enable terms (one for each I/O)
- 1 global synchronous present term
- 1 global asynchronous clear term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term which is connected to both the true and compliment of an input signal will always be FALSE and thus will not affect the OR function that it drives. When all the connections on a product term are opened, a don't care state exists and that term will always be TRUE.

When programming the PEEL20CG10, the device programmer first performs a bulk erase to instantly remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program all of the connections on unused product terms so that they will have no effect on the output function.)

Programmable I/O Macrocell

The unique twelve-configuration output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL20CG10 to the precise requirements of their designs.

Macrocell Architecture

Each I/O macrocell, as shown in figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configurations of each macrocell is determined by the four EEPROM bits controlling these multiplexers. These bits determine: output polarity; output type (registered or non-registered); and input/feedback path (bi-directional I/O, combinational feedback, or register feedback). Refer to table 1 for details.

Equivalent circuits for the twelve macrocell configurations are illustrated in figure 5. In addition to emulating the four PAL-type output structures (configurations 3, 4, 9 and 10) the macrocell provides eight configurations that are unavailable in any PAL device. When creating a PEEL device design, the desired macrocell configuration generally is specified explicitly in the design file. When the design is assembled or compiled, the macrocell configuration bits are defined in the last lines of the JEDEC programming file.

Output Type

The signal from the OR array can be fed directly to the output pin or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising

edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity

Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the ouput enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select

The PEEL20CG10 macrocell also provides control over the feedback path. The input/feedback signal associated with each I/O macrocell may be obtained from three different locations: from the I/O pin (bi-directional I/O); directly from the Q output of the flip-flop (registered feedback) or directly from the OR gate (combinational feedback).

Bi-directional I/O

The input/feedback signal is taken from the I/O pin when using the pin as a dedicated input or as a bi-directional I/O. (Note that it is possible to create a registerd output function with bi-directional I/O.)

Combinational Feedback

The signal-select multiplexer gives the macrocell the ability to feedback the output of either the OR gate, bypassing the ouput buffer, regardless of whether the output function is registered or combinational. This feature allows the creation of asynchronous latches, even when the output must be disabled. (Refer to configurations 5, 6, 7, and 8 in figure 5.)

Figure 4. Block Diagram of the PEEL20CG10 Macrocell

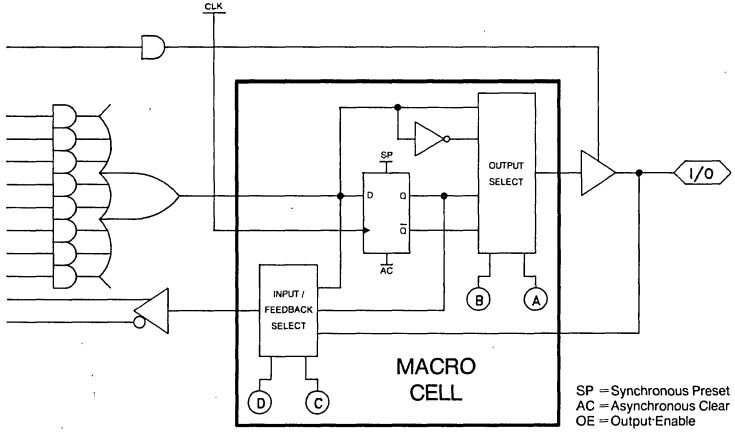


Figure 5. Equivalent Circuits for the Twelve Configurations of the PEEL20CG10 I/O Macrocell.

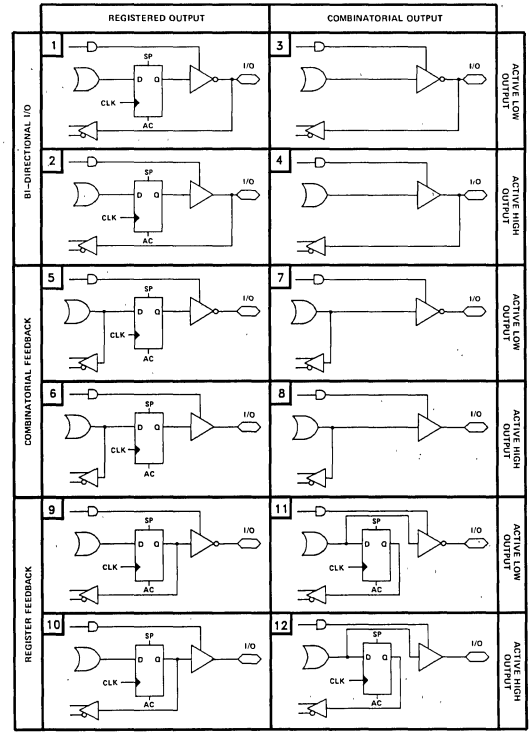


Table 1. PEEL20CG10 Macrocell Configuration Bits

Configuration					Input/Feedback Select	Output Select	
#	A	B	C	D			
1	0	0	1	0	Bi-Directional I/O	Register	Active Low
2	1	0	1	0	Bi-Directional I/O	Register	Active High
3	0	1	0	0	Bi-Directional I/O	Combinatorial	Active Low
4	1	1	0	0	Bi-Directional I/O	Combinatorial	Active High
5	0	0	1	1	Combinational Feedback	Register	Active Low
6	1	0	1	1	Combinational Feedback	Register	Active High
7	0	1	0	1	Combinational Feedback	Combinatorial	Active Low
8	1	1	0	1	Combinational Feedback	Combinatorial	Active High
9	0	0	1	0	Register Feedback	Register	Active Low
10	1	0	1	0	Register Feedback	Register	Active High
11	0	1	0	0	Register Feedback	Combinatorial	Active Low
12	1	1	0	0	Register Feedback	Combinatorial	Active High

Registered Feeback

Feedback also can be taken from the register, regardless of whether the output function is to be combinational or registered. When implementing combinational output function, registered feedback allows for the internal latching of states without giving up the use of the external output.

Design Security

The PEEL20CG10 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

Signature Word

The signature word feature allows a 24-bit code to be programmed into the PEEL20CG10. This code then can be read back even after the security bit has been set. The signature word can be used to identify the pattern that has been programmed into the device or to record the date of programming, design revision, etc.

Absolute Maximum Ratings Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	−0.5 to +7.0	V
V_I, V_O	Voltage Applied to Any Pin[3]	Relative to GND [1,2]	−0.5 to V_{CC} +0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	±25	mA
T_{ST}	Storage Temperature		−65 to +125	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+300	°C

Operating Ranges

Symbol	Alternate Source Symbol*	Parameter	Conditions	Min	Max	Unit
V_{CC}	V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
T_A	T_A	Ambient Temperature	Commercial	0	70	°C
T_R		Clock Rise Time	See Note 4		250	ns
F_F		Clock Fall Time	See Note 4		250	ns
T_{RVCC}		V_{CC} Rise Time	See Note 4		10	ms

D.C. Electrical Characteristics Over the operating range.

Symbol	Alternate Source Symbol*	Parameter	Conditions	Min	Max	Unit
V_{OH}	V_{OH}	Output HIGH Voltage—TTL	V_{CC}=Min, I_{OH}=−4.0mA	2.4		V
V_{OL}	V_{OL}	Output LOW Voltage—TTL	V_{CC}=Min, I_{OL}=8mA		0.5	V
V_{IH}	V_{IH}	Input HIGH Level		2.0	V_{CC}+0.3	V
V_{IL}	V_{IL}	Input LOW Level		−0.3	0.8	V
I_{IX}	I_{IX}	Input Leakage Current	V_{CC}=Max, GND≤V_{IN}≤V_{CC}		±10	μA
I_{OZ}	I_{OZ}	Output Leakage Current	I/O=High-Z, GND≤V_O≤V_{CC}		±10	μA
I_{SC}	I_{SC}	Output Short Circuit Current	V_{CC}=Max, V_O=0.5V[10]	−30	−90	mA
I_{CCST}	I_{CC}	V_{CC} Current, Standby, TTL	V_{IN}=V_{IL} or V_{IH}[5]		55	mA
I_{CCAT}	I_{CC}	V_{CC} Current, Active, TTL	V_{IN}=V_{IL} or V_{IH}[5]		I_{CCST}+ 0.5mA/MHz	mA
C_{IN}[8]	C_{IN}	Input Capacitance	T_A=25°C, V_{CC}=5.0V @ f=1MHz		6	pF
C_{OUT}[8]	C_{OUT}	Output Capacitance	T_A=25°C, V_{CC}=5.0V @ f=1MHz		12	pF

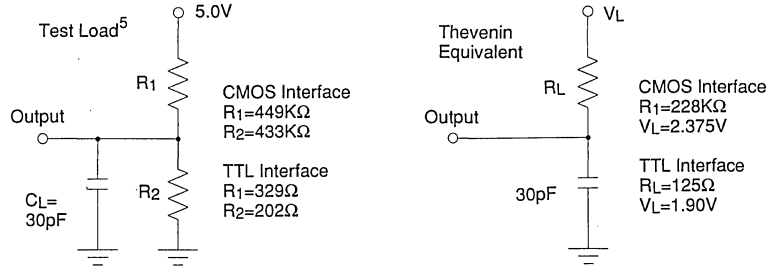
*Alternate source symbols are shown for convenience of those who wish to compare the specifications of the PEEL22CG10 against the specifications of other pin-compatible devices.

A.C. Electrical Characteristics Over the Operating Range[9]

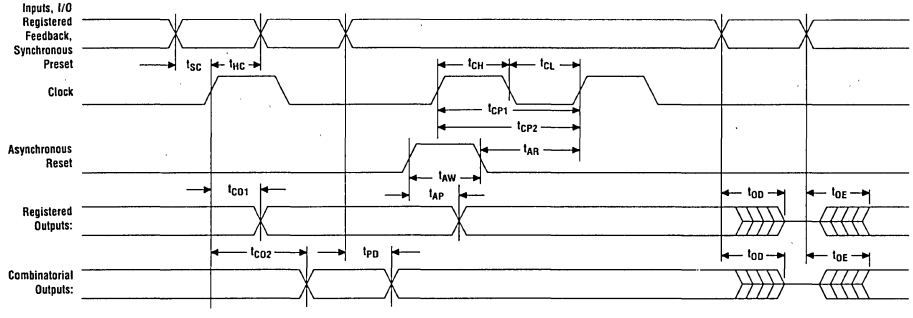
Symbol	Alternate Source Symbol*	Parameter	20CG10-25		20CG10-35		Unit
			Min	Max	Min	Max	
t_{PD}	t_{PD}	Input[6] or feedback to non-registered output		25		35	ns
t_{OE}	t_{EA}	Input[6] to output enable[7]		25		30	ns
t_{OD}	t_{ER}	Input[6] to output disable[7]		25		30	ns
t_{CO1}	t_{CO}	Clock to output		15		20	ns
t_{CO2}		Clock to combinational output delay via internal registered feedback		30		40	ns
t_{SC}	t_S	Input[6] or feedback setup to clock	15		30		ns
t_{HC}	t_H	Input[6] hold after clock	0		0		ns
t_{CL}, t_{CH}	t_W	Clock width—clock low time, clock high time[4]	12		15		ns
t_{CP1}		Clock period (register feedback to registered output via internal path)	25		45		ns
f_{max1}		Maximum clock frequency ($1/t_{CP1}$)	40		22.2		MHz
f_{CP2}	t_P	Clock period (t_{SC} +t_{CO1})	30		50		ns
f_{max2}	f_{max}	Maximum clock frequency ($1/t_{CP2}$)	33.3		20		MHz
t_{AW}	t_{AW}	Asynchronous clear pulse width	25		25		ns
t_{AP}	t_{AP}	Input[6] to Asynchronous Reset		25		35	ns
t_{AR}	t_{AR}	Asynchronous Reset Recovery Time		25		35	ns
t_{RESET}		Power-on reset time for registers in clear state[4]		5		5	μs

*Alternate source symbols are shown for convenience of those who wish to compare the specifications of the PEEL22CG10 against the specifications of other pin-compatible devices.

Test Loads



Switching Waveforms



Notes:

1. Minimum DC input is −0.5V,however inputs may undershoot to −2.0V for periods less than 20nS.
2. Voltage applied to input or output must not exceed V_{CC} +1.0V.
3. V_I and V_O are not specified for program/verify operation.
4. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
5. I/O pins open (no load).
6. "Input" refers to an Input pin signal.
7. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$; V_{REF} =1.90V for TTL interface or 2.375V for CMOS interface.
8. Capacitances are tested on a sample basis.
9. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points; timing reference levels of 1.5V (unless otherwise specified).
10. Test one output at at time for a duration of less than 1 second.

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CMOS Programmable Electrically Erasable Logic Device

Preliminary Data Sheet

PEEL™ 22CV10

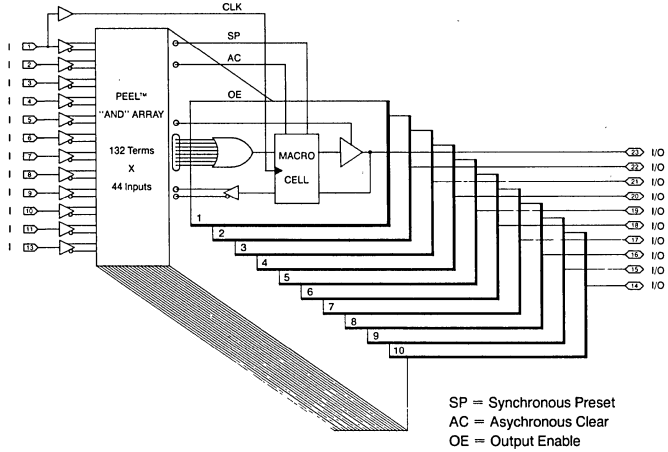
Features

- **Advanced CMOS EEPROM Technology**
- **Low Power Consumption**
  —55mA + 0.5mA/MHz max
- **High Performance**
  —t_{PD} = 25ns max, t_{CO} = 15ns max
- **EE Reprogrammability**
  —Superior programming and functional yield
  —Low cost windowless package
  —Erases and programs in seconds
- **Development/Programmer Support**
  —Third-party software and programmers
  —Gould PEEL Development System with APEEL™ Logic Assembler
- **Architectural Flexibility**
  —132 product term X 44 input AND array
  —Up to 22 inputs and 10 outputs
  —Variable product term distribution (8 to 16 per output) for greater logic flexibility
  —Independently programmable 12-configuration I/O macrocells
  —Synchronous preset, asynchronous clear
  —Independent programmable output enables
- **Application Versatility**
  —Replaces random SSI/MSI logic
  —Emulates 24-pin bipolar PAL devices
  —Superset compatible with the bipolar AmPAL22V10 and CMOS PALC22V10

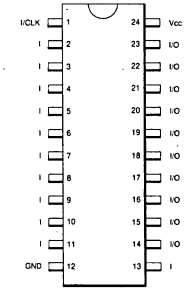
General Description

The Gould PEEL22CV10 is a CMOS Programmable Electrically Erasable Logic Device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to conventional programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PEEL22CV10 rivals speed parameters of comparable

Block Diagram



Pin Configuration



Pin Names

I/CLK = Input Only/Clock
I = Input Only
I/O = Bi-Directional Input/Output
GND = Ground
Vcc = Power Supply (+5V)

PEEL™ 22CV10

Absolute Maximum Ratings Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	−0.5 to +7.0	V
V_I, V_O	Voltage Applied to Any Pin[10]	Relative to GND[1,2]	−0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per Pin (I_{OL}, I_{OH})	±25	mA
T_A	Ambient Temperature, Power Applied		−10 to +85	*C
T_{ST}	Storage Temperature		−65 to +150	*C
T_{LT}	Lead Temperature	Soldering 10 Seconds	+300	*C

Operating Ranges

Symbol	Alternate Source Symbol*	Parameter	Conditions	Min	Max	Unit
V_{CC}	V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
T_A	T_A	Ambient Temperature	Commercial	0	70	*C
T_R		Clock Rise Time	See Note 5		250	ns
T_F		Clock Fall Time	See Note 5		250	ns
T_{RVCC}		V_{CC} Rise Time	See Note 5		10	ms

D.C. Electrical Characteristics Over the operating range.

Symbol	Alternate Source Symbol*	Parameter	Conditions	Min	Max	Unit
V_{OH}	V_{OH}	Output HIGH Voltage—TTL	V_{CC} = Min, I_{OH} = −4.0mA	2.4		V
V_{OL}	V_{OL}	Output LOW Voltage—TTL	V_{CC} = Min, I_{OL} = 8mA		0.5	V
V_{IH}	V_{IH}				V_{CC} + 0.3	V
V_{IL}	V_{IL}				0.8	V
I_{IX}	I_{IL}, I_{IH}, I_{IX}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	
I_{OZ}	I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}		±10	
I_{SC}	I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_O = 0.5V	−30	−90	
I_{CCST}	I_{CC}	V_{CC} Current, Standby, TTL	V_{IN} = V_{IL} or V_{IH}[9]		55	
I_{CCAT}	I_{CC}	V_{CC} Current, Active, TTL	V_{IN} = V_{IL} or V_{IH}[9] All outputs open.		I_{CCST} + 0.5mA/MHz	mA
C_{IN}[14]	C_{IN}	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT}[14]	C_{OUT}	Output Capacitance			12	pF

*Alternate source symbols are shown for the convenience of those who wish to compare the specifications of the PEEL22CV10 against the specifications of other, similar devices.

A.C. Electrical Characteristics Over the operating range[3].

Symbol	Alternate Source Symbol*	Parameter	22CV10Z-25		22CV10Z-30		22CV10Z-35		Unit
			Min	Max	Min	Max	Min	Max	
t_{PD}	t_{PD}	Input[4] or feedback to non-registered output		25		30		35	ns
t_{OE}	t_{EA}	Input[4] to output enable[6]		25		25		30	ns
t_{OD}	t_{ER}	Input[4] to output disable[6]		25		25		30	ns
t_{CO1}	t_{CO}	Clock to output		15		18		20	ns
t_{CO2}		Clock to combinatorial output delay via internal registered feedback		30		35		40	ns
t_{SC}	t_S	Input[4] or feedback setup to clock	15		25		30		ns
t_{HC}	t_H	Input[4] hold after clock	0		0		0		ns
t_{CL}, t_{CH}	t_W	Clock width—clock low time, clock high time[5]	12		15		15		ns
t_{CP1}		Clock period (register feedback to register output via internal path)	25		30		45		ns
f_{MAX1}		Maximum clock frequency ($1/t_{CP1}$)	40		43		22.2		MHz
t_{CP2}	t_P	Clock period ($t_{SC} + t_{CO1}$)	30		?		50		ns
f_{MAX2}	f_{MAX}	Maximum clock frequency ($1/t_{CP2}$)	33.3		23.2		20		MHz
t_{AW}	t_{AW}	Asynchronous clear pulse width	25		25		25		ns
t_{AP}	t_{AP}	Input[4] to asynchronous clear		25		30		35	ns
t_{AR}	t_{AR}	Asynchronous clear recovery time		25		30		35	ns
t_{RESET}		Power-on reset time for registers in clear state		5		5		5	µs

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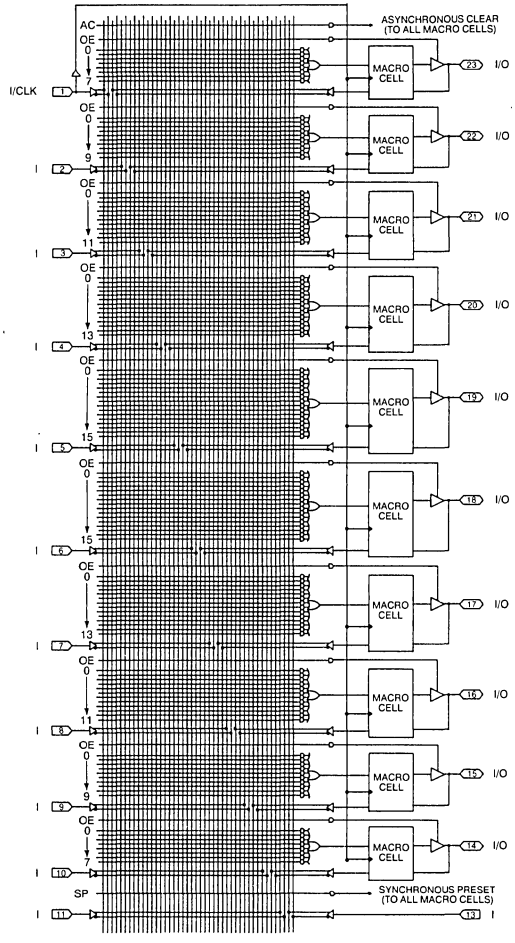
bipolar PLDs while providing a dramatic improvement in active power consumption. The EE reprogrammability of the PEEL22CV10 reduces development and field retrofit costs and enhances testability to ensure 100% field programmability and function. PEEL technology allows for low cost "windowless" packaging in a 24-pin, 300-mil DIP.

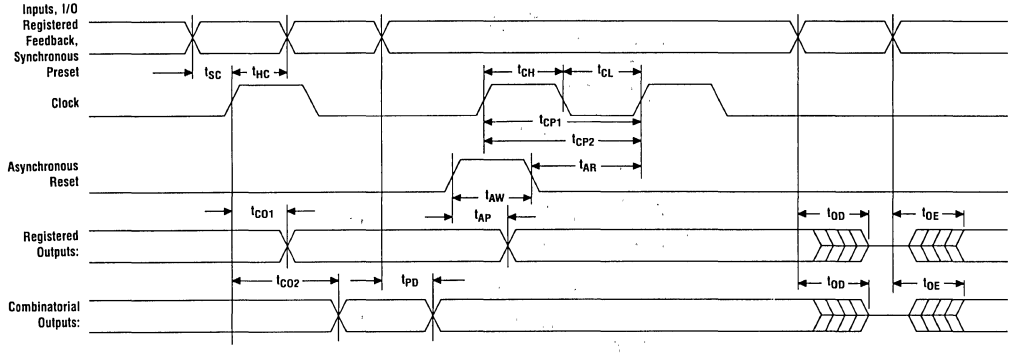
The PEEL22CV10's flexible architecture offers complete function and JEDEC-file compatibility with the bipolar AmPAL22V10 and the CMOS PALC22V10 plus eight additional macrocell configurations (a total of twelve) that further expand its I/O and feedback design capabilities. Applications for the PEEL22CV10 include: replacement of random SSI/MSI logic circuitry; emulation of 24-pin bipolar PAL devices; and user customized sequential and combinatorial functions such as counters, shift registers, state machines, address decoders, multiplexers, etc. Development and programming support for the PEEL22CV10 is provided by Gould and third-party manufacturers.

PEEL22CV10 Logic Array Diagram



PLDs

Switching Waveforms



Preliminary Designation

The "Preliminary" designation on a Gould data sheet indicates that the product is not characterized. The specifications are subject to change, are based on design goals or preliminary part evaluation, and are not guaranteed. Gould or an authorized sales representative should be consulted for current information before using this product.

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CMOS Programmable Electrically Erasable Logic Device

Preliminary Data Sheet

PEEL™ 22CV10Z

Features

- **Advanced CMOS EEPROM Technology**
- **Low Power Consumption**
  - —Zero Power Mode—200μA max standby
  - —55mA + 0.5mA/MHz max
- **High Performance**
  - —t_{PD} = 25ns max, t_{CO} = 15ns max
- **EE Reprogrammability**
  - —Superior programming and functional yield
  - —Low cost windowless package
  - —Erases and programs in seconds
- **Development/Programmer Support**
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  - —Gould PEEL Development System with APEEL™ Logic Assembler
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  - —132 product term X 44 input AND array
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  - —Synchronous preset, asynchronous clear
  - —Independent programmable output enables
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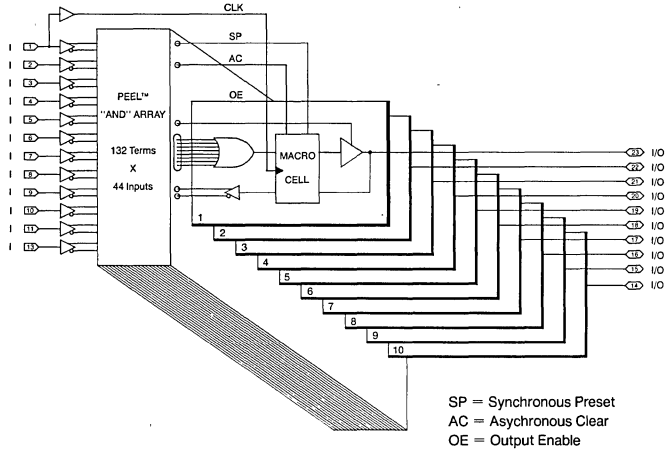
  - —Replaces random SSI/MSI logic
  - —Emulates 24-pin bipolar PAL devices
  - —Superset compatible with the bipolar AmPAL22V10 and CMOS PALC22V10

General Description

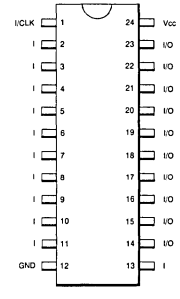
The Gould PEEL22CV10Z is a CMOS Programmable Electrically Erasable Logic Device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to conventional programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PEEL22CV10Z rivals speed parameters of comparable

PLDs

Block Diagram



Pin Configuration



Pin Names

I/CLK = Input Only/Clock
I = Input Only
I/O = Bi-Directional Input/Output
GND = Ground
Vcc = Power Supply (+5V)

Absolute Maximum Ratings Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	−0.5 to +7.0	V
V_I, V_O	Voltage Applied to Any Pin[10]	Relative to GND[1,2]	−0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per Pin (I_{OL}, I_{OH})	±25	mA
T_A	Ambient Temperature, Power Applied		−10 to +85	*C
T_{ST}	Storage Temperature		−65 to +150	*C
T_{LT}	Lead Temperature	Soldering 10 Seconds	+300	*C

Operating Ranges

Symbol	Alternate Source Symbol*	Parameter	Conditions	Min	Max	Unit
V_{CC}	V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
T_A	T_A	Ambient Temperature	Commercial	0	70	*C
T_R		Clock Rise Time	See Note 5		250	ns
T_F		Clock Fall Time	See Note 5		250	ns
T_{RVCC}		V_{CC} Rise Time	See Note 5		10	ms

D.C. Electrical Characteristics Over the operating range.

Symbol	Alternate Source Symbol*	Parameter	Conditions	Min	Max	Unit
V_{OH}	V_{OH}	Output HIGH Voltage—TTL	V_{CC} = Min, I_{OH} = −4.0mA	2.4		V
V_{OL}	V_{OL}	Output LOW Voltage—TTL	V_{CC} = Min, I_{OL} = 8mA		0.5	V
V_{IH}	V_{IH}				V_{CC} + 0.3	V
V_{IL}	V_{IL}				0.8	V
I_{IX}	I_{IL}, I_{IH}, I_{IX}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}		±10	
I_{OZ}	I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}		±10	
I_{SC}	I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_O = 0.5V	−30	−90	
I_{CCST}	I_{CC}	V_{CC} Current, Standby, TTL	V_{IN} = V_{IL} or V_{IH}[9]		55	
I_{CCAT}	I_{CC}	V_{CC} Current, Active, TTL	V_{IN} = V_{IL} or V_{IH}.[9] All outputs open.		I_{CCST} + 0.5mA/MHz	mA
I_{CCSB}		V_{CC} Current, "0 Power Mode"	V_{IN}=V_{IL} or V_{IH}[9]		200	μA
C_{IN}[14]	C_{IN}	Input Capacitance	T_A = 25°C, V_{CC} = 5.0V @ f = 1MHz		6	pF
C_{OUT}[14]	C_{OUT}	Output Capacitance			12	pF

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A.C. Electrical Characteristics Over the operating range[3].

Symbol	Alternate Source Symbol*	Parameter	22CV10Z-25		22CV10Z-30		22CV10Z-35		Unit
			Min	Max	Min	Max	Min	Max	
t_{PD}	t_{PD}	Input[4] or feedback to non-registered output		25		30		35	ns
t_{OE}	t_{EA}	Input[4] to output enable[6]		25		25		30	ns
t_{OD}	t_{ER}	Input[4] to output disable[6]		25		25		30	ns
t_{CO1}	t_{CO}	Clock to output		15		18		20	ns
t_{CO2}		Clock to combinatorial output delay via internal registered feedback		30		35		40	ns
t_{SC}	t_S	Input[4] or feedback setup to clock	15		25		30		ns
t_{HC}	t_H	Input[4] hold after clock	0		0		0		ns
t_{CL}, t_{CH}	t_W	Clock width—clock low time, clock high time[5]	12		15		15		ns
t_{CP1}		Clock period (register feedback to register output via internal path)	25		30		45		ns
f_{MAX1}		Maximum clock frequency ($1/t_{CP1}$)	40		43		22.2		MHz
t_{CP2}	t_P	Clock period ($t_{SC} + t_{CO1}$)	30		?		50		ns
f_{MAX2}	f_{MAX}	Maximum clock frequency ($1/t_{CP2}$)	33.3		23.2		20		MHz
t_{AW}	t_{AW}	Asynchronous clear pulse width	25		25		25		ns
t_{AP}	t_{AP}	Input[4] to asynchronous clear		25		30		35	ns
t_{AR}	t_{AR}	Asynchronous clear recovery time		25		30		35	ns
t_{RESET}		Power-on reset time for registers in clear state		5		5		5	µs

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bipolar PLDs while providing a dramatic improvement in active power consumption, along with a "zero-power" standby mode. The EE reprogrammability of the PEEL22CV10 reduces development and field retrofit costs and enhances testability to ensure 100% field programmability and function. PEEL technology allows for low cost "windowless" packaging in a 24-pin, 300-mil DIP.

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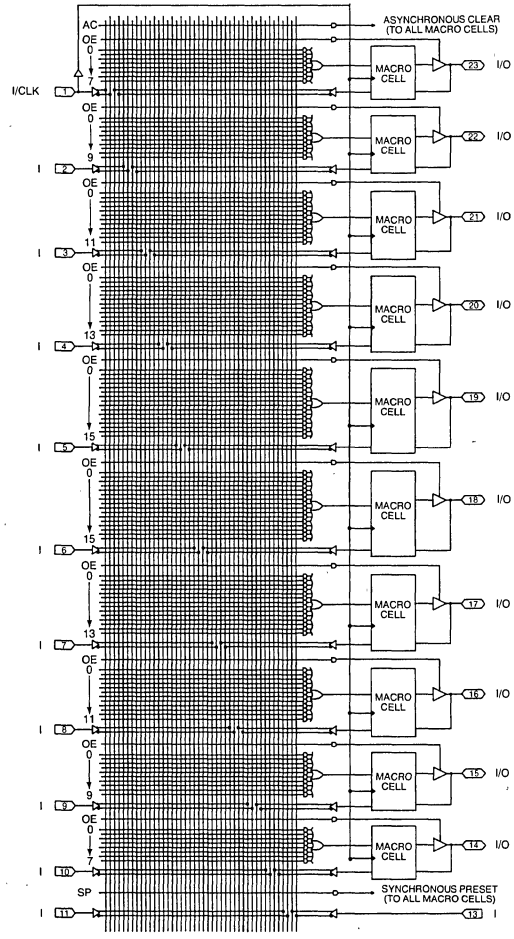
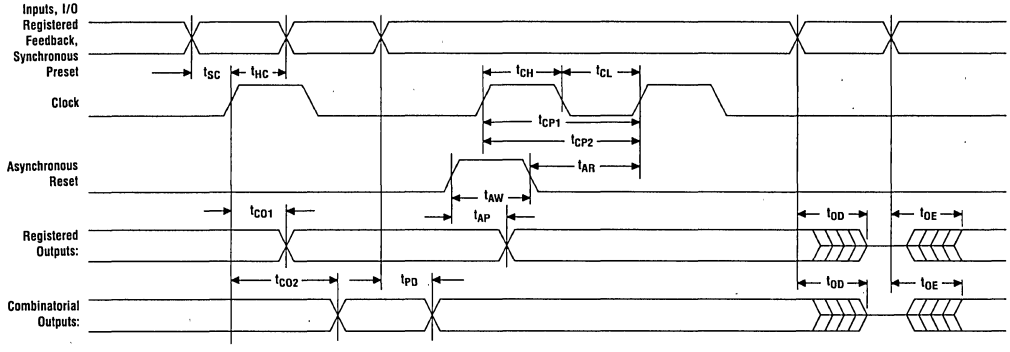
PEEL™ 22CV10Z

PEEL22CV10 Logic Array Diagram



Switching Waveforms



Preliminary Designation

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GOULD

AMI Semiconductors

CMOS Programmable Electrically Erasable Logic Device

Preliminary Data Sheet

PEEL™153

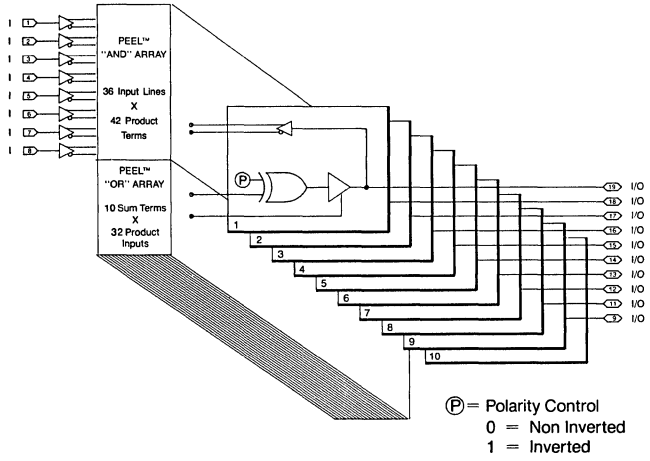
Features

- **Advanced CMOS EEPROM Technology**
- **Low Power Consumption**
  —65mA + 0.5mA/MHz max
- **High Performance**
  —t_{PD} = 30ns max, t_{OE} = 30ns max
- **Architectural Flexibility**
  —8 inputs and 10 I/Os
  —Programmable AND/OR arrays with 42 product terms/20 sum terms
- **EE Reprogrammability**
  —Superior programming and functional yield
  —Low cost windowless package
  —Erases and programs in seconds
- **Replacement for PLS153**
  —Ten additional product terms
  —Output-enable terms in OR array
  —Signature word
  —Foolproof design security
- **Application Versatility**
  —Replace random SSI/MSI logic
  —Create customized comparators, multiplexers, encoders, converters, etc.
- **Development Support**
  —Third-party software and programmers
  —Gould PEEL Development System with APEEL™ Logic Assembler

General Description

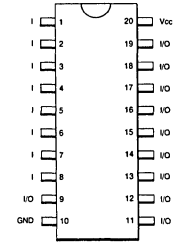
The Gould PEEL153 is a CMOS Programmable Electrically Erasable Logic device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to conventional programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PEEL153 rivals speed parameters of comparable bipolar PLDs while providing a dramatic improvement in active power consumption. The EE-reprogrammability of the PEEL153 reduces development and field retrofit costs and enhances testability to ensure 100% field programmability

Block Diagram



Ⓟ = Polarity Control
0 = Non Inverted
1 = Inverted

Pin Diagram



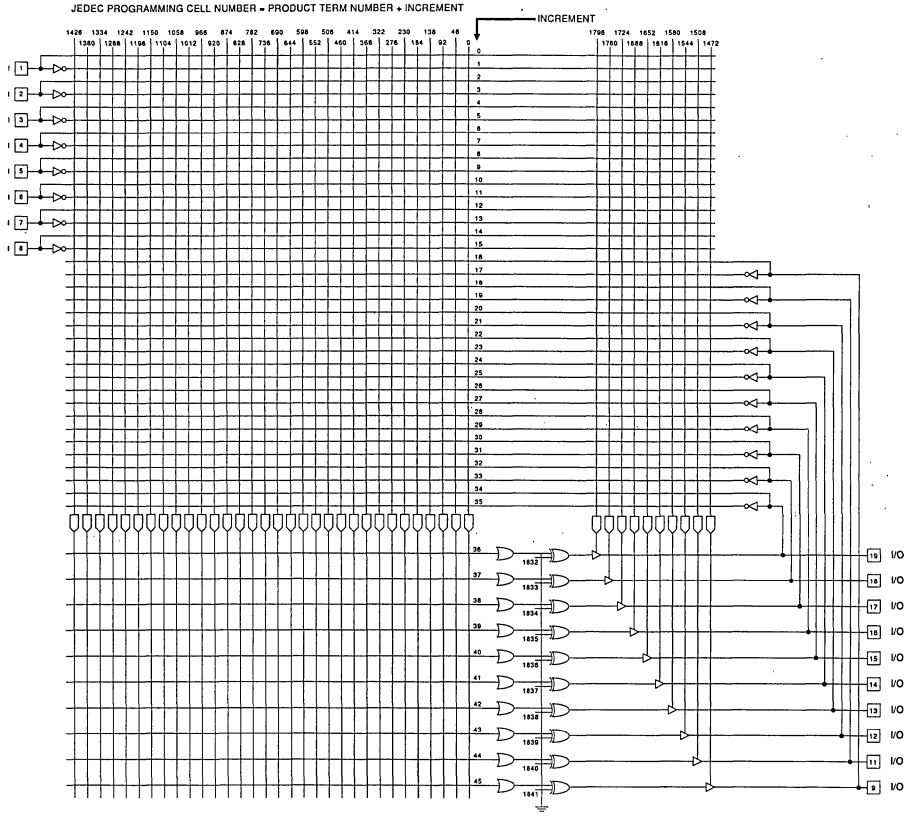
Pin Names

I = Input Only
I/O = Bi-Directional Input/Output
GND = Ground
Vcc = Power Supply (+5V)

and function. PEEL technology allows for low cost "windowless" packaging in a ceramic or plastic 20-pin, 300-mil DIP.

The PEEL153 provides both a programmable AND array and a programmable OR array. It offers superset compatibility with the bipolar PLS153 with several architectural enhancements, including: output enable terms in the OR array, 20 additional product terms, and signature word. Applications for the PEEL153 cover a wide range of combinatorial functions, such as: replacement of random SSI/MSI logic circuitry, priority encoders, comparators, parity generators, code converters, address decoders, and multiplexers. The PEEL153 is supported by popular development tools and programmers from third-party manufacturers and by Gould's PEEL Development System and APEEL™ Logic Assembler.

PEEL153 Logic Array Diagram



Absolute Maximum Ratings Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	−0.6 to +7.0	V
V_{IO}	Voltage Applied to Any Pin[8]	Relative to GND[1]	−0.6 to V_{CC} + 0.6	V
T_A	Ambient Temp, Power Applied		−10 to +85	*C
T_{ST}	Storage Temperature		−65 to +150	*C
T_{LT}	Lead Temperature	Soldering 10 Seconds	+300	*C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
T_A	Ambient Temperature	Commercial	0	70	*C

D.C. Electrical Characteristics Over the operating range.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		−0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = −3.2mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8mA[4]		0.5	V
I_L	Input Leakage Current	V_{CC} = Max, GND ≤ V_I ≤ V_{CC}		10	µA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max, V_O = GND	−30	−90	mA
I_{OZ}	Output Leakage Current	I/O = High Impedence V_{CC} = Max, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{CCST}	Power Supply Current, Standby, TTL Interface	V_{IN} = V_{IL} or V_{IH}[3]		65	mA
I_{CCAT}	Power Supply Current, Active, TTL Interface	V_{IN} = V_{IL} or V_{IH}. All inputs, feedback, and I/Os switching[3].		I_{CCST}+ 0.5mA/MHz	mA

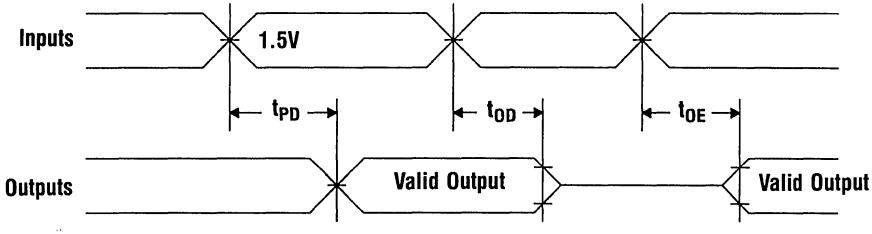
Capacitance These measurements are periodically sample tested.

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C V_{CC} = 5.0V, f = 1kHz		6	pF
C_{OUT}	Output Capacitance			12	pF

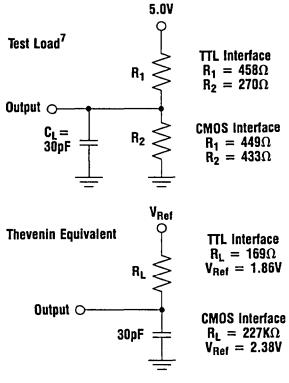
A.C. Electrical Characteristics Over the operating range[5].

Symbol	Parameter	PEEL153C-30		PEEL153-35		PEEL153C-40		Unit
		Min	Max	Min	Max	Min	Max	
t_{PD}	Propagation Delay, Input to Output		30		35		40	ns
t_{OE}	Input to Output Enable[6]		30		35		40	ns
t_{OD}	Input to Output Disable[6,7]		30		35		40	ns

Switching Waveforms



Test Loads



Notes:

1. Minimum DC input is −0.5V, however, inputs may undershoot to −2.0V for periods less than 30ns.
2. Test one output at a time. Duration of short circuit should not exceed 1 second.
3. All I/O pins open (no load).
4. Assumes worst-case conditions—all outputs loaded. V_{OL} = 0.5V @ I_{OL} = 15mA with one output loaded.
5. Test conditions assume: signal transitions of 5ns or less from the 10% and 90% points; timing reference levels of 1.5V (unless otherwise specified); and test loads shown.
6. t_{OD} and t_{OE} are measured at V_{OH} −0.1V and V_{OL} +0.1V.
7. C_L includes scope and jig capacitance. t_{OD} is measured with C_L = 5pF.
8. V_{IO} specified is not for program/verify operation. Contact Gould for information regarding PEEL153 program/verify specifications.

Preliminary Designation

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Specifications, Patents, and Life Support Policy

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GOULD
AMI Semiconductors

CMOS Programmable Electrically Erasable Logic Device

Preliminary Data Sheet

PEEL™ 173

Features

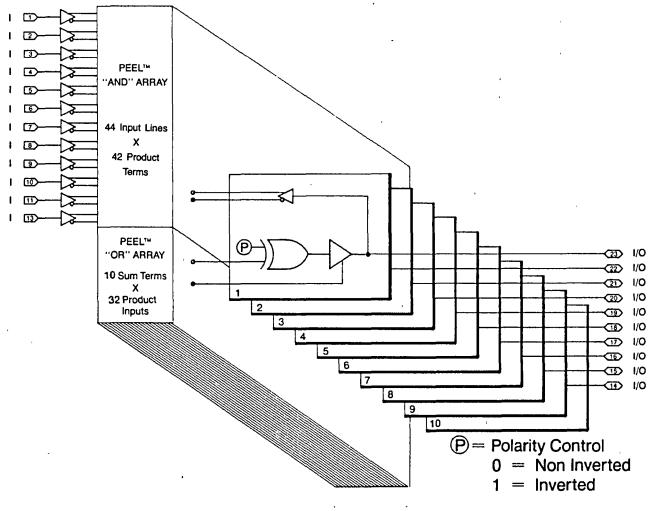
- **Advanced CMOS EEPROM Technology**
- **Low Power Consumption**
  —65mA + 0.5mA/MHz max
- **High Performance**
  —t_{PD} = 30ns max, t_{OE} = 30ns max
- **Architectural Flexibility**
  —12 inputs and 10 I/Os
  —Programmable AND/OR arrays with 42 product terms/20 sum terms
- **EE Reprogrammability**
  —Superior programming and functional yield
  —Low cost windowless package
  —Erases and programs in seconds
- **Replacement for PLS173**
  —Ten additional product terms
  —Output-enable terms in OR array
  —Signature word
  —Foolproof design security
- **Application Versatility**
  —Replace random SSI/MSI logic
  —Create customized comparators, multiplexers, encoders, converters, etc.
- **Development Support**
  —Third-party software and programmers
  —Gould PEEL Development System with APEEL™ Logic Assembler

General Description

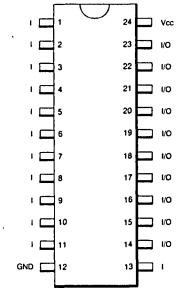
The Gould PEEL173 is a CMOS Programmable Electrically Erasable Logic device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to conventional programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PEEL173 rivals speed parameters of comparable bipolar PLDs while providing a dramatic improvement in active power consumption. The EE-reprogrammability of the PEEL173 reduces development and field retrofit costs and enhances testability to ensure 100% field programmability

PLDs

Block Diagram



Pin Configuration



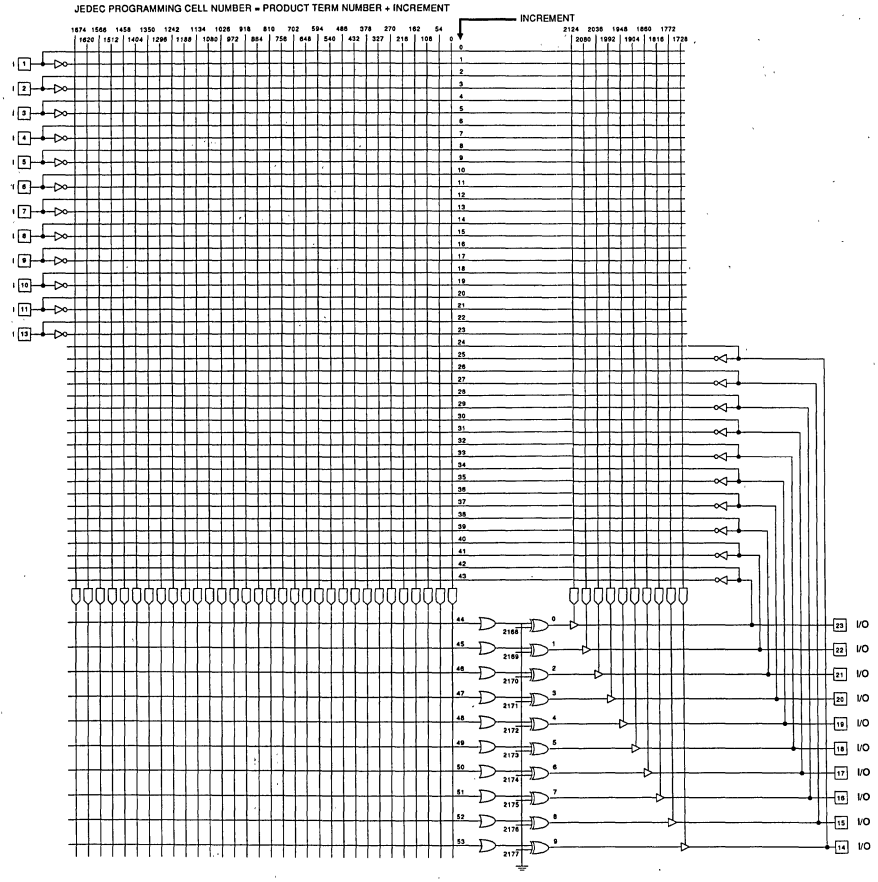
Pin Names

I = Input Only
I/O = Bi-Directional Input/Output
GND = Ground
Vcc = Power Supply (+5V)

and function. PEEL technology allows for low cost "windowless" packaging in a ceramic or plastic 24-pin, 300-mil DIP.

The PEEL173 provides both a programmable AND array and a programmable OR array. It offers superset compatibility with the bipolar PLS173 with several architectural enhancements, including: output enable terms in the OR array, 10 additional product terms, and signature word. Applications for the PEEL173 cover a wide range of combinatorial functions, such as: replacement of random SSI/MSI logic circuitry, priority encoders, comparators, parity generators, code converters, address decoders, and multiplexers. The PEEL173 is supported by popular development tools and programmers from third-party manufacturers and by Gould's PEEL Development System and APEEL™ Logic Assembler.

PEEL173C Logic Array Diagram



Absolute Maximum Ratings Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	−0.6 to +7.0	V
V_{IO}	Voltage Applied to Any Pin[8]	Relative to GND[1]	−0.6 to V_{CC} + 0.6	V
T_A	Ambient Temp, Power Applied		−10 to +85	*C
T_{ST}	Storage Temperature		−65 to +150	*C
T_{LT}	Lead Temperature	Soldering 10 Seconds	+300	*C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
T_A	Ambient Temperature	Commercial	0	70	*C

D.C. Electrical Characteristics Over the operating range.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		−0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = −3.2mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8mA[4]		0.5	V
I_L	Input Leakage Current	V_{CC} = Max, GND ≤ V_I ≤ V_{CC}		10	µA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max, V_O = GND	−30	−90	mA
I_{OZ}	Output Leakage Current	I/O = High Impedence V_{CC} = Max, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{CCST}	Power Supply Current, Standby, TTL Interface	V_{IN} = V_{IL} or V_{IH}[3]		65	mA
I_{CCAT}	Power Supply Current, Active, TTL Interface	V_{IN} = V_{IL} or V_{IH}. All inputs, feedback, and I/Os switching[3].		I_{CCST}+ 0.5mA/MHz	mA

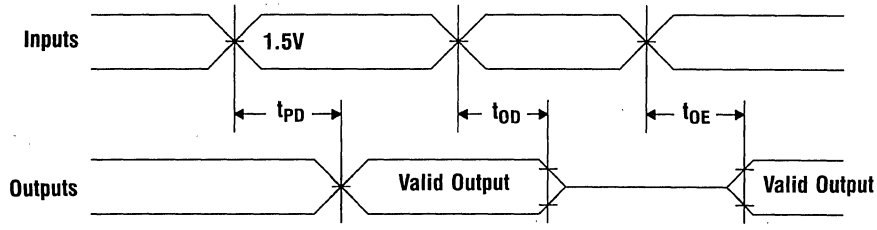
Capacitance These measurements are periodically sample tested.

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C V_{CC} = 5.0V, f = 1kHz		6	pF
C_{OUT}	Output Capacitance			12	pF

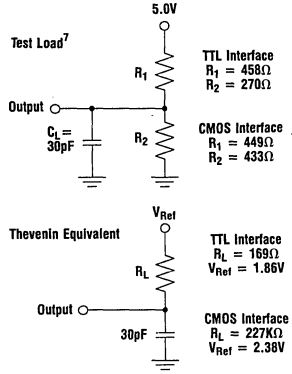
A.C. Electrical Characteristics Over the operating range[5].

Symbol	Parameter	PEEL173C-30		PEEL173-35		PEEL173C-40		Unit
		Min	Max	Min	Max	Min	Max	
t_{PD}	Propagation Delay, Input to Output		30		35		40	ns
t_{OE}	Input to Output Enable[6]		30		35		40	ns
t_{OD}	Input to Output Disable[6,7]		30		35		40	ns

Switching Waveforms



Test Loads



Notes:

1. Minimum DC input is −0.5V, however, inputs may undershoot to −2.0V for periods less than 30ns.
2. Test one output at a time. Duration of short circuit should not exceed 1 second.
3. All I/O pins open (no load).
4. Assumes worst-case conditions—all outputs loaded. V_{OL} = 0.5V @ I_{OL} = 15mA with one output loaded.
5. Test conditions assume: signal transitions of 5ns or less from the 10% and 90% points; timing reference levels of 1.5V (unless otherwise specified); and test loads shown.
6. t_{OD} and t_{OE} are measured at V_{OH} −0.1V and V_{OL} +0.1V.
7. C_L includes scope and jig capacitance. t_{OD} is measured with C_L = 5pF.
8. V_{IO} specified is not for program/verify operation. Contact Gould for information regarding PEEL173 program/verify specifications.

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GOULD

AMI Semiconductors

CMOS Programmable Electrically Erasable Logic Device

Preliminary Data Sheet

PEEL™ 253

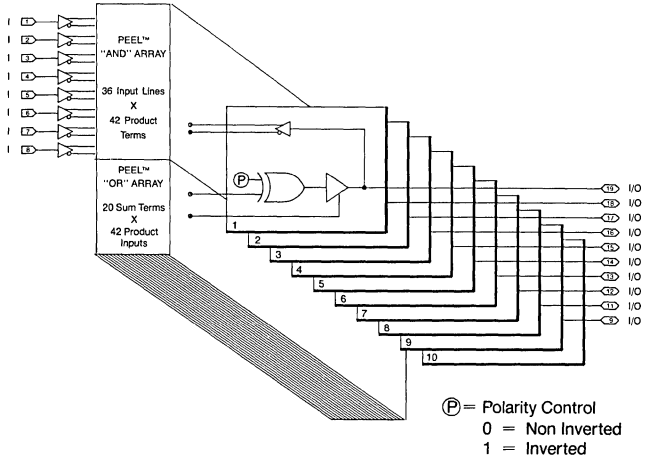
Features

- **Advanced CMOS E^2PROM Technology**
- **Low Power Consumption**
  —TTL: 65mA+0.5mA/MHz Max
- **High Performance**
  —T_{PD} 30nS Max, T_{OE} 30nS Max
- **Reprogrammability**
  —100% factory tested
  —Cost effective window-less package
  —Erases and programs in seconds
  —Adds convenience, reduces field retrofit and development cost
- **Development/Programmer Support**
  —Popular third party development tools and stand alone programmers
  —PC based evaluation and development tools from Gould
- **Plug-in Compatibility**
  —Signetics PLS 153, ICT 253
  —PC-based software translates existing JEDEC files to PEEL253 format
- **Architectural and Design Enhancements**
  —8 dedicated inputs, 10 I/O pins
  —Dual programmable logic arrays: AND (36 inputs X 42 product terms) OR (20 sum terms X 42 products)
  —Sharing of all 42 product terms
  —I/O polarity controls
  —Output enable terms in OR array
  —Security from unauthorized copying
  —Signature word for user specified ID
- **Application Versatility**
  —Replaces random SSI/MSI logic
  —Ideal for customized combinatorial functions: comparators, multiplexers, encoders, converters, etc.

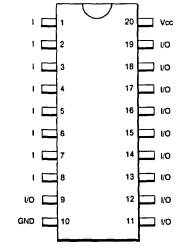
General Description

The Gould PEEL™ 253 is a CMOS Programmable Electrically Erasable Logic device that provides a high performance, low power, reprogrammable, and architecturally enhanced alternative to conventional programma-

Block Diagram



Pin Diagram



Pin Names

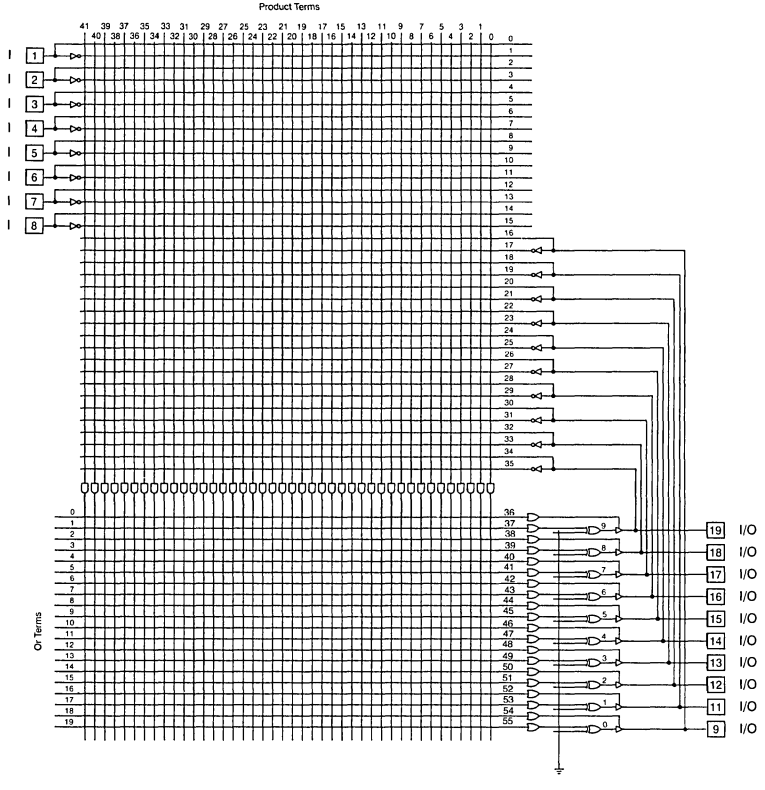
I = Input Only
I/O = Bi-Directional Input/Output
GND = Ground
Vcc = Power Supply (+5V)

PEEL™ 253

ble logic devices (PLDs). Designed in advanced CMOS E^2PROM technology, the PEEL 253 rivals speed parameters of comparable bipolar PLDs with a substantial improvement in power consumption. The E^2 reprogrammability of the PEEL 253 not only reduces development and field retrofit costs but enhances testability ensuring 100% field programmability and function. Additionally, the PEEL 253 technology allows for cost effective "window-less" packaging in a 20-pin 300-mil DIP.

Providing both programmable "AND" and programmable "OR" arrays, the PEEL 253 offers functional compatibility to the Signetics PLS153 (previously numbered 82S153) plus several architectural enhancements including: output enable terms in the "OR" array, 10 additional general purpose product terms, security from unauthorized copying of designs, and signature word for user specified device identification. Applications of the PEEL 253 include replacement of random SSI/MSI logic circuitry and a wide range of combinatorial logic functions, such as priority encoders, comparators, parity generators, code converters, address decoders, and multiplexers. Development and programming for the PEEL 253 is supported by popular development tools and programmers from third-party manufacturers, plus PC-based PEEL Development System from Gould.

PEEL253 Logic Array Diagram



Absolute Maximum Ratings Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	−0.6 to +7.0	V
V_{IO}	Voltage Applied to Any Pin[8]	Relative to GND[1]	−0.6 to V_{CC} + 0.6	V
T_A	Ambient Temp, Power Applied		−10 to +85	°C
T_{ST}	Storage Temperature		−65 to +150	°C
T_{LT}	Lead Temperature	Soldering 10 Seconds	+300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
T_A	Ambient Temperature	Commercial	0	70	°C

D.C. Electrical Characteristics Over the operating range.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		−0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = −3.2mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8mA[4]		0.5	V
I_L	Input Leakage Current	V_{CC} = Max, GND ≤ V_I ≤ V_{CC}		10	µA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max, V_O = GND	−30	−90	mA
I_{OZ}	Output Leakage Current	I/O = High Impedence V_{CC} = Max, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{CCST}	Power Supply Current, Standby, TTL Interface	V_{IN} = V_{IL} or V_{IH}[3]		65	mA
I_{CCAT}	Power Supply Current, Active, TTL Interface	V_{IN} = V_{IL} or V_{IH}. All inputs, feedback, and I/Os switching[3].		I_{CCST}+ 0.5mA/MHz	mA

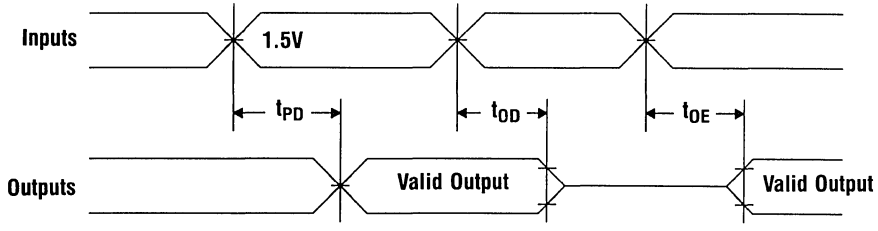
Capacitance These measurements are periodically sample tested.

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C V_{CC} = 5.0V, f = 1kHz		6	pF
C_{OUT}	Output Capacitance			12	pF

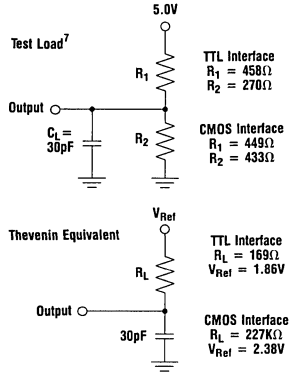
A.C. Electrical Characteristics Over the operating range[5]

Symbol	Parameter	253–30		253–35		253–40		Unit
		Min	Max	Min	Max	Min	Max	
t_{PD}	Propagation Delay, Input to Output		30		35		40	ns
t_{OE}	Input to Output Enable[6]		30		35		40	ns
t_{OD}	Input to Output Disable[6,7]		30		35		40	ns

Switching Waveforms



Test Loads



Notes:

1. Minimum DC input is −0.5V, however, inputs may undershoot to −2.0V for periods less than 30ns.
2. Test one output at a time. Duration of short circuit should not exceed 1 second.
3. All I/O pins open (no load).
4. Assumes worst-case conditions—all outputs loaded. V_{OL} = 0.5V @ I_{OL} = 15mA with one output loaded.
5. Test conditions assume: signal transitions of 5ns or less from the 10% and 90% points; timing reference levels of 1.5V (unless otherwise specified); and test loads shown.
6. t_{OD} and t_{OE} are measured at V_{OH} −0.1V and V_{OL} +0.1V.
7. C_L includes scope and jig capacitance. t_{OD} is measured with C_L = 5pF.
8. V_{IO} specified is not for program/verify operation. Contact Gould for information regarding PEEL253 program/verify specifications.

Preliminary Designation

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GOULD

AMI Semiconductors

CMOS Programmable Electrically Erasable Logic Device

Preliminary Data Sheet

PEEL™ 273

Features

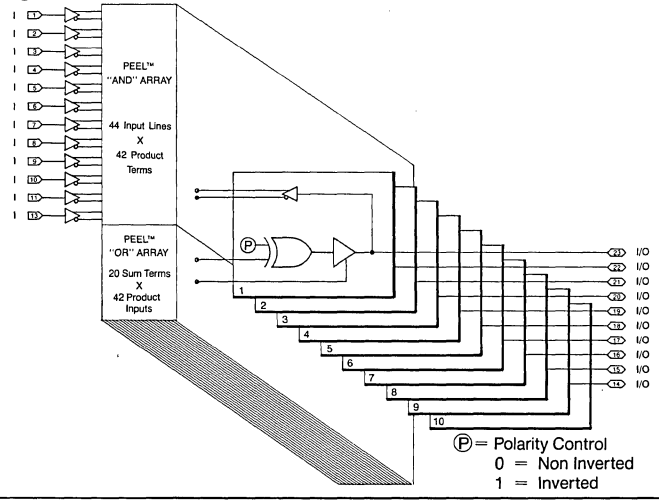
- **Advanced CMOS E^2PROM Technology**
- **Low Power Consumption**
  —TTL: 65mA+0.5mA/MHz Max
- **High Performance**
  —T_{PD} 30nS Max, T_{OE} 30nS Max
- **Reprogrammability**
  —100% factory tested
  —Cost effective window-less package
  —Erases and programs in seconds
  —Adds convenience, reduces field retrofit and development cost
- **Development/Programmer Support**
  —Popular third party development tools and stand alone programmers
  —PC based evaluation and development tools from Gould
- **Plug-in Compatibility**
  —Signetics PLS 173, ICT 273
  —PC-based software translates existing JEDEC files to 273 format
- **Architectural and Design Enhancements**
  —12 dedicated inputs, 10 I/O pins
  —Dual programmable logic arrays: AND (44 inputs X 44 product terms) OR (20 sum terms X 42 products)
  —Sharing of all 42 product terms
  —I/O polarity controls
  —Output enable terms in OR array
  —Security from unauthorized copying
  —Signature word for user specified ID
- **Application Versatility**
  —Replaces random SSI/MSI logic
  —Ideal for customized combinatorial functions: comparators, multiplexers, encoders, converters, etc.

General Description

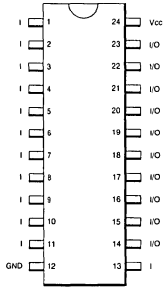
The Gould PEEL™ 273 is a CMOS Programmable Electrically Erasable Logic device that provides a high performance, low power, reprogrammable, and architecturally enhanced alternative to conventional programma-

PLDs

Block Diagram



Pin Diagram



Pin Names

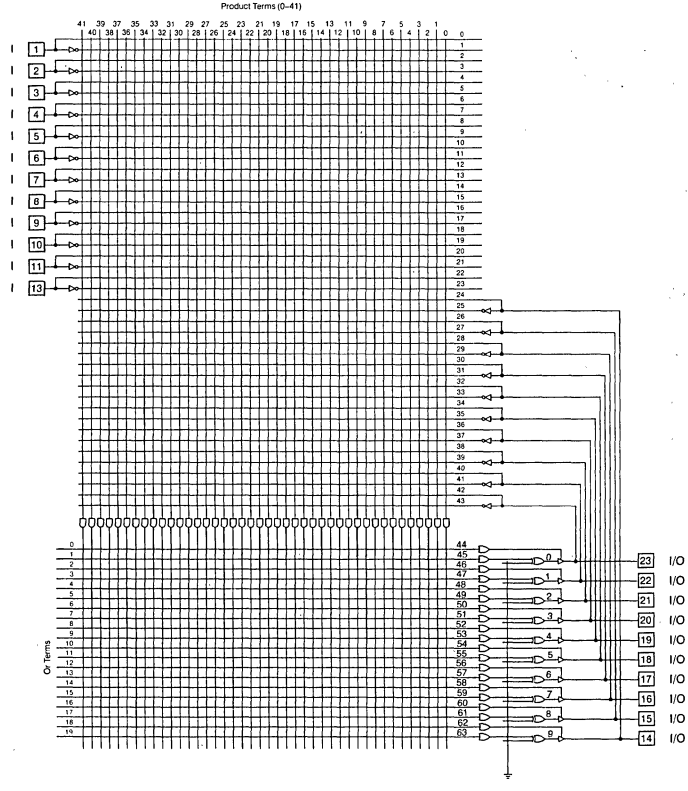
I = Input Only
I/O = Bi-Directional Input/Output
GND = Ground
Vcc = Power Supply (+5V)

PEEL™ 273

ble logic devices (PLDs). Designed in advanced CMOS E^2PROM technology, the PEEL 273 rivals speed parameters of comparable bipolar PLDs with a substantial improvement in power consumption. The E^2 reprogrammability of the PEEL 273 not only reduces development and field retrofit costs but enhances testability ensuring 100% field programmability and function. Additionally, the PEEL 273 technology allows for cost effective "window-less" packaging in a 24-pin 300-mil DIP.

Providing both programmable "AND" and programmable "OR" arrays, the PEEL 273 offers functional compatibility to the Signetics PLS173 (previously numbered 82S173) plus several architectural enhancements including: output enable terms in the "OR" array, 10 additional general purpose product terms, security from unauthorized copying of designs, and signature word for user specified device identification. Applications of the PEEL 273 include replacement of random SSI/MSI logic circuitry, and a wide range of combinatorial logic functions, such as priority encoders, comparators, parity generators, code converters, address decoders, and multiplexers. Development and programming for the PEEL 273 is supported by popular development tools and programmers from third-party manufacturers, plus PC-based PEEL Development System from Gould.

PEEL273 Logic Array Diagram



Absolute Maximum Ratings Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	−0.6 to +7.0	V
V_{IO}	Voltage Applied to Any Pin[8]	Relative to GND[1]	−0.6 to V_{CC} + 0.6	V
T_A	Ambient Temp, Power Applied		−10 to +85	°C
T_{ST}	Storage Temperature		−65 to +150	°C
T_{LT}	Lead Temperature	Soldering 10 Seconds	+300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
T_A	Ambient Temperature	Commercial	0	70	°C

D.C. Electrical Characteristics Over the operating range.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		−0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = −3.2mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8mA[4]		0.5	V
I_L	Input Leakage Current	V_{CC} = Max, GND ≤ V_I ≤ V_{CC}		10	µA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max, V_O = GND	−30	−90	mA
I_{OZ}	Output Leakage Current	I/O = High Impedence V_{CC} = Max, GND ≤ V_O ≤ V_{CC}		±10	µA
I_{CCST}	Power Supply Current, Standby, TTL Interface	V_{IN} = V_{IL} or V_{IH}[3]		65	mA
I_{CCAT}	Power Supply Current, Active, TTL Interface	V_{IN} = V_{IL} or V_{IH}. All inputs, feedback, and I/Os switching[3].		I_{CCST}+ 0.5mA/MHz	mA

PLDs

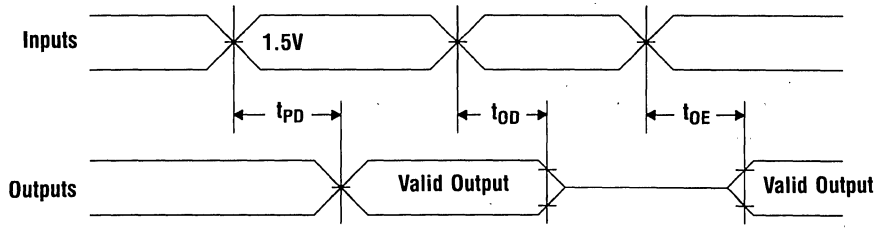
Capacitance These measurements are periodically sample tested.

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C V_{CC} = 5.0V, f = 1kHz		6	pF
C_{OUT}	Output Capacitance			12	pF

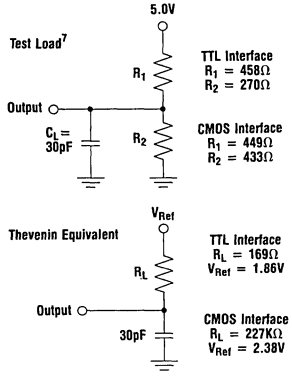
A.C. Electrical Characteristics Over the operating range[5].

Symbol	Parameter	273–30		273–35		273–40		Unit
		Min	Max	Min	Max	Min	Max	
t_{PD}	Propagation Delay, Input to Output		30		35		40	ns
t_{OE}	Input to Output Enable[6]		30		35		40	ns
t_{OD}	Input to Output Disable[6,7]		30		35		40	ns

Switching Waveforms



Test Loads



Notes:

1. Minimum DC input is −0.5V, however, inputs may undershoot to −2.0V for periods less than 30ns.
2. Test one output at a time. Duration of short circuit should not exceed 1 second.
3. All I/O pins open (no load).
4. Assumes worst-case conditions—all outputs loaded. V_{OL} = 0.5V @ I_{OL} = 15mA with one output loaded.
5. Test conditions assume: signal transitions of 5ns or less from the 10% and 90% points; timing reference levels of 1.5V (unless otherwise specified); and test loads shown.
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7. C_L includes scope and jig capacitance. t_{OD} is measured with C_L = 5pF.
8. V_{IO} specified is not for program/verify operation. Contact Gould for information regarding PEEL273 program/verify specifications.

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GOULD
AMI Semiconductors

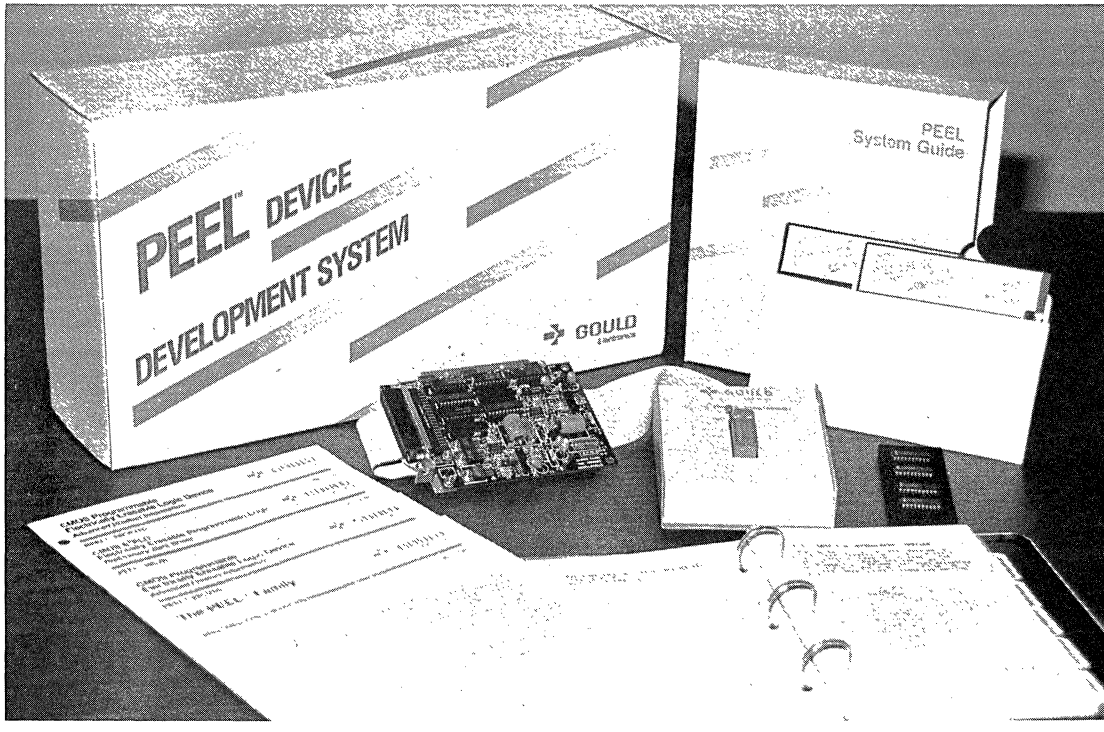
PEEL™ Development System, PDS

Features

- Development System for PEEL Devices
  - —Editor, logic assembler, translator programmer, and tester all in one system
  - —Runs on PC-compatible computers
- Conventional PLD Programmer Functions
  - —Program, Load, Verify, Secure
- APEEL™ Boolean Logic Assembler
  - —Supports all advanced features of PEEL devices
  - —"PALASM®-like" sum-of-products equations
  - —"ABEL™-like" macro cell definitions
  - —Logic simulation
- Translates Standard PLDs to PEEL Devices
  - —Loads PLD or reads JEDEC file
  - —Automatically translates to PEEL device
- Built-in File Editor
  - —Edit source, JEDEC, or test-vector files
- Enhanced Logic-Test Capabilities
  - —Tests device in socket to JEDEC test vectors
  - —Special features: single step, loop, capture
- Expandable and Accessible
  - —New features and devices supported with software updates
  - —No copy protection

General Description

The PEEL™ Development System is a powerful, yet inexpensive, PC-based system for designing with PEEL (Programmable Electrically Erasable Logic) devices. The PDS is a personal PLD work-station providing

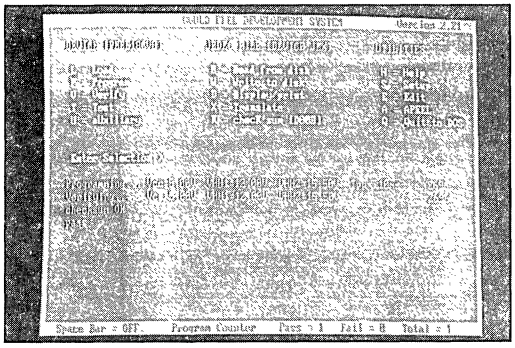


PEEL Development System, PDS

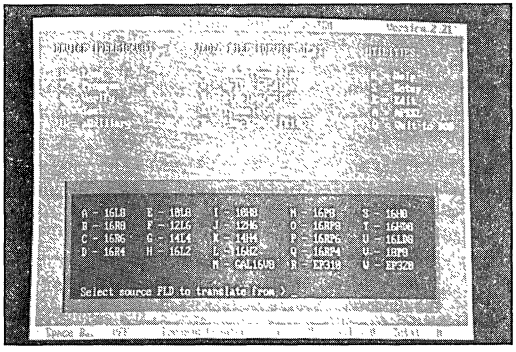
GOULD

AMI Semiconductors

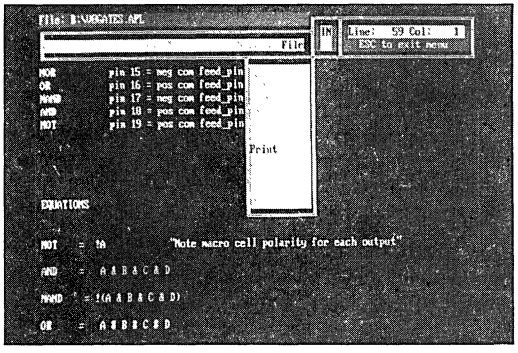
PEEL Development System, PDS



The PEEL Development System provides an editor, logic assembler, translator, programmer, and tester all in one integrated package.



Existing PLDs (i.e., PAL or EPLD) can be translated and programmed to a PEEL device



Built-in file editor with "WordStar®-like" commands allows design entry for APEEL source, test-vector, and formatted JEDEC files.

everything needed to implement your logic designs from concept to silicon. Several options for designing with PEEL devices are available with the PDS. For example, an existing PLD design (i.e., a PAL® or EPLD JEDEC file) can be automatically translated and programmed into a PEEL device. Additionally, the translation capability allows you to use your present PLD logic assembler or compiler to design with PEEL devices.

To fully support the advanced features of PEEL devices, the PDS also provides the tools needed to design from start to finish, including a built-in word processor for design entry and editing, the APEEL™ boolean-logic assembler, a complete PEEL-device programmer and enhanced logic tester.

The capabilities of the software-controlled programmer will be expanded as new devices are released by Gould. Registered owners are enrolled in the Gould software update service and receive programmer/development-software updates.

SYSTEM CONTENTS

Software

- PEEL Development System Software (on 5 1/4" 360K diskettes)

Hardware

- PEEL-device-programmer module with ribbon-cable connector
- PEEL-device programmer card
- Sample PEEL 18CV8 devices

Literature

- PEEL Development System Manual
- PEEL-device data sheets
- Gould license agreement and warranty
- Gould warranty/update registration card

SYSTEM REQUIREMENTS

- IBM-PC/XT/AT or compatible computer
- Minimum 256K RAM memory
- Monochrome or color display
- Two 360K floppy-disk drives or one floppy-disk drive and a hard disk
- DOS version 2.1 or greater

For more information contact:
Gould Inc., Semiconductor Division
2300 Buckskin Rd.
Pocatello, ID 83201
(208) 233-4690

PDS00189

GOULD

AMI Semiconductors

Static CMOS & NMOS ROMs

GOULD
AMI Semiconductors

Static CMOS & NMOS Family of ROMs

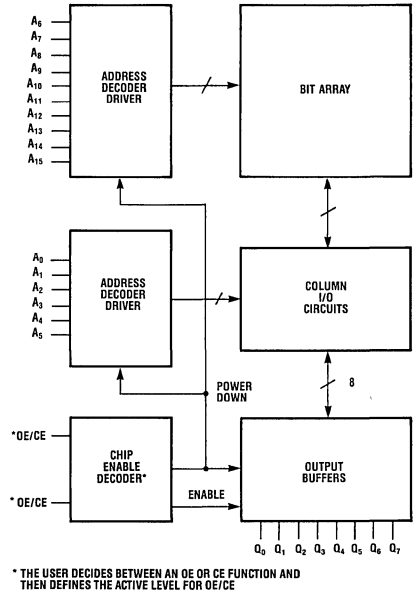
Features

- 16K, 32K, 64K, 128K, 256K, 512K, 1 Meg Selections
- Fast Access Time
- Mate With State Of The Art 32 Bit Microprocessors
- Low Standby Power CMOS
- Fully Static Operation
- Single +5V ±10% Power Supply
- Directly TTL Compatible For Clean Interface
- Three-State TTL Compatible Outputs
- EPROM Pin Compatible
- Late Mask Programmable For Quick Turn Times
- Programmable Output/Chip Enable

General Description

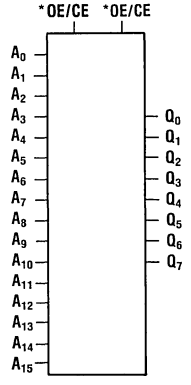
The Gould AMI family of ROMs are static mask programmable and organized by 8 bits. The device is fully TTL compatible on all inputs and outputs and uses a single +5V power supply. There are no requirements for clocks or refreshing, because they are static in operation. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices. OE/CE active level inputs and the memory contents are user defined.

Block Diagram



* THE USER DECIDES BETWEEN AN OE OR CE FUNCTION AND THEN DEFINES THE ACTIVE LEVEL FOR OE/CE

Logic Symbol



Pin Names

A_0–A_{15}	Address Inputs
Q_0–Q_7	Data Outputs
OE/CE	Output Enable/Chip Enable
V_{CC}; GND; NC	5V; Ground; No Contact

ROM FAMILY

Static CMOS & NMOS Family of ROMs

Table 1.

Device Name	S6316	S6333/S63332	S63364
Process	CMOS	CMOS	CMOS
Capacity	16K	32K	64K
Organization	2K x 8	4K x 8	8K x 8
Compatible EPROM	2516	2732/2532	68764
Number of Pins	24	24 (A)/24 (B)	24
Plastic Dip Package Available	YES	YES	YES
Ceramic Dip Package Available	YES	YES	YES
SOIC Plastic Package Available	NO	NO	NO
Temperature Range: C/I/M; 0 to 70°C/−40 to 85°C/−55 to 125°C	C/I/M	C/I/M	C/I/M

Electrical Characteristics: V_{CC} = +5V ±10%

Symbol	Parameter	Units	Min.	Max.	Min.	Max.	Min.	Max.
V_{ol}	Output LOW Voltage (I_{ol}=3.2mA)	V		0.4		0.4		0.4
V_{oh}	Output HIGH Voltage	V	2.4		2.4		2.4	
I_{oh}	Output HIGH Current		−1.0 mA		−1.0 mA		−1.0 mA	
V_{il}	Input LOW Voltage	V	−0.3	0.8	−0.3	0.8	−0.3	0.8
V_{ih}	Input HIGH Voltage	V	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3
IL_i	Input Leakage Current	µA	−1	1	−1	1	−1	1
IL_o	Output Leakage Current	µA	−10	10	−10	10	−10	10
I_{cc1}	Power Supply Current—TTL Active	mA	Note 3	40	Note 3	40	Note 3	40
I_{cc2}	Power Supply Current—CMOS Active	mA	Note 4	35	Note 4	35	Note 4	35
I_{sb1}	Power Supply Current—TTL	mA	Note 5	2	Note 5	2	Note 5	2
I_{sb2}	Power Supply Current—CMOS	µA	Note 6	100	Note 6	100	Note 6	100
t_{AA}	Address Access Time—Commercial Temp.	ns		100/120		100/120		100/120
	Industrial Temp.			150		150		150
	Mil Temp.			175		175		175
t_{ACE}	Chip Enable Access Time	ns		100/120		100/120		100/120
	Industrial Temp.			150		150		150
	Mil Temp.			175		175		175
t_{OE}	Output Enable Access Time	ns		70		70		70
	Industrial Temp.			75		75		75
	Mil Temp.			80		80		80
t_{CEO}	Disable Time From Chip Enable	ns	0	50	0	50	0	50
	Industrial Temp.		0	65	0	65	0	65
	Mil Temp.		0	70	0	70	0	70
t_{OEO}	Disable Time From Output Enable (Note 5)	ns	0	50	0	50	0	50
	Industrial Temp.		0	65	0	65	0	65
	Mil Temp.		0	70	0	70	0	70
t_{OH}	Output Hold Time	ns	0		0		0	
	Industrial Temp.		0		0		0	
	Mil Temp.		0		0		0	

Notes
1. NMOS Power Test: $V_{CC}=V_{CCmax}$; OE/CE=Active; Address inputs @ V_{il}
2. NMOS Standby Power Test: Same as Note 1 except CE=Deselected
3. CMOS Power Test: TR=150ns, duty=100%
4. CMOS Active Test: TR=150ns, duty=100%, V_i=Gnd or V_{cc}
5. Deselect Power Test: Chip in Standby Mode, $V_i=V_{il}$ or V_{ih}
6. Standby Power Test: Chip in Standby Mode, V_i=Gnd or V_{cc}
7. In Notes 1 through 6 the Output Loads are Disconnected.

‡ Package under development

Static CMOS & NMOS Family of ROMs

Table 1. (continued)

					Preliminary
Device Name	S6364	S23128	S63256	S63512	S631000/S631001
Process	CMOS	NMOS	CMOS	CMOS	CMOS
Capacity	64K	128K	256K	512K	1 Meg
Organization	8K x 8	16K x 8	32K x 8	64K x 8	128K×8
Compatible EPROM	2764	27128	27256	27512	27011/27010
Number of Pins	28	28	28	28	28/32
Plastic Dip Package Available	YES	YES	YES	YES	YES
Ceramic Dip Package Available	YES	YES	YES	NO	YES
SOIC Plastic Package Available	YES	YES	YES	NO	NO
PLCC Package Available	YES	NO	YES	YES	YES
Temp Range: C/I/M; 0 to 70°C/−40 to 85°C/−55 to 125°C	C/I/M	C/I/M	C/I/M	C/I/M‡	C/I/M

Electrical Characteristics: V_{CC} = +5V ±10%

Symbol	Parameter	Units	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{ol}	Output LOW Voltage (I_{ol}=3.2mA)	V		0.4		0.4		0.4		0.4		0.4
V_{oh}	Output HIGH Voltage	V	2.4		2.4		2.4		2.4		2.4	
I_{oh}	Output HIGH Current		−1.0 mA		−220 µA		−1.0 mA		−1.0 mA		−1.0mA	
V_{il}	Input LOW Voltage	V	−0.3	0.8	−0.5	0.8	−0.3	0.8	−0.3	0.8	−0.3	0.8
V_{ih}	Input HIGH Voltage	V	2.2	V_{CC} + 0.3	2.0	V_{CC}	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC}+0.3
IL_i	Input Leakage Current	µA	−1	1	−10	10	−1	1	−1	1	−1	1
IL_o	Output Leakage Current	µA	−10	10	−10	10	−10	10	−10	10	−10	10
I_{cc1}	Power Supply Current—TTL Active	mA	Note 3	40	Note 1	80	Note 3	40	Note 3	50	Note 3	50
I_{cc2}	Power Supply Current—CMOS Active	mA	Note 4	35			Note 4	35	Note 4	45	Note 4	45
I_{sb1}	Power Supply Current—TTL	mA	Note 5	2	Note 2	20	Note 5	2	Note 5	2	Note 5	2
I_{sb2}	Power Supply Current—CMOS	µA	Note 6	100			Note 6	100	Note 6	150	Note 6	150
t_{AA}	Address Access Time—Commercial Temp.	ns		100/120		250		120/150		150		150/200
	Industrial Temp.			150		280		175		175		200
	Mil Temp.			175		300		200		200		250
t_{ACE}	Chip Enable Access Time	ns		100/120		250		120/150		150		150/200
	Industrial Temp.			150		280		175		175		200
	Mil Temp.			175		300		200		200		250
t_{OE}	Output Enable Access Time	ns		70		80		70		80		80
	Industrial Temp.			75		115		75		85		90
	Mil Temp.			80		120		80		90		100
t_{CEO}	Disable Time From Chip Enable	ns	0	50	0	80	0	50	0	60	0	70
	Industrial Temp.		0	65	0	115	0	65	0	75	0	80
	Mil Temp.		0	70	0	120	0	70	0	80	0	90
t_{OEO}	Disable Time From Output Enable (Note 5)	ns	0	50	0	80	0	50	0	60	0	70
	Industrial Temp.		0	65	0	115	0	65	0	75	0	80
	Mil Temp.		0	70	0	120	0	70	0	80	0	90
t_{OH}	Output Hold Time	ns	0		0		0		0		0	
	Industrial Temp.		0		0		0		0		0	
	Mil Temp.		0		0		0		0		0	

Notes
1. NMOS Power Test: $V_{cc}=V_{ccmax}$; OE/CE=Active; Address inputs @ V_{il}
2. NMOS Standby Power Test: Same as Note 1 except CE=Deselected
3. CMOS Power Test: TR=150ns, duty=100%
4. CMOS Active Test: TR=150ns, duty=100%, V_i=Gnd or V_{cc}
5. Deselect Power Test: Chip in Standby Mode, $V_i=V_{il}$ or V_{ih}
6. Standby Power Test: Chip in Standby Mode, V_i=Gnd or V_{cc}
7. In Notes 1 through 6 the Output Loads are Disconnected.

‡ Package under development

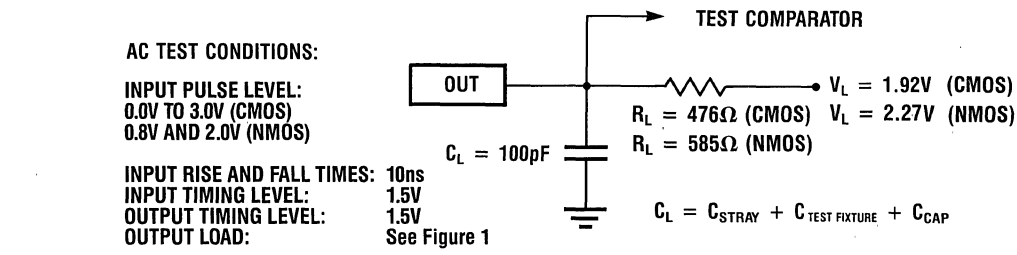
ROM FAMILY

Static CMOS & NMOS Family of ROMs

Capacitance: T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Minimum	Maximum	Units	Conditions
C_{IN}	Input Capacitance		7	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance		10	pF	V_{OUT} = 0V

Figure 1



Application of Gould ROMs

All of the ROMs offered by Gould are fully static, asynchronous, non-multiplexed devices. No matter what microprocessor you're using in your system, careful planning will give you the greatest flexibility in using our ever-expanding family of ROMs.

No Clocks Are Required

A clock is *not* required by our ROMs to latch addresses, precharge internal circuitry, or perform any other function. All control lines (CE, or OE) may remain in a valid read state for an indefinite period of time, during which the address inputs may be changed as desired to access various stored data.

The Address Inputs Must Be Valid for the Entire Cycle

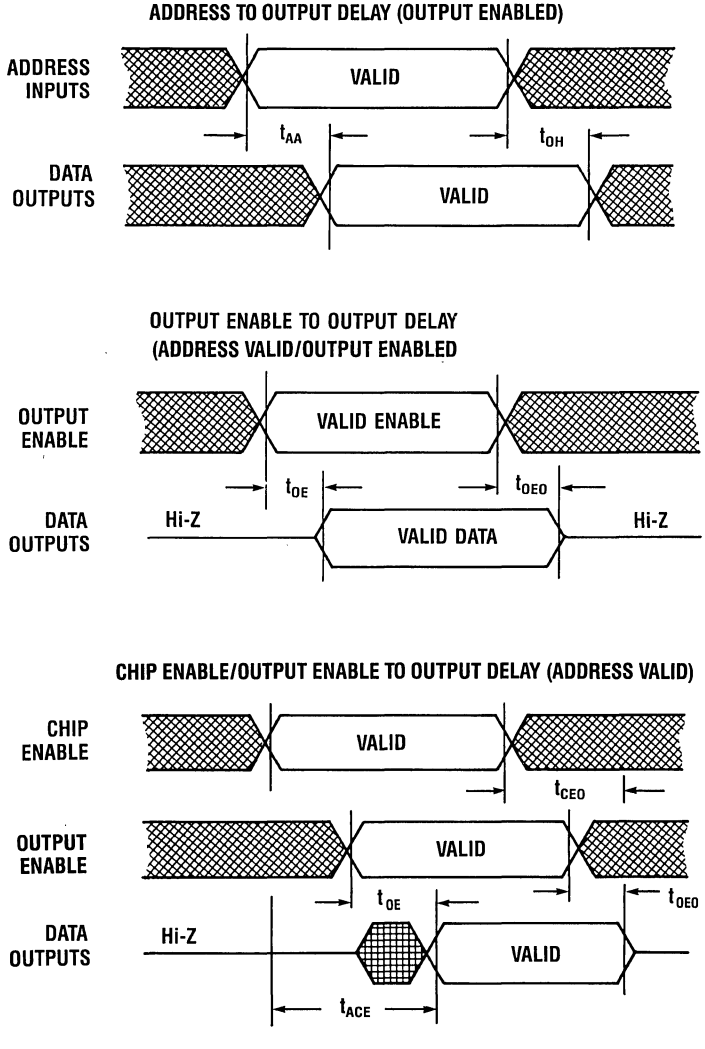
The addresses must be held constant to a Gould ROM until the output data has been placed onto the system data bus and read by the microprocessor or a peripheral device. If the microprocessor is one of several common types using a multiplexed address/data bus, the system design must incorporate latches to extract address information from this bus and supply the latched addresses to our ROM.

Flexibility on Control Line Programming

You can use the programmable control functions to your best advantage. Let's take the S6364 as an example. If four S6364s are used in a system, pin 22 on each device could be a common OE signal for a master tristate control; pin 20 on each device could be a master powerdown control; and pins 26 and 27 could serve as 1-of-4 addressing to select which of four ROMs is active.

Another possibility would be to use all four control lines on the S6364 as higher order addresses. While the data sheet may show different labels on these pins to conform with common industry practice, all control lines on the S6364 can in reality be programmed with equal flexibility. Taking advantage of this, sixteen S6364 devices can be addressed from four control lines. These control lines can be all powerdown, all non-powerdown, or any combination. With this approach, a later system evolution to higher density ROMs means that the correct signals are already in place for both addressing and bus control.

AC Timing Diagram



ROM FAMILY

Figure 1. Example of minimum configuration for a Gould ROM and a microprocessor using a non-multiplexed address bus.

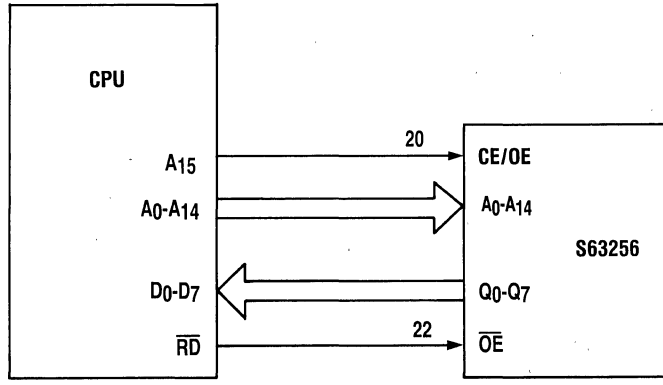
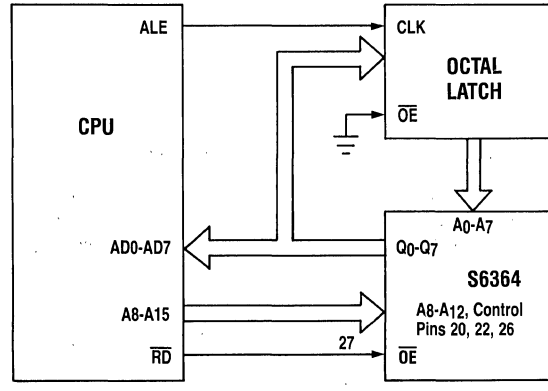


Figure 2. Example of a minimum configuration for a system using a multiplexed address/data bus.



Static CMOS & NMOS Family of ROMs

Powerdown or Not: It's Up to You
Finally, you have the option on most of our ROMs to choose whether or not to incorporate powerdown or standby capability. The key is in the control line programming that you specify when the order is placed. Any pin specified as a Chip Enable, either high or low, can place the device into a powerdown mode as well as place all outputs in a tristate condition. In powerdown, or standby, the device draws much less current than in the active mode.

If, instead a pin is programmed as Output Enable, that pin controls only the output mode (active or tristate); device current is relatively constant. All Gould ROMs which provide powerdown capability allow you to choose your own combination of CE and OE. For example, the S23128 can be programmed with three CE functions, or one CE and two OE, etc.

When you are making a decision between CE and OE programming, note that standby current is not the only difference in the two options. Because of the differences in internal circuitry being controlled, a CE pin has relatively long access time, perhaps 250ns, compared to a OE pin, perhaps 80ns. Therefore, system timing requirements must be evaluated when weighing the relative merits of programming for powerdown.

Another item to consider is printed circuit (PC) board layout. A powerdown device has a noticeable change in power supply current when it is switched into the active mode. Careful PC board layout and power supply decoupling will prevent the introduction of noise into your system. This noise is due to the interaction of the change in current and the inherent inductance of PC board wiring traces.

Note that a device whose outputs are switched to the active state by a OE pin will not exhibit this change in power supply current, however, power supply decoupling is still recommended. A device which is simply in an output tristate mode and not in powerdown shows little difference in current compared to the active mode.

Table 2. Control Line Options
AMI ROMs offer you the choice of control line functions as well as the active level. The possible functions and active level for each pin are shown below (a "bar" above the function name means active low).

CE Function = Power Down
OE Function = Non Power Down, tristate output control only
DC = Don't Care (Control pins programmed as DC have no effect on either the powerdown mode or tristate control but are still connected to input protection devices.)

2K x 8 (16K) 24 Pin S6316 CMOS
Pins 21-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
20-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
18-OE, $\overline{OE}$, CE, $\overline{CE}$, DC

4K x 8 (32K) 24 Pin S6333 CMOS
Pins 20-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
18-OE, $\overline{OE}$, CE, $\overline{CE}$, DC

4K x 8 (32K) 24 Pin S63A332 CMOS
Pins 20-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
21-OE, $\overline{OE}$, CE, $\overline{CE}$, DC

8K x 8 (64K) 24 Pin S63364 (CMOS)
Pin 20-OE, $\overline{OE}$, CE, $\overline{CE}$, DC

8K x 8 (64K) 28 Pin S6364 CMOS
Pins 27-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
26-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
22-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
20-OE, $\overline{OE}$, CE, $\overline{CE}$, DC

16K x 8 (128K) 28 Pins S23128 NMOS
Pins 27-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
22-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
20-OE, $\overline{OE}$, CE, $\overline{CE}$, DC

32K x 8 (256K) 28 Pin S63256 CMOS
Pins 22-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
20-OE, $\overline{OE}$, CE, $\overline{CE}$, DC

64K x 8 (512K) 28 Pin S63512 CMOS
Pins 22-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
20-OE, $\overline{OE}$, CE, $\overline{CE}$, DC

128K x 8 (1 MEG) 28 Pin S631000 CMOS
Pin 20-OE, $\overline{OE}$, CE, $\overline{CE}$, DC

128K x 8 (1 MEG) 32 Pin S631001 CMOS
Pins 31-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
30-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
24-OE, $\overline{OE}$, CE, $\overline{CE}$, DC
22-OE, $\overline{OE}$, CE, $\overline{CE}$, DC

Static CMOS & NMOS Family of ROMs

Truth Table: (For simplicity, all control functions in the Truth Table are defined as active high).

OE/CE	OE/CE	Outputs	Power
$\overline{CE}$	X	HI-Z	STANDBY
X	$\overline{CE}$	HI-Z	STANDBY
$\overline{OE}$	$\overline{OE}$/CE	HI-Z	ACTIVE
OE/CE	$\overline{OE}$	HI-Z	ACTIVE
OE/CE	OE/CE	DATA OUT	ACTIVE

How to Get Your ROMs Fast

ROM Ordering Simplified
The following information should be included in the purchase order when ROM devices are being ordered:

—Part number
—Quantity of prototypes for each pattern (if any)
—Total quantity of each pattern
—Pricing and delivery (quotes can be obtained from any Gould AMI sales office)
—Package type (plastic or ceramic)
—Special marking (if required)
—Access speed
—Required temperature range

ROM Code Data

The preferred method of receiving ROM CODE DATA is by electronic data transmission or in EPROM. For EPROM ROM CODE DATA submission, two EPROMs should be submitted. One is programmed to the desired code and the other is blank. Gould AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees the the EPROM has been properly entered into the Gould AMI computer system. The Gould AMI programmed EPROM is returned to the customer for verification of the ROM data. Unless otherwise requested, Gould AMI will not proceed until the customer has returned the ROM CODE VERIFICATION form.

For electronic data transmission, contact your Gould AMI sales office for details.

Customer Requirements
Upon your approval of the returned EPROM and receipt of your purchase order by Gould, masks are generated for production. Prototypes can be furnished to you upon request. Depending upon the volume required, production shipments are made within six to eight weeks after code approval and receipt of the purchase order. Under the Gould corporate policy, if at any time you wish to cancel your code, you are liable for all work in process (WIP). For additional information on cancellation charges, please contact your local Gould sales office.

Other Programming Requirements
Depending upon the ROM required, you must define the correct pinout options. Programmable pins are either chip enable (CE) high or low, don't care (DC), or output enable (OE) high or low. *If a device pin is designated with a CE function, that pin can put the device into a powerdown condition. If OE function is used for a pin, that pin cannot control powerdown for the device. If a device has all control pins designated with OE functions, it is a non-powerdown device.*

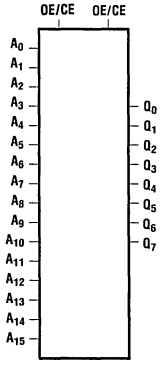
If a drawing of your pin configuration is available, it should be provided at the time of EPROM conversion along with any special package marking requirements.

Your Access Time Requirements
As a further guarantee that the correct Gould device type has been specified, the following switching characteristics need to be defined by you when the order is placed.

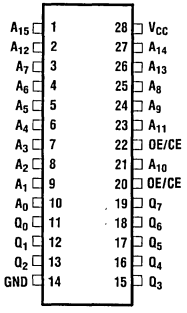
TAA (Address Access Time)
TACE (Chip Enable Access Time)
TAOE (Output Enable Access Time)

Static CMOS & NMOS Family of ROMs

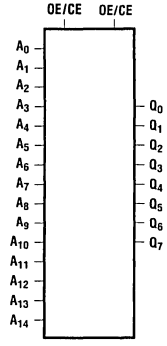
Logic Symbol 512K



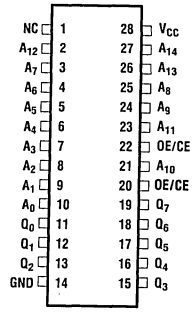
Pin Configuration 512K



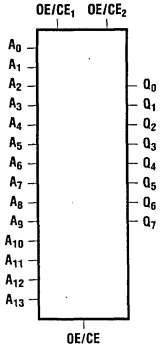
Logic Symbol 256K



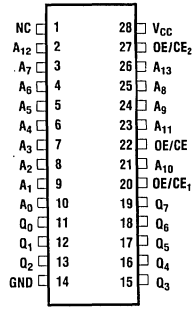
Pin Configuration 256K



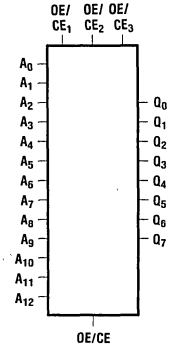
Logic Symbol 128K



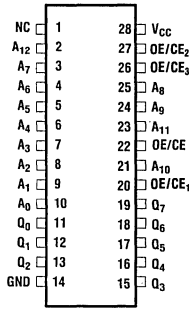
Pin Configuration 128K



Logic Symbol 64K



Pin Configuration 64K 28 Pin

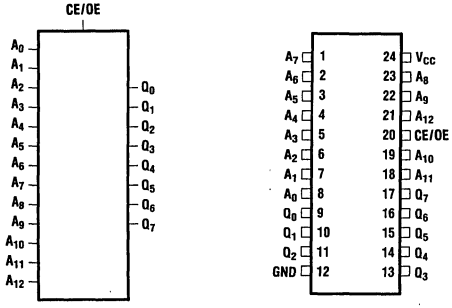


ROM FAMILY

Static CMOS & NMOS Family of ROMs

Logic Symbol 64K — Pin Configuration 64K

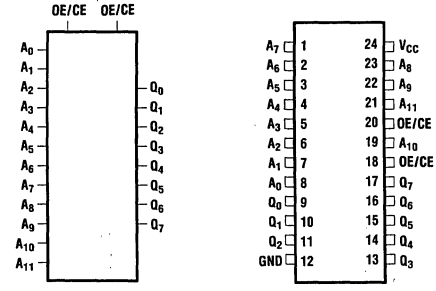
24 Pin



(A)

Logic Symbol 32K — Pin Configuration 32K

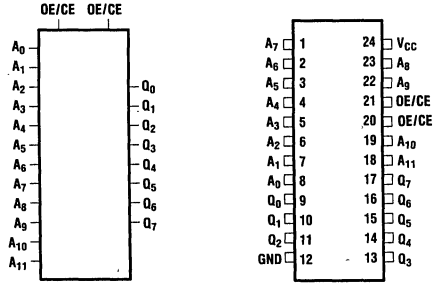
S6333



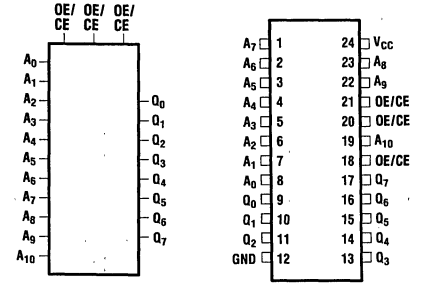
(B)

Logic Symbol 32K — Pin Configuration 32K

S63332



Logic Symbol 16K — Pin Configuration 16K



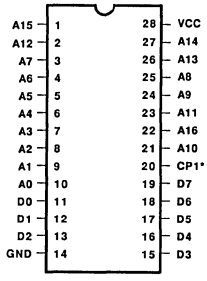
GOULD

AMI Semiconductors

Static CMOS & NMOS Family of ROMs

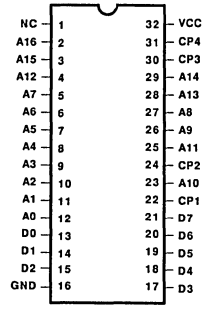
28 Pin P-Dip

S361000



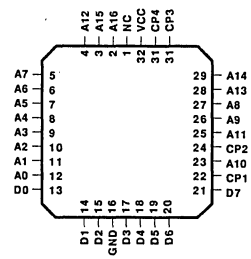
32 Pin P-Dip

S361001



32 Pin PLCC

S631001

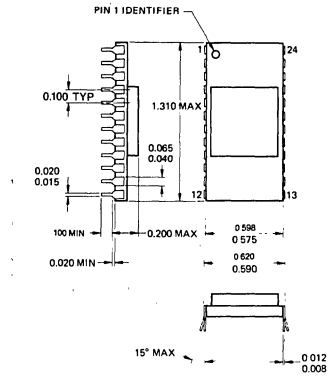


CP=OE/CE/DC

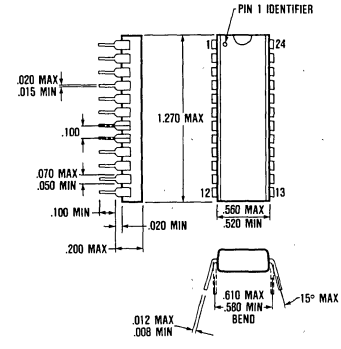
ROM FAMILY

Static CMOS & NMOS Family of ROMs

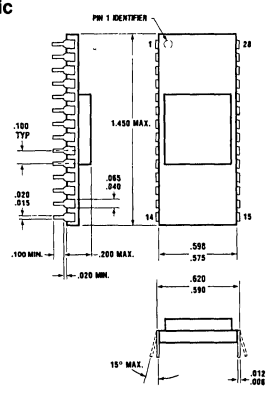
24-Lead Ceramic DIP Outline



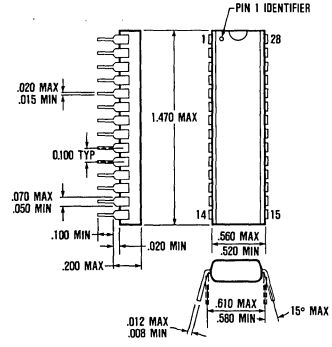
24-Lead PDIP Outline



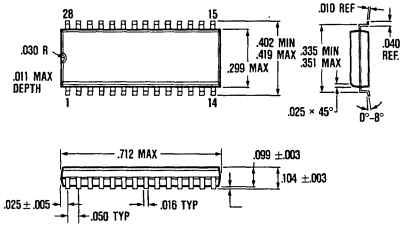
28-Lead Ceramic DIP Outline



28-Lead PDIP Outline

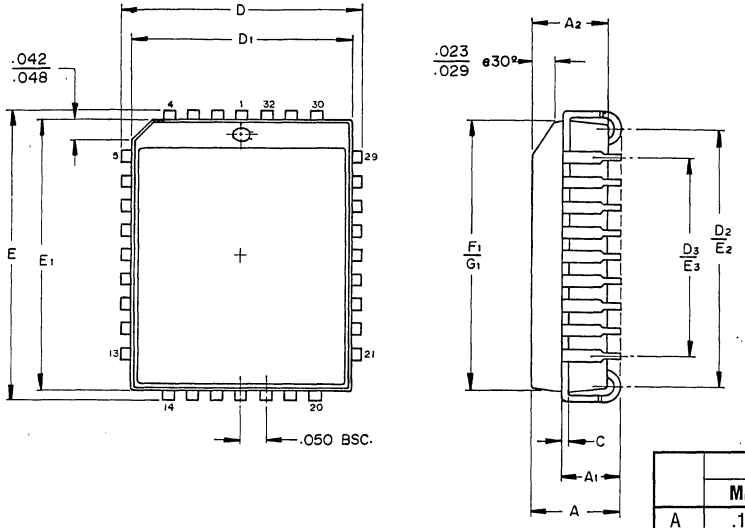


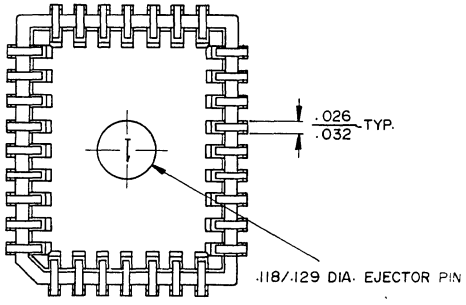
28-Lead SOIC Outline



Static CMOS & NMOS Family of ROMs

PLCC Outline



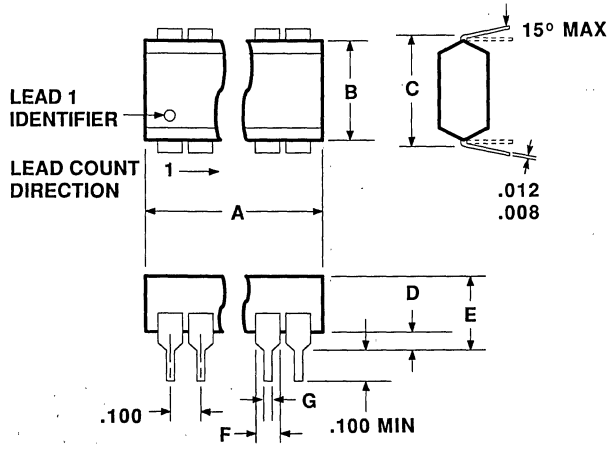


	DIMENSIONS (INCHES)			NOTE
	MIN.	NOM.	MAX.	
A	.123	.130	.140	
A_1	.078	.085	.095	
A_2	.106	.109	.112	
D	.485	.490	.495	
D_1	.449	.451	.453	3
D_2	.390	.420	.430	2
D_3		.300 REF.		
E	.585	.590	.595	
E_1	.549	.551	.553	3
E_2	.490	.520	.530	2
E_3		.400 REF.		
F_1	.441	.443	.445	9
G_1	.541	.543	.545	9
N		32		5
N_D		7		
N_E		9		
C	.0097	.0100	.0103	

ROM FAMILY

Static CMOS & NMOS Family of ROMs

P-DIP Outline



SYM	Dimensions	
	Lead Count	
	28	32
A	1.470 MAX	1.655 MAX
B	.560 .520	.560 .520
C	.610 .580	.610 .580
D	.020 MIN	.020 MIN
E	.200 MAX	.200 MAX
F	.070 .050	.040 .060
G	.020 .015	.020 .015

GOULD

AMI Semiconductors

1M Bit (131,072×8) Static CMOS Mask ROM

Preliminary Data Sheet

S631000/S631001

Features

- Fast Access Time:
  S631000-15/S631001-15—150ns
  S631000-20/S631001-20—200ns
- Fully Static Operation
- Low Power Dissipation
  Active: 275mW Maximum
  Standby: 825μW Maximum
- Single +5V$\pm$10% Power Supply
- Directly TTL Compatible Inputs
- Three-State TTL Compatible Outputs
- Late Mask Programmable
- Programmable Chip Select/Enable or Programmable Output Enable
- EPROM Compatible (see table 1)
- JEDEC Standard 32 pin dip—S631001
- JEDEC Standard 28 pin dip—S631000
- 32 Lead PLCC package available—S631001

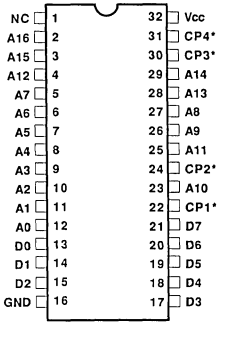
General Description

The Gould AMI S631000 device is a 1,048,576 bit static mask programmable CMOS ROM organized as 131,072 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and uses a single +5V power supply. The three-state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

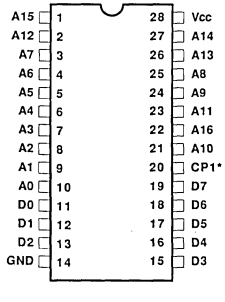
The S631000 is pin compatible with most UV EPROMS, making system development much easier and more cost effective. The device is fully static, requiring no clocks for operation. The four control pins are mask programmable, with the active level and function for each being specified by the user. When a chip enable pin is not enabled, the power supply current is reduced to a 150μA maximum.

Pin Configuration

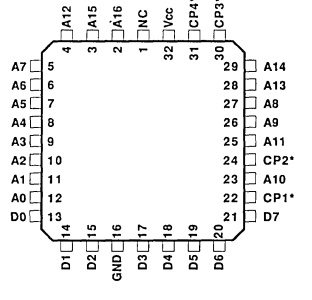
S631001
32 PIN P-DIP



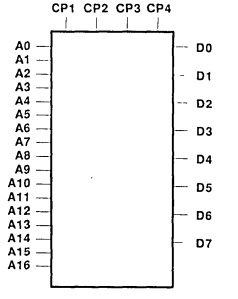
S631000
28 PIN P-DIP



S631001
32 PIN PLCC



Logic Symbol



NOTE: CP2, CP3 AND CP4 - S631001 ONLY

Pin Names	
A0 - A16	Address Inputs
D0 - D7	Data Outputs
CP1 - CP4	Control Pins
V_{CC}	+5 Volts Supply
GND	Ground

The user decides the control pin function and then defines the active level. The function may also be defined as Don't Care (DC). The chip is enabled when the inputs match the user defined states. Don't Care pins are still connected to input protection diodes and are subject to "Absolute Maximum Ratings"

Control Pin Options

All control pins CP1 - CP4, can be programmed as:
* CE, /CE, OE, /OE, Don't Care
S631000
Pin 20 (CP1)
S631001
Pin 22 (CP1)
Pin 24 (CP2)
Pin 30 (CP3)
Pin 31 (CP4)

*CS is equivalent to OE.

ROM FAMILY

Absolute Maximum Ratings

Ambient Temperature Under Bias—T_A	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Operating Temperature	+125°C
Input or Output Voltages	−0.3 to V_{CC} +0.3V
Maximum Current	50mA
Maximum Power	350mW

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics: V_{CC} =5V±10%, T_A =0°C to 70°C

Symbol	Parameter	Minimum	Maximum	Units	Conditions
V_{OL}	Output LOW Voltage		0.4	V	
V_{OH}	Output HIGH Voltage	2.4		V	
V_{IL}	Input LOW Voltage	−0.3	0.8	V	
V_{IH}	Input HIGH Voltage	2.2	V_{CC}+0.3	V	
I_{LI}	Input Leakage Current	−1.0	1.0	μA	V_{IN}=0V to V_{CC}
I_{LO}	Output Leakage Current	−10	10	μA	V_O=0V to V_{CC}, Chip Deselected
I_{CC1}	Power Supply Current—Active		50.0	mA	I_O=0, TR=T_{CYC}, duty=100% V_I=0.8V or 2.2V
I_{CC2}	Power Supply Current—Active		30.0	mA	I_O=0, TR=T_{CYC}, duty=100% V_I=GND or V_{CC}
I_{SB1}	Power Supply Current—Standby		2.0	mA	Chip in standby mode, V_I=V_{IL} or V_{IH}
I_{SB2}	Power Supply Current—Standby		150	μA	Chip in standby mode, V_I=GND or V_{CC}

Capacitance: T_A =25°C, f=1.0MHz

Symbol	Parameter	Minimum	Maximum	Units	Conditions
C_{IN}	Input Capacitance		7	pf	V_{IN}=0V
C_{OUT}	Output Capacitance		10	pf	V_{IN}=0V

AC Electrical Characteristics: V_{CC} = +5V±10%, T_A = 0°C to 70°C

Symbol	Parameter		Minimum	Maximum
T_{CYC}	Period	S631000-15/S631001-15 S631000-20/S631001-20	150ns 200ns	
T_{AA}	Address Access Time	S631000-15/S631001-15 S631000-20/S631001-20		150ns 200ns
T_{ACE}	Chip Enable Access Time	S631000-15/S631001-15 S631000-20/S631001-20		150ns 200ns
T_{OE}	Output Enable Access Time	S631000-15/S631001-15 S631000-20/S631001-20		80ns 100ns
T_{HOLD}	Output Hold Time	S631000-15/S631001-15 S631000-20/S631001-20	0ns 0ns	
T_{CD}	Chip Disable Time	S631000-15/S631001-15 S631000-20/S631001-20	0ns 0ns	50ns 50ns

NOTE: See AC Timing Diagram and Test Load for Conditions

ROM Code Data

The preferred method of receiving ROM CODE DATA is by electronic data transmission or in EPROM. For EPROM ROM CODE DATA submission, two EPROMs should be submitted. One is programmed to the desired code and the other is blank. Gould AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees the the EPROM has been properly entered into the Gould AMI computer system. The Gould AMI programmed EPROM is returned to the customer for verification of the ROM data. Unless otherwise requested, Gould AMI will not proceed until the customer has returned the ROM CODE VERIFICATION form.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 27010/27011
Optional 2 - 27512

If two EPROMS are used to specify one ROM pattern, the programmed EPROMs must clearly state which of the EPROMs is for the lower and upper address locations in the ROM.

For electronic data transmission consult Gould sales office for details.

Pattern Data from ROMs

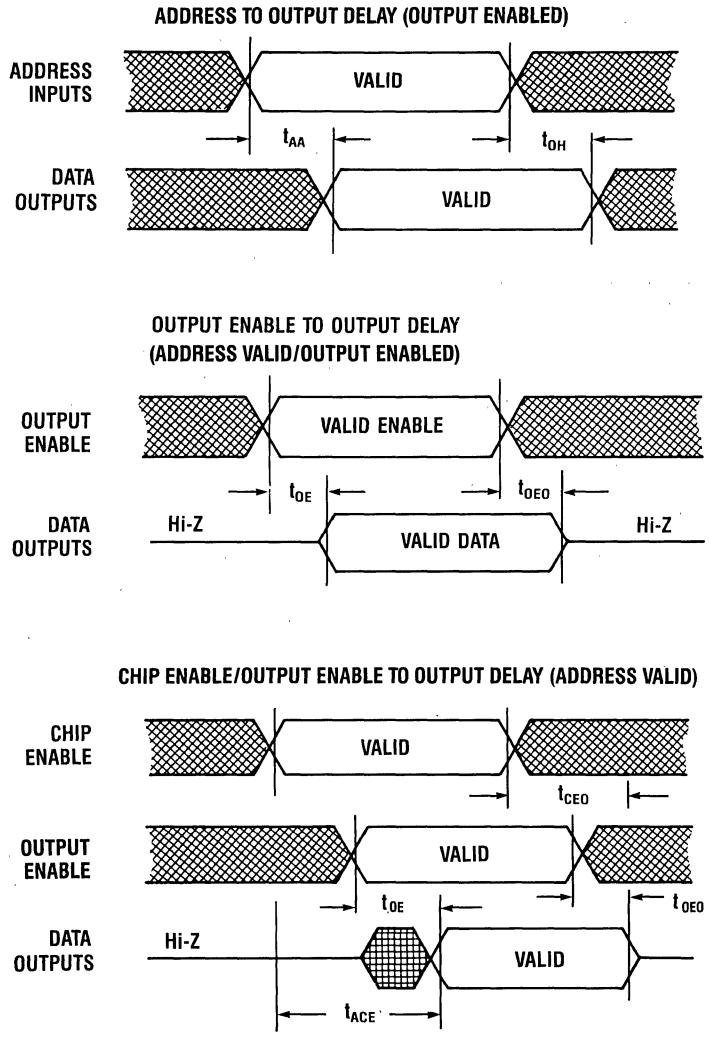
If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern instead of EPROMs. Obviously, these ROMs must be pin compatible with the Gould device. (NOTE: In some cases a competitor's ROM may have a different chip select or enable that is not customer defined. However, if this pin is customer defined for the Gould ROM, the required active logic level for this input must be specified.)

Optional Method of Supplying ROM Data*

If an EPROM or ROM cannot be supplied, and electronic data transmission cannot be used, the ROM CODE DATA can be provided on floppy disc (5¼" floppy disc).

*Consult Gould sales office for format.

AC Timing Diagram

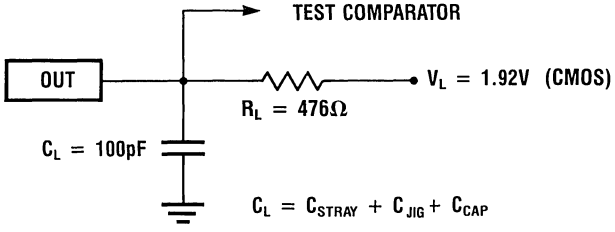


Test Load

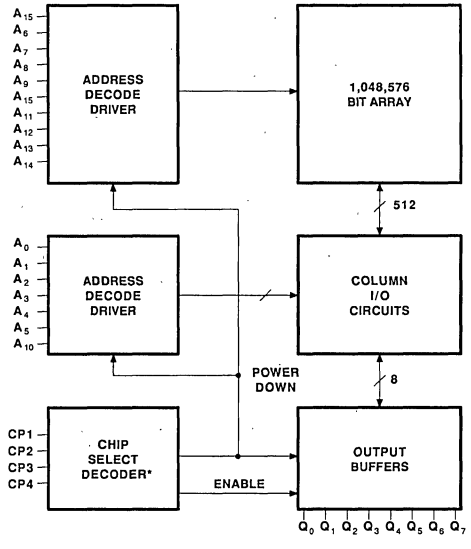
AC TEST CONDITIONS:

OUTPUT REFERENCE LEVELS:
LOW 0.8V
HIGH 2.0V

INPUT PULSE LEVEL:
0.6V AND 2.2V



Block Diagram

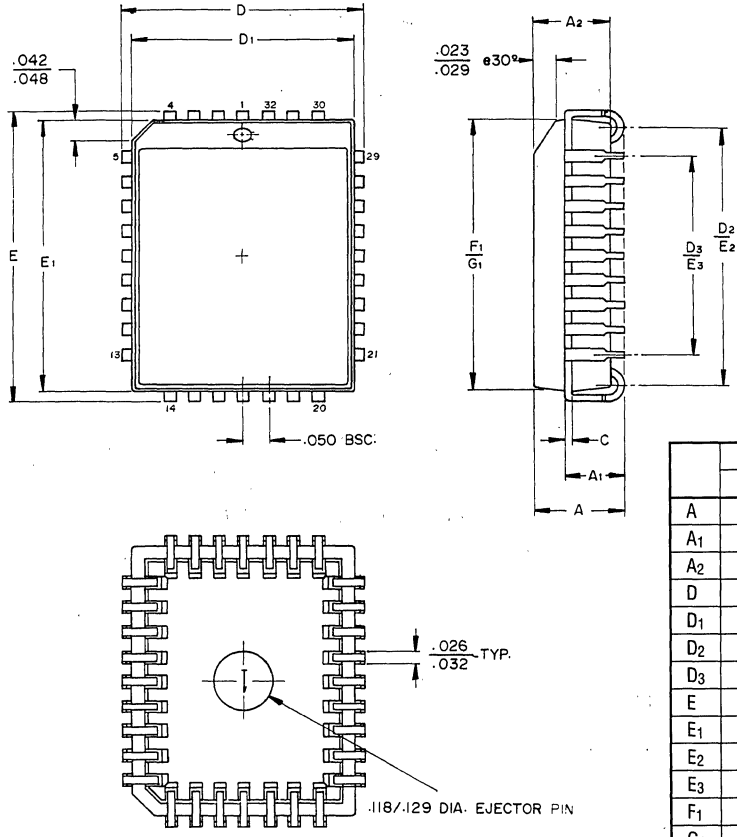


EPROM Cross Reference

UV EPROM Manufacturer	Gould AMI Device S631000 28 pin dip	Gould AMI Device S631001 32 pin dip
AMD		27C010
Fujitsu	27C100	27C1001
Hitachi	27C301	27C1001
Intel	27011	27010 27C010
Mitsubishi	27C100	27C101
National		27C1023
NEC	27C1000	27C1001

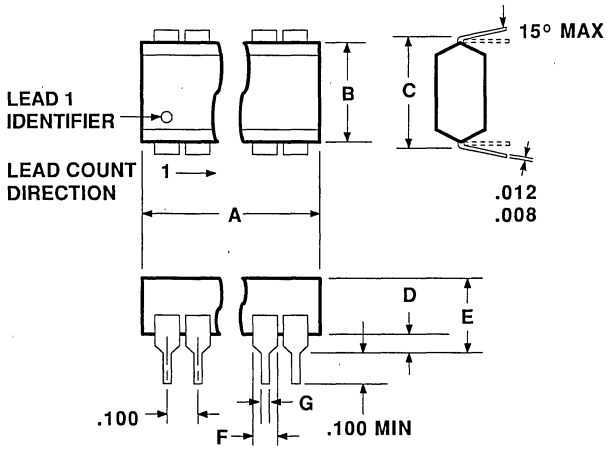
ROM FAMILY

PLCC Outline



	DIMENSIONS (INCHES)			NOTE
	MIN.	NOM.	MAX.	
A	.123	.130	.140	
A_1	.078	.085	.095	
A_2	.106	.109	.112	
D	.485	.490	.495	
D_1	.449	.451	.453	3
D_2	.390	.420	.430	2
D_3	.300 REF.			
E	.585	.590	.595	
E_1	.549	.551	.553	3
E_2	.490	.520	.530	2
E_3	.400 REF.			
F_1	.441	.443	.445	9
G_1	.541	.543	.545	9
N	32			5
N_D	7			
N_E	9			
C	.0097	.0100	.0103	

P-DIP Outline



SYM	Dimensions	
	Lead Count	
	28	32
A	1.470 MAX	1.655 MAX
B	.560 .520	.560 .520
C	.610 .580	.610 .580
D	.020 MIN	.020 MIN
E	.200 MAX	.200 MAX
F	.070 .050	.040 .060
G	.020 .015	.020 .015

ROM FAMILY

GOULD
AMI Semiconductors

Mask ROMs Minimize Cost

Application Note

Using mask ROMs in place of EPROMs offers an ideal solution to many manufacturers seeking cost reduction.

Although EPROMs offer the flexibility to debug code and to do field upgrades, this flexibility comes at a higher price.

This application note is a quick, comprehensive reference for a buyer of EPROMs who is interested in the advantages of using Gould late mask programmable ROMs in a debugged, volume application.

Included are:

- Cost/Volume considerations
- Compatibility issues
- Specific EPROMs which can be replaced
- Ordering information

Cost/Volume Considerations

Mask ROMs require fewer fabrication steps than EPROMs and are often assembled in plastic, not window cerdip packages. This is why mask ROMs can inherently cost less than EPROMs. However, the additional fixed mask charge increases the effective piece price for ROMs in low volumes.

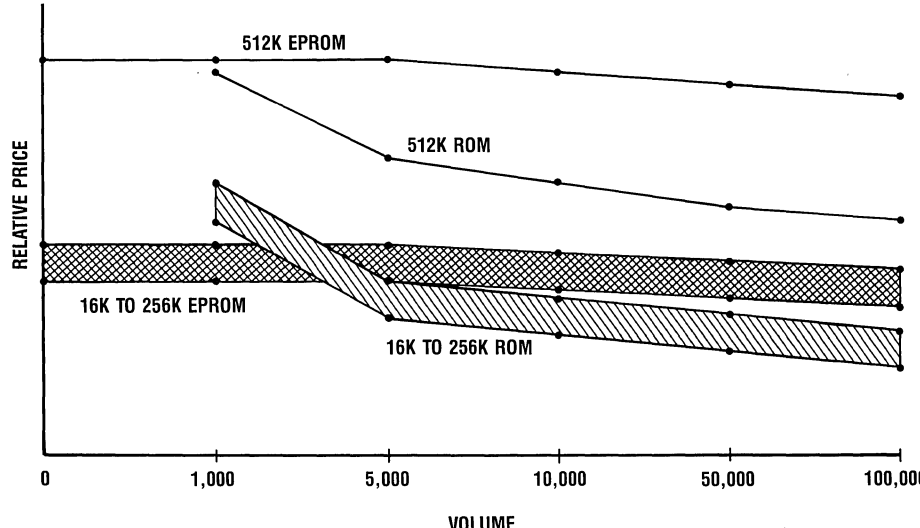
The total cost of EPROMs includes programming fees (as high as $.50 per part) or equipment, programming personnel, part labeling and inventory costs after the EPROMs are completed. This inventory cost can be comparable to mask ROM inventory costs.

Compatibility Issues

Many performance issues are nearly identical between ROMs and EPROMs such as:

- Storage and operating temperature
- V_{CC} Tolerance
- Input and output leakage
- Packaging (600mil dip, standard pinouts)
- Access times (for popularly priced devices)

Relative ROM Pricing



(Price source is 1987–88 Dataquest)

Other issues usually favor Gould Semiconductor late mask programmable ROMs:

- Alternate packages (28 pin SOIC, for example)
- Lower power dissipation
- Reliability: EPROMs are typically programmed by accumulating electrons on a floating gate which changes the control gate voltage necessary to turn on the memory cell. Any leakage path through the surrounding oxides can drain off the electron charge and cause the cell to be marginal or to fail. This failure mode is not present in a ROM, which is typically programmed by implanting dopant ions into the channel region of the memory cell (which changes the gate voltage necessary to turn on the memory cell). The dopant ions are trapped in the silicon and are virtually immobile except at temperatures above approximately 900°C.

EPROM Replacements

"Best" EPROM to be replaced[5]			Gould Semiconductor ROM			Specify these Control options to replace EPROM:						Other parameter comparison (√ = ROM is better or equal)				
						Pin Number						V_{CC}	V_{IN}			
Device[6] Number	Access time (ns)	Power (mA) ICC/ISB/ISB_{CMOS}	Device[6] Number	Access time (ns)	Power (mA) ICC/ISB/ISB_{CMOS}	18	20	21	22	26	27	10%	I_{LEAK}	V_{OUT}	I_{OUT}	T_AOE
2716[1]	350	100/25	S68A316[1,2]	350	80/-	CS/	CS/	DC	—	—	—	5%	√	√	√[3]	√
				150	20/5/0.1	CE/	CS/	DC	—	—	—	√	√	√	√	√
2532[1]	450	150/30	S68A322[1,2]	350	70/-	—	CS/	DC	—	—	—	5%	√	√	√[3]	√
				150	20/5/0.1	—	CS/	DC	—	—	—	√	√	√	√	√
2732[1]	350	150/30	S2333[1]	200	70/15	CE/	CS/	—	—	—	—	√	√	√	√[3]	√
			S6333	150	20/5/0.1	CE/	CS/	—	—	—	—	√	√	√	√	√
2764[1]	150	80/20	S2364	200	90[4]/15	—	CE/	—	OE/	DC	CS	√	√	√	√[3]	√
27C64	200	30/1/0.1	S6364	150	20/5/0.1	—	CE/	—	OE/	DC	CS	√	√	√	√	√
27128[1]	150	100/30	S23128	200	80/20	—	CE/	—	OE/	—	CS	√	√	√	√[3]	√
27256[1]	150	100/30	S23256	200	80/20	—	CE/	—	OE/	—	—	√	√	√	√[3]	100ns
27C256[1]	120	30/1/0.1	S63256	120	40/2/0.1	—	CE/	—	OE/	—	—	√	√	√	√	√
27C512	150	30/1/0.1	S63512	150	50/2/0.15	—	CE/	—	OE/	—	—	√	√	√	√	√

1. Typically tested at 5% V_{CC}, a 10% V_{CC} screened part is available in some cases. Gould Semiconductor ROMs 64K and larger are specified at 10% V_{CC} tolerance.
2. These two Gould Semiconductor NMOS ROMs do not provide powerdown operation. However, the CMOS versions do.
3. Gould Semiconductor specification is I_{OL} = 3.2mA, I_{OH} = −220µA, a typical I_{OH} is greater than −800µA.
4. The typical I_{CC} value is less than 40mA over a temperature range of 0–70°C.
5. The "best" EPROM specifications come from many catalogs. No single EPROM may meet all these listed specifications simultaneously. Because the device specifications frequently change, the information provided here should be considered representative. The intent is to show performance similarity, and to provide control pin options for replacement compatibility.
6. The NMOS version of each device type is listed first, the CMOS version is second.

Notes:
—Optional Gould Semiconductor ROM test limits to match a particular EPROM can be specified.
—Gould Semiconductor nomenclature for an output control pin which provides powerdown operation is "CE". An output control pin which does not provide powerdown is "CS" or "OE". These functions, along with polarity, are programmable.

Application Note

Specific Ordering Information

1. Choose the appropriate Gould Semiconductor part number.
2. Specify speed and chip select, chip enable information.

———or———

1, 2. Specify which EPROM is to be replaced (part number and speed).

———then———

3. Specify marking:

Gould logo, date code
line 1, 13 characters max
line 2, 13 characters max

4. Supply one programmed and one blank, EPROM, Gould Semiconductor will read your code and burn it into the blank. It will then be returned along with a form showing exactly what was ordered, for your approval.

Conclusion

Gould Semiconductor late mask ROMs provide the same or better direct replacement for EPROMs in debugged, volume applications. The cost is substantially less, for mid to high volumes.

GOULD

AMI Semiconductors

General Information

Quality Program

Introduction

The most important activities in maintaining quality are controlling and monitoring through the effective use of Quality Improvement, Quality Assurance, Manufacturing Quality Control, Reliability, Failure Analysis, and Corrective Action. Controlling and monitoring assure a consistently good, reliable product that can be manufactured and delivered with predictable consistency.

The Quality Program is based on MIL-Q-9858 and MIL-M-38510, using statistical methods to regulate all aspects of the design and manufacture of Gould AMI products.

Committed to Quality through SPC

Statistical Process Control (SPC), a scientific method of collecting, analyzing, responding, and continually improving processes, is a culture at Gould AMI. Gould AMI's SPC program, begun in 1981, is the oldest among U.S. semiconductor manufacturers. Customers therefore benefit from years of accumulated knowledge in quality control. The SPC system provides continuous feedback, drawing attention to problems and focusing resources on collective problem solving to create solutions.

Quality Improvement

The Quality Improvement Department is responsible for training in the Quality Improvement Process throughout Gould AMI, including but not limited to the use of SPC and experimental design. Training includes the philosophy of constant improvement and control chart concepts, as well as statistical classes in Regression Analysis and Design of Experiments.

The classes are designed to approach problem solving in a logical progression using more sophisticated tools with each phase of the process. The definition of process is given to be any task that has an input from some source and an output going to a customer. Beginning with process flow charts, the analytic tools are explained with emphasis on practical application, using actual data whenever possible.

Quality Assurance

There are two functions within the scope of Quality Assurance (QA), QA Operations and QA Engineering. These areas are involved in checking the ability of manufactured parts to meet specific limits. QA audits all internal product specifications and procedures to assure that they conform to customer specifications or Gould AMI requirements, whichever are more stringent.

QA Operations checks all phases of the manufacturing process, including incoming material, to insure adherence to specifications and procedures through the use of audits, inspections, and other monitoring techniques. In conjunction with audits, QA Operations administers the Customers Returns and Corrective Action systems.

The Customer Return System documents quality system failures which result in returned product. This aids in elimination of the causes for such failures, with the long range purpose of eliminating returned products completely. A Corrective Action Request is initiated after the cause for the return has been identified.

The Corrective Action System addresses quality system failures to insure appropriate corrective action is taken to preclude subsequent failures. QA Operations follows up on each Corrective Action Request to insure the proper resolution is attained.

QA Engineering provides the technical expertise for QA Operations in addition to assuring that design and manufacturing processes and documents are consistent with company standards and customer requirements. QA Engineering is also responsible for determining the significance of product and process configuration changes as they pertain to customer requirements.

Manufacturing Quality Control

Manufacturing Quality Control (MQC) is principally comprised of Fabrication QC and Test QC. Fabrication QC is not a formal organization, rather an integral part of Fabrication. Having these quality activities reporting to

Quality Program

Manufacturing reinforces the concept of individual responsibility for quality.

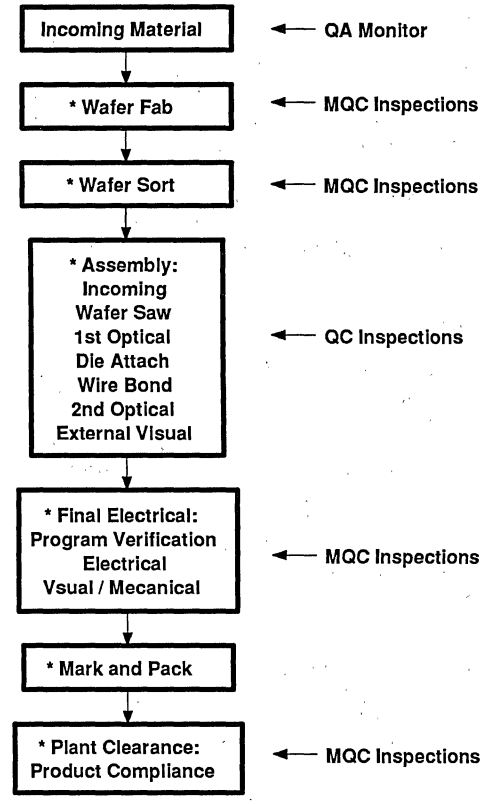
Fabrication QC makes extensive use of SPC via the Shewart control charts maintained at each major step of the fabrication process on one or more measured variables. Equipment and test wafers are measured as well as the actual product in evaluating the results of operations.

Test QC performs internal and customer specified Lot Acceptance Testing (LAT) after Production screening and/or environmental processing. Lots are defined, sample sizes are determined, and using the product specifications, the type of tests to be performed and equipment to be used are determined. In lieu of specifying a particular AQL for lot acceptance of standard products, Test QC strives to reduce defects through continual improvement using SPC and other process control methods.

All lots go through Plant Clearance where a final inspection for visual/mechanical criteria and all supporting documentation for the lot is verified (including LAT sheets, special customer specifications, certificates of compliance, etc.). The material is packed and sent to the customer immediately after acceptance for "Just In Time" delivery.

If a lot is rejected, analysis is done on the rejected unit(s) to determine the cause(s). If the failure was due to inadequate screening, it is returned for 100% rescreening, identified as a resubmission, and LAT is again performed, but to a tighter sampling plan. If the resubmitted lot fails, an engineering review is done to ensure proper corrective action is taken before submitting for the third time. No further submissions are allowed beyond the third without a detailed analysis and correction of the root cause.

Gould AMI Standard Product Flow



*** All manufacturing operations are audited by QA.**

Reliability

The Reliability Department is responsible for demonstrating the dependability of Gould AMI products. Reliability is assured through the evaluation of processes, devices, and packages to establish that they are capable of meeting both the Gould AMI internal requirements and any special customer requirements.

Reliability analyses are performed on a routine basis to observe the degree of control in the manufacturing processes. This is accomplished by the testing of parts in numerous environments, e.g. temperature cycling, vibration, constant acceleration, autoclave, etc..

Quality Program

All aspects of new processes or process changes are monitored and analyzed to determine what the final effect is on product reliability. Qualifications are performed to establish the capability of any significant configuration changes. Reports are distributed, when appropriate, on the results of such analyses.

Failure Analysis

The Failure Analysis (FA) organization provides physics of failure investigations. Results are supplied to Manufacturing to continually improve quality and reliability. Complete analysis of failures from life, tests, environmental tests, field applications, and critical factory applications are routinely provided by the department.

The FA laboratory is equipped to do post mortem examinations of failed devices employing, as required, electrical measurements and many advanced analytical techniques of physics, metallurgy, chemistry, and electronics in order to verify, identify, and characterize the mechanisms of failure. The analysis procedure produces documented evidence to support the conclusions of the cause of failure.

Corrective Action System

While Gould AMI strives for prevention of errors, Corrective Action is occasionally required. There are many sources of information which can generate corrective action including customer returns, receiving inspection records, Failure Analysis reports, process audit reports, and final lot acceptance inspection records.

Each Corrective Action Request will clearly state the quality system failure along with the specific product or material lot/run numbers, the date of discovery of the failure, and the expected result of corrective action. Records of all requests are maintained and followed up to ensure against recurrence of deficiencies.

GOULD

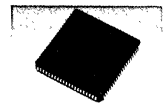
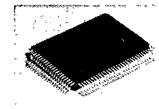
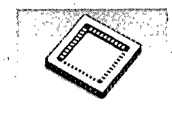
AMI Semiconductors

Package Availability / Testability

Gould AMI, a semiconductor industry leader in ASIC, offers you space-saving and cost-efficient packages and package processes spanning a broad spectrum of capabilities.

We can meet your package requirements in a variety of ways. You can choose from eight basic package types, including advanced technologies such as plastic and ceramic chip carriers, small outline ICs and pin grid arrays, with up to 180 lead test handling capability.

SURFACE MOUNT PACKAGES

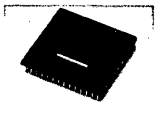
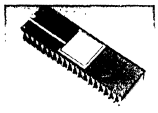
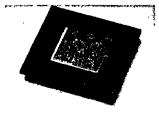
	PLASTIC					CERAMIC	
							
PACKAGE TYPE	LEADED CHIP CARRIER (PLCC)	SMALL OUTLINE INTEGRATED CIRCUIT (SOIC)	QUAD FLATPACK (QFP)			LEADLESS CHIP CARRIER (CLCC)	
LEAD SHAPE	J	Gullwing	Gullwing			Pad	
LEAD ℄ - ℄	50 mils	50 mils	1mm	.8mm	.65mm	50 mils	40 mils
LEADS:							
16		A					
20	A					B	
24						A	
28	A	A				B	
32	A						
40							A
44	A					B	
48							A
52						B	
64			A				
68	A					B	
80				A			
84	A					B	
100					A		
120				A			
128				A			
144				A			
160					A		
MATERIAL COST	Low	Low	Intermediate			High	High
BOARD DENSITY (I/O's per sq. in.)	High	High	Highest			High	High
THERMAL DISSIPATION	Good	Fair	Fair			Inter-mediate	Inter-mediate
RELIABILITY	Good	Fair	Good			Best	Best

GOULD

AMI Semiconductors

Package Availability / Testability

THROUGH-HOLE PACKAGES

	PLASTIC		CERAMIC	
				
PACKAGE TYPE	DUAL-IN-LINE (P-DIP)	PIN GRID ARRAY (PPGA)	SIDE BRAZE	PIN GRID ARRAY (CPGA)
LEAD SHAPE	Lead	Pin	Lead	Pin
LEAD ℄ - ℄	100 mils	100 mils	100 mils	100 mils
LEADCOUNT:				
8	A			
14	A		A	
16	A		A	
18	A		A	
20	A		A	
22	A		A	
24	*A		A	
28	A		A	
32	A			
40	A		A	
48	A		A	
68		A		A
84		A		A
100		A		A
108		A		
120		A		A
132		A		
144		A		A
180		A		
MATERIAL COST	Lowest	High	High	Highest
BOARD DENSITY (I/O's per sq. in.)	Low	High	Low	High
THERMAL DISSIPATION	Fair	Good	Very Good	Best
RELIABILITY	Good	Fair	Best	Best

* Skinny body width (.300 inches) also available

Legend:
A. Test -50°C to 150°C
B. Test -50°C to 150°C (leaded version available)

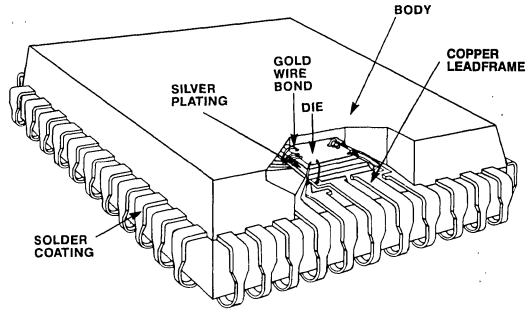
GENERAL INFORMATION

Package Description

Plastic Leaded Chip Carrier (PLCC)

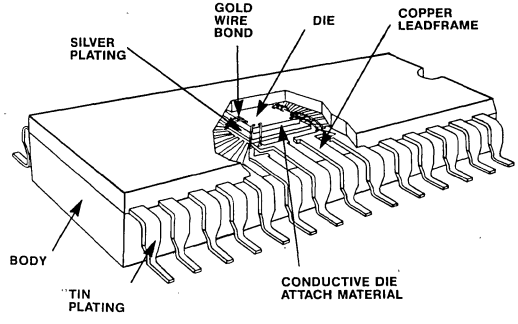
For gate arrays, standard cell designs and custom ICs, our PLCC meets your need for a quality surface-mount quad package to support complex integrated circuits requiring high lead counts. An added benefit is the PLCC's J-form leads which make it ideal for easy handling and shipping.

The PLCC is transfer molded and thermosonically wire bonded. Die are mounted on a copper leadframe and external leads are wave soldered to provide improved solderability required for vapor phase reflow application.



Small Outline Integrated Circuit (SOIC)

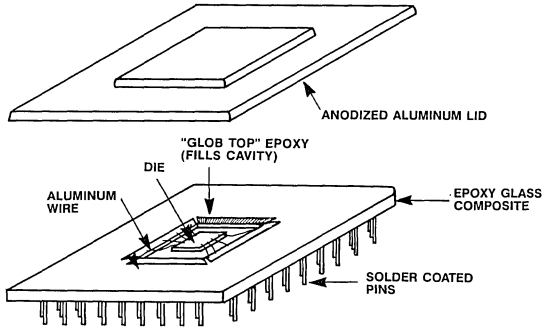
Our SOIC package is the smallest dual-in-line package available, and is an excellent choice for maximum board density. It can be surface mounted on your printed circuit board and is ideal for the automotive, telecommunications and computer industries, or any industry that requires dense placement of chips on boards.



Package Description

Plastic Pin Grid Array (PPGA)

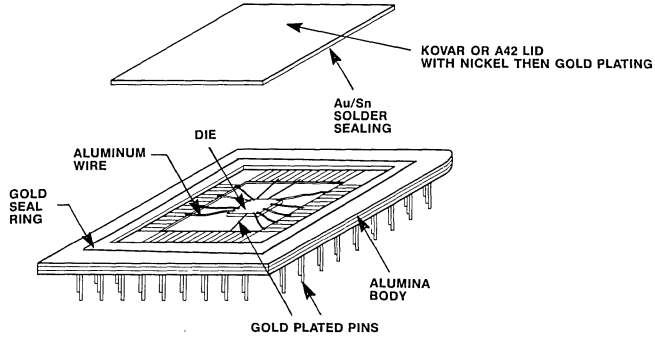
The PPGA is a lower cost alternative to the Ceramic Pin Grid Array if high reliability is not required. The body is an epoxy glass composite with a gold plated cavity. The pins are soldered in place (not force fit) and have a tin lead (90/10) solder finish. The seal is an epoxy "glob top" beneath a black anodized aluminum lid.



Ceramic Pin Grid Array (CPGA)

The CPGA is a through-hole mount package for high density packaging with very high pin counts. The lead design also makes it compatible with socket insertion mounting.

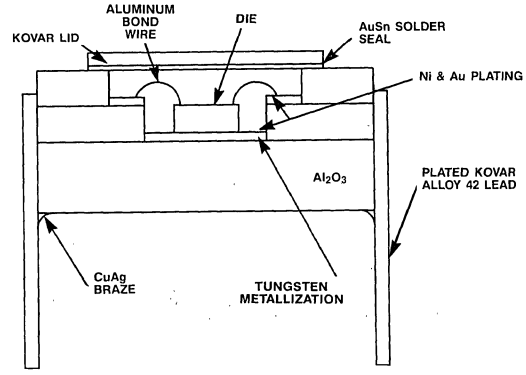
The CPGAs are built on the same concept as the ceramic side brazed packages and are designed for high reliability applications. They have an Al_2O_3 ceramic body, gold plating on the pins and die cavity, and are sealed with a Kovar/alloy 42 lid with gold-tin eutectic solder.



Package Description

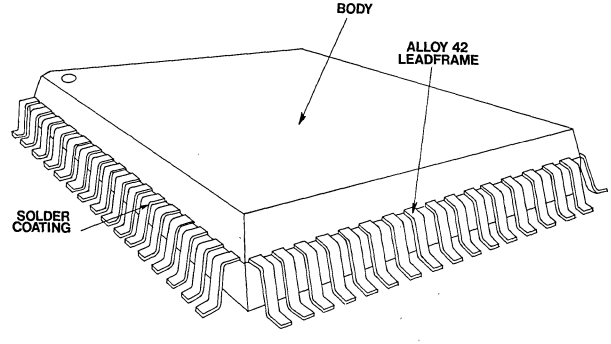
Ceramic Side Braze

The ceramic side braze is an industry standard high performance, high reliability package, made of three layers of Al_2O_3 ceramic and Tungsten refractory metal. A gold tin eutectic sealed Kovar lid is used to form the hermetic cavity of this package. Package leads are available with gold or tin plating covered with 200 microinches of Sn/Pb 60/40 solder.



Quad Flatpack (QFP)

Quad flatpack is a high-density, low-cost plastic package for high leadcount applications. It uses a smaller lead-to-lead spacing than the PLCC, has gull-wing leads bent outward on all four sides which permits better inspection of solder joints, solder-plated external leads. The package is registered with the Electronics Industry Association of Japan. QFPs are assembled with the latest technology of low stress die-attach material and molding compound and exhibit better reliability.



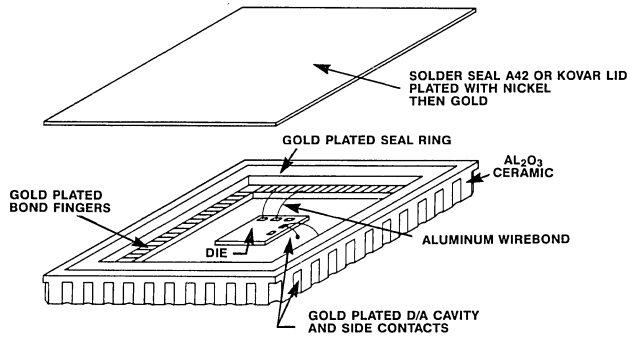
Package Description

Ceramic Leadless Chip Carrier (CLCC)

Built on the same concept as the highly reliable sidebraze ceramic package, the CLCC is made of three layers of Al_2O_3 ceramic, refractory metallization, gold over nickel plating, and contact pads equally spaced on all four sides of the carrier.

The package comes with a gold tin eutectic sealed metal lid creating a hermetic cavity.

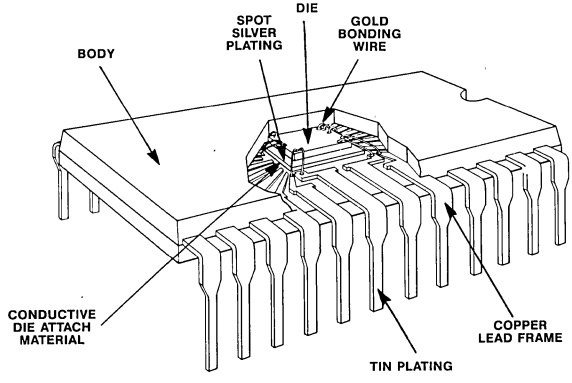
(All Type C except 68 lead where both Type B and Type C are available.)



Plastic Dual-In-Line Package (PDIP)

The Gould AMI PDIP package is the equivalent of the widely accepted industry standard, refined by Gould AMI for MOS/VLSI applications. The package consists of a plastic body, transfer-molded around the leadframe and die. The leadframe is copper alloy, with external pins tin plated. Internally, there is 150μ in silver spot plating on the die attach pad and on each bonding fingertip. These fingers are electrically connected to the die by thermosonic gold ball bonding techniques.

During manufacture every critical step of the process is statistically monitored and controlled to assure maximum quality.



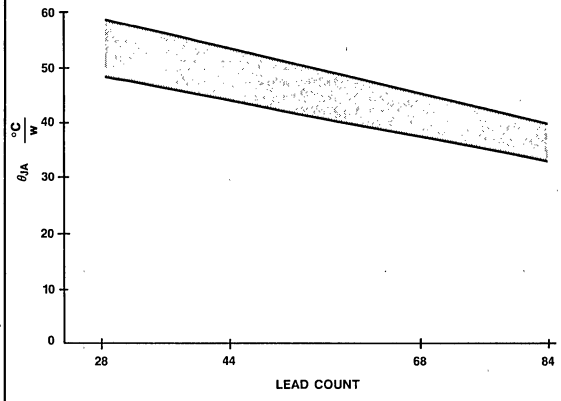
Package Thermal Resistance

The ability of the package to conduct heat from the device to the environment is measured by thermal resistance. This thermal resistance is calculated from the temperature difference between the die junction and the surrounding ambient air environment (θ_{JA}).

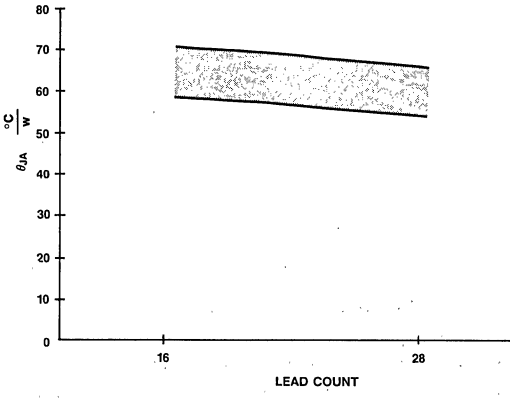
θ_{JA} data is based on a still-air environment where the device is mounted in a package and the package mounted on a board. The graph ranges reflect deviations in package parameters within a lead count such as, but not limited to die size, die attach pad size, etc. Chart values are given as a guideline. Thermal resistance from junction to case (θ_{JC}) is typically better than junction to ambient. Use θ_{JA} for worst case condition.

Surface-Mount Package Thermal Resistance

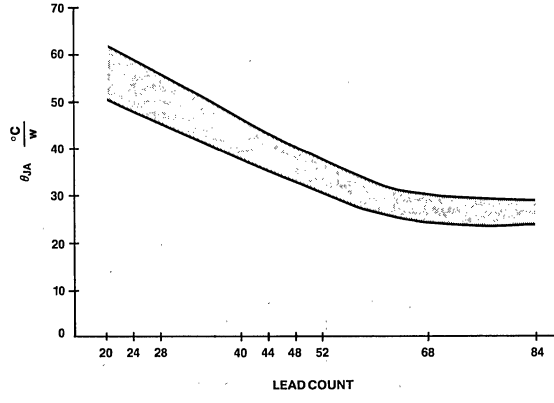
PLASTIC CHIP CARRIERS



PLASTIC SMALL OUTLINE I.C.



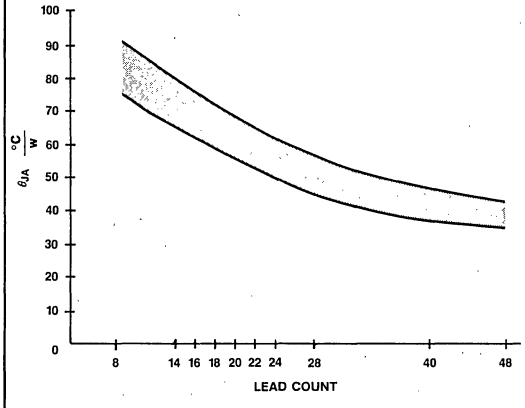
CERAMIC LEADLESS CHIP CARRIER



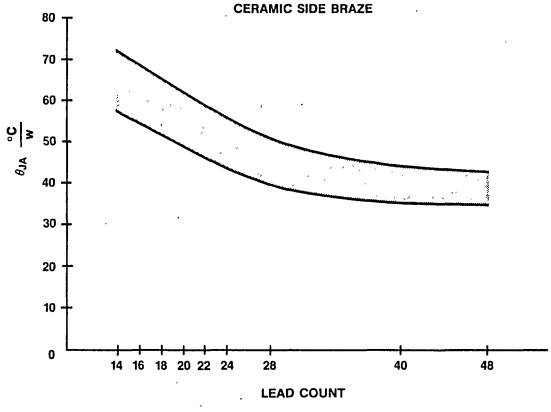
Package Thermal Resistance

Through-Hole Package Thermal Resistance

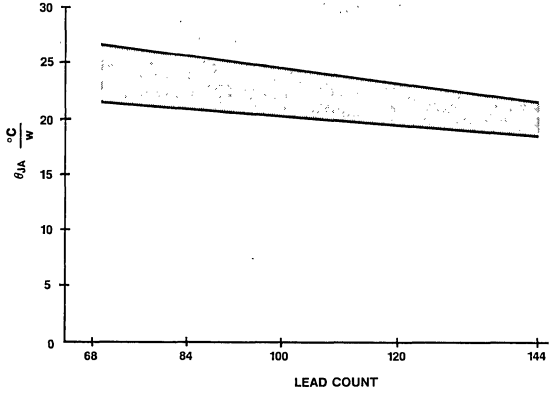
PLASTIC DUAL-IN-LINE



CERAMIC SIDE BRAZE



CERAMIC PIN GRID ARRAY



GENERAL INFORMATION

Quality / Reliability

Product Assurance

To assure a high level of reliability, Gould AMI uses a wide variety of tests that are performed on a routine basis as part of the Product Assurance program. This includes the use of industry standard environmental stress tests so that the data is directly comparable to that of Gould AMI's competitors.

Operating Life Test

Operating life testing is predicated on accelerating the failure mechanisms that could cause devices to fail in use by operating the devices at elevated temperatures. Typically, this is for a period of 1,000 hours of operation at 125° C. With proper device designs, those conditions affect failures due to latent defects and do not affect failures due to the fundamental physical limitations of the materials used to make the devices.

Temperature Humidity Bias (THB)

THB is a test for plastic packaged devices and is predicated on corrosion of the die metallization being the primary failure mechanism. Thus, in a sense THB appraises the degree of hermeticity achieved by a molded plastic package. Typically this test is performed for a period of 1,000 hours at conditions of 85° C and 85 ± 5% relative humidity with bias. The bias applied to all pins is D.C. and is such that the device is set in a configuration of minimal power dissipation with the full D.C. bias stress set between adjacent package pins. This will affect galvanic corrosion of the die metallization if applicable soluble electrolytes exist at the die or along a moisture penetration path.

Temperature Cycle Test

Temperature cycling evaluates the thermal compatibility of the variety of materials which make up a device. There are differing coefficients of thermal expansion between ceramic packages and metal lids, between the molding compound of a plastic package and the leadframe, and even between the metallization and glasses of the die itself, to name a few. Typically, temperature cycling is performed for 1,000 cycles from an ambient of -65° C to an ambient of 150° C and back to -65° C.

Thermal Shock Test

The intents of thermal shock testing are the same as temperature cycling except that liquid media instead of gaseous media are employed. Consequently there is a much more rapid thermal transfer than in temperature cycling. This may or may not produce longer thermal gradients within the device, depending upon the differences in the thermal conductivities and thermal capacities of the device materials.

Autoclave or Pressure Cooker Test (PCT)

PCT is another standard test of plastic packaged devices. Like THB, it is predicated on inducing corrosion of the die metallization, but without any electrical bias under the saturated steam conditions of 121° C, 100% relative humidity. The effects of increased temperature and relative humidity tend to make PCT an acceleration of THB. But this is opposed by the absence of a bias voltage in PCT which effectively decreases the reaction rate of the die metallization to electrolytes dissolved in water absorbed by the package. Nevertheless, PCT is often used interchangeably with THB throughout the industry, particularly when the costs of the device sockets and bias boards necessary for THB are prohibitive.

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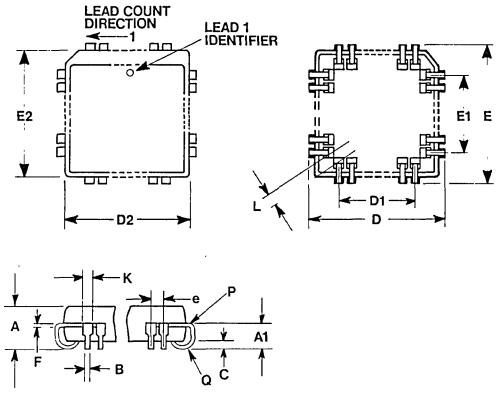
Package Outline Dimensions

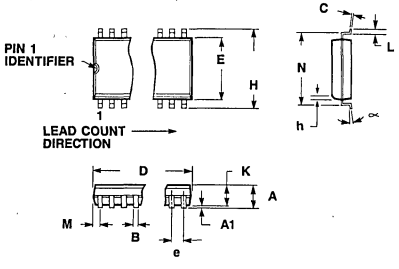
PLCC Outline



	LEAD COUNT											
	20		28		32		44		68		84	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.165	.180	.155	.175	.123	.140	.155	.175	1.65	.175	.165	.175
A1	.100	.110	.098	.105	078	.095	.098	.104	097	.103	.097	.103
B	.013	.021	.015	.21	.013	.021	.016	.024	.016	.024	.016	.024
C	.015	.025	.017	.027	.017	.027	.017	.037	.017	.027	.017	.027
D	.385	.395	.482	.502	.549	.553	.680	.704	.976	1.000	1.170	1.200
E	.385	.395	.482	.502	.585	.595	.680	.704	.976	1.000	1.170	1.200
D1	.195	.205	.295	.305	.300	REF	.495	.505	.795	805	.995	1.005
E1	.195	.205	.295	.305	.400	REF	.495	.505	.795	805	.995	1.005
D2	.350	.354	.440	.460	.390	.430	.640	.660	.940	.960	1.940	1.160
E2	.350	.354	.440	.460	.449	.453	.640	.660	.940	.960	1.140	1.160
e	.047	.053	.047	.053	.047	.053	.047	.053	.047	.053	.047	.053
F	0097	012	.010	012	010	.012	.010	012	.008	.012	.008	.012
K	.027	.033	.025	.031	026	.032	.026	.034	.026	.034	.026	.034
L	.005	—	.005	—	.005	—	.005	—	.005	—	.005	—
P	.009	TYP	.009	TYP	.009	TYP	.009	TYP	009	TYP	.009	TYP
Q	.020	TYP	.021	TYP	.021	TYP	.021	TYP	.023	TYP	.023	TYP

(Dimensions in Inches)

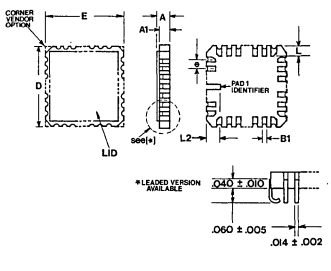
SOIC Outline



	LEAD COUNT			
	16		28	
SYMBOL	MIN	MAX	MIN	MAX
A	.099	.104	.099	.104
A1	.004	.009	.004	.009
B	014	.019	.014	.019
C	.010	REF	.010	REF
D	.405	.410	.707	.712
E	.294	.299	.292	.299
e	.050	TYP	.050	TYP
H	.402	.419	.402	419
h	.025 x 45°		.025 x 45°	
L	.030	.040	.030	.040
∝	0°	8°	0°	8°
K	.088	.098	.088	.098
M	.020	.030	.020	.030
N	.335	351	.335	.351

(Dimensions in Inches)

CLCC Outline



	LEAD COUNT																	
	20*		24*		28*		40		44*		48		52*		68*		84*	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.067	.087	069	.085	.067	.087	.067	087	.067	.087	.067	.087	.069	.085	.087	.107	.087	.107
A1	.055	.075	058	.072	.055	.075	.055	.075	.055	.075	.055	.075	.058	.072	.077	.093	.077	.093
B1	.020	.030	.015	.025	.020	.030	.015	.025	.020	.030	.017	.023	.020	.030	.020	.030	.020	.030
D / E	.345	.360	.395	.410	.445	.460	.475 .390	.490 .410	.643 .495	.662 .510	554	572	.735	.765	.940	.962	1.138	1.167
e	.050	BSC	.050	BSC	.050	BSC	.040	BSC	.050	BSC	.040	BSC	.050	BSC	050	BSC	.050	BSC
L	.042	.058	030	.040	045	.055	035	055	.042	.058	033	.047	.042	058	.042	.058	.042	.058
L2	.075	.095	090	.110	.075	.095	095	.105	075	.095	078	.092	.042	058	075	.095	078	.093

(Dimensions in Inches)

GENERAL INFORMATION

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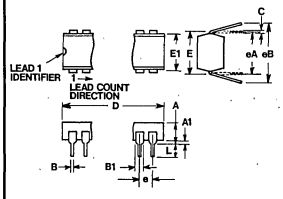
Package Outline Dimensions

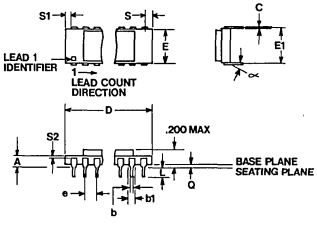
PDIP Outline



	LEAD COUNT																			
	8		14		16		18		20		22		24		24		28		40		48	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.155	.160	.195	.200	.195	.200	.195	.200	.195	.200	.195	.200	.195	.200	130	.160	.195	200	.195	.200	.195	200
A1	.015	—	015	—	.015	—	015	—	015	—	015	—	015	—	015	—	.015	—	.015	—	015	—
B	018	.022	015	.022	015	020	015	.020	.015	020	.015	020	.015	020	015	020	.015	020	015	020	015	020
B1	050	070	050	070	050	070	050	.070	050	070	050	070	050	070	040	065	050	.070	040	060	040	060
C	008	.012	008	012	008	012	008	012	008	012	008	012	008	012	008	012	008	.012	008	012	008	012
D	348	390	725	790	745	790	845	930	925	1030	1050	1.120	1125	1.270	1.235	1.265	1380	1.470	1980	2.065	2 455	2 460
E	290	310	290	310	290	310	290	310	290	310	380	410	580	610	290	330	580	610	580	610	580	610
E1	220	270	220	270	220	280	220	270	230	280	330	370	520	560	240	260	520	560	520	560	520	560
e	100	TYP	100	TYP	100	TYP	100	TYP	100	TYP	100	TYP	100	TYP	100	TYP	100	TYP	100	TYP	100	TYP
eA	290	—	290	—	290	—	290	—	290	—	380	—	580	—	290	—	580	—	580	—	580	—
eB	—	310	—	310	—	310	—	310	—	310	—	526	—	610	—	330	—	610	—	610	—	610
L	100	—	100	—	100	—	100	—	100	—	100	—	100	—	100	—	100	—	100	—	100	—

(Dimensions in inches)

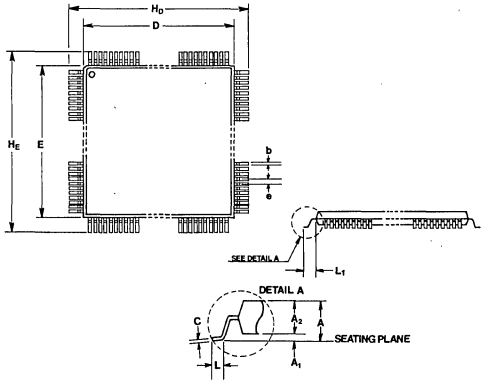
Ceramic Side Braze Outline



	LEAD COUNT																			
	14		.16		18		20		22		24		28		40		48			
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
A	—	.180	—	.180	—	.180	—	.180	—	.180	—	.180	—	.180	—	.180	—	.180		
b	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020		
b1	.040	.065	.040	.065	.040	.065	.040	.065	.040	.065	.040	.065	.040	.065	.040	.065	.040	.065		
c	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012		
D	—	.720	—	.810	—	.920	—	1.060	—	1.111	—	1.290	—	1.490	—	2.060	—	2.434		
E	.275	.305	.275	305	.275	.305	.220	.310	.375	.405	.575	.605	.575	605	.575	605	.575	.605		
E1	.290	.315	.290	.315	.290	.315	.290	.320	.390	.415	.590	.615	.590	.615	.590	.615	.590	.615		
e	.100	TYP	.100	TYP	.100	TYP	.100	TYP	.100	TYP	.100	TYP	.100	TYP	.100	TYP	.100	TYP		
L	.125	.200	.125	.200	.125	.200	.125	.200	.125	.200	.125	.200	.125	.200	.125	.200	.125	.200		
Q	.020	.060	.020	.060	.020	.070	.020	.070	.020	.070	.020	.075	.020	.060	.020	.070	.020	.060		
S	—	098	—	.080	—	.098	—	.080	—	.080	—	.098	—	.100	—	.098	—	.100		
S1	.005	—	.005	—	.005	—	.005	—	.005	—	.005	—	.005	—	.005	—	.005	—		
S2	.005	—	.005	—	.005	—	.005	—	.005	—	.005	—	.005	—	.005	—	.005	—		
∝	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°		

(Dimensions in inches)

QFP Outline

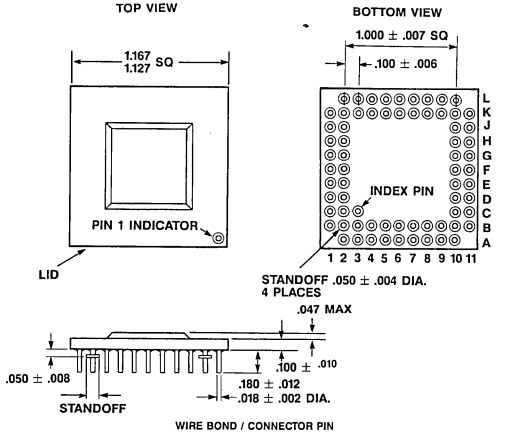


	LEAD COUNT																			
	64		80		100		120		128		144		160							
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX						
A	2.75	3.00	2.75	3.00	2.75	3.00	3.54	3.89	3.54	3.89	3.54	3.89	3.54	3.89						
A1	0.15	0.30	0.15	0.30	0.15	0.30	0.15	0.30	0.15	0.30	0.15	0.30	0.15	0.30						
A2	2.60	2.80	2.60	2.80	2.60	2.80	3.39	3.59	3.39	3.59	3.39	3.59	3.39	3.59						
b	0.36	0.46	0.36	0.46	0.30	0.40	0.31	0.40	0.31	0.40	0.25	0.40	0.25	0.40						
C	0.13	0.20	0.13	0.20	0.13	0.20	0.13	0.20	0.13	0.20	0.13	0.20	0.13	0.20						
D	13.62	14.12	1362	14.12	1362	14.12	27.61	28.11	27.61	28.11	27.61	28.11	27.61	28.11						
E	1962	20.12	1962	20.12	1962	20.12	27.61	28.11	27.61	28.11	27.61	28.11	27.61	28.11						
e	1.00	TYP	0.80	TYP	0.65	.TYP	0.80	TYP	0.80	TYP	0.65	TYP	0.65	TYP						
HD	23.77	24.03	23.77	24.03	23.77	24.03	31.87	32.13	31.87	32.13	31.87	32.13	31.87	32.13						
HE	17.77	18.03	17.77	18.03	17.77	18.03	31.87	32.13	31.87	32.13	31.87	32.13	31.87	32.13						
L	0.70	0.90	0.70	0.90	0.70	0.90	0.70	0.90	0.70	0.90	0.70	0.90	0.70	0.90						
L1	2.015	REF	2.015	REF	2.015	REF	2.015	REF	2.015	REF	2.015	REF	2.015	REF						

(Dimensions in Millimeters)

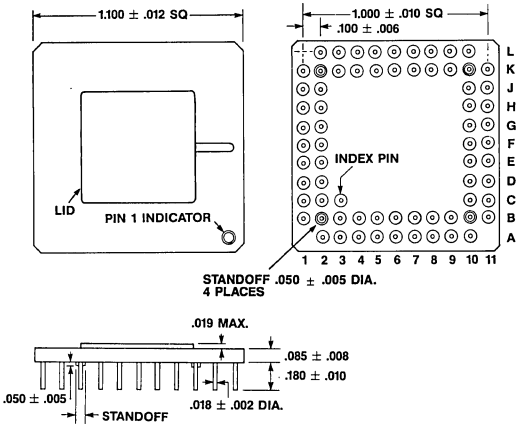
Package Outline Dimensions

68-Pin PPGA Outline

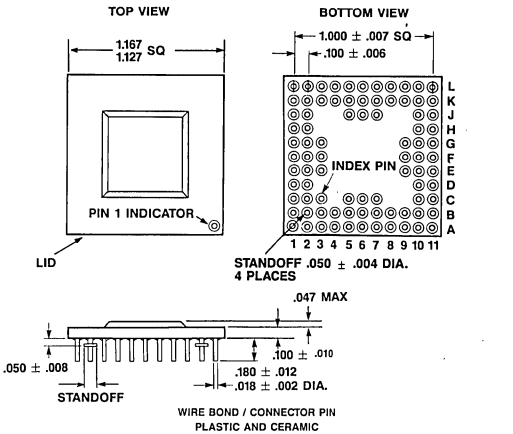


PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO
1	B2	18	K2	35	K10	52	B10
2	B1	19	L2	36	K11	53	A10
3	C2	20	K3	37	K10	54	B9
4	C1	21	L3	38	K11	55	A9
5	D2	22	K4	39	H10	56	B8
6	D1	23	L4	40	H11	57	A8
7	E2	24	K5	41	G10	58	B7
8	E1	25	L5	42	G11	59	A7
9	F2	26	K6	43	F10	60	B6
10	F1	27	L6	44	F11	61	A6
11	G2	28	K7	45	E10	62	B5
12	G1	29	L7	46	E11	63	A5
13	H2	30	K8	47	D10	64	B4
14	H1	31	L8	48	D11	65	A4
15	J2	32	K9	49	C10	66	B3
16	J1	33	L9	50	C11	67	A3
17	K1	34	L10	51	B11	68	A2

68-Pin CPGA Outline

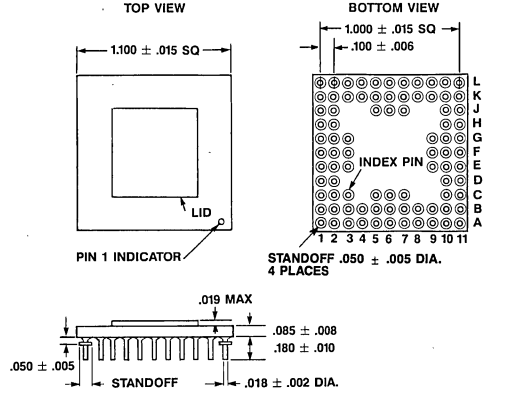


84-Pin PPGA Outline



PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO
1	B2	22	K2	43	K10	64	B10
2	C2	23	K3	44	J10	65	B9
3	B1	24	L2	45	K11	66	A10
4	C1	25	L3	46	J11	67	A9
5	D2	26	K4	47	H10	68	B8
6	D1	27	L4	48	H11	69	A8
7	E3	28	J5	49	F10	70	B6
8	E2	29	K5	50	G10	71	B7
9	E1	30	L5	51	G11	72	A7
10	F2	31	K6	52	G9	73	B7
11	F3	32	J6	53	F9	74	C6
12	G3	33	J7	54	F11	75	A6
13	G1	34	L7	55	E11	76	A5
14	G2	35	K7	56	E10	77	B5
15	F1	36	L6	57	E9	78	C5
16	H1	37	L8	58	D11	79	A4
17	H2	38	K8	59	D10	80	B4
18	J1	39	L9	60	C11	81	A3
19	K1	40	L10	61	B11	82	A2
20	J2	41	K9	62	C10	83	B3
21	L1	42	L11	63	A11	84	A1

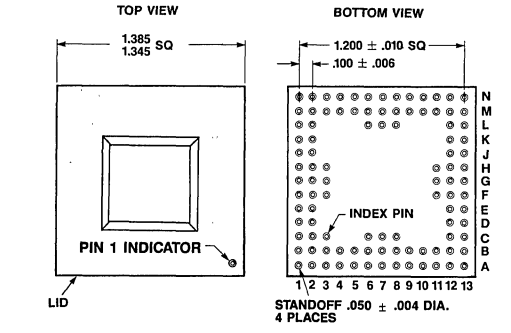
84-Pin CPGA Outline



GENERAL INFORMATION

Package Outline Dimensions

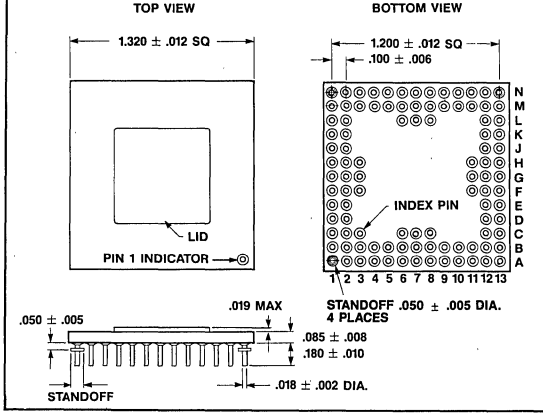
100-Pin PPGA Outline



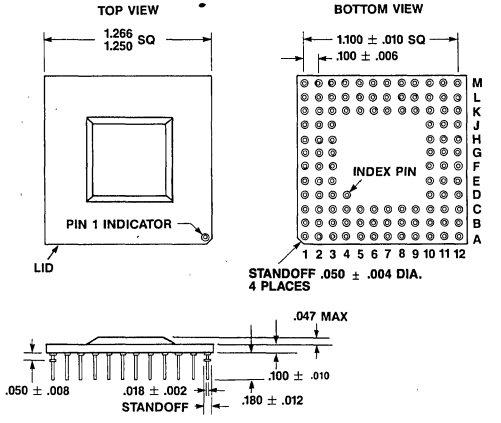
WIRE BOND / CONNECTOR PIN
PLASTIC AND CERAMIC

PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO
1	B2	21	K2	41	M8	61	H13	81	A10
2	B1	22	L1	42	L8	62	G12	82	B9
3	C2	23	M1	43	N9	63	G11	83	A9
4	C1	24	L2	44	M9	64	G13	84	C8
5	D2	25	N1	45	N10	65	F13	85	B8
6	D1	26	M2	46	M10	66	F12	86	A8
7	E2	27	N2	47	N11	67	F11	87	B7
8	E1	28	M3	48	N12	68	E13	88	C7
9	F3	29	N3	49	M11	69	E12	89	A7
10	F2	30	M4	50	N13	70	D13	90	A6
11	F1	31	N4	51	M12	71	D12	91	B6
12	G2	32	M5	52	M13	72	C13	92	C6
13	G3	33	N5	53	L12	73	B13	93	A5
14	G1	34	L6	54	L13	74	C12	94	B5
15	H1	35	M6	55	K12	75	A13	95	A4
16	H2	36	N6	56	K13	76	B12	96	B4
17	H3	37	M7	57	J12	77	A12	97	A3
18	J1	38	L7	58	J13	78	B11	98	A2
19	J2	39	N7	59	H11	79	A11	99	B3
20	K1	40	N8	60	H12	80	B10	100	A1

100-Pin CPGA Outline



108-Pin PPGA Outline

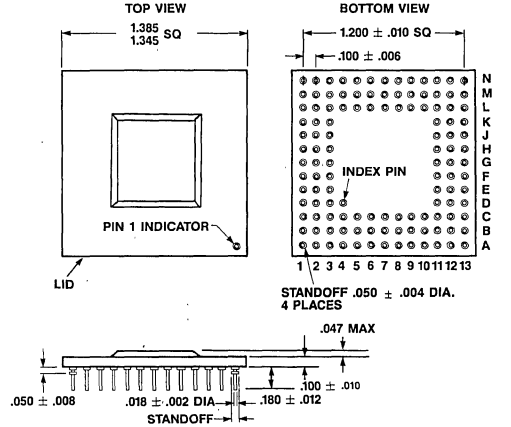


WIRE BOND / CONNECTOR PIN
PLASTIC AND CERAMIC

PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO
1	A1	28	M1	55	M12	82	A12
2	B1	29	M2	56	L12	83	A11
3	D3	30	K4	57	J10	84	C9
4	C2	31	L3	58	K11	85	B10
5	C1	32	M3	59	K12	86	A10
6	D2	33	L4	60	J11	87	B9
7	E3	34	K5	61	H10	88	C8
8	D1	35	M4	62	J12	89	A9
9	E2	36	L5	63	H11	90	B8
10	E1	37	M5	64	H12	91	A8
11	F3	38	K6	65	G10	92	C7
12	F2	39	L6	66	G11	93	B7
13	F1	40	M6	67	G12	94	A7
14	G2	41	L7	68	F11	95	B6
15	G3	42	K7	69	F10	96	C6
16	G1	43	M7	70	F12	97	A6
17	H1	44	M8	71	E12	98	A5
18	H2	45	L8	72	E11	99	B5
19	H3	46	K8	73	E10	100	C5
20	J1	47	M9	74	D12	101	A4
21	J2	48	L9	75	D11	102	B4
22	K1	49	M10	76	C12	103	A3
23	J3	50	K9	77	D10	104	C4
24	K2	51	L10	78	C11	105	B3
25	L1	52	M11	79	B12	106	A2
26	L2	53	L11	80	B11	107	B2
27	K3	54	K10	81	C10	108	C3

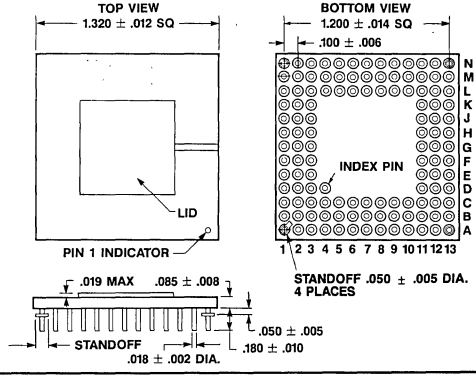
Package Outline Dimensions

120-Pin PPGA Outline

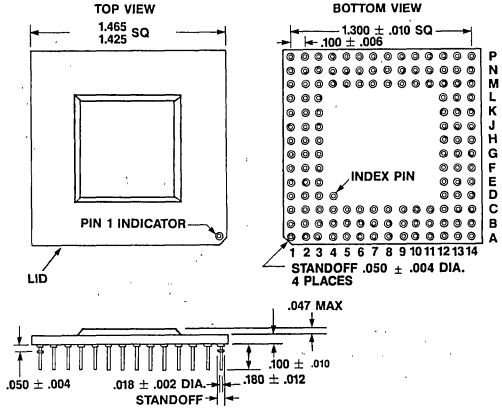


PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO
1	C3	25	K2	49	M8	73	H12	97	B10
2	B2	26	L1	50	L8	74	H13	98	C9
3	B1	27	M1	51	N9	75	G12	99	A10
4	D3	28	K3	52	M9	76	G11	100	B9
5	C2	29	L2	53	N10	77	G13	101	A9
6	C1	30	N1	54	L9	78	F13	102	C8
7	D2	31	L3	55	M10	79	F12	103	B8
8	E3	32	M2	56	N11	80	F11	104	A8
9	D1	33	N2	57	N12	81	E13	105	B7
10	E2	34	L4	58	L10	82	E12	106	C7
11	E1	35	M3	59	M11	83	D13	107	A7
12	F3	36	N3	60	N13	84	E11	108	A6
13	F2	37	M4	61	L11	85	D12	109	B6
14	F1	38	L5	62	M12	86	C13	110	C6
15	G2	39	N4	63	M13	87	B13	111	A5
16	G3	40	M5	64	K11	88	D11	112	B5
17	G1	41	N5	65	L12	89	C12	113	A4
18	H1	42	L6	66	L13	90	A13	114	C5
19	H2	43	M6	67	K12	91	C11	115	B4
20	H3	44	N6	68	J11	92	B12	116	A3
21	J1	45	M7	69	K13	93	A12	117	A2
22	J2	46	L7	70	J12	94	C10	118	C4
23	K1	47	N7	71	J13	95	B11	119	B3
24	J3	48	N8	72	H11	96	A11	120	A1

120-Pin CPGA Outline



132-Pin PPGA Outline



PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO
1	A1	23	K1	45	N6	67	P14	89	E14	111	B9
2	B1	24	K2	46	P6	68	N14	90	E13	112	A9
3	D3	25	L1	47	N7	69	L12	91	D14	113	B8
4	C2	26	K3	48	M7	70	M13	92	E12	114	C8
5	C1	27	L2	49	P7	71	M14	93	D13	115	A8
6	D2	28	M1	50	P8	72	L13	94	C14	116	A7
7	E3	29	M2	51	N8	73	K12	95	C13	117	B7
8	D1	30	L3	52	M8	74	L14	96	D12	118	C7
9	E2	31	N1	53	P9	75	K13	97	B14	119	A6
10	E1	32	N2	54	N9	76	K14	98	B13	120	B6
11	F3	33	M3	55	M9	77	J12	99	C12	121	C6
12	F2	34	P1	56	P10	78	J13	100	A14	122	A5
13	F1	35	P2	57	N10	79	J14	101	A13	123	B5
14	G2	36	M4	58	P11	80	H13	102	C11	124	A4
15	G3	37	N3	59	M10	81	H12	103	B12	125	C5
16	G1	38	P3	60	N11	82	H14	104	A12	126	B4
17	H1	39	N4	61	P12	83	G14	105	B11	127	A3
18	H2	40	M5	62	N12	84	G13	106	C10	128	B3
19	H3	41	P4	63	M11	85	G12	107	A11	129	C4
20	J1	42	N5	64	P13	86	F14	108	B10	130	A2
21	J2	43	P5	65	N13	87	F13	109	A10	131	B2
22	J3	44	M6	66	M12	88	F12	110	C9	132	C3

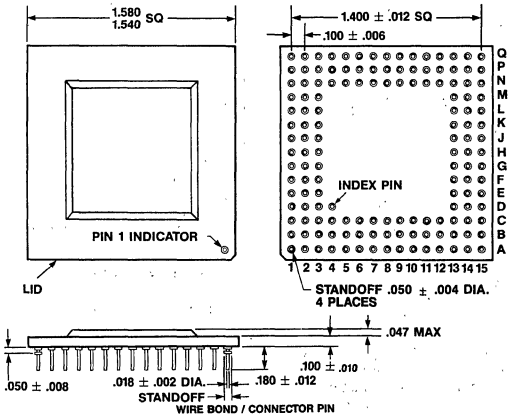
GENERAL INFORMATION

GOULD

AMI Semiconductors

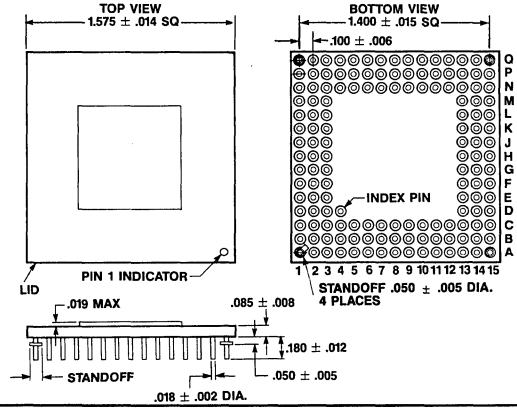
Package Outline Dimensions

144-Pin PPGA Outline

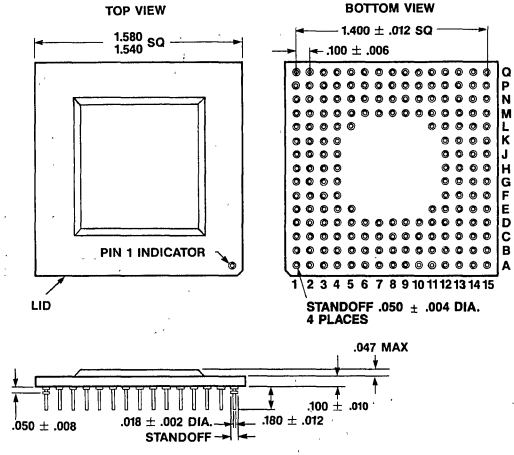


PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO
1	D3	25	L1	49	N7	73	M13	97	E15	121	C9
2	C2	26	L2	50	Q6	74	N14	98	E14	122	A10
3	B1	27	M1	51	Q7	75	P15	99	D15	123	A9
4	D2	28	N1	52	P8	76	M14	100	C15	124	B8
5	E3	29	M2	53	Q8	77	L13	101	D14	125	A8
6	C1	30	L3	54	N8	78	N15	102	E13	126	C8
7	E2	31	N2	55	N9	79	L14	103	C14	127	C7
8	D1	32	P1	56	Q9	80	M15	104	B15	128	A7
9	F3	33	M3	57	Q10	81	K13	105	D13	129	A6
10	F2	34	N3	58	P9	82	K14	106	C13	130	B7
11	E1	35	P2	59	P10	83	L15	107	B14	131	B6
12	G2	36	Q1	60	N10	84	J14	108	A15	132	C6
13	G3	37	N4	61	Q11	85	J13	109	C12	133	A5
14	F1	38	P3	62	P11	86	K15	110	B13	134	B5
15	G1	39	Q2	63	Q12	87	J15	111	A14	135	A4
16	H2	40	P4	64	Q13	88	H14	112	B12	136	A3
17	H1	41	N5	65	P12	89	H15	113	C11	137	B4
18	H3	42	Q3	66	N11	90	H13	114	A13	138	C5
19	J3	43	P5	67	P13	91	G13	115	B11	139	B3
20	J1	44	Q4	68	Q15	92	G15	116	A12	140	A2
21	K1	45	N6	69	N12	93	F15	117	C10	141	C4
22	J2	46	P6	70	N13	94	G14	118	B10	142	C3
23	K2	47	Q5	71	P14	95	F14	119	A11	143	B2
24	K3	48	P7	72	Q15	96	F13	120	B9	144	A1

144-Pin CPGA Outline



180-Pin PPGA Outline



WIRE BOND / CONNECTOR PIN

PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO	PAD NO	PIN NO
1	A1	31	K3	61	M7	91	Q15	121	F13	151	D9
2	C3	32	L1	62	Q6	92	N13	122	E15	152	A10
3	B1	33	L2	63	N7	93	P15	123	E14	153	C9
4	C2	34	K4	64	P7	94	N14	124	F12	154	B9
5	E4	35	M1	65	Q7	95	L12	125	D15	155	A9
6	D3	36	L3	66	N8	96	M13	126	E13	156	C8
7	C1	37	M2	67	M8	97	N15	127	D14	157	D8
8	E3	38	N1	68	P8	98	L13	128	C15	158	B8
9	D2	39	L4	69	Q8	99	M14	129	E12	159	A8
10	F4	40	M3	70	Q9	100	K12	130	D13	160	A7
11	D1	41	N2	71	P9	101	M15	131	C14	161	B7
12	E2	42	P1	72	N9	102	L14	132	B15	162	C7
13	F3	43	P2	73	M9	103	K13	133	B14	163	D7
14	E1	44	M4	74	Q10	104	L15	134	D12	164	A6
15	F2	45	L5	75	P10	105	K14	135	E11	165	B6
16	G4	46	Q1	76	N10	106	J12	136	A15	166	C6
17	F1	47	N3	77	Q11	107	K15	137	C13	167	A5
18	G3	48	Q2	78	P11	108	J13	138	A14	168	B5
19	G2	49	P3	79	M10	109	J14	139	B13	169	D6
20	G1	50	M5	80	Q12	110	J15	140	D11	170	A4
21	H3	51	N4	81	N11	111	H13	141	C12	171	C5
22	H4	52	Q3	82	P12	112	H12	142	A13	172	B4
23	H2	53	N5	83	Q13	113	H14	143	C11	173	A3
24	H1	54	P4	84	M11	114	H15	144	B12	174	D5
25	J1	55	M6	85	N12	115	G15	145	D10	175	C4
26	J2	56	Q4	86	P13	116	G14	146	A12	176	B3
27	J3	57	P5	87	Q14	117	G13	147	B11	177	A2
28	J4	58	N6	88	P14	118	G12	148	C10	178	B2
29	K1	59	Q5	89	M12	119	F15	149	A11	179	D4
30	K2	60	P6	90	L11	120	F14	150	B10	180	E5

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AMI Semiconductors

Packaging Capabilities

Tape Automated Bonding

Tape automated bonding (TAB) is an alternative to conventional plastic or ceramic packages. TAB permits interconnecting higher lead count devices than is possible by wirebonding. TAB also allows more connections for a given die perimeter, since bond pads can be put on a tighter pitch than wirebonding allows. TAB outer leads can also be on a tighter pitch than those of current packages. The combination of tighter inner and outer lead pitches can result in significant board area savings over other package types. In addition, TAB leads have a higher current carrying capacity than wire.

TAB parts have gold bumps plated onto the aluminum bond pads of the device, then the TAB inner leads are bonded to these bumps in a single operation. A conformal silicone elastomer coating is applied to the circuit side of the device. A conformal coating affords environmental protection, while subjecting the device to less stress than a plastic molded package. Inner lead bonded parts will be supplied in a carrier. Customers may then excise the device, form the outer leads and perform board attach. Devices with gold bumps but not bonded are also available for customers wishing to do their own inner lead bonding.

Lead Finish Selection

Gould AMI offers a variety of lead coatings on different package types:

Plastic DIP:	Tin plate
PLCC:	Wave solder (60/40 Sn/Pb)
SOIC:	Tin plate
Ceramic:	Wave solder (60/40 Sn/Pb), Plated (Au-Ni)
QFP:	Solder Plate (85/15 Sn/Pb)

We have been moving our customers toward lead coatings which include Pb to obtain the best solderability possible. This is particularly important on surface mount devices.

Gould AMI has a patented PLCC wave solder process which meets the toughest industry requirements, including total coplanarity of 4 mils.

Our packages must pass the following solderability test: 95% coverage with an RMA flux at 245° C.

Gould AMI Packaging Advantages

Gould AMI is an ASIC company which also produces specialized standard and foundry products. We have evolved over the last 20 years from a full custom to a semicustom company by maintaining close customer relationships and expertise in a wide variety of designs, while developing key semicustom attributes such as faster cycle times, sophisticated design tools, and a wide selection of high quality packages.

Gould AMI's packaging strength is based in a strong Package Development group and a modern, clean assembly plant in the Philippines. In addition to assembly in our own facility, we also assemble packages at subcontractors in U.S., Korea and Taiwan, to give us maximum flexibility on loading, cycle time, and package offering.

We believe that SPC, statistical process control, is the best method for continual improvement in process and material quality. Whether you visit our Fabrication or Assembly facilities in Pocatello, or our Assembly/Test facility in the Philippines, you will see operators, technicians, and engineers using SPC charts in order to provide our customers with consistent product of always improving quality. Every operator and engineer in Pocatello and the Philippines has received training in statistical control methods in Gould AMI's own class, as have many of our suppliers. In addition, we are now teaching statistically valid experimental techniques to our engineers so data we gather in experiments is statistically valid.

In Pocatello, we are developing TAB (tape automated bonding) technology to double the I/O's within the same footprint.

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AMI Semiconductors

Ordering Information

Standard Products

Any product in this MOS Products Catalog can be ordered using the simple system described below. With this system it is possible to completely specify any standard device in this catalog in a manner that is compatible with Gould's order processing methods. The example below shows how this ordering system works and will help you to order your parts in a manner that can be expedited rapidly and accurately.

All orders (except those in sample quantities) are normally shipped in plastic containers, which protect the devices from static electricity damage under all normal handling conditions. Either container is compatible with standard automatic IC handling equipment.

Any device described in this catalog is a Gould Standard Product. However, devices that require mask preparation or programming to the requirements of a particular user, devices that must be tested to other than Gould Quality Assurance standard procedures, or other devices requiring special masks are sold on a negotiated price basis.

S2559	- P
S2559F	- P
S2579	- SOIC
S3507A	- CLCC
S618839	- J
S618840	- PPGA

Device Number—prefix S, followed by numeric digits that define the basic device type. Versions to the basic device are indicated by an additional alpha or numeric digit as shown in the above examples.

Package Type—a letter designation which identifies the basic package type. The letters are coded as follows:

P — Plastic Dip package
D — Cerdip package
C — Ceramic (three-layer) Dip package
J — J-leaded PLCC (Plastic-Leaded Chip Carrier)
PPGA — Plastic Pin Grid Array
CPGA — Ceramic Pin Grid Array
SOIC — Small Outline Integrated Circuit
CLCC — Ceramic Leadless Chip Carrier

GOULD

AMI® Semiconductors

Terms of Sale

1. ACCEPTANCE: THE TERMS OF SALE CONTAINED HEREIN APPLY TO ALL QUOTATIONS MADE AND PURCHASE ORDERS ENTERED INTO BY THE SELLER. SOME OF THE TERMS SET OUT HERE MAY DIFFER FROM THOSE IN BUYER'S PURCHASE ORDER AND SOME MAY BE NEW. THIS ACCEPTANCE IS CONDITIONAL ON BUYER'S ASSENT TO THE TERMS SET OUT HERE IN LIEU OF THOSE IN BUYER'S PURCHASE ORDER. SELLER'S FAILURE TO OBJECT TO PROVISIONS CONTAINED IN ANY COMMUNICATION FROM BUYER SHALL NOT BE DEEMED A WAIVER OF THE PROVISIONS OF THIS ACCEPTANCE. ANY CHANGES IN THE TERMS CONTAINED HEREIN MUST SPECIFICALLY BE AGREED TO IN WRITING BY AN OFFICER OF THE SELLER BEFORE BECOMING BINDING ON EITHER THE SELLER OR THE BUYER. All orders or contracts must be approved and accepted by the Seller at its home office. These terms shall be applicable whether or not they are attached to or enclosed with the products to be sold or sold hereunder. Prices for the items called for hereby are not subject to audit.

2. PAYMENT:

(a) Unless otherwise agreed, all invoices are due and payable thirty (30) days from date of invoice. No discounts are authorized. Shipments, deliveries, and performance of work shall at all times be subject to the approval of the Seller's credit department and the Seller may at any time decline to make any shipments or deliveries or perform any work except upon receipt of payment or upon terms and conditions or security satisfactory to such department.

(b) If, in the judgment of the Seller, the financial condition of the Buyer at any time does not justify continuation of production or shipment on the terms of payment originally specified, the Seller may require full or partial payment in advance and, in the event of the bankruptcy or insolvency of the Buyer or in the event any proceeding is brought by or against the Buyer under the bankruptcy or insolvency laws, the Seller shall be entitled to cancel any order then outstanding and shall receive reimbursement for its cancellation charges.

(c) Each shipment shall be considered a separate and independent transaction, and payment therefore shall be made accordingly. If shipments are delayed by the Buyer, payments shall become due on the date when the Seller is prepared to make shipment. If the work covered by the purchase order is delayed by the Buyer, payments shall be made based on the purchase price and the percentage of completion. Products held for the Buyer shall be at the risk and expense of the Buyer.

3. TAXES: Unless otherwise provided herein, the amount of any present or future sales, revenue, excise or other taxes, fees, or other charges of any nature, imposed by any public authority, (national, state, local or other) applicable to the products covered by this order, or the manufacture or sale thereof, shall be added to the purchase price and shall be paid by the Buyer, or in lieu thereof, the Buyer shall provide the Seller with a tax exemption certificate acceptable to the taxing authority.

4. F.O.B. POINT: All sales are made F.O.B. point of shipment. Seller's title passes to Buyer, and Seller's liability as to delivery ceases upon making delivery of material purchased hereunder to carrier at shipping point, the carrier acting as Buyer's agent. All claims for damages must be filed with the carrier. Shipments will normally be made by Parcel Post, United Parcel Service (UPS), Air Express, or Air Freight. Unless specific instructions from Buyer specify which of the foregoing methods of shipment is to be used, the Seller will exercise his own discretion.

5. DELIVERY: Shipping dates are approximate and are based upon prompt receipt from Buyer of all necessary information. In no event will Seller be liable for any re-procurement costs, nor for delay or non-delivery, due to causes beyond its reasonable control including, but not limited to, acts of God, acts of civil or military authority, priorities, fires, strikes, lockouts, slow-downs, shortages, factory or labor conditions, yield problems, and inability due to causes beyond the Seller's reasonable control to obtain necessary labor, materials, or manufacturing facilities. In the event of any such delay, the date of delivery shall, at the request of the Seller, be deferred for a period equal to the time lost by reason of the delay.

In the event Seller's production is curtailed for any of the above reasons so that Seller cannot deliver the full amount released hereunder, Seller may allocate production deliveries among its various customers then under contract for similar goods. The allocation will be made in a commercially fair and reasonable manner. When allocation has been made, Buyer will be notified of the estimated quota made available.

6. PATENTS: The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents, trademarks, or unfair competition arising from compliance with Buyer's designs, specifications, or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise, under patent claims covering combinations of said products with other devices or elements.

Except as otherwise provided in the preceding paragraph, the Seller shall defend any suit or proceeding brought against the Buyer, so far as based on a claim that any product, or any part thereof, furnished under this contract constitutes an infringement of any patent of the United States, if notified promptly in writing and given authority, information, and assistance (at the Seller's expense) for defense of same, and the Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part thereof, is, in such suit, held to constitute infringement of patent, and the use of said product is enjoined, the Seller shall, at its own expense, either procure for the Buyer the right to continue using said product or part, replace same with non-infringing product, modify it so it becomes non-infringing, or remove said product and refund the purchase price and the transportation and installation costs thereof. In no event shall Seller's total liability to the Buyer under or as a result of compliance with the provisions of this paragraph exceed the aggregate sum paid by the Buyer for the allegedly infringing product. The foregoing states the entire liability of the Seller for patent infringement by the said products or any part thereof. THIS PROVISION IS STATED IN LIEU OF ANY OTHER EXPRESSED, IMPLIED, OR STATUTORY WARRANTY AGAINST INFRINGEMENT AND SHALL BE THE SOLE AND EXCLUSIVE REMEDY FOR PATENT INFRINGEMENT OF ANY KIND.

7. INSPECTION: Unless otherwise specified and agreed upon, the material to be furnished under this order shall be subject to the Seller's standard inspection at the place of manufacture. If it has been agreed upon and specified in this order that Buyer is to inspect or provide for inspection at place of manufacture such inspection shall be so conducted as to not interfere unreasonably with Seller's operations and consequent approval or rejection shall be made before shipment of the material. Notwithstanding the foregoing, if, upon receipt of such material by Buyer, the same shall appear not to conform to the contract, the Buyer shall immediately notify the Seller of such conditions and afford the Seller a reasonable opportunity to inspect the material. No material shall be returned without Seller's consent. Seller's Return Material Authorization form must accompany such returned material.

8. LIMITED WARRANTY: The Seller warrants that the products to be delivered under this purchase order will be free from defects in material and workmanship under normal use and service. Seller's obligations under this Warranty are limited to replacing or repairing or giving credit for, at its option, at its factory, any of said products which shall, within one (1) year after shipment, be returned to the Seller's factory of origin, transportation charges prepaid, and which are, after examination, disclosed to the Seller's satisfaction to be thus defective. THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES EXPRESSED, STATUTORY, OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON THE SELLER'S PART, AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR THE SELLER ANY OTHER LIABILITIES IN CONNECTION WITH THE SALE OF THE SAID ARTICLES. This Warranty shall not apply to any of such products which shall have been repaired or altered, except by the Seller, or which shall have been subjected to misuse, negligence, or accident. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by Seller.

It is understood that if this order calls for the delivery of semiconductor devices which are not finished and fully encapsulated, that no warranty, statutory, expressed or implied, including the implied warranty of merchantability and fitness for a particular purpose, shall apply. All such devices are sold as is where is.

9. PRODUCTS NOT WARRANTED BY SELLER: The second paragraph of Paragraph 6, Patents, and Paragraph 8, Limited Warranty, above apply only to integrated circuits of Seller's own manufacture. IN THE CASE OF PRODUCTS OTHER THAN INTEGRATED CIRCUITS OF SELLER'S OWN MANUFACTURE, SELLER MAKES NO WARRANTIES EXPRESSED, STATUTORY OR IMPLIED INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY, FREEDOM FROM PATENT INFRINGEMENT AND FITNESS FOR A PARTICULAR PURPOSE. Such products may be warranted by the original manufacturer of such products. For further information regarding the possible warranty of such products contact Seller.

10. PRICE ADJUSTMENTS: Seller's unit prices are based on certain material costs. These materials include, among other things, gold packages and silicon. Adjustments shall be as follows:

(a) Gold. The price at the time of shipment shall be adjusted for increases in the cost of gold in accordance with Seller's current Gold Price Adjustment List. This adjustment will be shown as a separate line item on each invoice.

(b) Other Materials. In the event of significant increases in other materials, Seller reserves the right to renegotiate the unit prices. If the parties cannot agree on such increase, then neither party shall have any further obligations with regard to the delivery or purchase of any units not then scheduled for production.

11. VARIATION IN QUANTITY: If this order calls for a product not listed in Seller's current catalog, or for a product which is specially programmed for Buyer, it is agreed that Seller may ship a quantity which is five percent (5%) more or less than the ordered quantity and that such quantity shipped will be accepted and paid for in full satisfaction of each party's obligation hereunder for the quantity order.

12. CONSEQUENTIAL DAMAGES: In no event shall Seller be liable for special, incidental or consequential damages.

13. GENERAL:

(a) The validity, performance and construction of these terms and all sales hereunder shall be governed by the laws of the State of California.

(b) The Seller represents that with respect to the production of articles and/or performance of the services covered by this order it will fully comply with all requirements of the Fair Labor Standards Act of 1938, as amended, Williams-Steiger Occupational Safety and Health Act of 1970, Executive Orders 11375 and 11246, Section 202 and 204.

(c) The Buyer may not unilaterally make changes in the drawings, designs or specifications for the items to be furnished hereunder without Seller's prior consent.

(d) Except to the extent provided in Paragraph 14, below, this order is not subject to cancellation or termination for convenience.

(e) If Buyer is in breach of its obligations under this order, Buyer shall remain liable for all unpaid charges and sums due to Seller and will reimburse Seller for all damages suffered or incurred by Seller as a result of Buyer's breach. The remedies provided herein shall be in addition to all other legal means and remedies available to Seller.

(f) Buyer acknowledges that all or part of the products purchased hereunder may be manufactured and/or assembled at any of Seller's facilities domestic or foreign.

(g) Unless otherwise agreed in a writing signed by both Buyer and Seller, Seller shall retain title to and possession of all tooling of any kind (including but not limited to masks and pattern generator tapes) used in the production of products furnished hereunder.

(h) Buyer, by accepting these products, certifies that he will not export or re-export the products furnished hereunder unless he complies fully with all laws and regulations of the United States relating to such export or re-export, including but not limited to the Export Administration Act of 1979 and the Export Administration Regulations of the U.S. Department of Commerce.

(i) Seller shall own all copyrights in or relating to each product developed by Seller whether or not such product is developed under contract with a third party.

14. GOVERNMENT CONTRACT PROVISIONS: If Buyer's original purchase order indicates by contract number, that it is placed under a government contract, only the following provisions of the current Defense Acquisition Regulations are applicable in accordance with the terms thereof, with an appropriate substitution of parties, as the case may be - i.e., "Contracting Officer" shall mean "Buyer", "Contractor" shall mean "Seller", and the term "Contract" shall mean this order:

7-103.1, Definitions; 7-103.3, Extras; 7-103.4, Variation in Quantity; 7-103.8, Assignment of Claims; 7-103.9, Additional Bond Security; 7-103.13, Renegotiation; 7-103.15, Rhodesia and Certain Communist Areas; 7-103.16, Contract Work Hours and Safety Standards Act - Overtime Compensation; 7-103.17, Walsh-Healey Public Contracts Act; 7-103.18, Equal Opportunity Clause; 7-103.19, Officials Not to Benefit; 7-103.20, Covenant Against Contingent Fees; 7-103.21, Termination for Convenience of the Government (only to the extent that Buyer's contract is terminated for the convenience of the government); 7-103.22, Authorization and Consent; 7-103.23, Notice and Assistance Regarding Patent Infringement; 7-103.24, Responsibility for Inspection; 7-103.25, Commercial Bills of Lading Covering Shipments Under FOB Origin Contracts; 7-103.27, Listing of Employment Openings; 7-104.4, Notice to the Government of Labor Disputes; 7-104.11, Excess Profit; 7-104.15, Examination of Records by Comptroller General; 7-104.20, Utilization of Labor Surplus Area Concerns.

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(714) 547-6466

FP Sales
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Albuquerque, NM 87109
(505) 345-5553

Thom Luke Sales, Inc.
2940 N. 67th Place
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Scottsdale, AZ 95251
(602) 941-1901

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P.O. Box 9327
Seattle, WA 98109
(206) 285-1300

James J. Backer Co.
10550 S.W. Allen Blvd.
Suite 225
Beaverton, OR 97005
(503) 627-0775

James J. Backer Co.
601 Hays, Suite 20
P.O. Box 2188
Boise, ID 83701
(208) 344-9558

Western Region Marketing.
2400 Industrial Lane
Suite 100
Broomfield, CO 80020
(303) 469-8088

Western Region Marketing
344 E. Park Creeke Lane
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(801) 486-1646

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Maryland Heights, MO 63043
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Gould AMI Representatives (continued)

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P.O. Box 68198
Wichita, KS 67208
(316) 683-1070

Ensco-Rep Inc.
5615 West 61st Street
Countryside, KS 66202
(913) 384-0840

Electron Marketing Corp.
3158 Des Plaines Ave.
Suite 109
Des Plaines, IL 60018
(312) 298-2330

COMTEK
6525 City West Parkway
Eden Prarie, MN 55344
(612) 941-7181

Electro Reps Inc.
7240 Shadeland Station
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Indianapolis, IN 46256
(317) 842-7202

Electro Reps Inc.
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Fort Wayne, IN 46818
(219) 489-8205

Electronic Salesmasters Inc.
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(216) 831-9555

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450 North Belt East, #228
Houston, TX 77060
(713) 820-3210

R-Squared Electronics, Inc.
2546 Merrell Road #105
Dallas, TX 75229
(214) 406-1117

Electronic Technical Sales
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JEBCO
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Vitel Electronics
300 March Road
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Kanata, Ontario
Canada K2K 2E2
(613) 592-0090

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ARIZONA, Phoenix
Future Electronics (602) 968-7140

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CALIFORNIA, Chatsworth
Future Electronics (818) 772-6240

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Future Electronics (619) 278-5020

CALIFORNIA, San Jose
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Future Electronics, (403) 235-5325

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Future Electronics (403) 438-2858

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Milgray (913) 236-8800

MARYLAND, Columbia
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Future Electronics (612) 944-2200

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Comprehensive Technical Sales Inc.
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